

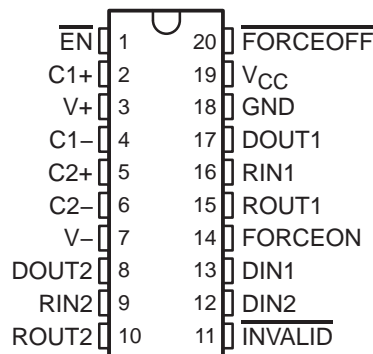
# MAX3223

## 3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH $\pm 15$ -kV ESD PROTECTION

SLLS409K – JANUARY 2000 – REVISED MARCH 2004

- RS-232 Bus-Pin ESD Protection Exceeds  $\pm 15$  kV Using Human-Body Model (HBM)
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates With 3-V to 5.5-V  $V_{CC}$  Supply
- Operates Up To 250 kbit/s
- Two Drivers and Two Receivers
- Low Standby Current . . . 1  $\mu$ A Typical
- External Capacitors . . .  $4 \times 0.1 \mu$ F
- Accepts 5-V Logic Input With 3.3-V Supply
- Alternative High-Speed Pin-Compatible Device (1 Mbit/s)
  - SNx5C3223
- Applications
  - Battery-Powered Systems, PDAs, Notebooks, Laptops, Palmtop PCs, and Hand-Held Equipment

DB, DW, OR PW PACKAGE  
(TOP VIEW)



### description/ordering information

The MAX3223 consists of two line drivers, two line receivers, and a dual charge-pump circuit with  $\pm 15$ -kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The device operates at data signaling rates up to 250 kbit/s and a maximum of 30-V/ $\mu$ s driver output slew rate.

### ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–0°C to 70°C	SOIC (DW)	Tube of 25	MAX3223CDW	MAX3223C
		Reel of 2000	MAX3223CDWR	
	SSOP (DB)	Tube of 70	MAX3223CDB	MA3223C
		Reel of 2000	MAX3223CDBR	
	TSSOP (PW)	Tube of 70	MAX3223CPW	MA3223C
		Reel of 2000	MAX3223CPWR	
–40°C to 85°C	SOIC (DW)	Tube of 25	MAX3223IDW	MAX3223I
		Reel of 2000	MAX3223IDWR	
	SSOP (DB)	Tube of 70	MAX3223IDB	MB3223I
		Reel of 2000	MAX3223IDBR	
	TSSOP (PW)	Tube of 70	MAX3223IPW	MB3223I
		Reel of 2000	MAX3223IPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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 **TEXAS  
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**description/ordering information (continued)**

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and  $\overline{\text{FORCEOFF}}$  is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If  $\overline{\text{FORCEOFF}}$  is set low and  $\overline{\text{EN}}$  is high, both drivers and receivers are shut off, and the supply current is reduced to 1  $\mu\text{A}$ . Disconnecting the serial port or turning off the peripheral drivers causes auto-powerdown to occur. Auto-powerdown can be disabled when FORCEON and  $\overline{\text{FORCEOFF}}$  are high. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The  $\overline{\text{INVALID}}$  output is used to notify the user if an RS-232 signal is present at any receiver input.  $\overline{\text{INVALID}}$  is high (valid data) if any receiver input voltage is greater than 2.7 V or less than  $-2.7$  V, or has been between  $-0.3$  V and 0.3 V for less than 30  $\mu\text{s}$ .  $\overline{\text{INVALID}}$  is low (invalid data) if the receiver input voltage is between  $-0.3$  V and 0.3 V for more than 30  $\mu\text{s}$ . Refer to Figure 4 for receiver input levels.

**Function Tables****EACH DRIVER**

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

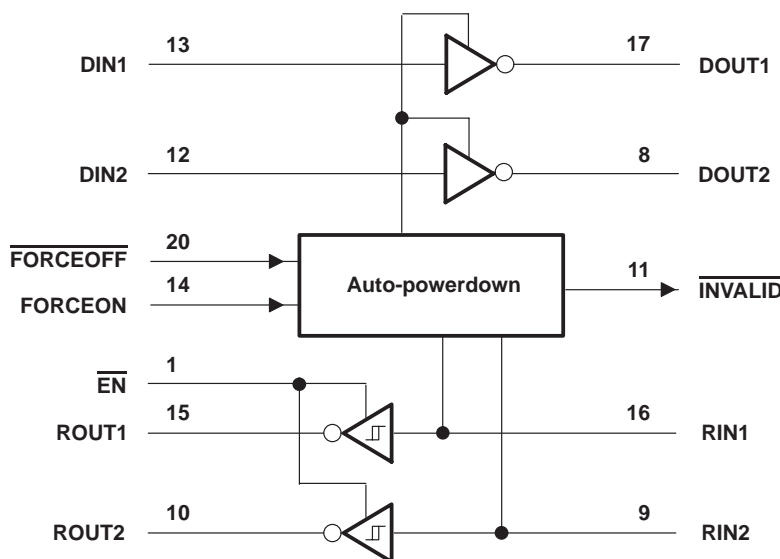
H = high level, L = low level, X = irrelevant, Z = high impedance

**EACH RECEIVER**

INPUTS			OUTPUT ROUT
RIN	$\overline{\text{EN}}$	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

H = high level, L = low level, X = irrelevant,  
Z = high impedance (off), Open = input  
disconnected or connected driver off

**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CC}$ (see Note 1)	–0.3 V to 6 V
Positive output supply voltage range, $V+$ (see Note 1)	–0.3 V to 7 V
Negative output supply voltage range, $V-$ (see Note 1)	0.3 V to –7 V
Supply voltage difference, $V+ - V-$ (see Note 1)	13 V
Input voltage range, $V_I$ : Driver, FORCEOFF, FORCEON, EN	–0.3 V to 6 V
Receiver	–25 V to 25 V
Output voltage range, $V_O$ : Driver	–13.2 V to 13.2 V
Receiver, INVALID	–0.3 V to $V_{CC} + 0.3$ V
Package thermal impedance, $\theta_{JA}$ (see Notes 2 and 3): DB package	70°C/W
DW package	58°C/W
PW package	83°C/W
Operating virtual junction temperature, $T_J$	150°C
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.

2. Maximum power dissipation is a function of  $T_J(\max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.

3. The package thermal impedance is calculated in accordance with JESD 51-7.

**MAX3223****3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER****WITH  $\pm 15$ -kV ESD PROTECTION**

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**recommended operating conditions (see Note 4 and Figure 6)**

			MIN	NOM	MAX	UNIT	
Supply voltage			V <sub>CC</sub> = 3.3 V	3	3.3	3.6	V
			V <sub>CC</sub> = 5 V	4.5	5	5.5	
V <sub>IH</sub>	Driver and control high-level input voltage	DIN, $\overline{\text{EN}}$ , $\overline{\text{FORCEOFF}}$ , FORCEON	V <sub>CC</sub> = 3.3 V	2		V	
			V <sub>CC</sub> = 5 V	2.4			
V <sub>IL</sub>	Driver and control low-level input voltage	DIN, $\overline{\text{EN}}$ , $\overline{\text{FORCEOFF}}$ , FORCEON			0.8	V	
V <sub>I</sub>	Driver and control input voltage	DIN, $\overline{\text{EN}}$ , $\overline{\text{FORCEOFF}}$ , FORCEON			0	V	
	Receiver input voltage			−25	25		
T <sub>A</sub>	Operating free-air temperature		MAX3223C	0	70	°C	
			MAX3223I	−40	85		

NOTE 4: Test conditions are C1–C4 = 0.1  $\mu\text{F}$  at  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ; C1 = 0.047  $\mu\text{F}$ , C2–C4 = 0.33  $\mu\text{F}$  at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$I_I$	Input leakage current	$\overline{EN}, \overline{FORCEOFF}, \overline{FORCEON}$			$\pm 0.01$	$\pm 1$	$\mu\text{A}$
$I_{CC}$	Supply current	Auto-powerdown disabled	No load, $\overline{FORCEOFF}$ and $\overline{FORCEON}$ at $V_{CC}$		0.3	1	mA
		Powered off	$V_{CC} = 3.3\text{ V or } 5\text{ V}, T_A = 25^\circ\text{C}$ No load, $\overline{FORCEOFF}$ at GND		1	10	$\mu\text{A}$
		Auto-powerdown enabled	No load, $\overline{FORCEOFF}$ at $V_{CC}$ , $\overline{FORCEON}$ at GND, All RIN are open or grounded		1	10	

† All typical values are at  $V_{CC} = 3.3\text{ V}$  or  $V_{CC} = 5\text{ V}$ , and  $T_A = 25^\circ\text{C}$ .NOTE 4: Test conditions are C1–C4 = 0.1  $\mu\text{F}$  at  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ; C1 = 0.047  $\mu\text{F}$ , C2–C4 = 0.33  $\mu\text{F}$  at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .

## DRIVER SECTION

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)**

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{OH}$ High-level output voltage	DOOUT at $R_L = 3\text{ k}\Omega$ to GND	5	5.4		V
$V_{OL}$ Low-level output voltage	DOOUT at $R_L = 3\text{ k}\Omega$ to GND	–5	–5.4		V
$I_{IH}$ High-level input current	$V_I = V_{CC}$		$\pm 0.01$	$\pm 1$	$\mu\text{A}$
$I_{IL}$ Low-level input current	$V_I$ at GND		$\pm 0.01$	$\pm 1$	$\mu\text{A}$
$I_{OS}$ Short-circuit output current‡	$V_{CC} = 3.6\text{ V}$ , $V_O = 0\text{ V}$		$\pm 35$	$\pm 60$	mA
	$V_{CC} = 5.5\text{ V}$ , $V_O = 0\text{ V}$		$\pm 35$	$\pm 60$	
$r_o$ Output resistance	$V_{CC}$ , $V_+$ , and $V_- = 0\text{ V}$ , $V_O = \pm 2\text{ V}$	300	10M		$\Omega$
$I_{off}$ Output leakage current	$\overline{\text{FORCEOFF}} = \text{GND}$ , $V_O = \pm 12\text{ V}$ , $V_{CC} = 3\text{ V to } 3.6\text{ V}$			$\pm 25$	$\mu\text{A}$
	$\overline{\text{FORCEOFF}} = \text{GND}$ , $V_O = \pm 10\text{ V}$ , $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$			$\pm 25$	

† All typical values are at  $V_{CC} = 3.3\text{ V}$  or  $V_{CC} = 5\text{ V}$ , and  $T_A = 25^\circ\text{C}$ .

‡ Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

NOTE 4: Test conditions are C1–C4 = 0.1  $\mu\text{F}$  at  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ; C1 = 0.047  $\mu\text{F}$ , C2–C4 = 0.33  $\mu\text{F}$  at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Maximum data rate		C <sub>L</sub> = 1000 pF, One DOUT switching,		R <sub>L</sub> = 3 kΩ, See Figure 1		250	kbit/s
t <sub>sk(p)</sub>	Pulse skew§	C <sub>L</sub> = 150 pF to 2500 pF, See Figure 2		R <sub>L</sub> = 3 kΩ to 7 kΩ,		100	ns
SR(tr)	Slew rate, transition region (See Figure 1)	V <sub>CC</sub> = 3.3 V, R <sub>L</sub> = 3 kΩ to 7 kΩ	C <sub>L</sub> = 150 pF to 1000 pF		6	30	V/μs
			C <sub>L</sub> = 150 pF to 2500 pF		4	30	

† All typical values are at  $V_{CC} = 3.3\text{ V}$  or  $V_{CC} = 5\text{ V}$ , and  $T_A = 25^\circ\text{C}$ .

§ Pulse skew is defined as  $|t_{pLH} - t_{pHL}|$  of each channel of the same device.

NOTE 4: Test conditions are C1–C4 = 0.1  $\mu\text{F}$  at  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ; C1 = 0.047  $\mu\text{F}$ , C2–C4 = 0.33  $\mu\text{F}$  at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .

## RECEIVER SECTION

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)**

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{OH}$ High-level output voltage	$I_{OH} = -1 \text{ mA}$	$V_{CC}-0.6$	$V_{CC}-0.1$		V
$V_{OL}$ Low-level output voltage	$I_{OL} = 1.6 \text{ mA}$			0.4	V
$V_{IT+}$ Positive-going input threshold voltage	$V_{CC} = 3.3 \text{ V}$		1.6	2.4	V
	$V_{CC} = 5 \text{ V}$		1.9	2.4	
$V_{IT-}$ Negative-going input threshold voltage	$V_{CC} = 3.3 \text{ V}$	0.6	1.1		V
	$V_{CC} = 5 \text{ V}$	0.8	1.4		
$V_{hys}$ Input hysteresis ( $V_{IT+} - V_{IT-}$ )			0.5		V
$I_{off}$ Output leakage current	$\overline{EN} = V_{CC}$		$\pm 0.05$	$\pm 10$	$\mu\text{A}$
$r_i$ Input resistance	$V_I = \pm 3 \text{ V to } \pm 25 \text{ V}$	3	5	7	$k\Omega$

† All typical values are at  $V_{CC} = 3.3 \text{ V}$  or  $V_{CC} = 5 \text{ V}$ , and  $T_A = 25^\circ\text{C}$ .

NOTE 4: Test conditions are  $C_1$ – $C_4 = 0.1 \mu\text{F}$  at  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ;  $C_1 = 0.047 \mu\text{F}$ ,  $C_2$ – $C_4 = 0.33 \mu\text{F}$  at  $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ .

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4)**

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{PLH}$ Propagation delay time, low- to high-level output	$C_L = 150 \text{ pF}$ , See Figure 3		150		ns
$t_{PHL}$ Propagation delay time, high- to low-level output	$C_L = 150 \text{ pF}$ , See Figure 3		150		ns
$t_{en}$ Output enable time	$C_L = 150 \text{ pF}$ , See Figure 4 $R_L = 3 \text{ k}\Omega$		200		ns
$t_{dis}$ Output disable time	$C_L = 150 \text{ pF}$ , See Figure 4 $R_L = 3 \text{ k}\Omega$		200		ns
$t_{sk(p)}$ Pulse skew‡	See Figure 3		50		ns

† All typical values are at  $V_{CC} = 3.3 \text{ V}$  or  $V_{CC} = 5 \text{ V}$ , and  $T_A = 25^\circ\text{C}$ .

‡ Pulse skew is defined as  $|t_{PLH} - t_{PHL}|$  of each channel of the same device.

NOTE 4: Test conditions are  $C_1$ – $C_4 = 0.1 \mu\text{F}$  at  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ;  $C_1 = 0.047 \mu\text{F}$ ,  $C_2$ – $C_4 = 0.33 \mu\text{F}$  at  $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ .

## AUTO-POWERDOWN SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

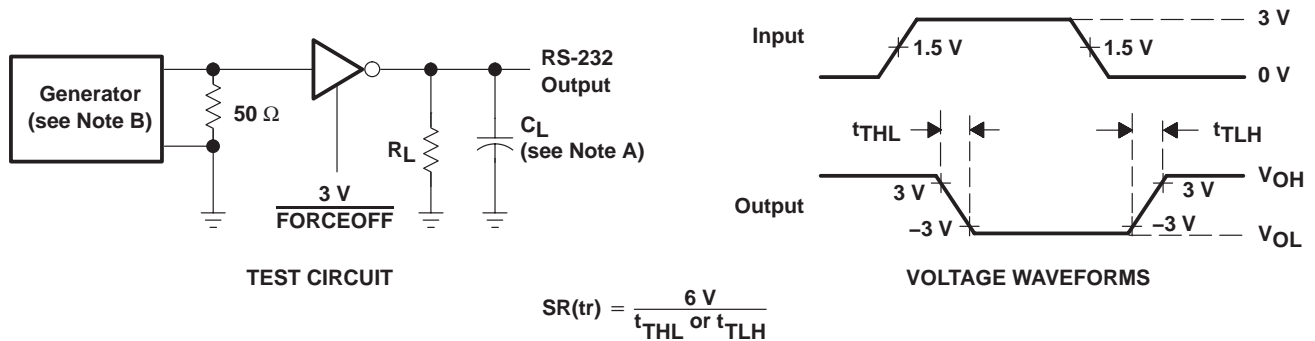
PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$V_{T+}(\text{valid})$ Receiver input threshold for <u>INVALID</u> high-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$		2.7	V
$V_{T-}(\text{valid})$ Receiver input threshold for <u>INVALID</u> high-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$	-2.7		V
$V_{T}(\text{invalid})$ Receiver input threshold for <u>INVALID</u> low-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$	-0.3	0.3	V
$V_{OH}$ <u>INVALID</u> high-level output voltage	$I_{OH} = -1 \text{ mA}$ , $\overline{\text{FORCEOFF}} = V_{CC}$ FORCEON = GND,	$V_{CC} - 0.6$		V
$V_{OL}$ <u>INVALID</u> low-level output voltage	$I_{OL} = 1.6 \text{ mA}$ , $\overline{\text{FORCEOFF}} = V_{CC}$ FORCEON = GND,		0.4	V

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

PARAMETER	TYP†	UNIT
$t_{\text{valid}}$ Propagation delay time, low- to high-level output	1	$\mu\text{s}$
$t_{\text{invalid}}$ Propagation delay time, high- to low-level output	30	$\mu\text{s}$
$t_{\text{en}}$ Supply enable time	100	$\mu\text{s}$

† All typical values are at  $V_{CC} = 3.3 \text{ V}$  or  $V_{CC} = 5 \text{ V}$ , and  $T_A = 25^\circ\text{C}$ .

## PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .

**Figure 1. Driver Slew Rate**

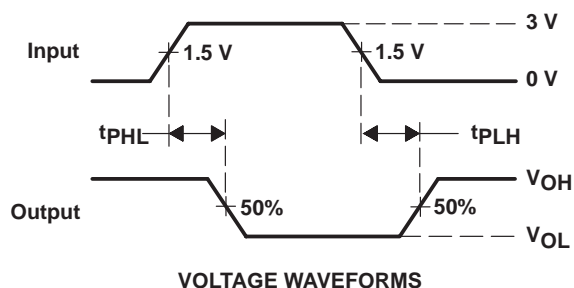
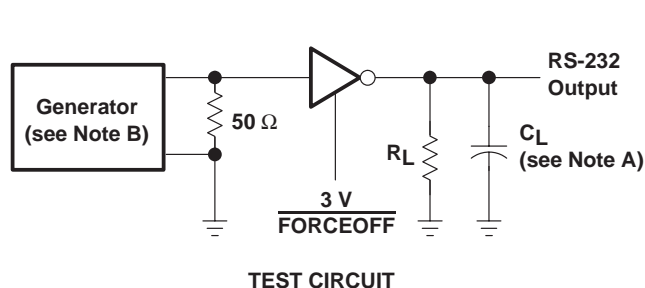
# MAX3223

## 3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER

### WITH $\pm 15$ -kV ESD PROTECTION

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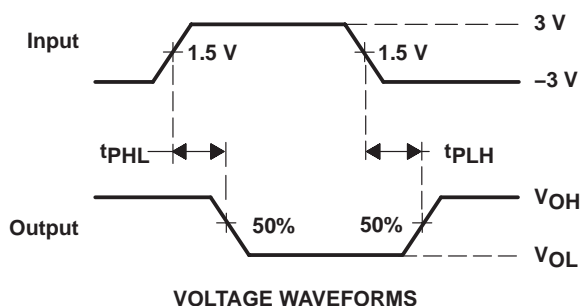
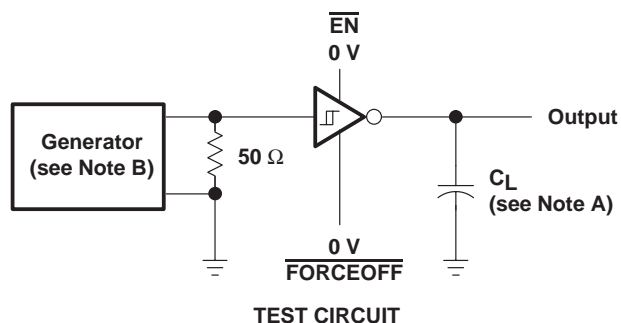
#### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.

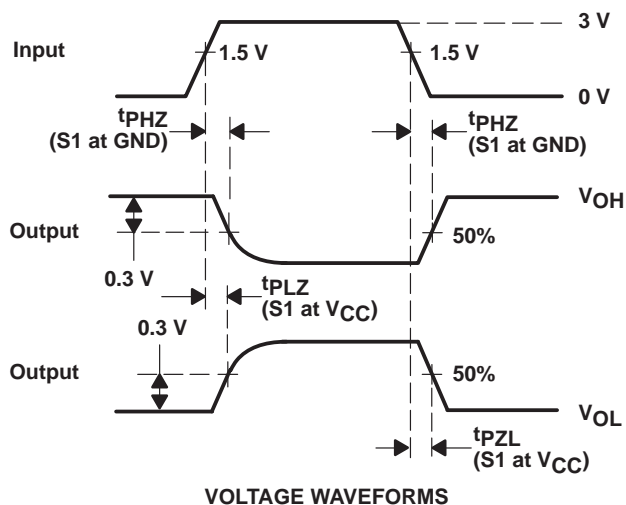
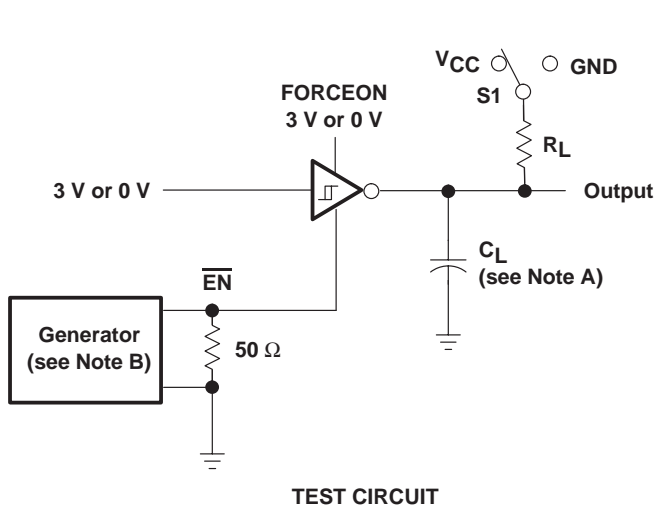
Figure 2. Driver Pulse Skew



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.

Figure 3. Receiver Propagation Delay Times



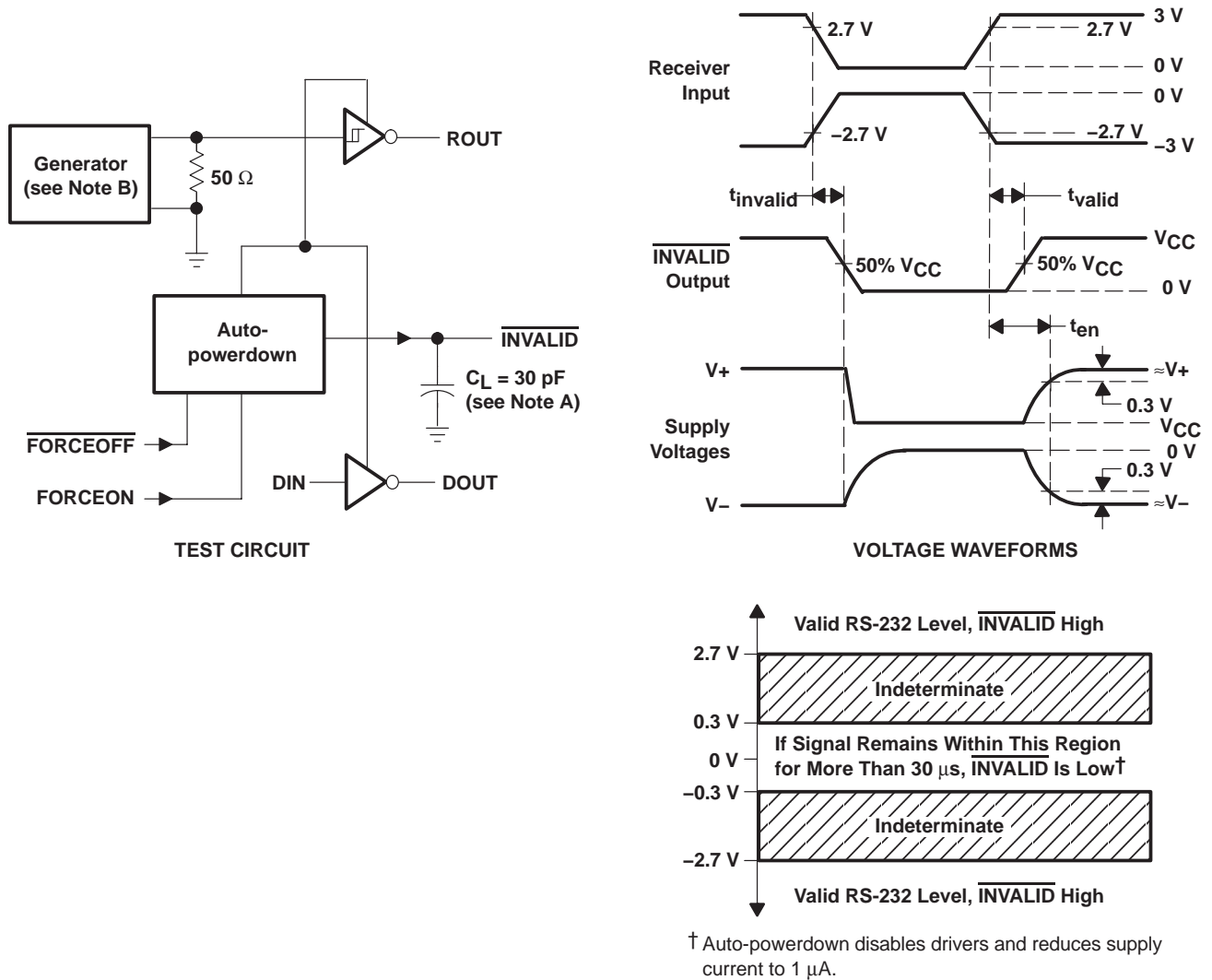
NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.

Figure 4. Receiver Enable and Disable Times



## PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 5 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.

**Figure 5.  $\overline{INVALID}$  Propagation Delay Times and Supply Enabling Time**

## SLLS409K – JANUARY 2000 – REVISED MARCH 2004

The schematic diagram illustrates the internal structure of the AD7524 8-bit DAC. The chip is divided into two main functional blocks by a vertical line. The left block contains the input and output logic, while the right block contains the core DAC circuitry and control logic.

**Pin Connections and Signals:**

- Pin 1:**  $\overline{\text{EN}}$  (Active Low Enable)
- Pin 2:**  $\text{C1}+$  (Capacitor C1 positive terminal)
- Pin 3:**  $\text{V}+$  (Positive supply voltage)
- Pin 4:**  $\text{C1}-$  (Capacitor C1 negative terminal)
- Pin 5:**  $\text{C2}+$  (Capacitor C2 positive terminal)
- Pin 6:**  $\text{C2}-$  (Capacitor C2 negative terminal)
- Pin 7:**  $\text{V}-$  (Negative supply voltage)
- Pin 8:**  $\text{DOUT2}$  (Digital Output 2)
- Pin 9:**  $\text{RIN2}$  (Resistor Input 2)
- Pin 10:**  $\text{ROUT2}$  (Resistor Output 2)
- Pin 11:**  $\overline{\text{INVALID}}$  (Active Low Invalid Signal)
- Pin 12:**  $\text{DIN2}$  (Digital Input 2)
- Pin 13:**  $\text{DIN1}$  (Digital Input 1)
- Pin 14:**  $\text{FORCEON}$  (Force On Signal)
- Pin 15:**  $\text{ROUT1}$  (Resistor Output 1)
- Pin 16:**  $\text{RIN1}$  (Resistor Input 1)
- Pin 17:**  $\text{DOUT1}$  (Digital Output 1)
- Pin 18:**  $\text{C}_{\text{BYPASS}} = 0.1 \mu\text{F}$  (Bypass Capacitor)
- Pin 19:**  $\text{V}_{\text{CC}}$  (Positive supply voltage)
- Pin 20:**  $\overline{\text{FORCEOFF}}$  (Active Low Force Off Signal)

**Internal Components and Connections:**

- Auto-powerdown:** A block that controls the power-down mode of the DAC.
- Capacitors:**  $\text{C1}$ ,  $\text{C2}$ ,  $\text{C3}$ , and  $\text{C4}$  are connected to the input and output lines.
- Resistors:** Two  $5 \text{ k}\Omega$  resistors are connected to the output lines  $\text{ROUT1}$  and  $\text{ROUT2}$ .
- Logic:** The circuit includes several logic gates (AND, OR, NOT) and a multiplexer to process the digital inputs and outputs.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V <sub>CC</sub>	C1	C2, C3, C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

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## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX3223CDB	ACTIVE	SSOP	DB	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3223C	<a href="#">Samples</a>
MAX3223CDBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3223C	<a href="#">Samples</a>
MAX3223CDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3223C	<a href="#">Samples</a>
MAX3223CDWG4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3223C	<a href="#">Samples</a>
MAX3223CDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3223C	<a href="#">Samples</a>
MAX3223CPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3223C	<a href="#">Samples</a>
MAX3223CPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3223C	<a href="#">Samples</a>
MAX3223IDB	ACTIVE	SSOP	DB	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3223I	<a href="#">Samples</a>
MAX3223IDBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3223I	<a href="#">Samples</a>
MAX3223IDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3223I	<a href="#">Samples</a>
MAX3223IDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3223I	<a href="#">Samples</a>
MAX3223IPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3223I	<a href="#">Samples</a>
MAX3223IPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3223I	<a href="#">Samples</a>
MAX3223IPWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3223I	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF MAX3223 :**

- Enhanced Product : [MAX3223-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3223CDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
MAX3223CDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MAX3223CPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
MAX3223IDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
MAX3223IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MAX3223IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

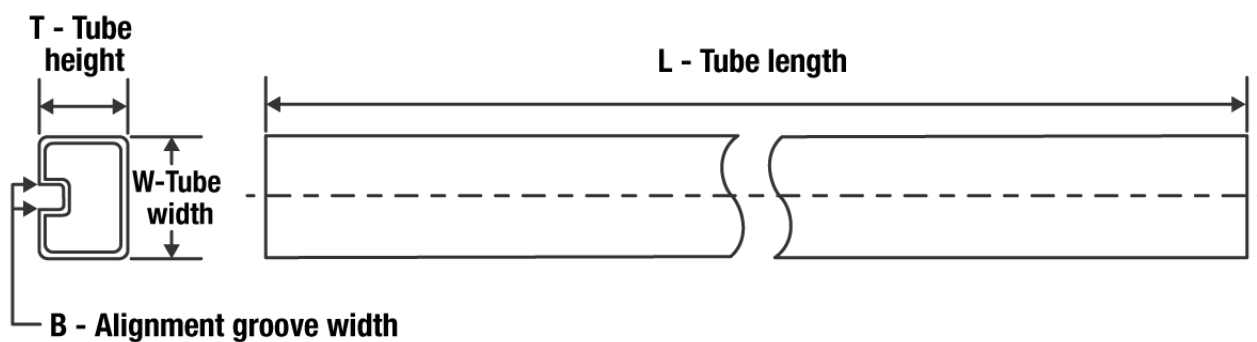
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

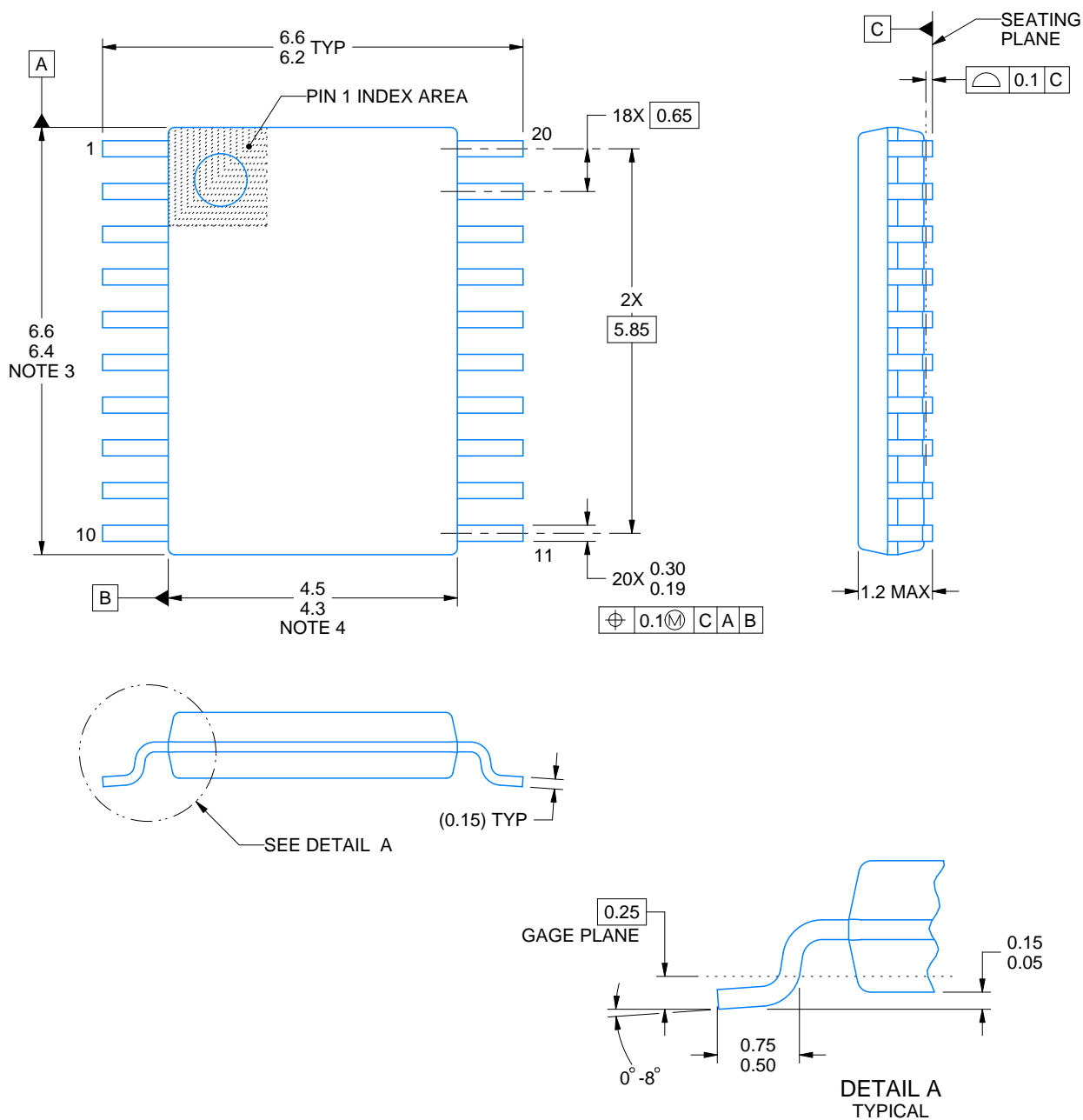
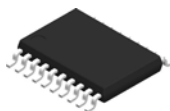
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3223CDBR	SSOP	DB	20	2000	853.0	449.0	35.0
MAX3223CDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MAX3223CPWR	TSSOP	PW	20	2000	853.0	449.0	35.0
MAX3223IDBR	SSOP	DB	20	2000	853.0	449.0	35.0
MAX3223IDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MAX3223IPWR	TSSOP	PW	20	2000	853.0	449.0	35.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
MAX3223CDB	DB	SSOP	20	70	530	10.5	4000	4.1
MAX3223CDW	DW	SOIC	20	25	507	12.83	5080	6.6
MAX3223CDWG4	DW	SOIC	20	25	507	12.83	5080	6.6
MAX3223CPW	PW	TSSOP	20	70	530	10.2	3600	3.5
MAX3223IDB	DB	SSOP	20	70	530	10.5	4000	4.1
MAX3223IDW	DW	SOIC	20	25	507	12.83	5080	6.6
MAX3223IPW	PW	TSSOP	20	70	530	10.2	3600	3.5



4220206/A 02/2017

## NOTES:

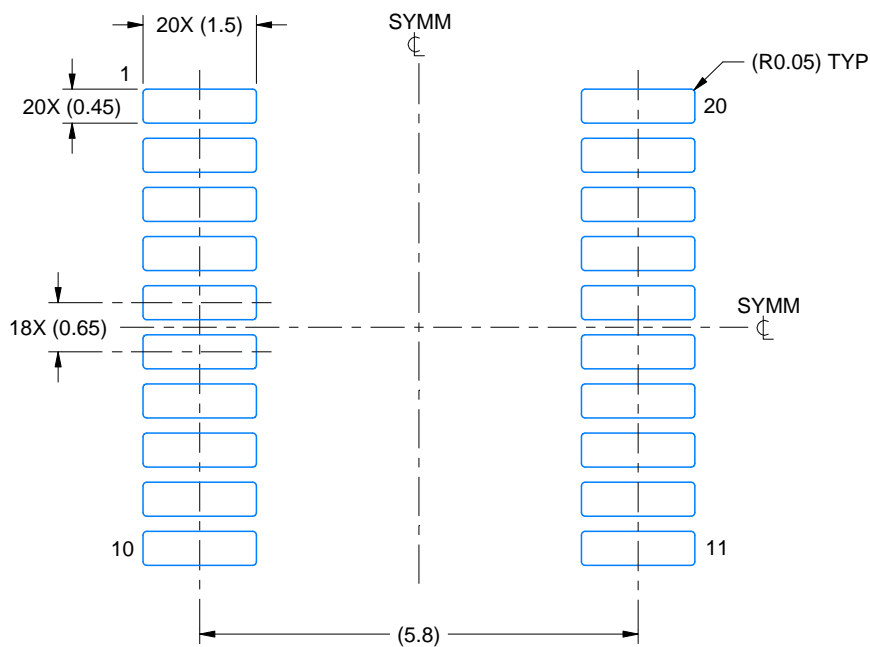
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



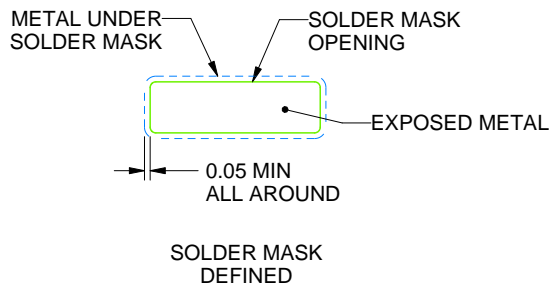
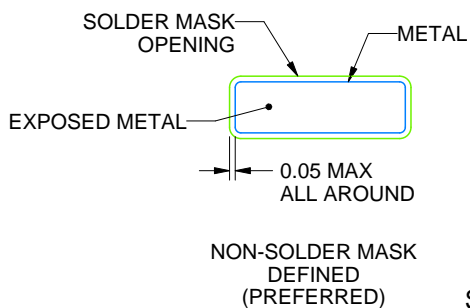
**PW0020A**

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



## SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

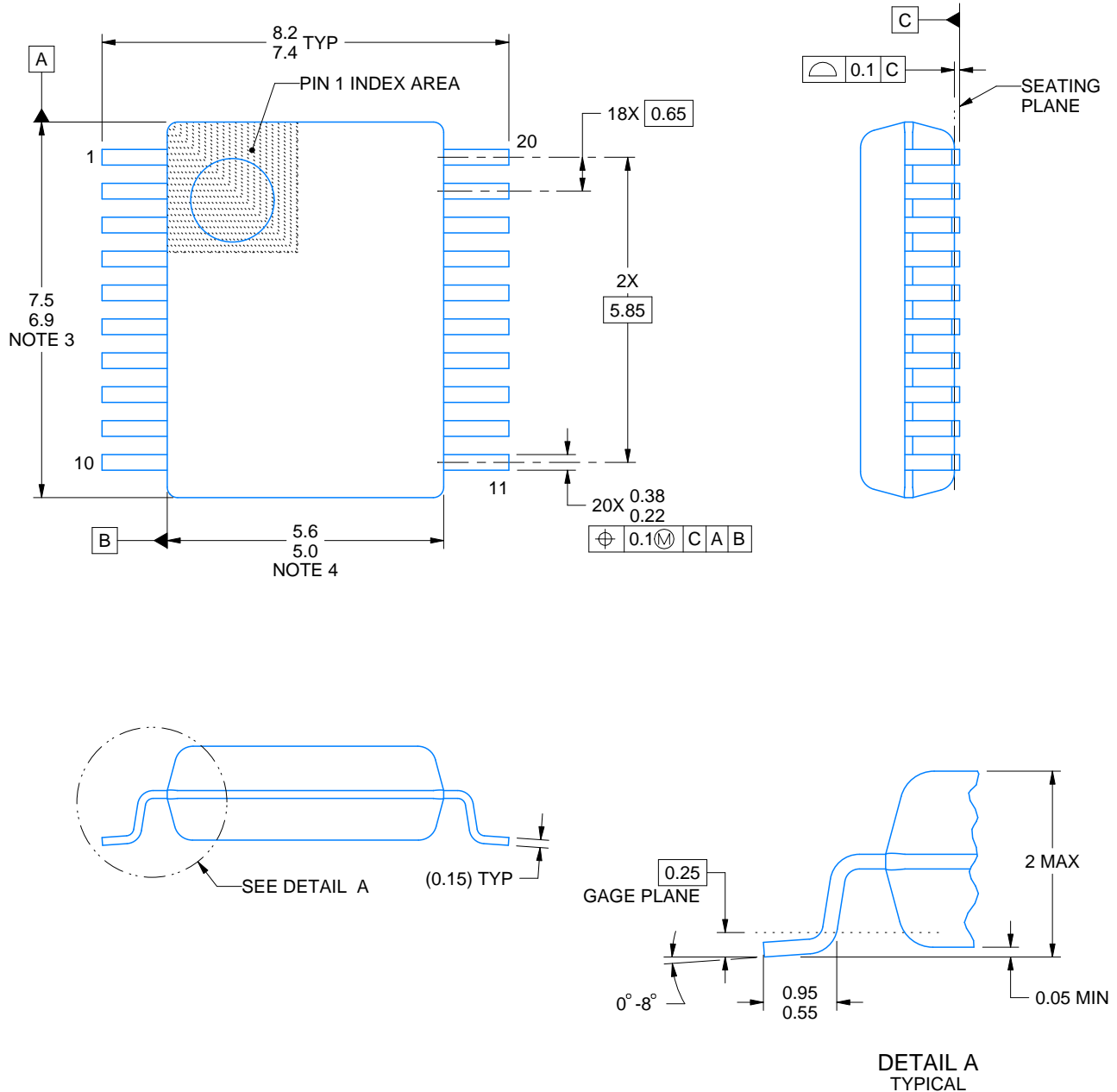
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4214851/B 08/2019

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

**DW0020A**

## PACKAGE OUTLINE

**SOIC - 2.65 mm max height**

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

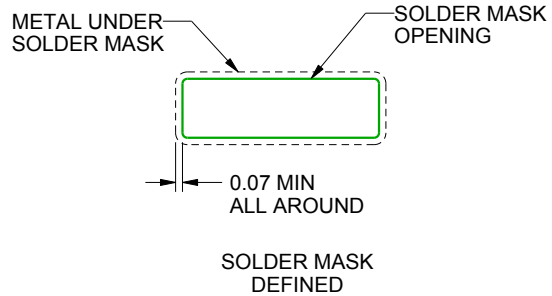
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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