

# SN54ALS374A, SN54AS374, SN74ALS374A, SN74AS374 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS167C – APRIL 1982 – REVISED NOVEMBER 1999

- D-Type Flip-Flops in a Single Package With 3-State Bus Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

## description

These octal D-type edge-triggered flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

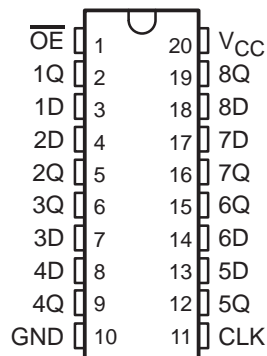
On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

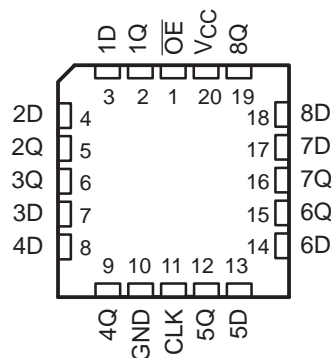
$\overline{OE}$  does not affect internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS374A and SN54AS374 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS374A and SN74AS374 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS374A, SN54AS374 . . . J PACKAGE  
SN74ALS374A, SN74AS374 . . . DW OR N PACKAGE  
(TOP VIEW)



SN54ALS374A, SN54AS374 . . . FK PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	H or L	X	$Q_0$
H	X	X	Z



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1999, Texas Instruments Incorporated  
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

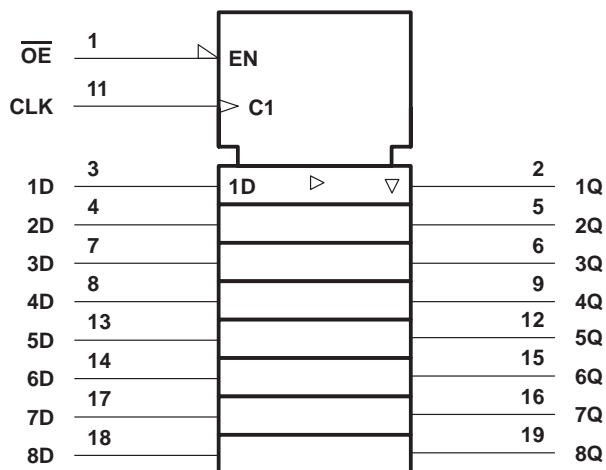
# SN54ALS374A, SN54AS374, SN74ALS374A, SN74AS374

## OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

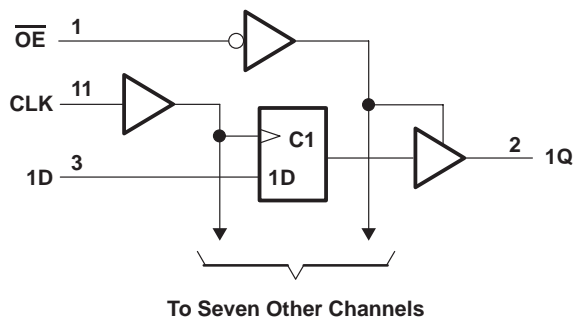
### WITH 3-STATE OUTPUTS

SDAS167C – APRIL 1982 – REVISED NOVEMBER 1999

#### logic symbol†



#### logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ .....	-0.5 V to 7 V
Voltage applied to a disabled 3-state output .....	-0.5 V to 5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 1): DW package .....	58°C/W
N package .....	69°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

#### recommended operating conditions

	SN54ALS374A			SN74ALS374A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.7			0.8	V
$I_{OH}$ High-level output current			-1			-2.6	mA
$I_{OL}$ Low-level output current			12			24	mA
$T_A$ Operating free-air temperature	-55		125	0		70	°C



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54ALS374A, SN54AS374, SN74ALS374A, SN74AS374 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS167C – APRIL 1982 – REVISED NOVEMBER 1999

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		SN54ALS374A			SN74ALS374A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$		-1.5			-1.5			V
$V_{OH}$	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $I_{OH} = -0.4\text{ mA}$		$V_{CC}-2$			$V_{CC}-2$			V
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -1\text{ mA}$	2.4	3.3					
		$I_{OH} = -2.6\text{ mA}$				2.4	3.2		
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 12\text{ mA}$	0.25 0.4		0.25 0.4				V
		$I_{OL} = 24\text{ mA}$				0.35	0.5		
$I_{OZH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.7\text{ V}$	20			20			$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0.4\text{ V}$	-20			-20			$\mu\text{A}$
$I_I$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 7\text{ V}$	0.1			0.1			mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$	20			20			$\mu\text{A}$
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.4\text{ V}$	-0.2			-0.2			mA
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.25\text{ V}$	-20	-112		-30	-112		mA
$I_{CC}$	$V_{CC} = 5.5\text{ V}$	Outputs high	11	20	11	19			mA
		Outputs low	19	28	19	28			
		Outputs disabled	20	31	20	31			

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

**timing requirements over recommended operating free-air temperature range (unless otherwise noted)**

		SN54ALS374A		SN74ALS374A		UNIT
		MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	30		35		MHz
$t_w$	Pulse duration	16.5		14		ns
$t_{su}$	Setup time	10		10		ns
$t_h$	Hold time	4		0		ns

**switching characteristics over recommended operating conditions (unless otherwise noted (see Figure 3))**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALS374A		SN74ALS374A		UNIT
			MIN	MAX	MIN	MAX	
$f_{\text{max}}$			30		35		MHz
$t_{PLH}$	CLK	Q	3	14	3	12	ns
$t_{PHL}$			5	17	5	16	
$t_{PZH}$	$\overline{OE}$	Q	3	18	3	17	ns
$t_{PZL}$			5	21	5	18	
$t_{PHZ}$	$\overline{OE}$	Q	1	11	1	10	ns
$t_{PLZ}$			2	19	2	18	



# SN54ALS374A, SN54AS374, SN74ALS374A, SN74AS374

## OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

### WITH 3-STATE OUTPUTS

SDAS167C – APRIL 1982 – REVISED NOVEMBER 1999

#### recommended operating conditions

		SN54AS374			SN74AS374			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage	0.7			0.8			V
$I_{OH}$	High-level output current	-12			-15			mA
$I_{OL}$	Low-level output current	32			48			mA
$T_A$	Operating free-air temperature	-55			125			°C

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS374			SN74AS374			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$	-1.2			-1.2			V
$V_{OH}$	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ , $I_{OH} = -2\text{ mA}$	$V_{CC}-2$			$V_{CC}-2$			V
	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -12\text{ mA}$	2.4	3.2					
	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -15\text{ mA}$				2.4	3.3		
$V_{OL}$	$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 32\text{ mA}$	0.29			0.5			V
	$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 48\text{ mA}$				0.34	0.5		
$I_{OZH}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.7\text{ V}$	50			50			$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 0.4\text{ V}$	-50			-50			$\mu\text{A}$
$I_I$	$V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$	0.1			0.1			mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$	20			20			$\mu\text{A}$
$I_{IL}$	$\overline{\text{OE}}$ , CLK	-0.5			-0.5			mA
	Data	-3			-2			
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$	-30		-112	-30		-112	mA
$I_{CC}$	$V_{CC} = 5.5\text{ V}$	Outputs high		77	120	77	120	mA
		Outputs low		84	128	84	128	
		Outputs disabled		84	128	84	128	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

#### timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		SN54AS374		SN74AS374		UNIT
		MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	100*		125		MHz
$t_w$	Pulse duration	CLK high		5.5*	4	ns
		CLK low		3*	3	
$t_{su}$	Setup time	Data before CLK $\uparrow$		3*	2	ns
$t_h$	Hold time	Data after CLK $\uparrow$		3*	2	ns

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.



**SN54ALS374A, SN54AS374, SN74ALS374A, SN74AS374**  
**OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS**  
**WITH 3-STATE OUTPUTS**

SDAS167C – APRIL 1982 – REVISED NOVEMBER 1999

**switching characteristics over recommended operating conditions (unless otherwise noted)**  
**(see Figure 3)**

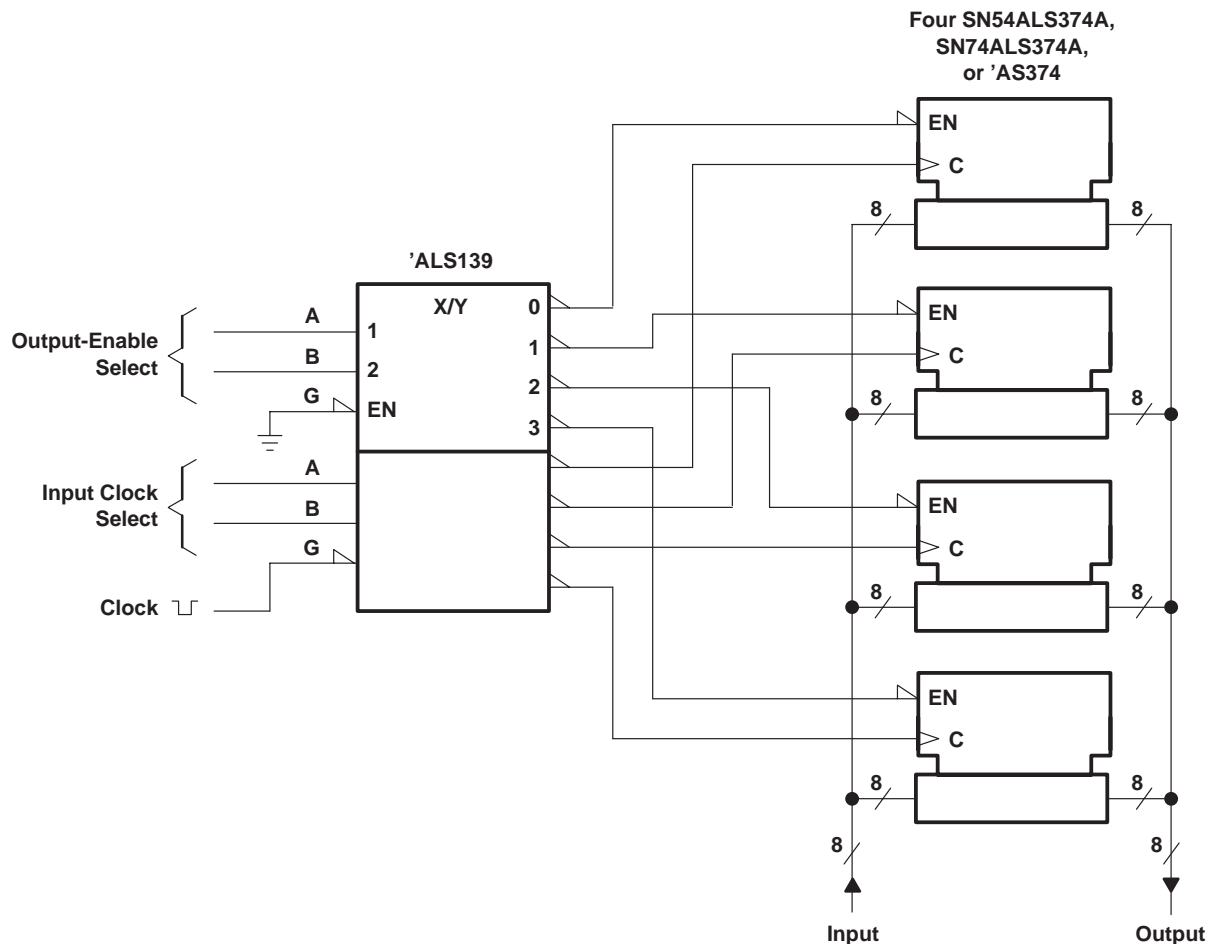
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54AS374		SN74AS374		UNIT
			MIN	MAX	MIN	MAX	
$f_{max}$			100*		125		MHz
$t_{PLH}$	CLK	Q	3	11	3	8	ns
$t_{PHL}$			4	11.5	4	9	
$t_{PZH}$	$\overline{OE}$	Q	2	7	2	6	ns
$t_{PZL}$			3	11	3	10	
$t_{PHZ}$	$\overline{OE}$	Q	2	10	2	6	ns
$t_{PLZ}$			2	7	2	6	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**SN54ALS374A, SN54AS374, SN74ALS374A, SN74AS374**  
**OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS**  
**WITH 3-STATE OUTPUTS**

SDAS167C – APRIL 1982 – REVISED NOVEMBER 1999

**APPLICATION INFORMATION**



**Figure 1. Expandable 4-Word by 8-Bit General File Register**

SN54ALS374A, SN54AS374, SN74ALS374A, SN74AS374  
 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS  
 WITH 3-STATE OUTPUTS

SDAS167C – APRIL 1982 – REVISED NOVEMBER 1999

APPLICATION INFORMATION

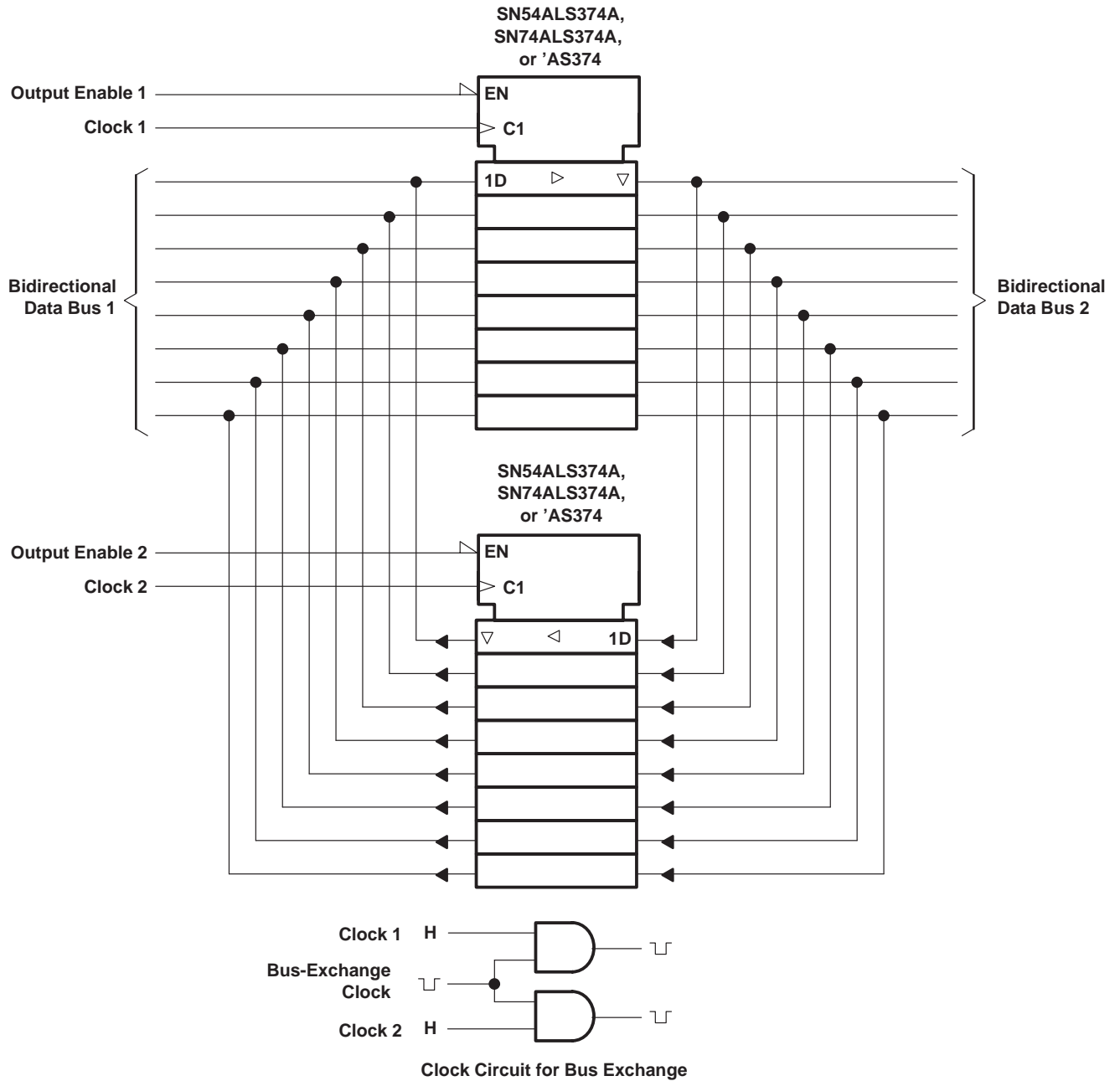
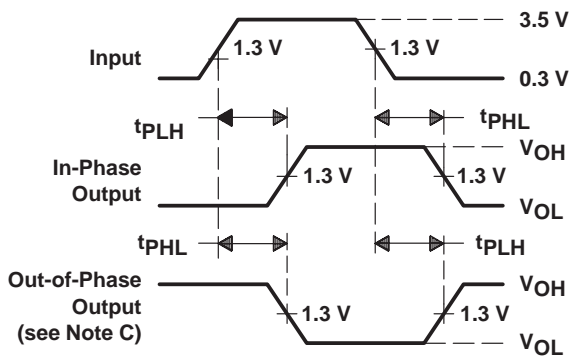
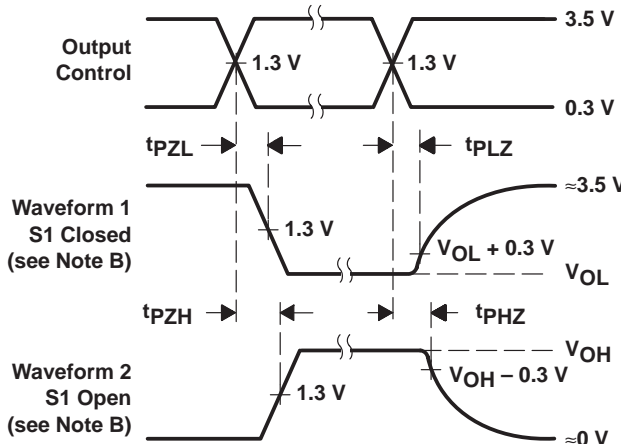
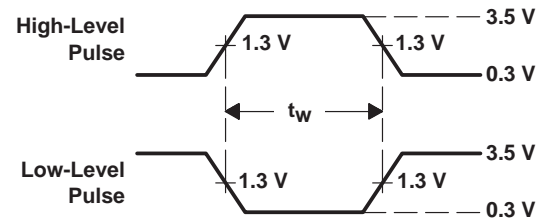
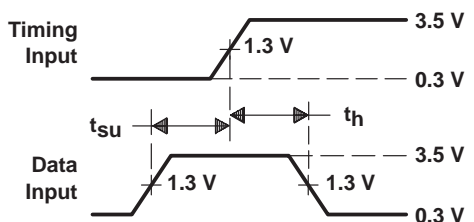
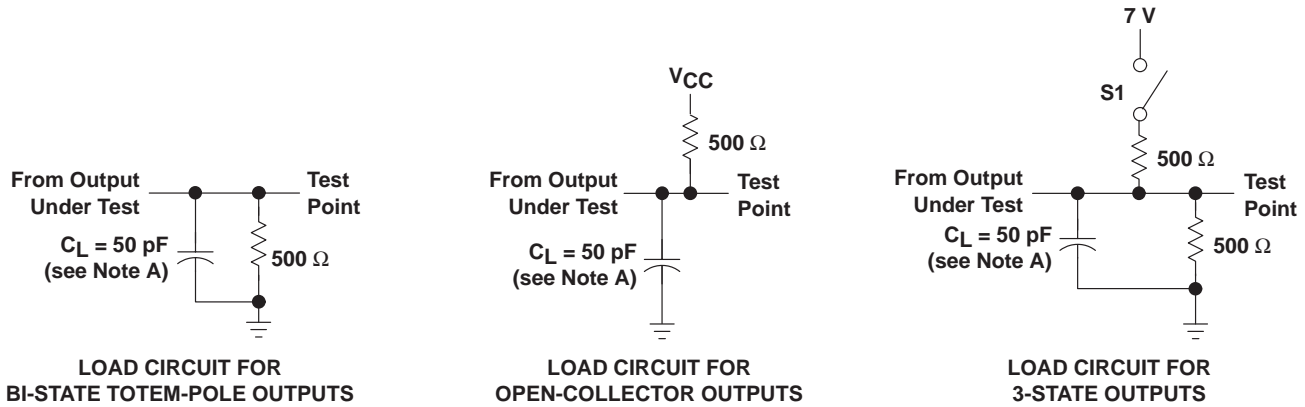


Figure 2. Bidirectional Bus Driver

**SN54ALS374A, SN54AS374, SN74ALS374A, SN74AS374**  
**OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS**  
**WITH 3-STATE OUTPUTS**

SDAS167C – APRIL 1982 – REVISED NOVEMBER 1999

**PARAMETER MEASUREMENT INFORMATION**  
**SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
  - D. All input pulses have the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $t_r = t_f = 2 \text{ ns}$ , duty cycle = 50%.
  - E. The outputs are measured one at a time with one transition per measurement.

**Figure 3. Load Circuits and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9756201QRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9756201QR A SNJ54AS374J	<a href="#">Samples</a>
83020022A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	83020022A SNJ54ALS 374AFK	<a href="#">Samples</a>
8302002RA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8302002RA SNJ54ALS374AJ	<a href="#">Samples</a>
8302002SA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8302002SA SNJ54ALS374AW	<a href="#">Samples</a>
JM38510/37204B2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type		JM38510/ 37204B2A	<a href="#">Samples</a>
JM38510/37204BRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type		JM38510/ 37204BRA	<a href="#">Samples</a>
M38510/37204B2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 37204B2A	<a href="#">Samples</a>
M38510/37204BRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 37204BRA	<a href="#">Samples</a>
SN54ALS374AJ	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type		SN54ALS374AJ	<a href="#">Samples</a>
SN54AS374J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54AS374J	<a href="#">Samples</a>
SN74ALS374ADW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS374A	<a href="#">Samples</a>
SN74ALS374ADWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS374A	<a href="#">Samples</a>
SN74ALS374ADWRE4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS374A	<a href="#">Samples</a>
SN74ALS374AN	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS374AN	<a href="#">Samples</a>
SN74ALS374ANE4	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS374AN	<a href="#">Samples</a>
SN74ALS374ANSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS374A	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AS374DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS374	<a href="#">Samples</a>
SN74AS374N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74AS374N	<a href="#">Samples</a>
SNJ54ALS374AFK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	83020022A SNJ54ALS 374AFK	<a href="#">Samples</a>
SNJ54ALS374AJ	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8302002RA SNJ54ALS374AJ	<a href="#">Samples</a>
SNJ54ALS374AW	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8302002SA SNJ54ALS374AW	<a href="#">Samples</a>
SNJ54AS374J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9756201QR A SNJ54AS374J	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54ALS374A, SN54AS374, SN74ALS374A, SN74AS374 :**

- Catalog : [SN74ALS374A](#), [SN74AS374](#)
- Military : [SN54ALS374A](#), [SN54AS374](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

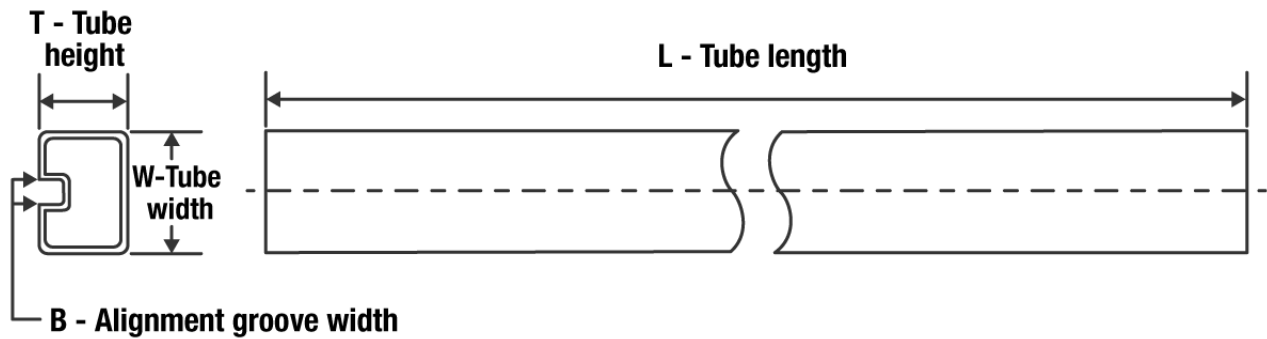

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS374ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ALS374ANSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS374ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ALS374ANSR	SO	NS	20	2000	367.0	367.0	45.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
83020022A	FK	LCCC	20	1	506.98	12.06	2030	NA
JM38510/37204B2A	FK	LCCC	20	1	506.98	12.06	2030	NA
M38510/37204B2A	FK	LCCC	20	1	506.98	12.06	2030	NA
SN74ALS374ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS374AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS374ANE4	N	PDIP	20	20	506	13.97	11230	4.32
SN74AS374DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74AS374N	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54ALS374AFK	FK	LCCC	20	1	506.98	12.06	2030	NA

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated