

CDx4HC243, CDx4HCT243 High-Speed CMOS Logic Quad-Bus Transceiver with Three-State Outputs

1 Features

- Typical propagation delay (A to B, B to A) of 7ns at $V_{CC} = 5$ V, $C_L = 15\text{pF}$, $T_A = 25^\circ\text{C}$
- Three-state outputs
- Buffered inputs
- Fanout (over temperature range)
 - Standard outputs : 10 LSTTL loads
 - Bus driver outputs : 15 LSTTL loads
- Wide operating temperature range : -55°C to 125°C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- HC types
 - 2 V to 6 V Operation
 - High noise immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5$ V
- HCT types
 - 4.5 V to 5.5 V operation
 - Direct LSTTL input logic compatibility, $V_{IL} = 0.8$ V (Max), $V_{IH} = 2$ V (Min)
 - CMOS input compatibility, $I_I \leq 1\mu\text{A}$ at V_{OL} , V_{OH}

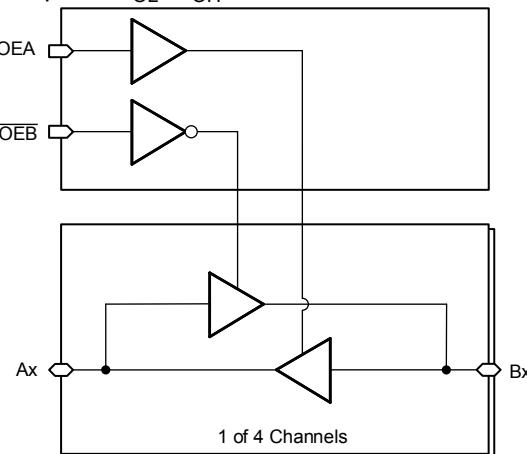
2 Description

The CDx4HC243 and CDx4HCT243 are quad bus transceivers with 3-state outputs. The OEA and OEB inputs control both the high-impedance state as well as the direction of communication through the device.

Device Information

| PART NUMBER | PACKAGE ⁽¹⁾ | BODY SIZE (NOM) |
|-------------|------------------------|--------------------|
| CD54HC243F | CDIP (14) | 19.55 mm × 6.71 mm |
| CD74HC243E | PDIP (14) | 19.31 mm × 6.35 mm |
| CD74HC243M | SOIC (14) | 8.65 mm × 3.90 mm |
| CD74HCT243E | PDIP (14) | 19.31 mm × 6.35 mm |
| CD74HCT243M | SOIC (14) | 8.65 mm × 3.90 mm |

(1) For all packages see the orderable addendum at the end of the datasheet.



Functional Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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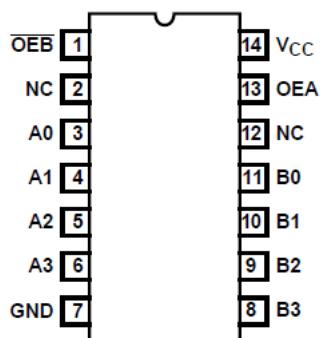
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3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision D (October 2003) to Revision E (March 2022) | Page |
|--|-------------|
| • Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards..... | 1 |

4 Pin Configuration and Functions



J, N, or D Package
14-Pin CDIP, PDIP, or SOIC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | | MIN | MAX | UNIT |
|------------------|---|---|------|-----|------|
| V _{CC} | Supply voltage | | -0.5 | 7 | V |
| I _{IK} | Input diode current | For V _I < -0.5V or V _O > V _{CC} + 0.5V | | ±20 | mA |
| I _{OK} | Output diode current | For V _C < -0.5V or V _O > V _{CC} + 0.5V | | ±20 | mA |
| I _O | Drain Current, per output | For -0.5V < V _O < V _{CC} + 0.5V | | ±35 | mA |
| I _O | Output source or sink current per output pin | For V _O > -0.5V or V _O < V _{CC} + 0.5V | | ±25 | mA |
| | Continuous current through V _{CC} or GND | | | ±70 | mA |
| T _{stg} | Storage temperature range | | -65 | 150 | °C |
| T _J | Junction temperature | | | 150 | °C |
| | Lead temperature (Soldering 10s)(SOIC - Lead Tips Only) | | | 300 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

| | | | MIN | MAX | UNIT |
|-----------------|--------------------------|------------------------|-----|-----------------|------|
| V _{CC} | Supply voltage range | HC Types | 2 | 6 | V |
| | | HCT Types | 4.5 | 5.5 | |
| V _I | Input voltage | | 0 | V _{CC} | V |
| V _O | Output voltage | | 0 | V _{CC} | V |
| t _l | Input rise and fall time | V _{CC} = 2V | | 1000 | ns |
| | | V _{CC} = 4.5V | | 500 | |
| | | V _{CC} = 6V | | 400 | |
| T _A | Temperature Range | | -55 | 125 | °C |

5.3 Thermal Information

| THERMAL METRIC | | N (PDIP) | D (SOIC) | UNIT |
|------------------|---|----------|----------|------|
| | | 14 PINS | 14 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance ⁽¹⁾ | 80 | 86 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.4 Electrical Characteristics

| PARAMETER | TEST CONDITIONS ⁽¹⁾ | V _{CC} (V) | 25°C | | | -40°C to 85°C | | -55°C to 125°C | | UNIT |
|-----------------------------------|---|------------------------------------|------------|------|------|---------------|------|----------------|------|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | |
| V _{IH} | High-level input voltage | | 2 | 1.5 | | 1.5 | | 1.5 | | V |
| | | | 4.5 | 3.15 | | 3.15 | | 3.15 | | |
| | | | 6 | 4.2 | | 4.2 | | 4.2 | | |
| V _{IL} | Low-level input voltage | | 2 | | 0.5 | | 0.5 | | 0.5 | V |
| | | | 4.5 | | 1.35 | | 1.35 | | 1.35 | |
| | | | 6 | | 1.8 | | 1.8 | | 1.8 | |
| V _{OH} | High-level output voltage CMOS loads | I _{OH} = -20µA | 2 | 1.9 | | 1.9 | | 1.9 | | V |
| | | I _{OH} = -20µA | 4.5 | 4.4 | | 4.4 | | 4.4 | | |
| | | I _{OH} = -20µA | 6 | 5.9 | | 5.9 | | 5.9 | | |
| | High-level output voltage TTL loads | I _{OH} = -6mA | 4.5 | 3.98 | | 3.84 | | 3.7 | | V |
| | | I _{OH} = -7.8mA | 6 | 5.48 | | 5.34 | | 5.2 | | |
| V _{OL} | Low-level output voltage CMOS loads | I _{OL} = 20µA | 2 | | 0.1 | | 0.1 | | 0.1 | V |
| | | I _{OL} = 20µA | 4.5 | | 0.1 | | 0.1 | | 0.1 | |
| | | I _{OL} = 20µA | 6 | | 0.1 | | 0.1 | | 0.1 | |
| | Low-level output voltage TTL | I _{OL} = 6mA | 4.5 | | 0.26 | | 0.33 | | 0.4 | V |
| | | I _{OL} = 7.8mA | 6 | | 0.26 | | 0.33 | | 0.4 | |
| I _I | Input leakage current | V _{CC} or GND | 6 | | ±0.1 | | ±1 | | ±1 | µA |
| I _{CC} | Supply Current | V _{CC} or GND | 6 | | 8 | | 80 | | 160 | µA |
| I _{OZ} | Three-state leakage current | V _{IL} or V _{IH} | 6 | | ±0.5 | | ±0.5 | | ±10 | µA |
| HCT TYPES | | | | | | | | | | |
| V _{IH} | High-level input voltage | | 4.5 to 5.5 | 2 | | 2 | | 2 | | V |
| V _{IL} | Low-level input voltage | | 4.5 to 5.5 | | 0.8 | | 0.8 | | 0.8 | V |
| V _{OH} | High-level output voltage CMOS loads | I _{OH} = -20µA | 4.5 | 4.4 | | 4.4 | | 4.4 | | V |
| | High-level output voltage TTL loads | I _{OH} = -6mA | 4.5 | 3.98 | | 3.84 | | 3.7 | | |
| V _{OL} | Low-level output voltage CMOS loads | I _{OL} = 20µA | 4.5 | | 0.1 | | 0.1 | | 0.1 | V |
| | Low-level output voltage TTL loads | I _{OL} = 6mA | 4.5 | | 0.26 | | 0.33 | | 0.4 | |
| I _I | Input leakage current | V _{CC} to GND | 5.5 | | ±0.1 | | ±1 | | ±1 | µA |
| I _{CC} | Supply current | V _{CC} or GND | 5.5 | | 8 | | 80 | | 160 | µA |
| ΔI_{CC} ⁽³⁾ | Additional supply current per input pin | One of An or Bn | 4.5 to 5.5 | 100 | 396 | | 495 | | 539 | µA |
| | | One of OEA or OEB | 4.5 to 5.5 | 100 | 216 | | 270 | | 294 | |
| I _{OZ} | Three-state leakage current | V _{IL} or V _{IH} | 5.5 | | ±0.5 | | ±5 | | ±10 | µA |

(1) V_I = V_{IH} or V_{IL}, unless otherwise noted.

(2) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

(3) Inputs held at V_{CC} – 2.1.

5.5 Switching Characteristics

Input $t_i = 6\text{ns}$. Unless otherwise specified, $C_L = 50\text{pF}$

| PARAMETER | V_{CC} (V) | 25°C | | -40°C to 85°C | -55°C to 125°C | UNIT |
|-----------------------------|---|------|-------------------|---------------|----------------|------|
| | | TYP | MAX | MAX | MAX | |
| HC TYPES | | | | | | |
| t_{pd} | Propagation delay data to outputs | 2 | 90 | 115 | 135 | ns |
| | | 4.5 | 7 ⁽¹⁾ | 18 | 23 | |
| | | 6 | 15 | 20 | 23 | |
| t_{PZL}, t_{PZH} | Output high-Z, to high level to low level | 2 | 150 | 190 | 225 | ns |
| | | 4.5 | 12 ⁽¹⁾ | 30 | 38 | |
| | | 6 | 26 | 33 | 38 | |
| t_{PHZ}, t_{PLZ} | Output high level, output low level to high-Z | 2 | 150 | 190 | 225 | ns |
| | | 4.5 | 12 ⁽¹⁾ | 30 | 38 | |
| | | 6 | 26 | 33 | 38 | |
| t_t | Output transition times | 2 | 60 | 75 | 90 | ns |
| | | 4.5 | 12 | 15 | 18 | |
| | | 6 | 10 | 13 | 15 | |
| C_i | Input capacitance | | 10 | 10 | 10 | pF |
| C_O | Three-state output capacitance | | 20 | 20 | 20 | pF |
| C_{pd} ^{(2) (3)} | Power dissipation capacitance | 5 | 80 | | | pF |
| HCT TYPES | | | | | | |
| t_{pd} | Propagation delay data to outputs | 4.5 | 9 ⁽¹⁾ | 22 | 28 | 33 |
| t_{PZH}, t_{PLZ} | Output high-Z to high level to low level | 4.5 | 14 ⁽¹⁾ | 34 | 43 | 51 |
| t_{PHZ}, t_{PLZ} | Output high level, output low level to high-Z | 4.5 | 14 ⁽¹⁾ | 35 | 44 | 53 |
| t_t | Output transition times | 4.5 | 12 | 15 | 18 | ns |
| C_i | Input capacitance | | 10 | 10 | 10 | pF |
| C_O | Three-state output capacitance | | 20 | 20 | 20 | pF |
| C_{pd} ^{(2) (3)} | Power dissipation capacitance | 5 | 91 | | | pF |

(1) Typical value tested at 5V, $C_L = 15\text{pF}$.

(2) C_{PD} is used to determine the dynamic power consumption, per channel.

(3) $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

6 Parameter Measurement Information

t_{PD} is the maximum between t_{PLH} and t_{PHL}

t_t is the maximum between t_{TLH} and t_{TDL}

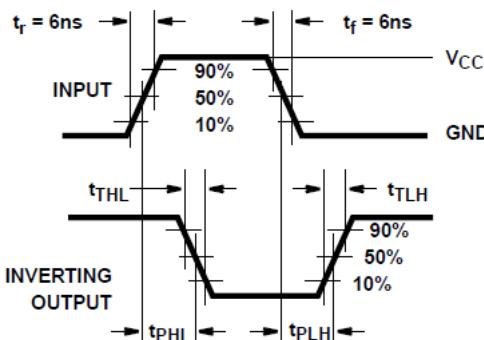


Figure 6-1. HC and HCT transition times and propagation delay times, combination logic

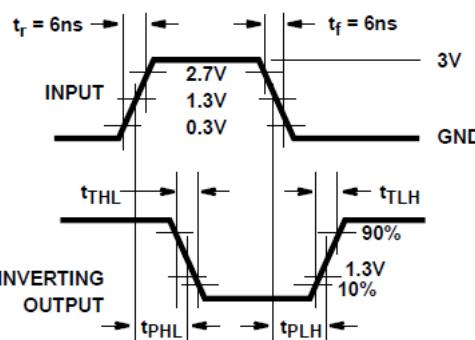


Figure 6-2. HCT transition times and propagation delay times, combination logic

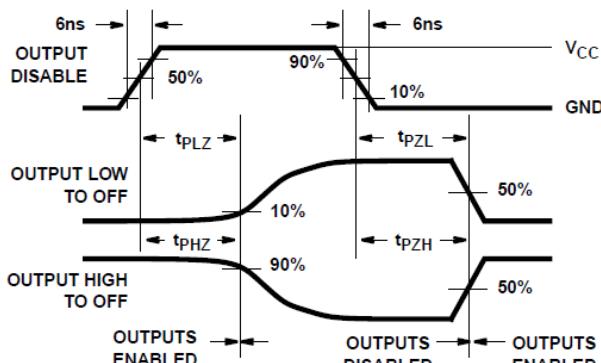


Figure 6-3. HC three-state propagation delay waveform

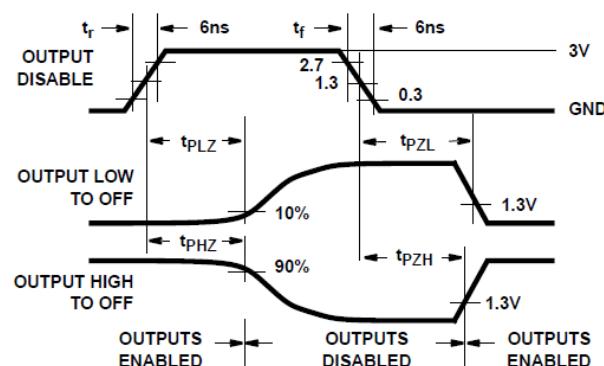
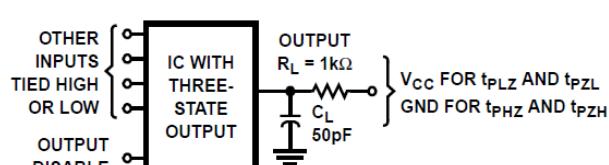


Figure 6-4. HCT three-state propagation delay waveform



NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output $R_L = 1k\Omega$ to V_{CC} , $C_L = 50pF$.

Figure 6-5. HC and HCT three-state propagation delay test circuit

7 Detailed Description

7.1 Overview

The CDx4HC243 and CDx4HCT243 silicon-gate CMOS three-state bidirectional noninverting buffers are intended for two-way asynchronous communication between data buses. They have high-drive-current outputs that enable high-speed operation when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuits and have speeds comparable to low-power Schottky TTL circuits. They can drive 15 LSTTL loads.

The states of the output-enable ($\overline{\text{OEB}}$, OEA) inputs determine both the direction of flow (A to B, B to A), and the three-state mode.

7.2 Functional Block Diagram

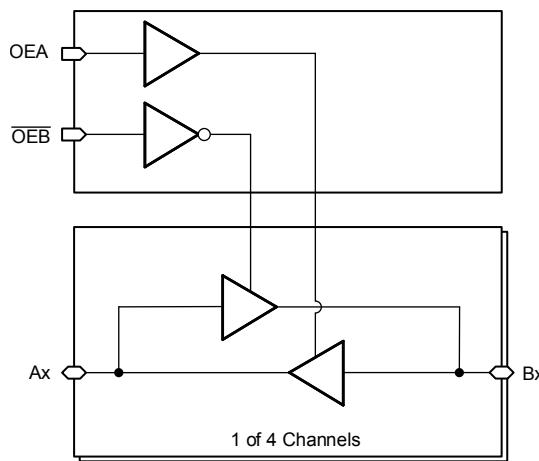


Figure 7-1. Functional Diagram

7.3 Device Functional Modes

Table 7-1. Truth Table⁽¹⁾⁽²⁾

| Control Inputs | | HC, HCT243 Series | |
|-------------------------|-----|-------------------|----|
| | | Data port status | |
| $\overline{\text{OEB}}$ | OEA | An | Bn |
| H | H | O | I |
| L | H | Z | Z |
| H | L | Z | Z |
| L | L | I | O |

(1) H = High voltage level. L = Low voltage level. I = Input. O = Output (Same level as input). Z = High Impedance
(2) To prevent excess currents in the High Z modes all I/O terminals should be terminated with $10\text{k}\Omega$ to $1\text{M}\Omega$ resistors.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|---------------------------|---|
| 8409001CA | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8409001CA CD54HC243F3A | Samples |
| CD54HC243F | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD54HC243F | Samples |
| CD54HC243F3A | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8409001CA CD54HC243F3A | Samples |
| CD74HC243E | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC243E | Samples |
| CD74HC243EE4 | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC243E | Samples |
| CD74HC243M | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC243M | Samples |
| CD74HC243M96 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC243M | Samples |
| CD74HC243MT | ACTIVE | SOIC | D | 14 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC243M | Samples |
| CD74HCT243E | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HCT243E | Samples |
| CD74HCT243EE4 | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HCT243E | Samples |
| CD74HCT243M | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT243M | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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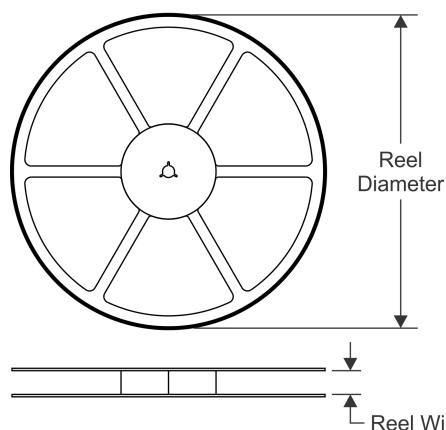
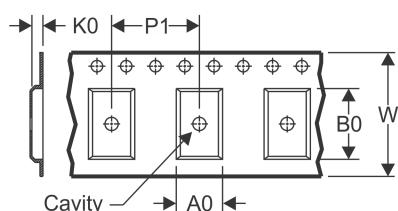
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC243, CD74HC243 :

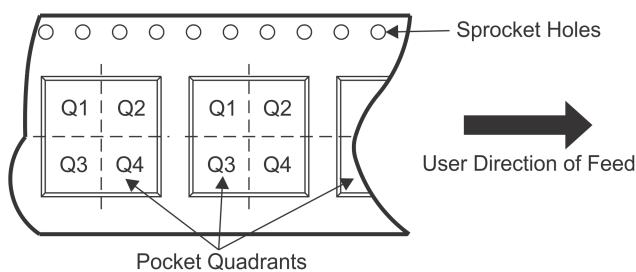
- Catalog : [CD74HC243](#)
- Military : [CD54HC243](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


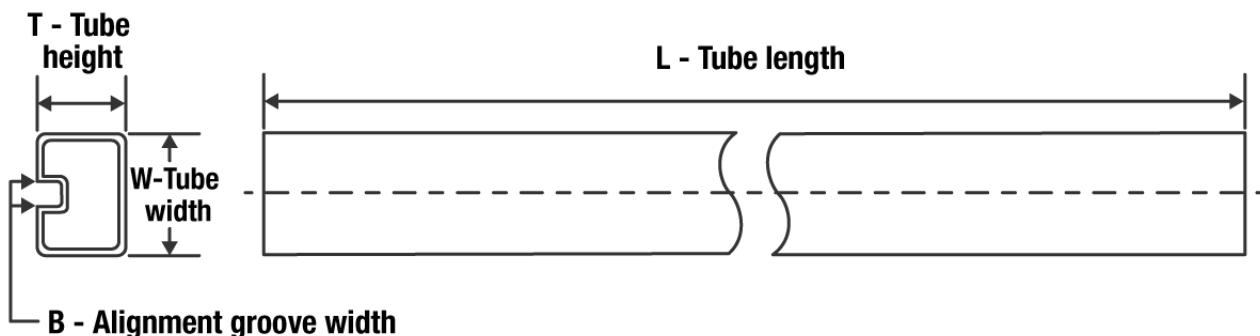
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC243M96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HC243MT | SOIC | D | 14 | 250 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC243M96 | SOIC | D | 14 | 2500 | 853.0 | 449.0 | 35.0 |
| CD74HC243MT | SOIC | D | 14 | 250 | 210.0 | 185.0 | 35.0 |

TUBE


*All dimensions are nominal

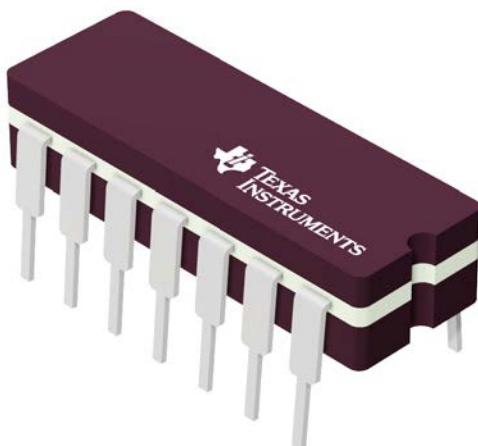
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD74HC243E | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC243E | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC243EE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC243EE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC243M | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| CD74HCT243E | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT243E | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT243EE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT243EE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT243M | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |

GENERIC PACKAGE VIEW

J 14

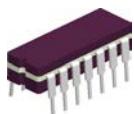
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

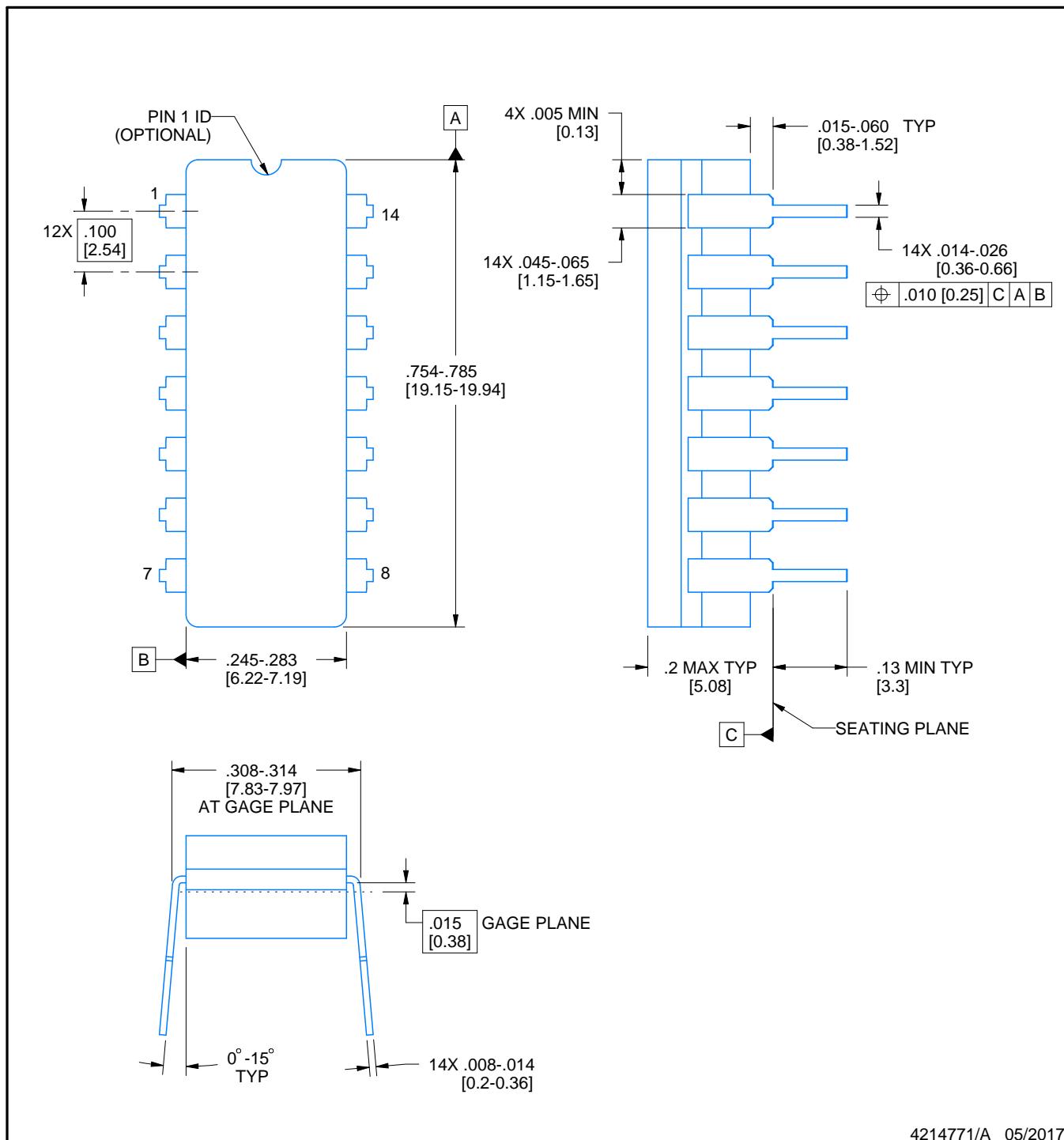


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

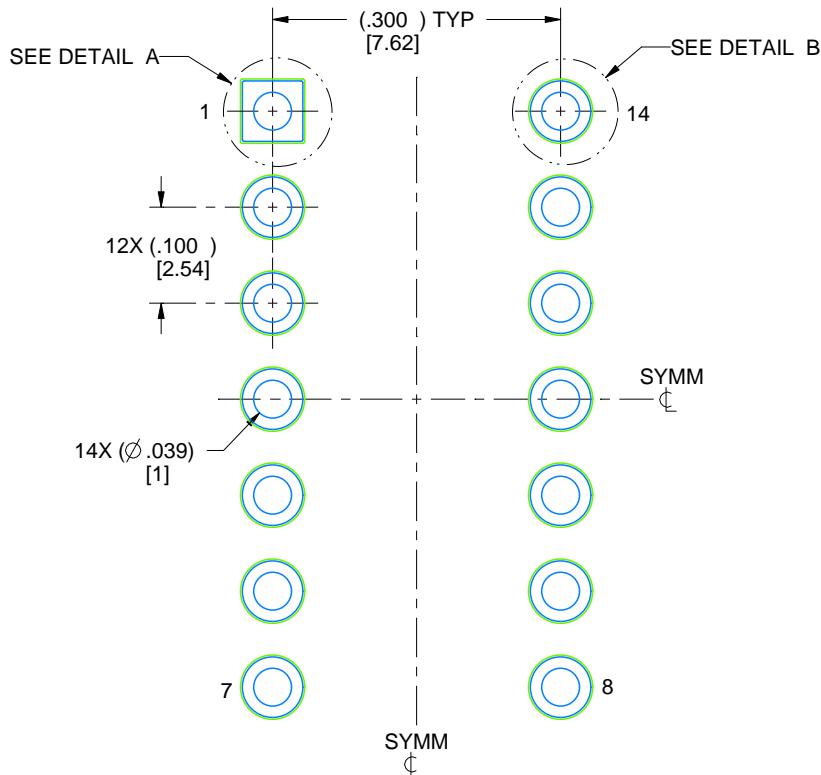
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

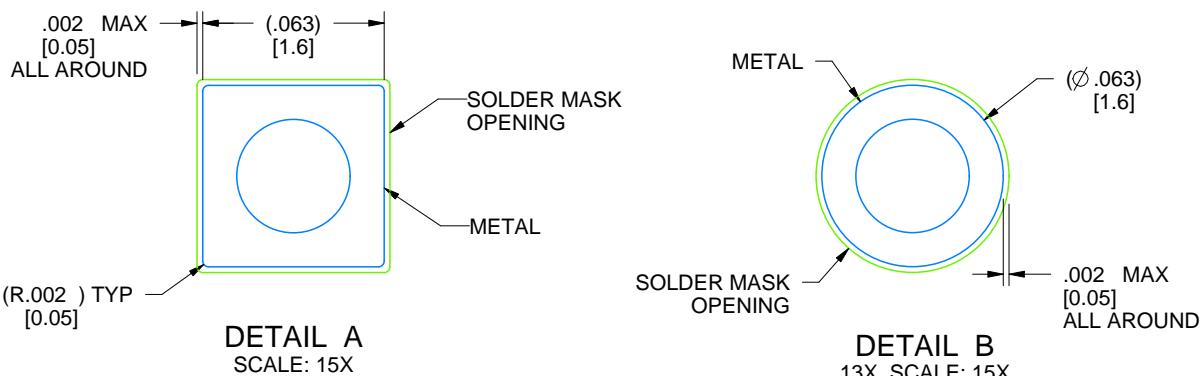
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



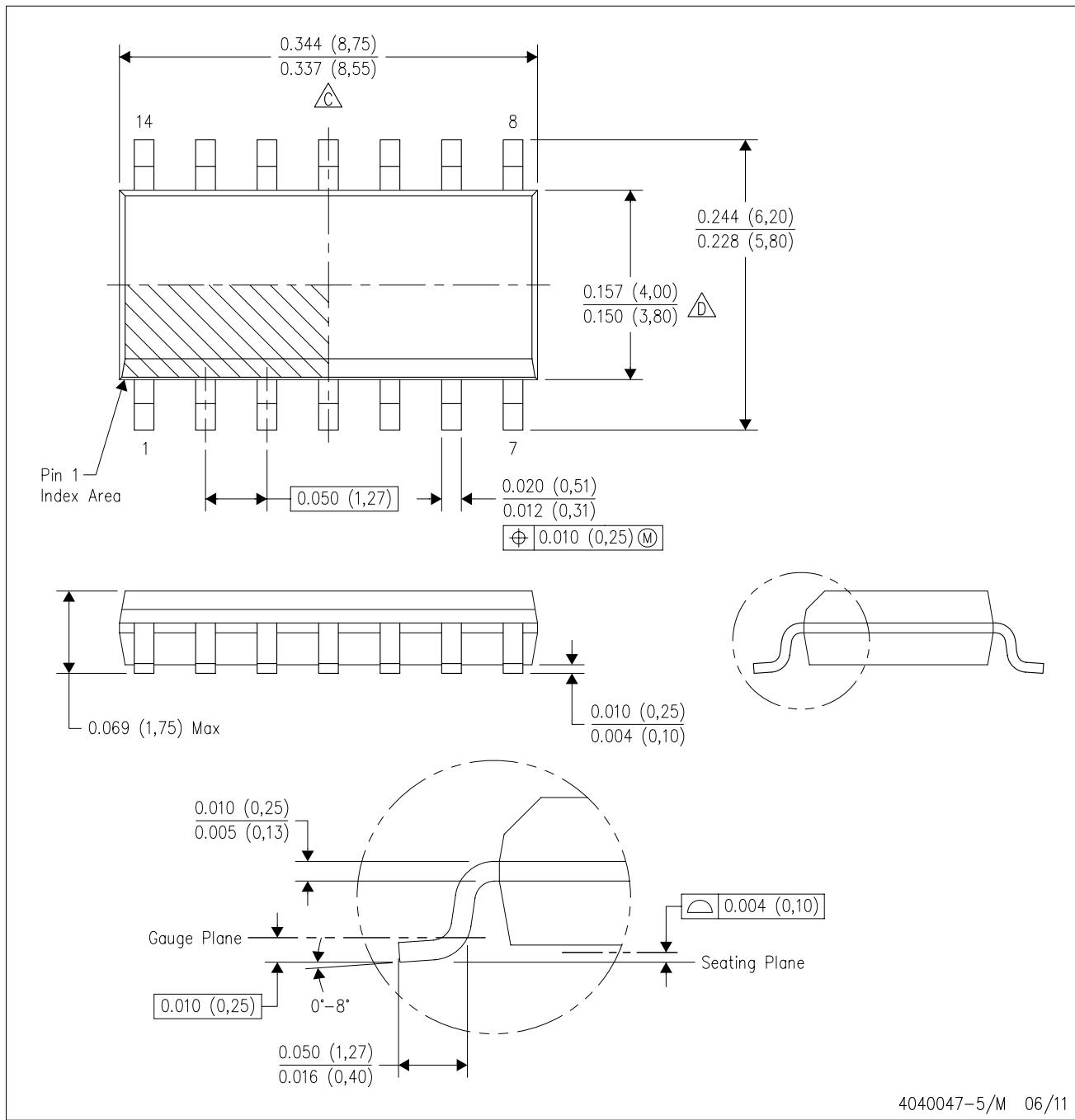
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

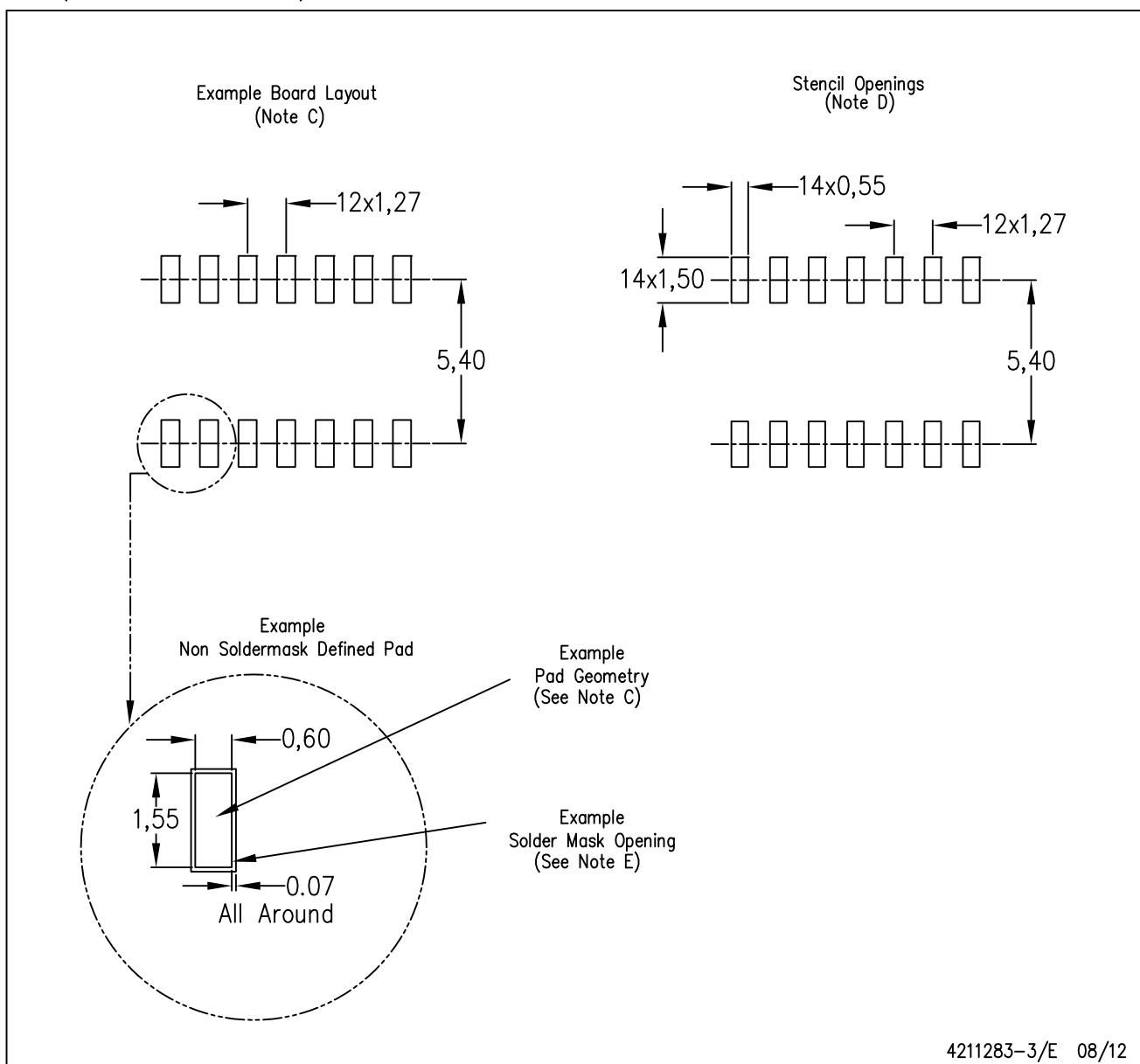
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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