

# CDx4HC243, CDx4HCT243 High-Speed CMOS Logic Quad-Bus Transceiver with Three-State Outputs

## 1 Features

- Typical propagation delay (A to B, B to A) of 7ns at  $V_{CC} = 5\text{ V}$ ,  $C_L = 15\text{ pF}$ ,  $T_A = 25^\circ\text{C}$
- Three-state outputs
- Buffered inputs
- Fanout (over temperature range)
  - Standard outputs : 10 LSTTL loads
  - Bus driver outputs : 15 LSTTL loads
- Wide operating temperature range :  $-55^\circ\text{C}$  to  $125^\circ\text{C}$
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- HC types
  - 2 V to 6 V Operation
  - High noise immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5\text{ V}$
- HCT types
  - 4.5 V to 5.5 V operation
  - Direct LSTTL input logic compatibility,  $V_{IL} = 0.8\text{ V (Max)}$ ,  $V_{IH} = 2\text{ V (Min)}$
  - CMOS input compatibility,  $I_I \leq 1\mu\text{A}$  at  $V_{OL}$ ,  $V_{OH}$

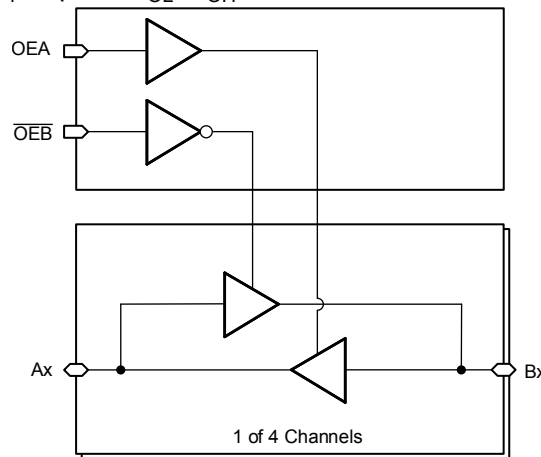
## 2 Description

The CDx4HC243 and CDx4HCT243 are quad bus transceivers with 3-state outputs. The OEA and  $\overline{\text{OEB}}$  inputs control both the high-impedance state as well as the direction of communication through the device.

### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
CD54HC243F	CDIP (14)	19.55 mm × 6.71 mm
CD74HC243E	PDIP (14)	19.31 mm × 6.35 mm
CD74HC243M	SOIC (14)	8.65 mm × 3.90 mm
CD74HCT243E	PDIP (14)	19.31 mm × 6.35 mm
CD74HCT243M	SOIC (14)	8.65 mm × 3.90 mm

(1) For all packages see the orderable addendum at the end of the datasheet.



**Functional Block Diagram**



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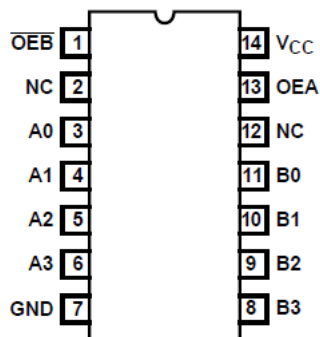
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## 3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision D (October 2003) to Revision E (March 2022)</b>	<b>Page</b>
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards.....	<b>1</b>

## 4 Pin Configuration and Functions



**J, N, or D Package**  
**14-Pin CDIP, PDIP, or SOIC**  
**Top View**

## 5 Specifications

### 5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		-0.5	7	V
$I_{IK}$	Input diode current	For $V_I < -0.5V$ or $V_O > V_{CC} + 0.5V$		$\pm 20$	mA
$I_{OK}$	Output diode current	For $V_C < -0.5V$ or $V_O > V_{CC} + 0.5V$		$\pm 20$	mA
$I_O$	Drain Current, per output	For $-0.5V < V_O < V_{CC} + 0.5V$		$\pm 35$	mA
$I_O$	Output source or sink current per output pin	For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$		$\pm 25$	mA
	Continuous current through $V_{CC}$ or GND			$\pm 70$	mA
$T_{stg}$	Storage temperature range		-65	150	°C
$T_J$	Junction temperature			150	°C
	Lead temperature (Soldering 10s)(SOIC - Lead Tips Only)			300	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	HC Types	2	6	V
		HCT Types	4.5	5.5	
$V_I$	Input voltage		0	$V_{CC}$	V
$V_O$	Output voltage		0	$V_{CC}$	V
$t_t$	Input rise and fall time	$V_{CC} = 2V$		1000	ns
		$V_{CC} = 4.5V$		500	
		$V_{CC} = 6V$		400	
$T_A$	Temperature Range		-55	125	°C

### 5.3 Thermal Information

THERMAL METRIC		N (PDIP)	D (SOIC)	UNIT
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)</sup>	80	86	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS <sup>(1)</sup>	V <sub>CC</sub> (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V <sub>IH</sub>	High-level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6	4.2			4.2		4.2		
V <sub>IL</sub>	Low-level input voltage		2	0.5			0.5		0.5		V
			4.5	1.35			1.35		1.35		
			6	1.8			1.8		1.8		
V <sub>OH</sub>	High-level output voltage CMOS loads	I <sub>OH</sub> = - 20μA	2	1.9			1.9		1.9		V
		I <sub>OH</sub> = - 20μA	4.5	4.4			4.4		4.4		
		I <sub>OH</sub> = - 20μA	6	5.9			5.9		5.9		
	High-level output voltage TTL loads	I <sub>OH</sub> = - 6mA	4.5	3.98			3.84		3.7		
		I <sub>OH</sub> = - 7.8mA	6	5.48			5.34		5.2		
V <sub>OL</sub>	Low-level output voltage CMOS loads	I <sub>OL</sub> = 20μA	2	0.1			0.1		0.1		V
		I <sub>OL</sub> = 20μA	4.5	0.1			0.1		0.1		
		I <sub>OL</sub> = 20μA	6	0.1			0.1		0.1		
	Low-level output voltage TTL	I <sub>OL</sub> = 6mA	4.5	0.26			0.33		0.4		
		I <sub>OL</sub> = 7.8mA	6	0.26			0.33		0.4		
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> or GND	6	±0.1			±1		±1		μA
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> or GND	6	8			80		160		μA
I <sub>OZ</sub>	Three-state leakage current	V <sub>IL</sub> or V <sub>IH</sub>	6	±0.5			±0.5		±10		μA
HCT TYPES											
V <sub>IH</sub>	High-level input voltage		4.5 to 5.5	2			2		2		V
V <sub>IL</sub>	Low-level input voltage		4.5 to 5.5	0.8			0.8		0.8		V
V <sub>OH</sub>	High-level output voltage CMOS loads	I <sub>OH</sub> = - 20μA	4.5	4.4			4.4		4.4		V
	High-level output voltage TTL loads	I <sub>OH</sub> = - 6mA	4.5	3.98			3.84		3.7		
V <sub>OL</sub>	Low-level output voltage CMOS loads	I <sub>OL</sub> = 20μA	4.5	0.1			0.1		0.1		V
	Low-level output voltage TTL loads	I <sub>OL</sub> = 6mA	4.5	0.26			0.33		0.4		
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> to GND	5.5	±0.1			±1		±1		μA
I <sub>CC</sub>	Supply current	V <sub>CC</sub> or GND	5.5	8			80		160		μA
ΔI <sub>CC</sub> <sup>(2)</sup> <sup>(3)</sup>	Additional supply current per input pin	One of An or Bn	4.5 to 5.5	100 396			495		539		μA
		One of OEA or OEB	4.5 to 5.5	100 216			270		294		
I <sub>OZ</sub>	Three-state leakage current	V <sub>IL</sub> or V <sub>IH</sub>	5.5	±0.5			±5		±10		μA

(1) V<sub>I</sub> = V<sub>IH</sub> or V<sub>IL</sub>, unless otherwise noted.

(2) For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA.

(3) Inputs held at V<sub>CC</sub> - 2.1.

## 5.5 Switching Characteristics

Input  $t_i = 6\text{ns}$ . Unless otherwise specified,  $C_L = 50\text{pF}$

PARAMETER		V <sub>CC</sub> (V)	25°C		-40°C to 85°C	-55°C to 125°C	UNIT	
			TYP	MAX	MAX	MAX		
HC TYPES								
t <sub>pd</sub>	Propagation delay data to outputs	2		90	115	135	ns	
		4.5		7 <sup>(1)</sup>	18	23		27
		6		15	20	23		
t <sub>PZL</sub> , t <sub>PZH</sub>	Output high-Z, to high level to low level	2		150	190	225	ns	
		4.5		12 <sup>(1)</sup>	30	38		45
		6		26	33	38		
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output high level, output low level to high-Z	2		150	190	225	ns	
		4.5		12 <sup>(1)</sup>	30	38		45
		6		26	33	38		
t <sub>t</sub>	Output transition times	2		60	75	90	ns	
		4.5		12	15	18		
		6		10	13	15		
C <sub>i</sub>	Input capacitance			10	10	10	pF	
C <sub>O</sub>	Three-state output capacitance			20	20	20	pF	
C <sub>pd</sub> <sup>(2) (3)</sup>	Power dissipation capacitance	5		80			pF	
HCT TYPES								
t <sub>pd</sub>	Propagation delay data to outputs	4.5		9 <sup>(1)</sup>	22	28	33	ns
t <sub>PZH</sub> , t <sub>PLZ</sub>	Output high-Z to high level to low level	4.5		14 <sup>(1)</sup>	34	43	51	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output high level, output low level to high-Z	4.5		14 <sup>(1)</sup>	35	44	53	ns
t <sub>t</sub>	Output transition times	4.5		12	15	18		ns
C <sub>i</sub>	Input capacitance			10	10	10		pF
C <sub>O</sub>	Three-state output capacitance			20	20	20		pF
C <sub>pd</sub> <sup>(2) (3)</sup>	Power dissipation capacitance	5		91				pF

(1) Typical value tested at 5V,  $C_L = 15\text{pF}$ .

(2)  $C_{PD}$  is used to determine the dynamic power consumption, per channel.

(3)  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = Input Frequency,  $f_O$  = Output Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

## 6 Parameter Measurement Information

$t_{PD}$  is the maximum between  $t_{PLH}$  and  $t_{PHL}$

$t_t$  is the maximum between  $t_{TLH}$  and  $t_{THL}$

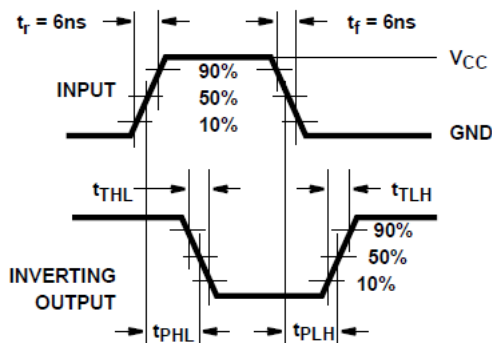


Figure 6-1. HC and HCT transition times and propagation delay times, combination logic

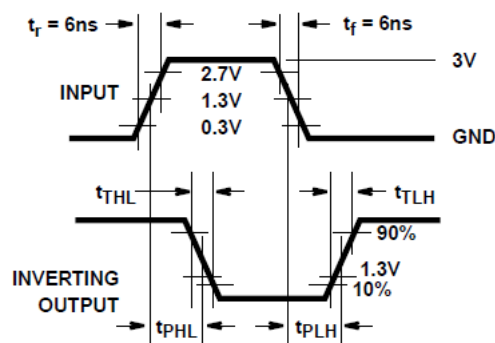


Figure 6-2. HCT transition times and propagation delay times, combination logic

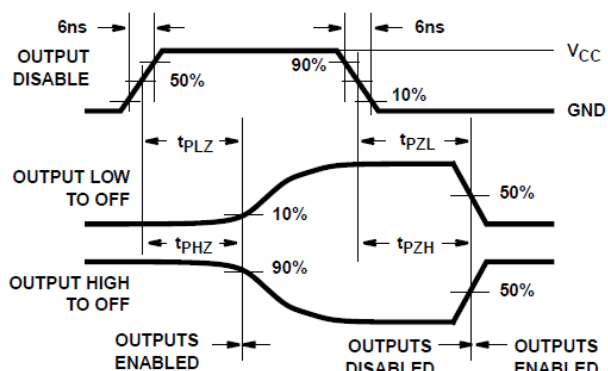


Figure 6-3. HC three-state propagation delay waveform

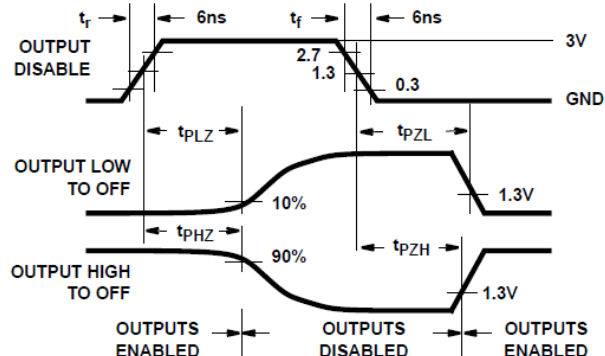
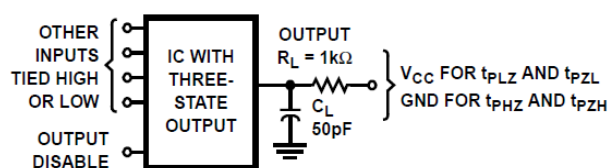


Figure 6-4. HCT three-state propagation delay waveform



NOTE: Open drain waveforms  $t_{PLZ}$  and  $t_{PZL}$  are the same as those for three-state shown on the left. The test circuit is Output  $R_L = 1k\Omega$  to  $V_{CC}$ ,  $C_L = 50pF$ .

Figure 6-5. HC and HCT three-state propagation delay test circuit

## 7 Detailed Description

### 7.1 Overview

The CDx4HC243 and CDx4HCT243 silicon-gate CMOS three-state bidirectional noninverting buffers are intended for two-way asynchronous communication between data buses. They have high-drive-current outputs that enable high-speed operation when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuits and have speeds comparable to low-power Schottky TTL circuits. They can drive 15 LSTTL loads.

The states of the output-enable ( $\overline{\text{OEB}}$ , OEA) inputs determine both the direction of flow (A to B, B to A), and the three-state mode.

### 7.2 Functional Block Diagram

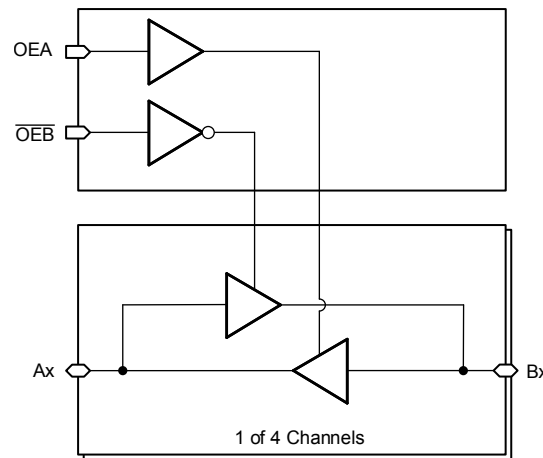


Figure 7-1. Functional Diagram

### 7.3 Device Functional Modes

Table 7-1. Truth Table<sup>(1)(2)</sup>

Control Inputs		HC, HCT243 Series	
		Data port status	
$\overline{\text{OEB}}$	OEA	An	Bn
H	H	O	I
L	H	Z	Z
H	L	Z	Z
L	L	I	O

- (1) H = High voltage level. L = Low voltage level. I = Input. O = Output (Same level as input). Z = High Impedance  
(2) To prevent excess currents in the High Z modes all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.



## 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 9 Layout

### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
8409001CA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8409001CA CD54HC243F3A	<a href="#">Samples</a>
CD54HC243F	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HC243F	<a href="#">Samples</a>
CD54HC243F3A	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8409001CA CD54HC243F3A	<a href="#">Samples</a>
CD74HC243E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC243E	<a href="#">Samples</a>
CD74HC243EE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC243E	<a href="#">Samples</a>
CD74HC243M	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC243M	<a href="#">Samples</a>
CD74HC243M96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC243M	<a href="#">Samples</a>
CD74HC243MT	ACTIVE	SOIC	D	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC243M	<a href="#">Samples</a>
CD74HCT243E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT243E	<a href="#">Samples</a>
CD74HCT243EE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT243E	<a href="#">Samples</a>
CD74HCT243M	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT243M	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54HC243, CD74HC243 :**

- Catalog : [CD74HC243](#)
- Military : [CD54HC243](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC243M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC243MT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

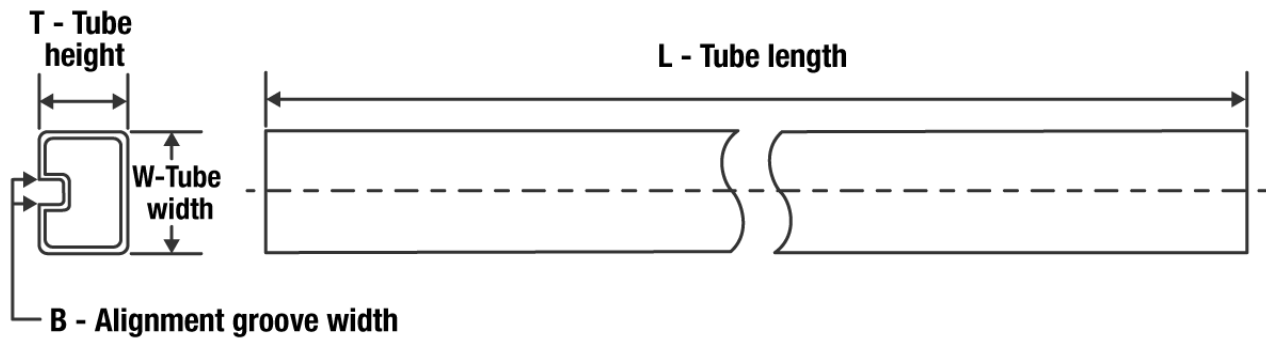
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC243M96	SOIC	D	14	2500	853.0	449.0	35.0
CD74HC243MT	SOIC	D	14	250	210.0	185.0	35.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC243E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC243E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC243EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC243EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC243M	D	SOIC	14	50	506.6	8	3940	4.32
CD74HCT243E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT243E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT243EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT243EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT243M	D	SOIC	14	50	506.6	8	3940	4.32

**J 14**

## GENERIC PACKAGE VIEW

**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G



**J0014A****PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



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**NOTES:**

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



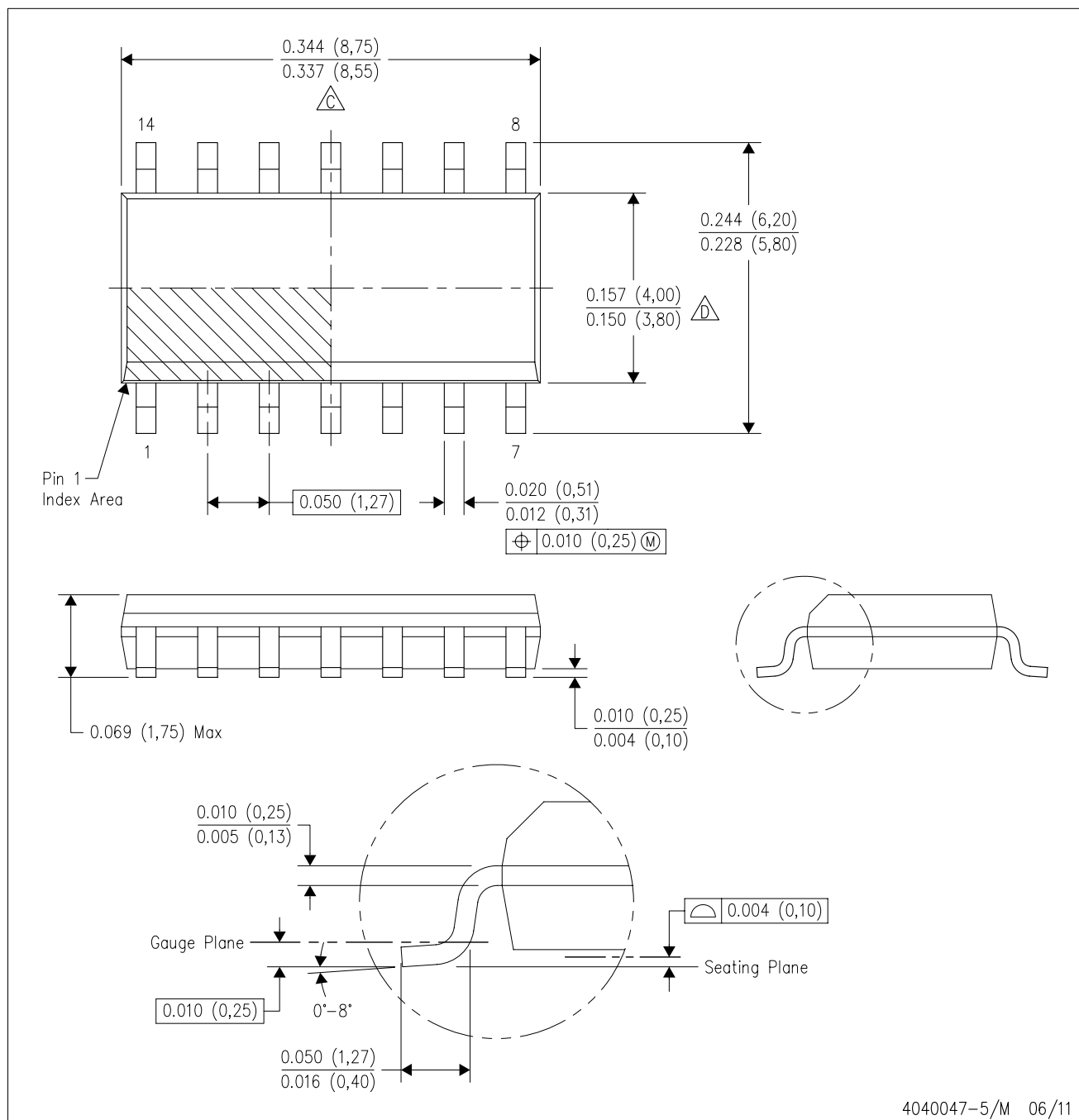
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



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## D (R-PDSO-G14)

## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.  
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.  
E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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