用于 I²C 总线的 PCF8574A 远程 8 位 I/O 扩展器

1 特性

- 10 µA 低待机电流消耗（最大值）
- I²C 至并行端口扩展器
- 开漏中断输出
- 兼容大多数微控制器
- 具有高电流驱动能力的锁存输出，用于直接驱动 LED
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求

2 应用

- 电信方舱：滤波器单元
- 服务器
- 路由器（电信交换设备）
- 个人计算机
- 个人电子产品
- 工业自动化
- 采用 GPIO 受限处理器的产品

3 说明

这个用于两线双向总线 (I²C) 的 8 位输入/输出 (I/O) 扩展器设计用于在 2.5V 至 6V V_{CC} 之间运行。

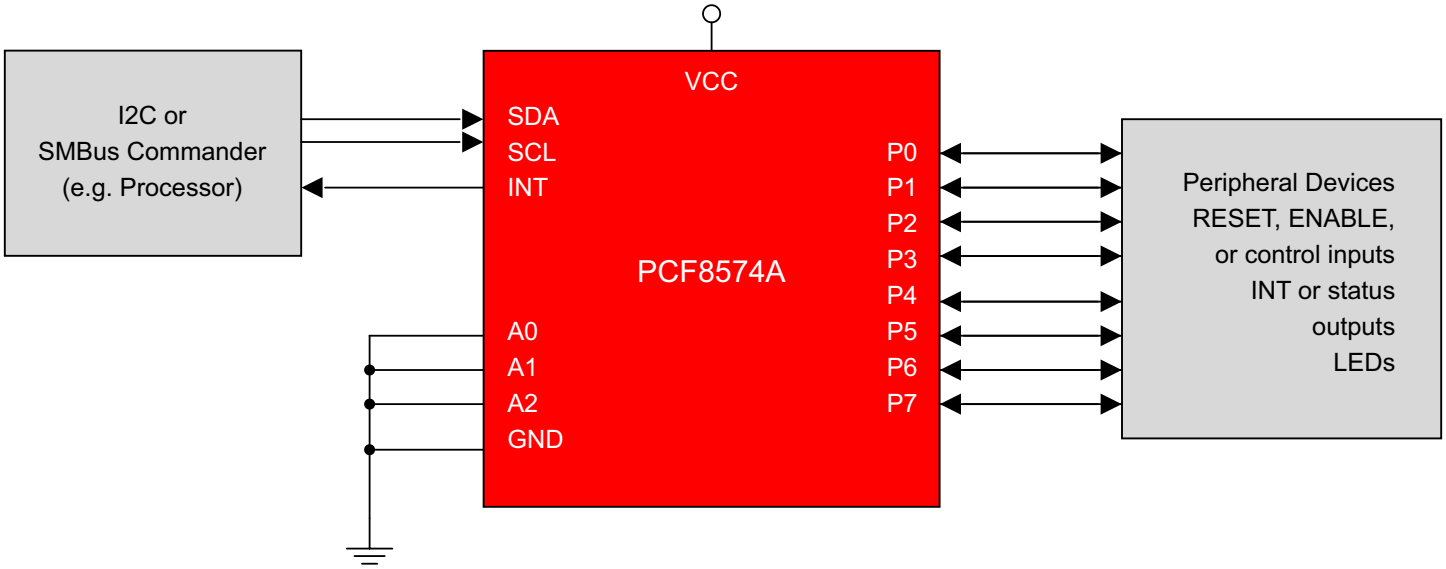
PCF8574A 器件通过 I²C 接口 [串行时钟 (SCL)、串行数据 (SDA)] 为大多数微控制器系列提供通用远程 I/O 扩展。

该器件具有一个 8 位准双向 I/O 端口 (P0 – P7)，其中包括具有高电流驱动能力的锁存输出，用于直接驱动 LED。每个准双向 I/O 都可以用作输入或输出（无需使用数据方向控制信号）。在上电时，这些 I/O 处于高电平。在该模式下，仅有一个连接到 V_{CC} 的电流源处于活动状态。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
PCF8574A	VQFN (20)	4.50mm × 3.50mm
	PDIP (16)	19.30mm x 6.35mm
	SOIC (16)	10.30mm × 7.50mm
	TSSOP (20)	6.50mm × 4.40mm
	TVSOP (20)	5.00mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



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4 Revision History

Changes from Revision F (January 2015) to Revision G (August 2021) **Page**

- 将提到的旧术语例全局更改为命令程序和响应程序 1
- Changed the *Thermal Information* table 5
- Changed 图 7-2 Responder address from: S0100 To: S0111 9
- Changed 图 8-1 14
- Changed Note B from: configured as 0100000to: configured as 0111000 16

Changes from Revision E (January 2015) to Revision F (January 2015) **Page**

- Added Junction temperature to the *Absolute Maximum Ratings* 4
- Changed Supply Current (A) To: Supply Current (µA) and f_{SCL} = 400 kHz to f_{SCL} = 100 kHz in 图 6-1 7
- Changed Supply Current (A) To: Supply Current (µA) in 图 6-2 7
- Changed Supply Current (A) To: Supply Current (µA) and f_{SCL} = 400 kHz to f_{SCL} = 100 kHz in 图 6-3 7

Changes from Revision D (October 2005) to Revision E (January 2015) **Page**

- 添加了*应用*、*器件信息* 表、*引脚功能* 表、*ESD 等级* 表、*热性能信息* 表、*典型特性*、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 1
- 删除了*订购信息* 表 1

5 Pin Configuration and Functions

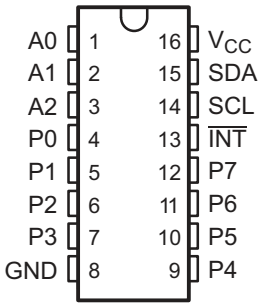


图 5-1. DW or N Package 16 Pins Top View

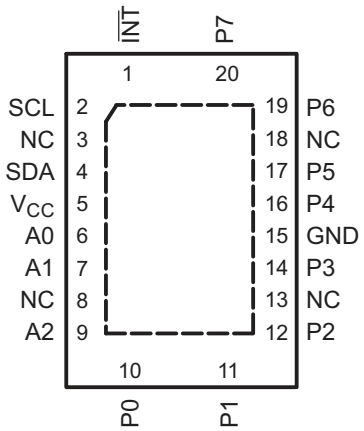


图 5-2. RGY Package 20 Pins Top View

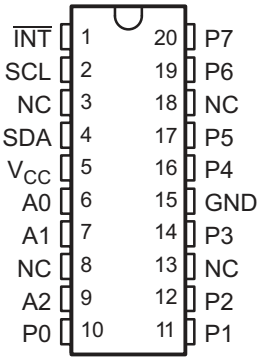


图 5-3. DGV or PW Package 20 Pins Top View

表 5-1. Pin Functions

PIN				TYPE	DESCRIPTION
NAME	RGY	DGV or PW	DW or N		
A[0..2]	6, 7, 9	6, 7, 9	1, 2, 3	I	Address inputs 0 through 2. Connect directly to V_{CC} or ground. Pullup resistors are not needed.
GND	15	15	8	—	Ground
$\overline{INT}$	1	1	13	O	Interrupt output. Connect to V_{CC} through a pullup resistor.
NC	3, 8, 13, 18	3, 8, 13, 18	-	—	Do not connect
P[0..7]	10, 11, 12, 14, 16, 17, 19, 20	10, 11, 12, 14, 16, 17, 19, 20	4, 5, 6, 7, 9, 10, 11, 12	I/O	P-port input/output. Push-pull design structure.
SCL	2	2	14	I	Serial clock line. Connect to V_{CC} through a pullup resistor
SDA	4	4	15	I/O	Serial data line. Connect to V_{CC} through a pullup resistor.
V_{CC}	5	5	16	—	Voltage supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		– 0.5	7	V
V_I	Input voltage range(2)		– 0.5	V_{CC} + 0.5	V
V_O	Output voltage range(2)		– 0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		– 20	mA
I_{OK}	Output clamp current	V_O < 0		– 20	mA
I_{OK}	Input/output clamp current	V_O < 0 or V_O > V_{CC}		±400	μA
I_{OL}	Continuous output low current	V_O = 0 to V_{CC}		50	mA
I_{OH}	Continuous output high current	V_O = 0 to V_{CC}		– 4	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		– 65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.5	6	V
V_{IH}	High-level input voltage	0.7 × V_{CC}	V_{CC} + 0.5	V
V_{IL}	Low-level input voltage	– 0.5	0.3 × V_{CC}	V
I_{OH}	High-level output current		– 1	mA
I_{OL}	Low-level output current		25	mA
T_A	Operating free-air temperature	– 40	85	°C

6.4 Thermal Information

THERMAL METRIC[1]		PCF8574					UNIT
		DGV	DW	N	PW	RGY	
		20 PINS	16 PINS	16 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.2	79.7	48.3	99.5	41.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.2	42.5	35.6	34.5	42.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53.4	44.4	28.2	50.5	16.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	14.8	20.5	2.0	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.8	43.8	28.1	49.9	16.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	5.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = – 18 mA	2.5 V to 6 V	– 1.2			V
V_{POR}	Power-on reset voltage[2]	$V_I = V_{CC}$ or GND, I_O = 0	6 V		1.3	2.4	V
I_{OH}	P port	V_O = GND	2.5 V to 6 V	30		300	µA
I_{OHT}	P-port transient pullup current	High during acknowledge, V_{OH} = GND	2.5 V		– 1		mA
I_{OL}	SDA	V_O = 0.4 V	2.5 V to 6 V	3			mA
	P port	V_O = 1 V	5 V	10	25		
	$\overline{INT}$	V_O = 0.4 V	2.5 V to 6 V	1.6			
I_I	SCL, SDA	$V_I = V_{CC}$ or GND	2.5 V to 6 V			±5	µA
	$\overline{INT}$					±5	
	A0, A1, A2					±5	
I_{IHL}	P port	$V_I \geq V_{CC}$ or $V_I \leq$ GND	2.5 V to 6 V			±400	µA
I_{CC}	Operating mode	$V_I = V_{CC}$ or GND, I_O = 0, f_{SCL} = 100 kHz	6 V		40	100	µA
	Standby mode	$V_I = V_{CC}$ or GND, I_O = 0			2.5	10	
C_i	SCL	$V_I = V_{CC}$ or GND	2.5 V to 6 V		1.5	7	pF
C_{io}	SDA	$V_{IO} = V_{CC}$ or GND	2.5 V to 6 V		3	7	pF
	P port				4	10	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) The power-on reset circuit resets the I^2C-bus logic with $V_{CC} < V_{POR}$ and sets all I/Os to logic high (with current source to V_{CC}).

6.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

			MIN	MAX	UNIT
f_{scl}	I²C clock frequency			100	kHz
t_{sch}	I²C clock high time		4		μs
t_{scl}	I²C clock low time		4.7		μs
t_{sp}	I²C spike time			100	ns
t_{sds}	I²C serial-data setup time		250		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time			1	μs
t_{icf}	I²C input fall time			0.3	μs
t_{ocf}	I²C output fall time (10-pF to 400-pF bus)			300	ns
t_{buf}	I²C bus free time between stop and start		4.7		μs
t_{sts}	I²C start or repeated start condition setup		4.7		μs
t_{sth}	I²C start or repeated start condition hold		4		μs
t_{sps}	I²C stop-condition setup		4		μs
t_{vd}	Valid-data time	SCL low to SDA output valid		3.4	μs
C_b	I²C bus capacitive load			400	pF

6.7 Switching Characteristics

over recommended operating free-air temperature range, $C_L \leqslant 100$ pF (unless otherwise noted) (see 图 7-2)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pv}	Output data valid	SCL	P port		4	μs
t_{su}	Input data setup time	P port	SCL	0		μs
t_h	Input data hold time	P port	SCL	4		μs
t_{iv}	Interrupt valid time	P port	$\overline{INT}$		4	μs
t_{ir}	Interrupt reset delay time	SCL	$\overline{INT}$		4	μs

6.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

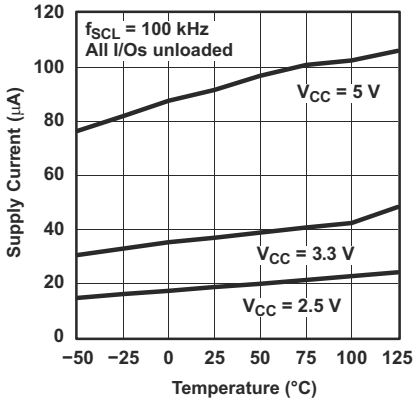


图 6-1. Supply Current vs Temperature

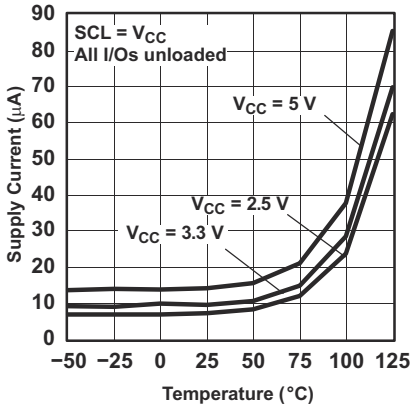


图 6-2. Standby Supply Current vs Temperature

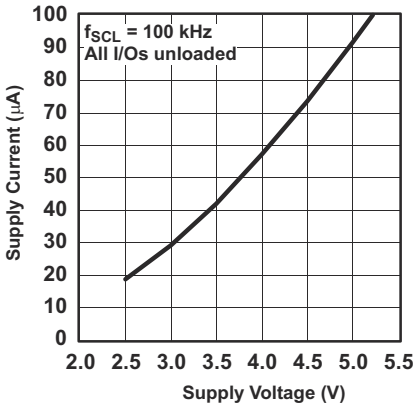


图 6-3. Supply Current vs Supply Voltage

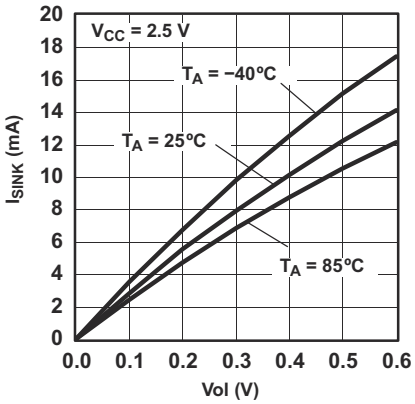


图 6-4. I/O Sink Current vs Output Low Voltage

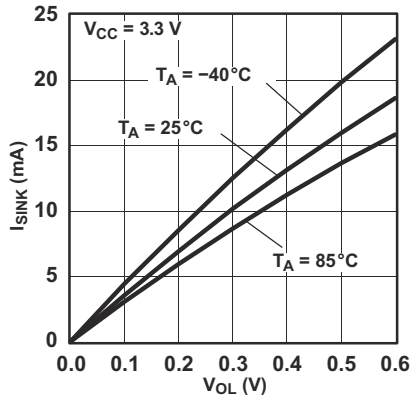


图 6-5. I/O Sink Current vs Output Low Voltage

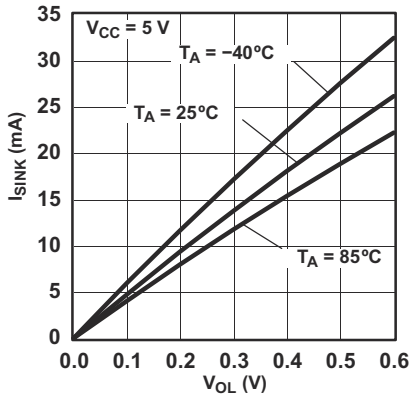


图 6-6. I/O Sink Current vs Output Low Voltage

6.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

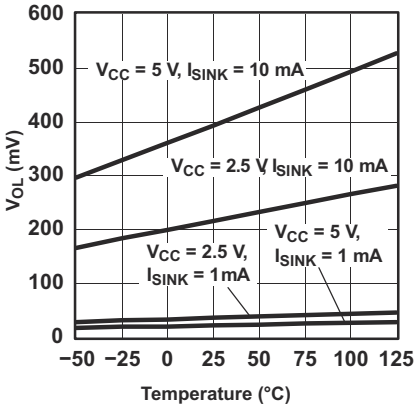


图 6-7. I/O Output Low Voltage vs Temperature

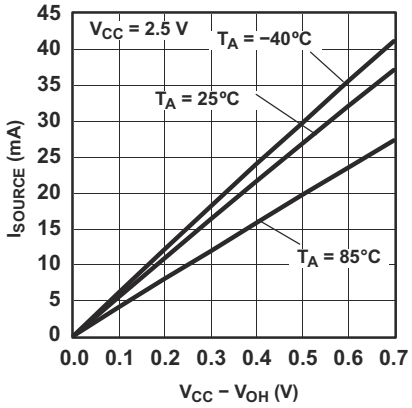


图 6-8. I/O Source Current vs Output High Voltage

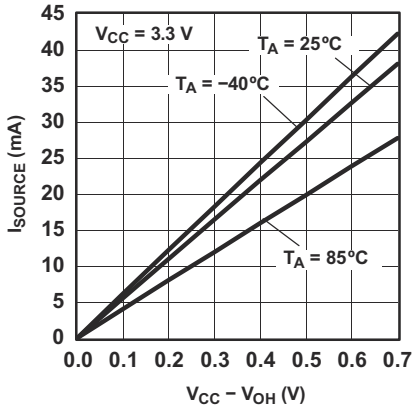


图 6-9. I/O Source Current vs Output High Voltage

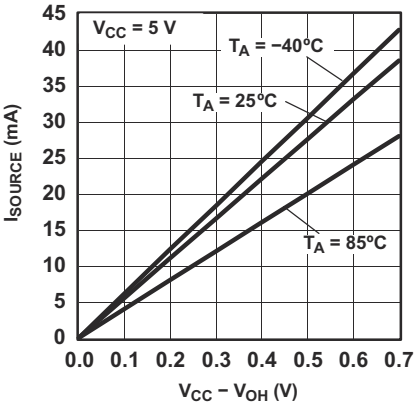


图 6-10. I/O Source Current vs Output High Voltage

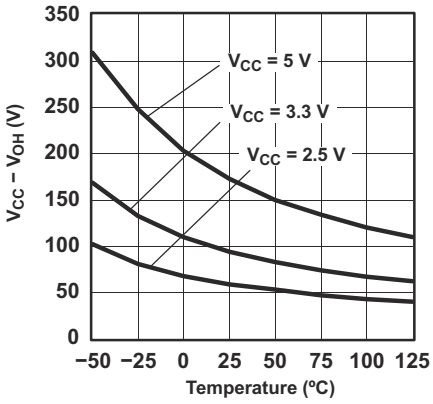


图 6-11. I/O High Voltage vs Temperature

7 Parameter Measurement Information

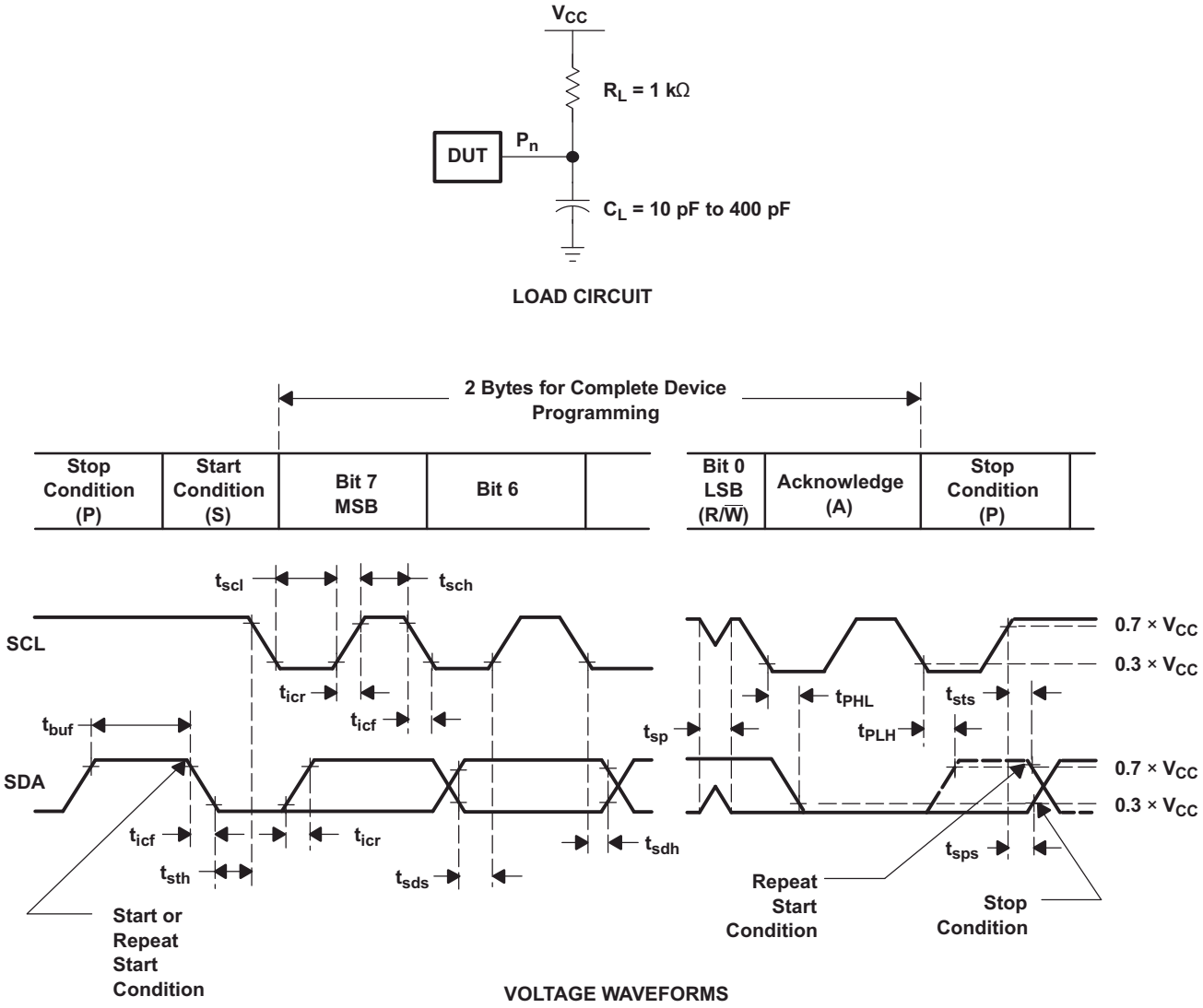


图 7-1. I²C Interface Load Circuit and Voltage Waveforms

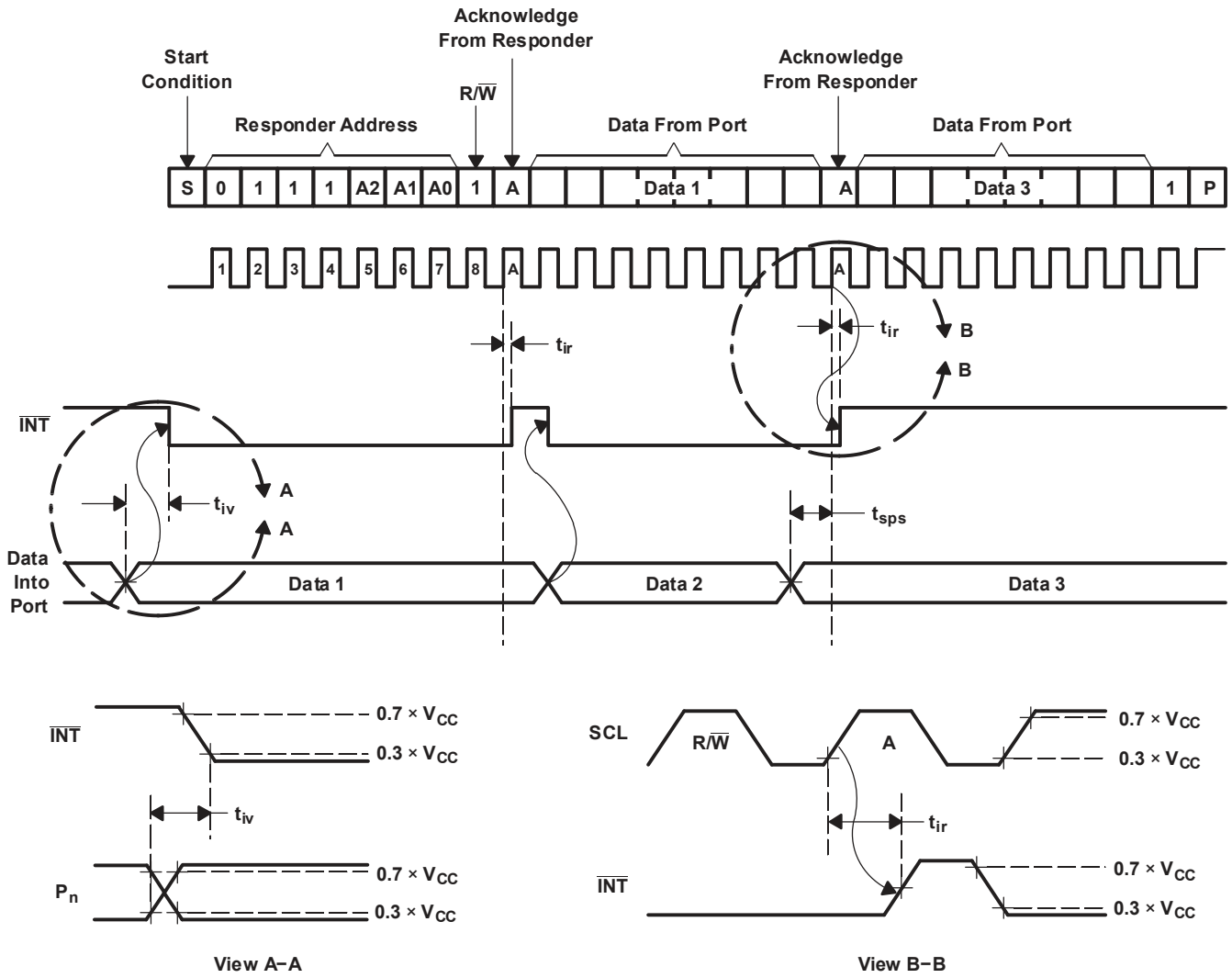


图 7-2. Interrupt Voltage Waveforms

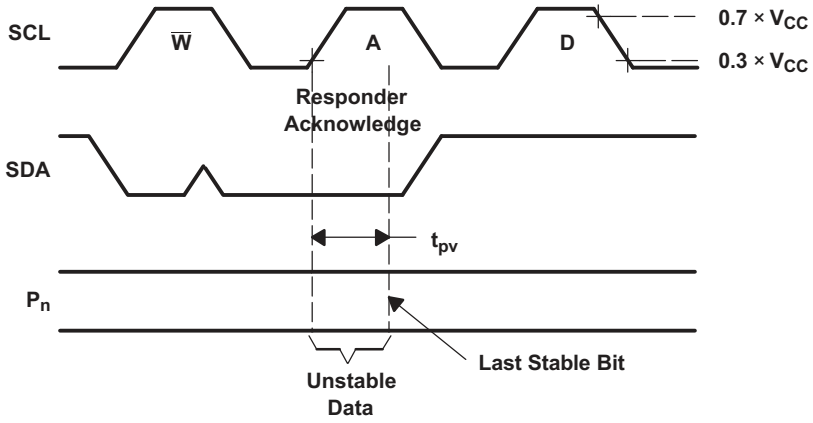


图 7-3. I²C Write Voltage Waveforms

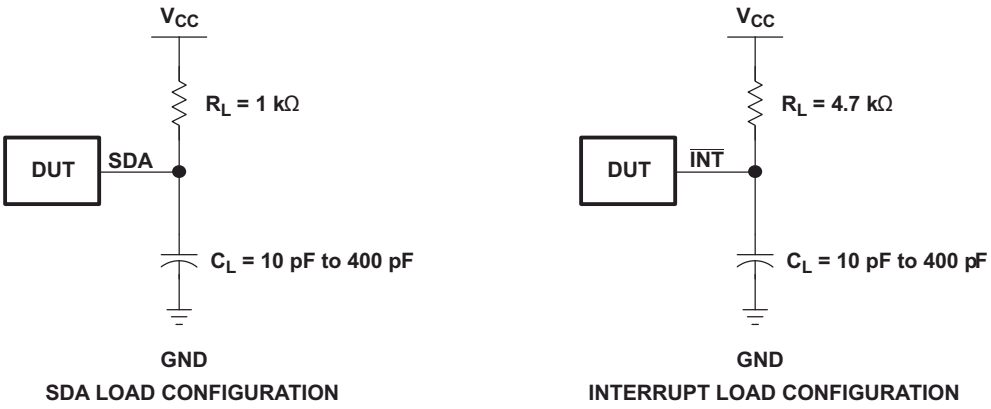


图 7-4. Load Circuits

8 Detailed Description

8.1 Overview

The PCF8574A device provides general-purpose remote I/O expansion for most microcontroller families via the I^2C interface [serial clock (SCL), serial data (SDA)].

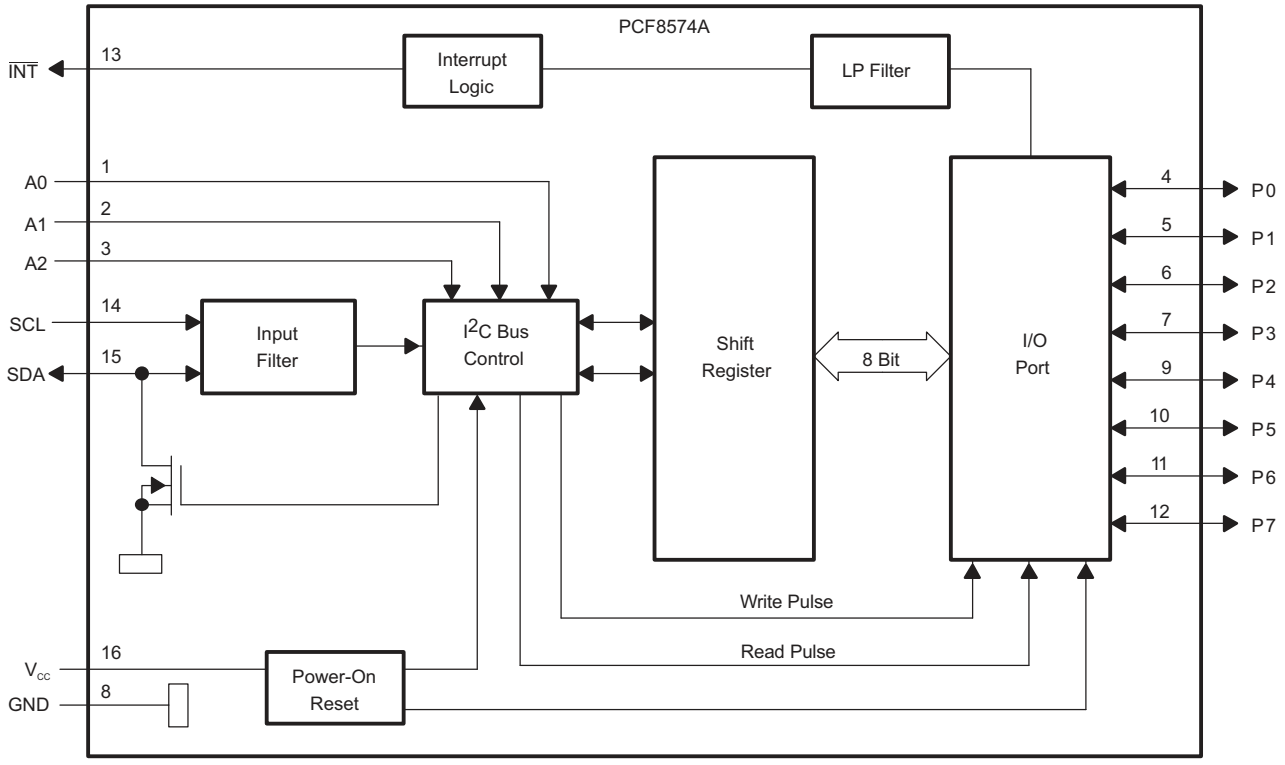
The device features an 8-bit quasi-bidirectional I/O port (P0 – P7), including latched outputs with high-current drive capability for directly driving LEDs. Each quasi-bidirectional I/O can be used as an input or output without the use of a data-direction control signal. At power on, the I/Os are high. In this mode, only a current source to V_{CC} is active. An additional strong pullup to V_{CC} allows fast rising edges into heavily loaded outputs. This device turns on when an output is written high and is switched off by the negative edge of SCL. The I/Os should be high before being used as inputs.

The PCF8574A device provides an open-drain output ($\overline{INT}$) that can be connected to the interrupt input of a microcontroller. An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv}, $\overline{INT}$ is valid. Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from, or written to, the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge bit after the rising edge of the SCL signal, or in the write mode at the acknowledge bit after the high-to-low transition of the SCL signal. Interrupts that occur during the acknowledge clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and, after the next rising clock edge, is transmitted as $\overline{INT}$. Reading from, or writing to, another device does not affect the interrupt circuit.

By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^2C bus. Therefore, the PCF8574A device can remain a simple responder device.

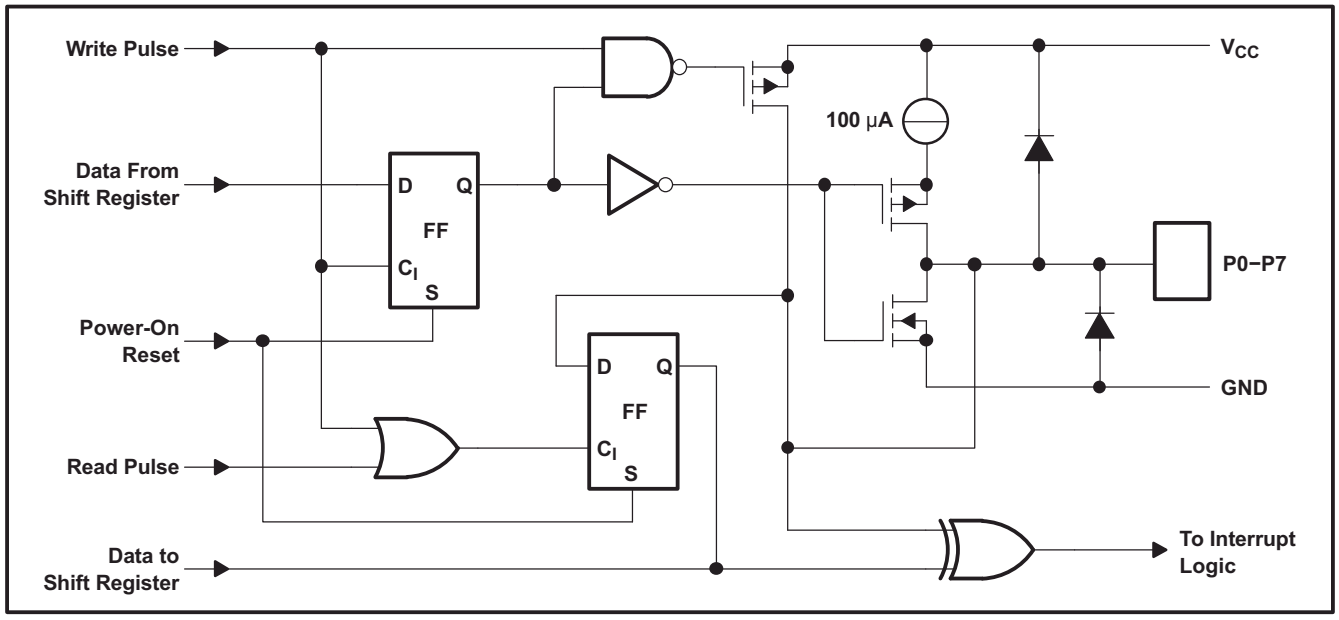
8.2 Functional Block Diagram

8.2.1 Simplified Block Diagram of Device



Pin numbers shown are for the DW and N packages.

8.2.2 Simplified Schematic Diagram of Each P-Port Input/Output



8.3 Feature Description

8.3.1 I²C Interface

I²C communication with this device is initiated by a commander sending a start condition, a high-to-low transition on the SDA I/O while the SCL input is high. After the start condition, the device address byte is sent, most-significant bit (MSB) first, including the data direction bit (R/ $\overline{W}$). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an acknowledge, a low on the SDA I/O during the high of the acknowledge-related clock pulse. The address inputs (A0 – A2) of the responder device must not be changed between the start and the stop conditions.

The data byte follows the address acknowledge. If the R/ $\overline{W}$ bit is high, the data from this device are the values read from the P port. If the R/ $\overline{W}$ bit is low, the data are from the commander, to be output to the P port. The data byte is followed by an acknowledge sent from this device. If other data bytes are sent from the commander, following the acknowledge, they are ignored by this device. Data are output only if complete bytes are received and acknowledged. The output data will be valid at time, t_{pv}, after the low-to-high transition of SCL and during the clock cycle for the acknowledge.

A stop condition, a low-to-high transition on the SDA I/O while the SCL input is high, is sent by the commander.

8.3.2 Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C responder address	L	H	H	H	A2	A1	A0	R/ $\overline{W}$
I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

8.3.3 Address Reference

INPUTS			I²C BUS responder 8-BIT READ ADDRESS	I²C BUS responder 8-BIT WRITE ADDRESS
A2	A1	A0		
L	L	L	113 (dec), 71 (hex)	112 (dec), 70 (hex)
L	L	H	115 (dec), 73 (hex)	114 (dec), 72 (hex)
L	H	L	117 (dec), 75 (hex)	116 (dec), 74 (hex)
L	H	H	119 (dec), 77 (hex)	118 (dec), 76 (hex)
H	L	L	121 (dec), 79 (hex)	120 (dec), 78 (hex)
H	L	H	123 (dec), 7B (hex)	122 (dec), 7A (hex)
H	H	L	125 (dec), 7D (hex)	124 (dec), 7C (hex)
H	H	H	127 (dec), 7F (hex)	126 (dec), 7E (hex)

8.4 Device Functional Modes

图 8-1 and 图 8-2 show the address and timing diagrams for the write and read modes, respectively.

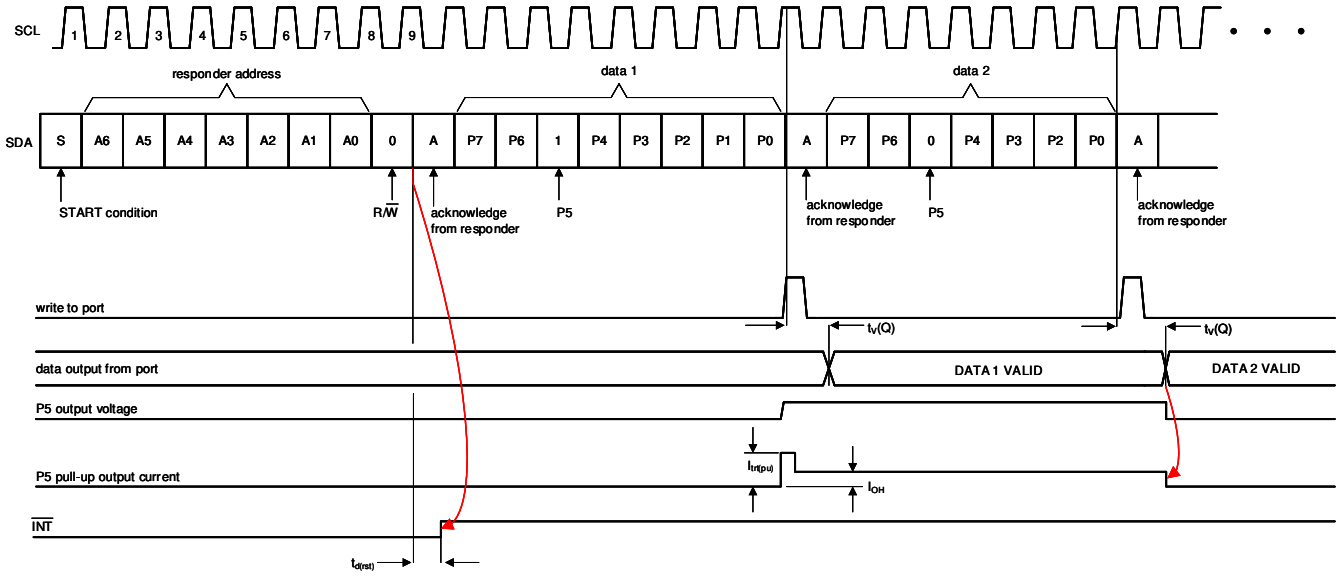
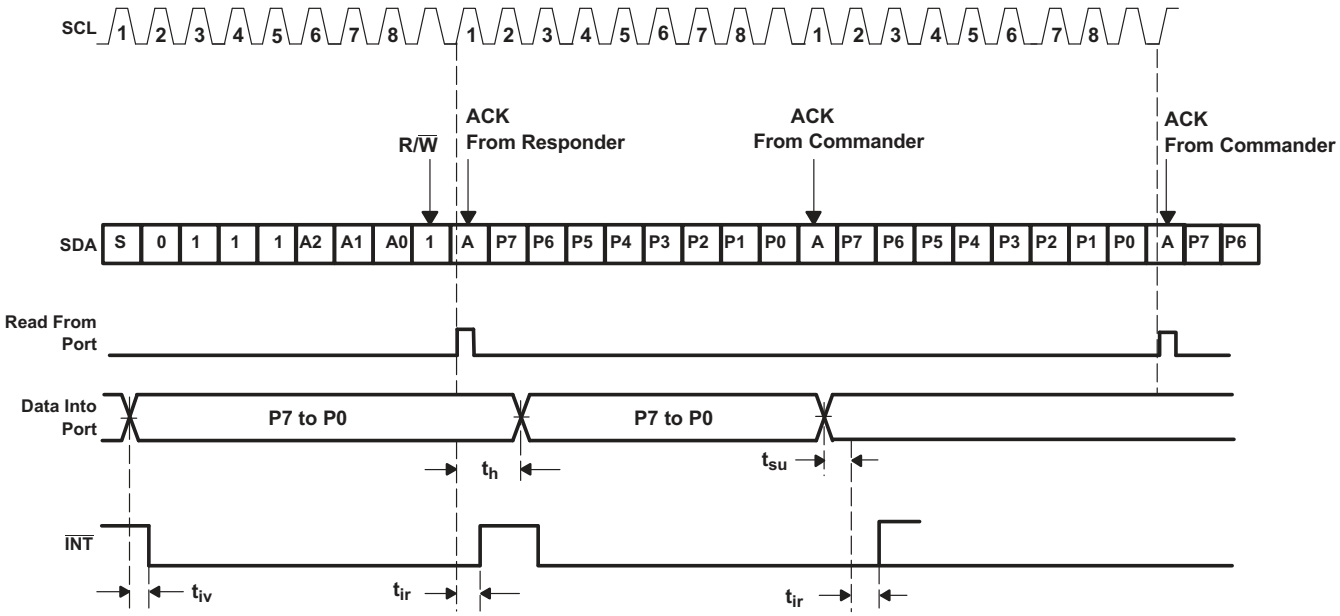


图 8-1. Write Mode (Output)



A. A low-to-high transition of SDA while SCL is high is defined as the stop condition (P). The transfer of data can be stopped at any moment bya stop condition. When this occurs, data present at the latest ACK phase is valid (output mode). Input data is lost.

图 8-2. Read Mode (Input)

9 Application Information Disclaimer

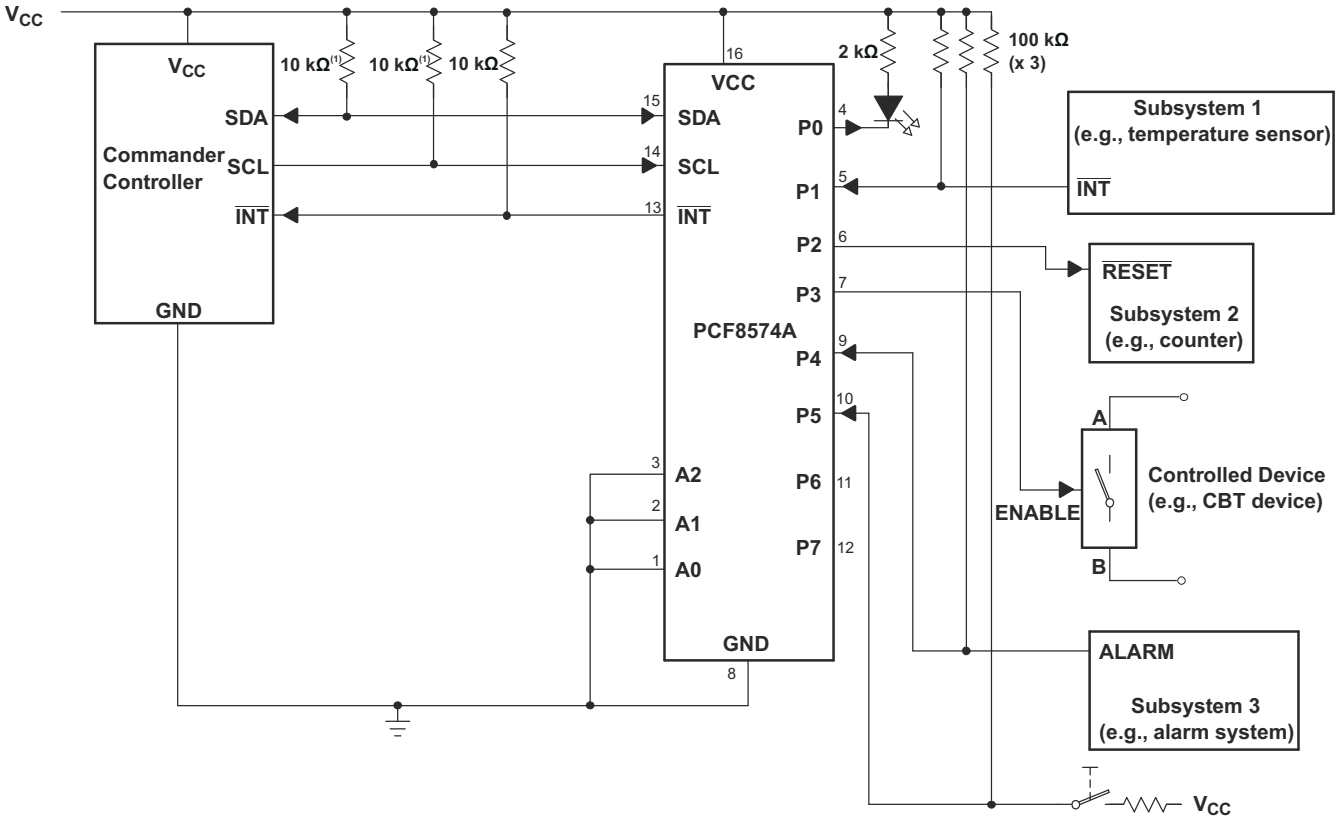
Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

图 9-1 shows an application in which the PCF8574A device can be used.

9.2 Typical Application



A. The SCL and SDA pins must be pulled up to V_{CC} because if SCL and SDA are pulled up to an auxiliary power supply that could be powered on while V_{CC} is powered off, then the supply current, I_{CC}, will increase as a result.
B. Device address is configured as 0111000 for this example.
C. P0, P2, and P3 are configured as outputs.
D. P1, P4, and P5 are configured as inputs.
E. P6 and P7 are not used and must be configured as outputs.

图 9-1. Application Schematic

9.2.1 Design Requirements

9.2.1.1 Minimizing I_{CC} When I/Os Control LEDs

When the I/Os are used to control LEDs, normally they are connected to V_{CC} through a resistor as shown in 图 11-1. For a P-port configured as an input, I_{CC} increases as V_I becomes lower than V_{CC}. The LED is a diode, with threshold voltage V_T, and when a P-port is configured as an input the LED will be off but V_I is a V_T drop below V_{CC}.

For battery-powered applications, it is essential that the voltage of P-ports controlling LEDs is greater than or equal to V_{CC} when the P-ports are configured as input to minimize current consumption. 图 9-2 shows a high-value resistor in parallel with the LED. 图 9-3 shows V_{CC} less than the LED supply voltage by at least V_T. Both of these methods maintain the I/O V_I at or above V_{CC} and prevents additional supply current consumption when the P-port is configured as an input and the LED is off.

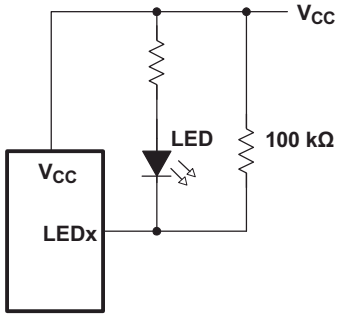


图 9-2. High-Value Resistor in Parallel With LED

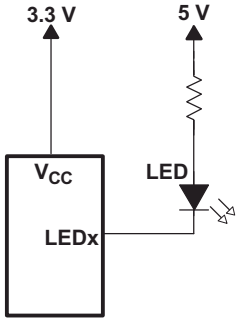


图 9-3. Device Supplied by a Lower Voltage

9.2.2 Detailed Design Procedure

The pull-up resistors, R_P, for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all responders on the I^2C bus. The minimum pull-up resistance is a function of V_{CC}, $V_{OL,(max)}$, and I_{OL}:

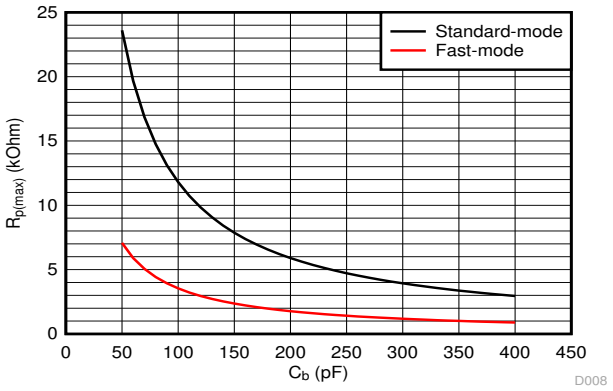
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, f_{SCL} = 400 kHz) and bus capacitance, C_b:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I^2C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the PCF8574A device, C_i for SCL or C_{io} for SDA, the capacitance of wires/connections/traces, and the capacitance of additional responders on the bus.

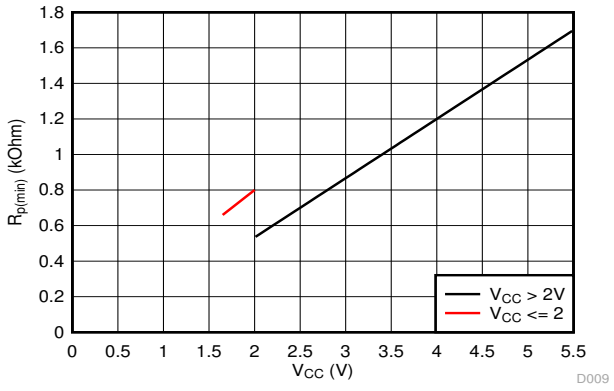
9.2.3 Application Curves



Standard-mode (f_{SCL}= 100 kHz, t_r = 1 µs)

Fast-mode (f_{SCL}= 400 kHz, t_r= 300 ns)

图 9-4. Maximum Pull-Up Resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



V_{OL} = 0.2*V_{CC}, I_{OL} = 2 mA when $V_{CC} \leqslant$ 2 V

V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{CC} > 2 V

图 9-5. Minimum Pull-Up Resistance ($R_{p(min)}$) vs Pull-Up Reference Voltage (V_{CC})

10 Power Supply Recommendations

10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, PCF8574A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in 图 10-1 and 图 10-2.

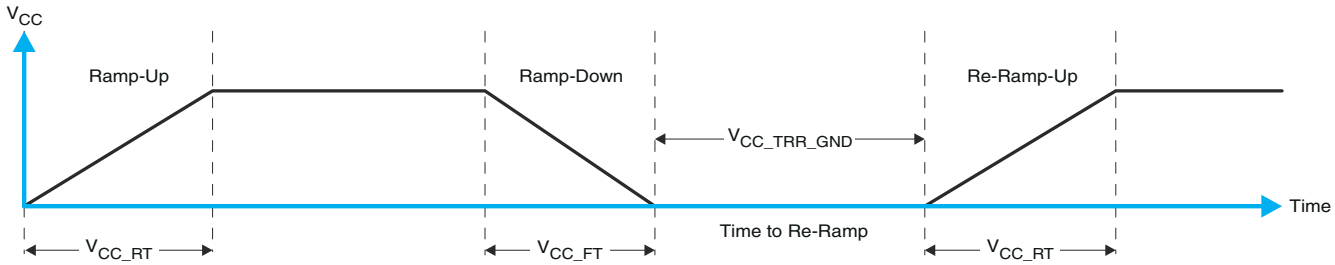


图 10-1. V_{CC} is Lowered Below 0.2 V or 0 V and Then Ramped Up to V_{CC}

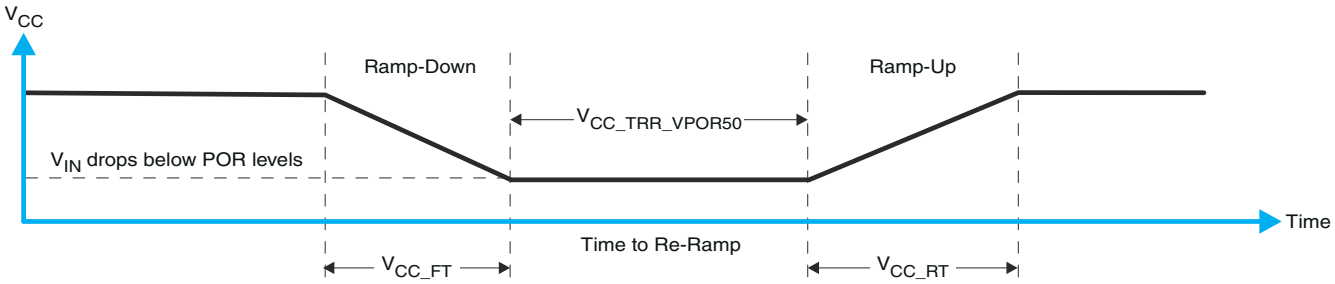


图 10-2. V_{CC} is Lowered Below the POR Threshold, Then Ramped Back Up to V_{CC}

表 10-1 specifies the performance of the power-on reset feature for PCF8574A for both types of power-on reset.

表 10-1. Recommended Supply Sequencing and Ramp Rates(1)

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall rate	See 图 10-1	1		100	ms
V_{CC_RT}	Rise rate	See 图 10-1	0.01		100	ms
$V_{CC\_TRR\_GND}$	Time to re-ramp (when V_{CC} drops to GND)	See 图 10-1	0.001			ms
$V_{CC\_TRR\_POR50}$	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50 mV)	See 图 10-2	0.001			ms
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when V_{CCX_GW} = 1 μs	See 图 10-3			1.2	V
V_{CC_GW}	Glitch width that will not cause a functional disruption when V_{CCX_GH} = 0.5 × V_{CCx}	See 图 10-3				μs
V_{PORF}	Voltage trip point of POR on falling V_{CC}		0.767		1.144	V
V_{PORR}	Voltage trip point of POR on fising V_{CC}		1.033		1.428	V

(1) T_A = –40°C to 85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. 图 10-3 and 表 10-1 provide more information on how to measure these specifications.

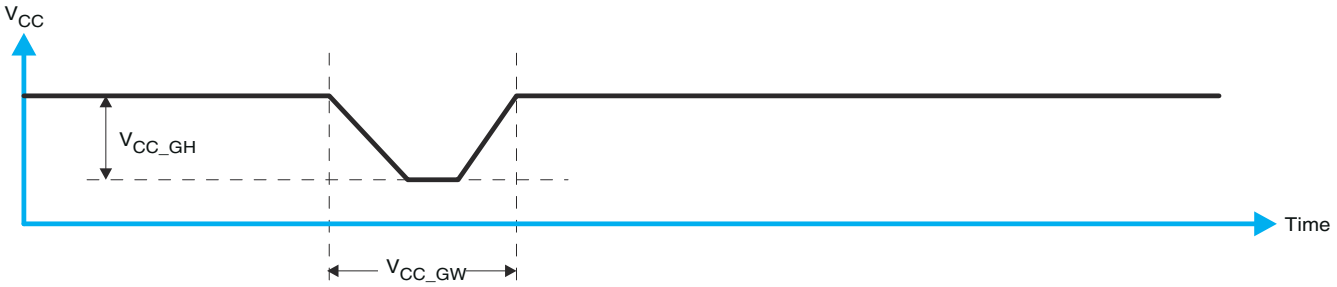


图 10-3. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. 图 10-4 and 表 10-1 provide more details on this specification.

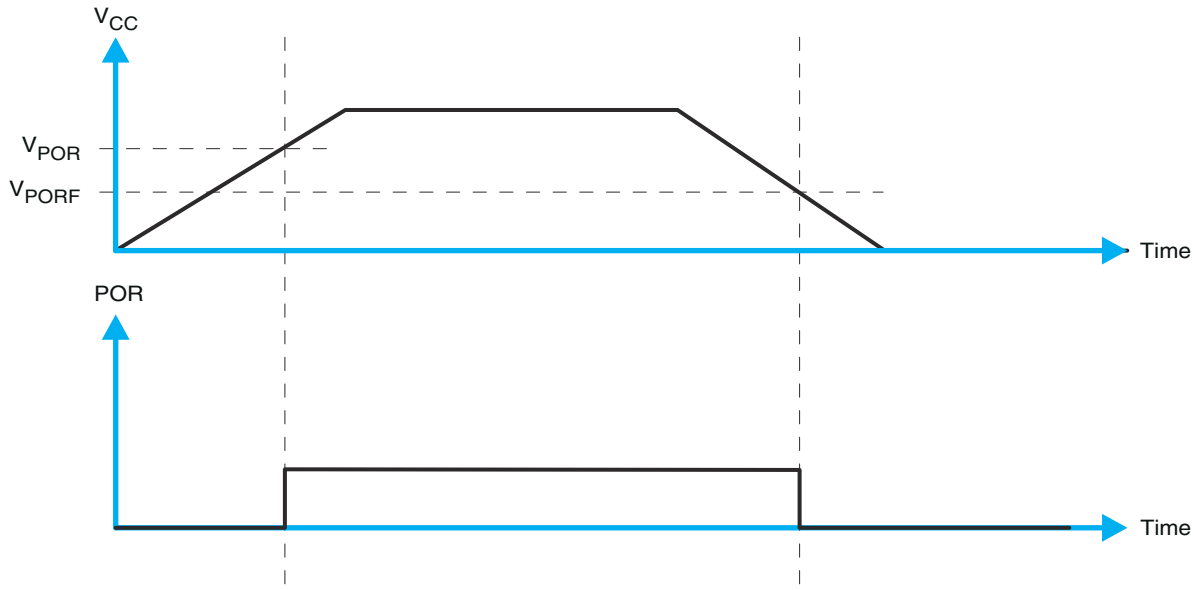


图 10-4. V_{POR}

11 Layout

11.1 Layout Guidelines

For printed circuit board (PCB) layout of PCF8574A, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I2C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the V_{CC} pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors should be placed as close to the PCF8574A device as possible. These best practices are shown in 图 11-1.

For the layout example provided in 图 11-1, it would be possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (V_{CC}) and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to VCC or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in 图 11-1.

11.2 Layout Example

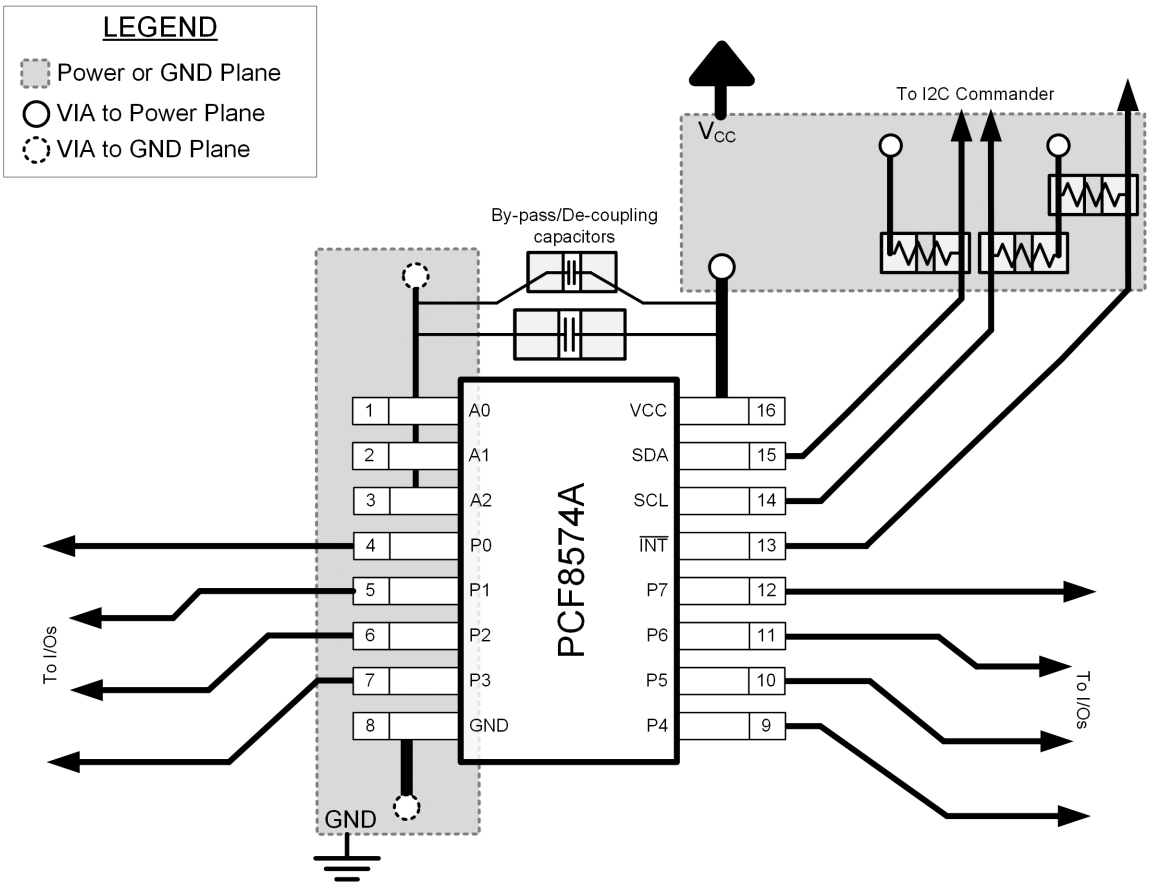


图 11-1. Layout Example for PCF8574A

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Glossary

SLYZ022 — *TI Glossary.*

This glossary lists and explains terms, acronyms and definitions.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCF8574ADGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574A	Samples
PCF8574ADGVRG4	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574A	Samples
PCF8574ADW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8574A	Samples
PCF8574ADWE4	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8574A	Samples
PCF8574ADWG4	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8574A	Samples
PCF8574ADWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8574A	Samples
PCF8574AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	PCF8574AN	Samples
PCF8574ANE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	PCF8574AN	Samples
PCF8574APW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574A	Samples
PCF8574APWG4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574A	Samples
PCF8574APWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574A	Samples
PCF8574APWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574A	Samples
PCF8574APWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574A	Samples
PCF8574ARGYR	ACTIVE	VQFN	RGY	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PF574A	Samples
PCF8574ARGYRG4	ACTIVE	VQFN	RGY	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PF574A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

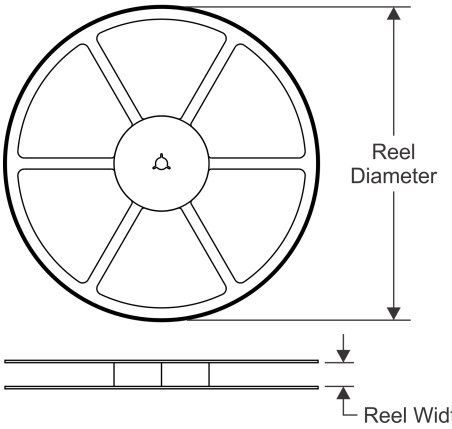
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

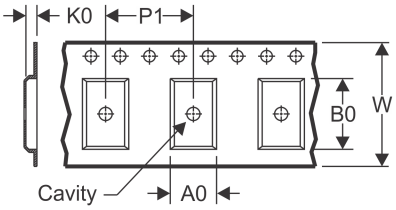
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

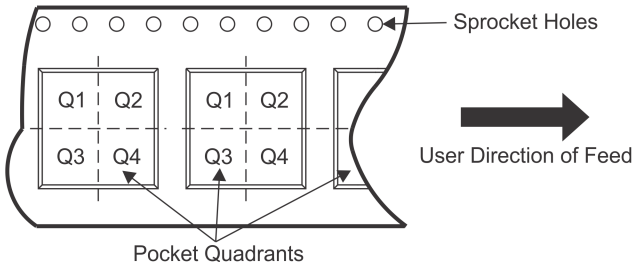


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

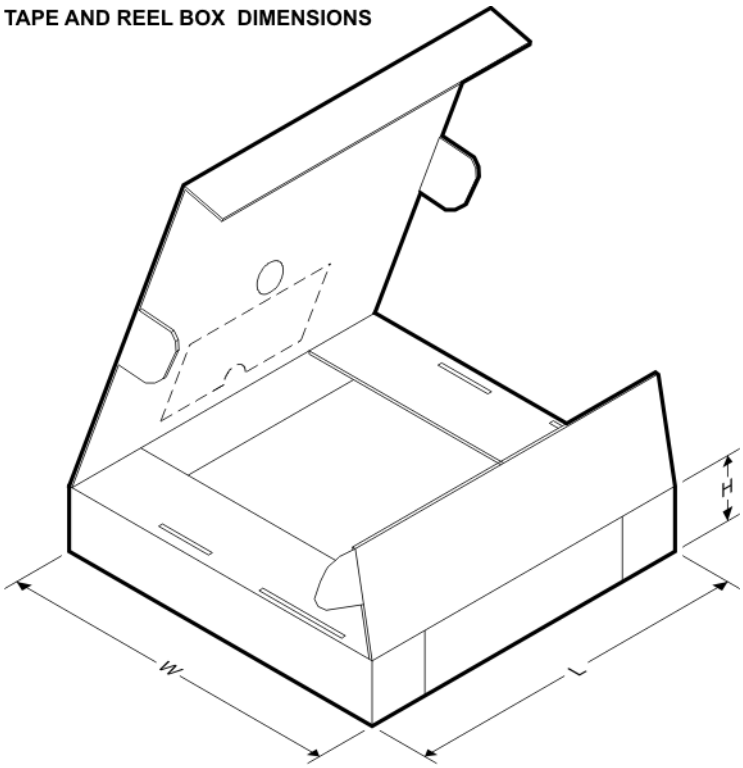
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCF8574ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCF8574ADWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
PCF8574APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
PCF8574ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

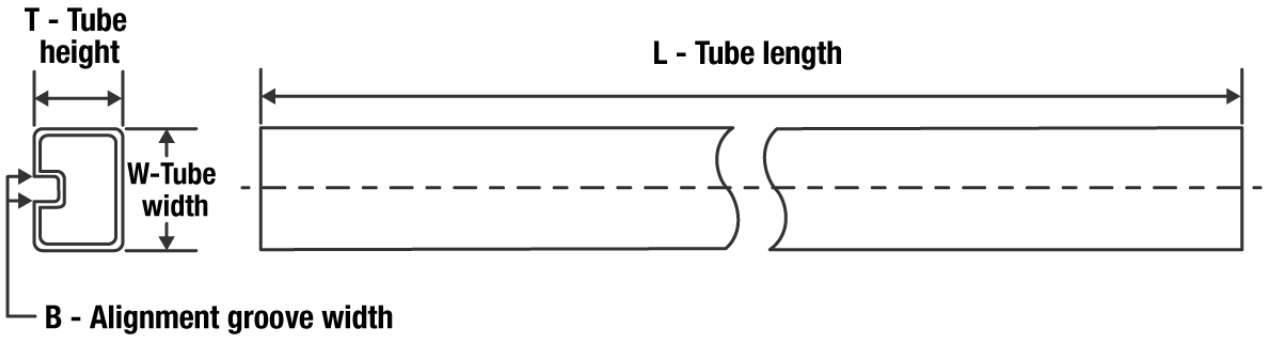
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCF8574ADGVR	TVSOP	DGV	20	2000	853.0	449.0	35.0
PCF8574ADWR	SOIC	DW	16	2000	350.0	350.0	43.0
PCF8574APWR	TSSOP	PW	20	2000	853.0	449.0	35.0
PCF8574ARGYR	VQFN	RGY	20	3000	853.0	449.0	35.0

TUBE



*All dimensions are nominal

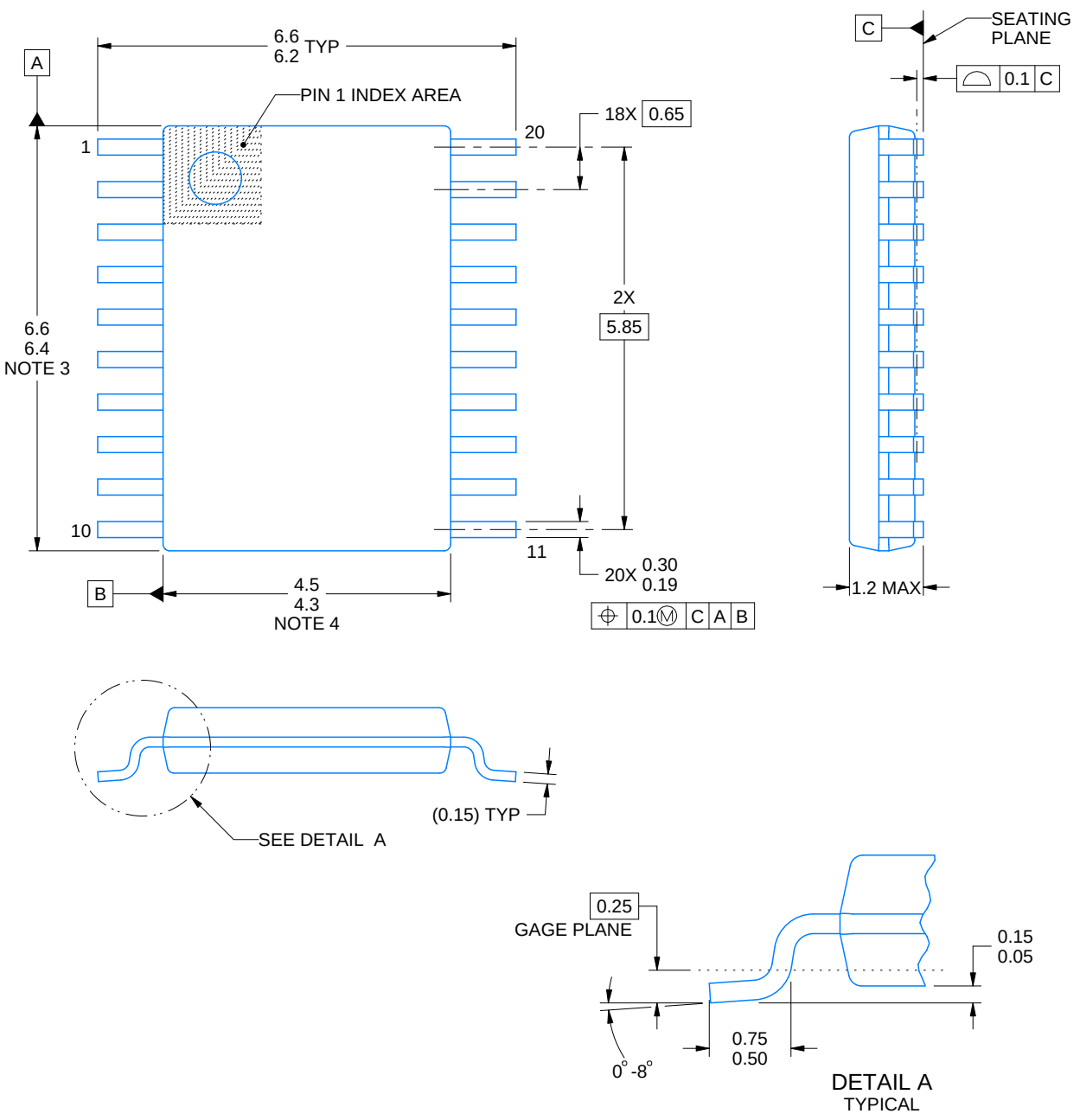
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PCF8574ADW	DW	SOIC	16	40	506.98	12.7	4826	6.6
PCF8574ADWE4	DW	SOIC	16	40	506.98	12.7	4826	6.6
PCF8574ADWG4	DW	SOIC	16	40	506.98	12.7	4826	6.6
PCF8574AN	N	PDIP	16	25	506	13.97	11230	4.32
PCF8574ANE4	N	PDIP	16	25	506	13.97	11230	4.32
PCF8574APW	PW	TSSOP	20	70	530	10.2	3600	3.5
PCF8574APWG4	PW	TSSOP	20	70	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0020A

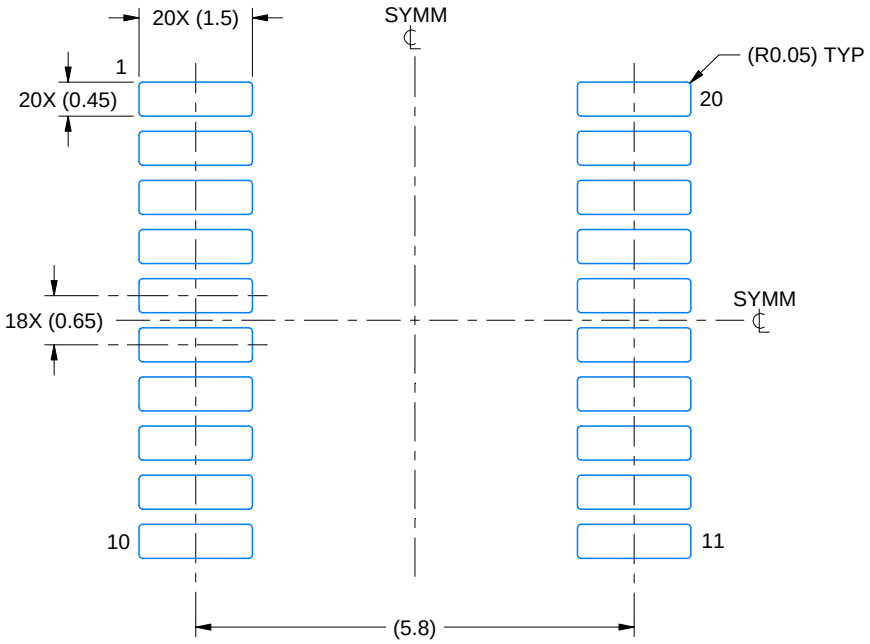
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



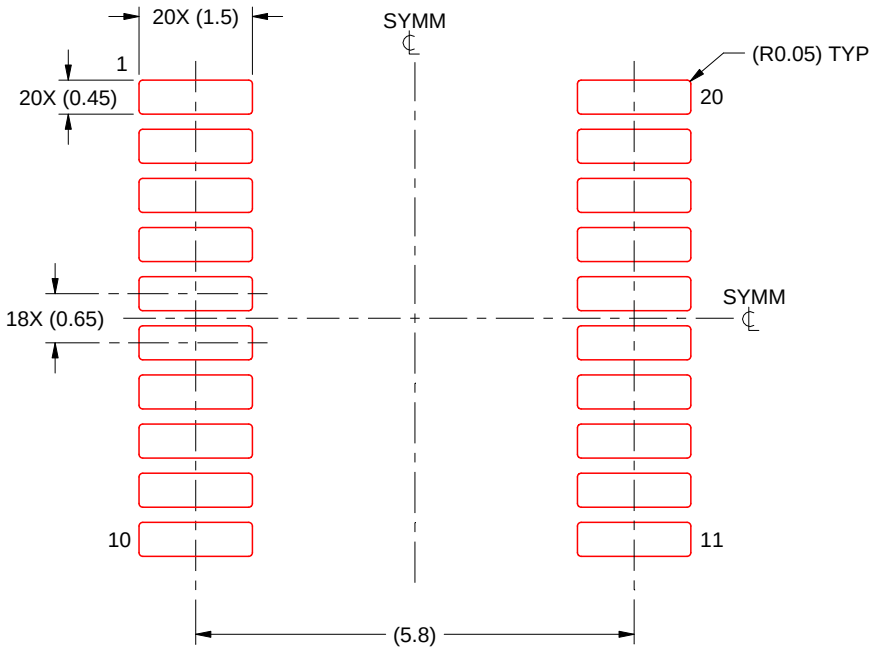
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



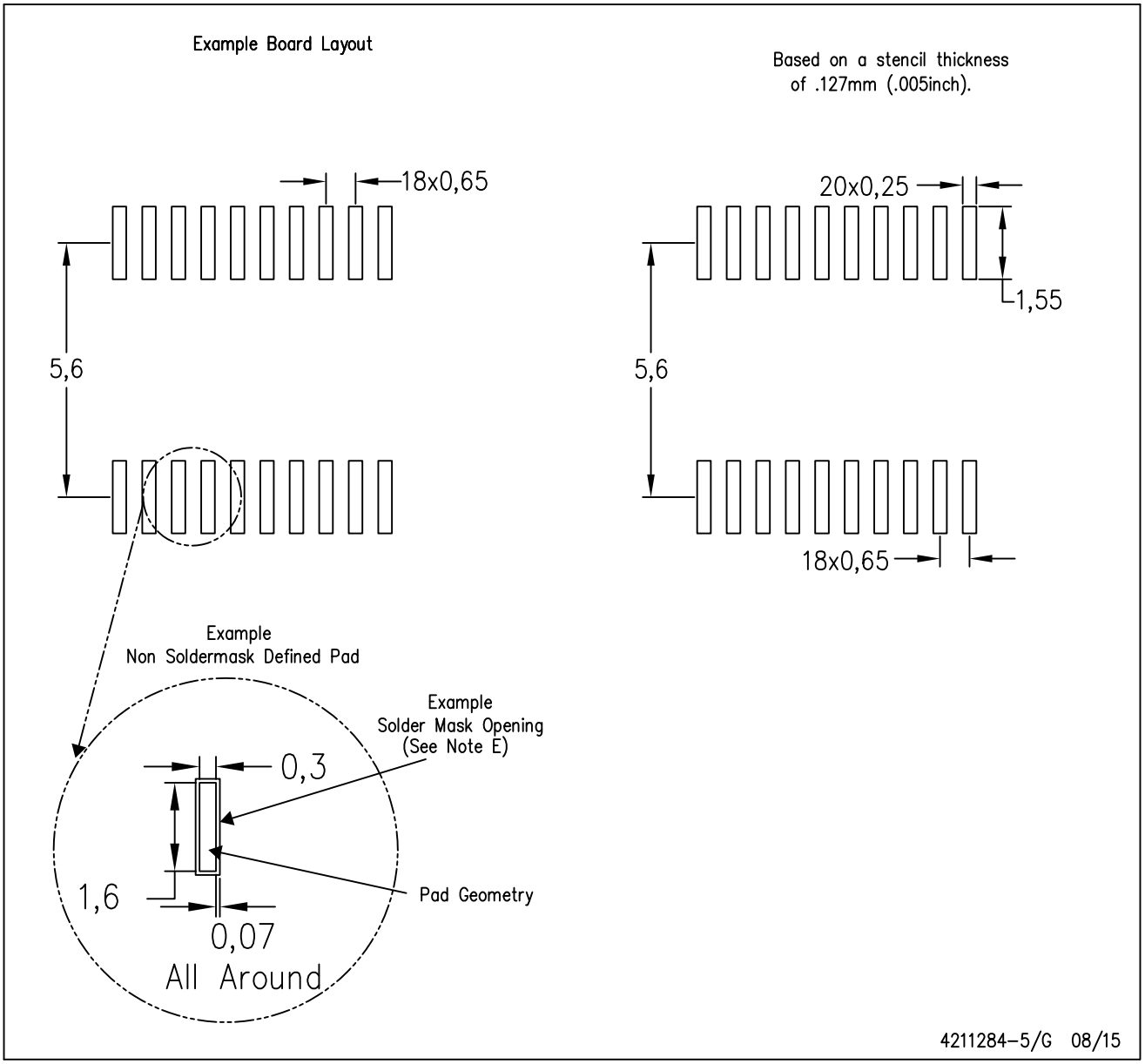
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

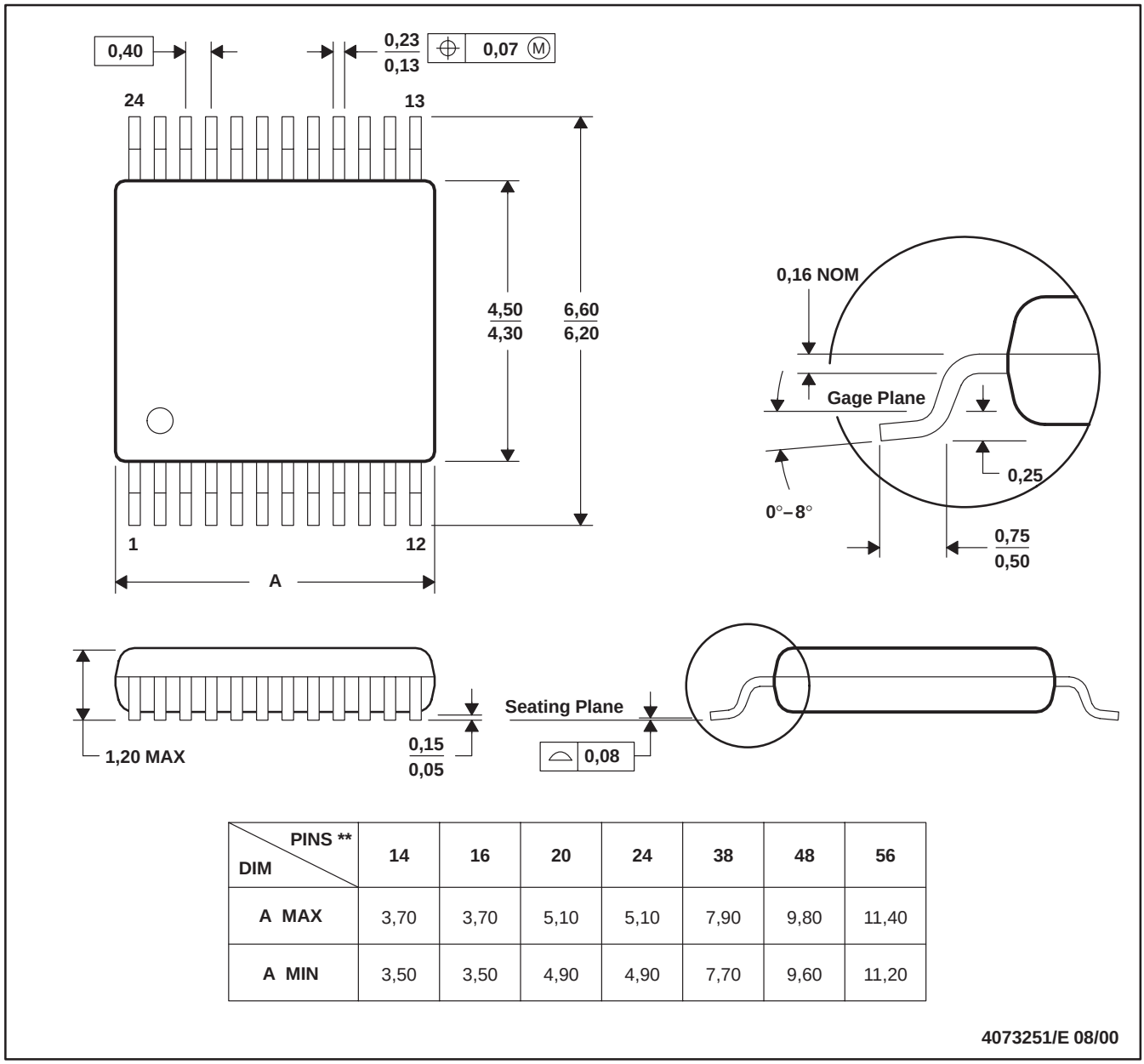
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

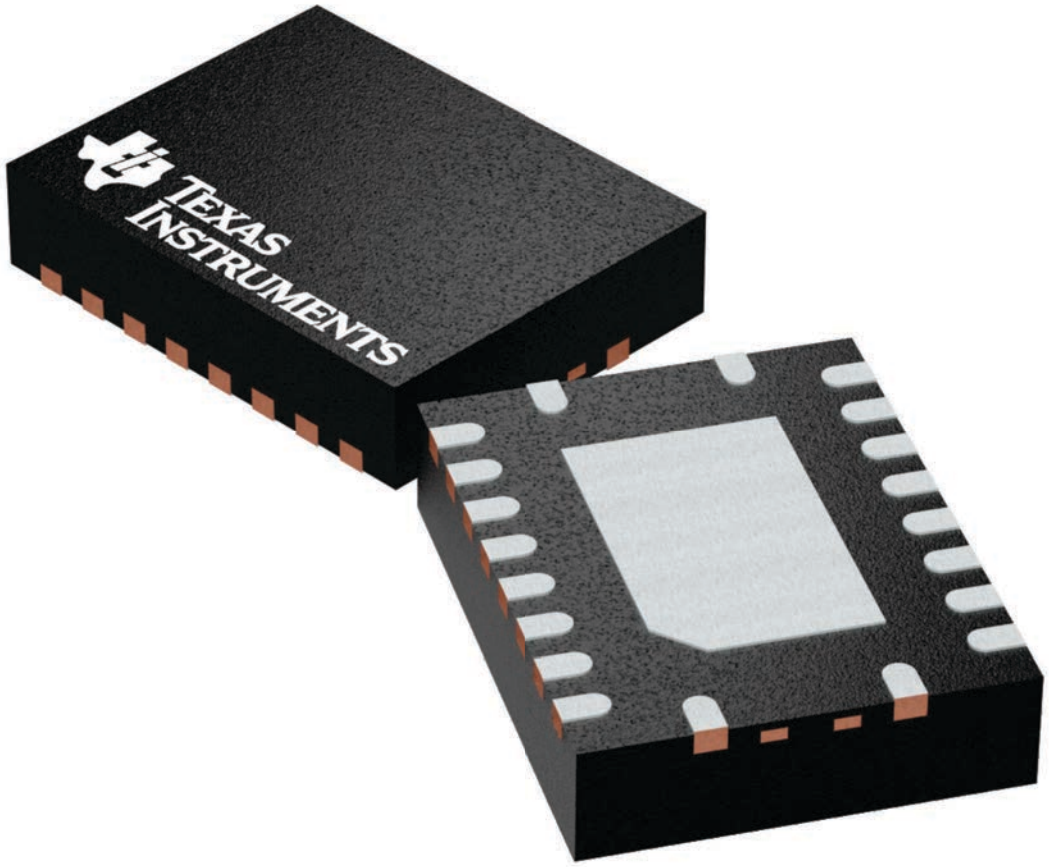
RGY 20

VQFN - 1 mm max height

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



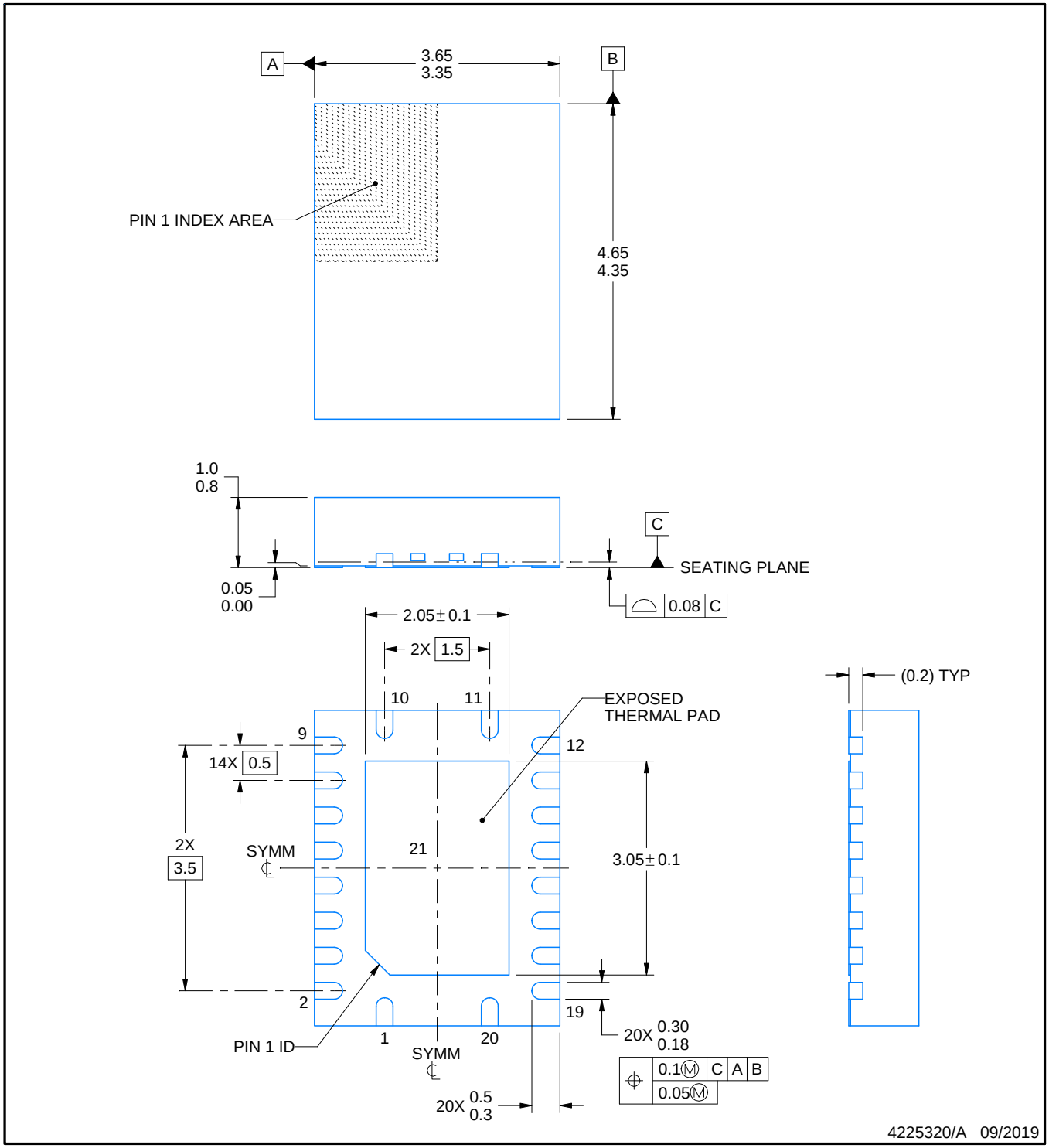
4225264/A

PACKAGE OUTLINE

RGY0020A

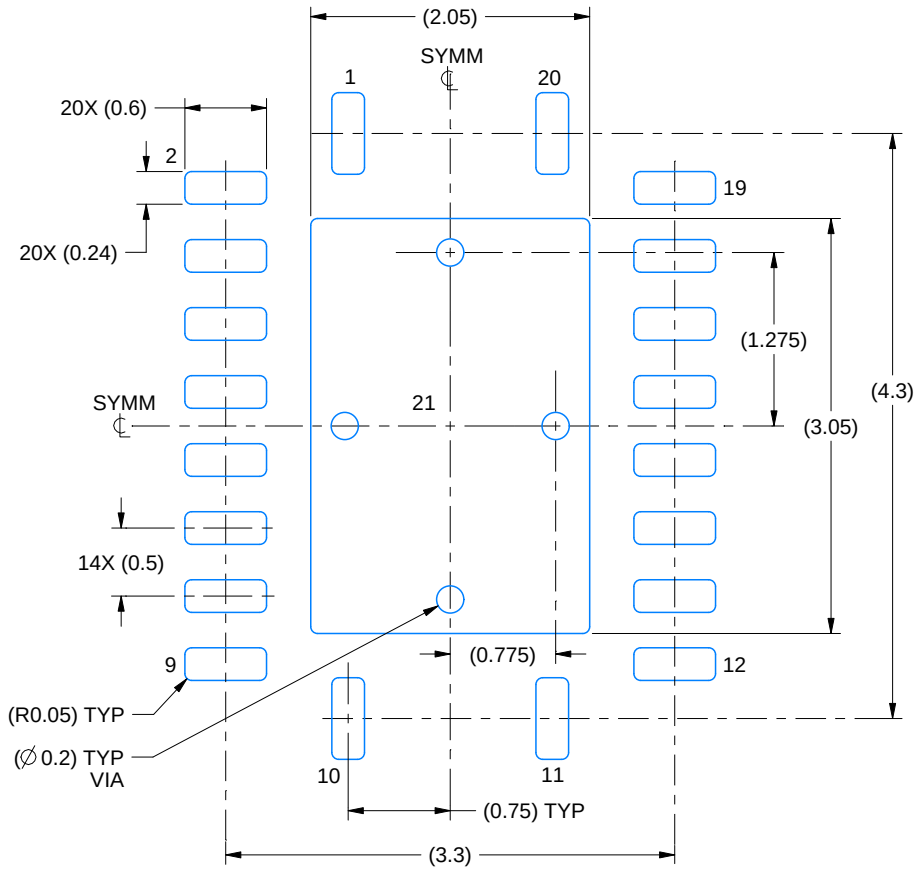
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

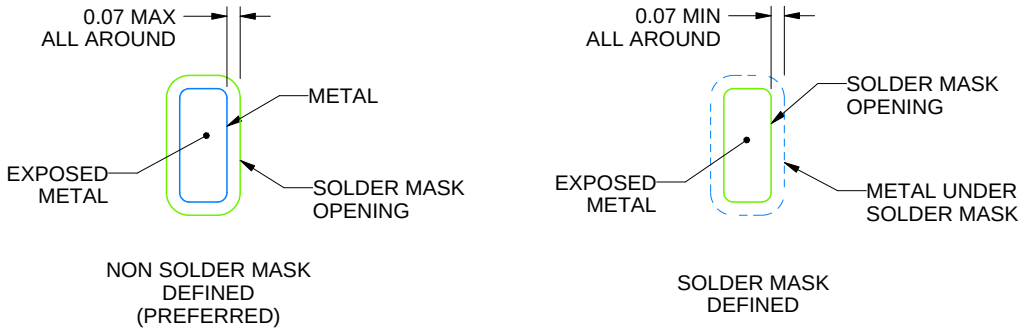


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

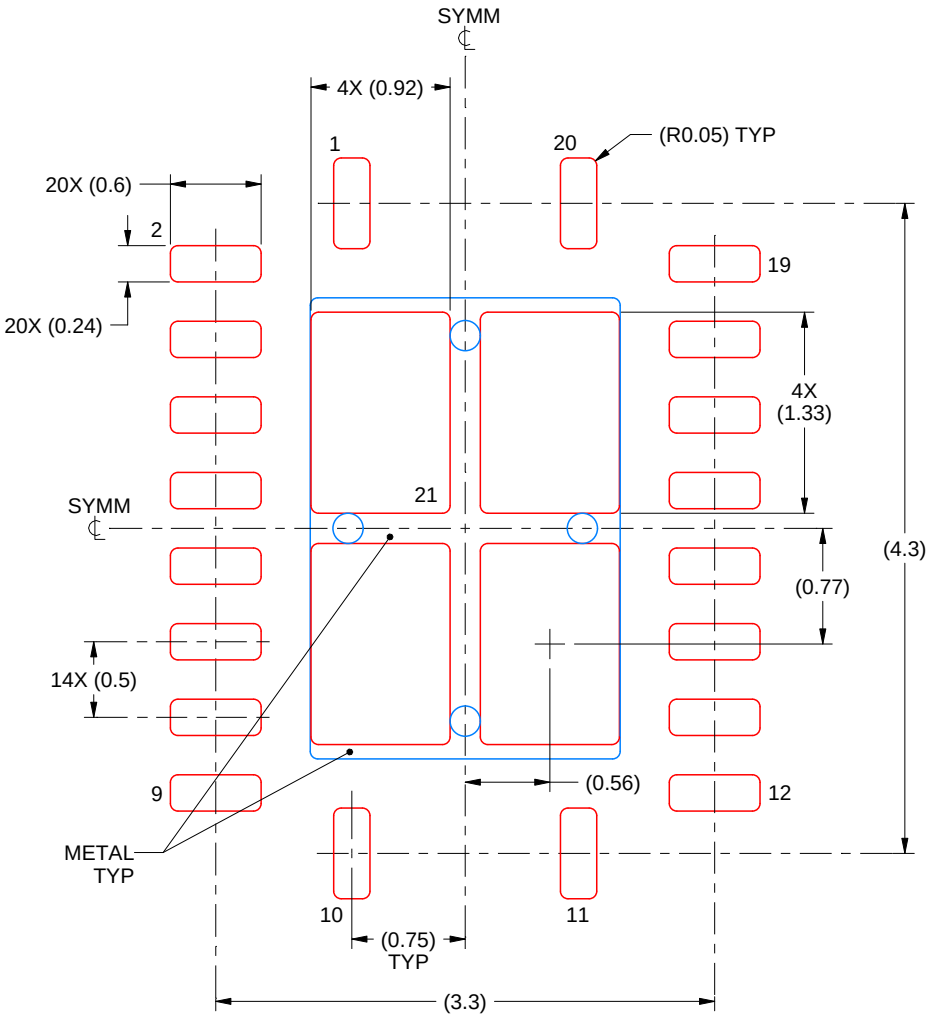


SOLDER MASK DETAILS

4225320/A 09/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

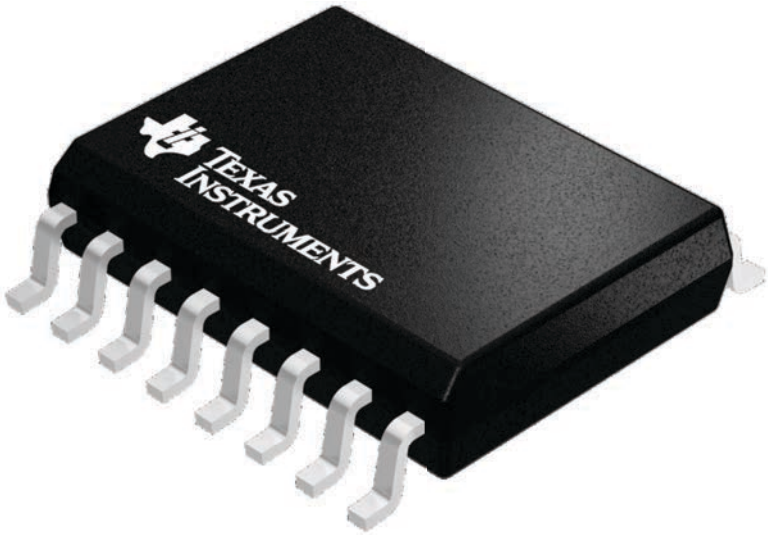
DW 16

SOIC - 2.65 mm max height

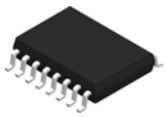
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

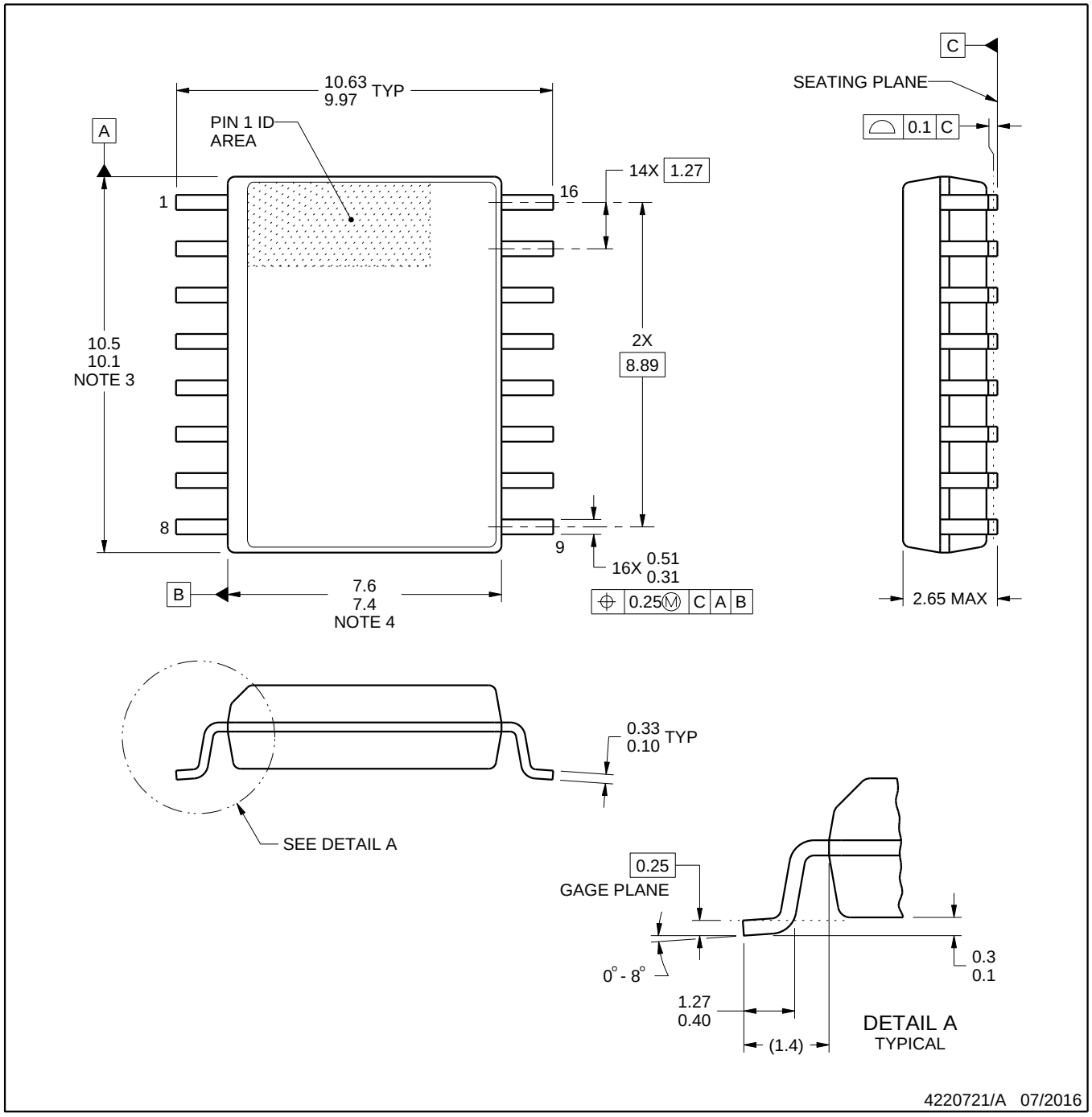


PACKAGE OUTLINE

DW0016A

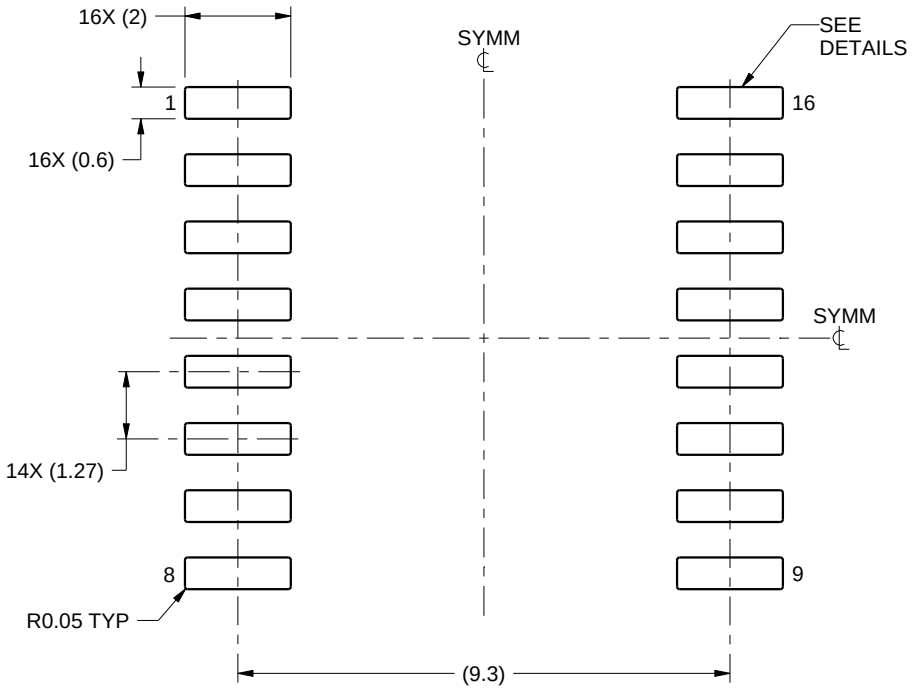
SOIC - 2.65 mm max height

SOIC

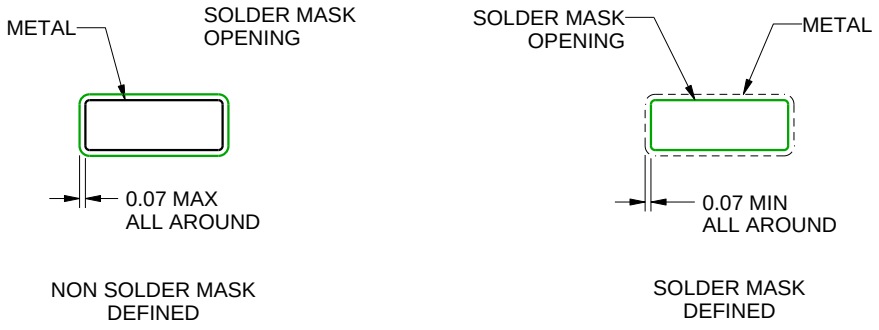


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

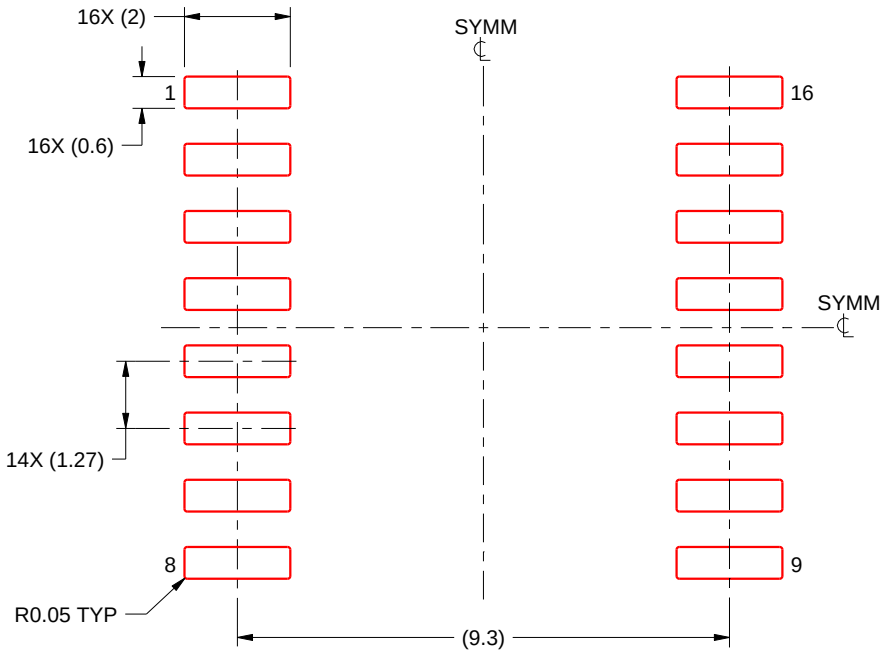


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

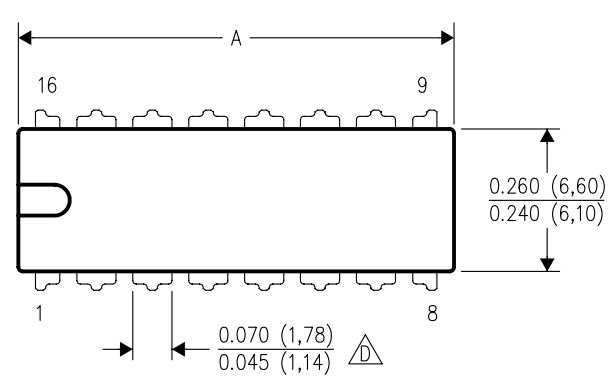
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

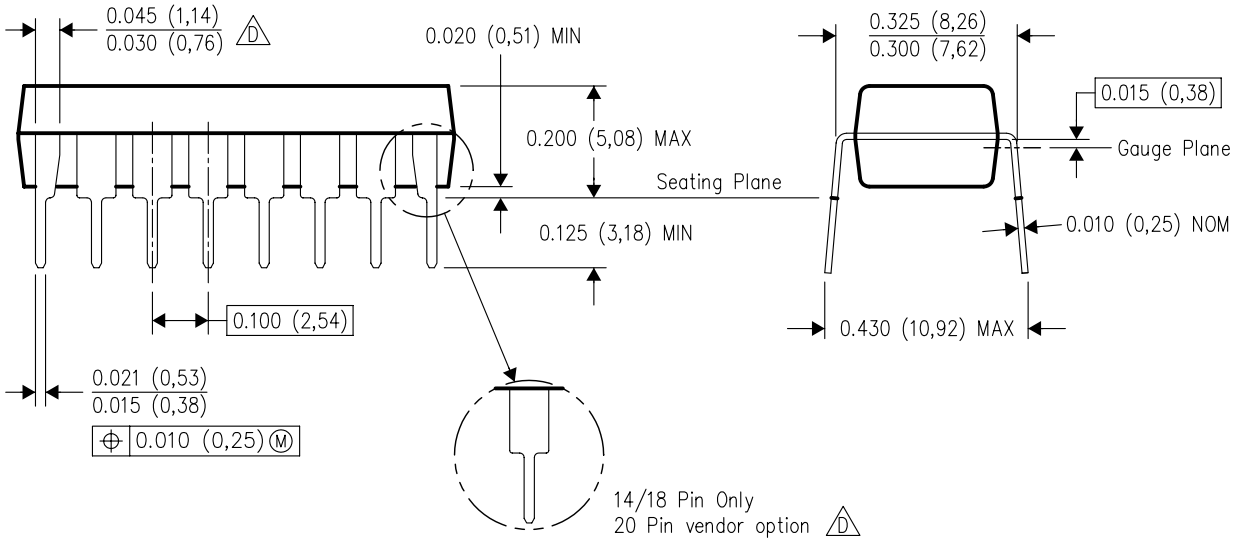
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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