

# MSP432E401Y SimpleLink™ 以太网微控制器

## 1 器件概述

### 1.1 特性

- 内核
  - 120MHz ARM® Cortex®- 具有浮点运算单元 (FPU) 的 M4F 处理器内核
- 连接
  - 以太网 MAC: 具有集成以太网 PHY 的 10/100 以太网 MAC
  - 以太网 PHY: 具有 IEEE 1588 PTP 硬件支持的 PHY
  - 通用串行总线 (USB): 具有 ULPI 接口选项和链路层电源管理 (LPM) 的 USB 2.0 OTG、主机或器件
  - 8 个通用异步接收器/发射器 (UART), 每个具有独立计时的发送器和接收器
  - 4 个四通道同步串行接口 (QSSI): 提供双通道、四通道和高级 SSI 支持
  - 提供高速模式支持的 10 个内部集成电路 (I<sup>2</sup>C) 模块
  - 2 个 CAN 2.0 A 和 B 控制器: 多播共享串行总线标准
- 存储器
  - 具有 4 个存储体的 1024KB 闪存存储器配置支持对每个存储体提供独立代码保护
  - 具有单周期访问的 256KB SRAM 以 120MHz 时钟频率提供近 2GB/s 的内存带宽
  - 6KB EEPROM: 每 2 个页块写入 500k、矫正、锁定保护
  - 内部 ROM: 搭载有 SimpleLink™ SDK 软件
    - 外设驱动程序库
    - 引导加载程序
  - 外部外设接口 (EPI): 8、16 或 32 位专用并行接口访问外部器件和存储器 (SDRAM、闪存或 SRAM)
- 安全性
  - 高级加密标准 (AES): 基于 128、192 和 256 位密钥的硬件加速数据加密和解密
  - 数据加密标准 (DES): 具有 168 位有效密钥长度并且支持块密码实施的硬件加速数据加密和解密
  - 安全哈希算法/消息摘要算法 (SHA/MD5): 支持 SHA-1、SHA-2 和 MD5 哈希计算的高级哈希引擎
  - 循环冗余校验 (CRC) 硬件
  - 篡改: 支持四个篡改输入和可配置篡改事件响应
- 模拟
  - 2 个基于 12 位 SAR 的 ADC 模块, 每个模块支持高达 200 万次/秒的采样率 (2Msps)
  - 3 个独立的模拟比较器控制器
  - 16 个数字比较器
- 系统管理
  - JTAG 和串行线调试 (SWD): 一个具有集成 ARM SWD 的 JTAG 模块提供访问和控制测试设计特性的途径, 如 I/O 引脚监督和控制、扫描测试和调试。
- 开发套件和软件 (请参阅 [工具和软件](#))
  - SimpleLink™ MSP-EXP432E401Y LaunchPad™ 开发套件
  - SimpleLink MSP432E4 软件开发套件 (SDK)
- 封装信息
  - 封装: 128 引脚 TQFP (PDT)
  - 扩展工作温度 (环境) 范围: -40°C 至 105°C

### 1.2 应用

- 工业以太网网关
- 工业智能网关
- 适用于楼宇自动化的区域控制器
- 工厂自动化数据收集器和网关
- 面向电网基础设施的数据集中器
- 无线转以太网网关

### 1.3 说明

SimpleLink MSP432E401Y ARM® Cortex®-M4F 微控制器具有顶级性能和高级集成功能。该产品系列用于需要强大的控制处理和连接功能且具有成本效益的应用。



MSP432E401Y 微控制器集成了大量丰富的通信 特性， 以实现全新的高度互连设计，在性能和功耗之间实现重要的实时控制。这些微控制器具有集成式通信外设以及其他高性能的模拟和数字功能，为开发从人机界面 (HMI) 到联网系统管理控制器在内的许多不同目标应用奠定了坚实的基础。

此外，MSP432E401Y 微控制器为基于 ARM 的微控制器提供了诸多优势，如广泛可用的开发工具、片上系统 (SoC) 基础架构，以及一个庞大的用户社区。另外，这些微控制器使用 ARM Thumb®兼容的 Thumb-2® 指令集来减少内存要求，并以此达到降低成本的目的。当使用 SimpleLink MSP432™SDK 时，MSP432E401Y 与 SimpleLink 系列的所有成员的代码兼容，因此使用灵活，可满足各类具体需求。

MSP432E401Y 器件是 SimpleLink 微控制器 (MCU) 平台的一部分，该平台包含 Wi-Fi®、低功耗 Bluetooth®、低于 1GHz、以太网、Zigbee、线程和主机 MCU，它们均共用一个通用、简单易用的开发环境，其中包含单核软件开发套件 (SDK) 和丰富的工具集。借助一次性集成的 SimpleLink 平台，可以将产品组合中的任何器件组合添加至您的设计中，从而在设计要求变更时实现 100% 代码重用。更多详细信息，请访问 [www.ti.com/simplelink](http://www.ti.com/simplelink)。

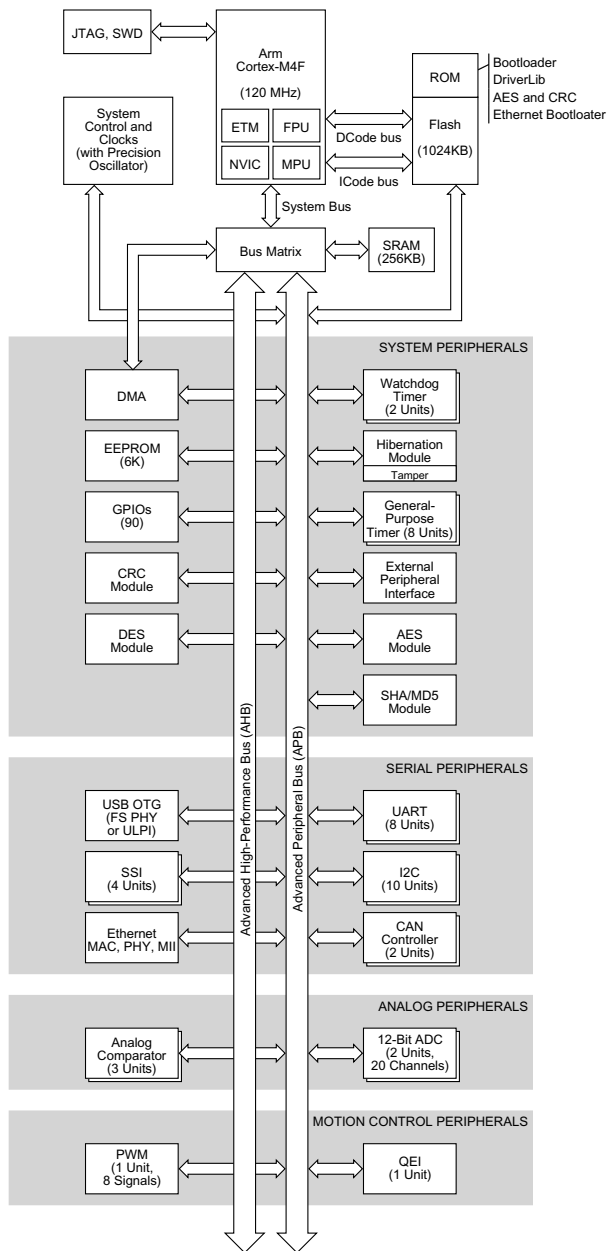
**Device Information<sup>(1)</sup>**

| PART NUMBER     | PACKAGE    | 封装尺寸        |
|-----------------|------------|-------------|
| MSP432E401YTPDT | TQFP (128) | 14mm x 14mm |

(1) 更多信息，请参见 节 9，机械、封装和可订购产品信息。

## 1.4 功能框图

图 1-1 给出了功能框图。



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图 1-1. MSP432E401Y 功能方框图

## 内容

|          |                                                |                           |          |                                                                |                            |
|----------|------------------------------------------------|---------------------------|----------|----------------------------------------------------------------|----------------------------|
| <b>1</b> | <b>器件概述</b>                                    | <b><a href="#">1</a></b>  | 5.11     | Peripheral Current Consumption                                 | <a href="#">41</a>         |
| 1.1      | 特性                                             | <a href="#">1</a>         | 5.12     | LDO Regulator Characteristics                                  | <a href="#">41</a>         |
| 1.2      | 应用                                             | <a href="#">1</a>         | 5.13     | Power Dissipation                                              | <a href="#">42</a>         |
| 1.3      | 说明                                             | <a href="#">1</a>         | 5.14     | Thermal Resistance Characteristics, 128-Pin PDT (TQFP) Package | <a href="#">42</a>         |
| 1.4      | 功能框图                                           | <a href="#">3</a>         | 5.15     | Timing and Switching Characteristics                           | <a href="#">43</a>         |
| <b>2</b> | <b>Revision History</b>                        | <b><a href="#">5</a></b>  | <b>6</b> | <b>Detailed Description</b>                                    | <b><a href="#">94</a></b>  |
| <b>3</b> | <b>Device Characteristics</b>                  | <b><a href="#">6</a></b>  | 6.1      | Overview                                                       | <a href="#">94</a>         |
| 3.1      | Related Products                               | <a href="#">7</a>         | 6.2      | Functional Block Diagram                                       | <a href="#">95</a>         |
| <b>4</b> | <b>Terminal Configuration and Functions</b>    | <b><a href="#">8</a></b>  | 6.3      | Arm Cortex-M4F Processor Core                                  | <a href="#">96</a>         |
| 4.1      | Pin Diagram                                    | <a href="#">8</a>         | 6.4      | On-Chip Memory                                                 | <a href="#">100</a>        |
| 4.2      | Pin Attributes                                 | <a href="#">9</a>         | 6.5      | Peripherals                                                    | <a href="#">102</a>        |
| 4.3      | Signal Descriptions                            | <a href="#">19</a>        | 6.6      | Identification                                                 | <a href="#">144</a>        |
| 4.4      | GPIO Pin Multiplexing                          | <a href="#">30</a>        | 6.7      | Boot Modes                                                     | <a href="#">144</a>        |
| 4.5      | Buffer Type                                    | <a href="#">33</a>        | <b>7</b> | <b>Applications, Implementation, and Layout</b>                | <b><a href="#">146</a></b> |
| 4.6      | Connections for Unused Pins                    | <a href="#">33</a>        | 7.1      | System Design Guidelines                                       | <a href="#">146</a>        |
| <b>5</b> | <b>Specifications</b>                          | <b><a href="#">35</a></b> | <b>8</b> | <b>器件和文档支持</b>                                                 | <b><a href="#">147</a></b> |
| 5.1      | Absolute Maximum Ratings                       | <a href="#">35</a>        | 8.1      | 入门和后续步骤                                                        | <a href="#">147</a>        |
| 5.2      | ESD Ratings                                    | <a href="#">35</a>        | 8.2      | 器件命名规则                                                         | <a href="#">147</a>        |
| 5.3      | Recommended Operating Conditions               | <a href="#">35</a>        | 8.3      | 工具和软件                                                          | <a href="#">148</a>        |
| 5.4      | Recommended DC Operating Conditions            | <a href="#">35</a>        | 8.4      | 文档支持                                                           | <a href="#">149</a>        |
| 5.5      | Recommended GPIO Operating Characteristics     | <a href="#">35</a>        | 8.5      | Community Resources                                            | <a href="#">150</a>        |
| 5.6      | Recommended Fast GPIO Pad Operating Conditions | <a href="#">36</a>        | 8.6      | 商标                                                             | <a href="#">150</a>        |
| 5.7      | Recommended Slow GPIO Pad Operating Conditions | <a href="#">36</a>        | 8.7      | 静电放电警告                                                         | <a href="#">150</a>        |
| 5.8      | GPIO Current Restrictions                      | <a href="#">37</a>        | 8.8      | 出口管制提示                                                         | <a href="#">150</a>        |
| 5.9      | I/O Reliability                                | <a href="#">37</a>        | 8.9      | 术语表                                                            | <a href="#">150</a>        |
| 5.10     | Current Consumption                            | <a href="#">38</a>        | <b>9</b> | <b>机械、封装和可订购信息</b>                                             | <b><a href="#">151</a></b> |

## 2 Revision History

注：之前版本的页码可能与当前版本有所不同。

| DATE        | REVISION | NOTES |
|-------------|----------|-------|
| 2017 年 10 月 | *        | 初始发行版 |

### 3 Device Characteristics

表 3-1 lists the characteristics of the MSP432E401Y MCU.

**表 3-1. Device Characteristics**

| Feature                                            | Description                                                                                      |
|----------------------------------------------------|--------------------------------------------------------------------------------------------------|
| <b>Performance</b>                                 |                                                                                                  |
| Core                                               | Arm Cortex-M4F processor core                                                                    |
| Performance                                        | 120-MHz operation, 150-DMIPS performance                                                         |
| Flash                                              | 1024KB of flash memory                                                                           |
| System SRAM                                        | 256KB of single-cycle system SRAM                                                                |
| EEPROM                                             | 6KB of EEPROM                                                                                    |
| Internal ROM                                       | Internal ROM loaded with SimpleLink SDK software                                                 |
| External Peripheral Interface (EPI)                | 8-, 16-, or 32-bit dedicated interface for peripherals and memory                                |
| <b>Security</b>                                    |                                                                                                  |
| Cyclical Redundancy Check (CRC)                    | 16- or 32-bit hash function that supports four CRC forms                                         |
| Advanced Encryption Standard (AES)                 | Hardware accelerated data encryption and decryption based on 128-, 192-, and 256-bit keys        |
| Data Encryption Standard (DES)                     | Block cipher implementation with 168-bit effective key length                                    |
| Hardware Accelerated Hash (SHA/MD5)                | Advanced hash engine that supports SHA-1, SHA-2, or MD5 hash computation                         |
| Tamper                                             | Support for four tamper inputs and configurable tamper event response                            |
| <b>Communication Interfaces</b>                    |                                                                                                  |
| Universal Asynchronous Receiver/Transmitter (UART) | Eight UARTs                                                                                      |
| Quad Synchronous Serial Interface (QSSI)           | Four SSI modules with bi-, quad-, and advanced-SSI support                                       |
| Inter-Integrated Circuit (I <sup>2</sup> C)        | Ten I <sup>2</sup> C modules with four transmission speeds including high-speed mode             |
| Controller Area Network (CAN)                      | Two CAN 2.0 A/B controllers                                                                      |
| Ethernet MAC                                       | 10/100 Ethernet MAC                                                                              |
| Ethernet PHY                                       | PHY with IEEE 1588 PTP hardware support                                                          |
| Universal Serial Bus (USB)                         | USB 2.0 OTG, Host, and Device with ULPI interface option and Link Power Management (LPM) support |
| <b>System Integration</b>                          |                                                                                                  |
| Micro Direct Memory Access (μDMA)                  | Arm PrimeCell® 32-channel configurable μDMA controller                                           |
| General-Purpose Timer (GPTM)                       | Eight 16- or 32-bit GPTM blocks                                                                  |
| Watchdog Timer (WDT)                               | Two watchdog timers                                                                              |
| Hibernation Module (HIB)                           | Low-power battery-backed Hibernation module                                                      |
| General-Purpose Input/Output (GPIO)                | 15 physical GPIO blocks                                                                          |
| <b>Advanced Motion Control</b>                     |                                                                                                  |
| Pulse Width Modulator (PWM)                        | One PWM module, with four PWM generator blocks and a control block, for a total of 8 PWM outputs |
| Quadrature Encoder Interface (QEI)                 | One QEI module                                                                                   |
| <b>Analog Support</b>                              |                                                                                                  |
| Analog-to-Digital Converter (ADC)                  | Two 12-bit ADC modules, each with a maximum sample rate of 2 Msps                                |
| Analog Comparator Controller                       | Three independent integrated analog comparators                                                  |
| Digital Comparator                                 | 16 digital comparators                                                                           |
| <b>System Management</b>                           |                                                                                                  |
| JTAG and Serial Wire Debug (SWD)                   | One JTAG module with integrated Arm SWD                                                          |
| <b>Package Information</b>                         |                                                                                                  |
| Package                                            | 128-pin TQFP (PDT)                                                                               |
| Operating Range (Ambient)                          | Extended temperature range (–40°C to 105°C)                                                      |

### 3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

**Products for TI Microcontrollers** Low-power and high-performance MCUs, with wired and wireless connectivity options.

**Products for SimpleLink MSP432 MCUs** SimpleLink MSP432 MCUs with an ultra-low-power Arm Cortex-M4 core are optimized for Internet-of-Things sensor node applications. With an integrated ADC, the family enables acquisition and processing of high-precision signals without sacrificing power and is an optimal host MCU for TI's SimpleLink wireless connectivity solutions.

**Companion Products for MSP432E401Y** Review products that are frequently purchased or used with this product.

**Reference Designs** The TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market.

## 4 Terminal Configuration and Functions

### 4.1 Pin Diagram

图 4-1 shows the pinout of the 128-pin TQFP (PDT) package.

Each GPIO signal is identified by its GPIO port unless it defaults to an alternate function on reset. In this case, the GPIO port name is followed by the default alternate function. For a complete list of functions for each pin, see 表 4-2.

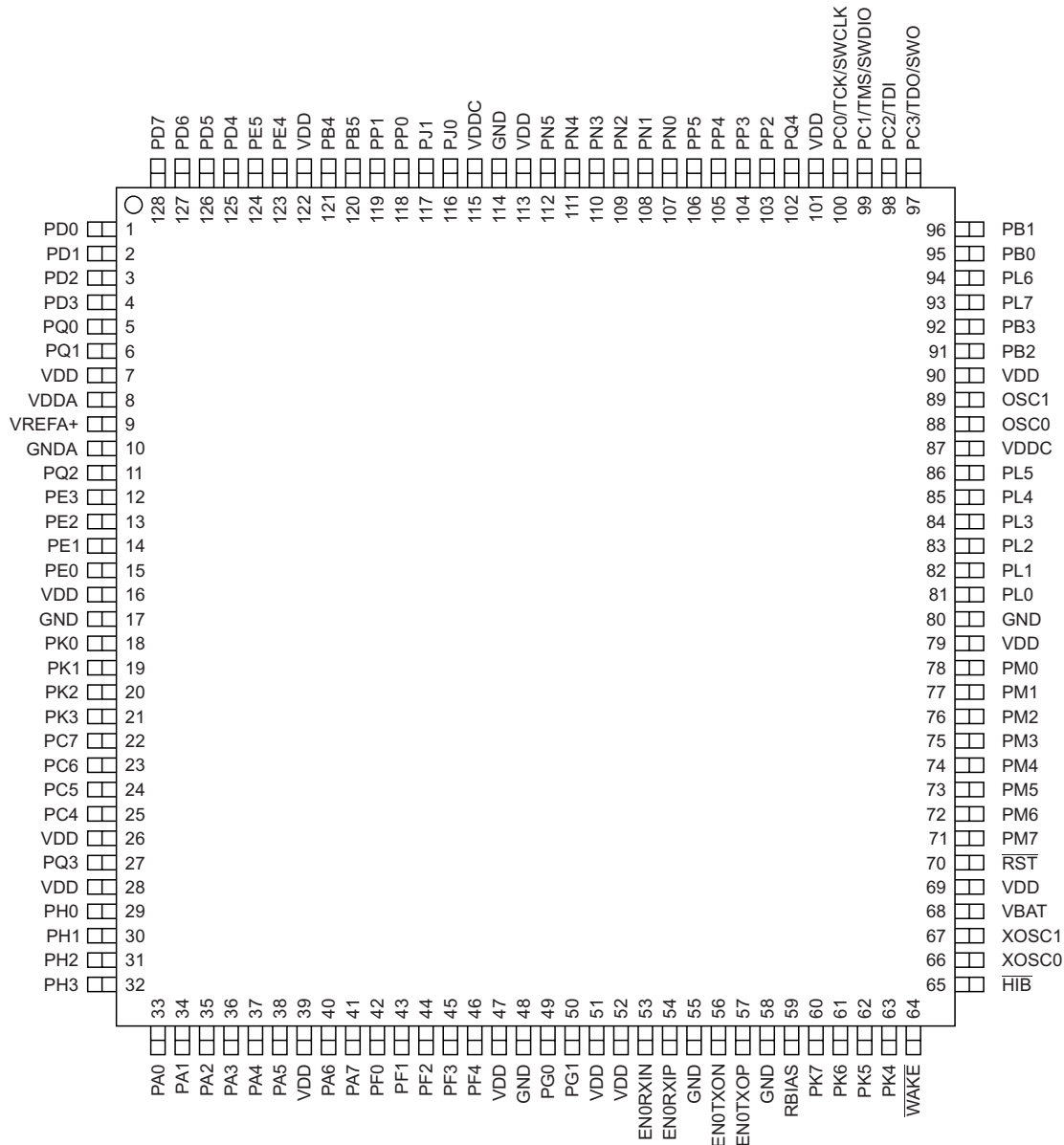


图 4-1. 128-Pin PDT Package (Top View)

## 4.2 Pin Attributes

表 4-1 lists GPIO pins with special considerations. Most GPIO pins are configured as GPIOs and are high-impedance by default (GPIOAFSEL = 0, GPIODEN = 0, GPIOPDR = 0, GPIOPUR = 0, and GPIOPCTL = 0). Special consideration pins may be programmed to a non-GPIO function or may have special commit controls out of reset. In addition, a POR returns these GPIOs to their original special consideration state.

**表 4-1. GPIO Pins With Special Considerations**

| GPIO PINS | DEFAULT RESET STATE | GPIOAFSEL | GPIODEN | GPIOPDR | GPIOPUR | GPIOPCTL | GPIOCR |
|-----------|---------------------|-----------|---------|---------|---------|----------|--------|
| PC[3:0]   | JTAG/SWD            | 1         | 1       | 0       | 1       | 0x1      | 0      |
| PD[7]     | GPIO <sup>(1)</sup> | 0         | 0       | 0       | 0       | 0x0      | 0      |
| PE[7]     | GPIO <sup>(1)</sup> | 0         | 0       | 0       | 0       | 0x0      | 0      |

- (1) This pin is configured as a GPIO by default but is locked and can only be reprogrammed by unlocking the pin in the GPIOLOCK register and uncommitting it by setting the GPIOCR register.

表 4-2 describes the pin attributes.

**表 4-2. Pin Attributes**

| PIN NUMBER | SIGNAL NAME | SIGNAL TYPE <sup>(1)</sup> | BUFFER TYPE <sup>(2)</sup> | PIN MUX ENCODING | POWER SOURCE <sup>(3)</sup> | STATE AFTER RESET RELEASE <sup>(4)</sup> |
|------------|-------------|----------------------------|----------------------------|------------------|-----------------------------|------------------------------------------|
| 1          | PD0         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | AIN15       | I                          | Analog                     | PD0              |                             | N/A                                      |
|            | C0o         | O                          | LVC MOS                    | PD0 (5)          |                             | N/A                                      |
|            | I2C7SCL     | I/O                        | LVC MOS                    | PD0 (2)          |                             | N/A                                      |
|            | SSI2XDAT1   | I/O                        | LVC MOS                    | PD0 (15)         |                             | N/A                                      |
|            | T0CCP0      | I/O                        | LVC MOS                    | PD0 (3)          |                             | N/A                                      |
| 2          | PD1         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | AIN14       | I                          | Analog                     | PD1              |                             | N/A                                      |
|            | C1o         | O                          | LVC MOS                    | PD1 (5)          |                             | N/A                                      |
|            | I2C7SDA     | I/O                        | LVC MOS                    | PD1 (2)          |                             | N/A                                      |
|            | SSI2XDAT0   | I/O                        | LVC MOS                    | PD1 (15)         |                             | N/A                                      |
|            | T0CCP1      | I/O                        | LVC MOS                    | PD1 (3)          |                             | N/A                                      |
| 3          | PD2         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | AIN13       | I                          | Analog                     | PD2              |                             | N/A                                      |
|            | C2o         | O                          | LVC MOS                    | PD2 (5)          |                             | N/A                                      |
|            | I2C8SCL     | I/O                        | LVC MOS                    | PD2 (2)          |                             | N/A                                      |
|            | SSI2Fss     | I/O                        | LVC MOS                    | PD2 (15)         |                             | N/A                                      |
|            | T1CCP0      | I/O                        | LVC MOS                    | PD2 (3)          |                             | N/A                                      |
| 4          | PD3         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | AIN12       | I                          | Analog                     | PD3              |                             | N/A                                      |
|            | I2C8SDA     | I/O                        | LVC MOS                    | PD3 (2)          |                             | N/A                                      |
|            | SSI2CIk     | I/O                        | LVC MOS                    | PD3 (15)         |                             | N/A                                      |
|            | T1CCP1      | I/O                        | LVC MOS                    | PD3 (3)          |                             | N/A                                      |
| 5          | PQ0         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S20     | I/O                        | LVC MOS                    | PQ0 (15)         |                             | N/A                                      |
|            | SSI3CIk     | I/O                        | LVC MOS                    | PQ0 (14)         |                             | N/A                                      |

- (1) Signal Types: I = Input, O = Output, I/O = Input or Output.

- (2) For details on buffer types, see 表 4-5.

- (3) N/A = Not applicable

- (4) State after reset release: PU = High impedance with an active pullup resistor, OFF = High impedance, N/A = not applicable

表 4-2. Pin Attributes (continued)

| PIN NUMBER | SIGNAL NAME | SIGNAL TYPE <sup>(1)</sup> | BUFFER TYPE <sup>(2)</sup> | PIN MUX ENCODING | POWER SOURCE <sup>(3)</sup> | STATE AFTER RESET RELEASE <sup>(4)</sup> |
|------------|-------------|----------------------------|----------------------------|------------------|-----------------------------|------------------------------------------|
| 6          | PQ1         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S21     | I/O                        | LVC MOS                    | PQ1 (15)         |                             | N/A                                      |
|            | SSI3Fss     | I/O                        | LVC MOS                    | PQ1 (14)         |                             | N/A                                      |
| 7          | VDD         | –                          | Power                      | Fixed            | N/A                         | N/A                                      |
| 8          | VDDA        | –                          | Power                      | Fixed            | N/A                         | N/A                                      |
| 9          | VREFA+      | –                          | Analog                     | Fixed            | N/A                         | N/A                                      |
| 10         | GNDA        | –                          | Power                      | Fixed            | N/A                         | N/A                                      |
| 11         | PQ2         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S22     | I/O                        | LVC MOS                    | PQ2 (15)         |                             | N/A                                      |
|            | SSI3XDAT0   | I/O                        | LVC MOS                    | PQ2 (14)         |                             | N/A                                      |
| 12         | PE3         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | AIN0        | I                          | Analog                     | PE3              |                             | N/A                                      |
|            | U1DTR       | O                          | LVC MOS                    | PE3 (1)          |                             | N/A                                      |
| 13         | PE2         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | AIN1        | I                          | Analog                     | PE2              |                             | N/A                                      |
|            | U1DCD       | I                          | LVC MOS                    | PE2 (1)          |                             | N/A                                      |
| 14         | PE1         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | AIN2        | I                          | Analog                     | PE1              |                             | N/A                                      |
|            | U1DSR       | I                          | LVC MOS                    | PE1 (1)          |                             | N/A                                      |
| 15         | PE0         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | AIN3        | I                          | Analog                     | PE0              |                             | N/A                                      |
|            | U1RTS       | O                          | LVC MOS                    | PE0 (1)          |                             | N/A                                      |
| 16         | VDD         | –                          | Power                      | Fixed            | N/A                         | N/A                                      |
| 17         | GND         | –                          | Power                      | Fixed            | N/A                         | N/A                                      |
| 18         | PK0         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | AIN16       | I                          | Analog                     | PK0              |                             | N/A                                      |
|            | EPI0S0      | I/O                        | LVC MOS                    | PK0 (15)         |                             | N/A                                      |
|            | U4Rx        | I                          | LVC MOS                    | PK0 (1)          |                             | N/A                                      |
| 19         | PK1         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | AIN17       | I                          | Analog                     | PK1              |                             | N/A                                      |
|            | EPI0S1      | I/O                        | LVC MOS                    | PK1 (15)         |                             | N/A                                      |
|            | U4Tx        | O                          | LVC MOS                    | PK1 (1)          |                             | N/A                                      |
| 20         | PK2         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | AIN18       | I                          | Analog                     | PK2              |                             | N/A                                      |
|            | EPI0S2      | I/O                        | LVC MOS                    | PK2 (15)         |                             | N/A                                      |
|            | U4RTS       | O                          | LVC MOS                    | PK2 (1)          |                             | N/A                                      |
| 21         | PK3         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | AIN19       | I                          | Analog                     | PK3              |                             | N/A                                      |
|            | EPI0S3      | I/O                        | LVC MOS                    | PK3 (15)         |                             | N/A                                      |
|            | U4CTS       | I                          | LVC MOS                    | PK3 (1)          |                             | N/A                                      |
| 22         | PC7         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | C0-         | I                          | Analog                     | PC7              |                             | N/A                                      |
|            | EPI0S4      | I/O                        | LVC MOS                    | PC7 (15)         |                             | N/A                                      |
|            | U5Tx        | O                          | LVC MOS                    | PC7 (1)          |                             | N/A                                      |

**表 4-2. Pin Attributes (continued)**

| PIN NUMBER | SIGNAL NAME | SIGNAL TYPE <sup>(1)</sup> | BUFFER TYPE <sup>(2)</sup> | PIN MUX ENCODING | POWER SOURCE <sup>(3)</sup> | STATE AFTER RESET RELEASE <sup>(4)</sup> |
|------------|-------------|----------------------------|----------------------------|------------------|-----------------------------|------------------------------------------|
| 23         | PC6         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | C0+         | I                          | Analog                     | PC6              |                             | N/A                                      |
|            | EPI0S5      | I/O                        | LVC MOS                    | PC6 (15)         |                             | N/A                                      |
|            | U5Rx        | I                          | LVC MOS                    | PC6 (1)          |                             | N/A                                      |
| 24         | PC5         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | C1+         | I                          | Analog                     | PC5              |                             | N/A                                      |
|            | EPI0S6      | I/O                        | LVC MOS                    | PC5 (15)         |                             | N/A                                      |
|            | RTCCLK      | O                          | LVC MOS                    | PC5 (7)          |                             | N/A                                      |
|            | U7Tx        | O                          | LVC MOS                    | PC5 (1)          |                             | N/A                                      |
| 25         | PC4         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | C1-         | I                          | Analog                     | PC4              |                             | N/A                                      |
|            | EPI0S7      | I/O                        | LVC MOS                    | PC4 (15)         |                             | N/A                                      |
|            | U7Rx        | I                          | LVC MOS                    | PC4 (1)          |                             | N/A                                      |
| 26         | VDD         | –                          | Power                      | Fixed            | N/A                         | N/A                                      |
| 27         | PQ3         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S23     | I/O                        | LVC MOS                    | PQ3 (15)         |                             | N/A                                      |
|            | SSI3XDAT1   | I/O                        | LVC MOS                    | PQ3 (14)         |                             | N/A                                      |
| 28         | VDD         | –                          | Power                      | Fixed            | N/A                         | N/A                                      |
| 29         | PH0         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S0      | I/O                        | LVC MOS                    | PH0 (15)         |                             | N/A                                      |
|            | U0RTS       | O                          | LVC MOS                    | PH0 (1)          |                             | N/A                                      |
| 30         | PH1         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S1      | I/O                        | LVC MOS                    | PH1 (15)         |                             | N/A                                      |
|            | U0CTS       | I                          | LVC MOS                    | PH1 (1)          |                             | N/A                                      |
| 31         | PH2         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S2      | I/O                        | LVC MOS                    | PH2 (15)         |                             | N/A                                      |
|            | U0DCD       | I                          | LVC MOS                    | PH2 (1)          |                             | N/A                                      |
| 32         | PH3         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S3      | I/O                        | LVC MOS                    | PH3 (15)         |                             | N/A                                      |
|            | U0DSR       | I                          | LVC MOS                    | PH3 (1)          |                             | N/A                                      |
| 33         | PA0         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | CAN0Rx      | I                          | LVC MOS                    | PA0 (7)          |                             | N/A                                      |
|            | I2C9SCL     | I/O                        | LVC MOS                    | PA0 (2)          |                             | N/A                                      |
|            | T0CCP0      | I/O                        | LVC MOS                    | PA0 (3)          |                             | N/A                                      |
|            | U0Rx        | I                          | LVC MOS                    | PA0 (1)          |                             | N/A                                      |
| 34         | PA1         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | CAN0Tx      | O                          | LVC MOS                    | PA1 (7)          |                             | N/A                                      |
|            | I2C9SDA     | I/O                        | LVC MOS                    | PA1 (2)          |                             | N/A                                      |
|            | T0CCP1      | I/O                        | LVC MOS                    | PA1 (3)          |                             | N/A                                      |
|            | U0Tx        | O                          | LVC MOS                    | PA1 (1)          |                             | N/A                                      |
| 35         | PA2         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | I2C8SCL     | I/O                        | LVC MOS                    | PA2 (2)          |                             | N/A                                      |
|            | SSI0Clk     | I/O                        | LVC MOS                    | PA2 (15)         |                             | N/A                                      |
|            | T1CCP0      | I/O                        | LVC MOS                    | PA2 (3)          |                             | N/A                                      |
|            | U4Rx        | I                          | LVC MOS                    | PA2 (1)          |                             | N/A                                      |

表 4-2. Pin Attributes (continued)

| PIN NUMBER | SIGNAL NAME | SIGNAL TYPE <sup>(1)</sup> | BUFFER TYPE <sup>(2)</sup> | PIN MUX ENCODING | POWER SOURCE <sup>(3)</sup> | STATE AFTER RESET RELEASE <sup>(4)</sup> |
|------------|-------------|----------------------------|----------------------------|------------------|-----------------------------|------------------------------------------|
| 36         | PA3         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | I2C8SDA     | I/O                        | LVC MOS                    | PA3 (2)          |                             | N/A                                      |
|            | SSI0Fss     | I/O                        | LVC MOS                    | PA3 (15)         |                             | N/A                                      |
|            | T1CCP1      | I/O                        | LVC MOS                    | PA3 (3)          |                             | N/A                                      |
|            | U4Tx        | O                          | LVC MOS                    | PA3 (1)          |                             | N/A                                      |
| 37         | PA4         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | I2C7SCL     | I/O                        | LVC MOS                    | PA4 (2)          |                             | N/A                                      |
|            | SSI0XDAT0   | I/O                        | LVC MOS                    | PA4 (15)         |                             | N/A                                      |
|            | T2CCP0      | I/O                        | LVC MOS                    | PA4 (3)          |                             | N/A                                      |
|            | U3Rx        | I                          | LVC MOS                    | PA4 (1)          |                             | N/A                                      |
| 38         | PA5         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | I2C7SDA     | I/O                        | LVC MOS                    | PA5 (2)          |                             | N/A                                      |
|            | SSI0XDAT1   | I/O                        | LVC MOS                    | PA5 (15)         |                             | N/A                                      |
|            | T2CCP1      | I/O                        | LVC MOS                    | PA5 (3)          |                             | N/A                                      |
|            | U3Tx        | O                          | LVC MOS                    | PA5 (1)          |                             | N/A                                      |
| 39         | VDD         | –                          | Power                      | Fixed            | N/A                         | N/A                                      |
| 40         | PA6         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S8      | I/O                        | LVC MOS                    | PA6 (15)         |                             | N/A                                      |
|            | I2C6SCL     | I/O                        | LVC MOS                    | PA6 (2)          |                             | N/A                                      |
|            | SSI0XDAT2   | I/O                        | LVC MOS                    | PA6 (13)         |                             | N/A                                      |
|            | T3CCP0      | I/O                        | LVC MOS                    | PA6 (3)          |                             | N/A                                      |
|            | U2Rx        | I                          | LVC MOS                    | PA6 (1)          |                             | N/A                                      |
|            | USB0EPEN    | O                          | LVC MOS                    | PA6 (5)          |                             | N/A                                      |
| 41         | PA7         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S9      | I/O                        | LVC MOS                    | PA7 (15)         |                             | N/A                                      |
|            | I2C6SDA     | I/O                        | LVC MOS                    | PA7 (2)          |                             | N/A                                      |
|            | SSI0XDAT3   | I/O                        | LVC MOS                    | PA7 (13)         |                             | N/A                                      |
|            | T3CCP1      | I/O                        | LVC MOS                    | PA7 (3)          |                             | N/A                                      |
|            | U2Tx        | O                          | LVC MOS                    | PA7 (1)          |                             | N/A                                      |
|            | USB0EPEN    | O                          | LVC MOS                    | PA7 (11)         |                             | N/A                                      |
|            | USB0PFLT    | I                          | LVC MOS                    | PA7 (5)          |                             | N/A                                      |
| 42         | PF0         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EN0LED0     | O                          | LVC MOS                    | PF0 (5)          |                             | N/A                                      |
|            | M0PWM0      | O                          | LVC MOS                    | PF0 (6)          |                             | N/A                                      |
|            | SSI3XDAT1   | I/O                        | LVC MOS                    | PF0 (14)         |                             | N/A                                      |
|            | TRD2        | O                          | LVC MOS                    | PF0 (15)         |                             | N/A                                      |
| 43         | PF1         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EN0LED2     | O                          | LVC MOS                    | PF1 (5)          |                             | N/A                                      |
|            | M0PWM1      | O                          | LVC MOS                    | PF1 (6)          |                             | N/A                                      |
|            | SSI3XDAT0   | I/O                        | LVC MOS                    | PF1 (14)         |                             | N/A                                      |
|            | TRD1        | O                          | LVC MOS                    | PF1 (15)         |                             | N/A                                      |
| 44         | PF2         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | M0PWM2      | O                          | LVC MOS                    | PF2 (6)          |                             | N/A                                      |
|            | SSI3Fss     | I/O                        | LVC MOS                    | PF2 (14)         |                             | N/A                                      |
|            | TRD0        | O                          | LVC MOS                    | PF2 (15)         |                             | N/A                                      |

**表 4-2. Pin Attributes (continued)**

| PIN NUMBER | SIGNAL NAME | SIGNAL TYPE <sup>(1)</sup> | BUFFER TYPE <sup>(2)</sup> | PIN MUX ENCODING | POWER SOURCE <sup>(3)</sup> | STATE AFTER RESET RELEASE <sup>(4)</sup> |
|------------|-------------|----------------------------|----------------------------|------------------|-----------------------------|------------------------------------------|
| 45         | PF3         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | M0PWM3      | O                          | LVC MOS                    | PF3 (6)          |                             | N/A                                      |
|            | SSI3Ck      | I/O                        | LVC MOS                    | PF3 (14)         |                             | N/A                                      |
|            | TRCLK       | O                          | LVC MOS                    | PF3 (15)         |                             | N/A                                      |
| 46         | PF4         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EN0LED1     | O                          | LVC MOS                    | PF4 (5)          |                             | N/A                                      |
|            | M0FAULT0    | I                          | LVC MOS                    | PF4 (6)          |                             | N/A                                      |
|            | SSI3XDAT2   | I/O                        | LVC MOS                    | PF4 (14)         |                             | N/A                                      |
|            | TRD3        | O                          | LVC MOS                    | PF4 (15)         |                             | N/A                                      |
| 47         | VDD         | –                          | Power                      | Fixed            | N/A                         | N/A                                      |
| 48         | GND         | –                          | Power                      | Fixed            | N/A                         | N/A                                      |
| 49         | PG0         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EN0PPS      | O                          | LVC MOS                    | PG0 (5)          |                             | N/A                                      |
|            | EPI0S11     | I/O                        | LVC MOS                    | PG0 (15)         |                             | N/A                                      |
|            | I2C1SCL     | I/O                        | LVC MOS                    | PG0 (2)          |                             | N/A                                      |
|            | M0PWM4      | O                          | LVC MOS                    | PG0 (6)          |                             | N/A                                      |
| 50         | PG1         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S10     | I/O                        | LVC MOS                    | PG1 (15)         |                             | N/A                                      |
|            | I2C1SDA     | I/O                        | LVC MOS                    | PG1 (2)          |                             | N/A                                      |
|            | M0PWM5      | O                          | LVC MOS                    | PG1 (6)          |                             | N/A                                      |
| 51         | VDD         | –                          | Power                      | Fixed            | N/A                         | N/A                                      |
| 52         | VDD         | –                          | Power                      | Fixed            | N/A                         | N/A                                      |
| 53         | EN0RXIN     | I/O                        | LVC MOS                    | Fixed            | VDD                         | N/A                                      |
| 54         | EN0RXIP     | I/O                        | LVC MOS                    | Fixed            | VDD                         | N/A                                      |
| 55         | GND         | –                          | Power                      | Fixed            | N/A                         | N/A                                      |
| 56         | EN0TXON     | I/O                        | LVC MOS                    | Fixed            | VDD                         | N/A                                      |
| 57         | EN0TXOP     | I/O                        | LVC MOS                    | Fixed            | VDD                         | N/A                                      |
| 58         | GND         | –                          | Power                      | Fixed            | N/A                         | N/A                                      |
| 59         | RBIAS       | O                          | Analog                     | Fixed            | VDD                         | N/A                                      |
| 60         | PK7         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S24     | I/O                        | LVC MOS                    | PK7 (15)         |                             | N/A                                      |
|            | I2C4SDA     | I/O                        | LVC MOS                    | PK7 (2)          |                             | N/A                                      |
|            | M0FAULT2    | I                          | LVC MOS                    | PK7 (6)          |                             | N/A                                      |
|            | RTCCLK      | O                          | LVC MOS                    | PK7 (5)          |                             | N/A                                      |
|            | U0RI        | I                          | LVC MOS                    | PK7 (1)          |                             | N/A                                      |
| 61         | PK6         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EN0LED1     | O                          | LVC MOS                    | PK6 (5)          |                             | N/A                                      |
|            | EPI0S25     | I/O                        | LVC MOS                    | PK6 (15)         |                             | N/A                                      |
|            | I2C4SCL     | I/O                        | LVC MOS                    | PK6 (2)          |                             | N/A                                      |
|            | M0FAULT1    | I                          | LVC MOS                    | PK6 (6)          |                             | N/A                                      |
| 62         | PK5         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EN0LED2     | O                          | LVC MOS                    | PK5 (5)          |                             | N/A                                      |
|            | EPI0S31     | I/O                        | LVC MOS                    | PK5 (15)         |                             | N/A                                      |
|            | I2C3SDA     | I/O                        | LVC MOS                    | PK5 (2)          |                             | N/A                                      |
|            | M0PWM7      | O                          | LVC MOS                    | PK5 (6)          |                             | N/A                                      |

表 4-2. Pin Attributes (continued)

| PIN NUMBER | SIGNAL NAME | SIGNAL TYPE <sup>(1)</sup> | BUFFER TYPE <sup>(2)</sup> | PIN MUX ENCODING | POWER SOURCE <sup>(3)</sup> | STATE AFTER RESET RELEASE <sup>(4)</sup> |
|------------|-------------|----------------------------|----------------------------|------------------|-----------------------------|------------------------------------------|
| 63         | PK4         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EN0LED0     | O                          | LVC MOS                    | PK4 (5)          |                             | N/A                                      |
|            | EPI0S32     | I/O                        | LVC MOS                    | PK4 (15)         |                             | N/A                                      |
|            | I2C3SCL     | I/O                        | LVC MOS                    | PK4 (2)          |                             | N/A                                      |
|            | M0PWM6      | O                          | LVC MOS                    | PK4 (6)          |                             | N/A                                      |
| 64         | WAKE        | I                          | LVC MOS                    | Fixed            | VBAT                        | N/A                                      |
| 65         | HIB         | O                          | LVC MOS                    | Fixed            | VBAT                        | N/A                                      |
| 66         | XOSC0       | I                          | Analog                     | Fixed            | VBAT                        | N/A                                      |
| 67         | XOSC1       | O                          | Analog                     | Fixed            | VBAT                        | N/A                                      |
| 68         | VBAT        | –                          | Power                      | Fixed            | N/A                         | N/A                                      |
| 69         | VDD         | –                          | Power                      | Fixed            | N/A                         | N/A                                      |
| 70         | RST         | I                          | LVC MOS                    | Fixed            | VDD                         | N/A                                      |
| 71         | PM7         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | T5CCP1      | I/O                        | LVC MOS                    | PM7 (3)          |                             | N/A                                      |
|            | TMPR0       | I/O                        | LVC MOS                    | PM7              |                             | N/A                                      |
|            | U0RI        | I                          | LVC MOS                    | PM7 (1)          |                             | N/A                                      |
| 72         | PM6         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | T5CCP0      | I/O                        | LVC MOS                    | PM6 (3)          |                             | N/A                                      |
|            | TMPR1       | I/O                        | LVC MOS                    | PM6              |                             | N/A                                      |
|            | U0DSR       | I                          | LVC MOS                    | PM6 (1)          |                             | N/A                                      |
| 73         | PM5         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | T4CCP1      | I/O                        | LVC MOS                    | PM5 (3)          |                             | N/A                                      |
|            | TMPR2       | I/O                        | LVC MOS                    | PM5              |                             | N/A                                      |
|            | U0DCD       | I                          | LVC MOS                    | PM5 (1)          |                             | N/A                                      |
| 74         | PM4         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | T4CCP0      | I/O                        | LVC MOS                    | PM4 (3)          |                             | N/A                                      |
|            | TMPR3       | I/O                        | LVC MOS                    | PM4              |                             | N/A                                      |
|            | U0CTS       | I                          | LVC MOS                    | PM4 (1)          |                             | N/A                                      |
| 75         | PM3         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S12     | I/O                        | LVC MOS                    | PM3 (15)         |                             | N/A                                      |
|            | T3CCP1      | I/O                        | LVC MOS                    | PM3 (3)          |                             | N/A                                      |
| 76         | PM2         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S13     | I/O                        | LVC MOS                    | PM2 (15)         |                             | N/A                                      |
|            | T3CCP0      | I/O                        | LVC MOS                    | PM2 (3)          |                             | N/A                                      |
| 77         | PM1         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S14     | I/O                        | LVC MOS                    | PM1 (15)         |                             | N/A                                      |
|            | T2CCP1      | I/O                        | LVC MOS                    | PM1 (3)          |                             | N/A                                      |
| 78         | PM0         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S15     | I/O                        | LVC MOS                    | PM0 (15)         |                             | N/A                                      |
|            | T2CCP0      | I/O                        | LVC MOS                    | PM0 (3)          |                             | N/A                                      |
| 79         | VDD         | –                          | Power                      | Fixed            | N/A                         | N/A                                      |
| 80         | GND         | –                          | Power                      | Fixed            | N/A                         | N/A                                      |

**表 4-2. Pin Attributes (continued)**

| PIN NUMBER | SIGNAL NAME | SIGNAL TYPE <sup>(1)</sup> | BUFFER TYPE <sup>(2)</sup> | PIN MUX ENCODING | POWER SOURCE <sup>(3)</sup> | STATE AFTER RESET RELEASE <sup>(4)</sup> |
|------------|-------------|----------------------------|----------------------------|------------------|-----------------------------|------------------------------------------|
| 81         | PL0         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S16     | I/O                        | LVC MOS                    | PL0 (15)         |                             | N/A                                      |
|            | I2C2SDA     | I/O                        | LVC MOS                    | PL0 (2)          |                             | N/A                                      |
|            | M0FAULT3    | I                          | LVC MOS                    | PL0 (6)          |                             | N/A                                      |
|            | USB0D0      | I/O                        | LVC MOS                    | PL0 (14)         |                             | N/A                                      |
| 82         | PL1         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S17     | I/O                        | LVC MOS                    | PL1 (15)         |                             | N/A                                      |
|            | I2C2SCL     | I/O                        | LVC MOS                    | PL1 (2)          |                             | N/A                                      |
|            | PhA0        | I                          | LVC MOS                    | PL1 (6)          |                             | N/A                                      |
|            | USB0D1      | I/O                        | LVC MOS                    | PL1 (14)         |                             | N/A                                      |
| 83         | PL2         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | C0o         | O                          | LVC MOS                    | PL2 (5)          |                             | N/A                                      |
|            | EPI0S18     | I/O                        | LVC MOS                    | PL2 (15)         |                             | N/A                                      |
|            | PhB0        | I                          | LVC MOS                    | PL2 (6)          |                             | N/A                                      |
|            | USB0D2      | I/O                        | LVC MOS                    | PL2 (14)         |                             | N/A                                      |
| 84         | PL3         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | C1o         | O                          | LVC MOS                    | PL3 (5)          |                             | N/A                                      |
|            | EPI0S19     | I/O                        | LVC MOS                    | PL3 (15)         |                             | N/A                                      |
|            | IDX0        | I                          | LVC MOS                    | PL3 (6)          |                             | N/A                                      |
|            | USB0D3      | I/O                        | LVC MOS                    | PL3 (14)         |                             | N/A                                      |
| 85         | PL4         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S26     | I/O                        | LVC MOS                    | PL4 (15)         |                             | N/A                                      |
|            | T0CCP0      | I/O                        | LVC MOS                    | PL4 (3)          |                             | N/A                                      |
|            | USB0D4      | I/O                        | LVC MOS                    | PL4 (14)         |                             | N/A                                      |
| 86         | PL5         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S33     | I/O                        | LVC MOS                    | PL5 (15)         |                             | N/A                                      |
|            | T0CCP1      | I/O                        | LVC MOS                    | PL5 (3)          |                             | N/A                                      |
|            | USB0D5      | I/O                        | LVC MOS                    | PL5 (14)         |                             | N/A                                      |
| 87         | VDDC        | –                          | Power                      | Fixed            | N/A                         | N/A                                      |
| 88         | OSC0        | I                          | Analog                     | Fixed            | VDD                         | N/A                                      |
| 89         | OSC1        | O                          | Analog                     | Fixed            | VDD                         | N/A                                      |
| 90         | VDD         | –                          | Power                      | Fixed            | N/A                         | N/A                                      |
| 91         | PB2         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S27     | I/O                        | LVC MOS                    | PB2 (15)         |                             | N/A                                      |
|            | I2C0SCL     | I/O                        | LVC MOS                    | PB2 (2)          |                             | N/A                                      |
|            | T5CCP0      | I/O                        | LVC MOS                    | PB2 (3)          |                             | N/A                                      |
|            | USB0STP     | O                          | LVC MOS                    | PB2 (14)         |                             | N/A                                      |
| 92         | PB3         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S28     | I/O                        | LVC MOS                    | PB3 (15)         |                             | N/A                                      |
|            | I2C0SDA     | I/O                        | LVC MOS                    | PB3 (2)          |                             | N/A                                      |
|            | T5CCP1      | I/O                        | LVC MOS                    | PB3 (3)          |                             | N/A                                      |
|            | USB0CLK     | O                          | LVC MOS                    | PB3 (14)         |                             | N/A                                      |
| 93         | PL7         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | T1CCP1      | I/O                        | LVC MOS                    | PL7 (3)          |                             | N/A                                      |
|            | USB0DM      | I/O                        | Analog                     | PL7              |                             | N/A                                      |

表 4-2. Pin Attributes (continued)

| PIN NUMBER | SIGNAL NAME | SIGNAL TYPE <sup>(1)</sup> | BUFFER TYPE <sup>(2)</sup> | PIN MUX ENCODING | POWER SOURCE <sup>(3)</sup> | STATE AFTER RESET RELEASE <sup>(4)</sup> |
|------------|-------------|----------------------------|----------------------------|------------------|-----------------------------|------------------------------------------|
| 94         | PL6         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | T1CCP0      | I/O                        | LVC MOS                    | PL6 (3)          |                             | N/A                                      |
|            | USB0DP      | I/O                        | Analog                     | PL6              |                             | N/A                                      |
| 95         | PB0         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | CAN1Rx      | I                          | LVC MOS                    | PB0 (7)          |                             | N/A                                      |
|            | I2C5SCL     | I/O                        | LVC MOS                    | PB0 (2)          |                             | N/A                                      |
|            | T4CCP0      | I/O                        | LVC MOS                    | PB0 (3)          |                             | N/A                                      |
|            | U1Rx        | I                          | LVC MOS                    | PB0 (1)          |                             | N/A                                      |
|            | USB0ID      | I                          | Analog                     | PB0              |                             | N/A                                      |
|            |             |                            |                            |                  |                             |                                          |
| 96         | PB1         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | CAN1Tx      | O                          | LVC MOS                    | PB1 (7)          |                             | N/A                                      |
|            | I2C5SDA     | I/O                        | LVC MOS                    | PB1 (2)          |                             | N/A                                      |
|            | T4CCP1      | I/O                        | LVC MOS                    | PB1 (3)          |                             | N/A                                      |
|            | U1Tx        | O                          | LVC MOS                    | PB1 (1)          |                             | N/A                                      |
|            | USB0VBUS    | I/O                        | Analog                     | PB1              |                             | N/A                                      |
|            |             |                            |                            |                  |                             |                                          |
| 97         | PC3         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | TDO/SWO     | O                          | LVC MOS                    | PC3 (1)          |                             | PU                                       |
| 98         | PC2         | I/O                        | LVC MOS                    | –                | VDD                         | N/A                                      |
|            | TDI         | I                          | LVC MOS                    | PC2 (1)          |                             | PU                                       |
| 99         | PC1         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | TMS/SWDIO   | I/O                        | LVC MOS                    | PC1 (1)          |                             | PU                                       |
| 100        | PC0         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | TCK/SWCLK   | I                          | LVC MOS                    | PC0 (1)          |                             | PU                                       |
| 101        | VDD         | –                          | Power                      | Fixed            | N/A                         | N/A                                      |
| 102        | PQ4         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | DIVSCLK     | O                          | LVC MOS                    | PQ4 (7)          |                             | N/A                                      |
|            | U1Rx        | I                          | LVC MOS                    | PQ4 (1)          |                             | N/A                                      |
| 103        | PP2         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S29     | I/O                        | LVC MOS                    | PP2 (15)         |                             | N/A                                      |
|            | U0DTR       | O                          | LVC MOS                    | PP2 (1)          |                             | N/A                                      |
|            | USB0NXT     | O                          | LVC MOS                    | PP2 (14)         |                             | N/A                                      |
| 104        | PP3         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S30     | I/O                        | LVC MOS                    | PP3 (15)         |                             | N/A                                      |
|            | RTCCLK      | O                          | LVC MOS                    | PP3 (7)          |                             | N/A                                      |
|            | U0DCD       | I                          | LVC MOS                    | PP3 (2)          |                             | N/A                                      |
|            | U1CTS       | I                          | LVC MOS                    | PP3 (1)          |                             | N/A                                      |
|            | USB0DIR     | O                          | LVC MOS                    | PP3 (14)         |                             | N/A                                      |
|            |             |                            |                            |                  |                             |                                          |
| 105        | PP4         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | U0DSR       | I                          | LVC MOS                    | PP4 (2)          |                             | N/A                                      |
|            | U3RTS       | O                          | LVC MOS                    | PP4 (1)          |                             | N/A                                      |
|            | USB0D7      | I/O                        | LVC MOS                    | PP4 (14)         |                             | N/A                                      |
| 106        | PP5         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | I2C2SCL     | I/O                        | LVC MOS                    | PP5 (2)          |                             | N/A                                      |
|            | U3CTS       | I                          | LVC MOS                    | PP5 (1)          |                             | N/A                                      |
|            | USB0D6      | I/O                        | LVC MOS                    | PP5 (14)         |                             | N/A                                      |

**表 4-2. Pin Attributes (continued)**

| PIN NUMBER | SIGNAL NAME | SIGNAL TYPE <sup>(1)</sup> | BUFFER TYPE <sup>(2)</sup> | PIN MUX ENCODING | POWER SOURCE <sup>(3)</sup> | STATE AFTER RESET RELEASE <sup>(4)</sup> |
|------------|-------------|----------------------------|----------------------------|------------------|-----------------------------|------------------------------------------|
| 107        | PN0         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | U1RTS       | O                          | LVC MOS                    | PN0 (1)          |                             | N/A                                      |
| 108        | PN1         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | U1CTS       | I                          | LVC MOS                    | PN1 (1)          |                             | N/A                                      |
| 109        | PN2         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S29     | I/O                        | LVC MOS                    | PN2 (15)         |                             | N/A                                      |
|            | U1DCD       | I                          | LVC MOS                    | PN2 (1)          |                             | N/A                                      |
|            | U2RTS       | O                          | LVC MOS                    | PN2 (2)          |                             | N/A                                      |
| 110        | PN3         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S30     | I/O                        | LVC MOS                    | PN3 (15)         |                             | N/A                                      |
|            | U1DSR       | I                          | LVC MOS                    | PN3 (1)          |                             | N/A                                      |
|            | U2CTS       | I                          | LVC MOS                    | PN3 (2)          |                             | N/A                                      |
| 111        | PN4         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S34     | I/O                        | LVC MOS                    | PN4 (15)         |                             | N/A                                      |
|            | I2C2SDA     | I/O                        | LVC MOS                    | PN4 (3)          |                             | N/A                                      |
|            | U1DTR       | O                          | LVC MOS                    | PN4 (1)          |                             | N/A                                      |
|            | U3RTS       | O                          | LVC MOS                    | PN4 (2)          |                             | N/A                                      |
| 112        | PN5         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EPI0S35     | I/O                        | LVC MOS                    | PN5 (15)         |                             | N/A                                      |
|            | I2C2SCL     | I/O                        | LVC MOS                    | PN5 (3)          |                             | N/A                                      |
|            | U1RI        | I                          | LVC MOS                    | PN5 (1)          |                             | N/A                                      |
|            | U3CTS       | I                          | LVC MOS                    | PN5 (2)          |                             | N/A                                      |
| 113        | VDD         | –                          | Power                      | Fixed            | N/A                         | N/A                                      |
| 114        | GND         | –                          | Power                      | Fixed            | N/A                         | N/A                                      |
| 115        | VDDC        | –                          | Power                      | Fixed            | N/A                         | N/A                                      |
| 116        | PJ0         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | EN0PPS      | O                          | LVC MOS                    | PJ0 (5)          |                             | N/A                                      |
|            | U3Rx        | I                          | LVC MOS                    | PJ0 (1)          |                             | N/A                                      |
| 117        | PJ1         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | U3Tx        | O                          | LVC MOS                    | PJ1 (1)          |                             | N/A                                      |
| 118        | PP0         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | C2+         | I                          | Analog                     | PP0              |                             | N/A                                      |
|            | SSI3XDAT2   | I/O                        | LVC MOS                    | PP0 (15)         |                             | N/A                                      |
|            | U6Rx        | I                          | LVC MOS                    | PP0 (1)          |                             | N/A                                      |
| 119        | PP1         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | C2-         | I                          | Analog                     | PP1              |                             | N/A                                      |
|            | SSI3XDAT3   | I/O                        | LVC MOS                    | PP1 (15)         |                             | N/A                                      |
|            | U6Tx        | O                          | LVC MOS                    | PP1 (1)          |                             | N/A                                      |
| 120        | PB5         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | AIN11       | I                          | Analog                     | PB5              |                             | N/A                                      |
|            | I2C5SDA     | I/O                        | LVC MOS                    | PB5 (2)          |                             | N/A                                      |
|            | SSI1CIk     | I/O                        | LVC MOS                    | PB5 (15)         |                             | N/A                                      |
|            | U0RTS       | O                          | LVC MOS                    | PB5 (1)          |                             | N/A                                      |

表 4-2. Pin Attributes (continued)

| PIN NUMBER | SIGNAL NAME | SIGNAL TYPE <sup>(1)</sup> | BUFFER TYPE <sup>(2)</sup> | PIN MUX ENCODING | POWER SOURCE <sup>(3)</sup> | STATE AFTER RESET RELEASE <sup>(4)</sup> |
|------------|-------------|----------------------------|----------------------------|------------------|-----------------------------|------------------------------------------|
| 121        | PB4         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | AIN10       | I                          | Analog                     | PB4              |                             | N/A                                      |
|            | I2C5SCL     | I/O                        | LVC MOS                    | PB4 (2)          |                             | N/A                                      |
|            | SSI1Fss     | I/O                        | LVC MOS                    | PB4 (15)         |                             | N/A                                      |
|            | U0CTS       | I                          | LVC MOS                    | PB4 (1)          |                             | N/A                                      |
| 122        | VDD         | –                          | Power                      | Fixed            | N/A                         | N/A                                      |
| 123        | PE4         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | AIN9        | I                          | Analog                     | PE4              |                             | N/A                                      |
|            | SSI1XDAT0   | I/O                        | LVC MOS                    | PE4 (15)         |                             | N/A                                      |
|            | U1RI        | I                          | LVC MOS                    | PE4 (1)          |                             | N/A                                      |
| 124        | PE5         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | AIN8        | I                          | Analog                     | PE5              |                             | N/A                                      |
|            | SSI1XDAT1   | I/O                        | LVC MOS                    | PE5 (15)         |                             | N/A                                      |
| 125        | PD4         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | AIN7        | I                          | Analog                     | PD4              |                             | N/A                                      |
|            | SSI1XDAT2   | I/O                        | LVC MOS                    | PD4 (15)         |                             | N/A                                      |
|            | T3CCP0      | I/O                        | LVC MOS                    | PD4 (3)          |                             | N/A                                      |
|            | U2Rx        | I                          | LVC MOS                    | PD4 (1)          |                             | N/A                                      |
| 126        | PD5         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | AIN6        | I                          | Analog                     | PD5              |                             | N/A                                      |
|            | SSI1XDAT3   | I/O                        | LVC MOS                    | PD5 (15)         |                             | N/A                                      |
|            | T3CCP1      | I/O                        | LVC MOS                    | PD5 (3)          |                             | N/A                                      |
|            | U2Tx        | O                          | LVC MOS                    | PD5 (1)          |                             | N/A                                      |
| 127        | PD6         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | AIN5        | I                          | Analog                     | PD6              |                             | N/A                                      |
|            | SSI2XDAT3   | I/O                        | LVC MOS                    | PD6 (15)         |                             | N/A                                      |
|            | T4CCP0      | I/O                        | LVC MOS                    | PD6 (3)          |                             | N/A                                      |
|            | U2RTS       | O                          | LVC MOS                    | PD6 (1)          |                             | N/A                                      |
|            | USB0EPEN    | O                          | LVC MOS                    | PD6 (5)          |                             | N/A                                      |
| 128        | PD7         | I/O                        | LVC MOS                    | –                | VDD                         | OFF                                      |
|            | AIN4        | I                          | Analog                     | PD7              |                             | N/A                                      |
|            | NMI         | I                          | LVC MOS                    | PD7 (8)          |                             | N/A                                      |
|            | SSI2XDAT2   | I/O                        | LVC MOS                    | PD7 (15)         |                             | N/A                                      |
|            | T4CCP1      | I/O                        | LVC MOS                    | PD7 (3)          |                             | N/A                                      |
|            | U2CTS       | I                          | LVC MOS                    | PD7 (1)          |                             | N/A                                      |
|            | USB0PFLT    | I                          | LVC MOS                    | PD7 (5)          |                             | N/A                                      |

## 4.3 Signal Descriptions

表 4-3 describes the signals. The signals are sorted by function.

**表 4-3. Signal Descriptions**

| FUNCTION                | SIGNAL NAME | PIN NO. | PIN TYPE | DESCRIPTION                                                                                                                                                                                                                                                                                                                              |
|-------------------------|-------------|---------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ADC                     | AIN0        | 12      | I        | Analog-to-digital converter input 0.                                                                                                                                                                                                                                                                                                     |
|                         | AIN1        | 13      | I        | Analog-to-digital converter input 1                                                                                                                                                                                                                                                                                                      |
|                         | AIN2        | 14      | I        | Analog-to-digital converter input 2                                                                                                                                                                                                                                                                                                      |
|                         | AIN3        | 15      | I        | Analog-to-digital converter input 3                                                                                                                                                                                                                                                                                                      |
|                         | AIN4        | 128     | I        | Analog-to-digital converter input 4                                                                                                                                                                                                                                                                                                      |
|                         | AIN5        | 127     | I        | Analog-to-digital converter input 5                                                                                                                                                                                                                                                                                                      |
|                         | AIN6        | 126     | I        | Analog-to-digital converter input 6                                                                                                                                                                                                                                                                                                      |
|                         | AIN7        | 125     | I        | Analog-to-digital converter input 7                                                                                                                                                                                                                                                                                                      |
|                         | AIN8        | 124     | I        | Analog-to-digital converter input 8                                                                                                                                                                                                                                                                                                      |
|                         | AIN9        | 123     | I        | Analog-to-digital converter input 9                                                                                                                                                                                                                                                                                                      |
|                         | AIN10       | 121     | I        | Analog-to-digital converter input 10                                                                                                                                                                                                                                                                                                     |
|                         | AIN11       | 120     | I        | Analog-to-digital converter input 11                                                                                                                                                                                                                                                                                                     |
|                         | AIN12       | 4       | I        | Analog-to-digital converter input 12                                                                                                                                                                                                                                                                                                     |
|                         | AIN13       | 3       | I        | Analog-to-digital converter input 13                                                                                                                                                                                                                                                                                                     |
|                         | AIN14       | 2       | I        | Analog-to-digital converter input 14                                                                                                                                                                                                                                                                                                     |
|                         | AIN15       | 1       | I        | Analog-to-digital converter input 15                                                                                                                                                                                                                                                                                                     |
|                         | AIN16       | 18      | I        | Analog-to-digital converter input 16                                                                                                                                                                                                                                                                                                     |
|                         | AIN17       | 19      | I        | Analog-to-digital converter input 17                                                                                                                                                                                                                                                                                                     |
|                         | AIN18       | 20      | I        | Analog-to-digital converter input 18                                                                                                                                                                                                                                                                                                     |
|                         | AIN19       | 21      | I        | Analog-to-digital converter input 19                                                                                                                                                                                                                                                                                                     |
|                         | VREFA+      | 9       | -        | A reference voltage used to specify the voltage at which the ADC converts to a maximum value. This pin is used in conjunction with GNDA. The voltage that is applied to VREFA+ is the voltage with which an AINn signal is converted to 4095. The VREFA+ voltage is limited to the range specified in the ADC electrical specifications. |
| Analog Comparators      | C0+         | 23      | I        | Analog comparator 0 positive input                                                                                                                                                                                                                                                                                                       |
|                         | C0-         | 22      | I        | Analog comparator 0 negative input                                                                                                                                                                                                                                                                                                       |
|                         | C0o         | 1<br>83 | O        | Analog comparator 0 output                                                                                                                                                                                                                                                                                                               |
|                         | C1+         | 24      | I        | Analog comparator 1 positive input                                                                                                                                                                                                                                                                                                       |
|                         | C1-         | 25      | I        | Analog comparator 1 negative input                                                                                                                                                                                                                                                                                                       |
|                         | C1o         | 2<br>84 | O        | Analog comparator 1 output                                                                                                                                                                                                                                                                                                               |
|                         | C2+         | 118     | I        | Analog comparator 2 positive input                                                                                                                                                                                                                                                                                                       |
|                         | C2-         | 119     | I        | Analog comparator 2 negative input                                                                                                                                                                                                                                                                                                       |
|                         | C2o         | 3       | O        | Analog comparator 2 output                                                                                                                                                                                                                                                                                                               |
| Controller Area Network | CAN0Rx      | 33      | I        | CAN module 0 receive                                                                                                                                                                                                                                                                                                                     |
|                         | CAN0Tx      | 34      | O        | CAN module 0 transmit                                                                                                                                                                                                                                                                                                                    |
|                         | CAN1Rx      | 95      | I        | CAN module 1 receive                                                                                                                                                                                                                                                                                                                     |
|                         | CAN1Tx      | 96      | O        | CAN module 1 transmit                                                                                                                                                                                                                                                                                                                    |

表 4-3. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NO.   | PIN TYPE | DESCRIPTION                                              |
|----------|-------------|-----------|----------|----------------------------------------------------------|
| Core     | TRCLK       | 45        | O        | Trace clock.                                             |
|          | TRD0        | 44        | O        | Trace data 0.                                            |
|          | TRD1        | 43        | O        | Trace data 1.                                            |
|          | TRD2        | 42        | O        | Trace data 2.                                            |
|          | TRD3        | 46        | O        | Trace data 3.                                            |
| Ethernet | EN0LED0     | 42<br>63  | O        | Ethernet 0 LED 0                                         |
|          | EN0LED1     | 46<br>61  | O        | Ethernet 0 LED 1                                         |
|          | EN0LED2     | 43<br>62  | O        | Ethernet 0 LED 2                                         |
|          | EN0PPS      | 49<br>116 | O        | Ethernet 0 pulse-per-second (PPS) output                 |
|          | EN0RXIN     | 53        | I/O      | Ethernet PHY negative receive differential input         |
|          | EN0RXIP     | 54        | I/O      | Ethernet PHY positive receive differential input         |
|          | EN0TXON     | 56        | I/O      | Ethernet PHY negative transmit differential output       |
|          | EN0TXOP     | 57        | I/O      | Ethernet PHY positive transmit differential output       |
|          | RBIAS       | 59        | O        | 4.87-k $\Omega$ resistor (1% precision) for Ethernet PHY |

**表 4-3. Signal Descriptions (continued)**

| FUNCTION                      | SIGNAL NAME | PIN NO.    | PIN TYPE | DESCRIPTION            |
|-------------------------------|-------------|------------|----------|------------------------|
| External Peripheral Interface | EPI0S0      | 18<br>29   | I/O      | EPI module 0 signal 0  |
|                               | EPI0S1      | 19<br>30   | I/O      | EPI module 0 signal 1  |
|                               | EPI0S2      | 20<br>31   | I/O      | EPI module 0 signal 2  |
|                               | EPI0S3      | 21<br>32   | I/O      | EPI module 0 signal 3  |
|                               | EPI0S4      | 22         | I/O      | EPI module 0 signal 4  |
|                               | EPI0S5      | 23         | I/O      | EPI module 0 signal 5  |
|                               | EPI0S6      | 24         | I/O      | EPI module 0 signal 6  |
|                               | EPI0S7      | 25         | I/O      | EPI module 0 signal 7  |
|                               | EPI0S8      | 40         | I/O      | EPI module 0 signal 8  |
|                               | EPI0S9      | 41         | I/O      | EPI module 0 signal 9  |
|                               | EPI0S10     | 50         | I/O      | EPI module 0 signal 10 |
|                               | EPI0S11     | 49         | I/O      | EPI module 0 signal 11 |
|                               | EPI0S12     | 75         | I/O      | EPI module 0 signal 12 |
|                               | EPI0S13     | 76         | I/O      | EPI module 0 signal 13 |
|                               | EPI0S14     | 77         | I/O      | EPI module 0 signal 14 |
|                               | EPI0S15     | 78         | I/O      | EPI module 0 signal 15 |
|                               | EPI0S16     | 81         | I/O      | EPI module 0 signal 16 |
|                               | EPI0S17     | 82         | I/O      | EPI module 0 signal 17 |
|                               | EPI0S18     | 83         | I/O      | EPI module 0 signal 18 |
|                               | EPI0S19     | 84         | I/O      | EPI module 0 signal 19 |
|                               | EPI0S20     | 5          | I/O      | EPI module 0 signal 20 |
|                               | EPI0S21     | 6          | I/O      | EPI module 0 signal 21 |
|                               | EPI0S22     | 11         | I/O      | EPI module 0 signal 22 |
|                               | EPI0S23     | 27         | I/O      | EPI module 0 signal 23 |
|                               | EPI0S24     | 60         | I/O      | EPI module 0 signal 24 |
|                               | EPI0S25     | 61         | I/O      | EPI module 0 signal 25 |
|                               | EPI0S26     | 85         | I/O      | EPI module 0 signal 26 |
|                               | EPI0S27     | 91         | I/O      | EPI module 0 signal 27 |
|                               | EPI0S28     | 92         | I/O      | EPI module 0 signal 28 |
|                               | EPI0S29     | 103<br>109 | I/O      | EPI module 0 signal 29 |
|                               | EPI0S30     | 104<br>110 | I/O      | EPI module 0 signal 30 |
|                               | EPI0S31     | 62         | I/O      | EPI module 0 signal 31 |
|                               | EPI0S32     | 63         | I/O      | EPI module 0 signal 32 |
|                               | EPI0S33     | 86         | I/O      | EPI module 0 signal 33 |
|                               | EPI0S34     | 111        | I/O      | EPI module 0 signal 34 |
|                               | EPI0S35     | 112        | I/O      | EPI module 0 signal 35 |

表 4-3. Signal Descriptions (continued)

| FUNCTION               | SIGNAL NAME | PIN NO.         | PIN TYPE | DESCRIPTION                             |
|------------------------|-------------|-----------------|----------|-----------------------------------------|
| General-Purpose Timers | T0CCP0      | 1<br>33<br>85   | I/O      | 16/32-Bit Timer 0 Capture/Compare/PWM 0 |
|                        | T0CCP1      | 2<br>34<br>86   | I/O      | 16/32-Bit Timer 0 Capture/Compare/PWM 1 |
|                        | T1CCP0      | 3<br>35<br>94   | I/O      | 16/32-Bit Timer 1 Capture/Compare/PWM 0 |
|                        | T1CCP1      | 4<br>36<br>93   | I/O      | 16/32-Bit Timer 1 Capture/Compare/PWM 1 |
|                        | T2CCP0      | 37<br>78        | I/O      | 16/32-Bit Timer 2 Capture/Compare/PWM 0 |
|                        | T2CCP1      | 38<br>77        | I/O      | 16/32-Bit Timer 2 Capture/Compare/PWM 1 |
|                        | T3CCP0      | 40<br>76<br>125 | I/O      | 16/32-Bit Timer 3 Capture/Compare/PWM 0 |
|                        | T3CCP1      | 41<br>75<br>126 | I/O      | 16/32-Bit Timer 3 Capture/Compare/PWM 1 |
|                        | T4CCP0      | 74<br>95<br>127 | I/O      | 16/32-Bit Timer 4 Capture/Compare/PWM 0 |
|                        | T4CCP1      | 73<br>96<br>128 | I/O      | 16/32-Bit Timer 4 Capture/Compare/PWM 1 |
|                        | T5CCP0      | 72<br>91        | I/O      | 16/32-Bit Timer 5 Capture/Compare/PWM 0 |
|                        | T5CCP1      | 71<br>92        | I/O      | 16/32-Bit Timer 5 Capture/Compare/PWM 1 |
| GPIO, Port A           | PA0         | 33              | I/O      | GPIO port A bit 0                       |
|                        | PA1         | 34              | I/O      | GPIO port A bit 1                       |
|                        | PA2         | 35              | I/O      | GPIO port A bit 2                       |
|                        | PA3         | 36              | I/O      | GPIO port A bit 3                       |
|                        | PA4         | 37              | I/O      | GPIO port A bit 4                       |
|                        | PA5         | 38              | I/O      | GPIO port A bit 5                       |
|                        | PA6         | 40              | I/O      | GPIO port A bit 6                       |
|                        | PA7         | 41              | I/O      | GPIO port A bit 7                       |
| GPIO, Port B           | PB0         | 95              | I/O      | GPIO port B bit 0                       |
|                        | PB1         | 96              | I/O      | GPIO port B bit 1                       |
|                        | PB2         | 91              | I/O      | GPIO port B bit 2                       |
|                        | PB3         | 92              | I/O      | GPIO port B bit 3                       |
|                        | PB4         | 121             | I/O      | GPIO port B bit 4                       |
|                        | PB5         | 120             | I/O      | GPIO port B bit 5                       |
| GPIO, Port C           | PC0         | 100             | I/O      | GPIO port C bit 0                       |
|                        | PC1         | 99              | I/O      | GPIO port C bit 1                       |
|                        | PC2         | 98              | I/O      | GPIO port C bit 2                       |
|                        | PC3         | 97              | I/O      | GPIO port C bit 3                       |
|                        | PC4         | 25              | I/O      | GPIO port C bit 4                       |
|                        | PC5         | 24              | I/O      | GPIO port C bit 5                       |
|                        | PC6         | 23              | I/O      | GPIO port C bit 6                       |
|                        | PC7         | 22              | I/O      | GPIO port C bit 7                       |

**表 4-3. Signal Descriptions (continued)**

| FUNCTION     | SIGNAL NAME | PIN NO. | PIN TYPE | DESCRIPTION       |
|--------------|-------------|---------|----------|-------------------|
| GPIO, Port D | PD0         | 1       | I/O      | GPIO port D bit 0 |
|              | PD1         | 2       | I/O      | GPIO port D bit 1 |
|              | PD2         | 3       | I/O      | GPIO port D bit 2 |
|              | PD3         | 4       | I/O      | GPIO port D bit 3 |
|              | PD4         | 125     | I/O      | GPIO port D bit 4 |
|              | PD5         | 126     | I/O      | GPIO port D bit 5 |
|              | PD6         | 127     | I/O      | GPIO port D bit 6 |
|              | PD7         | 128     | I/O      | GPIO port D bit 7 |
| GPIO, Port E | PE0         | 15      | I/O      | GPIO port E bit 0 |
|              | PE1         | 14      | I/O      | GPIO port E bit 1 |
|              | PE2         | 13      | I/O      | GPIO port E bit 2 |
|              | PE3         | 12      | I/O      | GPIO port E bit 3 |
|              | PE4         | 123     | I/O      | GPIO port E bit 4 |
|              | PE5         | 124     | I/O      | GPIO port E bit 5 |
| GPIO, Port F | PF0         | 42      | I/O      | GPIO port F bit 0 |
|              | PF1         | 43      | I/O      | GPIO port F bit 1 |
|              | PF2         | 44      | I/O      | GPIO port F bit 2 |
|              | PF3         | 45      | I/O      | GPIO port F bit 3 |
|              | PF4         | 46      | I/O      | GPIO port F bit 4 |
| GPIO, Port G | PG0         | 49      | I/O      | GPIO port G bit 0 |
|              | PG1         | 50      | I/O      | GPIO port G bit 1 |
| GPIO, Port H | PH0         | 29      | I/O      | GPIO port H bit 0 |
|              | PH1         | 30      | I/O      | GPIO port H bit 1 |
|              | PH2         | 31      | I/O      | GPIO port H bit 2 |
|              | PH3         | 32      | I/O      | GPIO port H bit 3 |
| GPIO, Port J | PJ0         | 116     | I/O      | GPIO port J bit 0 |
|              | PJ1         | 117     | I/O      | GPIO port J bit 1 |
| GPIO, Port K | PK0         | 18      | I/O      | GPIO port K bit 0 |
|              | PK1         | 19      | I/O      | GPIO port K bit 1 |
|              | PK2         | 20      | I/O      | GPIO port K bit 2 |
|              | PK3         | 21      | I/O      | GPIO port K bit 3 |
|              | PK4         | 63      | I/O      | GPIO port K bit 4 |
|              | PK5         | 62      | I/O      | GPIO port K bit 5 |
|              | PK6         | 61      | I/O      | GPIO port K bit 6 |
|              | PK7         | 60      | I/O      | GPIO port K bit 7 |
| GPIO, Port L | PL0         | 81      | I/O      | GPIO port L bit 0 |
|              | PL1         | 82      | I/O      | GPIO port L bit 1 |
|              | PL2         | 83      | I/O      | GPIO port L bit 2 |
|              | PL3         | 84      | I/O      | GPIO port L bit 3 |
|              | PL4         | 85      | I/O      | GPIO port L bit 4 |
|              | PL5         | 86      | I/O      | GPIO port L bit 5 |
|              | PL6         | 94      | I/O      | GPIO port L bit 6 |
|              | PL7         | 93      | I/O      | GPIO port L bit 7 |

表 4-3. Signal Descriptions (continued)

| FUNCTION     | SIGNAL NAME              | PIN NO.         | PIN TYPE | DESCRIPTION                                                                                                                                                                          |
|--------------|--------------------------|-----------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GPIO, Port M | PM0                      | 78              | I/O      | GPIO port M bit 0                                                                                                                                                                    |
|              | PM1                      | 77              | I/O      | GPIO port M bit 1                                                                                                                                                                    |
|              | PM2                      | 76              | I/O      | GPIO port M bit 2                                                                                                                                                                    |
|              | PM3                      | 75              | I/O      | GPIO port M bit 3                                                                                                                                                                    |
|              | PM4                      | 74              | I/O      | GPIO port M bit 4                                                                                                                                                                    |
|              | PM5                      | 73              | I/O      | GPIO port M bit 5                                                                                                                                                                    |
|              | PM6                      | 72              | I/O      | GPIO port M bit 6                                                                                                                                                                    |
|              | PM7                      | 71              | I/O      | GPIO port M bit 7                                                                                                                                                                    |
| GPIO, Port N | PN0                      | 107             | I/O      | GPIO port N bit 0                                                                                                                                                                    |
|              | PN1                      | 108             | I/O      | GPIO port N bit 1                                                                                                                                                                    |
|              | PN2                      | 109             | I/O      | GPIO port N bit 2                                                                                                                                                                    |
|              | PN3                      | 110             | I/O      | GPIO port N bit 3                                                                                                                                                                    |
|              | PN4                      | 111             | I/O      | GPIO port N bit 4                                                                                                                                                                    |
|              | PN5                      | 112             | I/O      | GPIO port N bit 5                                                                                                                                                                    |
| GPIO, Port P | PP0                      | 118             | I/O      | GPIO port P bit 0                                                                                                                                                                    |
|              | PP1                      | 119             | I/O      | GPIO port P bit 1                                                                                                                                                                    |
|              | PP2                      | 103             | I/O      | GPIO port P bit 2                                                                                                                                                                    |
|              | PP3                      | 104             | I/O      | GPIO port P bit 3                                                                                                                                                                    |
|              | PP4                      | 105             | I/O      | GPIO port P bit 4                                                                                                                                                                    |
|              | PP5                      | 106             | I/O      | GPIO port P bit 5                                                                                                                                                                    |
| GPIO, Port Q | PQ0                      | 5               | I/O      | GPIO port Q bit 0                                                                                                                                                                    |
|              | PQ1                      | 6               | I/O      | GPIO port Q bit 1                                                                                                                                                                    |
|              | PQ2                      | 11              | I/O      | GPIO port Q bit 2                                                                                                                                                                    |
|              | PQ3                      | 27              | I/O      | GPIO port Q bit 3                                                                                                                                                                    |
|              | PQ4                      | 102             | I/O      | GPIO port Q bit 4                                                                                                                                                                    |
| Hibernate    | HIB                      | 65              | O        | An output that indicates the processor is in Hibernate mode                                                                                                                          |
|              | RTCCLK                   | 24<br>60<br>104 | O        | Buffered version of the Hibernation module's 32.768-kHz clock. This signal is not output when the part is in Hibernate mode and before being configured after power-on reset.        |
|              | TMPR0                    | 71              | I/O      | Tamper signal 0                                                                                                                                                                      |
|              | TMPR1                    | 72              | I/O      | Tamper signal 1                                                                                                                                                                      |
|              | TMPR2                    | 73              | I/O      | Tamper signal 2                                                                                                                                                                      |
|              | TMPR3                    | 74              | I/O      | Tamper signal 3                                                                                                                                                                      |
|              | VBAT                     | 68              | -        | Power source for the Hibernation module. It is normally connected to the positive terminal of a battery and serves as the battery backup and Hibernation module power-source supply. |
|              | $\overline{\text{WAKE}}$ | 64              | I        | An external input that brings the processor out of Hibernate mode when asserted                                                                                                      |
|              | XOSC0                    | 66              | I        | Hibernation module oscillator crystal input or an external clock reference input. This is either a crystal or a 32.768-kHz oscillator for the Hibernation module RTC.                |
|              | XOSC1                    | 67              | O        | Hibernation module oscillator crystal output. Leave unconnected when using a single-ended clock source.                                                                              |

**表 4-3. Signal Descriptions (continued)**

| FUNCTION         | SIGNAL NAME | PIN NO.          | PIN TYPE | DESCRIPTION                                                                                                                           |
|------------------|-------------|------------------|----------|---------------------------------------------------------------------------------------------------------------------------------------|
| I <sup>2</sup> C | I2C0SCL     | 91               | I/O      | I <sup>2</sup> C module 0 clock. This signal has an active pullup. The corresponding port pin should not be configured as open drain. |
|                  | I2C0SDA     | 92               | I/O      | I <sup>2</sup> C module 0 data                                                                                                        |
|                  | I2C1SCL     | 49               | I/O      | I <sup>2</sup> C module 1 clock. This signal has an active pullup. The corresponding port pin should not be configured as open drain. |
|                  | I2C1SDA     | 50               | I/O      | I <sup>2</sup> C module 1 data                                                                                                        |
|                  | I2C2SCL     | 82<br>106<br>112 | I/O      | I <sup>2</sup> C module 2 clock. This signal has an active pullup. The corresponding port pin should not be configured as open drain. |
|                  | I2C2SDA     | 81<br>111        | I/O      | I <sup>2</sup> C module 2 data                                                                                                        |
|                  | I2C3SCL     | 63               | I/O      | I <sup>2</sup> C module 3 clock. This signal has an active pullup. The corresponding port pin should not be configured as open drain. |
|                  | I2C3SDA     | 62               | I/O      | I <sup>2</sup> C module 3 data                                                                                                        |
|                  | I2C4SCL     | 61               | I/O      | I <sup>2</sup> C module 4 clock. This signal has an active pullup. The corresponding port pin should not be configured as open drain. |
|                  | I2C4SDA     | 60               | I/O      | I <sup>2</sup> C module 4 data                                                                                                        |
|                  | I2C5SCL     | 95<br>121        | I/O      | I <sup>2</sup> C module 5 clock. This signal has an active pullup. The corresponding port pin should not be configured as open drain. |
|                  | I2C5SDA     | 96<br>120        | I/O      | I <sup>2</sup> C module 5 data                                                                                                        |
|                  | I2C6SCL     | 40               | I/O      | I <sup>2</sup> C module 6 clock. This signal has an active pullup. The corresponding port pin should not be configured as open drain. |
|                  | I2C6SDA     | 41               | I/O      | I <sup>2</sup> C module 6 data                                                                                                        |
|                  | I2C7SCL     | 1<br>37          | I/O      | I <sup>2</sup> C module 7 clock. This signal has an active pullup. The corresponding port pin should not be configured as open drain. |
|                  | I2C7SDA     | 2<br>38          | I/O      | I <sup>2</sup> C module 7 data                                                                                                        |
|                  | I2C8SCL     | 3<br>35          | I/O      | I <sup>2</sup> C module 8 clock. This signal has an active pullup. The corresponding port pin should not be configured as open drain. |
|                  | I2C8SDA     | 4<br>36          | I/O      | I <sup>2</sup> C module 8 data                                                                                                        |
|                  | I2C9SCL     | 33               | I/O      | I <sup>2</sup> C module 9 clock. This signal has an active pullup. The corresponding port pin should not be configured as open drain. |
|                  | I2C9SDA     | 34               | I/O      | I <sup>2</sup> C module 9 data                                                                                                        |
| JTAG, SWD, SWO   | TCK/SWCLK   | 100              | I        | JTAG/SWD clock                                                                                                                        |
|                  | TDI         | 98               | I        | JTAG TDI                                                                                                                              |
|                  | TDO/SWO     | 97               | O        | JTAG TDO and SWO                                                                                                                      |
|                  | TMS/SWDIO   | 99               | I        | JTAG TMS and SWDIO                                                                                                                    |

表 4-3. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NO.                                                                            | PIN TYPE | DESCRIPTION                                                                                                                                                                                                                                                                                                               |
|----------|-------------|------------------------------------------------------------------------------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PWM      | M0FAULT0    | 46                                                                                 | I        | Motion Control module 0 PWM fault 0                                                                                                                                                                                                                                                                                       |
|          | M0FAULT1    | 61                                                                                 | I        | Motion Control module 0 PWM fault 1                                                                                                                                                                                                                                                                                       |
|          | M0FAULT2    | 60                                                                                 | I        | Motion Control module 0 PWM fault 2                                                                                                                                                                                                                                                                                       |
|          | M0FAULT3    | 81                                                                                 | I        | Motion Control module 0 PWM fault 3                                                                                                                                                                                                                                                                                       |
|          | M0PWM0      | 42                                                                                 | O        | Motion Control module 0 PWM 0. This signal is controlled by module 0 PWM generator 0.                                                                                                                                                                                                                                     |
|          | M0PWM1      | 43                                                                                 | O        | Motion Control module 0 PWM 1. This signal is controlled by module 0 PWM generator 0.                                                                                                                                                                                                                                     |
|          | M0PWM2      | 44                                                                                 | O        | Motion Control module 0 PWM 2. This signal is controlled by module 0 PWM generator 1.                                                                                                                                                                                                                                     |
|          | M0PWM3      | 45                                                                                 | O        | Motion Control module 0 PWM 3. This signal is controlled by module 0 PWM generator 1.                                                                                                                                                                                                                                     |
|          | M0PWM4      | 49                                                                                 | O        | Motion Control module 0 PWM 4. This signal is controlled by module 0 PWM generator 2.                                                                                                                                                                                                                                     |
|          | M0PWM5      | 50                                                                                 | O        | Motion Control module 0 PWM 5. This signal is controlled by module 0 PWM generator 2.                                                                                                                                                                                                                                     |
|          | M0PWM6      | 63                                                                                 | O        | Motion Control module 0 PWM 6. This signal is controlled by module 0 PWM generator 3.                                                                                                                                                                                                                                     |
|          | M0PWM7      | 62                                                                                 | O        | Motion Control module 0 PWM 7. This signal is controlled by module 0 PWM generator 3.                                                                                                                                                                                                                                     |
| Power    | GND         | 17<br>48<br>55<br>58<br>80<br>114                                                  | -        | Ground reference for logic and I/O pins                                                                                                                                                                                                                                                                                   |
|          | GNDA        | 10                                                                                 | -        | The ground reference for the analog circuits (ADC, Analog Comparators, etc.). These are separated from GND to minimize the electrical noise contained on VDD from affecting the analog functions                                                                                                                          |
|          | VDD         | 7<br>16<br>26<br>28<br>39<br>47<br>51<br>52<br>69<br>79<br>90<br>101<br>113<br>122 | -        | Positive supply for I/O and some logic                                                                                                                                                                                                                                                                                    |
|          | VDDA        | 8                                                                                  | -        | The positive supply for the analog circuits (for example, ADC and Analog Comparators). These are separated from VDD to minimize the electrical noise contained on VDD from affecting the analog functions. VDDA pins must be supplied with a voltage that meets the specification in, regardless of system implementation |
|          | VDDC        | 87<br>115                                                                          | -        | Positive supply for most of the logic function, including the processor core and most peripherals. The voltage on this pin is 1.2 V and is supplied by the on-chip LDO. The VDDC pins should only be connected to each other and an external capacitor as specified in the LDO electrical specifications.                 |
| QEI      | IDX0        | 84                                                                                 | I        | QEI module 0 index                                                                                                                                                                                                                                                                                                        |
|          | PhA0        | 82                                                                                 | I        | QEI module 0 phase A                                                                                                                                                                                                                                                                                                      |
|          | PhB0        | 83                                                                                 | I        | QEI module 0 phase B                                                                                                                                                                                                                                                                                                      |

**表 4-3. Signal Descriptions (continued)**

| FUNCTION                  | SIGNAL NAME | PIN NO.   | PIN TYPE | DESCRIPTION                                                                                                                         |
|---------------------------|-------------|-----------|----------|-------------------------------------------------------------------------------------------------------------------------------------|
| SSI                       | SSI0Clk     | 35        | I/O      | SSI module 0 clock                                                                                                                  |
|                           | SSI0Fss     | 36        | I/O      | SSI module 0 frame signal                                                                                                           |
|                           | SSI0XDAT0   | 37        | I/O      | SSI module 0 bidirectional data pin 0 (SSI0TX in Legacy SSI mode)                                                                   |
|                           | SSI0XDAT1   | 38        | I/O      | SSI module 0 bidirectional data pin 1 (SSI0RX in Legacy SSI mode)                                                                   |
|                           | SSI0XDAT2   | 40        | I/O      | SSI module 0 bidirectional data pin 2                                                                                               |
|                           | SSI0XDAT3   | 41        | I/O      | SSI module 0 bidirectional data pin 3                                                                                               |
|                           | SSI1Clk     | 120       | I/O      | SSI module 1 clock                                                                                                                  |
|                           | SSI1Fss     | 121       | I/O      | SSI module 1 frame signal                                                                                                           |
|                           | SSI1XDAT0   | 123       | I/O      | SSI module 1 bidirectional data pin 0 (SSI1TX in Legacy SSI mode)                                                                   |
|                           | SSI1XDAT1   | 124       | I/O      | SSI module 1 bidirectional data pin 1 (SSI1RX in Legacy SSI mode)                                                                   |
|                           | SSI1XDAT2   | 125       | I/O      | SSI module 1 bidirectional data pin 2                                                                                               |
|                           | SSI1XDAT3   | 126       | I/O      | SSI module 1 bidirectional data pin 3                                                                                               |
|                           | SSI2Clk     | 4         | I/O      | SSI module 2 clock                                                                                                                  |
|                           | SSI2Fss     | 3         | I/O      | SSI module 2 frame signal                                                                                                           |
|                           | SSI2XDAT0   | 2         | I/O      | SSI module 2 bidirectional data pin 0 (SSI2TX in Legacy SSI mode)                                                                   |
|                           | SSI2XDAT1   | 1         | I/O      | SSI module 2 bidirectional data pin 1 (SSI2RX in Legacy SSI mode)                                                                   |
|                           | SSI2XDAT2   | 128       | I/O      | SSI module 2 bidirectional data pin 2                                                                                               |
|                           | SSI2XDAT3   | 127       | I/O      | SSI module 2 bidirectional data pin 3                                                                                               |
|                           | SSI3Clk     | 5<br>45   | I/O      | SSI module 3 clock                                                                                                                  |
|                           | SSI3Fss     | 6<br>44   | I/O      | SSI module 3 frame signal                                                                                                           |
|                           | SSI3XDAT0   | 11<br>43  | I/O      | SSI module 3 bidirectional data pin 0 (SSI3TX in Legacy SSI mode)                                                                   |
|                           | SSI3XDAT1   | 27<br>42  | I/O      | SSI module 3 bidirectional data pin 1 (SSI3RX in Legacy SSI mode)                                                                   |
|                           | SSI3XDAT2   | 46<br>118 | I/O      | SSI module 3 bidirectional data pin 2                                                                                               |
|                           | SSI3XDAT3   | 119       | I/O      | SSI module 3 bidirectional data pin 3                                                                                               |
| System Control and Clocks | DIVSCLK     | 102       | O        | An optionally divided reference clock output based on a selected clock source. This signal is not synchronized to the system clock. |
|                           | NMI         | 128       | I        | Nonmaskable interrupt                                                                                                               |
|                           | OSC0        | 88        | I        | Main oscillator crystal input or an external clock reference input                                                                  |
|                           | OSC1        | 89        | O        | Main oscillator crystal output. Leave unconnected when using a single-ended clock source.                                           |
|                           | RST         | 70        | I        | System reset input                                                                                                                  |

表 4-3. Signal Descriptions (continued)

| FUNCTION      | SIGNAL NAME | PIN NO.         | PIN TYPE | DESCRIPTION                                                    |
|---------------|-------------|-----------------|----------|----------------------------------------------------------------|
| UART Module 0 | U0CTS       | 30<br>74<br>121 | I        | UART module 0 Clear To Send modem flow control input signal    |
|               | U0DCD       | 31<br>73<br>104 | I        | UART module 0 Data Carrier Detect modem status input signal    |
|               | U0DSR       | 32<br>72<br>105 | I        | UART module 0 Data Set Ready modem output control line         |
|               | U0DTR       | 103             | O        | UART module 0 Data Terminal Ready modem status input signal    |
|               | U0RI        | 60<br>71        | I        | UART module 0 Ring Indicator modem status input signal         |
|               | U0RTS       | 29<br>120       | O        | UART module 0 Request to Send modem flow control output signal |
|               | U0Rx        | 33              | I        | UART module 0 receive                                          |
|               | U0Tx        | 34              | O        | UART module 0 transmit                                         |
| UART Module 1 | U1CTS       | 104<br>108      | I        | UART module 1 Clear To Send modem flow control input signal    |
|               | U1DCD       | 13<br>109       | I        | UART module 1 Data Carrier Detect modem status input signal    |
|               | U1DSR       | 14<br>110       | I        | UART module 1 Data Set Ready modem output control line         |
|               | U1DTR       | 12<br>111       | O        | UART module 1 Data Terminal Ready modem status input signal    |
|               | U1RI        | 112<br>123      | I        | UART module 1 Ring Indicator modem status input signal         |
|               | U1RTS       | 15<br>107       | O        | UART module 1 Request to Send modem flow control output line   |
|               | U1Rx        | 95<br>102       | I        | UART module 1 receive.                                         |
|               | U1Tx        | 96              | O        | UART module 1 transmit                                         |
| UART Module 2 | U2CTS       | 110<br>128      | I        | UART module 2 Clear To Send modem flow control input signal    |
|               | U2RTS       | 109<br>127      | O        | UART module 2 Request to Send modem flow control output line   |
|               | U2Rx        | 40<br>125       | I        | UART module 2 receive                                          |
|               | U2Tx        | 41<br>126       | O        | UART module 2 transmit                                         |
| UART Module 3 | U3CTS       | 106<br>112      | I        | UART module 3 Clear To Send modem flow control input signal    |
|               | U3RTS       | 105<br>111      | O        | UART module 3 Request to Send modem flow control output line   |
|               | U3Rx        | 37<br>116       | I        | UART module 3 receive                                          |
|               | U3Tx        | 38<br>117       | O        | UART module 3 transmit                                         |
| UART Module 4 | U4CTS       | 21              | I        | UART module 4 Clear To Send modem flow control input signal    |
|               | U4RTS       | 20              | O        | UART module 4 Request to Send modem flow control output line   |
|               | U4Rx        | 18<br>35        | I        | UART module 4 receive                                          |
|               | U4Tx        | 19<br>36        | O        | UART module 4 transmit                                         |

**表 4-3. Signal Descriptions (continued)**

| FUNCTION      | SIGNAL NAME | PIN NO.         | PIN TYPE | DESCRIPTION                                                                                                                                                                                                                                                   |
|---------------|-------------|-----------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| UART Module 5 | U5Rx        | 23              | I        | UART module 5 receive                                                                                                                                                                                                                                         |
|               | U5Tx        | 22              | O        | UART module 5 transmit                                                                                                                                                                                                                                        |
| UART Module 6 | U6Rx        | 118             | I        | UART module 6 receive                                                                                                                                                                                                                                         |
|               | U6Tx        | 119             | O        | UART module 6 transmit                                                                                                                                                                                                                                        |
| UART Module 7 | U7Rx        | 25              | I        | UART module 7 receive                                                                                                                                                                                                                                         |
|               | U7Tx        | 24              | O        | UART module 7 transmit                                                                                                                                                                                                                                        |
| USB           | USB0CLK     | 92              | O        | 60-MHz clock to the external PHY                                                                                                                                                                                                                              |
|               | USB0D0      | 81              | I/O      | USB data 0                                                                                                                                                                                                                                                    |
|               | USB0D1      | 82              | I/O      | USB data 1                                                                                                                                                                                                                                                    |
|               | USB0D2      | 83              | I/O      | USB data 2                                                                                                                                                                                                                                                    |
|               | USB0D3      | 84              | I/O      | USB data 3                                                                                                                                                                                                                                                    |
|               | USB0D4      | 85              | I/O      | USB data 4                                                                                                                                                                                                                                                    |
|               | USB0D5      | 86              | I/O      | USB data 5                                                                                                                                                                                                                                                    |
|               | USB0D6      | 106             | I/O      | USB data 6                                                                                                                                                                                                                                                    |
|               | USB0D7      | 105             | I/O      | USB data 7                                                                                                                                                                                                                                                    |
|               | USB0DIR     | 104             | O        | Indicates that the external PHY is able to accept data from the USB controller                                                                                                                                                                                |
|               | USB0DM      | 93              | I/O      | Bidirectional differential data pin (D– per USB specification) for USB0                                                                                                                                                                                       |
|               | USB0DP      | 94              | I/O      | Bidirectional differential data pin (D+ per USB specification) for USB0                                                                                                                                                                                       |
|               | USB0EPEN    | 40<br>41<br>127 | O        | Optionally used in Host mode to control an external power source to supply power to the USB bus                                                                                                                                                               |
|               | USB0ID      | 95              | I        | This signal senses the state of the USB ID signal. The USB PHY enables an integrated pull-up, and an external element (USB connector) indicates the initial state of the USB controller (pulled down is the A side of the cable and pulled up is the B side). |
|               | USB0NXT     | 103             | O        | Asserted by the external PHY to throttle all data types                                                                                                                                                                                                       |
|               | USB0PFLT    | 41<br>128       | I        | Optionally used in Host mode by an external power source to indicate an error state by that power source                                                                                                                                                      |
|               | USB0STP     | 91              | O        | Asserted by the USB controller to signal the end of a USB transmit packet or register write operation                                                                                                                                                         |
|               | USB0VBUS    | 96              | I/O      | This signal is used during the session request protocol. This signal allows the USB PHY to both sense the voltage level of VBUS, and pull up VBUS momentarily during VBUS pulsing.                                                                            |

## 4.4 GPIO Pin Multiplexing

表 4-4 lists the GPIO pins and their analog and digital alternate functions. The AINx analog signals go through an isolation circuit before reaching their circuitry. These signals are configured by clearing the corresponding DEN bit in the GPIO Digital Enable (GPIODEN) register and setting the corresponding AMSEL bit in the GPIO Analog Mode Select (GPIOAMSEL) register. Other analog signals are 3.3-V tolerant and are connected directly to their circuitry (C0-, C0+, C1-, C1+, C2-, C2+, USB0VBUS, USB0ID). These signals are configured by clearing the DEN bit in the GPIODEN register. The digital signals are enabled by setting the appropriate bit in the GPIO Alternate Function Select (GPIOAFSEL) and GPIODEN registers and configuring the PMCx bit field in the GPIO Port Control (GPIOPCTL) register to the numeric encoding shown in 表 4-4.

表 4-4. GPIO Pins and Alternate Functions

| I/O | PIN | ANALOG<br>OR<br>SPECIAL<br>FUNCTION<br>(1) | DIGITAL FUNCTION (GPIOPCTL PMCx BIT FIELD ENCODING) |         |        |   |          |   |         |   |          |           |         |           |
|-----|-----|--------------------------------------------|-----------------------------------------------------|---------|--------|---|----------|---|---------|---|----------|-----------|---------|-----------|
|     |     |                                            | 1                                                   | 2       | 3      | 4 | 5        | 6 | 7       | 8 | 11       | 13        | 14      | 15        |
| PA0 | 33  | –                                          | U0Rx                                                | I2C9SCL | T0CCP0 | – | –        | – | CAN0Rx  | – | –        | –         | –       | –         |
| PA1 | 34  | –                                          | U0Tx                                                | I2C9SDA | T0CCP1 | – | –        | – | CAN0Tx  | – | –        | –         | –       | –         |
| PA2 | 35  | –                                          | U4Rx                                                | I2C8SCL | T1CCP0 | – | –        | – | –       | – | –        | –         | –       | SSI0Clk   |
| PA3 | 36  | –                                          | U4Tx                                                | I2C8SDA | T1CCP1 | – | –        | – | –       | – | –        | –         | –       | SSI0Fss   |
| PA4 | 37  | –                                          | U3Rx                                                | I2C7SCL | T2CCP0 | – | –        | – | –       | – | –        | –         | –       | SSI0XDAT0 |
| PA5 | 38  | –                                          | U3Tx                                                | I2C7SDA | T2CCP1 | – | –        | – | –       | – | –        | –         | –       | SSI0XDAT1 |
| PA6 | 40  | –                                          | U2Rx                                                | I2C6SCL | T3CCP0 | – | USB0EPEN | – | –       | – | –        | SSI0XDAT2 | –       | EPI0S8    |
| PA7 | 41  | –                                          | U2Tx                                                | I2C6SDA | T3CCP1 | – | USB0PFLT | – | –       | – | USB0EPEN | SSI0XDAT3 | –       | EPI0S9    |
| PB0 | 95  | USB0ID                                     | U1Rx                                                | I2C5SCL | T4CCP0 | – | –        | – | CAN1Rx  | – | –        | –         | –       | –         |
| PB1 | 96  | USB0VBUS                                   | U1Tx                                                | I2C5SDA | T4CCP1 | – | –        | – | CAN1Tx  | – | –        | –         | –       | –         |
| PB2 | 91  | –                                          | –                                                   | I2C0SCL | T5CCP0 | – | –        | – | –       | – | –        | –         | USB0STP | EPI0S27   |
| PB3 | 92  | –                                          | –                                                   | I2C0SDA | T5CCP1 | – | –        | – | –       | – | –        | –         | USB0CLK | EPI0S28   |
| PB4 | 121 | AIN10                                      | U0CTS                                               | I2C5SCL | –      | – | –        | – | –       | – | –        | –         | –       | SSI1Fss   |
| PB5 | 120 | AIN11                                      | U0RTS                                               | I2C5SDA | –      | – | –        | – | –       | – | –        | –         | –       | SSI1Clk   |
| PC0 | 100 | –                                          | TCK SWCLK                                           | –       | –      | – | –        | – | –       | – | –        | –         | –       | –         |
| PC1 | 99  | –                                          | TMS SWDIO                                           | –       | –      | – | –        | – | –       | – | –        | –         | –       | –         |
| PC2 | 98  | –                                          | TDI                                                 | –       | –      | – | –        | – | –       | – | –        | –         | –       | –         |
| PC3 | 97  | –                                          | TDO SWO                                             | –       | –      | – | –        | – | –       | – | –        | –         | –       | –         |
| PC4 | 25  | C1-                                        | U7Rx                                                | –       | –      | – | –        | – | –       | – | –        | –         | –       | EPI0S7    |
| PC5 | 24  | C1+                                        | U7Tx                                                | –       | –      | – | –        | – | RTCCCLK | – | –        | –         | –       | EPI0S6    |
| PC6 | 23  | C0+                                        | U5Rx                                                | –       | –      | – | –        | – | –       | – | –        | –         | –       | EPI0S5    |
| PC7 | 22  | C0-                                        | U5Tx                                                | –       | –      | – | –        | – | –       | – | –        | –         | –       | EPI0S4    |
| PD0 | 1   | AIN15                                      | –                                                   | I2C7SCL | T0CCP0 | – | C0o      | – | –       | – | –        | –         | –       | SSI2XDAT1 |
| PD1 | 2   | AIN14                                      | –                                                   | I2C7SDA | T0CCP1 | – | C1o      | – | –       | – | –        | –         | –       | SSI2XDAT0 |

(1) The TMPRn signals are digital signals enabled and configured by the Hibernation module. All other signals listed in this column are analog signals.

表 4-4. GPIO Pins and Alternate Functions (continued)

| I/O | PIN | ANALOG<br>OR<br>SPECIAL<br>FUNCTION<br>(1) | DIGITAL FUNCTION (GPIOCTL PMCx BIT FIELD ENCODING) |         |        |   |          |          |   |     |    |    |           |           |
|-----|-----|--------------------------------------------|----------------------------------------------------|---------|--------|---|----------|----------|---|-----|----|----|-----------|-----------|
|     |     |                                            | 1                                                  | 2       | 3      | 4 | 5        | 6        | 7 | 8   | 11 | 13 | 14        | 15        |
| PD2 | 3   | AIN13                                      | –                                                  | I2C8SCL | T1CCP0 | – | C2o      | –        | – | –   | –  | –  | –         | SSI2Fss   |
| PD3 | 4   | AIN12                                      | –                                                  | I2C8SDA | T1CCP1 | – | –        | –        | – | –   | –  | –  | –         | SSI2Clk   |
| PD4 | 125 | AIN7                                       | U2Rx                                               | –       | T3CCP0 | – | –        | –        | – | –   | –  | –  | –         | SSI1XDAT2 |
| PD5 | 126 | AIN6                                       | U2Tx                                               | –       | T3CCP1 | – | –        | –        | – | –   | –  | –  | –         | SSI1XDAT3 |
| PD6 | 127 | AIN5                                       | U2RTS                                              | –       | T4CCP0 | – | USB0EPEN | –        | – | –   | –  | –  | –         | SSI2XDAT3 |
| PD7 | 128 | AIN4                                       | U2CTS                                              | –       | T4CCP1 | – | USB0PFLT | –        | – | NMI | –  | –  | –         | SSI2XDAT2 |
| PE0 | 15  | AIN3                                       | U1RTS                                              | –       | –      | – | –        | –        | – | –   | –  | –  | –         | –         |
| PE1 | 14  | AIN2                                       | U1DSR                                              | –       | –      | – | –        | –        | – | –   | –  | –  | –         | –         |
| PE2 | 13  | AIN1                                       | U1DCD                                              | –       | –      | – | –        | –        | – | –   | –  | –  | –         | –         |
| PE3 | 12  | AIN0                                       | U1DTR                                              | –       | –      | – | –        | –        | – | –   | –  | –  | –         | –         |
| PE4 | 123 | AIN9                                       | U1RI                                               | –       | –      | – | –        | –        | – | –   | –  | –  | –         | SSI1XDAT0 |
| PE5 | 124 | AIN8                                       | –                                                  | –       | –      | – | –        | –        | – | –   | –  | –  | –         | SSI1XDAT1 |
| PF0 | 42  | –                                          | –                                                  | –       | –      | – | EN0LED0  | M0PWM0   | – | –   | –  | –  | SSI3XDAT1 | TRD2      |
| PF1 | 43  | –                                          | –                                                  | –       | –      | – | EN0LED2  | M0PWM1   | – | –   | –  | –  | SSI3XDAT0 | TRD1      |
| PF2 | 44  | –                                          | –                                                  | –       | –      | – | –        | M0PWM2   | – | –   | –  | –  | SSI3Fss   | TRD0      |
| PF3 | 45  | –                                          | –                                                  | –       | –      | – | –        | M0PWM3   | – | –   | –  | –  | SSI3Clk   | TRCLK     |
| PF4 | 46  | –                                          | –                                                  | –       | –      | – | EN0LED1  | M0FAULT0 | – | –   | –  | –  | SSI3XDAT2 | TRD3      |
| PG0 | 49  | –                                          | –                                                  | I2C1SCL | –      | – | EN0PPS   | M0PWM4   | – | –   | –  | –  | –         | EPI0S11   |
| PG1 | 50  | –                                          | –                                                  | I2C1SDA | –      | – | –        | M0PWM5   | – | –   | –  | –  | –         | EPI0S10   |
| PH0 | 29  | –                                          | U0RTS                                              | –       | –      | – | –        | –        | – | –   | –  | –  | –         | EPI0S0    |
| PH1 | 30  | –                                          | U0CTS                                              | –       | –      | – | –        | –        | – | –   | –  | –  | –         | EPI0S1    |
| PH2 | 31  | –                                          | U0DCD                                              | –       | –      | – | –        | –        | – | –   | –  | –  | –         | EPI0S2    |
| PH3 | 32  | –                                          | U0DSR                                              | –       | –      | – | –        | –        | – | –   | –  | –  | –         | EPI0S3    |
| PJ0 | 116 | –                                          | U3Rx                                               | –       | –      | – | EN0PPS   | –        | – | –   | –  | –  | –         | –         |
| PJ1 | 117 | –                                          | U3Tx                                               | –       | –      | – | –        | –        | – | –   | –  | –  | –         | –         |
| PK0 | 18  | AIN16                                      | U4Rx                                               | –       | –      | – | –        | –        | – | –   | –  | –  | –         | EPI0S0    |
| PK1 | 19  | AIN17                                      | U4Tx                                               | –       | –      | – | –        | –        | – | –   | –  | –  | –         | EPI0S1    |
| PK2 | 20  | AIN18                                      | U4RTS                                              | –       | –      | – | –        | –        | – | –   | –  | –  | –         | EPI0S2    |
| PK3 | 21  | AIN19                                      | U4CTS                                              | –       | –      | – | –        | –        | – | –   | –  | –  | –         | EPI0S3    |
| PK4 | 63  | –                                          | –                                                  | I2C3SCL | –      | – | EN0LED0  | M0PWM6   | – | –   | –  | –  | –         | EPI0S32   |
| PK5 | 62  | –                                          | –                                                  | I2C3SDA | –      | – | EN0LED2  | M0PWM7   | – | –   | –  | –  | –         | EPI0S31   |
| PK6 | 61  | –                                          | –                                                  | I2C4SCL | –      | – | EN0LED1  | M0FAULT1 | – | –   | –  | –  | –         | EPI0S25   |
| PK7 | 60  | –                                          | U0RI                                               | I2C4SDA | –      | – | RTCCLK   | M0FAULT2 | – | –   | –  | –  | –         | EPI0S24   |
| PL0 | 81  | –                                          | –                                                  | I2C2SDA | –      | – | –        | M0FAULT3 | – | –   | –  | –  | USB0D0    | EPI0S16   |

表 4-4. GPIO Pins and Alternate Functions (continued)

| I/O | PIN | ANALOG<br>OR<br>SPECIAL<br>FUNCTION<br>(1) | DIGITAL FUNCTION (GPIOCTL PMCx BIT FIELD ENCODING) |         |         |   |     |      |         |   |    |    |           |           |
|-----|-----|--------------------------------------------|----------------------------------------------------|---------|---------|---|-----|------|---------|---|----|----|-----------|-----------|
|     |     |                                            | 1                                                  | 2       | 3       | 4 | 5   | 6    | 7       | 8 | 11 | 13 | 14        | 15        |
| PL1 | 82  | –                                          | –                                                  | I2C2SCL | –       | – | –   | PhA0 | –       | – | –  | –  | USB0D1    | EPI0S17   |
| PL2 | 83  | –                                          | –                                                  | –       | –       | – | C0o | PhB0 | –       | – | –  | –  | USB0D2    | EPI0S18   |
| PL3 | 84  | –                                          | –                                                  | –       | –       | – | C1o | IDX0 | –       | – | –  | –  | USB0D3    | EPI0S19   |
| PL4 | 85  | –                                          | –                                                  | –       | T0CCP0  | – | –   | –    | –       | – | –  | –  | USB0D4    | EPI0S26   |
| PL5 | 86  | –                                          | –                                                  | –       | T0CCP1  | – | –   | –    | –       | – | –  | –  | USB0D5    | EPI0S33   |
| PL6 | 94  | USB0DP                                     | –                                                  | –       | T1CCP0  | – | –   | –    | –       | – | –  | –  | –         | –         |
| PL7 | 93  | USB0DM                                     | –                                                  | –       | T1CCP1  | – | –   | –    | –       | – | –  | –  | –         | –         |
| PM0 | 78  | –                                          | –                                                  | –       | T2CCP0  | – | –   | –    | –       | – | –  | –  | –         | EPI0S15   |
| PM1 | 77  | –                                          | –                                                  | –       | T2CCP1  | – | –   | –    | –       | – | –  | –  | –         | EPI0S14   |
| PM2 | 76  | –                                          | –                                                  | –       | T3CCP0  | – | –   | –    | –       | – | –  | –  | –         | EPI0S13   |
| PM3 | 75  | –                                          | –                                                  | –       | T3CCP1  | – | –   | –    | –       | – | –  | –  | –         | EPI0S12   |
| PM4 | 74  | TMPR3                                      | U0CTS                                              | –       | T4CCP0  | – | –   | –    | –       | – | –  | –  | –         | –         |
| PM5 | 73  | TMPR2                                      | U0DCD                                              | –       | T4CCP1  | – | –   | –    | –       | – | –  | –  | –         | –         |
| PM6 | 72  | TMPR1                                      | U0DSR                                              | –       | T5CCP0  | – | –   | –    | –       | – | –  | –  | –         | –         |
| PM7 | 71  | TMPR0                                      | U0RI                                               | –       | T5CCP1  | – | –   | –    | –       | – | –  | –  | –         | –         |
| PN0 | 107 | –                                          | U1RTS                                              | –       | –       | – | –   | –    | –       | – | –  | –  | –         | –         |
| PN1 | 108 | –                                          | U1CTS                                              | –       | –       | – | –   | –    | –       | – | –  | –  | –         | –         |
| PN2 | 109 | –                                          | U1DCD                                              | U2RTS   | –       | – | –   | –    | –       | – | –  | –  | –         | EPI0S29   |
| PN3 | 110 | –                                          | U1DSR                                              | U2CTS   | –       | – | –   | –    | –       | – | –  | –  | –         | EPI0S30   |
| PN4 | 111 | –                                          | U1DTR                                              | U3RTS   | I2C2SDA | – | –   | –    | –       | – | –  | –  | –         | EPI0S34   |
| PN5 | 112 | –                                          | U1RI                                               | U3CTS   | I2C2SCL | – | –   | –    | –       | – | –  | –  | –         | EPI0S35   |
| PP0 | 118 | C2+                                        | U6Rx                                               | –       | –       | – | –   | –    | –       | – | –  | –  | –         | SSI3XDAT2 |
| PP1 | 119 | C2-                                        | U6Tx                                               | –       | –       | – | –   | –    | –       | – | –  | –  | –         | SSI3XDAT3 |
| PP2 | 103 | –                                          | U0DTR                                              | –       | –       | – | –   | –    | –       | – | –  | –  | USB0NXT   | EPI0S29   |
| PP3 | 104 | –                                          | U1CTS                                              | U0DCD   | –       | – | –   | –    | RTCCLK  | – | –  | –  | USB0DIR   | EPI0S30   |
| PP4 | 105 | –                                          | U3RTS                                              | U0DSR   | –       | – | –   | –    | –       | – | –  | –  | USB0D7    | –         |
| PP5 | 106 | –                                          | U3CTS                                              | I2C2SCL | –       | – | –   | –    | –       | – | –  | –  | USB0D6    | –         |
| PQ0 | 5   | –                                          | –                                                  | –       | –       | – | –   | –    | –       | – | –  | –  | SSI3Clk   | EPI0S20   |
| PQ1 | 6   | –                                          | –                                                  | –       | –       | – | –   | –    | –       | – | –  | –  | SSI3Fss   | EPI0S21   |
| PQ2 | 11  | –                                          | –                                                  | –       | –       | – | –   | –    | –       | – | –  | –  | SSI3XDAT0 | EPI0S22   |
| PQ3 | 27  | –                                          | –                                                  | –       | –       | – | –   | –    | –       | – | –  | –  | SSI3XDAT1 | EPI0S23   |
| PQ4 | 102 | –                                          | U1Rx                                               | –       | –       | – | –   | –    | DIVSCLK | – | –  | –  | –         | –         |

## 4.5 Buffer Type

表 4-5 describes the buffer types that are referenced in 节 4.2.

表 4-5. Buffer Type

| BUFFER TYPE (STANDARD)               | NOMINAL VOLTAGE | HYSTERESIS              | PU OR PD     | NOMINAL PU OR PD STRENGTH ( $\mu$ A) | OUTPUT DRIVE STRENGTH (mA)   | OTHER CHARACTERISTICS                  |
|--------------------------------------|-----------------|-------------------------|--------------|--------------------------------------|------------------------------|----------------------------------------|
| Analog <sup>(1)</sup>                | 3.3 V           | N                       | N/A          | N/A                                  | N/A                          | See analog modules in 节 5 for details. |
| LVC MOS                              | 3.3 V           | $\gamma$ <sup>(2)</sup> | Programmable | See Input/Output Pin Characteristics | See Typical Characteristics. |                                        |
| Power (VDD) <sup>(3)</sup>           | 3.3 V           | N                       | N/A          | N/A                                  | N/A                          |                                        |
| Power (VDDA) <sup>(3)</sup>          | 3.3 V           | N                       | N/A          | N/A                                  | N/A                          |                                        |
| Power (GND and GND A) <sup>(3)</sup> | 0 V             | N                       | N/A          | N/A                                  | N/A                          |                                        |

(1) This is a switch, not a buffer.

(2) Only for input pins

(3) This is supply input, not a buffer.

## 4.6 Connections for Unused Pins

表 4-6 lists the recommended connections for unused pins.

表 4-6 lists two options: an acceptable practice and a preferred practice for reduced power consumption and improved EMC characteristics. If a module is not used in a system, and its inputs are grounded, it is important that the clock to the module is never enabled by setting the corresponding bit in the RCGCx register.

表 4-6. Connections for Unused Pins

| FUNCTION  | SIGNAL NAME              | PIN NUMBER | ACCEPTABLE PRACTICE                                 | PREFERRED PRACTICE                                  |
|-----------|--------------------------|------------|-----------------------------------------------------|-----------------------------------------------------|
| ADC       | VREF A+                  | 9          | VDDA                                                | VDDA                                                |
| Ethernet  | EN0RXIN                  | 53         | NC                                                  | NC                                                  |
|           | EN0RXIP                  | 54         | NC                                                  | NC                                                  |
|           | EN0TXON                  | 56         | NC                                                  | NC                                                  |
|           | EN0TXOP                  | 57         | NC                                                  | NC                                                  |
|           | RBIAS                    | 59         | Connect to ground through 4.87-k $\Omega$ resistor. | Connect to ground through 4.87-k $\Omega$ resistor. |
| GPIO      | PA1 (U0Tx)               | 34         | NC                                                  | GND <sup>(1)</sup>                                  |
|           | PA4 (SSI0XDAT0)          | 37         | NC                                                  | GND <sup>(2)</sup>                                  |
|           | All unused GPIOs         |            | NC                                                  | GND                                                 |
| Hibernate | $\overline{\text{HIB}}$  | 65         | NC                                                  | NC                                                  |
|           | VBAT                     | 68         | NC                                                  | VDD                                                 |
|           | $\overline{\text{WAKE}}$ | 64         | NC                                                  | GND                                                 |
|           | XOSC0                    | 66         | NC                                                  | GND                                                 |
|           | XOSC1                    | 67         | NC                                                  | NC                                                  |

(1) PA1 (U0Tx) may be enabled as an output by the ROM bootloader if no code is present in the flash and PA0 (U0Rx) receives a valid boot signature. Ensure that this condition will not occur if PA1 is to be connected directly to GND.

(2) PA4 (SSI0XDAT0) may be enabled as an output by the ROM bootloader if no code is present in the flash and the SSI0x (PA2, PA3, PA5) receives a valid boot signature. Ensure that this condition will not occur if PA4 is to be connected directly to GND.

表 4-6. Connections for Unused Pins (continued)

| FUNCTION       | SIGNAL NAME             | PIN NUMBER | ACCEPTABLE PRACTICE | PREFERRED PRACTICE                                               |
|----------------|-------------------------|------------|---------------------|------------------------------------------------------------------|
| System Control | OSC0                    | 88         | NC                  | GND                                                              |
|                | OSC1                    | 89         | NC                  | NC                                                               |
|                | $\overline{\text{RST}}$ | 70         | VDD                 | Pull up to VDD with 0 to 100-k $\Omega$ resistor. <sup>(3)</sup> |
| USB            | USB0DM / PL7            | 93         | NC                  | Pull down to GND with 1-k $\Omega$ resistor. <sup>(4)</sup>      |
|                | USB0DP / PL6            | 94         | NC                  | Pull down to GND with 1-k $\Omega$ resistor. <sup>(4)</sup>      |

(3) For details, see the *System Control* chapter of the [SimpleLink™ MSP432E4 Microcontrollers Technical Reference Manual](#)

(4) The ROM bootloader may configure these pins as USB pins if no code is present in the flash. Therefore, they should not be connected directly to ground.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup> <sup>(2)</sup>

|                      |                                                   | MIN  | MAX | UNIT |
|----------------------|---------------------------------------------------|------|-----|------|
| V <sub>DD</sub>      | V <sub>DD</sub> supply voltage                    | 0    | 4   | V    |
| V <sub>DDA</sub>     | V <sub>DDA</sub> supply voltage                   | 0    | 4   | V    |
| V <sub>BAT</sub>     | V <sub>BAT</sub> battery supply voltage           | 0    | 4   | V    |
| V <sub>BATRMP</sub>  | V <sub>BAT</sub> battery supply voltage ramp time | 0    | 0.7 | V/μs |
| V <sub>IN_GPIO</sub> | Input voltage <sup>(3)</sup>                      | –0.3 | 4   | V    |
| I <sub>GPIOMAX</sub> | Maximum current per output pin                    |      | 64  | mA   |
| T <sub>S</sub>       | Unpowered storage temperature range               | –65  | 150 | °C   |
| T <sub>JMAX</sub>    | Maximum junction temperature                      |      | 125 | °C   |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Voltages are measured with respect to GND.

(3) Applies to static and dynamic signals including overshoot.

### 5.2 ESD Ratings

over operating free-air temperature range (unless otherwise noted)

|                    |                         | VALUE                                                                            | UNIT  |
|--------------------|-------------------------|----------------------------------------------------------------------------------|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup> <sup>(2)</sup> | ±2000 |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(3)</sup>   | ±500  |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.

(2) All pins are HBM compliant to ±2000 V for all combinations as per JESD22-A114F, except for the following stress combinations:

- The Ethernet EN0RXIN, EN0TXON, EN0RXIP, and EN0TXOP pins to each other.
- The GPIO pins PM4, PM5, PM6, and PM7 to other pins.

These exceptions are compliant to 500 V and do not require any special handling beyond typical ESD control procedures during assembly operations per JEDEC publication JEP155. These pins do meet the 500-V CDM specification.

(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                |                                      |                      | MIN | MAX | UNIT |
|----------------|--------------------------------------|----------------------|-----|-----|------|
| T <sub>A</sub> | Ambient operating temperature range  | Extended temperature | −40 | 105 | °C   |
| T <sub>J</sub> | Junction operating temperature range | Extended temperature | −40 | 125 | °C   |

### 5.4 Recommended DC Operating Conditions

over operating free-air temperature (unless otherwise noted)

|                    |                                                  | MIN  | NOM | MAX  | UNIT |
|--------------------|--------------------------------------------------|------|-----|------|------|
| V <sub>DD</sub>    | V <sub>DD</sub> supply voltage                   | 2.97 | 3.3 | 3.63 | V    |
| V <sub>DDA</sub>   | V <sub>DDA</sub> supply voltage <sup>(1)</sup>   | 2.97 | 3.3 | 3.63 | V    |
| V <sub>DDC</sub>   | V <sub>DDC</sub> supply voltage, run mode        | 1.14 | 1.2 | 1.32 | V    |
| V <sub>DDCDS</sub> | V <sub>DDC</sub> supply voltage, deep-sleep mode | 0.85 |     | 0.95 | V    |

(1) To ensure proper operation, power on V<sub>DDA</sub> before V<sub>DD</sub> if sourced from different supplies, or connect V<sub>DDA</sub> to the same supply as V<sub>DD</sub>. No restriction exists for powering off.

### 5.5 Recommended GPIO Operating Characteristics

The following sections describe the recommended GPIO operating characteristics for the device.

Two types of pads are provided on the device:

- Fast GPIO pads: These pads provide variable, programmable drive strength and optimized voltage output levels.
- Slow GPIO pads: These pads provide 2-mA drive strength and are designed to be sensitive to voltage inputs. The PJ1 GPIOs port pins are slow GPIO pads. All other GPIOs have a fast GPIO pad type.

注

Port pins PL6 and PL7 operate as fast GPIO pads, but have 4-mA drive capability only. GPIO register controls for drive strength, slew rate and open drain have no effect on these pins. The registers which have no effect are as follows: GPIODR2R, GPIODR4R, GPIODR8R, GPIODR12R, GPIOSLR, and GPIOODR.

注

Port pins PM[7:4] operate as fast GPIO pads but support only 2-, 4-, 6-, and 8-mA drive capability. 10- and 12-mA drive are not supported. All standard GPIO register controls, except for the GPIODR12R register, apply to these port pins.

## 5.6 Recommended Fast GPIO Pad Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|           |                                                                      | MIN                             | NOM  | MAX                  | UNIT |
|-----------|----------------------------------------------------------------------|---------------------------------|------|----------------------|------|
| $V_{IH}$  | Fast GPIO high-level input voltage                                   | $0.65 \times V_{DD}$            |      | 4                    | V    |
| $I_{IH}$  | Fast GPIO high-level input current                                   |                                 |      | 300                  | nA   |
| $V_{IL}$  | Fast GPIO low-level input voltage                                    | 0                               |      | $0.35 \times V_{DD}$ | V    |
| $I_{IL}$  | Fast GPIO low-level input current <sup>(1)</sup>                     |                                 |      | -200                 | nA   |
| $V_{HYS}$ | Fast GPIO input hysteresis                                           | 0.49                            |      |                      | V    |
| $V_{OH}$  | Fast GPIO high-level output voltage                                  | 2.4                             |      |                      | V    |
| $V_{OL}$  | Fast GPIO low-level output voltage                                   |                                 |      | 0.40                 | V    |
| $I_{OH}$  | Fast GPIO high-level source current, $V_{OH} = 2.4$ V <sup>(2)</sup> | 2-mA drive                      | 2.0  |                      | mA   |
|           |                                                                      | 4-mA drive                      | 4.0  |                      |      |
|           |                                                                      | 8-mA drive                      | 8.0  |                      |      |
|           |                                                                      | 10-mA drive                     | 10.0 |                      |      |
|           |                                                                      | 12-mA drive                     | 12.0 |                      |      |
| $I_{OL}$  | Fast GPIO low-level sink current, $V_{OL} = 0.4$ V <sup>(2)</sup>    | 2-mA drive                      | 2.0  |                      | mA   |
|           |                                                                      | 4-mA drive                      | 4.0  |                      |      |
|           |                                                                      | 8-mA drive                      | 8.0  |                      |      |
|           |                                                                      | 10-mA drive                     | 10.0 |                      |      |
|           |                                                                      | 12-mA drive                     | 12.0 |                      |      |
|           |                                                                      | 12-mA drive overdriven to 18 mA | 18.0 |                      |      |

(1) Output, pullup, and pulldown are disabled; only input is enabled.

(2)  $I_O$  specifications reflect the maximum current where the corresponding output voltage meets the  $V_{OH}$  or  $V_{OL}$  thresholds.  $I_O$  current can exceed these limits (subject to absolute maximum ratings).

## 5.7 Recommended Slow GPIO Pad Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|          |                                    | MIN                  | NOM | MAX | UNIT |
|----------|------------------------------------|----------------------|-----|-----|------|
| $V_{IH}$ | Slow GPIO high-level input voltage | $0.65 \times V_{DD}$ |     | 4   | V    |
| $I_{IH}$ | Slow GPIO high-level input current |                      |     | 4.1 | nA   |

## Recommended Slow GPIO Pad Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

|                  |                                                                                       | MIN  | NOM | MAX                    | UNIT |
|------------------|---------------------------------------------------------------------------------------|------|-----|------------------------|------|
| V <sub>IL</sub>  | Slow GPIO low-level input voltage                                                     | 0    |     | 0.35 × V <sub>DD</sub> | V    |
| I <sub>IL</sub>  | Slow GPIO low-level input current <sup>(1)</sup>                                      |      |     | –1                     | nA   |
| V <sub>HYS</sub> | Slow GPIO input hysteresis                                                            | 0.49 |     |                        | V    |
| V <sub>OH</sub>  | Slow GPIO high-level output voltage                                                   | 2.4  |     |                        | V    |
| V <sub>OL</sub>  | Slow GPIO low-level output voltage                                                    |      |     | 0.4                    | V    |
| I <sub>OH</sub>  | Slow GPIO high-level source current, V <sub>OH</sub> = 2.4 V, 2-mA drive              | 2.0  |     |                        | mA   |
| I <sub>OL</sub>  | Slow GPIO low-level sink current, V <sub>OL</sub> = 0.4 V <sup>(2)</sup> , 2-mA drive | 2.0  |     |                        | mA   |

(1) Output, pullup, and pulldown are disabled; only input is enabled.

(2) I<sub>O</sub> specifications reflect the maximum current where the corresponding output voltage meets the V<sub>OH</sub> or V<sub>OL</sub> thresholds. I<sub>O</sub> current can exceed these limits (subject to absolute maximum ratings).

## 5.8 GPIO Current Restrictions

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|                   |                                                                 | MIN | NOM | MAX  | UNIT |
|-------------------|-----------------------------------------------------------------|-----|-----|------|------|
| I <sub>MAXL</sub> | Cumulative maximum GPIO current per side, left                  |     |     | 112  | mA   |
| I <sub>MAXB</sub> | Cumulative maximum GPIO current per side, bottom <sup>(2)</sup> |     |     | 97.6 | mA   |
| I <sub>MAXR</sub> | Cumulative maximum GPIO current per side, right <sup>(2)</sup>  |     |     | 112  | mA   |
| I <sub>MAXT</sub> | Cumulative maximum GPIO current per side, top <sup>(2)</sup>    |     |     | 80   | mA   |

(1) Based on design simulations, not tested in production.

(2) Sum of sink and source current for GPIOs as listed in 表 5-1.

**表 5-1. Maximum GPIO Package Side Assignments**

| SIDE   | GPIOs                                                                |
|--------|----------------------------------------------------------------------|
| Left   | PC[4-7], PD[0-3], PQ[0-3], PE[0-3], PK[0-3], PN[4-5], PH[0-3]        |
| Bottom | PA[0-7], PF[0-4], PG[0-1], PK[4-7]                                   |
| Right  | PM[0-7], PL[0-7], PB[0-3]                                            |
| Top    | PC[0-3], PQ[4], PP[0-5], PN[0-5], PJ[0-1], PB[4-5], PE[4-5], PD[4-7] |

## 5.9 I/O Reliability

For typical continuous drive applications, I/O pins configured in the range from 2 mA to 12 mA and operating at –40°C to 85°C meet the standard 10-year lifetime reliability. If a continuous current sink of 18 mA is required, then operation is limited to 0 to 75°C to meet the standard 10-year reliability.

At 105°C, I/O pins configured for continuous drive meet the standard 2.5-year lifetime reliability.

In typical switching applications (40% switch rate) operating at –40°C to 85°C, all I/O configurations except 2 mA meet the standard 10-year lifetime reliability with 50-pF loading. By limiting the capacitive loading to 20 pF for an I/O configured to 2 mA, the 10-year lifetime reliability can be met at –40°C to 85°C.

In typical switching applications (40% switch rate) operating at 105°C, all I/O configurations except 2 mA meet the standard 2.5-year lifetime reliability. By reducing the capacitive loading to 20 pF with a typical switching rate at 105°C, a 2-mA I/O configuration meets a 2.5-year lifetime reliability.

## 5.10 Current Consumption

over operating free-air temperature (unless otherwise noted) <sup>(1)</sup>

| PARAMETER           |                          | TEST CONDITIONS                                                                                            | SYSTEM CLOCK |               | TYP   |       |       |       | MAX   |                      | UNIT |
|---------------------|--------------------------|------------------------------------------------------------------------------------------------------------|--------------|---------------|-------|-------|-------|-------|-------|----------------------|------|
|                     |                          |                                                                                                            | FREQ         | CLOCK SOURCE  | −40°C | 25°C  | 85°C  | 105°C | 85°C  | 105°C <sup>(2)</sup> |      |
| I <sub>DD_RUN</sub> | Run mode<br>(flash loop) | V <sub>DD</sub> = 3.3 V,<br>V <sub>DDA</sub> = 3.3 V,<br>Peripherals = All on<br>including MAC and PHY     | 120 MHz      | MOSC with PLL | 96.4  | 105.3 | 107.2 | 108.7 | 129.9 | 140.0                | mA   |
|                     |                          |                                                                                                            | 60 MHz       | MOSC with PLL | 67.4  | 76.6  | 78.6  | 79.9  | 100.3 | 112.5                |      |
|                     |                          |                                                                                                            | 16 MHz       | PIOSC         | 11.9  | 24.4  | 25.5  | 26.7  | 45.0  | 56.4                 |      |
|                     |                          |                                                                                                            | 1 MHz        | PIOSC         | 5.75  | 10.9  | 12.1  | 13.3  | 31.3  | 42.6                 |      |
|                     |                          | V <sub>DD</sub> = 3.3 V,<br>V <sub>DDA</sub> = 3.3 V,<br>Peripherals = All on<br>including MAC but not PHY | 120 MHz      | MOSC with PLL | 69.9  | 77.8  | 79.6  | 80.8  | 98.8  | 108.4                |      |
|                     |                          |                                                                                                            | 60 MHz       | MOSC with PLL | 40.9  | 49.2  | 50.9  | 52.1  | 69.2  | 80.8                 |      |
|                     |                          |                                                                                                            | 16 MHz       | PIOSC         | 11.3  | 23.6  | 25.0  | 26.2  | 43.1  | 54.3                 |      |
|                     |                          |                                                                                                            | 1 MHz        | PIOSC         | 5.10  | 10.1  | 11.5  | 12.7  | 29.3  | 40.5                 |      |
|                     |                          | V <sub>DD</sub> = 3.3 V,<br>V <sub>DDA</sub> = 3.3 V,<br>Peripherals = All on<br>except MAC and PHY        | 120 MHz      | MOSC with PLL | 68.1  | 76.0  | 77.6  | 78.6  | 96.6  | 106.0                |      |
|                     |                          |                                                                                                            | 60 MHz       | MOSC with PLL | 40.0  | 48.2  | 49.8  | 50.8  | 67.9  | 79.2                 |      |
|                     |                          |                                                                                                            | 16 MHz       | PIOSC         | 11.1  | 23.3  | 24.6  | 25.6  | 42.5  | 53.3                 |      |
|                     |                          |                                                                                                            | 1 MHz        | PIOSC         | 5.07  | 10.1  | 11.3  | 12.3  | 29.0  | 39.8                 |      |
|                     |                          | V <sub>DD</sub> = 3.3 V,<br>V <sub>DDA</sub> = 3.3 V,<br>Peripherals = All off                             | 120 MHz      | MOSC with PLL | 35.2  | 39.1  | 40.4  | 41.5  | 55.8  | 65.3                 |      |
|                     |                          |                                                                                                            | 60 MHz       | MOSC with PLL | 23.2  | 29.4  | 30.7  | 31.7  | 45.8  | 55.5                 |      |
|                     |                          |                                                                                                            | 16 MHz       | PIOSC         | 7.38  | 17.9  | 19.0  | 20.0  | 34.5  | 44.1                 |      |
|                     |                          |                                                                                                            | 1 MHz        | PIOSC         | 4.12  | 9.13  | 10.3  | 11.4  | 25.7  | 35.5                 |      |
|                     | Run mode<br>(SRAM loop)  | V <sub>DD</sub> = 3.3 V,<br>V <sub>DDA</sub> = 3.3 V,<br>Peripherals = All on<br>including MAC and PHY     | 120 MHz      | MOSC with PLL | 93.8  | 103.6 | 111.6 | 113.2 | 133.4 | 144.6                |      |
|                     |                          |                                                                                                            | 60 MHz       | MOSC with PLL | 66.9  | 76.7  | 78.7  | 80.0  | 100.0 | 111.9                |      |
|                     |                          |                                                                                                            | 16 MHz       | PIOSC         | 12.6  | 19.0  | 20.1  | 21.3  | 39.1  | 50.3                 |      |
|                     |                          |                                                                                                            | 1 MHz        | PIOSC         | 5.73  | 10.6  | 11.7  | 12.8  | 30.9  | 42.2                 |      |
|                     |                          | V <sub>DD</sub> = 3.3 V,<br>V <sub>DDA</sub> = 3.3 V,<br>Peripherals = All on<br>including MAC but not PHY | 120 MHz      | MOSC with PLL | 67.2  | 76.1  | 84.0  | 85.4  | 102.3 | 113.0                |      |
|                     |                          |                                                                                                            | 60 MHz       | MOSC with PLL | 40.3  | 49.2  | 50.9  | 52.2  | 68.9  | 80.2                 |      |
|                     |                          |                                                                                                            | 16 MHz       | PIOSC         | 11.9  | 18.2  | 19.6  | 20.8  | 37.2  | 48.2                 |      |
|                     |                          |                                                                                                            | 1 MHz        | PIOSC         | 5.08  | 9.79  | 11.2  | 12.3  | 28.9  | 40.1                 |      |
|                     |                          | V <sub>DD</sub> = 3.3 V,<br>V <sub>DDA</sub> = 3.3 V,<br>Peripherals =All on<br>except MAC and PHY         | 120 MHz      | MOSC with PLL | 65.4  | 74.3  | 82.0  | 83.2  | 100.1 | 110.6                |      |
|                     |                          |                                                                                                            | 60 MHz       | MOSC with PLL | 39.4  | 48.2  | 49.8  | 50.9  | 67.6  | 78.6                 |      |
|                     |                          |                                                                                                            | 16 MHz       | PIOSC         | 11.7  | 17.9  | 19.2  | 20.2  | 36.6  | 47.2                 |      |
|                     |                          |                                                                                                            | 1 MHz        | PIOSC         | 5.05  | 9.75  | 11.0  | 11.9  | 28.6  | 39.4                 |      |
|                     |                          | V <sub>DD</sub> = 3.3 V,<br>V <sub>DDA</sub> = 3.3 V,<br>Peripherals = All off                             | 120 MHz      | MOSC with PLL | 35.4  | 43.3  | 44.7  | 45.8  | 59.8  | 69.0                 |      |
|                     |                          |                                                                                                            | 60 MHz       | MOSC with PLL | 23.4  | 29.4  | 30.7  | 31.7  | 45.5  | 54.9                 |      |
|                     |                          |                                                                                                            | 16 MHz       | PIOSC         | 7.08  | 12.4  | 13.6  | 14.6  | 28.7  | 38.0                 |      |
|                     |                          |                                                                                                            | 1 MHz        | PIOSC         | 4.60  | 8.78  | 10.0  | 11.0  | 25.3  | 34.9                 |      |

(1) [Section 5.11](#) lists the current consumption that specific peripherals contribute to the run mode current consumption in [Section 5.10](#). If these peripherals are not powered, then the peripheral current consumption can be subtracted from the run mode consumption in [Section 5.10](#).

(2) Applicable to extended temperature devices only.

## Current Consumption (continued)

over operating free-air temperature (unless otherwise noted) <sup>(1)</sup>

| PARAMETER       | TEST CONDITIONS            | SYSTEM CLOCK |                      | TYP   |      |      |       | MAX   |                      | UNIT |
|-----------------|----------------------------|--------------|----------------------|-------|------|------|-------|-------|----------------------|------|
|                 |                            | FREQ         | CLOCK SOURCE         | –40°C | 25°C | 85°C | 105°C | 85°C  | 105°C <sup>(2)</sup> |      |
| $I_{DD\_SLEEP}$ | Sleep mode (FLASHPM = 0x0) | 120 MHz      | MOSC with PLL        | 82.8  | 94.8 | 96.8 | 98.1  | 117.9 | 129.1                | mA   |
|                 |                            | 60 MHz       | MOSC with PLL        | 60.8  | 69.2 | 71.2 | 72.3  | 91.8  | 102.9                |      |
|                 |                            | 16 MHz       | PIOSC                | 11.2  | 16.8 | 18.1 | 19.1  | 35.4  | 45.9                 |      |
|                 |                            | 1 MHz        | PIOSC <sup>(3)</sup> | 5.10  | 10.3 | 11.5 | 12.6  | 28.9  | 39.6                 |      |
|                 |                            | 120 MHz      | MOSC with PLL        | 56.2  | 67.4 | 69.1 | 70.3  | 87.1  | 97.8                 |      |
|                 |                            | 60 MHz       | MOSC with PLL        | 34.4  | 41.9 | 43.4 | 44.5  | 60.7  | 71.6                 |      |
|                 |                            | 16 MHz       | PIOSC <sup>(3)</sup> | 10.6  | 16.2 | 17.5 | 18.5  | 34.5  | 45.1                 |      |
|                 |                            | 1 MHz        | PIOSC <sup>(3)</sup> | 4.47  | 9.60 | 10.9 | 12.0  | 28.0  | 38.7                 |      |
|                 |                            | 120 MHz      | MOSC with PLL        | 54.4  | 65.6 | 67.1 | 68.1  | 84.9  | 95.4                 |      |
|                 |                            | 60 MHz       | MOSC with PLL        | 33.5  | 40.9 | 42.3 | 43.2  | 59.4  | 70.0                 |      |
|                 |                            | 16 MHz       | PIOSC <sup>(3)</sup> | 10.4  | 15.9 | 17.1 | 17.9  | 33.9  | 44.1                 |      |
|                 |                            | 1 MHz        | PIOSC <sup>(3)</sup> | 4.44  | 9.56 | 10.7 | 11.6  | 27.7  | 38.0                 |      |
|                 |                            | 120 MHz      | MOSC with PLL        | 22.0  | 28.6 | 29.8 | 30.7  | 44.1  | 53.1                 |      |
|                 |                            | 60 MHz       | MOSC with PLL        | 16.3  | 22.0 | 23.2 | 24.1  | 37.5  | 46.6                 |      |
|                 |                            | 16 MHz       | PIOSC <sup>(3)</sup> | 5.37  | 10.4 | 11.5 | 12.4  | 26.1  | 35.1                 |      |
|                 |                            | 1 MHz        | PIOSC <sup>(3)</sup> | 4.37  | 8.60 | 9.71 | 10.6  | 24.6  | 33.9                 |      |
|                 | Sleep mode (FLASHPM = 0x2) | 120 MHz      | MOSC with PLL        | 86.5  | 89.0 | 91.2 | 92.5  | 112.1 | 123.5                |      |
|                 |                            | 60 MHz       | MOSC with PLL        | 61.6  | 63.4 | 65.6 | 66.7  | 86.0  | 97.2                 |      |
|                 |                            | 16 MHz       | PIOSC <sup>(3)</sup> | 10.4  | 11.1 | 12.4 | 13.5  | 29.8  | 40.4                 |      |
|                 |                            | 1 MHz        | PIOSC <sup>(3)</sup> | 4.45  | 4.49 | 5.83 | 6.98  | 23.4  | 34.2                 |      |
|                 |                            | 120 MHz      | MOSC with PLL        | 59.9  | 61.7 | 63.4 | 64.7  | 81.3  | 92.1                 |      |
|                 |                            | 60 MHz       | MOSC with PLL        | 35.1  | 36.1 | 37.8 | 38.9  | 54.9  | 66.0                 |      |
|                 |                            | 16 MHz       | PIOSC <sup>(3)</sup> | 9.75  | 10.4 | 11.8 | 12.9  | 28.9  | 39.6                 |      |
|                 |                            | 1 MHz        | PIOSC <sup>(3)</sup> | 3.82  | 3.82 | 5.25 | 6.38  | 22.5  | 33.4                 |      |
|                 |                            | 120 MHz      | MOSC with PLL        | 58.1  | 59.9 | 61.4 | 62.5  | 79.1  | 89.7                 |      |
|                 |                            | 60 MHz       | MOSC with PLL        | 34.2  | 35.1 | 36.7 | 37.6  | 53.6  | 64.4                 |      |
|                 |                            | 16 MHz       | PIOSC <sup>(3)</sup> | 9.50  | 10.1 | 11.4 | 12.3  | 28.3  | 38.6                 |      |
|                 |                            | 1 MHz        | PIOSC <sup>(3)</sup> | 3.79  | 3.78 | 5.06 | 5.96  | 22.2  | 32.7                 |      |
|                 |                            | 120 MHz      | MOSC with PLL        | 22.0  | 22.8 | 24.1 | 25.1  | 38.2  | 47.4                 |      |
|                 |                            | 60 MHz       | MOSC with PLL        | 15.7  | 16.2 | 17.5 | 18.5  | 31.7  | 40.9                 |      |
|                 |                            | 16 MHz       | PIOSC <sup>(3)</sup> | 4.50  | 4.60 | 5.80 | 6.80  | 20.5  | 29.8                 |      |
|                 |                            | 1 MHz        | PIOSC <sup>(3)</sup> | 3.00  | 2.80 | 4.10 | 5.20  | 19.1  | 28.7                 |      |

(3) If the MOSC is the source of the run-mode system clock and is powered down in sleep mode, wake time is increased by  $t_{MOSC\_SETTLE}$ .

## Current Consumption (continued)

over operating free-air temperature (unless otherwise noted) <sup>(4)</sup>

| PARAMETER                                     |                                              | TEST CONDITIONS                                                                                                            | SYSTEM CLOCK |               | TYP   |       |       |       | MAX   |                      | UNIT |
|-----------------------------------------------|----------------------------------------------|----------------------------------------------------------------------------------------------------------------------------|--------------|---------------|-------|-------|-------|-------|-------|----------------------|------|
|                                               |                                              |                                                                                                                            | FREQ         | CLOCK SOURCE  | −40°C | 25°C  | 85°C  | 105°C | 85°C  | 105°C <sup>(2)</sup> |      |
| I <sub>DD_DEEPSLEEP</sub>                     | Deep-sleep mode (FLASHPM = 0x2)              | V <sub>DD</sub> = 3.3 V, V <sub>DDA</sub> = 3.3 V, Peripherals = All on, LDO = 1.2 V                                       | 16 MHz       | PIOSC         | 9.74  | 9.78  | 10.8  | 11.6  | 24.1  | 32.1                 | mA   |
|                                               |                                              |                                                                                                                            | 30 kHz       | LFIOOSC       | 2.60  | 2.83  | 3.83  | 4.60  | 17.1  | 25.3                 |      |
|                                               |                                              | V <sub>DD</sub> = 3.3 V, V <sub>DDA</sub> = 3.3 V, Peripherals = All off, LDO = 1.2 V                                      | 16 MHz       | PIOSC         | 4.53  | 4.05  | 4.88  | 5.53  | 15.9  | 22.7                 |      |
|                                               |                                              |                                                                                                                            | 30 kHz       | LFIOOSC       | 0.614 | 0.762 | 1.69  | 2.46  | 13.3  | 20.7                 |      |
|                                               |                                              | V <sub>DD</sub> = 3.3 V, V <sub>DDA</sub> = 3.3 V, Peripherals = All on, LDO = 0.9 V                                       | 16 MHz       | PIOSC         | 5.21  | 7.33  | 7.97  | 8.48  | 15.3  | 20.1                 |      |
|                                               |                                              |                                                                                                                            | 30 kHz       | LFIOOSC       | 2.02  | 2.16  | 2.79  | 3.29  | 10.0  | 14.9                 |      |
|                                               |                                              | V <sub>DD</sub> = 3.3 V, V <sub>DDA</sub> = 3.3 V, Peripherals = All off, LDO = 0.9 V <sup>(4)</sup>                       | 16 MHz       | PIOSC         | 1.08  | 3.10  | 3.61  | 4.01  | 9.50  | 13.4                 |      |
|                                               |                                              |                                                                                                                            | 30 kHz       | LFIOOSC       | 0.367 | 0.454 | 0.954 | 1.36  | 6.86  | 10.8                 |      |
| I <sub>DDA_RUN</sub> , I <sub>DDA_SLEEP</sub> | All run modes                                | V <sub>DD</sub> = 3.3 V, V <sub>DDA</sub> = 3.3 V, Peripherals = All on                                                    | 120 MHz      | MOSC with PLL | 2.61  | 2.66  | 2.68  | 2.66  | 3.03  | 3.35                 | mA   |
|                                               |                                              |                                                                                                                            | 60 MHz       | MOSC with PLL | 2.61  | 2.66  | 2.68  | 2.66  | 3.04  | 3.10                 |      |
|                                               |                                              |                                                                                                                            | 16 MHz       | PIOSC         | 2.45  | 2.49  | 2.50  | 2.48  | 2.85  | 2.95                 |      |
|                                               |                                              |                                                                                                                            | 1 MHz        | PIOSC         | 2.45  | 2.48  | 2.50  | 2.48  | 2.84  | 2.90                 |      |
|                                               | All sleep modes                              | V <sub>DD</sub> = 3.3 V, V <sub>DDA</sub> = 3.3 V, Peripherals = All off                                                   | 120 MHz      | MOSC with PLL | 0.227 | 0.229 | 0.270 | 0.250 | 0.559 | 0.650                |      |
|                                               |                                              |                                                                                                                            | 60 MHz       | MOSC with PLL | 0.229 | 0.232 | 0.267 | 0.250 | 0.579 | 0.600                |      |
|                                               |                                              |                                                                                                                            | 16 MHz       | PIOSC         | 0.228 | 0.229 | 0.265 | 0.251 | 0.545 | 0.575                |      |
|                                               |                                              |                                                                                                                            | 1 MHz        | PIOSC         | 0.227 | 0.227 | 0.267 | 0.247 | 0.549 | 0.555                |      |
| I <sub>DDA_DEEPSLEEP</sub>                    | Deep-sleep mode (FLASHPM = 0x2)              | V <sub>DD</sub> = 3.3 V, V <sub>DDA</sub> = 3.3 V, Peripherals = All on, LDO = 1.2 V                                       | 16 MHz       | PIOSC         | 2.45  | 2.48  | 2.50  | 2.48  | 2.84  | 2.90                 | mA   |
|                                               |                                              |                                                                                                                            | 30 kHz       | LFIOOSC       | 2.45  | 2.48  | 2.50  | 2.48  | 2.85  | 2.90                 |      |
|                                               |                                              | V <sub>DD</sub> = 3.3 V, V <sub>DDA</sub> = 3.3 V, Peripherals = All off, LDO = 1.2 V                                      | 16 MHz       | PIOSC         | 0.226 | 0.227 | 0.265 | 0.249 | 0.558 | 0.635                |      |
|                                               |                                              |                                                                                                                            | 30 kHz       | LFIOOSC       | 0.228 | 0.227 | 0.272 | 0.247 | 0.558 | 0.600                |      |
|                                               |                                              | V <sub>DD</sub> = 3.3 V, V <sub>DDA</sub> = 3.3 V, Peripherals = All on, LDO = 0.9 V <sup>(4)</sup>                        | 16 MHz       | PIOSC         | 2.14  | 2.42  | 2.44  | 2.42  | 2.78  | 2.88                 |      |
|                                               |                                              |                                                                                                                            | 30 kHz       | LFIOOSC       | 2.44  | 2.42  | 2.44  | 2.42  | 2.86  | 2.88                 |      |
|                                               |                                              | V <sub>DD</sub> = 3.3 V, V <sub>DDA</sub> = 3.3 V, Peripherals = All off, LDO = 0.9 V <sup>(4)</sup>                       | 16 MHz       | PIOSC         | 0.216 | 0.166 | 0.209 | 0.193 | 0.563 | 0.580                |      |
|                                               |                                              |                                                                                                                            | 30 kHz       | LFIOOSC       | 0.223 | 0.167 | 0.209 | 0.189 | 0.508 | 0.580                |      |
| I <sub>HIB_NORTC</sub>                        | Hibernate mode (external wake, RTC disabled) | V <sub>BAT</sub> = 3.0 V V <sub>DD</sub> = 0 V, V <sub>DDA</sub> = 0 V, System clock = OFF, Hibernate module = 32.768 kHz  |              |               | 1.04  | 1.20  | 1.44  | 1.69  | 1.62  | 2.14                 | μA   |
| I <sub>HIB_RTC</sub>                          | Hibernate mode (RTC enabled)                 | V <sub>BAT</sub> = 3.0 V, V <sub>DD</sub> = 0 V, V <sub>DDA</sub> = 0 V, System clock = OFF, Hibernate module = 32.768 kHz |              |               | 1.12  | 1.29  | 1.54  | 1.82  | 1.75  | 2.33                 | μA   |

(4) See the System Control chapter of the [MSP432E4 SimpleLink™ Microcontrollers Technical Reference Manual](#) for information on lowering the LDO voltage to 0.9 V.

## Current Consumption (*continued*)

over operating free-air temperature (unless otherwise noted) <sup>(1)</sup>

| PARAMETER         |                                               | TEST CONDITIONS                                                                                                                               | SYSTEM CLOCK |              | TYP   |      |      |       | MAX  |                      | UNIT          |
|-------------------|-----------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|--------------|--------------|-------|------|------|-------|------|----------------------|---------------|
|                   |                                               |                                                                                                                                               | FREQ         | CLOCK SOURCE | –40°C | 25°C | 85°C | 105°C | 85°C | 105°C <sup>(2)</sup> |               |
| $I_{HIB\_VDD3ON}$ | Hibernate mode (VDD3ON mode, tamper enabled)  | $V_{BAT} = 3.0\text{ V}$ ,<br>$V_{DD} = 3.3\text{ V}$ ,<br>$V_{DDA} = 3.3\text{ V}$ ,<br>System clock = OFF,<br>Hibernate module = 32.768 kHz |              |              | 6.78  | 7.99 | 17.0 | 22.1  | 31.0 | 46.2                 | $\mu\text{A}$ |
|                   | Hibernate mode (VDD3ON mode, tamper disabled) | $V_{BAT} = 3.0\text{ V}$ ,<br>$V_{DD} = 3.3\text{ V}$ ,<br>$V_{DDA} = 3.3\text{ V}$ ,<br>System clock = OFF,<br>Hibernate module = 32.768 kHz |              |              | 5.42  | 6.39 | 15.4 | 17.8  | 28.9 | 32.0                 |               |

## 5.11 Peripheral Current Consumption

over operating free-air temperature (unless otherwise noted)

| PARAMETER       |                                          | TEST CONDITIONS                                       | SYSTEM CLOCK            | TYP | UNIT |
|-----------------|------------------------------------------|-------------------------------------------------------|-------------------------|-----|------|
| $I_{DDUSB}$     | USB (including USB PHY) run mode current | $V_{DD} = 3.3\text{ V}$ ,<br>$V_{DDA} = 3.3\text{ V}$ | 120 MHz (MOSC with PLL) | 4.0 | mA   |
| $I_{DDEMAC}$    | Ethernet MAC run mode current            | $V_{DD} = 3.3\text{ V}$ ,<br>$V_{DDA} = 3.3\text{ V}$ | 120 MHz (MOSC with PLL) | 1.9 | mA   |
| $I_{DDEMACPHY}$ | Ethernet MAC and PHY run mode current    | $V_{DD} = 3.3\text{ V}$ ,<br>$V_{DDA} = 3.3\text{ V}$ | 120 MHz (MOSC with PLL) | 30  | mA   |

## 5.12 LDO Regulator Characteristics

over operating free-air temperature (unless otherwise noted)

| PARAMETER    |                                                                         | MIN  | TYP | MAX  | UNIT             |
|--------------|-------------------------------------------------------------------------|------|-----|------|------------------|
| $C_{LDO}$    | External filter capacitor size for internal power supply <sup>(1)</sup> | 2.5  |     | 4.0  | $\mu\text{F}$    |
| ESR          | Filter capacitor equivalent series resistance                           | 0    |     | 100  | $\text{m}\Omega$ |
| ESL          | Filter capacitor equivalent series inductance                           |      |     | 0.5  | nH               |
| $V_{LDO}$    | LDO output voltage, run mode                                            | 1.13 | 1.2 | 1.27 | V                |
| $I_{INRUSH}$ | Inrush current                                                          | 50   |     | 250  | mA               |

(1) Connect the capacitor as close as possible to pin 115.

### 5.13 Power Dissipation

over operating free-air temperature (unless otherwise noted) <sup>(1)</sup> <sup>(2)</sup>

| PARAMETER       |                                               | T <sub>A</sub>                    | T <sub>J</sub>                    | MIN | MAX | UNIT |
|-----------------|-----------------------------------------------|-----------------------------------|-----------------------------------|-----|-----|------|
| P <sub>DE</sub> | Extended temperature device power dissipation | 105°C (extended temperature part) | 125°C (extended temperature part) |     | 452 | mW   |

- (1) If the device exceeds the power dissipation value shown, then modifications such as heat sinks or fans must be used to conform to the limits shown.
- (2) A larger power dissipation allowance can be achieved by lowering T<sub>A</sub> as long as T<sub>JMAX</sub> shown in [Section 5.1](#) is not exceeded.

### 5.14 Thermal Resistance Characteristics, 128-Pin PDT (TQFP) Package

over operating free-air temperature range (unless otherwise noted)

| THERMAL METRIC  |                                                         | VALUE                                                                                                                                                            | UNIT |
|-----------------|---------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| θ <sub>JA</sub> | Thermal resistance (junction to ambient) <sup>(1)</sup> | 44.2                                                                                                                                                             | °C/W |
| θ <sub>JB</sub> | Thermal resistance (junction to board) <sup>(1)</sup>   | 22.4                                                                                                                                                             | °C/W |
| θ <sub>JC</sub> | Thermal resistance (junction to case) <sup>(1)</sup>    | 6.8                                                                                                                                                              | °C/W |
| Ψ <sub>JT</sub> | Thermal metric (junction to top of package)             | 0.2                                                                                                                                                              | °C/W |
| Ψ <sub>JB</sub> | Thermal metric (junction to board)                      | 22.1                                                                                                                                                             | °C/W |
| T <sub>J</sub>  | Junction temperature formula                            | $T_C + (P \times \Psi_{JT})^{(2)}$<br>$T_{PCB} + (P \times \Psi_{JB})^{(3)}$<br>$T_A + (P \times \theta_{JA})^{(4)}$<br>$T_B + (P \times \theta_{JB})^{(5) (6)}$ | °C   |

- (1) Junction to ambient thermal resistance (θ<sub>JA</sub>), junction to board thermal resistance (θ<sub>JB</sub>), and junction to case thermal resistance (θ<sub>JC</sub>) numbers are determined by a package simulator.
- (2) T<sub>C</sub> is the case temperature and P is the device power consumption.
- (3) T<sub>PCB</sub> is the temperature of the board acquired by following the steps listed in the EAI/JESD 51-8 standard summarized in [Semiconductor and IC Package Thermal Metrics](#). P is the device power consumption.
- (4) Because θ<sub>JA</sub> is highly variable and based on factors such as board design, chip size, pad size, altitude, and external ambient temperature, TI recommends using the equations that contain Ψ<sub>JT</sub> and Ψ<sub>JB</sub> for best results.
- (5) T<sub>B</sub> is temperature of the board.
- (6) θ<sub>JB</sub> is not a pure reflection of the internal resistance of the package because it includes the resistance of the testing board and environment. TI recommends using equations that contain Ψ<sub>JT</sub> and Ψ<sub>JB</sub> for best results.

## 5.15 Timing and Switching Characteristics

### 5.15.1 Load Conditions

表 5-2 shows the load conditions used for timing measurements, and 表 5-2 lists the load values for the specified signals.

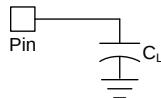


图 5-1. Load Conditions

表 5-2. Load Conditions

| SIGNALS                               | LOAD VALUE (C <sub>L</sub> ) |
|---------------------------------------|------------------------------|
| EPIOS[35:0] SDRAM interface           | 30 pF                        |
| EPIOS[35:0] general-purpose interface |                              |
| EPIOS[35:0] host-bus interface        |                              |
| EPIOS[35:0] PSRAM interface           | 40 pF                        |
| All other digital I/O signals         | 50 pF                        |

### 5.15.2 Power Supply Sequencing

To ensure proper operation, power on  $V_{DDA}$  before  $V_{DD}$  if sourced from different supplies, or connect  $V_{DDA}$  to the same supply as  $V_{DD}$ . No restriction exists for powering off.

#### 5.15.2.1 Power and Brownout

表 5-3. Power and Brownout Levels

over operating free-air temperature (unless otherwise noted)

| NO. | PARAMETER        |                                               | MIN  | TYP  | MAX      | UNIT    |
|-----|------------------|-----------------------------------------------|------|------|----------|---------|
| P1  | $t_{VDDA\_RISE}$ | Analog supply voltage ( $V_{DDA}$ ) rise time |      |      | $\infty$ | $\mu s$ |
| P2  | $t_{VDD\_RISE}$  | I/O supply voltage ( $V_{DD}$ ) rise time     |      |      | $\infty$ | $\mu s$ |
| P3  | $t_{VDDC\_RISE}$ | Core supply voltage ( $V_{DDC}$ ) rise time   | 10   |      | 150      | $\mu s$ |
| P4  | $V_{POR}$        | Power-on reset threshold (rising edge)        | 1.98 | 2.35 | 2.72     | V       |
|     |                  | Power-on reset threshold (falling edge)       | 1.84 | 2.20 | 2.56     |         |
|     |                  | Power-on reset hysteresis                     | 0.06 | 0.15 | 0.24     |         |
| P5  | $V_{DDA\_POK}$   | $V_{DDA}$ power-OK threshold (rising edge)    | 2.67 | 2.82 | 2.97     | V       |
| P6  | $V_{DDA\_BOR0}$  | $V_{DDA}$ brownout reset threshold            | 2.71 | 2.80 | 2.89     | V       |
| P7  | $V_{DD\_POK}$    | $V_{DD}$ power-OK threshold (rising edge)     | 2.65 | 2.80 | 2.90     | V       |
|     |                  | $V_{DD}$ power-OK threshold (falling edge)    | 2.67 | 2.76 | 2.85     |         |
| P8  | $V_{DD\_BOR0}$   | $V_{DD}$ brownout reset threshold             | 2.77 | 2.86 | 2.95     | V       |
| P9  | $V_{DDC\_POK}$   | $V_{DDC}$ power-OK threshold (rising edge)    | 0.85 | 0.95 | 1.10     | V       |
|     |                  | $V_{DDC}$ power-OK threshold (falling edge)   | 0.71 | 0.80 | 0.85     |         |

### 5.15.2.1.1 $V_{DDA}$ Levels

The  $V_{DDA}$  supply has three monitors:

- Power-on reset (POR)
- Power-OK (POK)
- Brownout reset (BOR)

The POR monitor is used to keep the analog circuitry in reset until the  $V_{DDA}$  supply reaches the correct range for the analog circuitry to begin operating. The POK monitor is used to keep the digital circuitry in reset until the  $V_{DDA}$  power supply is at an acceptable operational level. The digital reset is only released when the Power-On Reset has deasserted and the Power-OK monitor for each supply indicates that power levels are in operational ranges. The BOR monitor is used to generate a reset to the device or assert an interrupt if the  $V_{DDA}$  supply drops below its operational range.

注

$V_{DDA}$  BOR and  $V_{DD}$  BOR events are a combined BOR to the system logic, such that if either BOR event occurs, the following bits are affected:

- The BORRIS bit in the Raw Interrupt Status (RIS) register, System Control offset 0x050
- The BORMIS bit in the Masked Interrupt Status and Clear (MISC) register, System Control offset 0x058. This bit is set only if the BORIM bit in the Interrupt Mask Control (IMC) register has been set.
- The BOR bit in the Reset Cause (RESC) register, System Control offset 0x05C. This bit is set only if either of the BOR events have been configured to initiate a reset.

In addition, the following bits control both BOR events:

- The BORIM bit in the Interrupt Mask Control (IMC) register, System Control offset 0x054
- The VDDA\_UBOR0 and VDD\_UBOR0 bits in the Power-Temperature Cause (PWRTC) register

See the *System Control* chapter of the [MSP432E4 SimpleLink™ Microcontrollers Technical Reference Manual](#) for more information on how to configure these registers.

图 5-2 shows the relationship between  $V_{DDA}$ , POK, POR, and a BOR event.

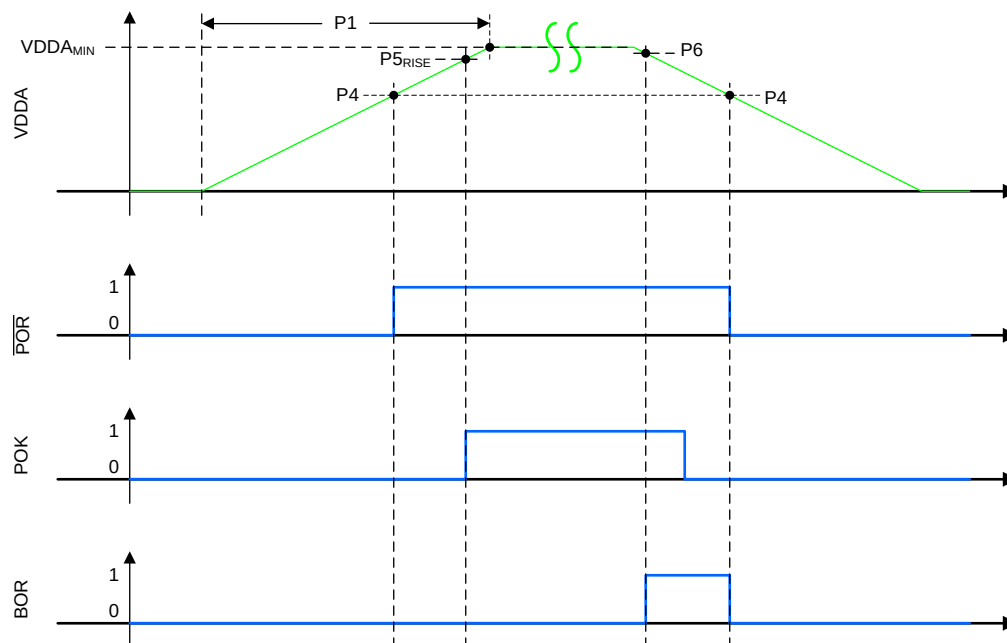


图 5-2. Power and Brownout Assertions vs  $V_{DDA}$  Levels

### 5.15.2.1.2 $V_{DD}$ Levels

The  $V_{DD}$  supply has two monitors:

- Power-OK (POK)
- Brownout reset (BOR)

The POK monitor is used to keep the digital circuitry in reset until the  $V_{DD}$  power supply reaches an acceptable operational level. The digital reset is only released when the POR has deasserted and the POK monitor for each supply indicates that power levels are in operational ranges. The BOR monitor is used to generate a reset to the device or assert an interrupt if the  $V_{DD}$  supply drops below its operational range.

注

$V_{DDA}$  BOR and  $V_{DD}$  BOR events are a combined BOR to the system logic, such that if either BOR event occurs, the following bits are affected:

- The BORRIS bit in the Raw Interrupt Status (RIS) register, System Control offset 0x050
- The BORMIS bit in the Masked Interrupt Status and Clear (MISC) register, System Control offset 0x058. This bit is set only if the BORIM bit in the Interrupt Mask Control (IMC) register has been set.
- The BOR bit in the Reset Cause (RESC) register, System Control offset 0x05C. This bit is set only if either of the BOR events have been configured to initiate a reset.

In addition, the following bits control both BOR events:

- The BORIM bit in the Interrupt Mask Control (IMC) register, System Control offset 0x054
- The VDDA\_UBOR0 and VDD\_UBOR0 bits in the Power-Temperature Cause (PWRTC) register

See the *System Control* chapter of the [MSP432E4 SimpleLink™ Microcontrollers Technical Reference Manual](#) for more information on how to configure these registers.

图 5-3 shows the relationship between  $V_{DD}$ , POK, POR, and a BOR event.

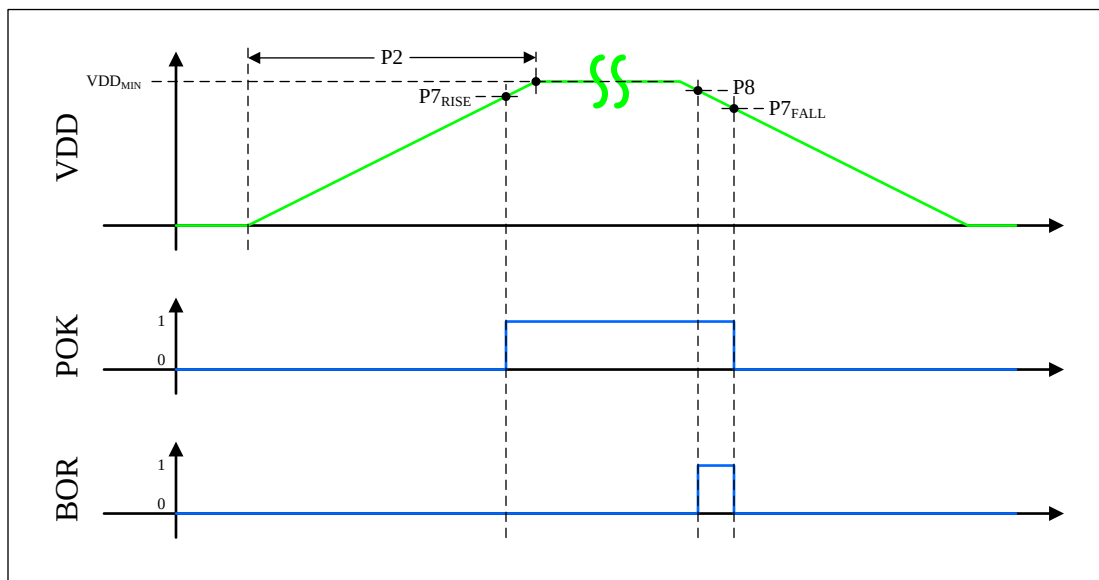


图 5-3. Power and Brownout Assertions vs  $V_{DD}$  Levels

### 5.15.2.1.3 $V_{DDC}$ Levels

The  $V_{DDC}$  supply has one monitor, the Power-OK (POK). The POK monitor is used to keep the digital circuitry in reset until the  $V_{DDC}$  power supply reaches an acceptable operational level. The digital reset is only released when the power-on reset has deasserted and the POK monitor for each supply indicates that power levels are in operational ranges. 图 5-4 shows the relationship between POK and  $V_{DDC}$ .

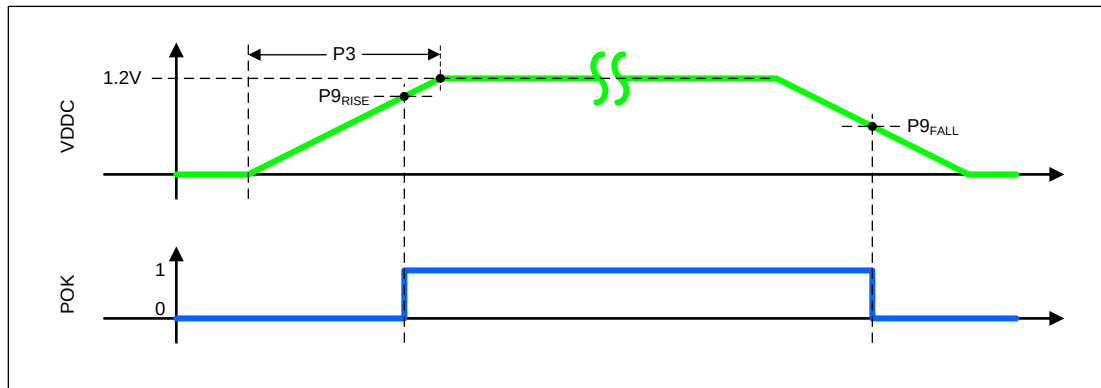


图 5-4. POK Assertion vs  $V_{DDC}$

### 5.15.2.1.4 $V_{DD}$ Glitch Response

图 5-5 shows the response of the BOR and the POR circuit to glitches on the  $V_{DD}$  supply.

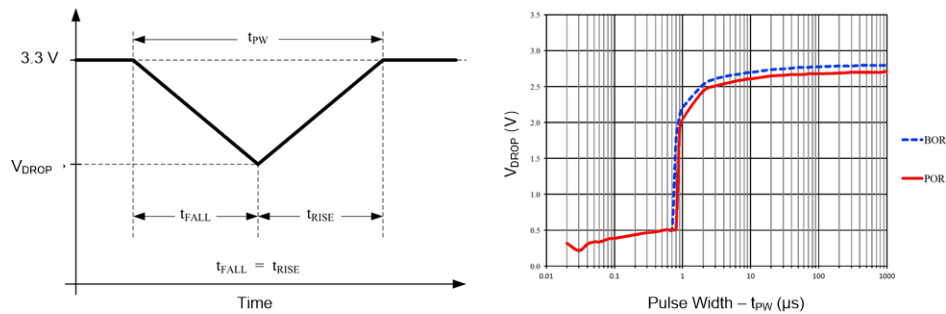


图 5-5. POR-BOR  $V_{DD}$  Glitch Response

### 5.15.2.1.5 $V_{DD}$ Droop Response

图 5-6 shows the response of the BOR and the POR monitors to a drop on the  $V_{DD}$  supply.

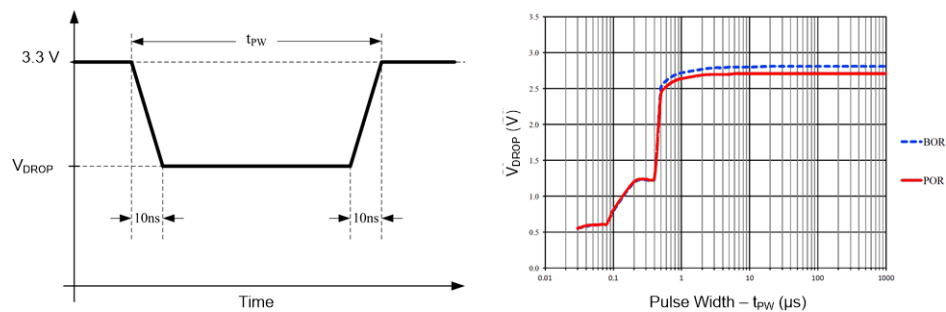


图 5-6. POR-BOR  $V_{DD}$  Droop Response

## 5.15.3 Reset Timing

表 5-4 lists the reset characteristics.

**表 5-4. Reset Characteristics**

over operating free-air temperature (unless otherwise noted)

| NO. | PARAMETER            |                                                                                 | MIN  | TYP                                          | MAX                 | UNIT    |
|-----|----------------------|---------------------------------------------------------------------------------|------|----------------------------------------------|---------------------|---------|
| R1  | $t_{DPORDLY}$        | Digital POR to internal reset assertion delay (see 图 5-7)                       | 0.44 |                                              | 126                 | $\mu s$ |
| R2  | $t_{IRTOU}^{(1)(2)}$ | Standard internal reset time                                                    |      | 14                                           | 16                  | ms      |
|     |                      | Internal reset time with recovery code repair (program or erase) <sup>(3)</sup> | 24.4 |                                              | 6400 <sup>(4)</sup> |         |
| R3  | $t_{BOR0DLY}^{(1)}$  | BOR0 to internal reset assertion delay <sup>(5)</sup> (see 图 5-8)               | 0.44 |                                              | 125                 | $\mu s$ |
| R4  | $t_{RSTMIN}$         | Minimum $\overline{RST}$ pulse duration                                         |      | 0.25 <sup>(6)</sup> or<br>100 <sup>(7)</sup> |                     | $\mu s$ |
| R5  | $t_{IRHWDLY}$        | $\overline{RST}$ to internal reset assertion delay (see 图 5-9)                  |      | 0.85                                         |                     | $\mu s$ |
| R6  | $t_{IRSWR}^{(1)}$    | Internal reset time-out after software-initiated system reset (see 图 5-10)      |      | 2.44                                         |                     | $\mu s$ |
| R7  | $t_{IRWDR}^{(1)}$    | Internal reset time-out after watchdog reset (see 图 5-11)                       |      | 2.44                                         |                     | $\mu s$ |
| R8  | $t_{IRMFR}^{(1)}$    | Internal reset time-out after MOSC failure reset (see 图 5-12)                   |      | 2.44                                         |                     | $\mu s$ |

(1) These values are based on simulation.

(2) This is the delay from the time POR is released until the reset vector is fetched.

(3) This parameter applies only in situations where a power-loss or brownout event occurs during an EEPROM program or erase operation, and EEPROM must be repaired (which is a rare case). For all other sequences, there is no change to normal POR timing. This delay is in addition to other POR delays.

(4) This value represents the maximum internal reset time when the EEPROM reaches its endurance limit.

(5) Timing values depend on the  $V_{DD}$  power-down ramp rate.

(6) Standard operation

(7) Deep-sleep operation with PLOSC powered down

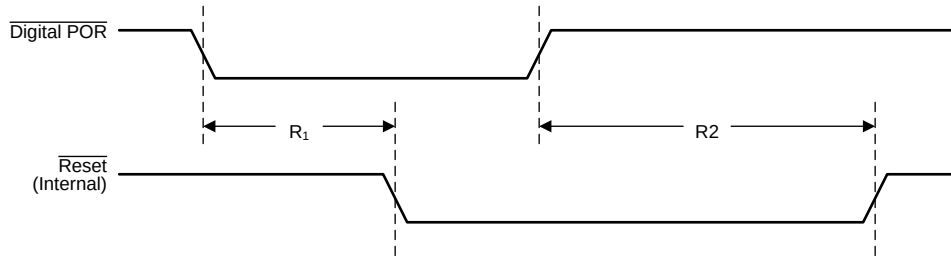


**图 5-7. Digital Power-On Reset Timing**

The digital power-on reset is released only when the analog power-on reset has deasserted and the Power-OK monitor for each supply indicates that power levels are in operational ranges.

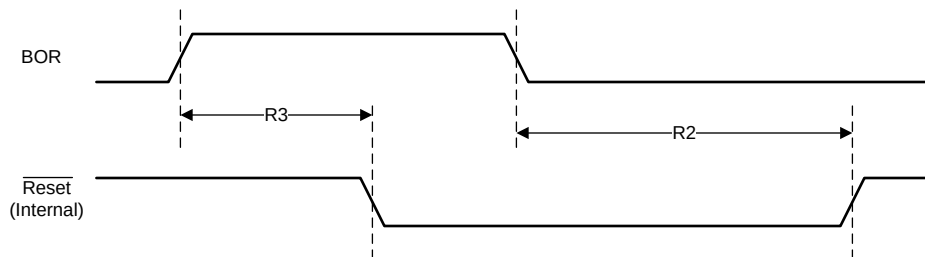


**图 5-8. Brownout Reset Timing**

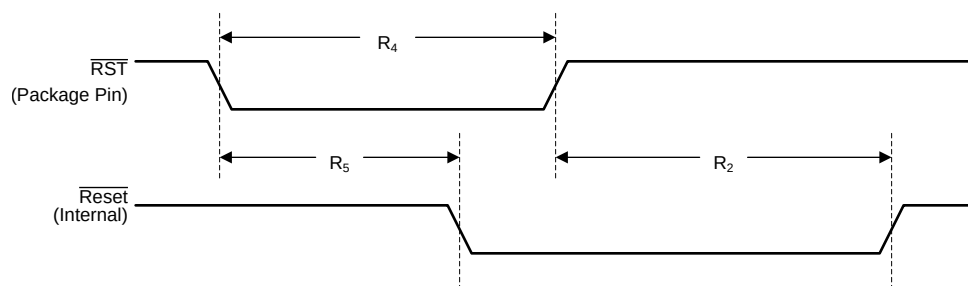
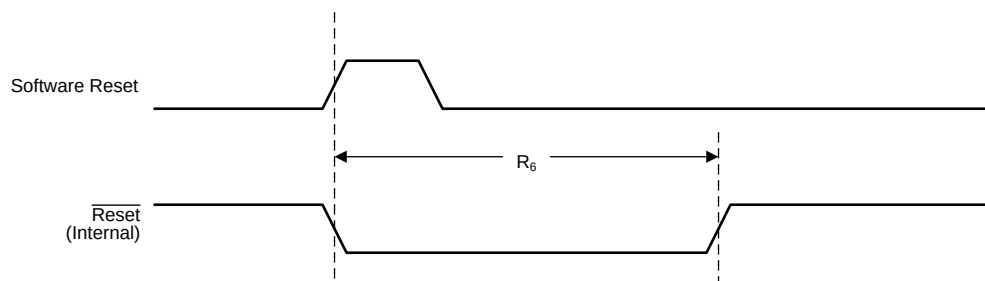
图 5-9. External Reset Timing ( $\overline{\text{RST}}$ )

图 5-10. Software Reset Timing

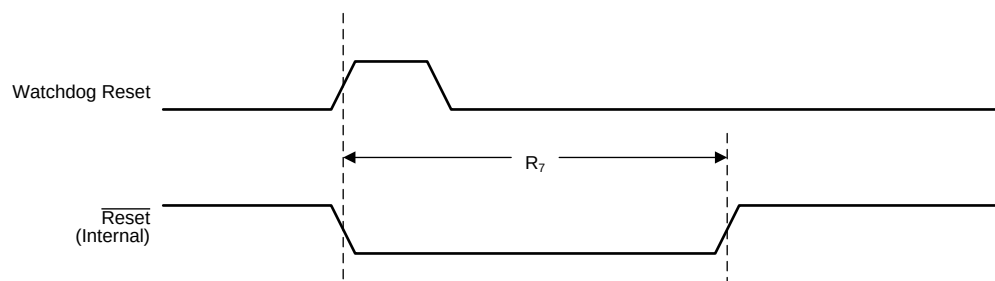


图 5-11. Watchdog Reset Timing

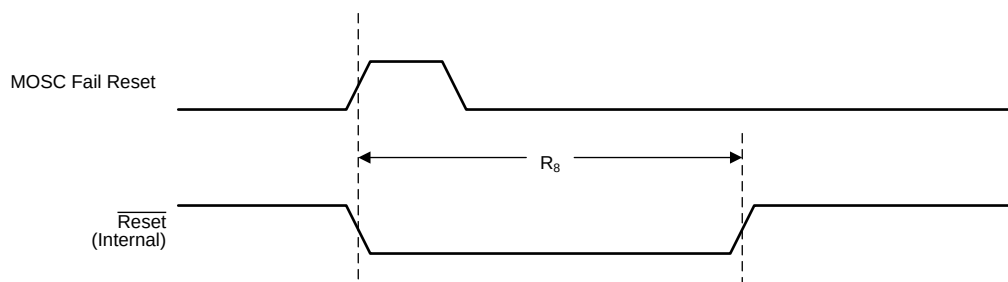


图 5-12. MOSC Failure Reset Timing

### 5.15.4 Clock Specifications

The following sections provide specifications on the various clock sources and mode.

#### 5.15.4.1 PLL Specifications

表 5-5 lists the PLL characteristics.

注

If the integrated Ethernet PHY is used,  $f_{\text{REF\_XTAL}}$  and  $f_{\text{REF\_EXT}}$  must be 25 MHz.

**表 5-5. Phase Locked Loop (PLL) Characteristics**

over operating free-air temperature (unless otherwise noted)

| PARAMETER              |                                                                         | MIN | MAX                               | UNIT |
|------------------------|-------------------------------------------------------------------------|-----|-----------------------------------|------|
| $f_{\text{REF\_XTAL}}$ | Crystal reference                                                       | 5   | 25                                | MHz  |
| $f_{\text{REF\_EXT}}$  | External clock reference                                                | 5   | 25                                | MHz  |
| $f_{\text{PLL}}$       | PLL VCO frequency at 1.2 V <sup>(1)</sup>                               | 100 | 480                               | MHz  |
| $f_{\text{PLLS}}$      | PLL VCO frequency at 0.9 V <sup>(2)</sup>                               | 100 | 480                               | MHz  |
| $t_{\text{READY}}$     | Enabling the PLL, when PLL is transitioning from power down to power up |     | 512 ×<br>(reference clock period) | μs   |
|                        | When the PLL VCO frequency is changed (PLL is already enabled)          |     | 128 ×<br>(reference clock period) |      |
|                        | Changing the OSCSRC between MOSC and PIOSC                              |     | 128 ×<br>(reference clock period) |      |

(1) PLL frequency is manually calculated using the values in the PLLFREQ0 and PLLFREQ1 registers.

(2) If the LDO is dropped to 0.9 V, the system must be run 1/4 of the maximum frequency at most. The Q value in the PLLFREQ1 register must be set to 0x3 rather than using the PSYSDIV field in the RSCLKCFG register for the divisor.

##### 5.15.4.1.1 PLL Configuration

The PLL is disabled by default during power-on reset and is enabled later by software if required. Software specifies the output divisor to set the system clock frequency and enables the PLL to drive the output. The PLL is controlled using the PLLFREQ0, PLLFREQ1, and PLLSTAT registers. Changes made to these registers do not become active until after the NEWFREQ bit in the RSCLKCFG register is enabled. The clock source for the main PLL is selected by configuring the PLLSRC field in the Run and Sleep Clock Configuration (RSCLKCFG) register. The PLL allows for the generation of system clock frequencies in excess of the reference clock provided. The reference clocks for the PLL are the PIOSC and the MOSC.

The PLL is controlled by two registers, PLLFREQ0 and PLLFREQ1. The PLL VCO frequency ( $f_{\text{VCO}}$ ) is determined through 公式 1.

$$f_{\text{VCO}} = f_{\text{IN}} \times \text{MDIV}$$

where

- $f_{\text{IN}} = f_{\text{XTAL}} / (Q+1)(N+1)$  or  $f_{\text{PIOSC}} / (Q+1)(N+1)$
- $\text{MDIV} = \text{MINT} + (\text{MFRAC} / 1024)$

(1)

The Q and N values are programmed in the PLLFREQ1 register. To reduce jitter, program MFRAC to 0x0.

When the PLL is active, the system clock frequency (SysClk) is calculated using 公式 2.

$$\text{SysClk} = f_{\text{VCO}} / (1 + 1)$$

(2)

The PLL system divisor factor (PSYSDIV) must be set as 1. 表 5-6 lists examples of the system clock frequency.

表 5-6. Examples of System Clock Frequencies

| $f_{VCO}$ (MHz) | Q | PSYSDIV + 1 | System Clock (SYSCLK) Frequency (MHz) |
|-----------------|---|-------------|---------------------------------------|
| 480             | 2 | 2           | 120                                   |
| 480             | 3 | 2           | 80                                    |
| 480             | 4 | 2           | 60                                    |
| 480             | 5 | 2           | 48                                    |
| 320             | 2 | 2           | 80                                    |
| 320             | 3 | 2           | 53                                    |
| 320             | 4 | 2           | 40                                    |

If the main oscillator provides the clock reference to the PLL, the translation provided by hardware and used to program the PLL is available for software in the PLL Frequency n (PLLREQn) registers. The internal translation provides a translation within  $\pm 1\%$  of the targeted PLL VCO frequency. 表 5-7 shows the actual PLL frequency and error for a given crystal choice.

表 5-7 provides examples of the programming expected for the PLLREQ0 and PLLREQ1 registers. The CRYSTAL FREQUENCY column specifies the input crystal frequency and the PLL FREQUENCY column displays the PLL frequency given the values of MINT and N, when Q = 0.

表 5-7. Actual PLL Frequency<sup>(1)</sup>

| CRYSTAL FREQUENCY (MHz) | MINT          |                   | N   | REFERENCE FREQUENCY (MHz) <sup>(2)</sup> | PLL FREQUENCY (MHz) |
|-------------------------|---------------|-------------------|-----|------------------------------------------|---------------------|
|                         | DECIMAL VALUE | HEXADECIMAL VALUE |     |                                          |                     |
| 5                       | 64            | 0x40              | 0x0 | 5                                        | 320                 |
| 6                       | 160           | 0x35              | 0x2 | 2                                        | 320                 |
| 8                       | 40            | 0x28              | 0x0 | 8                                        | 320                 |
| 10                      | 32            | 0x20              | 0x0 | 10                                       | 320                 |
| 12                      | 80            | 0x50              | 0x2 | 4                                        | 320                 |
| 16                      | 20            | 0x14              | 0x0 | 16                                       | 320                 |
| 18                      | 160           | 0xA0              | 0x8 | 2                                        | 320                 |
| 20                      | 16            | 0x10              | 0x0 | 20                                       | 320                 |
| 24                      | 40            | 0x28              | 0x2 | 8                                        | 320                 |
| 25                      | 64            | 0x40              | 0x4 | 5                                        | 320                 |
| 5                       | 96            | 0x60              | 0x0 | 5                                        | 480                 |
| 6                       | 80            | 0x50              | 0x0 | 6                                        | 480                 |
| 8                       | 60            | 0x3C              | 0x0 | 8                                        | 480                 |
| 10                      | 48            | 0x30              | 0x0 | 10                                       | 480                 |
| 12                      | 40            | 0x28              | 0x0 | 12                                       | 480                 |
| 16                      | 30            | 0x1E              | 0x0 | 16                                       | 480                 |
| 18                      | 80            | 0x50              | 0x2 | 6                                        | 480                 |
| 20                      | 24            | 0x18              | 0x0 | 20                                       | 480                 |
| 24                      | 20            | 0x14              | 0x0 | 24                                       | 480                 |
| 25                      | 96            | 0x60              | 0x4 | 5                                        | 480                 |

(1) For all examples listed, Q = 0.

(2) For a given crystal frequency, N should be chosen such that the reference frequency is 4 to 30 MHz.

#### 5.15.4.2 PIOSC Specifications

表 5-8 lists the PIOSC characteristics.

**表 5-8. PIOSC Clock Characteristics**

| PARAMETER   |                                                                                                                                                                     | MIN | NOM | MAX  | UNIT |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|------|------|
| $f_{PIOSC}$ | Factory calibration, 0°C to 105°C:<br>Internal 16-MHz precision oscillator frequency variance across voltage and temperature range when factory calibration is used |     |     | ±6%  |      |
|             | Factory calibration, –40°C to <0°C                                                                                                                                  |     |     | ±10% |      |
|             | Recalibration:<br>Internal 16-MHz precision oscillator frequency variance when recalibration is used at a specific temperature                                      |     |     | ±1%  |      |
| $t_{START}$ | PIOSC start-up time <sup>(1)</sup>                                                                                                                                  |     |     | 1    | μs   |

(1) PIOSC start-up time is part of reset and is included in the internal reset time-out value ( $T_{IRTOUT}$ ) in 表 5-4. The  $T_{START}$  value is based on simulation.

#### 5.15.4.3 Low-Frequency Oscillator Specifications

表 5-9 lists the characteristics of the low-frequency oscillator.

**表 5-9. Low-Frequency Oscillator Characteristics**

| PARAMETER   |                                             | MIN | NOM | MAX | UNIT |
|-------------|---------------------------------------------|-----|-----|-----|------|
| $f_{LFOSC}$ | Internal low-frequency oscillator frequency | 10  | 33  | 75  | kHz  |

#### 5.15.4.4 Hibernation Low-Frequency Oscillator Specifications

**表 5-10. Hibernation External Oscillator (XOSC) Input Characteristics**

| PARAMETER                    |                                                                                                                        | MIN                     | NOM    | MAX                     | UNIT |
|------------------------------|------------------------------------------------------------------------------------------------------------------------|-------------------------|--------|-------------------------|------|
| $f_{HIBXOSC}$ <sup>(1)</sup> | Parallel resonance frequency                                                                                           |                         | 32.768 |                         | kHz  |
| $C_1, C_2$                   | External load capacitance on XOSC0, XOSC1 pins <sup>(2)</sup>                                                          | 12                      |        | 24                      | pF   |
| $C_{PKG}$                    | Device package stray shunt capacitance <sup>(2)</sup>                                                                  |                         | 0.5    |                         | pF   |
| $C_{PCB}$                    | PCB stray shunt capacitance <sup>(2)</sup>                                                                             |                         | 0.5    |                         | pF   |
| $C_{SHUNT}$                  | Total shunt capacitance <sup>(2)</sup>                                                                                 |                         |        | 4                       | pF   |
| ESR                          | Crystal effective series resistance, OSCDRV = 0 <sup>(3)</sup>                                                         |                         |        | 50                      | kΩ   |
|                              | Crystal effective series resistance, OSCDRV = 1 <sup>(3)</sup>                                                         |                         |        | 75                      |      |
| DL                           | Oscillator output drive level                                                                                          |                         |        | 0.25                    | μW   |
| $t_{START}$                  | Oscillator start-up time, when using a crystal <sup>(4)</sup>                                                          |                         | 600    | 1500 <sup>(5)</sup>     | ms   |
| $V_{IH}$                     | CMOS input high level, when using an external oscillator with $V_{Supply} > 3.3\text{ V}$                              | 2.64                    |        |                         | V    |
|                              | CMOS input high level, when using an external oscillator with $1.8\text{ V} \leq V_{Supply} \leq 3.3\text{ V}$         | $0.8 \times V_{Supply}$ |        |                         |      |
| $V_{IL}$ <sup>(6)</sup>      | CMOS input low level, when using an external oscillator with $1.8\text{ V} \leq V_{Supply} \leq 3.63\text{ V}$         |                         |        | $0.2 \times V_{Supply}$ | V    |
| $V_{HYS}$ <sup>(6)</sup>     | CMOS input buffer hysteresis, when using an external oscillator with $1.8\text{ V} \leq V_{Supply} \leq 3.63\text{ V}$ | 360                     | 960    | 1390                    | mV   |
| $DC_{HIBOSC\_EXT}$           | External single-ended (bypass) reference duty cycle                                                                    | 30%                     |        | 70%                     |      |

(1) The Hibernation XOSC pins are not fail-safe and must follow the limits in 节 5.15.9.1.2.

(2) See the additional information about the load capacitors following this table.

(3) Crystal ESR specified by crystal manufacturer.

(4) Oscillator start-up time is specified from the time the oscillator is enabled to when it reaches a stable point of oscillation such that the internal clock is valid.

(5) Only valid for recommended supply conditions. Measured with OSCDRV bit set (high drive strength enabled, 24 pF).

(6) Specification is relative to the larger of  $V_{DD}$  or  $V_{BAT}$ .

Choose the load capacitors added on the board,  $C_1$  and  $C_2$ , such that 公式 3 is satisfied (see 表 5-10 for typical values).

$$C_L = (C_1 \times C_2) / (C_1 + C_2) + C_{SHUNT}$$

where

- $C_L$  = load capacitance specified by crystal manufacturer
- $C_{SHUNT} = C_{PKG} + C_{PCB} + C_0$  (total shunt capacitance seen across XOSC0 and XOSC1)
- $C_{PKG}$ ,  $C_{PCB}$  as measured across the XOSC0 and XOSC1 pins excluding the crystal
- Clear the OSCDRV bit in the Hibernation Control (HIBCTL) register for  $C_{1,2} \leq 18$  pF
- Set the OSCDRV bit for  $C_{1,2} > 18$  pF
- $C_0$  = Shunt capacitance of crystal specified by the crystal manufacturer

(3)

表 5-11 lists the characteristics of the Hibernation module low-frequency oscillator.

**表 5-11. Hibernation Internal Low-Frequency Oscillator Clock Characteristics**

| PARAMETER                                                              | MIN | NOM | MAX | UNIT |
|------------------------------------------------------------------------|-----|-----|-----|------|
| $f_{HIBLFOSC}$ Internal low-frequency hibernation oscillator frequency | 10  | 33  | 90  | kHz  |

#### 5.15.4.5 Main Oscillator Specifications

表 5-12 lists the required characteristics of the main oscillator input.

**表 5-12. Main Oscillator Input Characteristics**

over operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

| PARAMETER                                                                 | MIN                       | NOM         | MAX                  | UNIT     |
|---------------------------------------------------------------------------|---------------------------|-------------|----------------------|----------|
| $f_{MOSC}$ Parallel resonance frequency                                   | 4 <sup>(2)</sup>          |             | 25                   | MHz      |
| $f_{REF\_XTAL\_BYPASS}$ External clock reference (PLL in BYPASS mode)     | 0                         |             | 120                  | MHz      |
| $C_1, C_2$ External load capacitance on OSC0, OSC1 pins <sup>(3)</sup>    | 12                        |             | 24                   | pF       |
| $C_{PKG}$ Device package stray shunt capacitance <sup>(3)</sup>           |                           | 0.5         |                      | pF       |
| $C_{PCB}$ PCB stray shunt capacitance <sup>(3)</sup>                      |                           | 0.5         |                      | pF       |
| $C_{SHUNT}$ Total shunt capacitance <sup>(3)</sup>                        |                           |             | 4                    | pF       |
| ESR Crystal effective series resistance                                   | 4 MHz <sup>(4) (5)</sup>  |             | 300                  | $\Omega$ |
|                                                                           | 6 MHz <sup>(4) (5)</sup>  |             | 200                  |          |
|                                                                           | 8 MHz <sup>(4) (5)</sup>  |             | 130                  |          |
|                                                                           | 12 MHz <sup>(4) (5)</sup> |             | 120                  |          |
|                                                                           | 16 MHz <sup>(4) (5)</sup> |             | 100                  |          |
|                                                                           | 25 MHz <sup>(4) (5)</sup> |             | 50                   |          |
| DL Oscillator output drive level <sup>(6)</sup>                           |                           | $OSC_{PWR}$ |                      | mW       |
| $T_{START}$ Oscillator start-up time, when using a crystal <sup>(7)</sup> |                           |             | 18                   | ms       |
| $V_{IH}$ CMOS input high level, when using an external oscillator         | $0.65 \times V_{DD}$      |             | $V_{DD}$             | V        |
| $V_{IL}$ CMOS input low level, when using an external oscillator          | GND                       |             | $0.35 \times V_{DD}$ | V        |
| $V_{HYS}$ CMOS input buffer hysteresis, when using an external oscillator | 150                       |             |                      | mV       |
| $DC_{OSC\_EXT}$ External clock reference duty cycle                       | 45%                       |             | 55%                  |          |

(1) See 表 5-39 and 表 5-40 for additional Ethernet crystal requirements.

(2) 5 MHz is the minimum when using the PLL.

(3) See the additional information about the load capacitors following this table.

(4) Crystal ESR specified by crystal manufacturer.

(5) Crystal vendors can be contacted to confirm these specifications are met for a specific crystal part number if the vendors generic crystal datasheet show limits outside of these specifications.

(6)  $OSC_{PWR} = (2 \times \pi \times F_P \times C_L \times 2.5)^2 \times ESR / 2$ . An estimation of the typical power delivered to the crystal is based on the  $C_L$ ,  $F_P$  and ESR parameters of the crystal in the circuit as calculated by the  $OSC_{PWR}$  equation. Ensure that the value calculated for  $OSC_{PWR}$  does not exceed the crystal's drive-level maximum.

(7) Oscillator start-up time is specified from the time the oscillator is enabled to when it reaches a stable point of oscillation such that the internal clock is valid.

The load capacitors added on the board,  $C_1$  and  $C_2$ , should be chosen such that 公式 4 is satisfied (see 表 5-12 for typical values and 表 5-13 for detailed crystal parameter information).

$$C_L = (C_1 \times C_2) / (C_1 + C_2) + C_{SHUNT}$$

where

- $C_L$  = load capacitance specified by crystal manufacturer
- $C_{SHUNT} = C_0 + C_{PKG} + C_{PCB}$  (total shunt capacitance seen across OSC0 and OSC1 crystal inputs)
- $C_{PKG}, C_{PCB}$  = Mutual capacitance as measured across the OSC0 and OSC1 pins excluding the crystal
- $C_0$  = Shunt capacitance of crystal specified by the crystal manufacturer (4)

表 5-13 lists part numbers of crystals that have been simulated and confirmed to operate within the specifications in 表 5-12. Other crystals that have nearly identical crystal parameters can be expected to work as well.

In 表 5-13, the crystal parameters labeled C0, C1, and L1 are values that are obtained from the crystal manufacturer. These numbers are usually a result of testing a relevant batch of crystals on a network analyzer. The parameters labeled ESR, DL, and  $C_L$  are maximum numbers usually available in the data sheet for a crystal.

表 5-13 also includes three columns of Recommended Component Values. These values apply to system board components.  $C_1$  and  $C_2$  are the values in picofarads of the load capacitors that should be put on each leg of the crystal pins to ensure oscillation at the correct frequency.  $R_s$  is the value in  $k\Omega$  of a resistor that is placed in series with the crystal between the OSC1 pin and the crystal pin.  $R_s$  dissipates some of the power so the Max DL crystal parameter is not exceeded. Only use the recommended  $C_1$ ,  $C_2$ , and  $R_s$  values with the associated crystal part. The values in the table were used in the simulation to ensure crystal start-up and to determine the worst-case drive level (WC DL). The value in the WC DL column should not be greater than the Max DL crystal parameter. The WC DL value can be used to determine if a crystal with similar parameter values but a lower Max DL value is acceptable.

表 5-13. Crystal Parameters

| Manufacturer | Manufacturer Part Number     | Holder   | Package Size (mm × mm) | Frequency (MHz) | Crystal Specification (Tolerance / Stability) | Crystal Parameters |         |         |                    |             |                     | Recommended Component Values |                     |                     | WC DL (μW) |
|--------------|------------------------------|----------|------------------------|-----------------|-----------------------------------------------|--------------------|---------|---------|--------------------|-------------|---------------------|------------------------------|---------------------|---------------------|------------|
|              |                              |          |                        |                 |                                               | Typical Values     |         |         | Max Values         |             |                     |                              |                     |                     |            |
|              |                              |          |                        |                 |                                               | C0 (pF)            | C1 (fF) | L1 (mH) | ESR (Ω)            | Max DL (μW) | C <sub>L</sub> (pF) | C <sub>1</sub> (pF)          | C <sub>2</sub> (pF) | R <sub>s</sub> (kΩ) |            |
| NDK          | NX8045GB-4.000M-STD-CJL-5    | NX8045GB | 8 × 4.5                | 4               | 30 / 50 ppm                                   | 1.00               | 2.70    | 598.10  | 300                | 500         | 8                   | 12                           | 12                  | 0                   | 132        |
| FOX          | FQ1045A-4                    | 2-SMD    | 10 × 4.5               | 4               | 30 / 30 ppm                                   | 1.18               | 4.05    | 396.00  | 150                | 500         | 10                  | 14                           | 14                  | 0                   | 103        |
| NDK          | NX8045GB-5.000M-STD-CSF-4    | NX8045GB | 8 × 4.5                | 5               | 30 / 50 ppm                                   | 1.00               | 2.80    | 356.50  | 250                | 500         | 8                   | 12                           | 12                  | 0                   | 164        |
| NDK          | NX8045GB-6.000M-STD-CSF-4    | NX8045GB | 8 × 4.5                | 6               | 30 / 50 ppm                                   | 1.30               | 4.10    | 173.20  | 250                | 500         | 8                   | 12                           | 12                  | 0                   | 214        |
| FOX          | FQ1045A-6                    | 2-SMD    | 10 × 4.5               | 6               | 30 / 30 ppm                                   | 1.37               | 6.26    | 112.30  | 150                | 500         | 10                  | 14                           | 14                  | 0                   | 209        |
| NDK          | NX8045GB-8.000M-STD-CSF-6    | NX8045GB | 8 × 4.5                | 8               | 30 / 50 ppm                                   | 1.00               | 2.80    | 139.30  | 200                | 500         | 8                   | 12                           | 12                  | 0                   | 277        |
| FOX          | FQ7050B-8                    | 4-SMD    | 7 × 5                  | 8               | 30 / 30 ppm                                   | 1.95               | 6.69    | 59.10   | 80                 | 500         | 10                  | 14                           | 14                  | 0                   | 217        |
| ECS          | ECS-80-16-28A-TR             | HC49/US  | 12.5 × 4.85            | 8               | 50 / 30 ppm                                   | 1.82               | 4.90    | 85.70   | 80                 | 500         | 16                  | 24                           | 24                  | 0                   | 298        |
| Abracon      | AABMM-12.0000MHZ-10-D-1-X-T  | ABMM     | 7.2 × 5.2              | 12              | 10 / 20 ppm                                   | 2.37               | 8.85    | 20.5    | 50                 | 500         | 10                  | 12                           | 12                  | 2.0 <sup>(1)</sup>  | 124        |
| NDK          | NX3225GA-12.000MHZ-STD-CRG-2 | NX3225GA | 3.2 × 2.5              | 12              | 20 / 30 ppm                                   | 0.70               | 2.20    | 81.00   | 100                | 200         | 8                   | 12                           | 12                  | 2.5                 | 147        |
| NDK          | NX5032GA-12.000MHZ-LN-CD-1   | NX5032GA | 5 × 3.2                | 12              | 30 / 50 ppm                                   | 0.93               | 3.12    | 56.40   | 120                | 500         | 8                   | 12                           | 12                  | 0                   | 362        |
| FOX          | FQ5032B-12                   | 4-SMD    | 5 × 3.2                | 12              | 30 / 30 ppm                                   | 1.16               | 4.16    | 42.30   | 80                 | 500         | 10                  | 14                           | 14                  | 0                   | 370        |
| Abracon      | AABMM-16.0000MHZ-10-D-1-X-T  | ABMM     | 7.2 × 5.2              | 16              | 10 / 20 ppm                                   | 3.00               | 11.00   | 9.30    | 50                 | 500         | 10                  | 12                           | 12                  | 2.0 <sup>(1)</sup>  | 143        |
| Ecliptek     | ECX-6595-16.000M             | HC-49/UP | 13.3 × 4.85            | 16              | 15 / 30 ppm                                   | 3.00               | 12.7    | 8.1     | 50                 | 1000        | 10                  | 12                           | 12                  | 2.0 <sup>(1)</sup>  | 139        |
| NDK          | NX3225GA-16.000MHZ-STD-CRG-2 | NX3225GA | 3.2 × 2.5              | 16              | 20 / 30 ppm                                   | 1.00               | 2.90    | 33.90   | 80                 | 200         | 8                   | 12                           | 12                  | 2                   | 188        |
| NDK          | NX5032GA-16.000MHZ-LN-CD-1   | NX5032GA | 5 × 3.2                | 16              | 30 / 50 ppm                                   | 1.02               | 3.82    | 25.90   | 120 <sup>(2)</sup> | 500         | 8                   | 10                           | 10                  | 0                   | 437        |
| ECS          | ECS-160-9-42-CKM-TR          | ECX-42   | 4 × 2.5                | 16              | 10 / 10 ppm                                   | 1.47               | 3.90    | 25.84   | 60                 | 300         | 9                   | 12                           | 12                  | 0.5                 | 289        |
| Abracon      | AABMM-25.0000MHZ-10-D-1-X-T  | ABMM     | 7.2 × 5.2              | 25              | 10 / 20 ppm                                   | 3.00               | 11.00   | 3.70    | 50                 | 500         | 10                  | 12                           | 12                  | 2.0 <sup>(1)</sup>  | 158        |
| Ecliptek     | ECX-6593-25.000M             | HC-49/UP | 13.3 × 4.85            | 25              | 15 / 30 ppm                                   | 3.00               | 12.8    | 3.2     | 40                 | 1000        | 10                  | 12                           | 12                  | 1.5 <sup>(1)</sup>  | 159        |
| NDK          | NX3225GA-25.000MHZ-STD-CRG-2 | NX3225GA | 3.2 × 2.5              | 25              | 20 / 30 ppm                                   | 1.10               | 4.70    | 8.70    | 50                 | 200         | 8                   | 12                           | 12                  | 2                   | 181        |

(1) R<sub>s</sub> values as low as 0 Ω can be used. Using a lower R<sub>s</sub> value causes the WC DL to increase toward the maximum DL of the crystal.

(2) Although this ESR value is outside of the recommended crystal ESR maximum for this frequency, this crystal has been simulated to confirm proper operation and is valid for use with this device.

表 5-13. Crystal Parameters (continued)

| Manufacturer | Manufacturer Part Number           | Holder   | Package Size<br>(mm × mm) | Frequency<br>(MHz) | Crystal Specification<br>(Tolerance / Stability) | Crystal Parameters |            |         |            |                   |                     | Recommended Component Values |                        |                        | WC<br>DL<br>(μW) |
|--------------|------------------------------------|----------|---------------------------|--------------------|--------------------------------------------------|--------------------|------------|---------|------------|-------------------|---------------------|------------------------------|------------------------|------------------------|------------------|
|              |                                    |          |                           |                    |                                                  | Typical Values     |            |         | Max Values |                   |                     | C <sub>1</sub><br>(pF)       | C <sub>2</sub><br>(pF) | R <sub>s</sub><br>(kΩ) |                  |
|              |                                    |          |                           |                    |                                                  | C0<br>(pF)         | C1<br>(fF) | L1 (mH) | ESR<br>(Ω) | Max<br>DL<br>(μW) | C <sub>L</sub> (pF) |                              |                        |                        |                  |
| NDK          | NX5032GA-25.000MHZ-LD-CD-1         | NX5032GA | 5 × 3.2                   | 25                 | 30 / 50 ppm                                      | 1.3                | 5.1        | 7.1     | 70         | 500               | 8                   | 10                           | 10                     | 1.0 <sup>(1)</sup>     | 216              |
|              |                                    |          |                           |                    |                                                  |                    |            |         |            |                   |                     | 12                           | 12                     | 0.75 <sup>(3)</sup>    | 269              |
| AURIS        | Q-25.000M-HC3225/4-F-30-30-E-12-TR | HC3225/4 | 3.2 × 2.5                 | 25                 | 30 / 30 ppm                                      | 1.58               | 5.01       | 8.34    | 50         | 500               | 12                  | 16                           | 16                     | 1                      | 331              |
| FOX          | FQ5032B-25                         | 4-SMD    | 5 × 3.2                   | 25                 | 30 / 30 ppm                                      | 1.69               | 7.92       | 5.13    | 50         | 500               | 10                  | 14                           | 14                     | 0.5                    | 433              |
| TXC          | 7A2570018                          | NX5032GA | 5 × 3.2                   | 25                 | 20 / 25 ppm                                      | 2.0                | 6.7        | 6.1     | 30         | 350               | 10                  | 12                           | 12                     | 2.0 <sup>(3)</sup>     | 124              |

(3) R<sub>S</sub> values as low as 500 Ω can be used. Using a lower R<sub>S</sub> value causes the WC DL to increase toward the maximum DL of the crystal.

#### 5.15.4.6 Main Oscillator Specification With ADC

表 5-14 lists the system clock characteristics with ADC operation.

表 5-14. System Clock Characteristics With ADC Operation

| PARAMETER           |                                                                                | MIN | NOM | MAX | UNIT |
|---------------------|--------------------------------------------------------------------------------|-----|-----|-----|------|
| $f_{\text{sysadc}}$ | System clock frequency when the ADC module is operating (when PLL is bypassed) |     | 16  |     | MHz  |

#### 5.15.4.7 System Clock Characteristics With USB Operation

表 5-15 lists the system clock characteristics with USB operation.

表 5-15. System Clock Characteristics With USB Operation

| PARAMETER           |                                                                                                                               | MIN | NOM | MAX | UNIT |
|---------------------|-------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| $f_{\text{sysusb}}$ | System clock frequency when the USB module is operating (MOSC must be the clock source, either with or without using the PLL) | 30  |     |     | MHz  |

#### 5.15.5 Sleep Modes

The following tables can be used to calculate the maximum wake time from sleep or deep sleep mode, depending on the specific application. Depending on the application configuration, each parameter, except for  $t_{\text{FLASH}}$ , adds sequential latency to the wake time. Flash restoration happens in parallel to the other wake processes, and its wake time is normally absorbed by the other latencies. As an example, the wake time for a device in deep sleep mode with the PIOSC and PLL turned off and the flash and SRAM in low-power mode is calculated by 公式 5.

$$\text{Wake Time} = t_{\text{PIOSCDS}} + t_{\text{PLLDS}} + t_{\text{SRAMLPS}} \quad (5)$$

$t_{\text{FLASH}}$  does not contribute to this equation because the values of the other parameters are greater.

In sleep mode, the wake time due to a clock source is zero because the device uses the same clock configuration in run mode; thus, there is no latency involved with respect to the clocks.

表 5-16 lists the wake-up times from sleep mode.

表 5-16. Wake From Sleep Characteristics

over operating free-air temperature (unless otherwise noted)

| NO. | PARAMETER             |                                                                          | MIN | TYP | MAX | UNIT          |
|-----|-----------------------|--------------------------------------------------------------------------|-----|-----|-----|---------------|
| D1  | $t_{\text{PIOSC}}$    | Time to restore PIOSC as system clock in sleep mode                      |     |     | N/A | $\mu\text{s}$ |
| D2  | $t_{\text{MOSC}}$     | Time to restore MOSC as system clock in sleep mode                       |     |     | N/A | $\mu\text{s}$ |
| D3  | $t_{\text{PLL}}$      | Time to restore PLL as system clock in sleep mode                        |     |     | N/A | $\mu\text{s}$ |
| D4  | $t_{\text{LDO}}$      | Time to restore LDO to 1.2 V in sleep mode                               |     |     | 39  | $\mu\text{s}$ |
| D5  | $t_{\text{FLASH}}$    | Time to restore flash to active state from low-power state in sleep mode |     |     | 96  | $\mu\text{s}$ |
| D6  | $t_{\text{SRAMLPS}}$  | Time to restore SRAM to active state from low-power state in sleep mode  |     |     | 15  | $\mu\text{s}$ |
| D7  | $t_{\text{SRAMSTBY}}$ | Time to restore SRAM to active state from standby state in sleep mode    |     |     | 15  | $\mu\text{s}$ |

表 5-16 lists the wake-up times from deep sleep mode.

**表 5-17. Wake From Deep Sleep Characteristics**

over operating free-air temperature (unless otherwise noted)

| NO. | PARAMETER                                                                  | MIN | TYP | MAX                                                                            | UNIT                    |
|-----|----------------------------------------------------------------------------|-----|-----|--------------------------------------------------------------------------------|-------------------------|
| D8  | $t_{PIOSCDS}$ Time to restore PIOSC as system clock in deep sleep mode     |     |     | 14                                                                             | deep-sleep clock cycles |
| D9  | $t_{MOSCDS}$ Time to restore MOSC as system clock in deep sleep mode       |     |     | 18                                                                             | ms                      |
| D10 | $t_{PL LDS}$ Time to restore PLL as system clock in deep sleep mode        |     |     | 1 cycle of deep sleep clock + 512 cycles of PLL reference clock <sup>(1)</sup> | clock cycles            |
| D11 | $t_{LDODS}$ Time to restore LDO to 1.2 V in deep sleep mode                |     |     | 39                                                                             | μs                      |
| D12 | $t_{FLASHLPDS}$ Time to restore flash to active state from low-power state |     |     | 96                                                                             | μs                      |
| D13 | $t_{SRAML PDS}$ Time to restore SRAM to active state from low-power state  |     |     | 15                                                                             | μs                      |
| D14 | $t_{SRAMSTBYDS}$ Time to restore SRAM to active state from standby state   |     |     | 15                                                                             | μs                      |

(1) Deep sleep clock can vary. See the *System Control* chapter of the [MSP432E4 SimpleLink™ Microcontrollers Technical Reference Manual](#) for the deep sleep clock options.

### 5.15.6 Hibernation Module

The Hibernation module requires special system implementation considerations because it is intended to power down all other sections of its host device. See the *Hibernation Module* chapter of the [MSP432E4 SimpleLink™ Microcontrollers Technical Reference Manual](#).

表 5-18 lists the required characteristics of the Hibernation module battery.

**表 5-18. Hibernation Module Battery Characteristics**

over operating free-air temperature (unless otherwise noted)

| PARAMETER                                               | MIN           | NOM | MAX | UNIT |
|---------------------------------------------------------|---------------|-----|-----|------|
| $V_{BAT}$ Battery supply voltage                        | 1.8           | 3.0 | 3.6 | V    |
| $V_{BATRMP}$ $V_{BAT}$ battery supply voltage ramp time | 0             |     | 0.7 | V/μs |
| $V_{LOWBAT}$ Low-battery detect voltage                 | VBATSEL = 0x0 | 1.8 | 1.9 | 2.0  |
|                                                         | VBATSEL = 0x1 | 2.0 | 2.1 | 2.2  |
|                                                         | VBATSEL = 0x2 | 2.2 | 2.3 | 2.4  |
|                                                         | VBATSEL = 0x3 | 2.4 | 2.5 | 2.6  |

表 5-19 lists the timing characteristics of the HIB module.

**表 5-19. Hibernation Module Characteristics**

over operating free-air temperature (unless otherwise noted) (see 图 5-13)

| NO. | PARAMETER            |                                                                                                          | MIN | TYP                | MAX | UNIT                    |
|-----|----------------------|----------------------------------------------------------------------------------------------------------|-----|--------------------|-----|-------------------------|
| H1  | $t_{WAKE}$           | $\overline{WAKE}$ assertion time                                                                         | 100 |                    |     | ns                      |
| H2  | $t_{WAKE\_TO\_HIB}$  | $\overline{WAKE}$ assert to $\overline{HIB}$ desassert (wake-up time)                                    |     |                    | 1   | HIB module clock period |
| H3  | $t_{VDD\_RAMP}$      | $V_{DD}$ ramp to 3.0 V                                                                                   |     | See <sup>(1)</sup> |     | $\mu$ s                 |
| H4  | $t_{VDD\_CODE}$      | $V_{DD}$ at 3 V to internal POR deassert; first instruction executes                                     |     |                    | 500 | $\mu$ s                 |
| H5  | DC <sub>RTCCLK</sub> | Duty cycle for RTCCLK output signal, when using a 32.768-kHz crystal                                     | 40% |                    | 60% |                         |
|     |                      | Duty cycle for RTCCLK output signal, when using a 32.768-kHz external single-ended (bypass) clock source | 30% |                    | 70% |                         |

(1) Depends on characteristics of power supply.

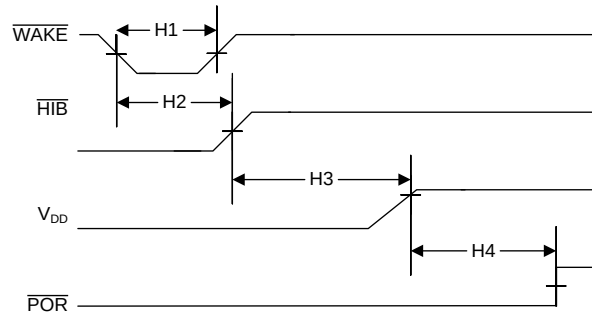


**图 5-13. Hibernation Module Timing**

表 5-20 lists the characteristics of the HIB module tamper detection.

**表 5-20. Hibernation Module Tamper I/O Characteristics**

over operating free-air temperature (unless otherwise noted)

| PARAMETER        |                                                                     | MIN                  | TYP | MAX | UNIT       |
|------------------|---------------------------------------------------------------------|----------------------|-----|-----|------------|
| R <sub>TPU</sub> | TMPRn pullup resistor                                               | 3.5                  | 4.4 | 5.2 | M $\Omega$ |
| $t_{SP}$         | TMPRn pulse duration with short glitch filter                       | 62                   |     |     | $\mu$ s    |
| $t_{LP}$         | TMPRn pulse duration with long glitch filter                        | 94                   |     |     | ms         |
| $t_{NMIS}$       | TMPRn assertion to NMI (short glitch filter)                        |                      |     | 95  | $\mu$ s    |
| $t_{NMIL}$       | TMPRn assertion to NMI (long glitch filter)                         |                      |     | 94  | ms         |
| V <sub>IH</sub>  | TMPRn high-level input voltage when operating from V <sub>BAT</sub> | $V_{BAT} \times 0.8$ |     |     | V          |

### 5.15.7 Flash Memory

表 5-21 lists the characteristics of the flash memory.

**表 5-21. Flash Memory Characteristics**

over operating free-air temperature (unless otherwise noted)

| PARAMETER            |                                                                                                                   | MIN         | TYP | MAX | UNIT   |
|----------------------|-------------------------------------------------------------------------------------------------------------------|-------------|-----|-----|--------|
| PE <sub>CYC</sub>    | Number of program and erase cycles                                                                                | 100000      |     |     | cycles |
| t <sub>RET</sub>     | Data retention with 100% power-on hours at T <sub>J</sub> = 85°C                                                  | 20          |     |     | years  |
| t <sub>RET_EXT</sub> | Data retention with 10% power-on hours at T <sub>J</sub> = 125°C and 90% power-on hours at T <sub>J</sub> = 100°C | 11          |     |     | years  |
| t <sub>PROG64</sub>  | Program time for double-word-aligned (64 bits) data                                                               | 30          | 100 | 300 | μs     |
| t <sub>ERASE</sub>   | Page erase time                                                                                                   | <1k cycles  |     | 8   | 15     |
|                      |                                                                                                                   | 10k cycles  |     | 15  | 40     |
|                      |                                                                                                                   | 100k cycles |     | 75  | 500    |
| t <sub>ME</sub>      | Mass erase time                                                                                                   | <1k cycles  |     | 10  | 25     |
|                      |                                                                                                                   | 10k cycles  |     | 20  | 70     |
|                      |                                                                                                                   | 100k cycles |     | 300 | 2500   |

### 5.15.8 EEPROM

表 5-22 lists the characteristics of the EEPROM.

**表 5-22. EEPROM Characteristics**

over operating free-air temperature (unless otherwise noted)

| PARAMETER             |                                                                                                                                                                | MIN         | TYP         | MAX         | UNIT                      |
|-----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|-------------|-------------|---------------------------|
| EPE <sub>CYC</sub>    | Number of mass program and erase cycles of a single word                                                                                                       | 500000      |             |             | cycles                    |
| ET <sub>RET</sub>     | Data retention with 100% power-on hours at T <sub>J</sub> = 85°C                                                                                               | 20          |             |             | years                     |
| ET <sub>RET_EXT</sub> | Data retention with 10% power-on hours at T <sub>J</sub> = 125°C and 90% power-on hours at T <sub>J</sub> = 100°C                                              | 11          |             |             | years                     |
| ET <sub>PROG</sub>    | Program time for 32 bits of data with memory space available                                                                                                   |             | 110         | 600         | μs                        |
|                       | Program time for 32 bits of data in which a copy to the copy buffer is required, the copy buffer has space, and less than 10% of EEPROM endurance used         |             | 30          |             | ms                        |
|                       | Program time for 32 bits of data in which a copy to the copy buffer is required, the copy buffer has space, and more than 90% of EEPROM endurance used         |             |             | 900         |                           |
|                       | Program time for 32 bits of data in which a copy of the copy buffer is required, the copy buffer requires an erase, and less than 10% of EEPROM endurance used |             | 60          |             |                           |
|                       | Program time for 32 bits of data a copy to the copy buffer is required, the copy buffer requires an erase, and more than 90% of EEPROM endurance used          |             |             | 1800        |                           |
| ET <sub>READ</sub>    | Read access time                                                                                                                                               |             | 7 +<br>2EWS | 9 +<br>4EWS | system<br>clock<br>cycles |
| ET <sub>ME</sub>      | Mass erase time                                                                                                                                                | <1k cycles  |             | 8           | 15                        |
|                       |                                                                                                                                                                | 10k cycles  |             | 15          | 40                        |
|                       |                                                                                                                                                                | 100k cycles |             | 75          | 500                       |

### 5.15.9 Input/Output Pin Characteristics

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注

All GPIO signals are 3.3-V tolerant, except for PB1 (USB0VBUS) which is 5-V tolerant. See the *General-Purpose Input/Outputs (GPIOs)* chapter of the [MSP432E4 SimpleLink™ Microcontrollers Technical Reference Manual](#) for more information on GPIO configuration.

---

Two types of pads are provided on the device:

- Fast GPIO pads: These pads provide variable, programmable drive strength and optimized voltage output levels.
- Slow GPIO pads: These pads provide 2-mA drive strength and are designed to be sensitive to voltage inputs. The following GPIOs port pins are designed with slow GPIO pads:
  - PJ1

---

注

Port pins PL6 and PL7 operate as fast GPIO pads, but have 4-mA drive capability only. GPIO register controls for drive strength, slew rate, and open drain have no effect on these pins. The following registers have no effect: GPIODR2R, GPIODR4R, GPIODR8R, GPIODR12R, GPIOSLR, and GPIOODR.

---

---

注

Port pins PM[7:4] operate as fast GPIO pads but support *only* 2-, 4-, 6-, and 8-mA drive capability. All standard GPIO register controls, except for the GPIODR12R register, apply to these port pins.

---

表 5-23 lists the characteristics of the fast GPIOs.

**表 5-23. Fast GPIO Module Characteristics**

over operating free-air temperature (unless otherwise noted) <sup>(1)</sup> <sup>(2)</sup> <sup>(3)</sup> <sup>(4)</sup>

| PARAMETER              |                                                                                                                                         | MIN                               | TYP  | MAX   | UNIT |
|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|------|-------|------|
| C <sub>LGPIO</sub>     | Capacitive loading for measurements given in this table <sup>(5)</sup>                                                                  |                                   |      | 50    | pF   |
| R <sub>GPIOPU</sub>    | Fast GPIO internal pullup resistor <sup>(6)</sup>                                                                                       | 12.1                              | 16.0 | 20.2  | kΩ   |
| R <sub>GPIOPU4MA</sub> | Fast GPIO PL6 and PL7 (4 mA only) pullup resistor                                                                                       | 25                                |      | 40    | kΩ   |
| R <sub>GPIOPD</sub>    | Fast GPIO internal pulldown resistor <sup>(6)</sup>                                                                                     | 13.0                              | 20.5 | 35.5  | kΩ   |
| R <sub>GPIOPD4MA</sub> | Fast GPIO PL6 and PL7 (4 mA only) pulldown resistor                                                                                     | 10                                | 14.3 | 17    | kΩ   |
| I <sub>LKG+</sub>      | Fast GPIO input leakage current, 0 V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub> GPIO pins <sup>(7)</sup>                                       |                                   |      | 400   | nA   |
|                        | Fast GPIO input leakage current, 0 V < V <sub>IN</sub> ≤ V <sub>DD</sub> , fast GPIO pins configured as ADC or analog comparator inputs |                                   |      | 400   |      |
| I <sub>INJ-</sub>      | DC injection current, V <sub>IN</sub> ≤ 0 V                                                                                             |                                   |      | 60    | μA   |
| I <sub>MAXINJ-</sub>   | Maximum negative injection if not voltage protected <sup>(8)</sup>                                                                      |                                   |      | −0.5  | mA   |
| t <sub>GPIOR</sub>     | Fast GPIO rise time <sup>(9)</sup>                                                                                                      | 2-mA drive                        | 7.85 | 11.73 | ns   |
|                        |                                                                                                                                         | 4-mA drive                        | 4.15 | 6.35  |      |
|                        |                                                                                                                                         | 8-mA drive                        | 2.33 | 3.73  |      |
|                        |                                                                                                                                         | 8-mA drive with slew rate control | 3.77 | 5.76  |      |
|                        |                                                                                                                                         | 10-mA drive                       | 1.98 | 3.22  |      |
|                        |                                                                                                                                         | 12-mA drive                       | 1.75 | 2.9   |      |
| t <sub>GPIOF</sub>     | Fast GPIO fall time <sup>(10)</sup>                                                                                                     | 2-mA drive                        | 10.3 | 16.5  | ns   |
|                        |                                                                                                                                         | 4-mA drive                        | 5.15 | 8.29  |      |
|                        |                                                                                                                                         | 8-mA drive                        | 2.58 | 4.16  |      |
|                        |                                                                                                                                         | 8-mA drive with slew rate control | 3.54 | 5.55  |      |
|                        |                                                                                                                                         | 10-mA drive                       | 2.07 | 3.34  |      |
|                        |                                                                                                                                         | 12-mA drive                       | 1.73 | 2.78  |      |

(1) V<sub>DD</sub> must be within the range specified in Section 5.4.

(2) Leakage and Injection current characteristics specified in this table also apply to XOSC0 and XOSC1 inputs.

(3) For the external reference inputs of the ADC, avoid a current-limiting resistor (see the I<sub>VREF</sub> specification in 表 5-33).

(4) I/O pads should be protected if the I/O voltage may go outside the limits shown in the table. If the part is unpowered, the I/O pad voltage or current must be limited (as shown in this table) to avoid powering the part through the I/O pad, which can potentially cause irreversible damage.

(5) See the individual peripheral sections for specific loading information.

(6) This value includes all GPIO except for port pins PL6 and PL7.

(7) The leakage current is measured with V<sub>IN</sub> applied to the corresponding pins. The leakage of digital port pins is measured individually. The port pin is configured as an input and the pullup/pulldown resistor is disabled.

(8) If the I/O pad is not voltage limited, it should be current limited (to I<sub>INJ</sub> + and I<sub>INJ-</sub>) if there is any possibility of the pad voltage exceeding the V<sub>IO</sub> limits (including transient behavior during supply ramp up, or at any time when the part is unpowered).

(9) Time measured from 20% to 80% of V<sub>DD</sub>.

(10) Time measured from 80% to 20% of V<sub>DD</sub>.

表 5-24 lists the characteristics of the slow GPIOs.

**表 5-24. Slow GPIO Module Characteristics**

over operating free-air temperature (unless otherwise noted)<sup>(1)(2)(3)</sup>

| PARAMETER           |                                                                                                                                    | MIN  | TYP  | MAX  | UNIT |
|---------------------|------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| C <sub>LGPIO</sub>  | Capacitive loading for measurements given in this table <sup>(4)</sup>                                                             |      |      | 50   | pF   |
| R <sub>GPIOPU</sub> | Slow GPIO internal pullup resistor                                                                                                 | 13.8 | 20.0 | 31.4 | kΩ   |
| R <sub>GPIOPD</sub> | Slow GPIO internal pulldown resistor                                                                                               | 13.0 | 20.5 | 35.5 | kΩ   |
| I <sub>LKG+</sub>   | Slow GPIO input leakage current, 0 V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub> , GPIO pins <sup>(5)</sup>                                |      |      | 3.25 | nA   |
|                     | Slow GPIO input leakage current, 0 V < V <sub>IN</sub> ≤ V <sub>DD</sub> , GPIO pins configured as ADC or analog comparator inputs |      |      | 3.25 |      |
| I <sub>INJ-</sub>   | DC injection current, V <sub>IN</sub> ≤ 0 V                                                                                        |      |      | 3.42 | μA   |
| t <sub>GPIOR</sub>  | Slow GPIO rise time, 2-mA drive <sup>(6)</sup>                                                                                     |      | 19.3 | 29.8 | ns   |
| t <sub>GPIOF</sub>  | Slow GPIO fall time, 2-mA drive <sup>(7)</sup>                                                                                     |      | 12.8 | 21.1 | ns   |

(1) V<sub>DD</sub> must be within the range specified in [Section 5.4](#).

(2) V<sub>IN</sub> must be within the range specified in [Section 5.1](#). Leakage current outside of this maximum voltage is not ensured and can result in permanent damage of the device.

(3) To avoid potential damage to the part, externally limit either the voltage or current on the I/Os other than power and WAKE as listed in this table.

(4) See the individual peripheral sections for specific loading information.

(5) The leakage current is measured with V<sub>IN</sub> applied to the corresponding pins. The leakage of digital port pins is measured individually. The port pin is configured as an input and the pullup/pulldown resistor is disabled.

(6) Time measured from 20% to 80% of V<sub>DD</sub>.

(7) Time measured from 80% to 20% of V<sub>DD</sub>.

### 5.15.9.1 Types of I/O Pins and ESD Protection

#### CAUTION

All device I/Os pins, except for PB1, are NOT 5-V tolerant; voltages in excess of the limits in [Section 5.4](#) can permanently damage the device. PB1 is used for the USB0VBUS signal, which requires a 5-V input.

#### 5.15.9.1.1 Hibernate $\overline{\text{WAKE}}$ pin

The Hibernate  $\overline{\text{WAKE}}$  pin uses ESD protection, similar to the one shown in [图 5-14](#). This ESD protection prevents a direct path between this pad and any power supply rails in the device. The  $\overline{\text{WAKE}}$  pad input voltage should be kept inside the maximum ratings specified in [Section 5.1](#) to ensure current leakage and current injections are within acceptable range. [表 5-25](#) lists current leakages and current injection for these pins.

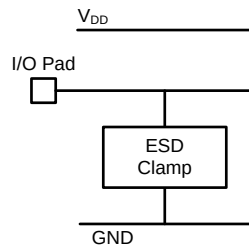


图 5-14. ESD Protection

表 5-25. Pad Voltage and Current Characteristics for Hibernate  $\overline{\text{WAKE}}$  Pin

over operating free-air temperature (unless otherwise noted) <sup>(1)(2)</sup>

| PARAMETER         |                                                                                                 | MIN | TYP | MAX  | UNIT          |
|-------------------|-------------------------------------------------------------------------------------------------|-----|-----|------|---------------|
| $I_{\text{LKG+}}$ | Positive I/O leakage for $V_{\text{DD}} \leq V_{\text{IN}} \leq V_{\text{BAT}} + 0.3 \text{ V}$ |     |     | 300  | nA            |
| $I_{\text{LKG-}}$ | Negative I/O leakage for $-0.3 \text{ V} \leq V_{\text{IN}} \leq 0 \text{ V}^{(3)}$             |     |     | 43.3 | $\mu\text{A}$ |
| $I_{\text{INJ+}}$ | Maximum positive injection if not voltage protected                                             |     |     | 2    | mA            |
| $I_{\text{INJ-}}$ | Maximum negative injection if not voltage protected <sup>(4)</sup>                              |     |     | -0.5 | mA            |

- (1)  $V_{\text{IN}}$  must be within the range specified in [Section 5.1](#). Leakage current outside of this maximum voltage is not ensured and can result in permanent damage of the device.
- (2)  $V_{\text{DD}}$  must be within the range specified in [Section 5.4](#).
- (3) Leakage outside the minimum range ( $-0.3 \text{ V}$ ) is unbounded and must be limited to  $I_{\text{INJ-}}$  using an external resistor.
- (4) If the I/O pad is not voltage limited, it should be current limited (to  $I_{\text{INJ+}}$  and  $I_{\text{INJ-}}$ ) if there is any possibility of the pad voltage exceeding the  $V_{\text{IO}}$  limits (including transient behavior during supply ramp up, or at any time when the part is unpowered).

### 5.15.9.1.2 Nonpower I/O Pins

Most nonpower I/Os (with the exception of the I/O pad for Hibernate  $\overline{\text{WAKE}}$  input) have ESD protection as shown in 图 5-15.

These I/Os have an ESD clamp to ground and a diode connection to the corresponding power supply rail. To prevent potential damage to the device, follow the specifications in 表 5-26 for the voltage and current of these I/Os. In addition, comply with that the ADC external reference specifications in 表 5-33 to prevent gain error.

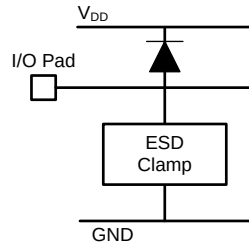


图 5-15. ESD Protection for Nonpower Pins (Except  $\overline{\text{WAKE}}$  Signal)

表 5-26. Nonpower I/O Pad Voltage and Current Characteristics

over operating free-air temperature (unless otherwise noted) <sup>(1)</sup> <sup>(2)</sup> <sup>(3)</sup>

| PARAMETER  |                                                                                  | MIN  | TYP      | MAX            | UNIT    |
|------------|----------------------------------------------------------------------------------|------|----------|----------------|---------|
| $V_{IO}$   | I/O pad voltage limits if voltage protected                                      | -0.3 | $V_{DD}$ | $V_{DD} + 0.3$ | V       |
| $I_{LKG+}$ | Positive I/O leakage for $V_{DD} \leq V_{IN} \leq V_{IO}$ <sup>(4)</sup>         |      |          | 400            | nA      |
| $I_{LKG-}$ | Negative I/O leakage for $V_{IO} \text{ MIN} \leq V_{IN} \leq 0V$ <sup>(4)</sup> |      |          | 60             | $\mu A$ |
| $I_{INJ+}$ | Maximum positive injection if not voltage protected <sup>(5)</sup>               |      |          | 2              | mA      |
| $I_{INJ-}$ | Maximum negative injection if not voltage protected <sup>(5)</sup>               |      |          | -0.5           | mA      |

- (1) To avoid potential damage to the part, externally limit either the voltage or current on I/Os other than power and  $\overline{\text{WAKE}}$  as listed in this table.
- (2) For the external reference inputs of the ADC, avoid a current-limiting resistor (see the  $I_{VREF}$  specification in 表 5-33).
- (3) I/O pads should be protected if at any point the I/O voltage has a possibility of going outside the limits shown in the table. If the part is unpowered, the I/O pad voltage and current must be limited (as shown in this table) to avoid powering the part through the I/O pad, which can potentially cause irreversible damage.
- (4) MIN and MAX leakage current for the case when the I/O is voltage protected to  $V_{IO} \text{ MIN}$  or  $V_{IO} \text{ MAX}$ .
- (5) If the I/O pad is not voltage limited, it should be current limited (to  $I_{INJ+}$  and  $I_{INJ-}$ ) if there is any possibility of the pad voltage exceeding the  $V_{IO}$  limits (including transient behavior during supply ramp up, or at any time when the part is unpowered).

### 5.15.10 External Peripheral Interface (EPI)

表 5-27 lists the load conditions used to characterize the EPI interface.

**表 5-27. EPI Interface Load Conditions**

| SIGNALS                               | LOAD VALUE ( $C_L$ ) |
|---------------------------------------|----------------------|
| EPIOS[35:0] SDRAM interface           | 30 pF                |
| EPIOS[35:0] General-Purpose interface |                      |
| EPIOS[35:0] Host-Bus interface        |                      |
| EPIOS[35:0] PSRAM interface           | 40 pF                |

When the EPI module is in SDRAM mode, EPI CLK (EPIOS31) must be configured to 12 mA. The EPI data bus can be configured to 8 mA. 表 5-28 lists the rise and fall times in SDRAM mode.

**表 5-28. EPI SDRAM Characteristics**

over operating free-air temperature (unless otherwise noted)

| PARAMETER                                                 | TEST CONDITIONS            | MIN | TYP | MAX | UNIT |
|-----------------------------------------------------------|----------------------------|-----|-----|-----|------|
| $t_{SDRAMR}$ EPI rise time (from 20% to 80% of $V_{DD}$ ) | 12-mA drive, $C_L = 30$ pF |     | 2   | 3   | ns   |
| $t_{SDRAMF}$ EPI fall time (from 80% to 20% of $V_{DD}$ ) | 12-mA drive, $C_L = 30$ pF |     | 2   | 3   | ns   |

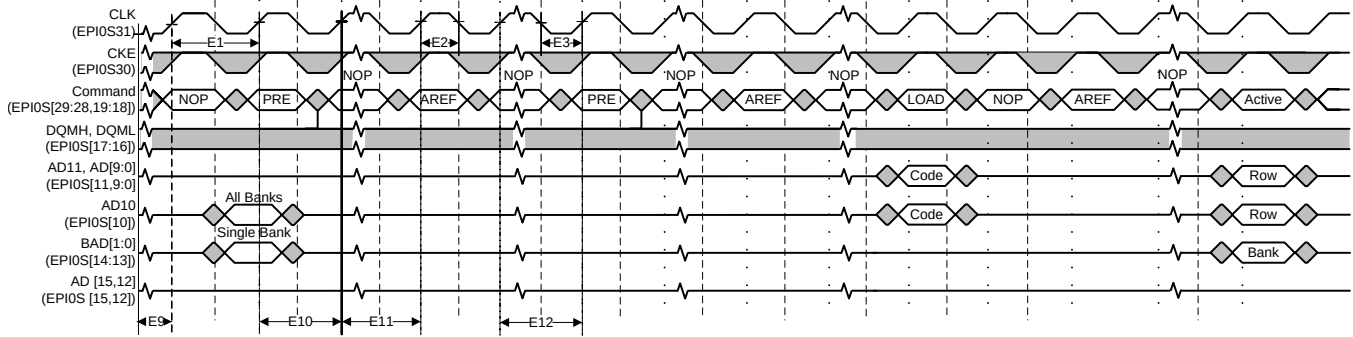
表 5-29 lists the switching characteristics of the SDRAM interface.

**表 5-29. EPI SDRAM Interface Characteristics**

over operating free-air temperature (unless otherwise noted) <sup>(1)</sup> (see 图 5-16, 图 5-17, and 图 5-18)

| NO. | PARAMETER                        | MIN   | TYP | MAX | UNIT    |
|-----|----------------------------------|-------|-----|-----|---------|
| E1  | $t_{CK}$ SDRAM clock period      | 16.67 |     |     | ns      |
| E2  | $t_{CH}$ SDRAM clock high time   | 8.33  |     |     | ns      |
| E3  | $t_{CL}$ SDRAM clock low time    | 8.33  |     |     | ns      |
| E4  | $t_{COV}$ CLK to output valid    |       |     | 4   | ns      |
| E5  | $t_{COI}$ CLK to output invalid  |       |     | 4   | ns      |
| E6  | $t_{COT}$ CLK to output tristate |       |     | 4   | ns      |
| E7  | $t_S$ Input set up to CLK        | 8.5   |     |     | ns      |
| E8  | $t_H$ CLK to input hold          | 0     |     |     | ns      |
| E9  | $t_{PU}$ Power-up time           | 100   |     |     | μs      |
| E10 | $t_{RP}$ Precharge all banks     | 20    |     |     | ns      |
| E11 | $t_{RFC}$ Auto refresh           | 66    |     |     | ns      |
| E12 | $t_{MRD}$ Program mode register  | 2     |     |     | EPI CLK |

(1) The EPI SDRAM interface must use 12-mA drive.



- (1) If CS is high at clock high time, all applied commands are NOP.
- (2) The Mode register can be loaded before the autorefresh cycles.
- (3) JEDEC and PC100 specify 3 clock cycles.
- (4) Outputs are Hi-Z after the command is issued.

**图 5-16. SDRAM Initialization and Load Mode Register Timing**

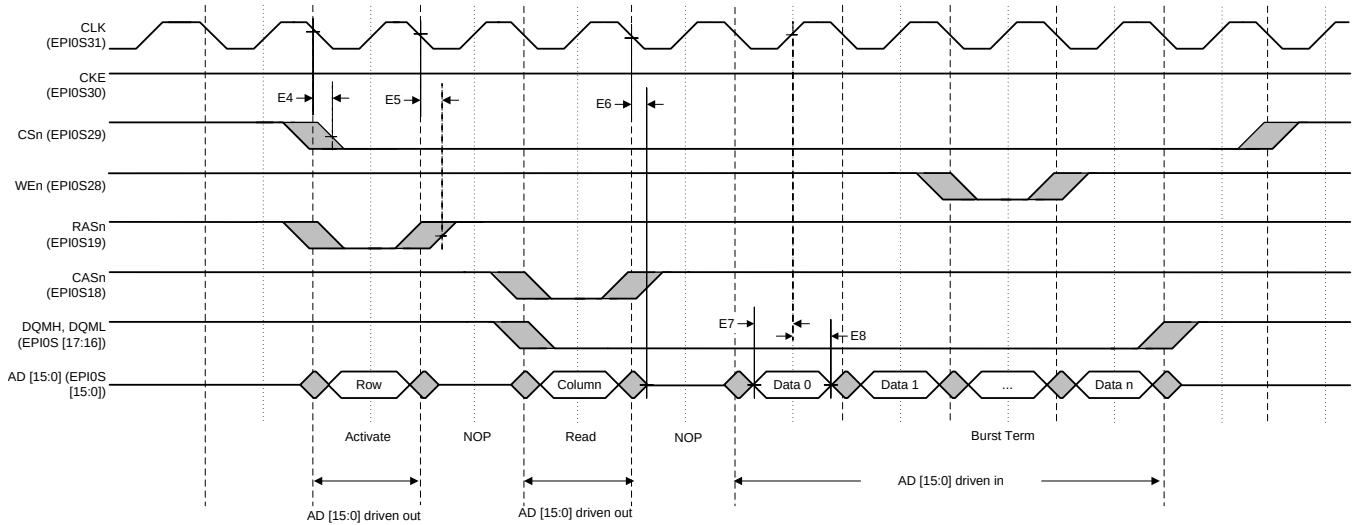


**图 5-17. SDRAM Read Timing**

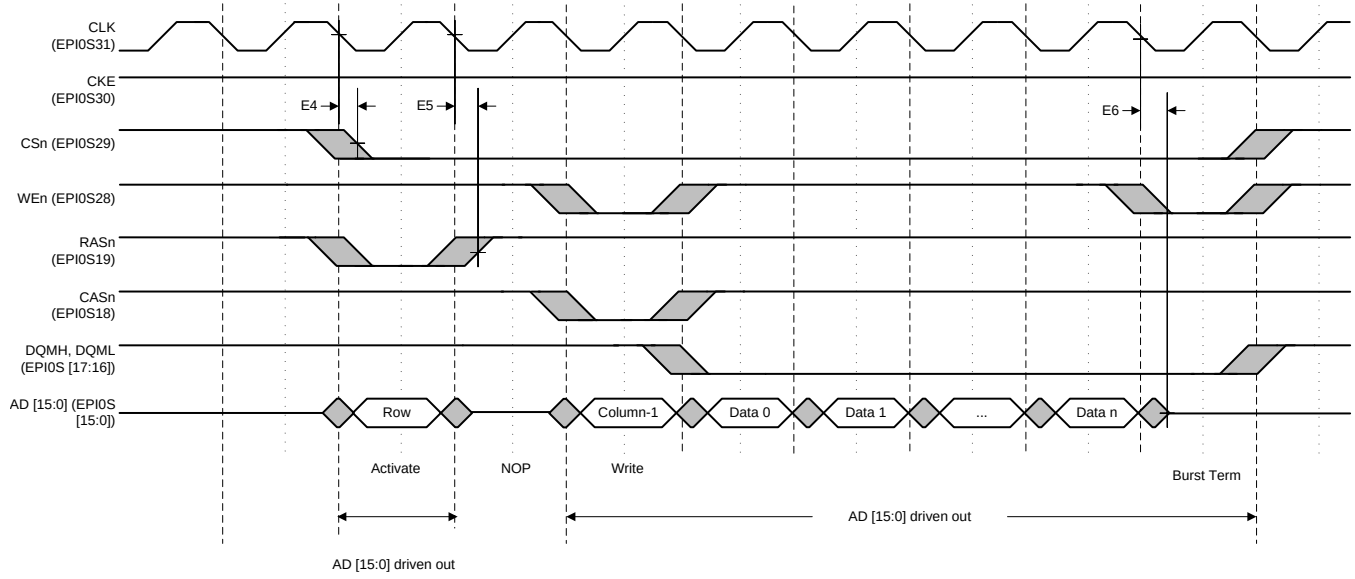


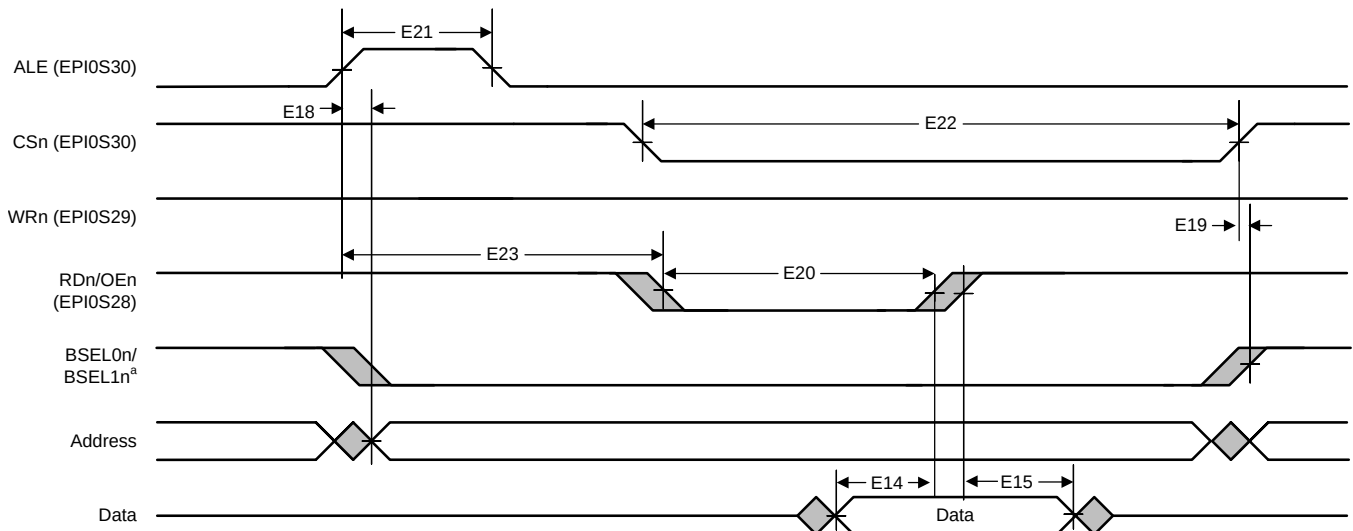
图 5-18. SDRAM Write Timing

表 5-30 lists the characteristics of the Host-Bus 8 and Host-Bus 16 interface.

**表 5-30. EPI Host-Bus 8 and Host-Bus 16 Interface Characteristics**

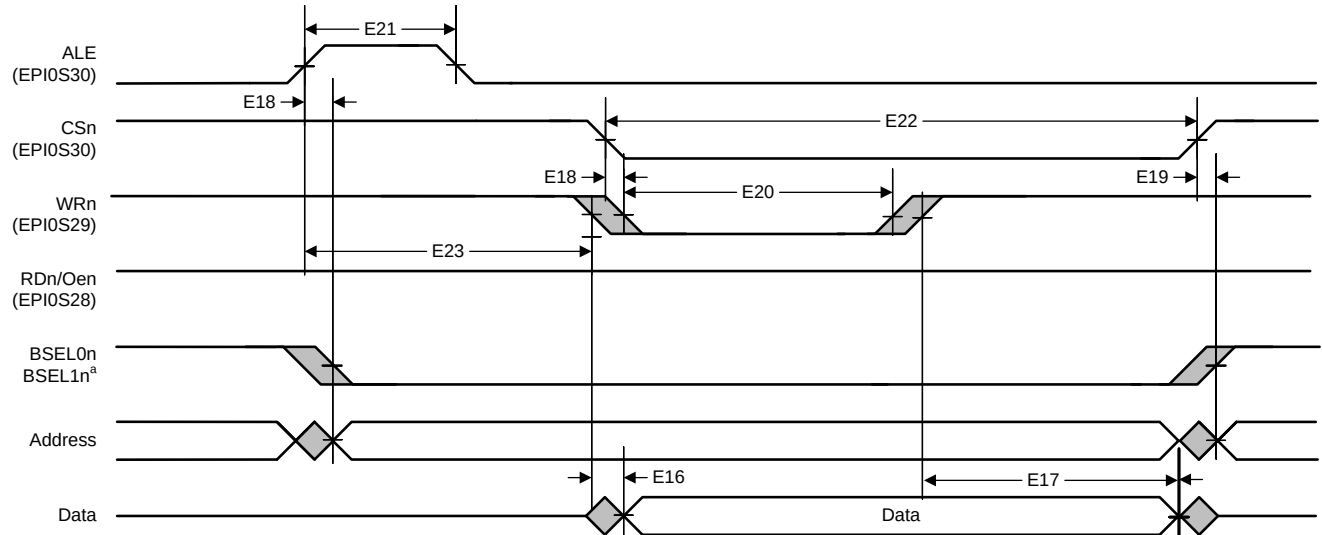
over operating free-air temperature (unless otherwise noted) (see 图 5-19, 图 5-20, 图 5-21, and 图 5-22)

| NO. | PARAMETER            |                                        | MIN | TYP | MAX | UNIT             |
|-----|----------------------|----------------------------------------|-----|-----|-----|------------------|
| E14 | $t_{\text{ISU}}$     | Read data set up time                  | 10  |     |     | ns               |
| E15 | $t_{\text{IH}}$      | Read data hold time                    | 0   |     |     | ns               |
| E16 | $t_{\text{DV}}$      | WRn to write data valid                |     |     | 3.6 | ns               |
| E17 | $t_{\text{DI}}$      | Data hold from WRn invalid             | 1   |     |     | EPI clock cycles |
| E18 | $t_{\text{OV}}$      | ALE/CSn to output valid                |     |     | 4   | ns               |
| E19 | $t_{\text{OINV}}$    | CSn to output invalid                  |     |     | 4   | ns               |
| E20 | $t_{\text{STLOW}}$   | WRn / RDn strobe duration low          | 1   |     |     | EPI clock cycles |
| E21 | $t_{\text{ALEHIGH}}$ | ALE duration high                      |     | 1   |     | EPI clock cycles |
| E22 | $t_{\text{CSLOW}}$   | CSn duration low                       | 2   |     |     | EPI clock cycles |
| E23 | $t_{\text{ALEST}}$   | ALE rising to WRn / RDn strobe falling | 2   |     |     | EPI clock cycles |
| E24 | $t_{\text{ALEADD}}$  | ALE falling to Address high impedance  | 1   |     |     | EPI clock cycles |



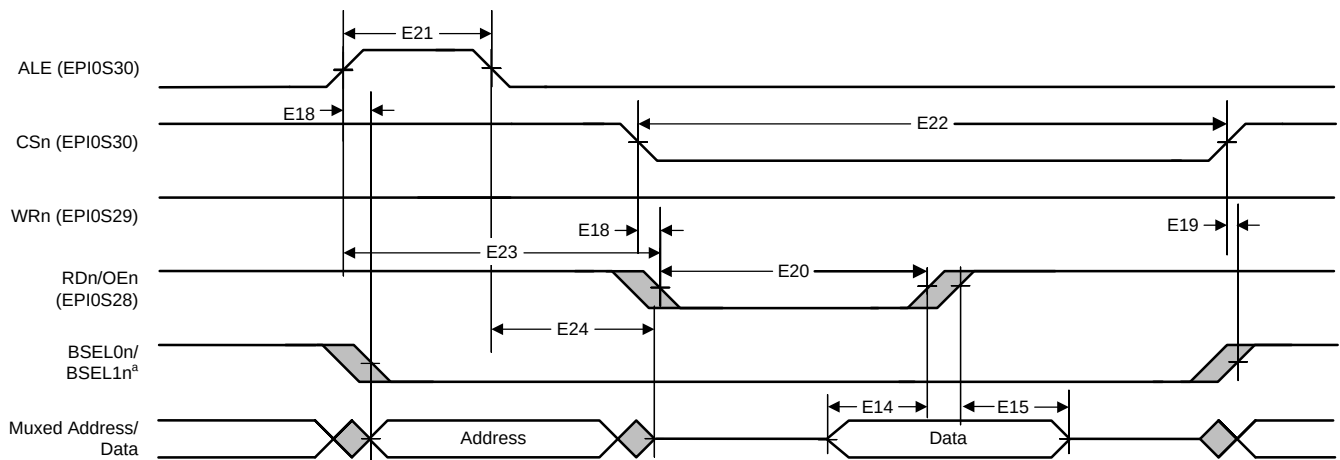
<sup>a</sup> BSEL0n and BSEL1n are available in Host-Bus 16 mode only.

**图 5-19. Host-Bus 8/16 Asynchronous Mode Read Timing**



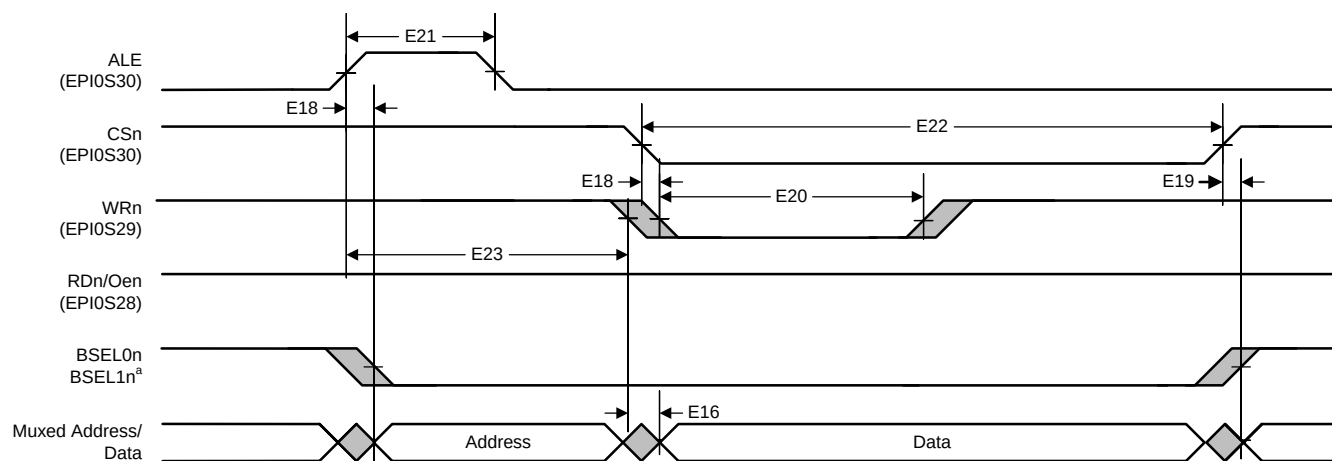
<sup>a</sup> BSEL0n and BSEL1n are available in Host-Bus 16 mode only.

**图 5-20. Host-Bus 8/16 Asynchronous Mode Write Timing**



<sup>a</sup> BSEL0n and BSEL1n are available in Host-Bus 16 mode only.

**图 5-21. Host-Bus 8/16 Mode Asynchronous Muxed Read Timing**



<sup>a</sup> BSEL0n and BSEL1n are available in Host-Bus 16 mode only.

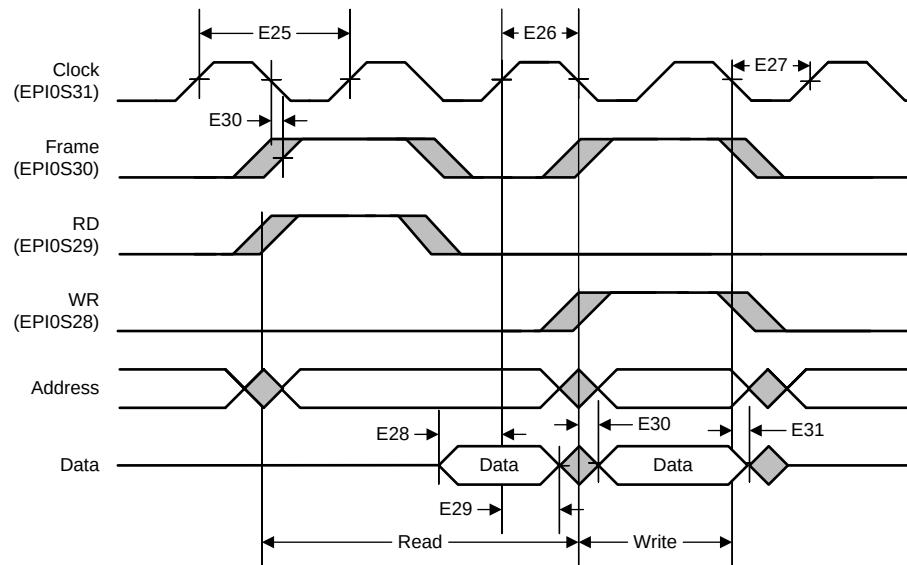
**图 5-22. Host-Bus 8/16 Mode Asynchronous Muxed Write Timing**

表 5-31 lists the switching characteristics of the general-purpose interface.

**表 5-31. EPI General-Purpose Interface Characteristics**

over operating free-air temperature (unless otherwise noted) (see 图 5-23)

| NO. | PARAMETER |                                               | MIN   | TYP | MAX | UNIT |
|-----|-----------|-----------------------------------------------|-------|-----|-----|------|
| E25 | $t_{CK}$  | General-purpose clock period                  | 16.67 |     |     | ns   |
| E26 | $t_{CH}$  | General-purpose clock high time               | 8.33  |     |     | ns   |
| E27 | $t_{CL}$  | General-purpose clock low time                | 8.33  |     |     | ns   |
| E28 | $t_{ISU}$ | Input signal set up time to rising clock edge | 8.50  |     |     | ns   |
| E29 | $t_{IH}$  | Input signal hold time from rising clock edge | 0     |     |     | ns   |
| E30 | $t_{DV}$  | Falling clock edge to output valid            |       |     | 4   | ns   |
| E31 | $t_{DI}$  | Falling clock edge to output invalid          |       |     | 4   | ns   |



NOTE: This figure shows accesses when the FRM50 bit is clear, the FRMCNT field is 0x0, and the WR2CYC bit is clear.

**图 5-23. General-Purpose Mode Read and Write Timing**

表 5-32 lists the switching characteristics of the PSRAM interface.

**表 5-32. EPI PSRAM Interface Characteristics**

over operating free-air temperature (unless otherwise noted) (see 图 5-24 and 图 5-25)

| NO. | PARAMETER                                                                                    | MIN | TYP | MAX | UNIT |
|-----|----------------------------------------------------------------------------------------------|-----|-----|-----|------|
| E33 | $t_{\text{EPICLK}}$ EPI_CLK period                                                           | 20  |     |     | ns   |
| E34 | $t_{\text{RTFT}}$ EPI_CLK rise or fall time                                                  |     |     | 1.8 | ns   |
| E35 | $t_{\text{OV}}$ Falling EPI_CLK to address/write data or control output valid <sup>(1)</sup> | 4.5 |     | 20  | ns   |
| E36 | $t_{\text{HT}}$ Falling EPI_CLK to address/write data or control hold time <sup>(1)</sup>    | 2   |     |     | ns   |
| E37 | $t_{\text{SUP}}$ Read data setup time from EPI_CLK rising                                    |     |     | 9   | ns   |
| E38 | $t_{\text{DH}}$ Read data output hold from EPI_CLK rising                                    | 0   |     |     | ns   |
| E39 | $t_{\text{IRV}}$ iRDY setup time                                                             |     |     | 9   | ns   |
| E40 | $t_{\text{IRH}}$ iRDY hold time                                                              |     |     | 9   | ns   |

(1) Control output includes WRn, RDn, OEn, BSELn, ALE, and CSn.

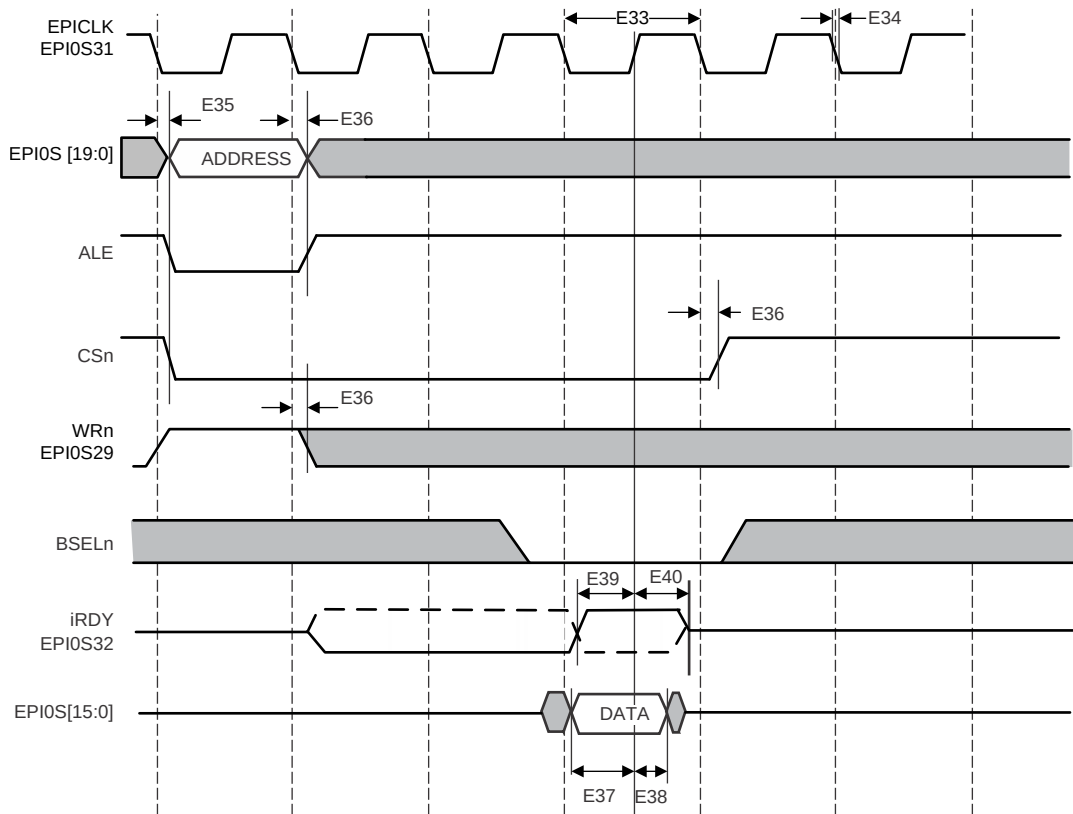


**图 5-24. PSRAM Single Burst Read**

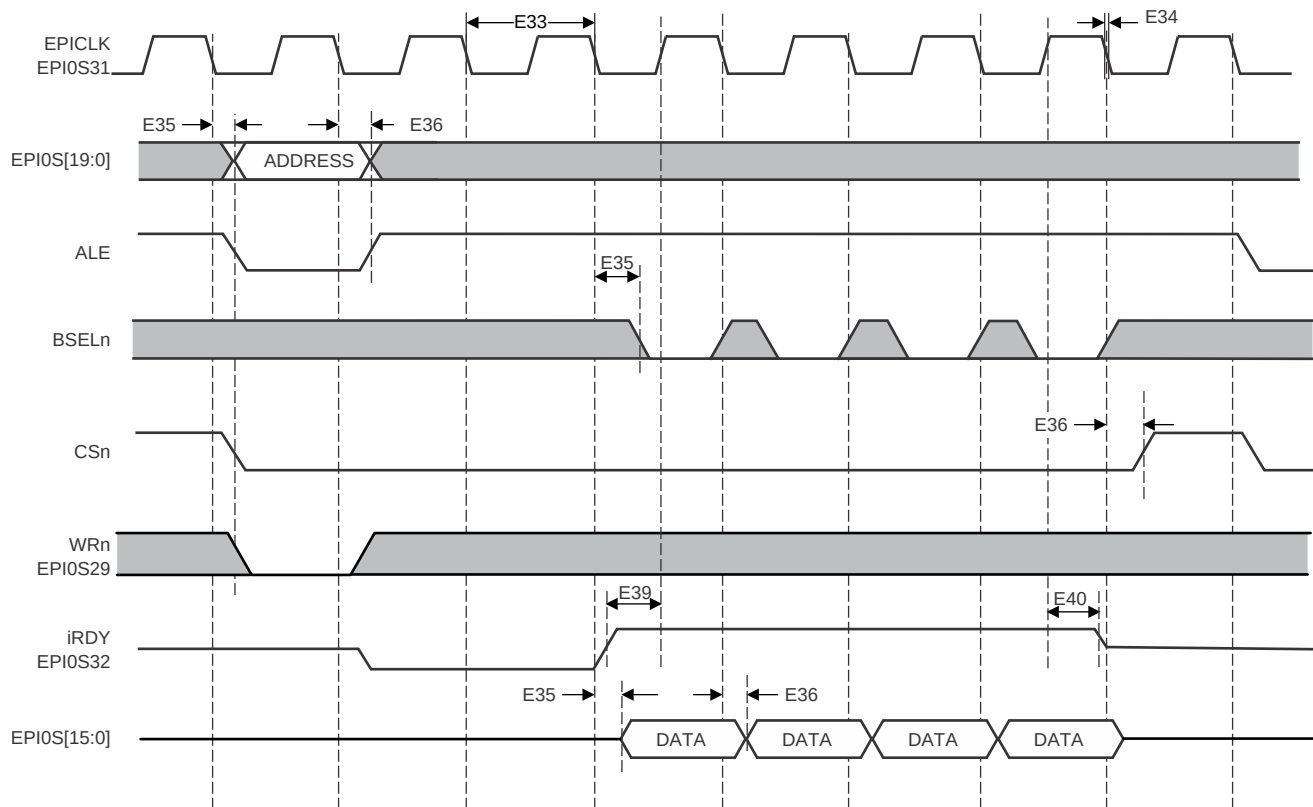


**图 5-25. PSRAM Single Burst Write**

### 5.15.11 Analog-to-Digital Converter (ADC)

表 5-33 lists the electrical characteristics for the ADC at 1 Msps.

表 5-33. Electrical Characteristics for ADC at 1 Msps

$V_{REF+} = 3.3\text{ V}$ ,  $f_{ADC} = 16\text{ MHz}$  (unless otherwise noted)<sup>(1)</sup>

| PARAMETER                               |                                                                                                           | MIN                        | TYP                        | MAX                                       | UNIT |
|-----------------------------------------|-----------------------------------------------------------------------------------------------------------|----------------------------|----------------------------|-------------------------------------------|------|
| <b>Power supply requirements</b>        |                                                                                                           |                            |                            |                                           |      |
| $V_{DDA}$                               | ADC supply voltage                                                                                        | 2.97                       | 3.3                        | 3.63                                      | V    |
| $G_{NDA}$                               | ADC ground voltage                                                                                        |                            | 0                          |                                           | V    |
| <b>VDDA and GNDA voltage reference</b>  |                                                                                                           |                            |                            |                                           |      |
| $C_{REF}$                               | Voltage reference decoupling capacitance                                                                  |                            | 1.0 // 0.01 <sup>(2)</sup> |                                           | μF   |
| <b>External voltage reference input</b> |                                                                                                           |                            |                            |                                           |      |
| $V_{REFA+}$                             | Positive external voltage reference for ADC, when VREF field in the ADCCTL register is 0x1 <sup>(3)</sup> | 2.4                        | $V_{DDA}$                  | $V_{DDA}$                                 | V    |
| $V_{REFA-}$                             | Negative external voltage reference for ADC, when VREF field in the ADCCTL register is 0x1 <sup>(3)</sup> | $G_{NDA}$                  | $G_{NDA}$                  | 0.3                                       | V    |
| $I_{VREF}$                              | Current on VREF+ input, using external $V_{REF+} = 3.3\text{ V}$                                          |                            | 330.5                      | 440                                       | μA   |
| $I_{LVREF}$                             | DC leakage current on VREF+ input when external VREF disabled                                             |                            |                            | 2.0                                       | μA   |
| $C_{REF}$                               | External reference decoupling capacitance <sup>(3)</sup>                                                  |                            | 1.0 // 0.01 <sup>(2)</sup> |                                           | μF   |
| <b>Analog input</b>                     |                                                                                                           |                            |                            |                                           |      |
| $V_{ADCIN}$                             | Single-ended, full-scale analog input voltage, internal reference <sup>(4) (5)</sup>                      | 0                          |                            | $V_{DDA}$                                 | V    |
|                                         | Differential, full-scale analog input voltage, internal reference <sup>(4)(6)</sup>                       | $-V_{DDA}$                 |                            | $V_{DDA}$                                 |      |
|                                         | Single-ended, full-scale analog input voltage, external reference <sup>(3) (5)</sup>                      | $V_{REFA-}$                |                            | $V_{REFA+}$                               |      |
|                                         | Differential, full-scale analog input voltage, external reference <sup>(3)(7)</sup>                       | $-(V_{REFA+} - V_{REFA-})$ |                            | $V_{REFA+} - V_{REFA-}$                   |      |
| $V_{INCM}$                              | Input common-mode voltage, differential mode <sup>(8)</sup>                                               |                            |                            | $[(V_{REFA+} + V_{REFA-}) / 2] \pm 0.025$ | V    |
| $I_L$                                   | ADC input leakage current <sup>(9)</sup>                                                                  |                            |                            | 2.0                                       | μA   |
| $R_{ADC}$                               | ADC equivalent input resistance <sup>(9)</sup>                                                            |                            |                            | 2.5                                       | kΩ   |
| $C_{ADC}$                               | ADC equivalent input capacitance <sup>(9)</sup>                                                           |                            |                            | 10                                        | pF   |
| $R_S$                                   | Analog source resistance <sup>(9)</sup>                                                                   |                            |                            | 500                                       | Ω    |
| <b>Sampling dynamics</b>                |                                                                                                           |                            |                            |                                           |      |
| $f_{ADC}$                               | ADC conversion clock frequency <sup>(10)</sup>                                                            |                            | 16                         |                                           | MHz  |
| $f_{CONV}$                              | ADC conversion rate                                                                                       |                            | 1                          |                                           | Msps |
| $t_S$                                   | ADC sample time                                                                                           |                            | 250                        |                                           | ns   |
| $t_C$                                   | ADC conversion time <sup>(11)</sup>                                                                       |                            | 1                          |                                           | μs   |

- (1) Best design practices suggest placing static or quiet digital I/O signals adjacent to sensitive analog inputs to reduce capacitive coupling and crosstalk. Unexpected results can occur if a switching digital I/O is placed adjacent to an ADC input channel or voltage reference input. In addition, analog signals that are adjacent to ADC input channels or reference inputs must meet the  $R_{ADC}$  equivalent input resistance given in this table and must be band-limited to 100 kHz or lower.
- (2) Two capacitors in parallel. These capacitors should be as close to the die as possible.
- (3) Assumes external filtering network between  $V_{REFA+}$  and  $V_{REFA-}$  as shown in 图 5-26. External reference noise level must be under 12-bit (–74 dB) full-scale input, over input bandwidth, measured at  $V_{REFA+} - V_{REFA-}$ .
- (4) Internal reference is connected directly between  $V_{DDA}$  and  $G_{NDA}$  ( $V_{REFi} = V_{DDA} - G_{NDA}$ ). In this mode,  $E_O$ ,  $E_G$ ,  $E_T$ , and dynamic specifications are adversely affected due to internal voltage drop and noise on  $V_{DDA}$  and  $G_{NDA}$ . Internal reference voltage is selected when VREF field in the ADCCTL register is 0x0.
- (5)  $V_{ADCIN} = V_{INP} - V_{INN}$
- (6) With signal common-mode voltage as  $V_{DDA} / 2$ .
- (7) With signal common-mode voltage as  $V_{REF+} + G_{NDA}$ .
- (8) This parameter is defined as the average of the differential inputs.
- (9) As shown in 图 5-27,  $R_{ADC}$  is the total equivalent resistance in the input line all the way up to the sampling node at the input of the ADC.
- (10) See 表 5-14 for full ADC clock frequency specification.
- (11) ADC conversion time ( $t_C$ ) includes the ADC sample time ( $t_S$ ).

**表 5-33. Electrical Characteristics for ADC at 1 Msps (continued)**
 $V_{REF+} = 3.3\text{ V}$ ,  $f_{ADC} = 16\text{ MHz}$  (unless otherwise noted)<sup>(1)</sup>

| PARAMETER                                                                    |                                                                                                               | MIN | TYP   | MAX                       | UNIT             |
|------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------|-----|-------|---------------------------|------------------|
| $t_{LT}$                                                                     | Latency from trigger to start of conversion                                                                   |     | 2     |                           | ADC clock cycles |
| <b>System performance when using external reference</b> <sup>(12) (13)</sup> |                                                                                                               |     |       |                           |                  |
| N                                                                            | Resolution                                                                                                    |     | 12    |                           | bits             |
| INL                                                                          | Integral nonlinearity error, over full input range                                                            |     | ±1.5  | ±3.0                      | LSB              |
| DNL                                                                          | Differential nonlinearity error, over full input range                                                        |     | ±0.8  | +2.0/–1.0 <sup>(14)</sup> | LSB              |
| $E_O$                                                                        | Offset error                                                                                                  |     | ±1.0  | ±3.0                      | LSB              |
| $E_G$                                                                        | Gain error <sup>(15)</sup>                                                                                    |     | ±2.0  | ±3.0                      | LSB              |
| $E_T$                                                                        | Total unadjusted error, over full input range <sup>(16)</sup>                                                 |     | ±2.5  | ±4.0                      | LSB              |
| <b>System performance when using internal reference</b>                      |                                                                                                               |     |       |                           |                  |
| N                                                                            | Resolution                                                                                                    |     | 12    |                           | bits             |
| INL                                                                          | Integral nonlinearity error, over full input range                                                            |     | ±1.5  | ±3.0                      | LSB              |
| DNL                                                                          | Differential nonlinearity error, over full input range                                                        |     | ±0.8  | +2.0/–1.0 <sup>(14)</sup> | LSB              |
| $E_O$                                                                        | Offset error                                                                                                  |     | ±5.0  | ±15.0                     | LSB              |
| $E_G$                                                                        | Gain error <sup>(15)</sup>                                                                                    |     | ±10.0 | ±30.0                     | LSB              |
| $E_T$                                                                        | Total unadjusted error, over full input range <sup>(16)</sup>                                                 |     | ±10.0 | ±30.0                     | LSB              |
| <b>Dynamic characteristics</b> <sup>(12) (17)</sup>                          |                                                                                                               |     |       |                           |                  |
| $SNR_D$                                                                      | Signal-to-noise-ratio, Differential input, $V_{ADCIN}$ : –20 dB FS, 1 kHz <sup>(18)</sup>                     | 70  | 72    |                           | dB               |
| $SDR_D$                                                                      | Signal-to-distortion ratio, Differential input, $V_{ADCIN}$ : –3 dB FS, 1 kHz <sup>(18) (19) (20)</sup>       | 72  | 75    |                           | dB               |
| $SNDR_D$                                                                     | Signal-to-Noise+Distortion ratio, Differential input, $V_{ADCIN}$ : –3 dB FS, 1 kHz <sup>(18) (21) (22)</sup> | 68  | 70    |                           | dB               |
| $SNR_S$                                                                      | Signal-to-noise-ratio, Single-ended input, $V_{ADCIN}$ : –20 dB FS, 1 kHz <sup>(23)</sup>                     | 60  | 65    |                           | dB               |
| $SDR_S$                                                                      | Signal-to-distortion ratio, Single-ended input, $V_{ADCIN}$ : –3 dB FS, 1 kHz <sup>(19) (20)</sup>            | 70  | 72    |                           | dB               |
| $SNDR_S$                                                                     | Signal-to-Noise+Distortion ratio, Single-ended input, $V_{ADCIN}$ : –3 dB FS, 1 kHz <sup>(23) (21) (22)</sup> | 60  | 63    |                           | dB               |
| <b>Temperature sensor</b>                                                    |                                                                                                               |     |       |                           |                  |
| $V_{TSENS}$                                                                  | Temperature sensor voltage, junction temperature 25°C                                                         |     | 1.633 |                           | V                |
| $S_{TSENS}$                                                                  | Temperature sensor slope at: –40°C to 105°C ambient (extended temperature part)                               |     | –13.3 |                           | mV/°C            |

(12) A low-noise environment is assumed to obtain values close to specifications. The board must have good ground isolation between analog and digital grounds and a clean reference voltage. The input signal must be band-limited to Nyquist bandwidth. No antialiasing filter is provided internally.

(13) ADC static measurements taken by averaging over several samples. At least 20-sample averaging is assumed to obtain expected typical or maximum specification values.

(14) 12-bit DNL

(15) Gain error is measured at maximum code after compensating for offset. Gain error is equivalent to the full-scale error. It can be given in % of slope error, or in LSB, as done here.

(16) Total unadjusted error is the maximum error at any one code versus the ideal ADC curve. It includes all other errors (offset error, gain error and INL) at any given ADC code.

(17) ADC dynamic characteristics are measured using low-noise board design, with low-noise reference voltage (< –74-dB noise level in signal bandwidth) and low-noise analog supply voltage. Board noise and ground bouncing couple into the ADC and affect dynamic characteristics. A clean external reference must be used to achieve the listed specifications.

(18) Differential signal with correct common-mode voltage, applied between two ADC inputs.

(19)  $SDR = -THD$  in dB.

(20) For higher-frequency inputs, expect degradation in SDR.

(21)  $SNDR = S/(N+D) = SINAD$  (in dB)

(22) Effective number of bits (ENOB) can be calculated from SNDR:  $ENOB = (SNDR - 1.76) / 6.02$ .

(23) Single-ended inputs are more sensitive to board and trace noise than differential inputs; SNR and SNDR measurements on single-ended inputs are highly dependent on how clean the test setup is. If the input signal is not well isolated on the board, higher noise than specified could be seen at the ADC output.

表 5-33. Electrical Characteristics for ADC at 1 Msps (continued)

 $V_{REF+} = 3.3\text{ V}$ ,  $f_{ADC} = 16\text{ MHz}$  (unless otherwise noted)<sup>(1)</sup>

| PARAMETER   |                                                                                                       | MIN | TYP | MAX | UNIT |
|-------------|-------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| $E_{TSENS}$ | Temperature sensor accuracy <sup>(24)</sup> at:<br>–40°C to 105°C ambient (extended temperature part) |     |     | ±5  | °C   |

(24) This parameter does not include ADC error.

表 5-34 lists the electrical characteristics for the ADC at 2 Msps.

**表 5-34. Electrical Characteristics for ADC at 2 Msps**

$V_{REF+} = 3.3\text{ V}$ ,  $f_{ADC} = 32\text{ MHz}$ , over operating free-air temperature (unless otherwise noted) (see 图 5-26 and 图 5-27)<sup>(1)</sup>

| PARAMETER                        |                                                                                                           | MIN                                         | TYP              | MAX                                                     | UNIT             |
|----------------------------------|-----------------------------------------------------------------------------------------------------------|---------------------------------------------|------------------|---------------------------------------------------------|------------------|
| Power supply requirements        |                                                                                                           |                                             |                  |                                                         |                  |
| V <sub>DDA</sub>                 | ADC supply voltage                                                                                        | 2.97                                        | 3.3              | 3.63                                                    | V                |
| GNDA                             | ADC ground voltage                                                                                        |                                             | 0                |                                                         | V                |
| VDDA and GNDA voltage reference  |                                                                                                           |                                             |                  |                                                         |                  |
| C <sub>REF</sub>                 | Voltage reference decoupling capacitance                                                                  | 1.0 // 0.01 <sup>(2)</sup>                  |                  |                                                         | μF               |
| External voltage reference input |                                                                                                           |                                             |                  |                                                         |                  |
| V <sub>REFA+</sub>               | Positive external voltage reference for ADC, when VREF field in the ADCCTL register is 0x1 <sup>(3)</sup> | 2.4                                         | V <sub>DDA</sub> | V <sub>DDA</sub>                                        | V                |
| V <sub>REFA-</sub>               | Negative external voltage reference for ADC, when VREF field in the ADCCTL register is 0x1 <sup>(3)</sup> | GNDA                                        | GNDA             | 0.3                                                     | V                |
| I <sub>VREF</sub>                | Current on VREF+ input, using external V <sub>REF+</sub> = 3.3 V                                          |                                             | 330.5            | 440                                                     | μA               |
| I <sub>LVREF</sub>               | DC leakage current on VREF+ input when external VREF disabled                                             |                                             |                  | 2.0                                                     | μA               |
| C <sub>REF</sub>                 | External reference decoupling capacitance <sup>(3)</sup>                                                  | 1.0 // 0.01 <sup>(2)</sup>                  |                  |                                                         | μF               |
| Analog input                     |                                                                                                           |                                             |                  |                                                         |                  |
| V <sub>ADCIN</sub>               | Single-ended, full-scale analog input voltage, internal reference <sup>(4)(5)</sup>                       | 0                                           |                  | V <sub>DDA</sub>                                        | V                |
|                                  | Differential, full-scale analog input voltage, internal reference <sup>(4)(6)</sup>                       | −V <sub>DDA</sub>                           |                  | V <sub>DDA</sub>                                        |                  |
|                                  | Single-ended, full-scale analog input voltage, external reference <sup>(3)(5)</sup>                       | V <sub>REFA-</sub>                          |                  | V <sub>REFA+</sub>                                      |                  |
|                                  | Differential, full-scale analog input voltage, external reference <sup>(3)(7)</sup>                       | −(V <sub>REFA+</sub> − V <sub>REFA-</sub> ) |                  | V <sub>REFA+</sub> − V <sub>REFA-</sub>                 |                  |
| VIN <sub>CM</sub>                | Input common-mode voltage, differential mode <sup>(8)</sup>                                               |                                             |                  | [(V <sub>REFA+</sub> + V <sub>REFA-</sub> ) / 2] ±0.025 | V                |
| I <sub>L</sub>                   | ADC input leakage current <sup>(9)</sup>                                                                  |                                             |                  | 2.0                                                     | μA               |
| R <sub>ADC</sub>                 | ADC equivalent input resistance <sup>(9)</sup>                                                            |                                             |                  | 2.5                                                     | kΩ               |
| C <sub>ADC</sub>                 | ADC equivalent input capacitance <sup>(9)</sup>                                                           |                                             |                  | 10                                                      | pF               |
| R <sub>S</sub>                   | Analog source resistance <sup>(9)</sup>                                                                   |                                             |                  | 250                                                     | Ω                |
| Sampling dynamics                |                                                                                                           |                                             |                  |                                                         |                  |
| f <sub>ADC</sub>                 | ADC conversion clock frequency <sup>(10)</sup>                                                            |                                             | 32               |                                                         | MHz              |
| f <sub>CONV</sub>                | ADC conversion rate                                                                                       |                                             |                  | 2                                                       | Msps             |
| t <sub>S</sub>                   | ADC sample time                                                                                           |                                             | 125              |                                                         | ns               |
| t <sub>C</sub>                   | ADC conversion time <sup>(11)</sup>                                                                       |                                             | 0.5              |                                                         | μs               |
| t <sub>LT</sub>                  | Latency from trigger to start of conversion                                                               |                                             | 2                |                                                         | ADC clock cycles |

- (1) Best design practices suggest placing static or quiet digital I/O signals adjacent to sensitive analog inputs to reduce capacitive coupling and crosstalk. Unexpected results can occur if a switching digital I/O is placed adjacent to an ADC input channel or voltage reference input. In addition, analog signals configured adjacent to ADC input channels or reference inputs must meet the  $R_{ADC}$  equivalent input resistance given in this table and must be band-limited to 100 kHz or lower.
- (2) Two capacitors in parallel. These capacitors should be as close to the die as possible.
- (3) Assumes external filtering network between  $V_{REFA+}$  and  $V_{REFA-}$  as shown in 图 5-26. External reference noise level must be under 12-bit (–74-dB) full scale input, over input bandwidth, measured at  $V_{REFA+} - V_{REFA-}$ .
- (4) Internal reference is connected directly between  $V_{DDA}$  and  $V_{GNDA}$  ( $V_{REFI} = V_{DDA} - V_{GNDA}$ ). In this mode,  $E_O$ ,  $E_G$ ,  $E_T$ , and dynamic specifications are adversely affected due to internal voltage drop and noise on  $V_{DDA}$  and  $G_{NDA}$ . Internal reference voltage is selected when VREF field in the ADCCTL register is 0x0.
- (5)  $V_{ADCIN} = V_{INP} - V_{INN}$
- (6) With signal common-mode voltage as  $V_{DDA} / 2$ .
- (7) With signal common-mode voltage as  $(V_{REF+} + V_{REF-}) / 2$ .
- (8) This parameter is defined as the average of the differential inputs.
- (9) As shown in 图 5-27,  $R_{ADC}$  is the total equivalent resistance in the input line all the way up to the sampling node at the input of the ADC.
- (10) See 表 5-14 for full ADC clock frequency specification.
- (11) ADC conversion time ( $t_C$ ) includes the ADC sample time ( $t_S$ ).

表 5-34. Electrical Characteristics for ADC at 2 Msps (continued)

$V_{REF+} = 3.3\text{ V}$ ,  $f_{ADC} = 32\text{ MHz}$ , over operating free-air temperature (unless otherwise noted) (see 图 5-26 and 图 5-27)<sup>(1)</sup>

| PARAMETER                                                                    |                                                                                                                      | MIN | TYP   | MAX                       | UNIT |
|------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------|-----|-------|---------------------------|------|
| <b>System performance when using external reference</b> <sup>(12) (13)</sup> |                                                                                                                      |     |       |                           |      |
| N                                                                            | Resolution                                                                                                           |     | 12    |                           | bits |
| INL                                                                          | Integral nonlinearity error, over full input range                                                                   |     | ±1.5  | ±3.0                      | LSB  |
| DNL                                                                          | Differential nonlinearity error, over full input range                                                               |     | ±0.8  | +2.0/–1.0 <sup>(14)</sup> | LSB  |
| E <sub>O</sub>                                                               | Offset error                                                                                                         |     | ±1.0  | ±3.0                      | LSB  |
| E <sub>G</sub>                                                               | Gain error <sup>(15)</sup>                                                                                           |     | ±2.0  | ±3.0                      | LSB  |
| E <sub>T</sub>                                                               | Total unadjusted error, over full input range <sup>(16)</sup>                                                        |     | ±2.5  | ±4.0                      | LSB  |
| <b>System performance when using internal reference</b>                      |                                                                                                                      |     |       |                           |      |
| N                                                                            | Resolution                                                                                                           |     | 12    |                           | bits |
| INL                                                                          | Integral nonlinearity error, over full input range                                                                   |     | ±1.5  | ±3.0                      | LSB  |
| DNL                                                                          | Differential nonlinearity error, over full input range                                                               |     | ±0.8  | +2.0/–1.0 <sup>(14)</sup> | LSB  |
| E <sub>O</sub>                                                               | Offset error                                                                                                         |     | ±5.0  | ±15.0                     | LSB  |
| E <sub>G</sub>                                                               | Gain error <sup>(15)</sup>                                                                                           |     | ±10.0 | ±30.0                     | LSB  |
| E <sub>T</sub>                                                               | Total unadjusted error, over full input range <sup>(16)</sup>                                                        |     | ±10.0 | ±30.0                     | LSB  |
| <b>Dynamic characteristics</b> <sup>(17) (18)</sup>                          |                                                                                                                      |     |       |                           |      |
| SNR <sub>D</sub>                                                             | Signal-to-noise-ratio, differential input, V <sub>ADCIN</sub> : –20 dB FS, 1 kHz <sup>(19)</sup>                     | 68  | 72    |                           | dB   |
| SDR <sub>D</sub>                                                             | Signal-to-distortion ratio, differential input, V <sub>ADCIN</sub> : –3 dB FS, 1 kHz <sup>(19) (20) (21)</sup>       | 70  | 75    |                           | dB   |
| SNDR <sub>D</sub>                                                            | Signal-to-noise+distortion ratio, differential input, V <sub>ADCIN</sub> : –3 dB FS, 1 kHz <sup>(19) (22) (23)</sup> | 65  | 70    |                           | dB   |
| SNR <sub>S</sub>                                                             | Signal-to-noise-ratio, single-ended input, V <sub>ADCIN</sub> : –20 dB FS, 1 kHz <sup>(24)</sup>                     | 58  | 65    |                           | dB   |
| SDR <sub>S</sub>                                                             | Signal-to-distortion ratio, single-ended input, V <sub>ADCIN</sub> : –3 dB FS, 1 kHz <sup>(20) (21)</sup>            | 68  | 72    |                           | dB   |
| SNDR <sub>S</sub>                                                            | Signal-to-noise+distortion ratio, single-ended input, V <sub>ADCIN</sub> : –3 dB FS, 1 kHz <sup>(24) (22) (23)</sup> | 58  | 63    |                           | dB   |

(12) A low-noise environment is assumed to obtain values close to specifications. The board must have good ground isolation between analog and digital grounds, a clean reference voltage is assumed, and input signal must be bandlimited to Nyquist bandwidth. No antialiasing filter is provided internally.

(13) ADC static measurements taken by averaging over several samples. At least 20-sample averaging is assumed to obtain expected typical or maximum specification values.

(14) 12-bit DNL

(15) Gain error is measured at maximum code after compensating for offset. Gain error is equivalent to "Full Scale Error." It can be given in % of slope error, or in LSB, as done here.

(16) Total Unadjusted Error is the maximum error at any one code versus the ideal ADC curve. It includes all other errors (offset error, gain error and INL) at any given ADC code.

(17) A low noise environment is assumed to obtain values close to spec. The board must have good ground isolation between analog and digital grounds and a clean reference voltage. The input signal must be band-limited to Nyquist bandwidth. No antialiasing filter is provided internally.

(18) ADC dynamic characteristics are measured using low-noise board design, with low-noise reference voltage (< –74 dB noise level in signal BW) and low-noise analog supply voltage. Board noise and ground bouncing couple into the ADC and affect dynamic characteristics. Clean external reference must be used to achieve the listed specifications.

(19) Differential signal with correct common-mode voltage, applied between two ADC inputs.

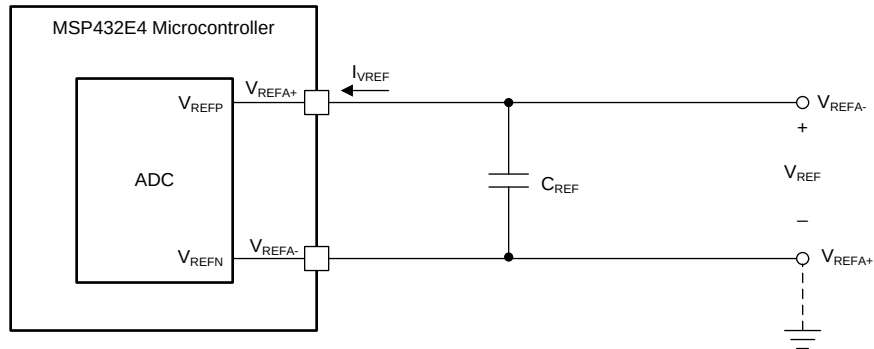
(20) SDR = –THD in dB.

(21) For higher-frequency inputs, expect degradation in SDR.

(22) SNDR = S/(N+D) = SINAD (in dB)

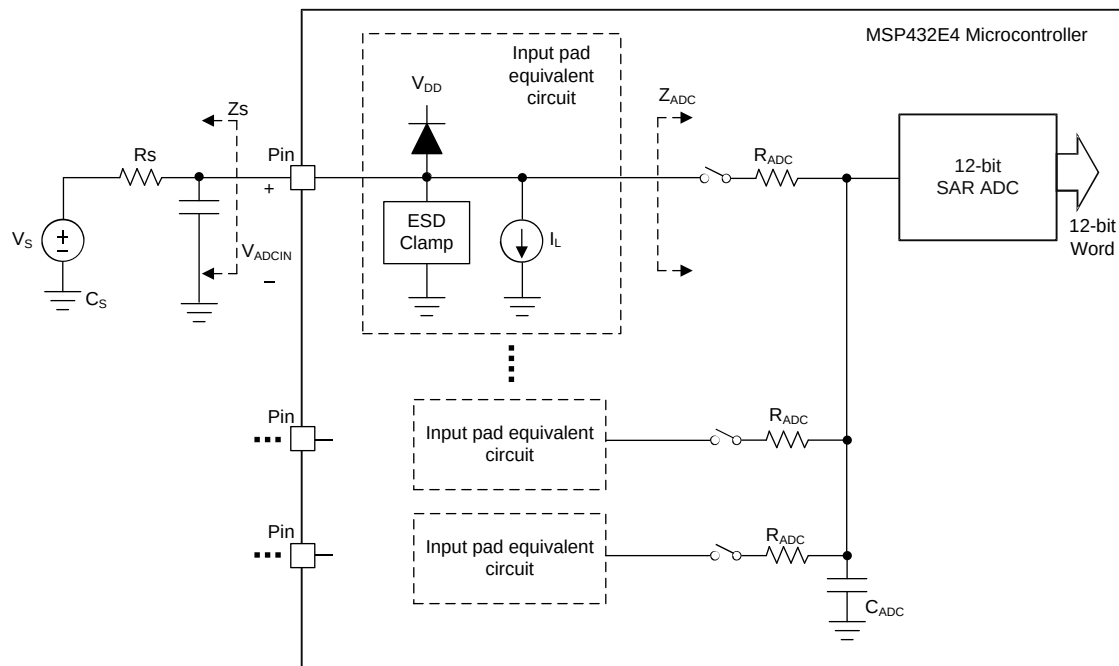
(23) Effective number of bits (ENOB) can be calculated from SNDR: ENOB = (SNDR – 1.76) / 6.02.

(24) Single-ended inputs are more sensitive to board and trace noise than differential inputs; SNR and SNDR measurements on single-ended inputs are highly dependent on how clean the test setup is. If the input signal is not well isolated on the board, higher noise than specified could be seen at the ADC output.



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图 5-26. ADC External Reference Filtering



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图 5-27. ADC Input Equivalency

### 5.15.12 Synchronous Serial Interface (SSI)

表 5-35. SSI Characteristics

over operating free-air temperature (unless otherwise noted) (see 图 5-28, 图 5-29, and 图 5-30)

| NO. | PARAMETER       |                                                                              | MIN                      | TYP   | MAX                  | UNIT |
|-----|-----------------|------------------------------------------------------------------------------|--------------------------|-------|----------------------|------|
| S1  | $t_{CLK\_PER}$  | SSIClk cycle time                                                            | As master <sup>(1)</sup> | 16.67 |                      | ns   |
|     |                 |                                                                              | As slave <sup>(2)</sup>  | 100   |                      |      |
| S2  | $t_{CLK\_HIGH}$ | SSIClk high time                                                             | As master                | 8.33  |                      | ns   |
|     |                 |                                                                              | As slave                 | 50    |                      |      |
| S3  | $t_{CLK\_LOW}$  | SSIClk low time                                                              | As master                | 8.33  |                      | ns   |
|     |                 |                                                                              | As slave                 | 50    |                      |      |
| S4  | $t_{CLKR}$      | SSIClk rise time <sup>(3)</sup>                                              | 1.25                     |       |                      | ns   |
| S5  | $t_{CLKF}$      | SSIClk fall time <sup>(3)</sup>                                              | 1.25                     |       |                      | ns   |
| S6  | $t_{TXDMOV}$    | Master mode: master Tx data output (to slave) valid time from edge of SSIClk |                          |       | 4.00                 | ns   |
| S7  | $t_{TXDMOH}$    | Master mode: master Tx data output (to slave) hold time after next SSIClk    | 0.60                     |       |                      | ns   |
| S8  | $t_{RXDMS}$     | Master mode: master Rx data In (from slave) setup time                       | 7.89                     |       |                      | ns   |
| S9  | $t_{RXDMH}$     | Master mode: master Rx data In (from slave) hold time                        | 0                        |       |                      | ns   |
| S10 | $t_{TXDSOV}$    | Slave mode: master Tx data output (to master) valid time from edge of SSIClk |                          |       | 47.60 <sup>(4)</sup> | ns   |
| S11 | $t_{TXDSOH}$    | Slave mode: slave Tx data output (to master) hold time from next SSIClk      | 37.4 <sup>(5)</sup>      |       |                      | ns   |
| S13 | $t_{RXDSSU}$    | Slave mode: Rx data in (from master) setup time                              | 0                        |       |                      | ns   |
| S14 | $t_{RXDSH}$     | Slave mode: Rx data in (from master) hold time                               | 37.03 <sup>(6)</sup>     |       |                      | ns   |

(1) In master mode, the system clock must be at least twice as fast as the SSIClk.

(2) In slave mode, the system clock must be at least 12 times faster than the SSIClk.

(3) The delays shown are using 12-mA drive strength.

(4) This MAX value is for the minimum slave mode  $t_{SYSCLK}$  period (8.33 ns). To find the MAX  $t_{TXDSOV}$  value for a larger  $t_{SYSCLK}$ , use the equation:  $4 \times t_{SYSCLK} + 14.25$ .

(5) This MIN value is for the minimum slave mode  $t_{SYSCLK}$  (8.33 ns). To find the MIN  $t_{TXDSOH}$  value for a larger  $t_{SYSCLK}$ , use the equation:  $4 \times t_{SYSCLK} + 4.08$ .

(6) This MIN value is for the minimum slave mode  $t_{SYSCLK}$  (8.33 ns). To find the MIN  $t_{TXDSH}$  value for a larger  $t_{SYSCLK}$ , use the equation:  $4 \times t_{SYSCLK} + 3.70$ .

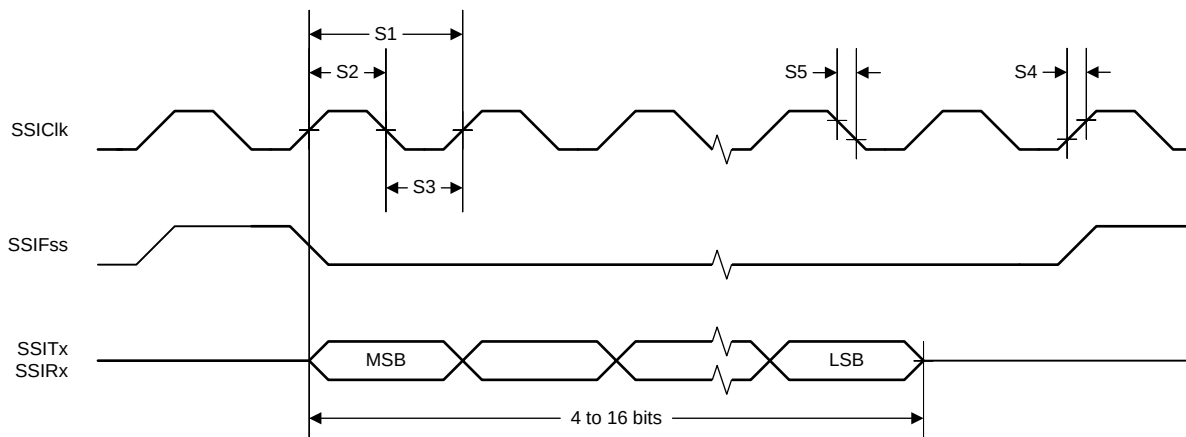


图 5-28. SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement

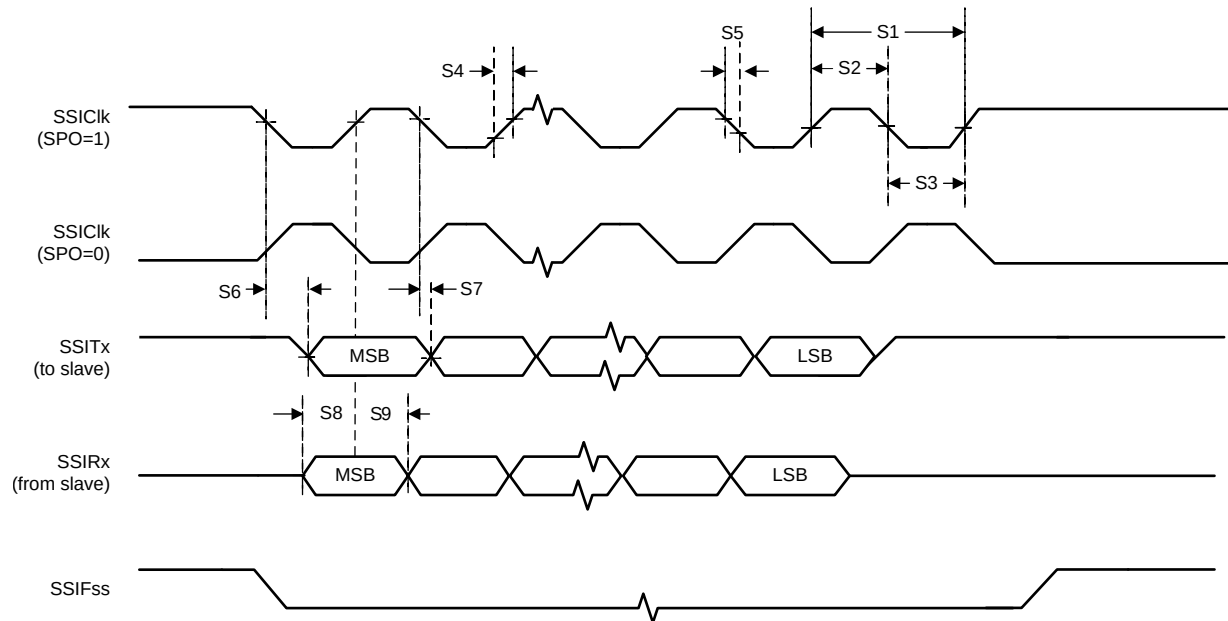


图 5-29. Master Mode SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1

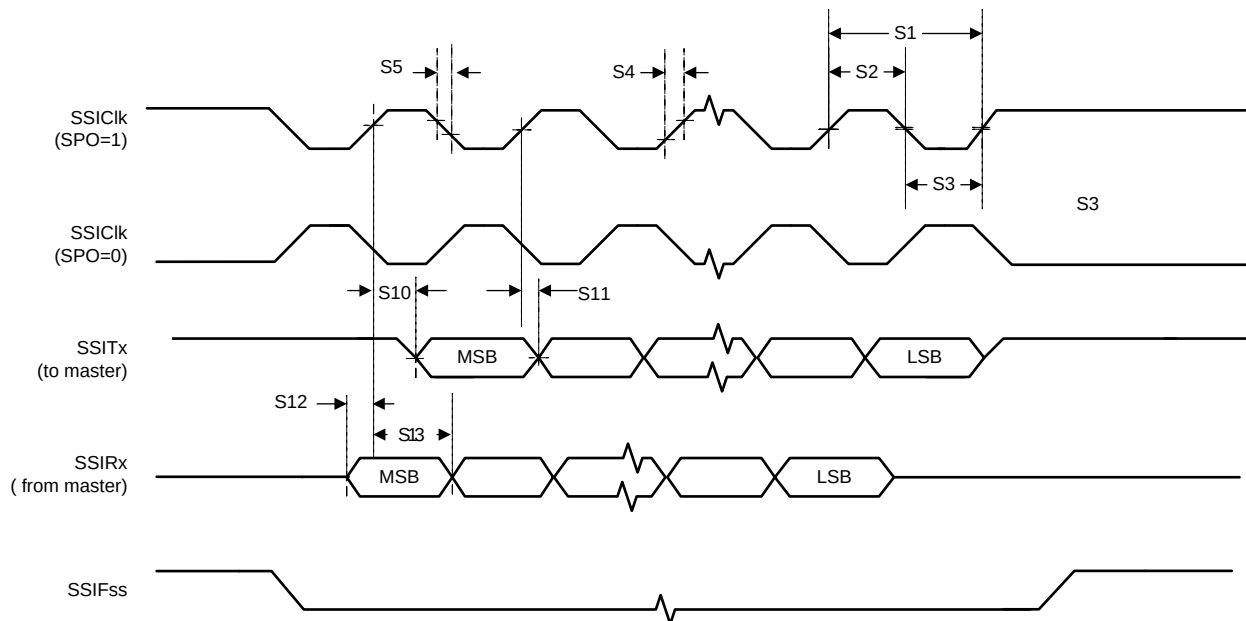


图 5-30. Slave Mode SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1

表 5-36 lists the characteristics for Bi-SSI and Quad-SSI.

**表 5-36. Bi- and Quad-SSI Characteristics<sup>(1)</sup>**

over operating free-air temperature (unless otherwise noted)

| NO. | PARAMETER             |                                                                                     | MIN   | TYP | MAX  | UNIT |
|-----|-----------------------|-------------------------------------------------------------------------------------|-------|-----|------|------|
| S15 | t <sub>CLK_PER</sub>  | SSIClk cycle time, as master <sup>(2)</sup>                                         | 16.67 |     |      | ns   |
| S16 | t <sub>CLK_HIGH</sub> | SSIClk high time, as master                                                         | 8.33  |     |      | ns   |
| S17 | t <sub>CLK_LOW</sub>  | SSIClk low time, as master                                                          | 8.33  |     |      | ns   |
| S18 | t <sub>CLKR</sub>     | SSIClk rise time <sup>(3)</sup>                                                     | 1.25  |     |      | ns   |
| S19 | t <sub>CLKF</sub>     | SSIClk fall time <sup>(3)</sup>                                                     | 1.25  |     |      | ns   |
| S20 | t <sub>TXDMOV</sub>   | Master mode: master SSInXDATn data output (to slave) valid time from edge of SSIClk |       |     | 4.04 | ns   |
| S21 | t <sub>TXDMOH</sub>   | Master mode: master SSInXDATn data output (to slave) hold time after next SSIClk    | 0.60  |     |      | ns   |
| S22 | t <sub>RXDMS</sub>    | Master mode: master SSInXDATn data in (from slave) setup time                       | 5.78  |     |      | ns   |
| S23 | t <sub>RXDMH</sub>    | Master mode: master SSInXDATn data in (from slave) hold time                        | 0     |     |      | ns   |

(1) Parameters S15 to S23 correspond to parameters S1 to S9 in 图 5-28 and 图 5-29.

(2) In master mode, the system clock must be at least twice as fast as the SSIClk.

(3) The delays shown are using 12-mA drive strength.

### 5.15.13 Inter-Integrated Circuit (I<sup>2</sup>C) Interface

表 5-37 lists the characteristics for the I<sup>2</sup>C interface.

表 5-37. I<sup>2</sup>C Characteristics

over operating free-air temperature (unless otherwise noted) (see 图 5-31)

| NO.               | PARAMETER         |                                                                                  | MIN | TYP                 | MAX | UNIT                |
|-------------------|-------------------|----------------------------------------------------------------------------------|-----|---------------------|-----|---------------------|
| I1 <sup>(1)</sup> | t <sub>SCH</sub>  | Start condition hold time                                                        | 36  |                     |     | system clock cycles |
| I2 <sup>(1)</sup> | t <sub>LP</sub>   | Clock low period                                                                 | 36  |                     |     | system clock cycles |
| I3 <sup>(2)</sup> | t <sub>SRT</sub>  | I2CSCL and I2CSDA rise time (V <sub>IL</sub> = 0.5 V to V <sub>IH</sub> = 2.4 V) |     | See <sup>(2)</sup>  |     | ns                  |
| I4                | t <sub>DH</sub>   | Slave Data hold time                                                             |     | 2                   |     | system clock cycles |
|                   |                   | Master                                                                           |     | 7                   |     |                     |
| I5 <sup>(3)</sup> | t <sub>SFT</sub>  | I2CSCL and I2CSDA fall time (V <sub>IH</sub> = 2.4 V to V <sub>IL</sub> = 0.5 V) |     | 9                   | 10  | ns                  |
| I6 <sup>(1)</sup> | t <sub>HT</sub>   | Clock high time                                                                  | 24  |                     |     | system clock cycles |
| I7                | t <sub>DS</sub>   | Data setup time                                                                  | 18  |                     |     | system clock cycles |
| I8 <sup>(1)</sup> | t <sub>SCSR</sub> | Start condition setup time (for repeated start condition only)                   | 36  |                     |     | system clock cycles |
| I9 <sup>(1)</sup> | t <sub>SCS</sub>  | Stop condition setup time                                                        | 24  |                     |     | system clock cycles |
| I10               | t <sub>DV</sub>   | Slave Data valid                                                                 |     | 2                   |     | system clock cycles |
|                   |                   | Master                                                                           |     | (6 × (1 + TPR)) + 1 |     | system clock cycles |

- (1) Values depend on the value programmed into the TPR bit in the I<sup>2</sup>C Master Timer Period (I2CMTPR) register; a TPR programmed for the maximum I2CSCL frequency (TPR = 0x2) results in a minimum output timing listed in this table. The I<sup>2</sup>C interface is designed to scale the actual data transition time to move it to the middle of the I2CSCL low period. The actual position is affected by the value programmed into the TPR; however, the values in this table are minimum values.
- (2) Because I2CSCL and I2CSDA operate as open-drain-type signals, which the controller can only actively drive low, the time I2CSCL or I2CSDA takes to reach a high level depends on external signal capacitance and pullup resistor values.
- (3) Specified at a nominal 50-pF load

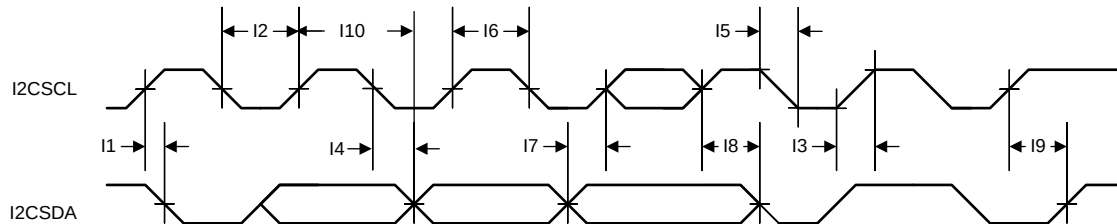


图 5-31. I<sup>2</sup>C Timing

### 5.15.14 Ethernet Controller

#### 5.15.14.1 DC Characteristics

The parameters listed in 表 5-38, with the exception of  $R_{BIAS}$ , apply to transmit pins of the Ethernet PHY, which are generally the EN0TXOP and EN0TXON signals during standard operation but can also be the EN0RXIN and EN0RXIP signals if Auto-MDIX is enabled.

表 5-38. Ethernet PHY DC Characteristics

over operating free-air temperature (unless otherwise noted)

| PARAMETER       |                                                 | MIN  | TYP  | MAX  | UNIT      |
|-----------------|-------------------------------------------------|------|------|------|-----------|
| $R_{BIAS}$      | Value of the pulldown resistor on the RBIAS pin | 4.82 | 4.87 | 4.92 | $k\Omega$ |
| $V_{TPTD\_100}$ | 100M transmit voltage                           | 0.95 | 1    | 1.05 | V         |
| $V_{TPTDSYM}$   | 100M transmit voltage symmetry                  | -2%  |      | 2%   |           |
| $V_{OVRSH}$     | Output overshoot                                |      |      | 5%   |           |
| $V_{TPTD\_10}$  | 10M transmit voltage                            | 2.2  | 2.5  | 2.8  | V         |
| $V_{TH1}$       | 10Base-T Receive threshold                      |      | 200  |      | mV        |

#### 5.15.14.2 Clock Characteristics for Ethernet

表 5-39 lists the specifications of the MOSC 25-MHz crystal.

表 5-39. MOSC 25-MHz Crystal Specification<sup>(1)</sup>

over operating free-air temperature (unless otherwise noted) (see 图 5-32)

| NO. | PARAMETER    |                                                | MIN | TYP | MAX      | UNIT |
|-----|--------------|------------------------------------------------|-----|-----|----------|------|
| N1  | $f_{MOSC25}$ | Frequency                                      |     | 25  |          | MHz  |
|     | $f_{TOL}$    | Frequency tolerance at operational temperature | 0   |     | $\pm 50$ | ppm  |
|     | $f_{STA}$    | Frequency stability at 1-year aging            |     |     | $\pm 5$  | ppm  |

(1) See 表 5-12 for additional MOSC requirements.

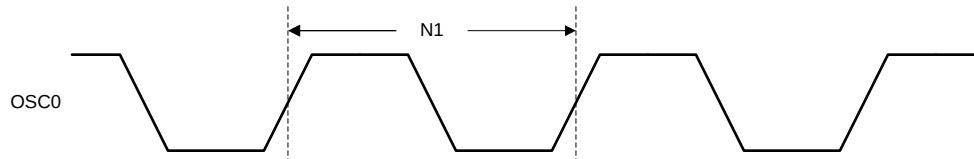


图 5-32. MOSC Crystal Characteristics for Ethernet

表 5-40 lists the specifications of the single-ended 25-MHz oscillator.

**表 5-40. MOSC Single-Ended 25-MHz Oscillator Specification <sup>(1)</sup>**

over operating free-air temperature (unless otherwise noted) (see 图 5-33)

| NO. | PARAMETER |                                                | MIN            | TYP | MAX | UNIT |
|-----|-----------|------------------------------------------------|----------------|-----|-----|------|
| N4  | $f_{OSC}$ | Frequency                                      |                | 25  |     | MHz  |
|     | $f_{TOL}$ | Frequency tolerance at operational temperature | 0              |     | ±50 | ppm  |
|     | $t_{STA}$ | Frequency stability at 1-year aging            |                |     | ±50 | ppm  |
| N5  | $t_{RF}$  | Frequency rise and fall time                   |                |     | 1   | ns   |
|     | $t_j$     | Jitter                                         | Cycle to cycle |     | 50  | ps   |
|     |           |                                                | Over 10 ms     |     | 1   | ns   |
|     | DC        | Duty cycle                                     | 40%            |     | 60% |      |

(1) See 表 5-12 for additional MOSC requirements.

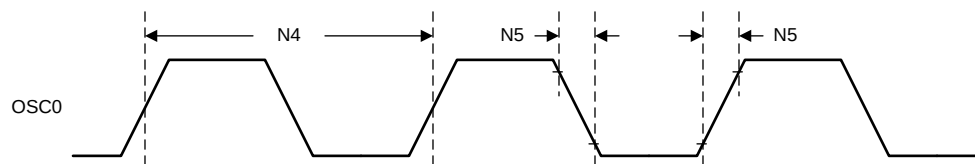


**图 5-33. Single-Ended MOSC Characteristics for Ethernet**

5.15.14.3 AC Characteristics

表 5-41 lists the timing characterists of the enable and reset.

表 5-41. Ethernet Controller Enable and Software Reset Timing

over operating free-air temperature (unless otherwise noted) (see 图 5-34)

| NO. | PARAMETER                                                                                                             | MIN | TYP | MAX | UNIT    |
|-----|-----------------------------------------------------------------------------------------------------------------------|-----|-----|-----|---------|
| N16 | $t_{EN}$ Time from the System Control enable of the PHY to energy on the PMD output pin <sup>(1)</sup> <sup>(2)</sup> | 45  |     |     | $\mu$ s |
| N17 | $t_{SWRST}$ Time from software reset of the PHY to energy on the PMD output pin                                       | 110 |     |     | ns      |

- (1) The PHY is enabled through System Control by setting the P0 bit in the PCEPHY register and the R0 bit in the RCGCPHY register.  
(2) This minimum timing assumes the PHYHOLD bit in the EMACPC register is not set.

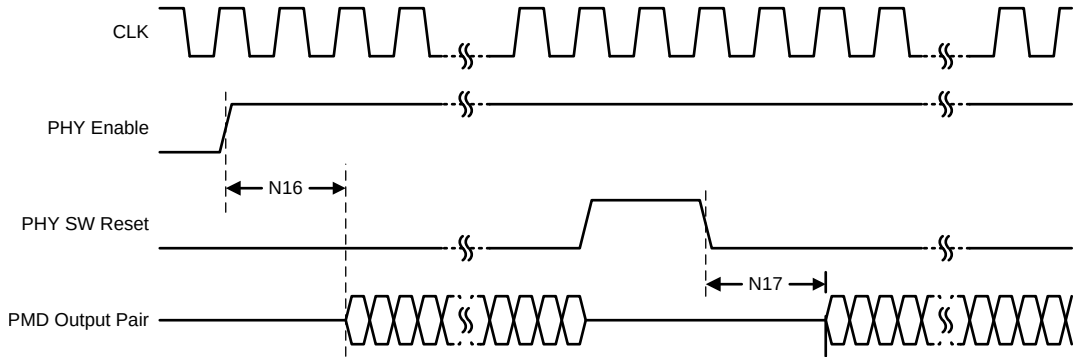


图 5-34. Reset Timing

表 5-42 lists the 100Base-TX transmit timing.

**表 5-42. 100Base-TX Transmit Timing**

over operating free-air temperature (unless otherwise noted) (see 图 5-35)

| NO. | PARAMETER                                                         | MIN | TYP | MAX | UNIT |
|-----|-------------------------------------------------------------------|-----|-----|-----|------|
| N38 | $t_{RF}$ 100-Mbps PMD output pair $t_R$ and $t_F$ <sup>(1)</sup>  | 3   | 4   | 5   | ns   |
|     | $t_{RF\_MM}$ 100-Mbps $t_R$ and $t_F$ symmetry <sup>(2) (3)</sup> |     |     | 500 | ps   |
| N39 | $t_{RF\_JTTR}$ 100-Mbps PMD output pair transmit jitter           |     |     | 1.4 | ns   |

- (1) Rise and fall times taken at 10% and 90% of the +1 or –1 amplitude.  
(2) Normal mismatch is the difference between the maximum and minimum of all rise and fall times  
(3) Choice of Ethernet transformer magnetics can affect this parameter.

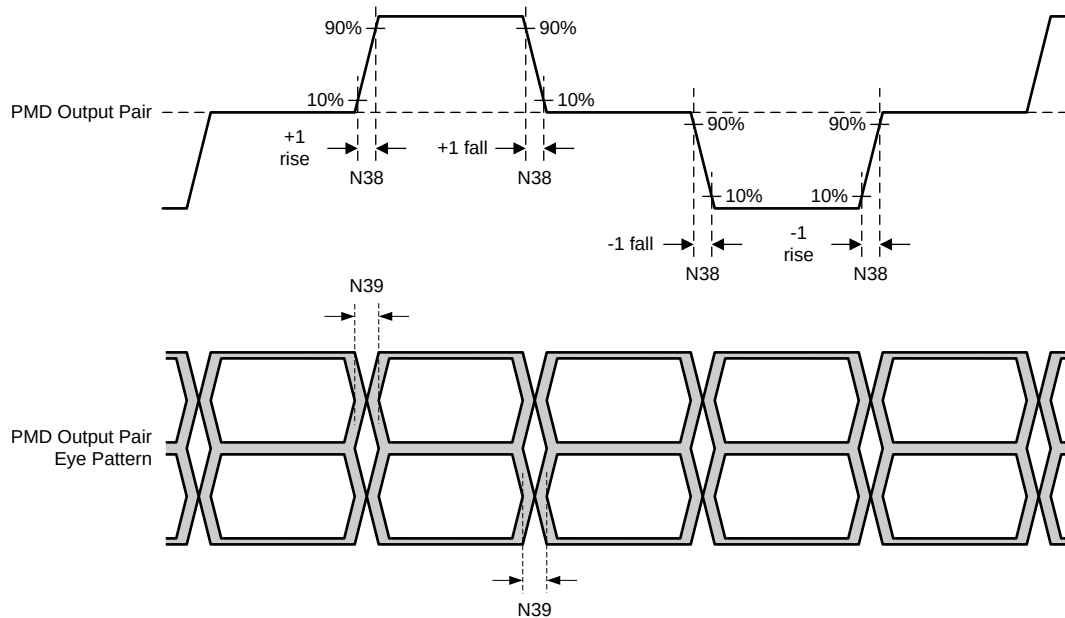


**图 5-35. 100 Base-TX Transmit Timing**

表 5-43 lists the 10Base-T normal link pulse timing.

**表 5-43. 10Base-T Normal Link Pulse Timing**

over operating free-air temperature (unless otherwise noted) (see 图 5-36)

| NO. | PARAMETER                       | MIN | TYP | MAX | UNIT |
|-----|---------------------------------|-----|-----|-----|------|
| N69 | $t_{LP\_PER}$ Link pulse period |     | 76  |     | ms   |
| N70 | $t_{LP\_WID}$ Link pulse width  |     | 100 |     | μs   |

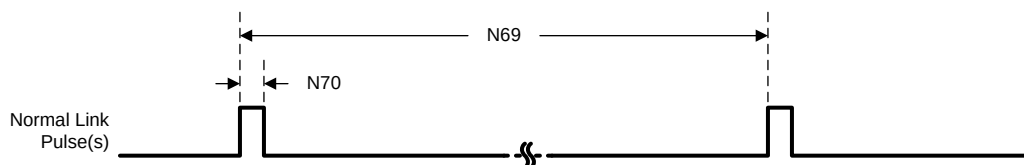


**图 5-36. 10Base-TX Normal Link Pulse Timing**

表 5-44 lists the Auto-Negotiation FLP timing.

表 5-44. Auto-Negotiation Fast Link Pulse (FLP) Timing

over operating free-air temperature (unless otherwise noted) (see 图 5-37)

| NO. | PARAMETER   |                                   | MIN | TYP | MAX | UNIT    |
|-----|-------------|-----------------------------------|-----|-----|-----|---------|
| N72 | $t_{CLKP}$  | Clock pulse to clock pulse period |     | 125 |     | $\mu s$ |
| N73 | $t_{CLKDP}$ | Clock pulse to data pulse period  |     | 62  |     | $\mu s$ |
| N74 | $t_{PUL}$   | Clock, data pulse width           |     | 110 |     | ns      |
| N75 | $t_{BRSTP}$ | FLP burst to flp burst period     |     | 16  |     | ms      |
| N76 | $t_{BRSTW}$ | Burst width                       |     | 2   |     | ms      |

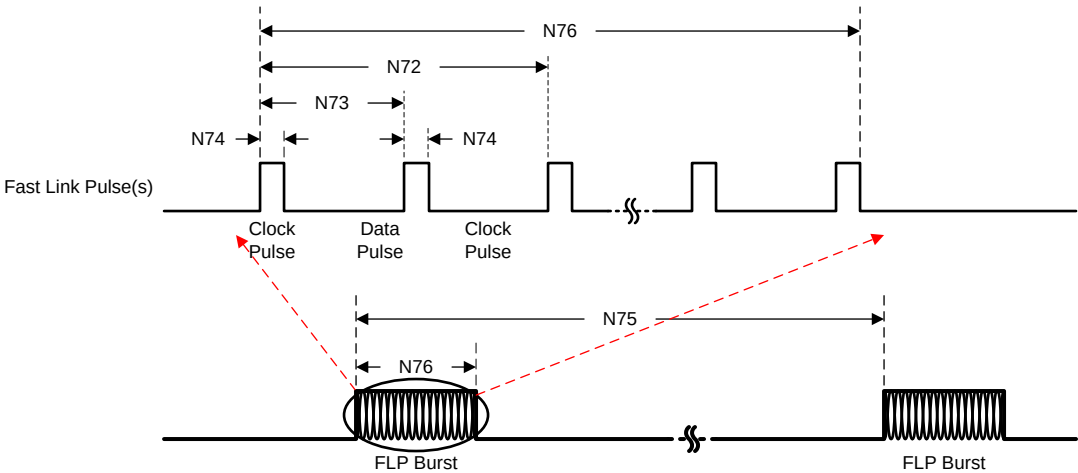


图 5-37. Auto-Negotiation Fast Link Pulse Timing

表 5-45 lists the 100Base-TX signal detect timing.

表 5-45. 100Base-TX Signal Detect Timing

over operating free-air temperature (unless otherwise noted) (see 图 5-38)

| NO. | PARAMETER |                         | MIN | TYP | MAX | UNIT    |
|-----|-----------|-------------------------|-----|-----|-----|---------|
| N79 | $t_{ON}$  | SD internal turnon time |     |     | 100 | $\mu s$ |
| N80 | $t_{OFF}$ | Internal turnoff time   |     |     | 200 | $\mu s$ |

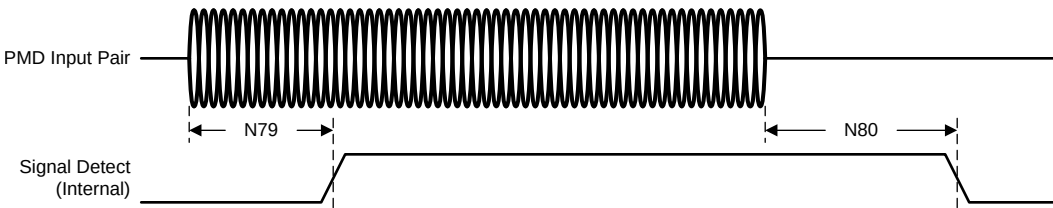


图 5-38. 100Base-TX Signal Detect Timing

### 5.15.15 Universal Serial Bus (USB) Controller

The USB controller electrical specifications are compliant with the Universal Serial Bus Specification Rev 2.0 (full-speed and low-speed support) and the On-The-Go Supplement to the USB 2.0 Specification Rev 1.0. Some components of the USB system are integrated within the microcontroller and specific to the microcontroller design.

注

GPIO pin PB1, which can be configured as the USB0VBUS signal, is the only pin that is 5-V tolerant on the device.

表 5-46 lists the timing characteristics of the ULPI interface.

表 5-46. ULPI Interface Timing

over operating free-air temperature (unless otherwise noted) (see 图 5-39)

| NO.                                                            | PARAMETER        |                                          | MIN | TYP | MAX  | UNIT |
|----------------------------------------------------------------|------------------|------------------------------------------|-----|-----|------|------|
| Timings with respect to external clock source input to USB0CLK |                  |                                          |     |     |      |      |
| U1                                                             | t <sub>SUC</sub> | Setup time (control in) USB0DIR, USB0NXT | 4.8 |     |      | ns   |
| U2                                                             | t <sub>SUD</sub> | Setup time (data in) USB0Dn              | 3.5 |     |      | ns   |
| U3                                                             | t <sub>HTC</sub> | Hold time (control in) USB0DIR, USB0NXT  | 0   |     |      | ns   |
| U4                                                             | t <sub>HTD</sub> | Hold time (data in) USB0Dn               | 0   |     |      | ns   |
| U5                                                             | t <sub>ODC</sub> | Output delay (control out) USB0STP       | 3.7 |     | 9.5  | ns   |
| U6                                                             | t <sub>ODD</sub> | Output delay (data out) USB0Dn           | 3.7 |     | 9.5  | ns   |
| Timings with USB0CLK as clock output                           |                  |                                          |     |     |      |      |
| U1                                                             | t <sub>SUC</sub> | Setup time (control in) USB0DIR, USB0NXT | 6.0 |     |      | ns   |
| U2                                                             | t <sub>SUD</sub> | Setup time (data in) USB0Dn              | 4.6 |     |      | ns   |
| U3                                                             | t <sub>HTC</sub> | Hold time (control in) USB0DIR, USB0NXT  | 0   |     |      | ns   |
| U4                                                             | t <sub>HTD</sub> | Hold time (data in) USB0Dn               | 0   |     |      | ns   |
| U5                                                             | t <sub>ODC</sub> | Output delay (control out) USB0STP       | 4.0 |     | 10.6 | ns   |
| U6                                                             | t <sub>ODD</sub> | Output delay (data out) USB0Dn           | 4.0 |     | 10.6 | ns   |

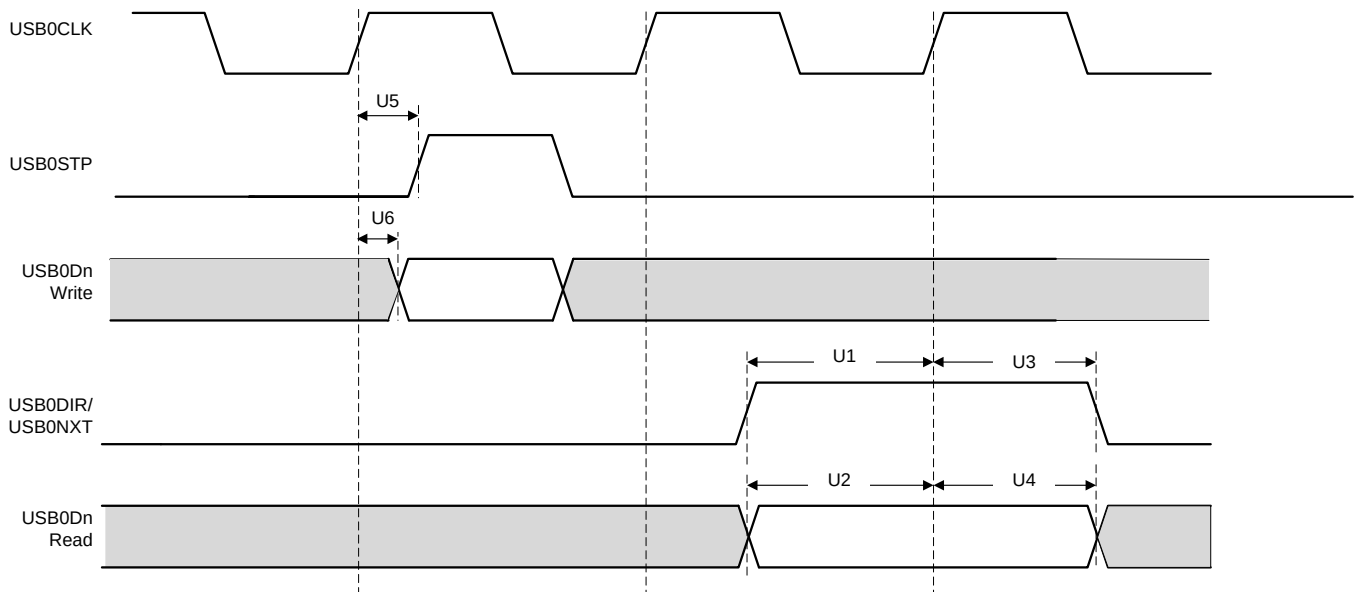


图 5-39. ULPI Interface Timing Diagram

### 5.15.16 Analog Comparator

表 5-47 lists the characteristics of the comparator.

**表 5-47. Analog Comparator Characteristics**

over operating free-air temperature (unless otherwise noted) <sup>(1)</sup> <sup>(2)</sup>

| PARAMETER                                                           | MIN  | TYP      | MAX                     | UNIT    |
|---------------------------------------------------------------------|------|----------|-------------------------|---------|
| $V_{INP}$ , $V_{INN}$ <sup>(3)</sup> Input voltage range            | GNDA |          | $V_{DDA}$               | V       |
| $V_{CM}$ Input common-mode voltage range                            | GNDA |          | $V_{DDA}$               | V       |
| $V_{OS}$ Input offset voltage                                       |      | $\pm 10$ | $\pm 50$ <sup>(4)</sup> | mV      |
| $I_{INP}$ , $I_{INN}$ Input leakage current over full voltage range |      |          | 2.0                     | $\mu A$ |
| $C_{MRR}$ Common-mode rejection ratio                               |      | 50       |                         | dB      |
| $t_{RT}$ Response time                                              |      |          | 1.0 <sup>(5)</sup>      | $\mu s$ |
| $t_{MC}$ Comparator mode change to output valid                     |      |          | 10                      | $\mu s$ |

(1) Best design practices suggest placing static or quiet digital I/O signals adjacent to sensitive analog inputs to reduce capacitive coupling and crosstalk.

(2) To achieve best analog results, keep the source resistance driving the analog inputs,  $V_{INP}$  and  $V_{INN}$ , low.

(3) The external voltage inputs to the analog comparator are designed to be highly sensitive and can be affected by external noise on the board. For this reason,  $V_{INP}$  and  $V_{INN}$  must be set to different voltage levels during idle states to ensure the analog comparator triggers are not enabled. If an internal voltage reference is used, it should be set to a mid-supply level. When operating in sleep or deep-sleep modes, disable the analog comparator module or set the external voltage inputs to different levels (greater than the input offset voltage) to achieve minimum current draw.

(4) Measured at  $V_{REF} = 100$  mV

(5) Measured at external  $V_{REF} = 100$  mV, input signal switching from 75 mV to 125 mV

表 5-48 lists the characteristics for the comparator.

**表 5-48. Analog Comparator Characteristics**

over operating free-air temperature (unless otherwise noted)

| PARAMETER                             | MIN | TYP               | MAX              | UNIT |
|---------------------------------------|-----|-------------------|------------------|------|
| $R_{HR}$ Resolution in high range     |     | $V_{DDA} / 29.4$  |                  | V    |
| $R_{LR}$ Resolution in low range      |     | $V_{DDA} / 22.12$ |                  | V    |
| $A_{HR}$ Absolute accuracy high range |     |                   | $\pm R_{HR} / 2$ | V    |
| $A_{LR}$ Absolute accuracy low range  |     |                   | $\pm R_{LR} / 2$ | V    |

表 5-49 和 表 5-50 list the reference voltages for the comparator under different conditions.

**表 5-49. Analog Comparator Voltage Reference Characteristics**

$V_{DDA} = 3.3\text{ V}$ ,  $EN = 1$ ,  $RNG = 0$ , over operating free-air temperature (unless otherwise noted)

| PARAMETER                    | TEST CONDITIONS | MIN   | TYP   | MAX   | UNIT |
|------------------------------|-----------------|-------|-------|-------|------|
| $V_{IREF}$ Reference voltage | $VREF = 0x0$    | 0.731 | 0.786 | 0.841 | V    |
|                              | $VREF = 0x1$    | 0.843 | 0.898 | 0.953 |      |
|                              | $VREF = 0x2$    | 0.955 | 1.010 | 1.065 |      |
|                              | $VREF = 0x3$    | 1.067 | 1.122 | 1.178 |      |
|                              | $VREF = 0x4$    | 1.180 | 1.235 | 1.290 |      |
|                              | $VREF = 0x5$    | 1.292 | 1.347 | 1.402 |      |
|                              | $VREF = 0x6$    | 1.404 | 1.459 | 1.514 |      |
|                              | $VREF = 0x7$    | 1.516 | 1.571 | 1.627 |      |
|                              | $VREF = 0x8$    | 1.629 | 1.684 | 1.739 |      |
|                              | $VREF = 0x9$    | 1.741 | 1.796 | 1.851 |      |
|                              | $VREF = 0xA$    | 1.853 | 1.908 | 1.963 |      |
|                              | $VREF = 0xB$    | 1.965 | 2.020 | 2.076 |      |
|                              | $VREF = 0xC$    | 2.078 | 2.133 | 2.188 |      |
|                              | $VREF = 0xD$    | 2.190 | 2.245 | 2.300 |      |
|                              | $VREF = 0xE$    | 2.302 | 2.357 | 2.412 |      |
|                              | $VREF = 0xF$    | 2.414 | 2.469 | 2.525 |      |

**表 5-50. Analog Comparator Voltage Reference Characteristics**

$V_{DDA} = 3.3\text{ V}$ ,  $EN = 1$ ,  $RNG = 1$ , over operating free-air temperature (unless otherwise noted)

| PARAMETER                    | TEST CONDITIONS | MIN   | TYP   | MAX   | UNIT |
|------------------------------|-----------------|-------|-------|-------|------|
| $V_{IREF}$ Reference voltage | $VREF = 0x0$    | 0.000 | 0.000 | 0.074 | V    |
|                              | $VREF = 0x1$    | 0.076 | 0.149 | 0.223 |      |
|                              | $VREF = 0x2$    | 0.225 | 0.298 | 0.372 |      |
|                              | $VREF = 0x3$    | 0.374 | 0.448 | 0.521 |      |
|                              | $VREF = 0x4$    | 0.523 | 0.597 | 0.670 |      |
|                              | $VREF = 0x5$    | 0.672 | 0.746 | 0.820 |      |
|                              | $VREF = 0x6$    | 0.822 | 0.895 | 0.969 |      |
|                              | $VREF = 0x7$    | 0.971 | 1.044 | 1.118 |      |
|                              | $VREF = 0x8$    | 1.120 | 1.193 | 1.267 |      |
|                              | $VREF = 0x9$    | 1.269 | 1.343 | 1.416 |      |
|                              | $VREF = 0xA$    | 1.418 | 1.492 | 1.565 |      |
|                              | $VREF = 0xB$    | 1.567 | 1.641 | 1.715 |      |
|                              | $VREF = 0xC$    | 1.717 | 1.790 | 1.864 |      |
|                              | $VREF = 0xD$    | 1.866 | 1.939 | 2.013 |      |
|                              | $VREF = 0xE$    | 2.015 | 2.089 | 2.162 |      |
|                              | $VREF = 0xF$    | 2.164 | 2.238 | 2.311 |      |

### 5.15.17 Pulse-Width Modulator (PWM)

表 5-51 lists the PWM timing characteristics.

**表 5-51. PWM Timing Characteristics**

over operating free-air temperature (unless otherwise noted)

| PARAMETER    |                                                   | MIN | TYP | MAX                | UNIT              |
|--------------|---------------------------------------------------|-----|-----|--------------------|-------------------|
| $t_{FLTW}$   | Minimum fault pulse width                         | 2   |     |                    | PWM clock periods |
| $t_{FLTMAX}$ | MnFAULTn assertion to PWM inactive <sup>(1)</sup> |     |     | 24 + (1 PWM clock) | ns                |
| $t_{FLTMIN}$ | MnFAULTn deassertion to PWM active <sup>(2)</sup> | 5   |     |                    | ns                |

(1) This parameter value can vary depending on the PWM clock frequency which is controlled by the System Clock and a programmable divider field in the PWMCC register.

(2) The latch and minimum fault period functions that can be enabled in the PWMnCTL register can change the timing of this parameter.

### 5.15.18 Emulation and Debug

表 5-52 lists the JTAG characteristics.

**表 5-52. JTAG Characteristics**

over operating free-air temperature (unless otherwise noted) (see 图 5-40 and 图 5-41)

| NO. | PARAMETER       |                                        | MIN                               | TYP           | MAX | UNIT |
|-----|-----------------|----------------------------------------|-----------------------------------|---------------|-----|------|
| J1  | $f_{TCK}$       | TCK operational clock frequency        | 0                                 |               | 10  | MHz  |
| J2  | $t_{TCK}$       | TCK operational clock period           | 100                               |               |     | ns   |
| J3  | $t_{TCK\_LOW}$  | TCK clock low time                     |                                   | $t_{TCK} / 2$ |     | ns   |
| J4  | $t_{TCK\_HIGH}$ | TCK clock high time                    |                                   | $t_{TCK} / 2$ |     | ns   |
| J5  | $t_{TCK\_R}$    | TCK rise time                          | 0                                 |               | 10  | ns   |
| J6  | $t_{TCK\_F}$    | TCK fall time                          | 0                                 |               | 10  | ns   |
| J7  | $t_{TMS\_SU}$   | TMS setup time to TCK rise             | 8                                 |               |     | ns   |
| J8  | $t_{TMS\_HLD}$  | TMS hold time from TCK rise            | 4                                 |               |     | ns   |
| J9  | $t_{TDI\_SU}$   | TDI setup time to TCK rise             | 18                                |               |     | ns   |
| J10 | $t_{TDI\_HLD}$  | TDI hold time from TCK rise            | 4                                 |               |     | ns   |
| J11 | $t_{TDO\_ZDV}$  | TCK fall to data valid from Hi-Z       | 2-mA drive                        | 13            | 35  | ns   |
|     |                 |                                        | 4-mA drive                        | 9             | 26  |      |
|     |                 |                                        | 8-mA drive                        | 8             | 26  |      |
|     |                 |                                        | 8-mA drive with slew rate control | 10            | 29  |      |
|     |                 |                                        | 10-mA drive                       | 11            | 13  |      |
|     |                 |                                        | 12-mA drive                       | 11            | 14  |      |
| J12 | $t_{TDO\_DV}$   | TCK fall to data valid from data valid | 2-mA drive                        | 14            | 20  | ns   |
|     |                 |                                        | 4-mA drive                        | 10            | 26  |      |
|     |                 |                                        | 8-mA drive                        | 8             | 21  |      |
|     |                 |                                        | 8-mA drive with slew rate control | 10            | 26  |      |
|     |                 |                                        | 10-mA drive                       | 12            | 14  |      |
|     |                 |                                        | 12-mA drive                       | 12            | 15  |      |
| J13 | $t_{TDO\_DVZ}$  | TCK fall to Hi-Z from data valid       | 2-mA drive                        | 7             | 16  | ns   |
|     |                 |                                        | 4-mA drive                        | 7             | 16  |      |
|     |                 |                                        | 8-mA drive                        | 7             | 16  |      |
|     |                 |                                        | 8-mA drive with slew rate control | 8             | 19  |      |
|     |                 |                                        | 10-mA drive                       | 20            | 22  |      |
|     |                 |                                        | 12-mA drive                       | 20            | 25  |      |

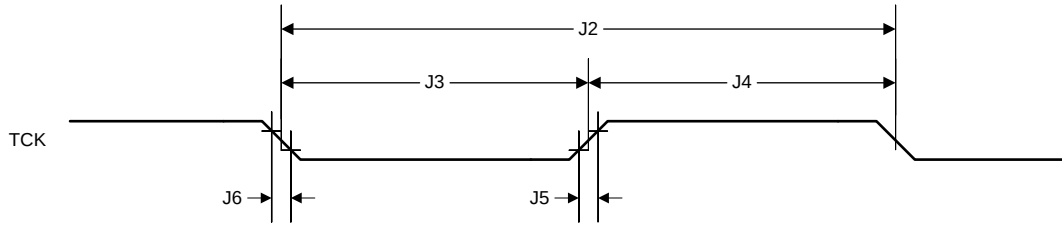


**图 5-40. JTAG Test Clock Input Timing**

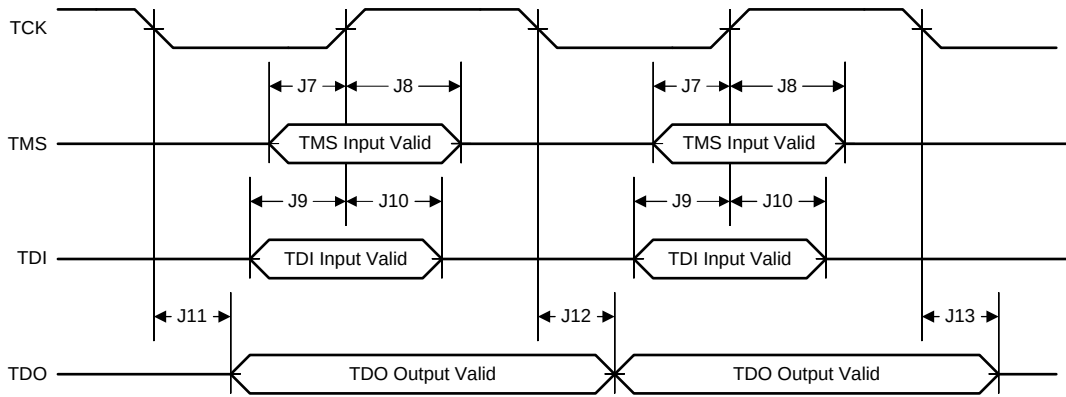


**图 5-41. JTAG Test Access Port (TAP) Timing**

## 6 Detailed Description

### 6.1 Overview

The SimpleLink MSP432E401Y Arm Cortex-M4 microcontroller (MCU) provides top performance and advanced integration. The MSP432E4 product family is positioned for cost-effective applications requiring significant control processing and connectivity capabilities such as the following:

- Industrial communication equipment
- Network appliances, gateways, and adapters
- Residential and commercial site monitoring and control
- Remote connectivity and monitoring
- Security and access systems
- HMI control panels
- Factory automation control
- Test and measurement equipment
- Fire and security systems
- Motion control and power inversion
- Medical instrumentation
- Gaming equipment
- Electronic point-of-sale (POS) displays
- Smart energy and smart grid solutions
- Intelligent lighting control
- Vehicle tracking

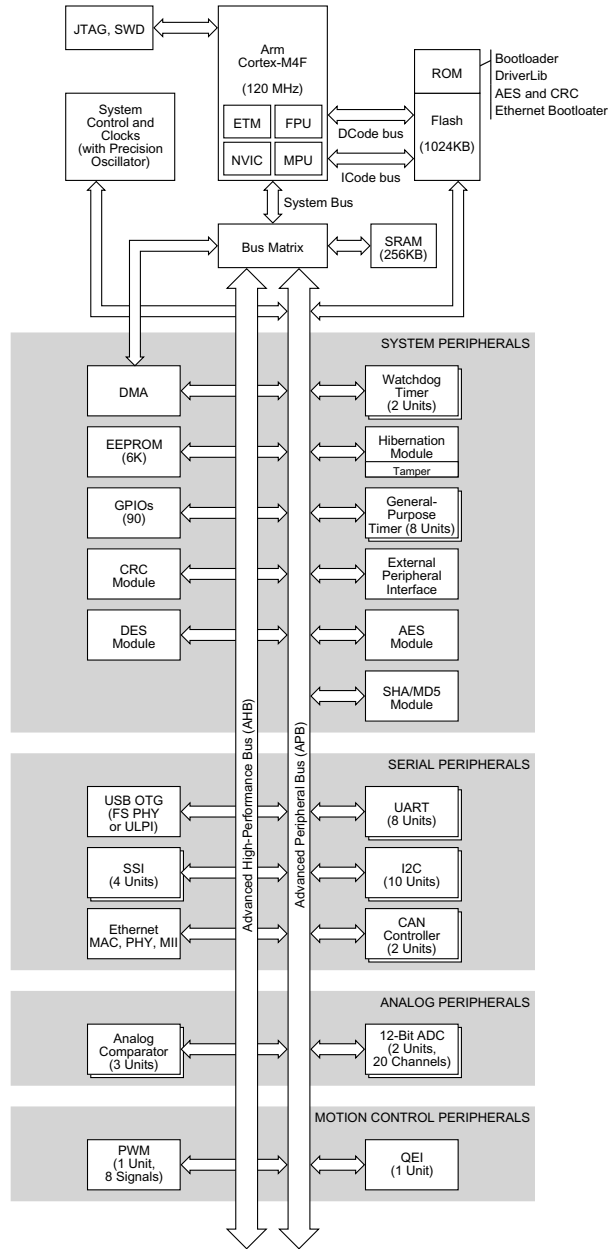
The MSP432E401Y MCU integrates a large variety of rich communication features to enable a new class of highly connected designs that can support critical, real-time control with a balance between performance and power. The MCU features integrated communication peripherals and other high-performance analog and digital functions to offer a strong foundation for many different target uses, from human-machine interface to networked system management controllers.

In addition, the MSP432E401Y MCU offers the advantages of widely available development tools from Arm, System-on-Chip (SoC) infrastructure, and a large user community. Additionally, this MCU uses the Thumb-compatible Thumb-2 instruction set from Arm to reduce memory requirements and, thereby, cost. Finally, when using the SimpleLink SDK, the MSP432E401Y MCU is code-compatible with all members of the SimpleLink series, providing flexibility to fit precise needs.

TI offers a complete solution to get to market quickly, with evaluation and development boards; white papers and application notes; an easy-to-use peripheral driver library; and a strong support, sales, and distributor network.

## 6.2 Functional Block Diagram

图 6-1 shows the features on the MSP432E401Y MCU. Two on-chip buses connect the core to the peripherals. The Advanced Peripheral Bus (APB) bus is the legacy bus. The Advanced High-Performance Bus (AHB) bus provides better back-to-back access performance than the APB bus.



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图 6-1. MSP432E401Y High-Level Block Diagram

## 6.3 Arm Cortex-M4F Processor Core

All members of the MSP432E4 family are designed around an Arm Cortex-M processor core. The Arm Cortex-M processor provides the core for a high-performance low-cost platform that meets the needs of minimal memory implementation, reduced pin count, and low power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

### 6.3.1 Processor Core

Features of the processor core include:

- 32-bit Arm Cortex-M4F architecture optimized for small-footprint embedded applications
- 120-MHz operation; 150 DMIPS performance
- Outstanding processing performance combined with fast interrupt handling
- Thumb-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit Arm core in a compact memory size usually associated with 8- and 16-bit devices, typically in the range of a few kilobytes of memory for MCU-class applications.
  - Single-cycle multiply instruction and hardware divide
  - Atomic bit manipulation (bit-banding), delivering maximum memory use and streamlined peripheral control
  - Unaligned data access, enabling data to be efficiently packed into memory
- IEEE 754-compliant single-precision floating-point unit (FPU)
- 16-bit SIMD vector processing unit
- Fast code execution permits slower processor clock or increases sleep mode time
- Harvard architecture characterized by separate buses for instruction and data
- Efficient processor core, system, and memories
- Hardware division and fast digital-signal-processing orientated multiply accumulate
- Saturating arithmetic for signal processing
- Deterministic high-performance interrupt handling for time-critical applications
- Memory protection unit (MPU) to provide a privileged mode for protected operating system functionality
- Enhanced system debug with extensive breakpoint and trace capabilities
- Serial Wire Debug and Serial Wire Trace reduce the number of pins required for debugging and tracing
- Migration from the Arm7<sup>®</sup> processor family for better performance and power efficiency
- Optimized for single-cycle flash memory use up to specific frequencies; see the *Internal Memory* chapter of the [MSP432E4 SimpleLink™ Microcontrollers Technical Reference Manual](#) for more information.
- Ultra-low-power consumption with integrated sleep modes

### 6.3.2 System Timer (SysTick)

SysTick provides a simple, 24-bit, clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used in several different ways, for example:

- An RTOS tick timer that fires at a programmable rate (for example, 100 Hz) and invokes a SysTick routine
- A high-speed alarm timer using the system clock
- A variable rate alarm or signal timer—the duration is range-dependent on the reference clock used and the dynamic range of the counter
- A simple counter used to measure time to completion and time used
- An internal clock-source control based on missing or meeting durations

### 6.3.3 Nested Vectored Interrupt Controller (NVIC)

The NVIC and Cortex-M4F core prioritize and handle all exceptions in handler mode. The processor state is automatically stored to the stack on an exception and automatically restored from the stack at the end of the interrupt service routine (ISR). The interrupt vector is fetched in parallel to the state saving, enabling efficient interrupt entry. The processor supports tail-chaining, meaning that back-to-back interrupts can be performed without the overhead of state saving and restoration. Software can set 8 priority levels on 7 exceptions (system handlers) and 109 interrupts.

- Deterministic, fast interrupt processing: always 12 cycles, or just 6 cycles with tail-chaining (these values reflect no FPU stacking)
- External nonmaskable interrupt signal (NMI) available for immediate execution of NMI handler for safety critical applications
- Dynamically reprioritizable interrupts
- Exceptional interrupt handling through hardware implementation of required register manipulations

表 6-1 lists the interrupts.

**表 6-1. Interrupts**

| VECTOR NUMBER | INTERRUPT NUMBER<br>(BIT IN INTERRUPT<br>REGISTERS) | VECTOR ADDRESS OR<br>OFFSET   | DESCRIPTION             |
|---------------|-----------------------------------------------------|-------------------------------|-------------------------|
| 0 to 15       | –                                                   | 0x0000.0000 to<br>0x0000.003C | Processor exceptions    |
| 16            | 0                                                   | 0x0000.0040                   | GPIO Port A             |
| 17            | 1                                                   | 0x0000.0044                   | GPIO Port B             |
| 18            | 2                                                   | 0x0000.0048                   | GPIO Port C             |
| 19            | 3                                                   | 0x0000.004C                   | GPIO Port D             |
| 20            | 4                                                   | 0x0000.0050                   | GPIO Port E             |
| 21            | 5                                                   | 0x0000.0054                   | UART0                   |
| 22            | 6                                                   | 0x0000.0058                   | UART1                   |
| 23            | 7                                                   | 0x0000.005C                   | SSI0                    |
| 24            | 8                                                   | 0x0000.0060                   | I2C0                    |
| 25            | 9                                                   | 0x0000.0064                   | PWM fault               |
| 26            | 10                                                  | 0x0000.0068                   | PWM generator 0         |
| 27            | 11                                                  | 0x0000.006C                   | PWM generator 1         |
| 28            | 12                                                  | 0x0000.0070                   | PWM generator 2         |
| 29            | 13                                                  | 0x0000.0074                   | QEI0                    |
| 30            | 14                                                  | 0x0000.0078                   | ADC0 sequence 0         |
| 31            | 15                                                  | 0x0000.007C                   | ADC0 sequence 1         |
| 32            | 16                                                  | 0x0000.0080                   | ADC0 sequence 2         |
| 33            | 17                                                  | 0x0000.0084                   | ADC0 sequence 3         |
| 34            | 18                                                  | 0x0000.0088                   | Watchdog timers 0 and 1 |
| 35            | 19                                                  | 0x0000.008C                   | 16-/32-Bit Timer 0A     |
| 36            | 20                                                  | 0x0000.0090                   | 16-/32-Bit Timer 0B     |
| 37            | 21                                                  | 0x0000.0094                   | 16-/32-Bit Timer 1A     |
| 38            | 22                                                  | 0x0000.0098                   | 16-/32-Bit Timer 1B     |
| 39            | 23                                                  | 0x0000.009C                   | 16-/32-Bit Timer 2A     |
| 40            | 24                                                  | 0x0000.00A0                   | 16-/32-Bit Timer 2B     |
| 41            | 25                                                  | 0x0000.00A4                   | Analog comparator 0     |
| 42            | 26                                                  | 0x0000.00A8                   | Analog comparator 1     |
| 43            | 27                                                  | 0x0000.00AC                   | Analog comparator 2     |
| 44            | 28                                                  | 0x0000.00B0                   | System control          |

表 6-1. Interrupts (continued)

| VECTOR NUMBER | INTERRUPT NUMBER<br>(BIT IN INTERRUPT<br>REGISTERS) | VECTOR ADDRESS OR<br>OFFSET | DESCRIPTION                          |
|---------------|-----------------------------------------------------|-----------------------------|--------------------------------------|
| 45            | 29                                                  | 0x0000.00B4                 | Flash memory control                 |
| 46            | 30                                                  | 0x0000.00B8                 | GPIO port F                          |
| 47            | 31                                                  | 0x0000.00BC                 | GPIO port G                          |
| 48            | 32                                                  | 0x0000.00C0                 | GPIO port H                          |
| 49            | 33                                                  | 0x0000.00C4                 | UART2                                |
| 50            | 34                                                  | 0x0000.00C8                 | SSI1                                 |
| 51            | 35                                                  | 0x0000.00CC                 | 16-/32-Bit Timer 3A                  |
| 52            | 36                                                  | 0x0000.00D0                 | 16-/32-Bit Timer 3B                  |
| 53            | 37                                                  | 0x0000.00D4                 | I2C1                                 |
| 54            | 38                                                  | 0x0000.00D8                 | CAN0                                 |
| 55            | 39                                                  | 0x0000.00DC                 | CAN1                                 |
| 56            | 40                                                  | 0x0000.00E0                 | Ethernet MAC                         |
| 57            | 41                                                  | 0x0000.00E4                 | HIB                                  |
| 58            | 42                                                  | 0x0000.00E8                 | USB MAC                              |
| 59            | 43                                                  | 0x0000.00EC                 | PWM generator 3                      |
| 60            | 44                                                  | 0x0000.00F0                 | μDMA 0 Software                      |
| 61            | 45                                                  | 0x0000.00F4                 | μDMA 0 Error                         |
| 62            | 46                                                  | 0x0000.00F8                 | ADC1 sequence 0                      |
| 63            | 47                                                  | 0x0000.00FC                 | ADC1 sequence 1                      |
| 64            | 48                                                  | 0x0000.0100                 | ADC1 sequence 2                      |
| 65            | 49                                                  | 0x0000.0104                 | ADC1 sequence 3                      |
| 66            | 50                                                  | 0x0000.0108                 | EPI0                                 |
| 67            | 51                                                  | 0x0000.010C                 | GPIO port J                          |
| 68            | 52                                                  | 0x0000.0110                 | GPIO port K                          |
| 69            | 53                                                  | 0x0000.0114                 | GPIO port L                          |
| 70            | 54                                                  | 0x0000.0118                 | SSI2                                 |
| 71            | 55                                                  | 0x0000.011C                 | SSI3                                 |
| 72            | 56                                                  | 0x0000.0120                 | UART3                                |
| 73            | 57                                                  | 0x0000.0124                 | UART4                                |
| 74            | 58                                                  | 0x0000.0128                 | UART5                                |
| 75            | 59                                                  | 0x0000.012C                 | UART6                                |
| 76            | 60                                                  | 0x0000.0130                 | UART7                                |
| 77            | 61                                                  | 0x0000.0134                 | I2C2                                 |
| 78            | 62                                                  | 0x0000.0138                 | I2C3                                 |
| 79            | 63                                                  | 0x0000.013C                 | Timer 4A                             |
| 80            | 64                                                  | 0x0000.0140                 | Timer 4B                             |
| 81            | 65                                                  | 0x0000.0144                 | Timer 5A                             |
| 82            | 66                                                  | 0x0000.0148                 | Timer 5B                             |
| 83            | 67                                                  | 0x0000.014C                 | Floating-Point Exception (imprecise) |
| 84            | 68                                                  | –                           | Reserved                             |
| 85            | 69                                                  | –                           | Reserved                             |
| 86            | 70                                                  | 0x0000.0158                 | I2C4                                 |
| 87            | 71                                                  | 0x0000.015C                 | I2C5                                 |
| 88            | 72                                                  | 0x0000.0160                 | GPIO port M                          |
| 89            | 73                                                  | 0x0000.0164                 | GPIO port N                          |
| 90            | 74                                                  | –                           | Reserved                             |

**表 6-1. Interrupts (continued)**

| VECTOR NUMBER | INTERRUPT NUMBER<br>(BIT IN INTERRUPT<br>REGISTERS) | VECTOR ADDRESS OR<br>OFFSET | DESCRIPTION                 |
|---------------|-----------------------------------------------------|-----------------------------|-----------------------------|
| 91            | 75                                                  | 0x0000.016C                 | Tamper                      |
| 92            | 76                                                  | 0x0000.017                  | GPIO port P (Summary or P0) |
| 93            | 77                                                  | 0x0000.0174                 | GPIO port P1                |
| 94            | 78                                                  | 0x0000.0178                 | GPIO port P2                |
| 95            | 79                                                  | 0x0000.017C                 | GPIO port P3                |
| 96            | 80                                                  | 0x0000.0180                 | GPIO port P4                |
| 97            | 81                                                  | 0x0000.0184                 | GPIO port P5                |
| 98            | 82                                                  | 0x0000.0188                 | GPIO port P6                |
| 99            | 83                                                  | 0x0000.018C                 | GPIO port P7                |
| 100           | 84                                                  | 0x0000.0190                 | GPIO port Q (summary or Q0) |
| 101           | 85                                                  | 0x0000.0194                 | GPIO port Q1                |
| 102           | 86                                                  | 0x0000.0198                 | GPIO port Q2                |
| 103           | 87                                                  | 0x0000.019C                 | GPIO port Q3                |
| 104           | 88                                                  | 0x0000.01A0                 | GPIO port Q4                |
| 105           | 89                                                  | 0x0000.01A4                 | GPIO port Q5                |
| 106           | 90                                                  | 0x0000.01A8                 | GPIO port Q6                |
| 107           | 91                                                  | 0x0000.01AC                 | GPIO port Q7                |
| 108           | 92                                                  | –                           | Reserved                    |
| 109           | 93                                                  | –                           | Reserved                    |
| 110           | 94                                                  | 0x0000.01B8                 | SHA/MD5                     |
| 111           | 95                                                  | 0x0000.01BC                 | AES                         |
| 112           | 96                                                  | 0x0000.01C0                 | DES                         |
| 113           | 97                                                  | –                           | Reserved                    |
| 114           | 98                                                  | 0x0000.01C8                 | 16-/32-Bit Timer 6A         |
| 115           | 99                                                  | 0x0000.01CC                 | 16-/32-Bit Timer 6B         |
| 116           | 100                                                 | 0x0000.01D0                 | 16-/32-Bit Timer 7A         |
| 117           | 101                                                 | 0x0000.01D4                 | 16-/32-Bit Timer 7B         |
| 118           | 102                                                 | 0x0000.01D8                 | I2C6                        |
| 119           | 103                                                 | 0x0000.01DC                 | I2C7                        |
| 120           | 104                                                 | –                           | Reserved                    |
| 121           | 105                                                 | –                           | Reserved                    |
| 122           | 106                                                 | –                           | Reserved                    |
| 123           | 107                                                 | –                           | Reserved                    |
| 124           | 108                                                 | –                           | Reserved                    |
| 125           | 109                                                 | 0x0000.01F4                 | I2C8                        |
| 126           | 110                                                 | 0x0000.01F8                 | I2C9                        |
| 127           | 111                                                 | –                           | Reserved                    |

### 6.3.4 System Control Block (SCB)

The SCB provides system implementation information and system control, including configuration, control, and reporting of system exceptions.

### 6.3.5 Memory Protection Unit (MPU)

The MPU supports the standard Arm7 Protected Memory System Architecture (PMSA) model. The MPU provides full support for protection regions, overlapping protection regions, access permissions, and exporting memory attributes to the system.

### 6.3.6 Floating-Point Unit (FPU)

The FPU fully supports single-precision add, subtract, multiply, divide, multiply-and-accumulate, and square root operations. It also provides conversions between fixed-point and floating-point data formats, and floating-point constant instructions.

- 32-bit instructions for single-precision (C float) data-processing operations
- Combined multiply and accumulate instructions for increased precision (fused MAC)
- Hardware support for conversion, addition, subtraction, multiplication with optional accumulate, division, and square-root
- Hardware support for denormals and all IEEE rounding modes
- 32 dedicated 32-bit single-precision registers, also addressable as 16 double-word registers
- Decoupled 3-stage pipeline

## 6.4 On-Chip Memory

The following on-chip memories are supported:

- 256KB of single-cycle SRAM
- 1024KB of flash memory
- 6KB of EEPROM
- Internal ROM loaded with SimpleLink SDK software:
  - Peripheral driver library
  - Bootloader

### 6.4.1 SRAM

The MSP432E401Y MCU provides 256KB of single-cycle on-chip SRAM. The internal SRAM of the device is at offset 0x2000.0000 of the device memory map.

The SRAM is implemented using four 32-bit-wide interleaving SRAM banks (separate SRAM arrays), which allow for increased speed between memory accesses. The SRAM memory provides nearly 2 GBps of memory bandwidth at a 120-MHz clock frequency.

Because read-modify-write (RMW) operations are time consuming, Arm has introduced bit-banding technology in the Cortex-M4F processor. With a bit-band-enabled processor, certain regions in the memory map (SRAM and peripheral space) can use address aliases to access individual bits in an atomic operation.

Data can be transferred to and from SRAM by the following masters:

- $\mu$ DMA
- USB
- Ethernet controller

### 6.4.2 Flash Memory

The MSP432E401Y MCU provides 1024KB of on-chip flash memory. The flash memory is configured as four banks of 16K  $\times$  128 bits (4  $\times$  256KB total) that are 2-way interleaved. Memory blocks can be marked as read only or execute only, providing different levels of code protection. Read-only blocks cannot be erased or programmed, protecting the contents of those blocks from being modified. Execute-only blocks cannot be erased or programmed, and can only be read by the controller instruction fetch mechanism, protecting the contents of those blocks from being read by either the controller or a debugger.

Two sets of instruction prefetch buffers provide enhanced performance and power savings. Each prefetch buffer is 2  $\times$  256 bits and can be combined as a 4  $\times$  256-bit prefetch buffer.

The flash can also be accessed by the  $\mu$ DMA in run mode.

### **6.4.3 ROM**

The ROM is preprogrammed with the following software and programs:

- Peripheral driver library
- Bootloader

The SimpleLink MSP432E4 SDK driver library is a royalty-free software library for controlling on-chip peripherals with a bootloader capability. The library performs both peripheral initialization and control functions, with a choice of polled or interrupt-driven peripheral support. In addition, the library is designed to take full advantage of the stellar interrupt performance of the Arm Cortex-M4F core. No special pragmas or custom assembly code prologue or epilogue functions are required. For applications that require in-field programmability, the royalty-free bootloader can act as an application loader and support in-field firmware updates.

### **6.4.4 EEPROM**

The EEPROM includes the following features:

- 6KB of memory accessible as 1536 32-bit words
- 96 blocks of 16 words (64 bytes) each
- Built-in wear leveling
- Access protection per block
- Lock protection option for the whole peripheral as well as per block using 32-bit to 96-bit unlock codes (application selectable)
- Interrupt support for write completion to avoid polling
- Endurance of 500k writes (when writing at fixed offset in every alternate page in circular fashion) to 15M operations (when cycling through two pages) per each 2-page block.

### 6.4.5 Memory Map

The device supports a 4GB address space that is divided into eight 512MB zones (see 图 6-2).

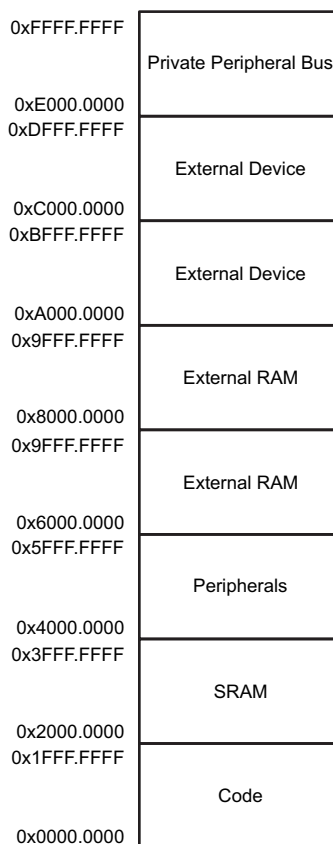


图 6-2. Device Memory Zones

## 6.5 Peripherals

### 6.5.1 External Peripheral Interface (EPI)

The EPI provides access to external devices using a parallel path. Unlike communications peripherals such as SSI, UART, and I<sup>2</sup>C, the EPI acts as a bus to external peripherals and memory.

The EPI has the following features:

- 8-, 16-, or 32-bit dedicated parallel bus for external peripherals and memory
- Memory interface supports contiguous memory access independent of data bus width, thus enabling code execution directly from SDRAM, SRAM, and flash memory
- Blocking and nonblocking reads
- Separates processor from timing details through use of an internal write FIFO
- Efficient transfers using  $\mu$ DMA
  - Separate channels for read and write
  - Read channel request asserted by programmable levels on the internal Nonblocking Read FIFO (NBRFIFO)
  - Write channel request asserted by empty on the internal Write FIFO (WFIFO)

The EPI supports three primary functional modes: SDRAM mode, traditional host-bus mode, and general-purpose mode. The EPI module also provides custom GPIOs; however, unlike regular GPIOs, the EPI module uses a FIFO in the same way as a communication mechanism and is speed-controlled using clocking.

- SDRAM mode
  - Supports  $\times 16$  (single data rate) SDRAM at up to 60 MHz
  - Supports low-cost SDRAMs up to 64MB (512 Mb)
  - Includes automatic refresh and access to all banks and rows
  - Includes a sleep (standby) mode to keep contents active with minimal power draw
  - Multiplexed address and data interface for reduced pin count
- Host-bus mode
  - Traditional  $\times 8$  and  $\times 16$  MCU bus interface capabilities
  - Similar device compatibility options as PIC, ATmega, 8051, and others
  - Access to SRAM, NOR flash memory, and other devices, with up to 1MB of addressing in nonmultiplexed mode and 256MB in multiplexed mode (512MB in host bus 16 mode with no byte selects)
  - Support for up to 512Mb PSRAM in quad chip select mode, with dedicated configuration register read and write enable
  - Support of both muxed and demuxed address and data
  - Access to a range of devices supporting the nonaddress FIFO  $\times 8$  and  $\times 16$  interface variant, with support for external FIFO (XFIFO) EMPTY and FULL signals
  - Speed controlled, with read and write data wait-state counters
  - Support for read or write burst mode to Host Bus
  - Multiple chip-select modes including single, dual, and quad chip selects, with and without ALE
  - External iRDY signal provided for stall capability of reads and writes
  - Manual chip-enable (or use extra address pins)
- General-purpose mode
  - Wide parallel interfaces for fast communications with CPLDs and FPGAs
  - Data widths up to 32 bits
  - Data rates up to 150 MB/second
  - Optional "address" sizes from 4 bits to 20 bits
  - Optional clock output, read and write strobes, framing (with counter-based size), and clock-enable input
- General parallel GPIO
  - 1 to 32 bits, FIFO with speed control
  - Useful for custom peripherals or for digital data acquisition and actuator controls

### 6.5.2 Cyclical Redundancy Check (CRC)

The CRC computation module is for uses such as message transfer and safety system checks. This module can be used with the AES and DES modules. The CRC has the following features:

- Support four major CRC forms:
  - CRC16-CCITT as used by CCITT/ITU X.25
  - CRC16-IBM as used by USB and ANSI
  - CRC32-IEEE as used by IEEE 802.3 and MPEG-2
  - CRC32C as used by G.Hn
- Allows word and byte feed
- Supports automatic initialization and manual initialization
- Supports MSb and LSb
- Supports CCITT post-processing
- Can be fed by  $\mu$ DMA, flash memory, and code

### 6.5.3 Advanced Encryption Standard (AES) Accelerator

The AES accelerator module provides hardware-accelerated data encryption and decryption operations based on a binary key. The AES module is a symmetric cipher module that supports a 128-, 192-, or 256-bit key in hardware for both encryption and decryption.

The AES has following features:

- Support for basic AES encryption and decryption operations:
  - Galois/counter mode (GCM) with basic GHASH operation
  - Counter mode with CBC-MAC (CCM)
  - XTS mode
- Availability of the following feedback operating modes:
  - Electronic code book mode (ECB)
  - Cipher block chaining mode (CBC)
  - Counter mode (CTR)
  - Cipher feedback mode (CFB), 128-bit
  - F8 mode
- Key sizes 128-, 192-, and 256-bits
- Support for CBC\_MAC and Fedora 9 (F9) authentication modes
- Basic GHASH operation (when selecting no encryption)
- Key scheduling in hardware
- Support for  $\mu$ DMA transfers
- Fully synchronous design

### 6.5.4 Data Encryption Standard (DES) Accelerator

The DES module provides hardware accelerated data encryption and decryption functions. The module runs either the single DES or the triple DES (3DES) algorithm and supports electronic codebook (ECB), cipher block chaining (CBC), and cipher feedback (CFB) modes of operation.

The DES accelerator includes the following main features:

- DES/3DES encryption and decryption algorithm compliant with the [FIPS 180-3 standard](#)
- Feedback modes: ECB, CBC, CFB
- Host interrupt or  $\mu$ DMA driven modes of operation.  $\mu$ DMA support for data and context in and result out
- Fully synchronous design
- Internal wide-bus interface

### 6.5.5 Secure Hash Algorithm/Message Digest Algorithm (SHA/MD5) Accelerator

The SHA/MD5 module provides hardware-accelerated hash functions and can run:

- MD5 message digest algorithm developed by Ron Rivest in 1991
- SHA-1 algorithm compliant with the [FIPS 180-3 standard](#)
- SHA-2 (SHA-224 and SHA-256) algorithm compliant with the [FIPS 180-3 standard](#)
- Hash message authentication code (HMAC) operation

The algorithms produce a condensed representation of a message or a data file, which can then be used to verify the message integrity.

The SHA/MD5 accelerator module includes the following main features:

- Hashing of 0 to  $(2^{33} - 2)$  bytes of data [of which  $(2^{32} - 1)$  bytes are in one pass] using the MD5, SHA-1, SHA-224, or SHA-256 hash algorithm (byte granularity only, no support for bit granularity)
- Automatic HMAC key preprocessing for HMAC keys up to 64 bytes

- Host-assisted HMAC key preprocessing for HMAC keys larger than 64 bytes
- HMAC from precomputes (inner and outer digest) for improved performance on small blocks
- Supports  $\mu$ DMA operation for data and context in and result out transfers
- Supports interrupt to read the digest (signature)

### 6.5.6 Serial Communications Peripherals

Both asynchronous and synchronous serial communications are supported with:

- 10/100 Ethernet MAC with advanced IEEE 1588 PTP hardware; integrated PHY provided
- Two CAN 2.0 A and B controllers
- USB 2.0 controller OTG, host, or device with optional high speed using external PHY through ULPI interface
- Eight UARTs with IrDA, 9-bit, and ISO 7816 support
- Ten I2C modules with four transmission speeds including high-speed mode
- Four Quad Synchronous Serial Interface (QSSI) modules with bi- and quad-SSI support

The following sections provide more detail on each of these communications functions.

#### 6.5.6.1 Ethernet MAC and PHY

The Ethernet controller consists of a fully integrated media access controller (MAC) and network physical (PHY) interface with the following features:

- Conforms to the IEEE 802.3 specification
  - 10BASE-T and 100BASE-TX IEEE-802.3 compliant
  - Supports 10- and 100-Mbps data transmission rates
  - Supports full-duplex and half-duplex (CSMA/CD) operation
  - Supports flow control and back pressure
  - Full-featured and enhanced auto-negotiation
  - Supports IEEE 802.1Q VLAN tag detection
- Conforms to IEEE 1588-2002 timestamp PTP protocol and the IEEE 1588-2008 advanced timestamp specification
  - Transmit and receive frame timestamping
  - Precision time protocol
  - Flexible pulse per second output
  - Supports coarse and fine correction methods
- Multiple addressing modes
  - Four MAC address filters
  - Programmable 64-bit hash filter for multicast address filtering
  - Promiscuous mode support
- Processor offloading
  - Programmable insertion (TX) or deletion (RX) of preamble and start-of-frame data
  - Programmable generation (TX) or deletion (RX) of CRC and pad data
  - IP header and hardware checksum checking (IPv4, IPv6, TCP, UDP, ICMP)
- Highly configurable
  - LED activity selection
  - Supports network statistics with RMON and MIB counters
  - Supports magic packet and wake-up frames

- Efficient transfers using integrated  $\mu$ DMA
  - Dual-buffer (ring) or linked-list (chained) descriptors
  - Round-robin or fixed priority arbitration between TX and RX
  - Descriptors support transfer blocks size up to 8KB
  - Programmable interrupts for flexible system implementation
- Physical media manipulation
  - MDI/MDI-X cross-over support
  - Register-programmable transmit amplitude
  - Automatic polarity correction and 10BASE-T signal reception

#### 6.5.6.2 Controller Area Network (CAN)

CAN is a multicast shared serial-bus standard for connecting electronic control units (ECUs). CAN was specifically designed to be robust in electromagnetically noisy environments and can use a differential balanced line like RS-485 or twisted-pair wire. Originally created for automotive purposes, it is now used in many embedded control applications (for example, industrial or medical). Bit rates up to 1 Mbps are possible at network lengths below 40 meters. Decreased bit rates allow longer network distances (for example, 125 kbps at 500 m).

A transmitter sends a message to all CAN nodes (broadcasting). Each node decides on the basis of the identifier received whether it should process the message. The identifier also determines the priority that the message enjoys in competition for bus access. Each CAN message can transmit from 0 to 8 bytes of user information.

Each of the two CAN units includes the following features:

- CAN protocol version 2.0 part A/B
- Bit rates up to 1 Mbps
- 32 message objects with individual identifier masks
- Maskable interrupt
- Disable Automatic Retransmission mode for Time-Triggered CAN (TTCAN) applications
- Programmable loopback mode for self-test operation
- Programmable FIFO mode enables storage of multiple message objects
- Gluelessly attaches to an external CAN transceiver through the CANnTX and CANnRX signals

#### 6.5.6.3 Universal Serial Bus (USB)

USB is a serial bus standard designed to allow connection and disconnection of peripherals using a standardized interface without rebooting the system.

One USB controller supports high-speed and full-speed multiple-point communications and complies with the USB 2.0 standard for high-speed function. The USB controller can have three configurations: USB device, USB host, and USB OTG (negotiated on-the-go as host or device when connected to other USB-enabled systems). Support for full-speed communication is provided by using the integrated USB PHY or optionally, a high-speed ULPI can communicate to an external PHY.

The USB module has the following features:

- Complies with USB-IF (Implementer's Forum) certification standards
- USB 2.0 high-speed (480 Mbps) operation with the integrated ULPI communicating with an external PHY
- Link power-management support that uses link-state awareness to reduce power usage
- Four transfer types: control, interrupt, bulk, and isochronous
- 16 endpoints
  - 1 dedicated control IN endpoint and 1 dedicated control OUT endpoint
  - 7 configurable IN endpoints and 7 configurable OUT endpoints

- 4KB of dedicated endpoint memory: one endpoint may be defined for double-buffered 1023-byte isochronous packet size
- VBUS droop detection and interrupt
- Integrated USB DMA with bus master capability
  - Up to eight RX endpoint channels and up to eight TX endpoint channels are available.
  - Each channel can be separately programmed to operate in different modes.
  - Incremental burst transfers of 4, 8, 16, or unspecified length supported

#### 6.5.6.4 Universal Asynchronous Receiver/Transmitter (UART)

A UART is an integrated circuit used for RS-232C serial communications, containing a transmitter (parallel-to-serial converter) and a receiver (serial-to-parallel converter), each clocked separately.

Eight fully programmable 16C550-type UARTs are integrated. Although the functionality is similar to a 16C550 UART, this UART design is not register compatible. The UART can generate individually masked interrupts from the RX, TX, modem flow control, modem status, and error conditions. The module generates one combined interrupt when any of the interrupts are asserted and are unmasked.

The UARTs have the following features:

- Programmable baud-rate generator allowing speeds up to 7.5 Mbps for regular speed (divide by 16) and 15 Mbps for high speed (divide by 8)
- Separate 16×8 transmit (TX) and receive (RX) FIFOs to reduce CPU interrupt service loading
- Programmable FIFO length, including a 1-byte-deep operation providing conventional double-buffered interface
- FIFO trigger levels of 1/8, 1/4, 1/2, 3/4, and 7/8
- Standard asynchronous communication bits for start, stop, and parity
- Line-break generation and detection
- Fully programmable serial interface characteristics
  - 5, 6, 7, or 8 data bits
  - Even, odd, stick, or no-parity bit generation/detection
  - 1 or 2 stop bit generation
- IrDA serial-IR (SIR) encoder and decoder providing
  - Programmable use of IrDA Serial Infrared (SIR) or UART I/O
  - Support of IrDA SIR encoder and decoder functions for data rates up to 115.2 kbps half-duplex
  - Support of normal 3/16 and low-power (1.41 to 2.23 μs) bit durations
  - Programmable internal clock generator enabling division of reference clock by 1 to 256 for low-power mode bit duration
- Support for communication with ISO 7816 smart cards
- Modem functionality available on the following UARTs:
  - UART0 (modem flow control and modem status)
  - UART1 (modem flow control and modem status)
  - UART2 (modem flow control)
  - UART3 (modem flow control)
  - UART4 (modem flow control)
- EIA-485 9-bit support
- Standard FIFO-level and end-of-transmission interrupts

- Efficient transfers using  $\mu$ DMA
  - Separate channels for transmit and receive
  - Receive single request asserted when data is in the FIFO; burst request asserted at programmed FIFO level
  - Transmit single request asserted when there is space in the FIFO; burst request asserted at programmed FIFO level
- The Global Alternate Clock (ALTCLK) resource or System Clock (SYSCLK) can be used to generate the baud clock

#### 6.5.6.5 Inter-Integrated Circuit (I<sup>2</sup>C)

The I<sup>2</sup>C bus provides bidirectional data transfer through a 2-wire design (a serial data line SDA and a serial clock line SCL). The I<sup>2</sup>C bus interfaces to external I<sup>2</sup>C devices such as serial memory (RAMs and ROMs), networking devices, LCDs, tone generators, and so on. The I<sup>2</sup>C bus can also be used for system testing and diagnostic purposes in product development and manufacture.

Each device on the I<sup>2</sup>C bus can be designated as either a master or a slave. The I<sup>2</sup>C module supports both sending and receiving data as either a master or a slave and can operate simultaneously as both a master and a slave. Both the I<sup>2</sup>C master and slave can generate interrupts.

The I<sup>2</sup>C modules include the following features:

- Devices on the I<sup>2</sup>C bus can be designated as either a master or a slave
  - Supports both transmitting and receiving data as either a master or a slave
  - Supports simultaneous master and slave operation
- Four I<sup>2</sup>C modes
  - Master transmit
  - Master receive
  - Slave transmit
  - Slave receive
- Two 8-entry FIFOs for receive and transmit data
  - FIFOs can be independently assigned to master or slave
- Four transmission speeds:
  - Standard (100 kbps)
  - Fast-mode (400 kbps)
  - Fast-mode plus (1 Mbps)
  - High-speed mode (3.33 Mbps)
- Glitch suppression
- SMBus support through software
  - Clock low time-out interrupt
  - Dual slave address capability
  - Quick command capability
- Master and slave interrupt generation
  - Master generates interrupts when a transmit or receive operation completes (or aborts due to an error)
  - Slave generates interrupts when data has been transferred or requested by a master or when a START or STOP condition is detected
- Master with arbitration and clock synchronization, multiple-master support, and 7-bit addressing mode
- Efficient transfers using  $\mu$ DMA
  - Separate channels for transmit and receive
  - Ability to execute single data transfers or burst data transfers using the RX and TX FIFOs in the I<sup>2</sup>C

#### 6.5.6.6 Quad Synchronous Serial Interface (QSSI)

QSSI is a bidirectional communications interface that converts data between parallel and serial. The QSSI module performs serial-to-parallel conversion on data received from a peripheral device and performs parallel-to-serial conversion on data transmitted to a peripheral device. The QSSI module can be configured as either a master or slave device. As a slave device, the QSSI module can also be configured to disable its output, which allows a master device to be coupled with multiple slave devices. The TX and RX paths are buffered with separate internal FIFOs.

The QSSI module also includes a programmable bit rate clock divider and prescaler to generate the output serial clock derived from the input clock of the QSSI module. Bit rates are generated based on the input clock, and the maximum bit rate is determined by the connected peripheral.

The four QSSI modules each support the following features:

- Four QSSI channels with advanced, bi-SSI, and quad-SSI functionality
- Programmable interface operation for Freescale SPI or TI synchronous serial interfaces in legacy mode. Support for Freescale interface in Bi- and Quad-SSI mode.
- Master or slave operation
- Programmable clock bit rate and prescaler
- Separate transmit and receive FIFOs, each 16 bits wide and 8 locations deep
- Programmable data frame size from 4 to 16 bits
- Internal loopback test mode for diagnostic/debug testing
- Standard FIFO-based interrupts and end-of-transmission interrupt
- Efficient transfers using  $\mu$ DMA
  - Separate channels for transmit and receive
  - Receive single request asserted when data is in the FIFO; burst request asserted when FIFO contains four entries
  - Transmit single request asserted when there is space in the FIFO; burst request asserted when four or more entries are available to be written in the FIFO
  - Maskable  $\mu$ DMA interrupts for receive and transmit complete
- Global alternate clock (ALTCLK) resource or system clock (SYSCLK) can be used to generate baud clock.

#### 6.5.7 System Integration

A variety of standard system functions are integrated into the device, including:

- Direct memory access (DMA) controller (see [节 6.5.7.1](#))
- System control and clocks including on-chip precision 16-MHz oscillator (see [节 6.5.7.2](#))
- Eight 32-bit timers (each timer can be configured as two 16-bit timers) (see [节 6.5.7.3](#))
- Lower-power battery-backed Hibernation module (see [节 6.5.7.5](#))
- RTC in Hibernation module
- Two watchdog timers (see [节 6.5.7.6](#))
  - One timer runs off the main oscillator.
  - One timer runs off the precision internal oscillator.
- 90 GPIOs, depending on configuration (see [节 6.5.7.7](#))
  - Highly flexible pin multiplexing allows use as GPIO or one of several peripheral functions.
  - GPIOs are independently configurable to 2-, 4-, 8-, 10-, or 12-mA drive capability.
  - Up to 4 GPIOs can have 18-mA drive capability.

### 6.5.7.1 Direct Memory Access (DMA)

The DMA controller is known as micro-DMA ( $\mu$ DMA). The  $\mu$ DMA controller provides a way to offload data transfer tasks from the Cortex-M4F processor, allowing for more efficient use of the processor and the available bus bandwidth. The  $\mu$ DMA controller can perform transfers between memory and peripherals. It has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory as the peripheral is ready to transfer more data. The  $\mu$ DMA controller provides the following features:

- Arm PrimeCell 32-channel configurable  $\mu$ DMA controller
- Support for memory-to-memory, memory-to-peripheral, and peripheral-to-memory in multiple transfer modes
  - Basic for simple transfer scenarios
  - Ping-pong for continuous data flow
  - Scatter-gather for a programmable list of up to 256 arbitrary transfers initiated from one request
- Highly flexible and configurable channel operation
  - Independently configured and operated channels
  - Dedicated channels for supported on-chip modules
  - Flexible channel assignments
  - One channel each for receive and transmit path for bidirectional modules
  - Dedicated channel for software-initiated transfers
  - Per-channel configurable priority scheme
  - Optional software-initiated requests for any channel
- Two levels of priority
- Design optimizations for improved bus access performance between  $\mu$ DMA controller and the processor core
  - $\mu$ DMA controller access is subordinate to core access
  - RAM striping
  - Peripheral bus segmentation
- Data sizes of 8, 16, and 32 bits
- Transfer size is programmable in binary steps from 1 to 1024
- Source and destination address increment size of byte, halfword, word, or no increment
- Maskable peripheral requests
- Interrupt on transfer completion, with a separate interrupt per channel

Each DMA channel has up to nine possible assignments that are selected using the DMA Channel Map Select n (DMACHMAPn) registers with 4-bit assignment fields for each  $\mu$ DMA channel.

表 6-2 lists the  $\mu$ DMA channel mapping. The Encoding column lists the encoding for the respective DMACHMAPn bit field. Encodings 0x9 to 0xF are reserved. The Type column indicates if a particular peripheral uses a single request (S), burst request (B), or either (SB).

### 注

Channels or encodings marked as Reserved cannot be used for  $\mu$ DMA transfers. Channels designated in the table as only "Software" are dedicated software channels. When only one software request is required in an application, dedicated software channels can be used. If multiple software requests in code are required, then peripheral channel software requests should be used for proper  $\mu$ DMA completion acknowledgement.

表 6-2.  $\mu$ DMA Channel Assignments

| Channel | Encoding   |      |                  |      |            |      |            |      |            |      |                |      |            |      |            |      |            |      |
|---------|------------|------|------------------|------|------------|------|------------|------|------------|------|----------------|------|------------|------|------------|------|------------|------|
|         | 0          |      | 1                |      | 2          |      | 3          |      | 4          |      | 5              |      | 6          |      | 7          |      | 8          |      |
|         | Peripheral | Type | Peripheral       | Type | Peripheral | Type | Peripheral | Type | Peripheral | Type | Peripheral     | Type | Peripheral | Type | Peripheral | Type | Peripheral | Type |
| 0       | Reserved   | –    | UART2 RX         | SB   | Reserved   | –    | GPTimer 4A | B    | Reserved   | –    | Reserved       | –    | I2C0 RX    | SB   | Reserved   | –    | Reserved   | –    |
| 1       | Reserved   | –    | UART2 TX         | SB   | Reserved   | –    | GPTimer 4B | B    | Reserved   | –    | Reserved       | –    | I2C0 TX    | SB   | Reserved   | –    | Reserved   | –    |
| 2       | Reserved   | –    | GPTimer 3A       | B    | Reserved   | –    | Reserved   | –    | Reserved   | –    | Reserved       | –    | I2C1RX     | SB   | Reserved   | –    | Reserved   | –    |
| 3       | Reserved   | –    | GPTimer 3B       | B    | Reserved   | –    | Software   | S    | Reserved   | –    | Reserved       | –    | I2C1 TX    | SB   | Reserved   | –    | Reserved   | –    |
| 4       | Reserved   | –    | GPTimer 2A       | B    | Reserved   | –    | GPIO A     | B    | Reserved   | –    | SHA/MD5 0 Cin  | B    | I2C2 RX    | SB   | Reserved   | –    | Reserved   | –    |
| 5       | Reserved   | –    | GPTimer 2B       | B    | Reserved   | –    | GPIO B     | B    | Reserved   | –    | SHA/MD5 0 Din  | B    | I2C2 TX    | SB   | Reserved   | –    | Reserved   | –    |
| 6       | Reserved   | –    | GPTimer 2A       | B    | UART5 RX   | SB   | GPIO C     | B    | I2C0 RX    | SB   | SHA/MD5 0 Cout | B    | Reserved   | –    | Reserved   | –    | Reserved   | –    |
| 7       | Reserved   | –    | GPTimer 2B       | B    | UART5 TX   | SB   | GPIO D     | B    | I2C0 TX    | SB   | Reserved       | –    | Reserved   | –    | Reserved   | –    | Reserved   | –    |
| 8       | UART0 RX   | SB   | UART1 RX         | SB   | Reserved   | –    | GPTimer 5A | B    | I2C1RX     | SB   | Reserved       | –    | Reserved   | –    | Reserved   | –    | Reserved   | –    |
| 9       | UART0 TX   | SB   | UART1 TX         | SB   | Reserved   | –    | GPTimer 5B | B    | I2C1 TX    | SB   | Reserved       | –    | Reserved   | –    | Reserved   | –    | Reserved   | –    |
| 10      | SSIO RX    | SB   | SSI1 RX          | SB   | UART6 RX   | SB   | Reserved   | –    | I2C2 RX    | SB   | Reserved       | –    | Reserved   | –    | GPTimer 6A | B    | Reserved   | –    |
| 11      | SSIO TX    | SB   | SSI1 TX          | SB   | UART6 TX   | SB   | Reserved   | –    | I2C2 TX    | SB   | Reserved       | –    | Reserved   | –    | GPTimer 6B | B    | Reserved   | –    |
| 12      | Reserved   | –    | UART2 RX         | SB   | SSI2 RX    | SB   | Reserved   | –    | GPIO K     | B    | AES0 Cin       | B    | Reserved   | –    | GPTimer 7A | B    | Reserved   | –    |
| 13      | Reserved   | –    | UART2 TX         | SB   | SSI2 TX    | SB   | Reserved   | –    | GPIO L     | B    | AES0 Cout      | B    | Reserved   | –    | GPTimer 7B | B    | Reserved   | –    |
| 14      | ADC0 SS0   | SB   | GPTimer 2A       | B    | SSI3 RX    | SB   | GPIO E     | B    | GPIO M     | B    | AES0 Din       | B    | Reserved   | –    | Reserved   | –    | Reserved   | –    |
| 15      | ADC0 SS1   | SB   | GPTimer 2B       | B    | SSI3 TX    | SB   | GPIO F     | B    | GPIO N     | B    | AES0 Dout      | B    | Reserved   | –    | Reserved   | –    | Reserved   | –    |
| 16      | ADC0 SS2   | SB   | Reserved         | –    | UART3 RX   | SB   | Reserved   | –    | GPIO P     | B    | Reserved       | –    | Reserved   | –    | Reserved   | –    | Reserved   | –    |
| 17      | ADC0 SS3   | SB   | Reserved         | –    | UART3 TX   | SB   | Reserved   | –    | Reserved   | –    | Reserved       | –    | Reserved   | –    | Reserved   | –    | Reserved   | –    |
| 18      | GPTimer 0A | B    | GPTimer 1A       | B    | UART4 RX   | SB   | GPIO B     | B    | I2C3 RX    | SB   | Reserved       | –    | Reserved   | –    | Reserved   | –    | Reserved   | –    |
| 19      | GPTimer 0B | B    | GPTimer 1B       | B    | UART4 TX   | SB   | GPIO G     | B    | I2C3 TX    | SB   | Reserved       | –    | Reserved   | –    | Reserved   | –    | Reserved   | –    |
| 20      | GPTimer 1A | B    | EPI0 RX Software | B    | UART7 RX   | SB   | GPIO H     | B    | I2C4 RX    | SB   | DES0 Cin       | B    | Reserved   | –    | Reserved   | –    | Reserved   | –    |
| 21      | GPTimer 1B | B    | EPI0 TX Software | B    | UART7 TX   | SB   | GPIO J     | B    | I2C4 TX    | SB   | DES0 Din       | B    | Reserved   | –    | Reserved   | –    | Reserved   | –    |
| 22      | UART1 RX   | SB   | Software         | B    | Reserved   | –    | Software   | B    | I2C5 RX    | SB   | DES0 Dout      | B    | Reserved   | –    | Reserved   | –    | I2C8 RX    | B    |
| 23      | UART1 TX   | SB   | Software         | B    | Reserved   | –    | Software   | B    | I2C5 TX    | SB   | Reserved       | –    | Reserved   | –    | Reserved   | –    | I2C8 TX    | B    |
| 24      | SSI1 RX    | SB   | ADC1 SS0         | SB   | Reserved   | –    | Reserved   | –    | GPIO Q     | B    | Reserved       | –    | Reserved   | –    | Reserved   | –    | I2C9 RX    | B    |
| 25      | SSI1 TX    | SB   | ADC1 SS1         | SB   | Reserved   | –    | Reserved   | –    | Reserved   | –    | Reserved       | –    | Reserved   | –    | Reserved   | –    | I2C9 TX    | B    |

表 6-2.  $\mu$ DMA Channel Assignments (continued)

| Channel | Encoding   |      |            |      |            |      |            |      |            |      |            |      |            |      |            |      |            |      |
|---------|------------|------|------------|------|------------|------|------------|------|------------|------|------------|------|------------|------|------------|------|------------|------|
|         | 0          |      | 1          |      | 2          |      | 3          |      | 4          |      | 5          |      | 6          |      | 7          |      | 8          |      |
|         | Peripheral | Type | Peripheral | Type | Peripheral | Type | Peripheral | Type | Peripheral | Type | Peripheral | Type | Peripheral | Type | Peripheral | Type | Peripheral | Type |
| 26      | Software   | B    | ADC1 SS2   | SB   | Reserved   | –    | Reserved   | –    | Reserved   | –    | Reserved   | –    | Reserved   | –    | Reserved   | –    | I2C6 RX    | B    |
| 27      | Software   | B    | ADC1 SS3   | SB   | Reserved   | –    | Reserved   | –    | Reserved   | –    | Reserved   | –    | Reserved   | –    | Reserved   | –    | I2C6 TX    | B    |
| 28      | Reserved   | –    | Reserved   | –    | Reserved   | –    | Reserved   | –    | Reserved   | –    | Reserved   | –    | Reserved   | –    | Reserved   | –    | I2C7 RX    | B    |
| 29      | Reserved   | –    | Reserved   | –    | Reserved   | –    | Reserved   | –    | Reserved   | –    | Reserved   | –    | Reserved   | –    | Reserved   | –    | I2C7 TX    | B    |
| 30      | Software   | B    | Software   | B    | Reserved   | –    | Software   | B    | Reserved   | –    | Reserved   | –    | Reserved   | –    | EPI0 RX    | B    | Reserved   | –    |
| 31      | Reserved   | –    | Reserved   | –    | Reserved   | –    | Reserved   | B    | Reserved   | –    | Reserved   | –    | Reserved   | –    | EPI0 TX    | B    | Reserved   | –    |

### 6.5.7.2 System Control and Clocks

System control determines the overall operation of the device. It provides information about the device, controls power-saving features, controls the clocking of the device and individual peripherals, and handles reset detection and reporting.

- Device identification information: version, part number, SRAM size, flash memory size, and so on
- Power control
  - On-chip fixed low dropout (LDO) voltage regulator
  - Hibernation module manages the power-up and power-down 3.3-V sequencing and control for the core digital logic and analog circuits
  - Low-power options for MCU: sleep and deep-sleep modes with clock gating
  - Low-power options for on-chip modules: software controls shutdown of individual peripherals and memory
  - 3.3-V supply brownout detection and reporting through interrupt or reset
- Multiple clock sources for the system clock. The MCU is clocked by the system clock (SYSCLK) that is distributed to the processor and integrated peripherals after clock gating. The SYSCLK frequency is based on the frequency of the clock source and a divisor factor. A PLL is provided for the generation of system clock frequencies in excess of the reference clock provided. The reference clocks for the PLL are the PIOSC and the main crystal oscillator. The following clock sources are provided to the MCU:
  - 16-MHz precision oscillator (PIOSC)
  - Main oscillator (MOSC): A frequency-accurate clock source by one of two means: an external single-ended clock source is connected to the OSC0 input pin, or an external crystal is connected across the OSC0 input and OSC1 output pins.
  - Low-frequency internal oscillator (LFIOSC): On-chip resource used during power-saving modes.
  - Hibernate RTC oscillator (RTCOSC): A clock that can be configured to be the 32.768-kHz external oscillator source from the HIB module or the HIB low-frequency clock source (HIB LFIOSC), which is in the HIB module.
- Flexible reset sources
  - Power-on reset (POR)
  - Reset pin assertion
  - Brownout reset (BOR) detector alerts to system power drops
  - Software reset
  - Watchdog timer reset
  - Hibernation module event
  - MOSC failure
- 128-bit unique identifier for individual device identification

### 6.5.7.3 Programmable Timers

Programmable timers can be used to count or time external events that drive the Timer input pins. Each 16- or 32-bit General-Purpose Timer Module (GPTM) block provides two 16-bit timers/counters that can be configured to operate independently as timers or event counters. These two timers/counters can also be configured to operate as one 32-bit timer or one 32-bit RTC. Timers can also be used to trigger analog-to-digital conversions and DMA transfers.

The GPTM contains eight 16- or 32-bit GPTM blocks with the following functional options:

- Operating modes
  - 16- or 32-bit programmable one-shot timer
  - 16- or 32-bit programmable periodic timer
  - 16-bit general-purpose timer with an 8-bit prescaler
  - 32-bit RTC when using an external 32.768-kHz clock as the input
  - 16-bit input-edge count- or time-capture modes with an 8-bit prescaler
  - 16-bit PWM mode with an 8-bit prescaler and software-programmable output inversion of the PWM signal
- Count up or down
- Sixteen 16- or 32-bit capture/compare PWM (CCP) pins
- Daisy-chaining of timer modules lets one timer initiate multiple timing events
- Timer synchronization lets selected timers start counting on the same clock cycle
- ADC event trigger
- User-enabled stalling when the MCU asserts the CPU halt flag during debug (excluding RTC mode)
- Can determine the elapsed time between the assertion of the timer interrupt and entry into the ISR
- Efficient transfers using  $\mu$ DMA
  - Dedicated channel for each timer
  - Burst request generated on timer interrupt

#### 6.5.7.4 Capture Compare PWM (CCP) Pins

CCP pins can be used by the General-Purpose Timer module to time or count external events using the CCP pin as an input. Alternatively, the GPTM can generate a simple PWM output on the CCP pin.

The 16/32-bit CCP pins can be programmed to operate in the following modes:

- Capture: The GP timer is incremented or decremented by programmed events on the CCP input. The GP timer captures and stores the current timer value when a programmed event occurs.
- Compare: The GP timer is incremented or decremented by programmed events on the CCP input. The GP timer compares the current value with a stored value and generates an interrupt when a match occurs.
- PWM: The GP timer is incremented or decremented by the system clock. A PWM signal is generated based on a match between the counter value and a value stored in a match register and is output on the CCP pin.

#### 6.5.7.5 Hibernation (HIB) Module

The HIB module provides logic to switch power off to the main processor and peripherals and to wake on external or time-based events. The HIB module includes power-sequencing logic and has the following features:

- 32-bit RTC with 1/32768-second resolution and a 15-bit subseconds counter
  - 32-bit RTC seconds match register and a 15-bit subseconds match for timed wakeup and interrupt generation with 1/32768-second resolution
  - RTC predivider trim for making fine adjustments to the clock rate
- Hardware calendar function
  - Year, month, day, day of week, hours, minutes, and seconds
  - Four-year leap compensation
  - 24-hour or AM and PM configuration
- Two mechanisms for power control
  - System power control using a discrete external regulator
  - On-chip power control using internal switches under register control
- $V_{DD}$  supplies power when valid, even if  $V_{BAT} > V_{DD}$

- Dedicated pin for wake using an external signal
- Can configure the external reset ( $\overline{\text{RST}}$ ) pin or up to four GPIO port pins as wake sources, with programmable wake level
- Tamper functionality
  - Support for four tamper inputs
  - Configurable level, weak pullup, and glitch filter
  - Configurable tamper event response
  - Logging of up to four tamper events
  - Optional BBRAM erase on tamper detection
  - Tamper detection and wake-from-hibernate capability
  - Hibernation clock input failure detect with a switch to the internal oscillator on detection
- RTC operational and hibernation memory valid as long as  $V_{\text{DD}}$  or  $V_{\text{BAT}}$  is valid
- Low-battery detection, signaling, and interrupt generation, with optional wake on low battery
- GPIO pin state can be retained during hibernation
- Clock source from an internal low-frequency oscillator (HIB LFIOOSC) or a 32.768-kHz external crystal or oscillator
- Sixteen 32-bit words of battery-backed memory to save state during hibernation
- Programmable interrupts for:
  - RTC match
  - External wake
  - Low battery

#### 6.5.7.6 Watchdog Timers

A watchdog timer is used to regain control when a system has failed due to a software error or to the failure of an external device to respond in the expected way. The watchdog timer can generate an interrupt, a nonmaskable interrupt, or a reset when a time-out value is reached. In addition, the watchdog timer is Arm FiRM-compliant and can be configured to generate an interrupt to the MCU on its first time-out, and to generate a reset signal on its second time-out. After the watchdog timer has been configured, the lock register can be written to prevent inadvertently altering the timer configuration.

Two watchdog timer modules are supported: Watchdog Timer 0 uses the system clock for its timer clock; Watchdog Timer 1 uses the PIOOSC as its timer clock. The watchdog timer module has the following features:

- 32-bit down counter with a programmable load register
- Separate watchdog clock with an enable
- Programmable interrupt generation logic with interrupt masking and optional NMI function
- Lock register protection from runaway software
- Reset generation logic with an enable/disable
- User-enabled stalling when the MCU asserts the CPU Halt flag during debug

#### 6.5.7.7 Programmable GPIOs

General-purpose input/output (GPIO) pins offer flexibility for a variety of connections. The GPIO module is composed of 15 physical GPIO blocks, each corresponding to an individual GPIO port. The GPIO module is FiRM-compliant (compliant to the Arm Foundation IP for Real-Time MCUs specification) and supports 0 to 90 programmable I/O pins. The number of GPIOs available depends on the peripherals being used.

- Up to 90 GPIOs, depending on configuration
- Highly flexible pin multiplexing allows use as GPIO or one of several peripheral functions
- 3.3-V tolerant in input configuration

- Advanced high-performance bus (AHB) accesses all ports:
  - Ports A to H, K to N, P, and Q
- Fast toggle capable of a change every clock cycle for ports on AHB
- Programmable control for GPIO interrupts
  - Interrupt generation masking
  - Edge-triggered on rising, falling, or both
  - Level-sensitive on high or low values
  - Per-pin interrupts available on port P and port Q
- Bit masking in both read and write operations through address lines
- Can be used to initiate an ADC sample sequence or a  $\mu$ DMA transfer
- Pin state can be retained during hibernation mode; pins on port P can be programmed to wake on level in hibernation mode
- Pins configured as digital inputs are Schmitt triggered
- Programmable control for GPIO pad configuration
  - Weak pullup or pulldown resistors
  - 2-, 4-, 6-, 8-, 10-, or 12-mA pad drive for digital communication; up to four pads can sink 18-mA for high-current applications
  - Slew rate control for 8-, 10-, and 12-mA pad drive
  - Open-drain enables
  - Digital-input enables

### 6.5.8 Advanced Motion Control

The motion control functions that are integrated into the device support the following features:

- Eight advanced PWM outputs for motion and energy applications
- Four fault inputs to promote low-latency shutdown
- One quadrature encoder input (QEI)

The following sections provides more detail on these motion control functions.

#### 6.5.8.1 Pulse Width Modulation (PWM)

PWM is a powerful technique for digitally encoding analog signal levels. High-resolution counters are used to generate a square wave, and the duty cycle of the square wave is modulated to encode an analog signal. Typical applications include switching power supplies and motor control.

One PWM module is included, with four PWM generator blocks and a control block, for a total of eight PWM outputs. Each PWM generator block contains one timer (16-bit down or up/down counter), two comparators, a PWM signal generator, a dead-band generator, and an interrupt or ADC-trigger selector.

Each PWM generator block produces two PWM signals that can be either independent signals or a pair of complementary signals with dead-band delays inserted.

Each PWM generator has the following features:

- Four fault-condition handling inputs to quickly provide low-latency shutdown and prevent damage to the motor being controlled
- One 16-bit counter
  - Runs in down or up/down mode
  - Output frequency controlled by a 16-bit load value
  - Synchronized load value updates
  - Produces output signals at zero and load value

- Two PWM comparators
  - Synchronized comparator value updates
  - Produces output signals on match
- PWM signal generator
  - Output PWM signal is constructed based on actions taken as a result of the counter and PWM comparator output signals.
  - Produces two independent PWM signals
- Dead-band generator
  - Produces two PWM signals with programmable dead-band delays suitable for driving a half-H bridge
  - Can be bypassed, leaving input PWM signals unmodified
- Can initiate an ADC sample sequence

The control block determines the polarity of the PWM signals and which signals are passed through to the pins. The output of the PWM generation blocks are managed by the output control block before being passed to the device pins. The PWM control block has the following options:

- PWM output enable of each PWM signal
- Optional output inversion of each PWM signal (polarity control)
- Optional fault handling for each PWM signal
- Synchronization of timers in the PWM generator blocks
- Synchronization of timer/comparator updates across the PWM generator blocks
- Extended PWM synchronization of timer/comparator updates across the PWM generator blocks
- Interrupt status summary of the PWM generator blocks
- Extended PWM fault handling, with multiple fault signals, programmable polarities, and filtering
- PWM generators can be operated independently or synchronized with other generators

#### 6.5.8.2 Quadrature Encoder With Index (QEI) Module

A quadrature encoder, also known as a 2-channel incremental encoder, converts linear displacement into a pulse signal. By monitoring both the number of pulses and the relative phase of the two signals, the position, direction of rotation, and speed can be tracked. In addition, a third channel, or index signal, can be used to reset the position counter. The QEI module interprets the code produced by a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, it can capture a running estimate of the velocity of the encoder wheel. The input frequency of the QEI inputs may be as high as 1/4 of the system frequency (for example, 30 MHz for a 120-MHz system).

One QEI module provides control of one motor with the following features:

- Position integrator that tracks the encoder position
- Programmable noise filter on the inputs
- Velocity capture using built-in timer
- The input frequency of the QEI inputs may be as high as 1/4 of the system frequency (for example, 12.5 MHz for a 50-MHz system)
- Interrupt generation on:
  - Index pulse
  - Velocity-timer expiration
  - Direction change
  - Quadrature error detection

#### 6.5.9 Analog

Integrated analog functions include:

- Two 12-bit ADCs with a total of 20 analog input channels and each with a sample rate of 2 Msps (see [节 6.5.9.1](#))
- Three analog comparators (see [节 6.5.9.2](#))
- On-chip voltage regulator

#### 6.5.9.1 ADC

An ADC is a peripheral that converts a continuous analog voltage to a discrete digital number. The ADC module features 12-bit conversion resolution and supports 20 input channels plus an internal temperature sensor. Four buffered sample sequencers allow rapid sampling of up to 20 analog input sources without controller intervention. Each sample sequencer provides flexible programming with fully configurable input source, trigger events, interrupt generation, and sequencer priority. Each ADC module has a digital comparator function that lets the conversion value be sent to a comparison unit that provides eight digital comparators.

Both ADC modules support the following features:

- 20 shared analog input channels
- 12-bit precision ADC
- Single-ended and differential-input configurations
- On-chip internal temperature sensor
- Maximum sample rate of two million samples/second
- Optional, programmable phase delay
- Sample and hold window programmability
- Four programmable sample conversion sequencers from one to eight entries long, with corresponding conversion result FIFOs
- Flexible trigger control
  - Controller (software)
  - Timers
  - Analog comparators
  - PWM
  - GPIO
- Hardware averaging of up to 64 samples
- Eight digital comparators
- Converter uses two external reference signals (VREFA+ and VREFA–) or VDDA and GNDA as the voltage reference
- Power and ground for the analog circuitry is separate from the digital power and ground
- Efficient transfers using  $\mu$ DMA
  - Dedicated channel for each sample sequencer
  - ADC module uses burst requests for DMA
- Global Alternate Clock (ALTCLK) resource or System Clock (SYSCLK) can be used to generate ADC clock.

#### 6.5.9.2 Analog Comparators

An analog comparator is a peripheral that compares two analog voltages and provides a logical output that signals the comparison result. The independent integrated analog comparators can be configured to drive an output or generate an interrupt or ADC event.

The comparator can provide its output to a device pin, acting as a replacement for an analog comparator on the board, or it can be used to signal the application via interrupts or triggers to the ADC to cause it to start capturing a sample sequence. The interrupt generation and ADC triggering logic is separate. This means, for example, that an interrupt can be generated on a rising edge and the ADC triggered on a falling edge.

Each analog comparator supports the following functions:

- Compare external pin input to external pin input or to internal programmable voltage reference
- Compare a test voltage against any one of the following voltages:
  - An individual external reference voltage
  - A shared single external reference voltage
  - A shared internal reference voltage

### 6.5.10 JTAG and Arm Serial Wire Debug

The Joint Test Action Group (JTAG) port is an IEEE standard that defines a Test Access Port (TAP) and Boundary Scan Architecture for digital integrated circuits and provides a standardized serial interface for controlling the associated test logic. The TAP, Instruction Register (IR), and Data Register (DR) can be used to test the interconnections of assembled printed circuit boards and obtain manufacturing information on the components. The JTAG port also provides a means of accessing and controlling design-for-test features such as I/O pin observation and control, scan testing, and debugging. TI replaces the Arm SW-DP and JTAG-DP with the Arm Serial Wire JTAG Debug Port (SWJ-DP) interface. The SWJ-DP interface combines the SWD and JTAG debug ports into one module. This module provides the standard JTAG debug and test functionality plus real-time access to system memory without halting the core or requiring any target resident code. The SWJ-DP interface has the following features:

- IEEE 1149.1-1990 compatible TAP controller
- Four-bit IR chain for storing JTAG instructions
- IEEE standard instructions: BYPASS, IDCODE, SAMPLE/PRELOAD, and EXTEST
- Arm additional instructions: APACC, DPACC, and ABORT
- Integrated Arm Serial Wire Debug (SWD)
  - Serial Wire JTAG Debug Port (SWJ-DP)
  - Flash Patch and Breakpoint (FPB) unit for implementing breakpoints
  - Data Watchpoint and Trace (DWT) unit for implementing watchpoints, trigger resources, and system profiling
  - Instrumentation Trace Macrocell (ITM) for support of printf-style debugging
  - Embedded Trace Macrocell (ETM) for instruction trace capture
  - Trace Port Interface Unit (TPIU) for bridging to a Trace Port Analyzer

### 6.5.11 Peripheral Memory Map

表 6-3 lists the address for each peripheral.

注

Within the memory map, attempts to read or write addresses in reserved spaces result in a bus fault. In addition, attempts to write addresses in the flash range also result in a bus fault.

表 6-3. Memory Map

| START       | END         | DESCRIPTION      | REGISTERS |
|-------------|-------------|------------------|-----------|
| 0x4000.0000 | 0x4000.0FFF | Watchdog Timer 0 | 表 6-32    |
| 0x4000.1000 | 0x4000.1FFF | Watchdog Timer 1 | 表 6-32    |
| 0x4000.2000 | 0x4000.3FFF | Reserved         |           |

表 6-3. Memory Map (continued)

| START       | END         | DESCRIPTION       | REGISTERS              |
|-------------|-------------|-------------------|------------------------|
| 0x4000.4000 | 0x4000.4FFF | GPIO Port A       | <a href="#">表 6-17</a> |
| 0x4000.5000 | 0x4000.5FFF | GPIO Port B       | <a href="#">表 6-17</a> |
| 0x4000.6000 | 0x4000.6FFF | GPIO Port C       | <a href="#">表 6-17</a> |
| 0x4000.7000 | 0x4000.7FFF | GPIO Port D       | <a href="#">表 6-17</a> |
| 0x4000.8000 | 0x4000.8FFF | SSI0              | <a href="#">表 6-25</a> |
| 0x4000.9000 | 0x4000.9FFF | SSI1              | <a href="#">表 6-25</a> |
| 0x4000.A000 | 0x4000.AFFF | SSI2              | <a href="#">表 6-25</a> |
| 0x4000.B000 | 0x4000.BFFF | SSI3              | <a href="#">表 6-25</a> |
| 0x4000.C000 | 0x4000.CFFF | UART0             | <a href="#">表 6-30</a> |
| 0x4000.D000 | 0x4000.DFFF | UART1             | <a href="#">表 6-30</a> |
| 0x4000.E000 | 0x4000.EFFF | UART2             | <a href="#">表 6-30</a> |
| 0x4000.F000 | 0x4000.FFFF | UART3             | <a href="#">表 6-30</a> |
| 0x4001.0000 | 0x4001.0FFF | UART4             | <a href="#">表 6-30</a> |
| 0x4001.1000 | 0x4001.1FFF | UART5             | <a href="#">表 6-30</a> |
| 0x4001.2000 | 0x4001.2FFF | UART6             | <a href="#">表 6-30</a> |
| 0x4001.3000 | 0x4001.3FFF | UART7             | <a href="#">表 6-30</a> |
| 0x4001.4000 | 0x4001.FFFF | Reserved          |                        |
| 0x4002.0000 | 0x4002.0FFF | I2C 0             | <a href="#">表 6-20</a> |
| 0x4002.1000 | 0x4002.1FFF | I2C 1             | <a href="#">表 6-20</a> |
| 0x4002.2000 | 0x4002.2FFF | I2C 2             | <a href="#">表 6-20</a> |
| 0x4002.3000 | 0x4002.3FFF | I2C 3             | <a href="#">表 6-20</a> |
| 0x4002.4000 | 0x4002.4FFF | GPIO Port E       | <a href="#">表 6-17</a> |
| 0x4002.5000 | 0x4002.5FFF | GPIO Port F       | <a href="#">表 6-17</a> |
| 0x4002.6000 | 0x4002.6FFF | GPIO Port G       | <a href="#">表 6-17</a> |
| 0x4002.7000 | 0x4002.7FFF | GPIO Port H       | <a href="#">表 6-17</a> |
| 0x4002.8000 | 0x4002.8FFF | PWM 0             | <a href="#">表 6-23</a> |
| 0x4002.9000 | 0x4002.BFFF | Reserved          |                        |
| 0x4002.C000 | 0x4002.CFFF | QE10              | <a href="#">表 6-24</a> |
| 0x4002.D000 | 0x4002.FFFF | Reserved          |                        |
| 0x4003.0000 | 0x4003.0FFF | 16/32-bit Timer 0 | <a href="#">表 6-18</a> |
| 0x4003.1000 | 0x4003.1FFF | 16/32-bit Timer 1 | <a href="#">表 6-18</a> |
| 0x4003.2000 | 0x4003.2FFF | 16/32-bit Timer 2 | <a href="#">表 6-18</a> |
| 0x4003.3000 | 0x4003.3FFF | 16/32-bit Timer 3 | <a href="#">表 6-18</a> |
| 0x4003.4000 | 0x4003.4FFF | 16/32-bit Timer 4 | <a href="#">表 6-18</a> |
| 0x4003.5000 | 0x4003.5FFF | 16/32-bit Timer 5 | <a href="#">表 6-18</a> |
| 0x4003.6000 | 0x4003.7FFF | Reserved          |                        |
| 0x4003.8000 | 0x4003.8FFF | ADC0              | <a href="#">表 6-6</a>  |
| 0x4003.9000 | 0x4003.9FFF | ADC1              | <a href="#">表 6-6</a>  |
| 0x4003.A000 | 0x4003.BFFF | Reserved          |                        |
| 0x4003.C000 | 0x4003.CFFF | Analog Comparator | <a href="#">表 6-8</a>  |
| 0x4003.D000 | 0x4003.DFFF | GPIO Port J       | <a href="#">表 6-17</a> |
| 0x4003.E000 | 0x4003.FFFF | Reserved          |                        |
| 0x4004.0000 | 0x4004.0FFF | CAN0 Controller   | <a href="#">表 6-7</a>  |
| 0x4004.1000 | 0x4004.1FFF | CAN1 Controller   | <a href="#">表 6-7</a>  |
| 0x4004.2000 | 0x4004.FFFF | Reserved          |                        |
| 0x4005.0000 | 0x4005.0FFF | USB               | <a href="#">表 6-31</a> |
| 0x4005.1000 | 0x4005.7FFF | Reserved          |                        |

**表 6-3. Memory Map (continued)**

| START       | END         | DESCRIPTION                                         | REGISTERS              |
|-------------|-------------|-----------------------------------------------------|------------------------|
| 0x4005.8000 | 0x4005.8FFF | GPIO Port A (AHB aperture)                          | <a href="#">表 6-17</a> |
| 0x4005.9000 | 0x4005.9FFF | GPIO Port B (AHB aperture)                          | <a href="#">表 6-17</a> |
| 0x4005.A000 | 0x4005.AFFF | GPIO Port C (AHB aperture)                          | <a href="#">表 6-17</a> |
| 0x4005.B000 | 0x4005.BFFF | GPIO Port D (AHB aperture)                          | <a href="#">表 6-17</a> |
| 0x4005.C000 | 0x4005.CFFF | GPIO Port E (AHB aperture)                          | <a href="#">表 6-17</a> |
| 0x4005.D000 | 0x4005.DFFF | GPIO Port F (AHB aperture)                          | <a href="#">表 6-17</a> |
| 0x4005.E000 | 0x4005.EFFF | GPIO Port G (AHB aperture)                          | <a href="#">表 6-17</a> |
| 0x4005.F000 | 0x4005.FFFF | GPIO Port H (AHB aperture)                          | <a href="#">表 6-17</a> |
| 0x4006.0000 | 0x4006.0FFF | GPIO Port J (AHB aperture)                          | <a href="#">表 6-17</a> |
| 0x4006.1000 | 0x4006.1FFF | GPIO Port K (AHB aperture)                          | <a href="#">表 6-17</a> |
| 0x4006.2000 | 0x4006.2FFF | GPIO Port L (AHB aperture)                          | <a href="#">表 6-17</a> |
| 0x4006.3000 | 0x4006.3FFF | GPIO Port M (AHB aperture)                          | <a href="#">表 6-17</a> |
| 0x4006.4000 | 0x4006.4FFF | GPIO Port N (AHB aperture)                          | <a href="#">表 6-17</a> |
| 0x4006.5000 | 0x4006.5FFF | GPIO Port P (AHB aperture)                          | <a href="#">表 6-17</a> |
| 0x4006.6000 | 0x4006.6FFF | GPIO Port Q (AHB aperture)                          | <a href="#">表 6-17</a> |
| 0x4006.7000 | 0x400A.EFFF | Reserved                                            |                        |
| 0x400A.F000 | 0x400A.FFFF | EEPROM and Key Locker                               | <a href="#">表 6-12</a> |
| 0x400B.0000 | 0x400B.5FFF | Reserved                                            |                        |
| 0x400B.6000 | 0x400B.6FFF | Reserved                                            |                        |
| 0x400B.7000 | 0x400B.7FFF | Reserved                                            |                        |
| 0x400B.8000 | 0x400B.8FFF | I2C 8                                               | <a href="#">表 6-20</a> |
| 0x400B.9000 | 0x400B.9FFF | I2C 9                                               | <a href="#">表 6-20</a> |
| 0x400B.A000 | 0x400B.FFFF | Reserved                                            |                        |
| 0x400C.0000 | 0x400C.0FFF | I2C 4                                               | <a href="#">表 6-20</a> |
| 0x400C.1000 | 0x400C.1FFF | I2C 5                                               | <a href="#">表 6-20</a> |
| 0x400C.2000 | 0x400C.2FFF | I2C 6                                               | <a href="#">表 6-20</a> |
| 0x400C.3000 | 0x400C.3FFF | I2C 7                                               | <a href="#">表 6-20</a> |
| 0x400C.4000 | 0x400C.FFFF | Reserved                                            |                        |
| 0x400D.0000 | 0x400D.0FFF | EPI0                                                | <a href="#">表 6-13</a> |
| 0x400D.1000 | 0x400D.FFFF | Reserved                                            |                        |
| 0x400E.0000 | 0x400E.0FFF | 16/32-bit Timer 6                                   | <a href="#">表 6-18</a> |
| 0x400E.1000 | 0x400E.1FFF | 16/32-bit Timer 7                                   | <a href="#">表 6-18</a> |
| 0x400E.2000 | 0x400E.BFFF | Reserved                                            |                        |
| 0x400E.C000 | 0x400E.CFFF | Ethernet Controller                                 | <a href="#">表 6-14</a> |
| 0x400E.D000 | 0x400F.8FFF | Reserved                                            |                        |
| 0x400F.9000 | 0x400F.9FFF | System Exception                                    | <a href="#">表 6-29</a> |
| 0x400F.A000 | 0x400F.BFFF | Reserved                                            |                        |
| 0x400F.C000 | 0x400F.CFFF | Hibernation                                         | <a href="#">表 6-19</a> |
| 0x400F.D000 | 0x400F.DFFF | Flash Memory Control                                | <a href="#">表 6-16</a> |
| 0x400F.E000 | 0x400F.EFFF | System Control                                      | <a href="#">表 6-28</a> |
| 0x400F.F000 | 0x400F.FFFF | μDMA                                                | <a href="#">表 6-21</a> |
| 0x4010.0000 | 0x41FF.FFFF | Reserved                                            |                        |
| 0x4200.0000 | 0x43FF.FFFF | Bit-banded alias of 0x4000.0000 through 0x400F.FFFF |                        |
| 0x4400.0000 | 0x4402.FFFF | Reserved                                            |                        |
| 0x4403.0000 | 0x4403.0FFF | CRC and Cryptographic Control                       | <a href="#">表 6-9</a>  |
| 0x4403.1000 | 0x4403.1FFF | Reserved (4KB)                                      |                        |
| 0x4403.2000 | 0x4403.3FFF | Reserved (8KB)                                      |                        |

表 6-3. Memory Map (continued)

| START       | END         | DESCRIPTION                    | REGISTERS      |
|-------------|-------------|--------------------------------|----------------|
| 0x4403.4000 | 0x4403.5FFF | SHA/MD5                        | 表 6-26         |
| 0x4403.6000 | 0x4403.7FFF | AES                            | 表 6-4, 表 6-5   |
| 0x4403.8000 | 0x4403.9FFF | DES                            | 表 6-10, 表 6-11 |
| 0x4403.A000 | 0x4403.EFFF | Reserved                       |                |
| 0x4403.F000 | 0x4403.FFFF | Reserved (4KB)                 |                |
| 0x4404.0000 | 0x4404.FFFF | Reserved (64KB)                |                |
| 0x4405.0000 | 0x4405.0FFF | Reserved                       |                |
| 0x4405.1000 | 0x4405.3FFF | Reserved                       |                |
| 0x4405.4000 | 0x4405.4FFF | EPHY 0                         | 表 6-15         |
| 0x4405.5000 | 0x5FFF.FFFF | Reserved                       |                |
| 0x6000.0000 | 0xDFFF.FFFF | EPI0 Mapped Peripheral and RAM | 表 6-13         |

表 6-4. AES Registers

| OFFSET       | ACRONYM                          | REGISTER NAME                                                              |
|--------------|----------------------------------|----------------------------------------------------------------------------|
| 0x00C        | AES_KEY2_5                       | AES Key 2_5                                                                |
| 0x010        | AES_KEY2_2                       | AES Key 2_2                                                                |
| 0x014        | AES_KEY2_3                       | AES Key 2_3                                                                |
| 0x018        | AES_KEY2_0                       | AES Key 2_0                                                                |
| 0x01C        | AES_KEY2_1                       | AES Key 2_1                                                                |
| 0x020        | AES_KEY1_6                       | AES Key 1_6                                                                |
| 0x024        | AES_KEY1_7                       | AES Key 1_7                                                                |
| 0x028        | AES_KEY1_4                       | AES Key 1_4                                                                |
| 0x02C        | AES_KEY1_5                       | AES Key 1_5                                                                |
| 0x030        | AES_KEY1_2                       | AES Key 1_2                                                                |
| 0x034        | AES_KEY1_3                       | AES Key 1_3                                                                |
| 0x038        | AES_KEY1_0                       | AES Key 1_0                                                                |
| 0x03C        | AES_KEY1_1                       | AES Key 1_1                                                                |
| 0x40 to 0x4C | AES_IV_IN_0 to AES_IV_IN_3       | AES Initialization Vector Input 0 to AES Initialization Vector Input 3     |
| 0x50         | AES_CTRL                         | AES Control                                                                |
| 0x54 to 0x58 | AES_C_LENGTH_0 to AES_C_LENGTH_1 | AES Crypto Data Length 0 to AES Crypto Data Length 1                       |
| 0x5C         | AES_AUTH_LENGTH                  | AES Authentication Data Length                                             |
| 0x60 to 0x6C | AES_DATA_IN_0 to AES_DATA_IN_3   | AES Data R/W Plaintext/Ciphertext 0 to AES Data R/W Plaintext/Ciphertext 3 |
| 0x70 to 0x7C | AES_TAG_OUT_0 to AES_TAG_OUT_3   | AES Hash Tag Out 0 to AES Hash Tag Out 3                                   |
| 0x80         | AES_REVISION                     | AES IP Revision Identifier                                                 |
| 0x84         | AES_SYSCONFIG                    | AES System Configuration                                                   |
| 0x88         | AES_SYSSTATUS                    | AES System Status                                                          |
| 0x8C         | AES_IRQSTATUS                    | AES Interrupt Status                                                       |
| 0x90         | AES_IRQENABLE                    | AES Interrupt Enable                                                       |
| 0x94         | AES_DIRTYBITS                    | AES Dirty Bits                                                             |

表 6-5. AES μDMA Registers

| OFFSET | ACRONYM    | REGISTER NAME                   |
|--------|------------|---------------------------------|
| 0x20   | AES_DMAIM  | AES DMA Interrupt Mask          |
| 0x24   | AES_DMARIS | AES DMA Raw Interrupt Status    |
| 0x28   | AES_DMAMIS | AES DMA Masked Interrupt Status |

**表 6-5. AES  $\mu$ DMA Registers (continued)**

| OFFSET | ACRONYM   | REGISTER NAME           |
|--------|-----------|-------------------------|
| 0x2C   | AES_DMAIC | AES DMA Interrupt Clear |

**表 6-6. ADC Registers**

| OFFSET | ACRONYM     | REGISTER NAME                                           |
|--------|-------------|---------------------------------------------------------|
| 0x0    | ADCACTSS    | ADC Active Sample Sequencer                             |
| 0x4    | ADCRIS      | ADC Raw Interrupt Status                                |
| 0x8    | ADCIM       | ADC Interrupt Mask                                      |
| 0xC    | ADCISC      | ADC Interrupt Status and Clear                          |
| 0x10   | ADCOSTAT    | ADC Overflow Status                                     |
| 0x14   | ADCEMUX     | ADC Event Multiplexer Select                            |
| 0x18   | ADCUSTAT    | ADC Underflow Status                                    |
| 0x1C   | ADCTSSEL    | ADC Trigger Source Select                               |
| 0x20   | ADCSSPRI    | ADC Sample Sequencer Priority                           |
| 0x24   | ADCSPC      | ADC Sample Phase Control                                |
| 0x28   | ADCPSSI     | ADC Processor Sample Sequence Initiate                  |
| 0x30   | ADCSAC      | ADC Sample Averaging Control                            |
| 0x34   | ADCDCISC    | ADC Digital Comparator Interrupt Status and Clear       |
| 0x38   | ADCCTL      | ADC Control                                             |
| 0x40   | ADCSSMUX0   | ADC Sample Sequence Input Multiplexer Select 0          |
| 0x44   | ADCSSCTL0   | ADC Sample Sequence Control 0                           |
| 0x48   | ADCSSFIFO0  | ADC Sample Sequence Result FIFO 0                       |
| 0x4C   | ADCSSFSTAT0 | ADC Sample Sequence FIFO 0 Status                       |
| 0x50   | ADCSSOP0    | ADC Sample Sequence 0 Operation                         |
| 0x54   | ADCSSDC0    | ADC Sample Sequence 0 Digital Comparator Select         |
| 0x58   | ADCSEMUX0   | ADC Sample Sequence Extended Input Multiplexer Select 0 |
| 0x5C   | ADCSSSTSH0  | ADC Sample Sequence 0 Sample and Hold Time              |
| 0x60   | ADCSSMUX1   | ADC Sample Sequence Input Multiplexer Select 1          |
| 0x64   | ADCSSCTL1   | ADC Sample Sequence Control 1                           |
| 0x068  | ADCSSFIFO1  | ADC Sample Sequence Result FIFO 1                       |
| 0x06C  | ADCSSFSTAT1 | ADC Sample Sequence FIFO 1 Status                       |
| 0x70   | ADCSSOP1    | ADC Sample Sequence 1 Operation                         |
| 0x74   | ADCSSDC1    | ADC Sample Sequence 1 Digital Comparator Select         |
| 0x78   | ADCSEMUX1   | ADC Sample Sequence Extended Input Multiplexer Select 1 |
| 0x7C   | ADCSSSTSH1  | ADC Sample Sequence 1 Sample and Hold Time              |
| 0x080  | ADCSSMUX2   | ADC Sample Sequence Input Multiplexer Select 2          |
| 0x084  | ADCSSCTL2   | ADC Sample Sequence Control 2                           |
| 0x088  | ADCSSFIFO2  | ADC Sample Sequence Result FIFO 2                       |
| 0x08C  | ADCSSFSTAT2 | ADC Sample Sequence FIFO 2 Status                       |
| 0x090  | ADCSSOP2    | ADC Sample Sequence 2 Operation                         |
| 0x094  | ADCSSDC2    | ADC Sample Sequence 2 Digital Comparator Select         |
| 0x098  | ADCSEMUX2   | ADC Sample Sequence Extended Input Multiplexer Select 2 |
| 0x09C  | ADCSSSTSH2  | ADC Sample Sequence 2 Sample and Hold Time              |
| 0xA0   | ADCSSMUX3   | ADC Sample Sequence Input Multiplexer Select 3          |
| 0xA4   | ADCSSCTL3   | ADC Sample Sequence Control 3                           |
| 0x0A8  | ADCSSFIFO3  | ADC Sample Sequence Result FIFO 3                       |
| 0x0AC  | ADCSSFSTAT3 | ADC Sample Sequence FIFO 3 Status                       |
| 0xB0   | ADCSSOP3    | ADC Sample Sequence 3 Operation                         |

表 6-6. ADC Registers (continued)

| OFFSET         | ACRONYM                | REGISTER NAME                                                        |
|----------------|------------------------|----------------------------------------------------------------------|
| 0xB4           | ADCSSDC3               | ADC Sample Sequence 3 Digital Comparator Select                      |
| 0xB8           | ADCSEMUX3              | ADC Sample Sequence Extended Input Multiplexer Select 3              |
| 0xBC           | ADCSTSH3               | ADC Sample Sequence 3 Sample and Hold Time                           |
| 0xD00          | ADCDCRIC               | ADC Digital Comparator Reset Initial Conditions                      |
| 0xE00 to 0xE1C | ADCDCCTL0 to ADCDCCTL7 | ADC Digital Comparator Control 0 to ADC Digital Comparator Control 7 |
| 0xE40 to 0xE5C | ADCDCCMP0 to ADCDCCMP7 | ADC Digital Comparator Range 0 to ADC Digital Comparator Range 7     |
| 0xFC0          | ADCPP                  | ADC Peripheral Properties                                            |
| 0xFC4          | ADPC                   | ADC Peripheral Configuration                                         |
| 0xFC8          | ADCCC                  | ADC Clock Configuration                                              |

表 6-7. CAN Registers

| OFFSET | ACRONYM    | REGISTER NAME                     |
|--------|------------|-----------------------------------|
| 0x0    | CANCTL     | CAN Control                       |
| 0x4    | CANSTS     | CAN Status                        |
| 0x8    | CANERR     | CAN Error Counter                 |
| 0xC    | CANBIT     | CAN Bit Timing                    |
| 0x10   | CANINT     | CAN Interrupt                     |
| 0x14   | CANTST     | CAN Test                          |
| 0x18   | CANBRPE    | CAN Baud Rate Prescaler Extension |
| 0x20   | CANIF1CRQ  | CAN IF1 Command Request           |
| 0x24   | CANIF1CMSK | CAN IF1 Command Mask              |
| 0x28   | CANIF1MSK1 | CAN IF1 Mask 1                    |
| 0x2C   | CANIF1MSK2 | CAN IF1 Mask 2                    |
| 0x30   | CANIF1ARB1 | CAN IF1 Arbitration 1             |
| 0x34   | CANIF1ARB2 | CAN IF1 Arbitration 2             |
| 0x38   | CANIF1MCTL | CAN IF1 Message Control           |
| 0x3C   | CANIF1DA1  | CAN IF1 Data A1                   |
| 0x40   | CANIF1DA2  | CAN IF1 Data A2                   |
| 0x44   | CANIF1DB1  | CAN IF1 Data B1                   |
| 0x48   | CANIF1DB2  | CAN IF1 Data B2                   |
| 0x80   | CANIF2CRQ  | CAN IF2 Command Request           |
| 0x84   | CANIF2CMSK | CAN IF2 Command Mask              |
| 0x88   | CANIF2MSK1 | CAN IF2 Mask 1                    |
| 0x8C   | CANIF2MSK2 | CAN IF2 Mask 2                    |
| 0x90   | CANIF2ARB1 | CAN IF2 Arbitration 1             |
| 0x94   | CANIF2ARB2 | CAN IF2 Arbitration 2             |
| 0x98   | CANIF2MCTL | CAN IF2 Message Control           |
| 0x9C   | CANIF2DA1  | CAN IF2 Data A1                   |
| 0xA0   | CANIF2DA2  | CAN IF2 Data A2                   |
| 0xA4   | CANIF2DB1  | CAN IF2 Data B1                   |
| 0xA8   | CANIF2DB2  | CAN IF2 Data B2                   |
| 0x100  | CANTXRQ1   | CAN Transmission Request 1        |
| 0x104  | CANTXRQ2   | CAN Transmission Request 2        |
| 0x120  | CANNWDA1   | CAN New Data 1                    |
| 0x124  | CANNWDA2   | CAN New Data 2                    |
| 0x140  | CANMSG1INT | CAN Message 1 Interrupt Pending   |
| 0x144  | CANMSG2INT | CAN Message 2 Interrupt Pending   |

**表 6-7. CAN Registers (continued)**

| OFFSET | ACRONYM    | REGISTER NAME       |
|--------|------------|---------------------|
| 0x160  | CANMSG1VAL | CAN Message 1 Valid |
| 0x164  | CANMSG2VAL | CAN Message 2 Valid |

**表 6-8. Comparator Registers**

| OFFSET | ACRONYM  | REGISTER NAME                               |
|--------|----------|---------------------------------------------|
| 0x0    | ACMIS    | Analog Comparator Masked Interrupt Status   |
| 0x4    | ACRIS    | Analog Comparator Raw Interrupt Status      |
| 0x8    | ACINTEN  | Analog Comparator Interrupt Enable          |
| 0x10   | ACREFCTL | Analog Comparator Reference Voltage Control |
| 0x20   | ACSTAT0  | Analog Comparator Status 0                  |
| 0x24   | ACCTL0   | Analog Comparator Control 0                 |
| 0x40   | ACSTAT1  | Analog Comparator Status 1                  |
| 0x44   | ACCTL1   | Analog Comparator Control 1                 |
| 0x60   | ACSTAT2  | Analog Comparator Status 2                  |
| 0x64   | ACCTL2   | Analog Comparator Control 2                 |
| 0xFC0  | ACMPPP   | Analog Comparator Peripheral Properties     |

**表 6-9. CRC Registers**

| OFFSET | ACRONYM   | REGISTER NAME              |
|--------|-----------|----------------------------|
| 400h   | CRCCTRL   | CRC Control                |
| 410h   | CRCSEED   | CRC SEED/Context           |
| 414h   | CRCDIN    | CRC Data Input             |
| 418h   | CRCRSLTPP | CRC Post Processing Result |

**表 6-10. DES Registers**

| OFFSET | ACRONYM       | REGISTER NAME                 |
|--------|---------------|-------------------------------|
| 0x00   | DES_KEY3_L    | DES Key 3 LSW for 192-Bit Key |
| 0x04   | DES_KEY3_H    | DES Key 3 MSW for 192-Bit Key |
| 0x08   | DES_KEY2_L    | DES Key 2 LSW for 128-Bit Key |
| 0x0C   | DES_KEY2_H    | DES Key 2 MSW for 128-Bit Key |
| 0x10   | DES_KEY1_L    | DES Key 1 LSW for 64-Bit Key  |
| 0x14   | DES_KEY1_H    | DES Key 1 MSW for 64-Bit Key  |
| 0x18   | DES_IV_L      | DES Initialization Vector     |
| 0x1C   | DES_IV_H      | DES Initialization Vector     |
| 0x20   | DES_CTRL      | DES Control                   |
| 0x24   | DES_LENGTH    | DES Cryptographic Data Length |
| 0x28   | DES_DATA_L    | DES LSW Data RW               |
| 0x2C   | DES_DATA_H    | DES MSW Data RW               |
| 0x30   | DES_REVISION  | DES Revision Number           |
| 0x34   | DES_SYSCONFIG | DES System Configuration      |
| 0x38   | DES_SYSSTATUS | DES System Status             |
| 0x3C   | DES_IRQSTATUS | DES Interrupt Status          |
| 0x40   | DES_IRQENABLE | DES Interrupt Enable          |
| 0x44   | DES_DIRTYBITS | DES Dirty Bits                |

表 6-11. DES  $\mu$ DMA Registers

| OFFSET | ACRONYM    | REGISTER NAME                   |
|--------|------------|---------------------------------|
| 0x30   | DES_DMAIM  | DES DMA Interrupt Mask          |
| 0x34   | DES_DMARIS | DES DMA Raw Interrupt Status    |
| 0x38   | DES_DMAMIS | DES DMA Masked Interrupt Status |
| 0x3C   | DES_DMAIC  | DES DMA Interrupt Clear         |

表 6-12. EEPROM Registers

| OFFSET       | ACRONYM            | REGISTER NAME                          |
|--------------|--------------------|----------------------------------------|
| 0x0          | EESIZE             | EEPROM Size Information                |
| 0x4          | EEBLOCK            | EEPROM Current Block                   |
| 0x8          | EEOFFSET           | EEPROM Current Offset                  |
| 0x10         | EERDWR             | EEPROM Read-Write                      |
| 0x14         | EERDWRINC          | EEPROM Read-Write with Increment       |
| 0x18         | EEDONE             | EEPROM Done Status                     |
| 0x1C         | EESUPP             | EEPROM Support Control and Status      |
| 0x20         | EEUNLOCK           | EEPROM Unlock                          |
| 0x30         | EEPROT             | EEPROM Protection                      |
| 0x34 to 0x3C | EEPASS0 to EEPASS2 | EEPROM Password 0 to EEPROM Password 2 |
| 0x40         | EEINT              | EEPROM Interrupt                       |
| 0x50         | EEHIDE0            | EEPROM Block Hide 0                    |
| 0x54         | EEHIDE1            | EEPROM Block Hide 1                    |
| 0x58         | EEHIDE2            | EEPROM Block Hide 2                    |
| 0x80         | EEDBGME            | EEPROM Debug Mass Erase                |
| 0xFC0        | EEPROMPP           | EEPROM Peripheral Properties           |

表 6-13. EPI Registers

| OFFSET       | ACRONYM                      | REGISTER NAME                      |
|--------------|------------------------------|------------------------------------|
| 0x000        | EPICFG                       | EPI Configuration                  |
| 0x004        | EPIBAUD                      | EPI Main Baud Rate                 |
| 0x008        | EPIBAUD2                     | EPI Main Baud Rate                 |
| 0x010        | EPISDRAMCFG                  | EPI SDRAM Configuration            |
| 0x010        | EPIHB8CFG                    | EPI Host-Bus 8 Configuration       |
| 0x010        | EPIHB16CFG                   | EPI Host-Bus 16 Configuration      |
| 0x010        | EPIGPCFG                     | EPI General-Purpose Configuration  |
| 0x014        | EPIHB8CFG2                   | EPI Host-Bus 8 Configuration 2     |
| 0x014        | EPIHB16CFG2                  | EPI Host-Bus 16 Configuration 2    |
| 0x01C        | EPIADDRMAP                   | EPI Address Map                    |
| 0x020        | EPIRSIZE0                    | EPI Read Size 0                    |
| 0x024        | EPIRADDR0                    | EPI Read Address 0                 |
| 0x028        | EPIRPSTD0                    | EPI Non-Blocking Read Data 0       |
| 0x030        | EPIRSIZE1                    | EPI Read Size 1                    |
| 0x034        | EPIRADDR1                    | EPI Read Address 1                 |
| 0x038        | EPIRPSTD1                    | EPI Non-Blocking Read Data 1       |
| 0x060        | EPISTAT                      | EPI Status                         |
| 0x06C        | EPIRFIFOCNT                  | EPI Read FIFO Count                |
| 0x70 to 0x8C | EPIREADFIFO0 to EPIREADFIFO7 | EPI Read FIFO 0 to EPI Read FIFO 7 |
| 0x200        | EPIFIFOLVL                   | EPI FIFO Level Selects             |
| 0x24         | EPIWFIFOCNT                  | EPI Write FIFO Count               |

**表 6-13. EPI Registers (continued)**

| OFFSET | ACRONYM      | REGISTER NAME                            |
|--------|--------------|------------------------------------------|
| 0x28   | EPIDMATXCNT  | EPI DMA Transmit Count                   |
| 0x210  | EPIIM        | EPI Interrupt Mask                       |
| 0x214  | EPIRIS       | EPI Raw Interrupt Status                 |
| 0x218  | EPIMIS       | EPI Masked Interrupt Status              |
| 0x21C  | EPIEISC      | EPI Error and Interrupt Status and Clear |
| 0x308  | EPIHB8CFG3   | EPI Host-Bus 8 Configuration 3           |
| 0x308  | EPIHB16CFG3  | EPI Host-Bus 16 Configuration 3          |
| 0x30C  | EPIHB8CFG4   | EPI Host-Bus 8 Configuration 4           |
| 0x30C  | EPIHB16CFG4  | EPI Host-Bus 16 Configuration 4          |
| 0x310  | EPIHB8TIME   | EPI Host-Bus 8 Timing Extension          |
| 0x310  | EPIHB16TIME  | EPI Host-Bus 16 Timing Extension         |
| 0x314  | EPIHB8TIME2  | EPI Host-Bus 8 Timing Extension          |
| 0x314  | EPIHB16TIME2 | EPI Host-Bus 16 Timing Extension         |
| 0x318  | EPIHB8TIME3  | EPI Host-Bus 8 Timing Extension          |
| 0x318  | EPIHB16TIME3 | EPI Host-Bus 16 Timing Extension         |
| 0x31C  | EPIHB8TIME4  | EPI Host-Bus 8 Timing Extension          |
| 0x31C  | EPIHB16TIME4 | EPI Host-Bus 16 Timing Extension         |
| 0x360  | EPIHBPSRAM   | EPI Host-Bus PSRAM                       |

**表 6-14. Ethernet MAC (EMAC) Registers**

| OFFSET | ACRONYM         | REGISTER NAME                                 |
|--------|-----------------|-----------------------------------------------|
| 0x0    | EMACCFG         | Ethernet MAC Configuration                    |
| 0x4    | EMACFRAMEFLTR   | Ethernet MAC Frame Filter                     |
| 0x8    | EMACHASHTBLH    | Ethernet MAC Hash Table High                  |
| 0xC    | EMACHASHTBLL    | Ethernet MAC Hash Table Low                   |
| 0x10   | EMACMIIADDR     | Ethernet MAC MII Address                      |
| 0x14   | EMACMIIDATA     | Ethernet MAC MII Data Register                |
| 0x18   | EMACFLOWCTL     | Ethernet MAC Flow Control                     |
| 0x1C   | EMACVLANTG      | Ethernet MAC VLAN Tag                         |
| 0x24   | EMACSTATUS      | Ethernet MAC Status                           |
| 0x28   | EMACRWUFF       | Ethernet MAC Remote Wake-Up Frame Filter      |
| 0x2C   | EMACPMCTCTLSTAT | Ethernet MAC PMT Control and Status           |
| 0x30   | EMACLPICTLSTAT  | LPI Control and Status                        |
| 0x34   | EMACLPIIMERCTRL | LPI Timers Control                            |
| 0x38   | EMACRIS         | Ethernet MAC Raw Interrupt Status             |
| 0x3C   | EMACIM          | Ethernet MAC Interrupt Mask                   |
| 0x40   | EMACADDR0H      | Ethernet MAC Address 0 High                   |
| 0x44   | EMACADDR0L      | Ethernet MAC Address 0 Low Register           |
| 0x48   | EMACADDR1H      | Ethernet MAC Address 1 High                   |
| 0x4C   | EMACADDR1L      | Ethernet MAC Address 1 Low                    |
| 0x50   | EMACADDR2H      | Ethernet MAC Address 2 High                   |
| 0x54   | EMACADDR2L      | Ethernet MAC Address 2 Low                    |
| 0x58   | EMACADDR3H      | Ethernet MAC Address 3 High                   |
| 0x5C   | EMACADDR3L      | Ethernet MAC Address 3 Low                    |
| 0xDC   | EMACWDOGTO      | Ethernet MAC Watchdog Time-out                |
| 0x100  | EMACMMCCTRL     | Ethernet MAC MMC Control                      |
| 0x104  | EMACMMCRXRIS    | Ethernet MAC MMC Receive Raw Interrupt Status |

表 6-14. Ethernet MAC (EMAC) Registers (continued)

| OFFSET | ACRONYM          | REGISTER NAME                                                                      |
|--------|------------------|------------------------------------------------------------------------------------|
| 0x108  | EMACMMCTXRIS     | Ethernet MAC MMC Transmit Raw Interrupt Status                                     |
| 0x10C  | EMACMMCRXIM      | Ethernet MAC MMC Receive Interrupt Mask                                            |
| 0x110  | EMACMMCTXIM      | Ethernet MAC MMC Transmit Interrupt Mask                                           |
| 0x118  | EMACTXCNTGB      | Ethernet MAC Transmit Frame Count for Good and Bad Frames                          |
| 0x14C  | EMACTXCNTSCOL    | Ethernet MAC Transmit Frame Count for Frames Transmitted After Single Collision    |
| 0x150  | EMACTXCNTMCOL    | Ethernet MAC Transmit Frame Count for Frames Transmitted After Multiple Collisions |
| 0x164  | EMACTXOCTCNTG    | Ethernet MAC Transmit Octet Count Good                                             |
| 0x180  | EMACRXCNTGB      | Ethernet MAC Receive Frame Count for Good and Bad Frames                           |
| 0x194  | EMACRXCNTCRCERR  | Ethernet MAC Receive Frame Count for CRC Error Frames                              |
| 0x198  | EMACRXCNTALGNERR | Ethernet MAC Receive Frame Count for Alignment Error Frames                        |
| 0x1C4  | EMACRXCNTGUNI    | Ethernet MAC Receive Frame Count for Good Unicast Frames                           |
| 0x584  | EMACVLNINCREP    | Ethernet MAC VLAN Tag Inclusion or Replacement                                     |
| 0x588  | EMACVLANHASH     | Ethernet MAC VLAN Hash Table                                                       |
| 0x700  | EMACTIMSTCTRL    | Ethernet MAC Timestamp Control                                                     |
| 0x704  | EMACSUBSECINC    | Ethernet MAC Sub-Second Increment                                                  |
| 0x708  | EMACTIMSEC       | Ethernet MAC System Time - Seconds                                                 |
| 0x70C  | EMACTIMNANO      | Ethernet MAC System Time - Nanoseconds                                             |
| 0x710  | EMACTIMSECU      | Ethernet MAC System Time - Seconds Update                                          |
| 0x714  | EMACTIMNANO      | Ethernet MAC System Time - Nanoseconds Update                                      |
| 0x718  | EMACTIMADD       | Ethernet MAC Timestamp Addend                                                      |
| 0x71C  | EMACTARGSEC      | Ethernet MAC Target Time Seconds                                                   |
| 0x720  | EMACTARGNANO     | Ethernet MAC Target Time Nanoseconds                                               |
| 0x724  | EMACHWORDSEC     | Ethernet MAC System Time-Higher Word Seconds                                       |
| 0x728  | EMACTIMSTAT      | Ethernet MAC Timestamp Status                                                      |
| 0x72C  | EMACPPSCTRL      | Ethernet MAC PPS Control                                                           |
| 0x760  | EMACPPS0INTVL    | Ethernet MAC PPS0 Interval                                                         |
| 0x764  | EMACPPS0WIDTH    | Ethernet MAC PPS0 Width                                                            |
| 0xC00  | EMACDMABUSMOD    | Ethernet MAC DMA Bus Mode                                                          |
| 0xC04  | EMACTXPOLL       | Ethernet MAC Transmit Poll Demand                                                  |
| 0xC08  | EMACRXPOLLD      | Ethernet MAC Receive Poll Demand                                                   |
| 0xC0C  | EMACRXDLADDR     | Ethernet MAC Receive Descriptor List Address                                       |
| 0xC10  | EMACTXDLADDR     | Ethernet MAC Transmit Descriptor List Address                                      |
| 0xC14  | EMACDMARIS       | Ethernet MAC DMA Interrupt Status                                                  |
| 0xC18  | EMACDMAOPMODE    | Ethernet MAC DMA Operation Mode                                                    |
| 0xC1C  | EMACDMAIM        | Ethernet MAC DMA Interrupt Mask Register                                           |
| 0xC20  | EMACMFBOC        | Ethernet MAC Missed Frame and Buffer Overflow Counter                              |
| 0xC24  | EMACRXINTWDT     | Ethernet MAC Receive Interrupt Watchdog Timer                                      |
| 0xC48  | EMACHOSTXDESC    | Ethernet MAC Current Host Transmit Descriptor                                      |
| 0xC4C  | EMACHOSRXDESC    | Ethernet MAC Current Host Receive Descriptor                                       |
| 0xC50  | EMACHOSTXBA      | Ethernet MAC Current Host Transmit Buffer Address                                  |
| 0xC54  | EMACHOSRXBA      | Ethernet MAC Current Host Receive Buffer Address                                   |
| 0xFC0  | EMACPP           | Ethernet MAC Peripheral Property Register                                          |
| 0xFC4  | EMACPC           | Ethernet MAC Peripheral Configuration                                              |
| 0xFC8  | EMACCC           | Ethernet MAC Clock Configuration                                                   |
| 0xFD0  | EPHYRIS          | Ethernet PHY Raw Interrupt Status                                                  |
| 0xFD4  | EPHYIM           | Ethernet PHY Interrupt Mask                                                        |

**表 6-14. Ethernet MAC (EMAC) Registers (continued)**

| OFFSET | ACRONYM  | REGISTER NAME                                  |
|--------|----------|------------------------------------------------|
| 0xFD8  | EPHYMISC | Ethernet PHY Masked Interrupt Status and Clear |

**表 6-15. Ethernet MII Management (EPHY) Registers (Accessed Through the EMACMIIADDR Register)**

| ADDRESS | ACRONYM     | REGISTER NAME                                                      |
|---------|-------------|--------------------------------------------------------------------|
| 0x00    | EPHYBMCR    | Ethernet PHY Basic Mode Control - MR0                              |
| 0x01    | EPHYBMSR    | Ethernet PHY Basic Mode Status - MR1                               |
| 0x02    | EPHYID1     | Ethernet PHY Identifier Register 1 - MR2                           |
| 0x03    | EPHYID2     | Ethernet PHY Identifier Register 2 - MR3                           |
| 0x04    | EPHYANA     | Ethernet PHY Auto-Negotiation Advertisement - MR4                  |
| 0x05    | EPHYANLPA   | Ethernet PHY Auto-Negotiation Link Partner Ability -MR5            |
| 0x06    | EPHYANER    | Ethernet PHY Auto-Negotiation Expansion - MR6                      |
| 0x07    | EPHYANNPTR  | Ethernet PHY Auto-Negotiation Next Page TX - MR7                   |
| 0x08    | EPHYANLNPTR | Ethernet PHY Auto-Negotiation Link Partner Ability Next Page - MR8 |
| 0x09    | EPHYCFG1    | Ethernet PHY Configuration 1 - MR9                                 |
| 0x0A    | EPHYCFG2    | Ethernet PHY Configuration 2 - MR10                                |
| 0x0B    | EPHYCFG3    | Ethernet PHY Configuration 3 - MR11                                |
| 0x0D    | EPHYREGCTL  | Ethernet PHY Register Control - MR13                               |
| 0x0E    | EPHYADDR    | Ethernet PHY Address or Data - MR14                                |
| 0x10    | EPHYSTS     | Ethernet PHY Status - MR16                                         |
| 0x11    | EPHYSCR     | Ethernet PHY Specific Control - MR17                               |
| 0x12    | EPHYMISR1   | Ethernet PHY MII Interrupt Status 1 - MR18                         |
| 0x13    | EPHYMISR2   | Ethernet PHY MII Interrupt Status 2 - MR19                         |
| 0x14    | EPHYFCSR    | Ethernet PHY False Carrier Sense Counter - MR20                    |
| 0x15    | EPHYRXERCNT | Ethernet PHY Receive Error Count - MR21                            |
| 0x16    | EPHYBISTCR  | Ethernet PHY BIST Control - MR22                                   |
| 0x18    | EPHYLEDCR   | Ethernet PHY LED Control - MR24                                    |
| 0x19    | EPHYCTL     | Ethernet PHY Control - MR25                                        |
| 0x1A    | EPHY10BTSC  | Ethernet PHY 10Base-T Status/Control - MR26                        |
| 0x1B    | EPHYBICSR1  | Ethernet PHY BIST Control and Status 1 - MR27                      |
| 0x1C    | EPHYBICSR2  | Ethernet PHY BIST Control and Status 2 - MR28                      |
| 0x1E    | EPHYCDCR    | Ethernet PHY Cable Diagnostic Control - MR30                       |
| 0x1F    | EPHYRCR     | Ethernet PHY Reset Control - MR31                                  |
| 0x25    | EPHYLEDCFG  | Ethernet PHY LED Configuration - MR37                              |

**表 6-16. Flash Registers**

| OFFSET         | ACRONYM       | REGISTER NAME                                      |
|----------------|---------------|----------------------------------------------------|
| 0x0            | FMA           | Flash Memory Address                               |
| 0x4            | FMD           | Flash Memory Data                                  |
| 0x8            | FMC           | Flash Memory Control                               |
| 0xC            | FCRIS         | Flash Controller Raw Interrupt Status              |
| 0x10           | FCIM          | Flash Controller Interrupt Mask                    |
| 0x14           | FCMISC        | Flash Controller Masked Interrupt Status and Clear |
| 0x20           | FMC2          | Flash Memory Control 2                             |
| 0x30           | FWBVAL        | Flash Write Buffer Valid                           |
| 0x3C           | FLPEKEY       | Flash Program/Erase Key                            |
| 0x100 to 0x17C | FWB0 to FWB31 | Flash Write Buffer 0 to Flash Write Buffer 32      |
| 0xFC0          | FLASHPP       | Flash Peripheral Properties                        |

表 6-16. Flash Registers (continued)

| OFFSET | ACRONYM    | REGISTER NAME                |
|--------|------------|------------------------------|
| 0xFC4  | SSIZE      | SRAM Size                    |
| 0xFC8  | FLASHCONF  | Flash Configuration Register |
| 0xFCC  | ROMSWMAP   | ROM Third-Party Software     |
| 0xFD0  | FLASHDMASZ | Flash DMA Address Size       |
| 0xFD4  | FLASHDMAST | Flash DMA Starting Address   |

表 6-17. GPIO Registers

| OFFSET | ACRONYM       | REGISTER NAME                    |
|--------|---------------|----------------------------------|
| 0x0    | GPIODATA      | GPIO Data                        |
| 0x400  | GPIODIR       | GPIO Direction                   |
| 0x404  | GPIOIS        | GPIO Interrupt Sense             |
| 0x408  | GPIOIBE       | GPIO Interrupt Both Edges        |
| 0x40C  | GPIOIEV       | GPIO Interrupt Event             |
| 0x410  | GPIOIM        | GPIO Interrupt Mask              |
| 0x414  | GPIORIS       | GPIO Raw Interrupt Status        |
| 0x418  | GPIOMIS       | GPIO Masked Interrupt Status     |
| 0x41C  | GPIOICR       | GPIO Interrupt Clear             |
| 0x420  | GPIOAFSEL     | GPIO Alternate Function Select   |
| 0x500  | GPIODR2R      | GPIO 2-mA Drive Select           |
| 0x504  | GPIODR4R      | GPIO 4-mA Drive Select           |
| 0x508  | GPIODR8R      | GPIO 8-mA Drive Select           |
| 0x50C  | GPIODR        | GPIO Open Drain Select           |
| 0x510  | GPIOPUR       | GPIO Pullup Select               |
| 0x514  | GPIOPDR       | GPIO Pulldown Select             |
| 0x518  | GPIOSLR       | GPIO Slew Rate Control Select    |
| 0x51C  | GPIODEN       | GPIO Digital Enable              |
| 0x520  | GPIOLOCK      | GPIO Lock                        |
| 0x524  | GPIOCR        | GPIO Commit                      |
| 0x528  | GPIOAMSEL     | GPIO Analog Mode Select          |
| 0x52C  | GPIOPCTL      | GPIO Port Control                |
| 0x530  | GPIOADCCTL    | GPIO ADC Control                 |
| 0x534  | GPIODMACTL    | GPIO DMA Control                 |
| 0x538  | GPIOSI        | GPIO Select Interrupt            |
| 0x53C  | GPIODR12R     | GPIO 12-mA Drive Select          |
| 0x540  | GPIOWAKEPEN   | GPIO Wake Pin Enable             |
| 0x544  | GPIOWAKELVL   | GPIO Wake Level                  |
| 0x548  | GPIOWAKESTAT  | GPIO Wake Status                 |
| 0xFC0  | GPIOPP        | GPIO Peripheral Property         |
| 0xFC4  | GPIOPC        | GPIO Peripheral Configuration    |
| 0xFD0  | GPIOPeriphID4 | GPIO Peripheral Identification 4 |
| 0xFD4  | GPIOPeriphID5 | GPIO Peripheral Identification 5 |
| 0xFD8  | GPIOPeriphID6 | GPIO Peripheral Identification 6 |
| 0xFDC  | GPIOPeriphID7 | GPIO Peripheral Identification 7 |
| 0xFE0  | GPIOPeriphID0 | GPIO Peripheral Identification 0 |
| 0xFE4  | GPIOPeriphID1 | GPIO Peripheral Identification 1 |
| 0xFE8  | GPIOPeriphID2 | GPIO Peripheral Identification 2 |
| 0xFEC  | GPIOPeriphID3 | GPIO Peripheral Identification 3 |

**表 6-17. GPIO Registers (continued)**

| OFFSET | ACRONYM     | REGISTER NAME                   |
|--------|-------------|---------------------------------|
| 0xFF0  | GPIOCellID0 | GPIO PrimeCell Identification 0 |
| 0xFF4  | GPIOCellID1 | GPIO PrimeCell Identification 1 |
| 0xFF8  | GPIOCellID2 | GPIO PrimeCell Identification 2 |
| 0xFFC  | GPIOCellID3 | GPIO PrimeCell Identification 3 |

**表 6-18. GPTM Registers**

| OFFSET | ACRONYM      | REGISTER NAME                  |
|--------|--------------|--------------------------------|
| 0x0    | GPTMCFG      | GPTM Configuration             |
| 0x4    | GPTMTAMR     | GPTM Timer A Mode              |
| 0x8    | GPTMTBMR     | GPTM Timer B Mode              |
| 0xC    | GPTMCTL      | GPTM Control                   |
| 0x10   | GPTMSYNC     | GPTM Synchronize               |
| 0x18   | GPTMIMR      | GPTM Interrupt Mask            |
| 0x1C   | GPTMRIS      | GPTM Raw Interrupt Status      |
| 0x20   | GPTMMIS      | GPTM Masked Interrupt Status   |
| 0x24   | GPTMICR      | GPTM Interrupt Clear           |
| 0x28   | GPTMTAILR    | GPTM Timer A Interval Load     |
| 0x2C   | GPTMTBILR    | GPTM Timer B Interval Load     |
| 0x30   | GPTMTAMATCHR | GPTM Timer A Match             |
| 0x34   | GPTMTBMATCHR | GPTM Timer B Match             |
| 0x38   | GPTMTAPR     | GPTM Timer A Prescale          |
| 0x3C   | GPTMTBPR     | GPTM Timer B Prescale          |
| 0x40   | GPTMTAPMR    | GPTM TimerA Prescale Match     |
| 0x44   | GPTMTBPMR    | GPTM TimerB Prescale Match     |
| 0x48   | GPTMTAR      | GPTM Timer A                   |
| 0x4C   | GPTMTBR      | GPTM Timer B                   |
| 0x50   | GPTMTAV      | GPTM Timer A Value             |
| 0x54   | GPTMTBV      | GPTM Timer B Value             |
| 0x58   | GPTMRTCPD    | GPTM RTC Predivide             |
| 0x5C   | GPTMTAPS     | GPTM Timer A Prescale Snapshot |
| 0x60   | GPTMTBPS     | GPTM Timer B Prescale Snapshot |
| 0x6C   | GPTMDMAEV    | GPTM DMA Event                 |
| 0x70   | GPTMADCEV    | GPTM ADC Event                 |
| 0xFC0  | GPTMPP       | GPTM Peripheral Properties     |
| 0xFC8  | GPTMCC       | GPTM Clock Configuration       |

**表 6-19. HIB Registers**

| OFFSET | ACRONYM  | REGISTER NAME                       |
|--------|----------|-------------------------------------|
| 0x0    | HIBRTCC  | Hibernation RTC Counter             |
| 0x4    | HIBRTCM0 | Hibernation RTC Match 0             |
| 0xC    | HIBRTCLD | Hibernation RTC Load                |
| 0x10   | HIBCTL   | Hibernation Control                 |
| 0x14   | HIBIM    | Hibernation Interrupt Mask          |
| 0x18   | HIBRIS   | Hibernation Raw Interrupt Status    |
| 0x1C   | HIBMIS   | Hibernation Masked Interrupt Status |
| 0x20   | HIBIC    | Hibernation Interrupt Clear         |
| 0x24   | HIBRTCT  | Hibernation RTC Trim                |

表 6-19. HIB Registers (continued)

| OFFSET       | ACRONYM   | REGISTER NAME                     |
|--------------|-----------|-----------------------------------|
| 0x28         | HIBRTCSS  | Hibernation RTC Sub Seconds       |
| 0x2C         | HIBIO     | Hibernation IO Configuration      |
| 0x30 to 0x6F | HIBDATA   | Hibernation Data                  |
| 0x300        | HIBCALCTL | Hibernation Calendar Control      |
| 0x310        | HIBCAL0   | Hibernation Calendar 0            |
| 0x314        | HIBCAL1   | Hibernation Calendar 1            |
| 0x320        | HIBCALLD0 | Hibernation Calendar Load 0       |
| 0x324        | HIBCALLD1 | Hibernation Calendar Load 1       |
| 0x330        | HIBCALM0  | Hibernation Calendar Match 0      |
| 0x334        | HIBCALM1  | Hibernation Calendar Match 1      |
| 0x360        | HIBLOCK   | Hibernation Lock                  |
| 0x400        | HIBTPCTL  | HIB Tamper Control                |
| 0x404        | HIBTPSTAT | HIB Tamper Status                 |
| 0x410        | HIBTPIO   | HIB Tamper I/O Control            |
| 0x4E0        | HIBTPLOG0 | HIB Tamper Log 0                  |
| 0x4E4        | HIBTPLOG1 | HIB Tamper Log 1                  |
| 0x4E8        | HIBTPLOG2 | HIB Tamper Log 2                  |
| 0x4EC        | HIBTPLOG3 | HIB Tamper Log 3                  |
| 0x4F0        | HIBTPLOG4 | HIB Tamper Log 4                  |
| 0x4F4        | HIBTPLOG5 | HIB Tamper Log 5                  |
| 0x4F8        | HIBTPLOG6 | HIB Tamper Log 6                  |
| 0x4FC        | HIBTPLOG7 | HIB Tamper Log 7                  |
| 0xFC0        | HIBPP     | Hibernation Peripheral Properties |
| 0xFC8        | HIBCC     | Hibernation Clock Control         |

表 6-20. I2C Registers

| OFFSET | ACRONYM     | REGISTER NAME                       |
|--------|-------------|-------------------------------------|
| 0x0    | I2CMSA      | I2C Master Slave Address            |
| 0x4    | I2CMCS      | I2C Master Control/Status           |
| 0x8    | I2CMRDR     | I2C Master Data                     |
| 0xC    | I2CMTPR     | I2C Master Timer Period             |
| 0x10   | I2CMIMR     | I2C Master Interrupt Mask           |
| 0x14   | I2CMRIS     | I2C Master Raw Interrupt Status     |
| 0x18   | I2CMMIS     | I2C Master Masked Interrupt Status  |
| 0x1C   | I2CMICR     | I2C Master Interrupt Clear          |
| 0x20   | I2CMCR      | I2C Master Configuration            |
| 0x24   | I2CMCLKOCNT | I2C Master Clock Low Time-out Count |
| 0x2C   | I2CMBMON    | I2C Master Bus Monitor              |
| 0x30   | I2CMBLEN    | I2C Master Burst Length             |
| 0x34   | I2CMBCNT    | I2C Master Burst Count              |
| 0x800  | I2CSOAR     | I2C Slave Own Address               |
| 0x804  | I2CSCSR     | I2C Slave Control/Status            |
| 0x808  | I2CSDR      | I2C Slave Data                      |
| 0x80C  | I2CSIMR     | I2C Slave Interrupt Mask            |
| 0x810  | I2CSRIS     | I2C Slave Raw Interrupt Status      |
| 0x814  | I2CSMIS     | I2C Slave Masked Interrupt Status   |
| 0x818  | I2CSICR     | I2C Slave Interrupt Clear           |

**表 6-20. I2C Registers (continued)**

| OFFSET | ACRONYM       | REGISTER NAME                |
|--------|---------------|------------------------------|
| 0x81C  | I2CSOAR2      | I2C Slave Own Address 2      |
| 0x820  | I2CSACKCTL    | I2C Slave ACK Control        |
| 0xF00  | I2CFIFODATA   | I2C FIFO Data                |
| 0xF04  | I2CFIFOCTL    | I2C FIFO Control             |
| 0xF08  | I2CFIFOSTATUS | I2C FIFO Status              |
| 0xFC0  | I2CPP         | I2C Peripheral Properties    |
| 0xFC4  | I2CPC         | I2C Peripheral Configuration |

**表 6-21.  $\mu$ DMA Registers**

| OFFSET | ACRONYM         | REGISTER NAME                              |
|--------|-----------------|--------------------------------------------|
| 0x0    | DMASTAT         | DMA Status                                 |
| 0x4    | DMACFG          | DMA Configuration                          |
| 0x8    | DMACTLBASE      | DMA Channel Control Base Pointer           |
| 0xC    | DMAALTBASE      | DMA Alternate Channel Control Base Pointer |
| 0x10   | DMAWAITSTAT     | DMA Channel Wait-on-Request Status         |
| 0x14   | DMASWREQ        | DMA Channel Software Request               |
| 0x18   | DMAUSEBURSTSET  | DMA Channel Useburst Set                   |
| 0x1C   | DMAUSEBURSTCLR  | DMA Channel Useburst Clear                 |
| 0x20   | DMAREQMASKSET   | DMA Channel Request Mask Set               |
| 0x24   | DMAREQMASKCLR   | DMA Channel Request Mask Clear             |
| 0x28   | DMAENASET       | DMA Channel Enable Set                     |
| 0x2C   | DMAENACLR       | DMA Channel Enable Clear                   |
| 0x30   | DMAALTSET       | DMA Channel Primary Alternate Set          |
| 0x34   | DMAALTCLR       | DMA Channel Primary Alternate Clear        |
| 0x38   | DMAPRIOSET      | DMA Channel Priority Set                   |
| 0x3C   | DMAPRIOCLR      | DMA Channel Priority Clear                 |
| 0x4C   | DMAERRCLR       | DMA Bus Error Clear                        |
| 0x510  | DMACHMAP0       | DMA Channel Map Select 0                   |
| 0x514  | DMACHMAP1       | DMA Channel Map Select 1                   |
| 0x518  | DMACHMAP2       | DMA Channel Map Select 2                   |
| 0x51C  | DMACHMAP3       | DMA Channel Map Select 3                   |
| 0xFD0  | DMAPeriphID4    | DMA Peripheral Identification 4            |
| 0xFE0  | DMAPeriphID0    | DMA Peripheral Identification 0            |
| 0xFE4  | DMAPeriphID1    | DMA Peripheral Identification 1            |
| 0xFE8  | DMAPeriphID2    | DMA Peripheral Identification 2            |
| 0xFEC  | DMAPeriphID3    | DMA Peripheral Identification 3            |
| 0xFF0  | DMAPrimeCellID0 | DMA PrimeCell Identification 0             |
| 0xFF4  | DMAPrimeCellID1 | DMA PrimeCell Identification 1             |
| 0xFF8  | DMAPrimeCellID2 | DMA PrimeCell Identification 2             |
| 0xFFC  | DMAPrimeCellID3 | DMA PrimeCell Identification 3             |

**表 6-22.  $\mu$ DMA Channel Control Structure Registers**

| OFFSET | ACRONYM    | REGISTER NAME                               |
|--------|------------|---------------------------------------------|
| 0x0    | DMASRCENDP | DMA Channel Source Address End Pointer      |
| 0x4    | DMADSTENDP | DMA Channel Destination Address End Pointer |
| 0x8    | DMACHCTL   | DMA Channel Control Word                    |

表 6-23. PWM Registers

| OFFSET | ACRONYM       | REGISTER NAME                     |
|--------|---------------|-----------------------------------|
| 0x0    | PWMCTL        | PWM Master Control                |
| 0x4    | PWMSYNC       | PWM Time Base Sync                |
| 0x8    | PWMENABLE     | PWM Output Enable                 |
| 0xC    | PWMINVERT     | PWM Output Inversion              |
| 0x10   | PWMFAULT      | PWM Output Fault                  |
| 0x14   | PWMINTEN      | PWM Interrupt Enable              |
| 0x18   | PWMRIS        | PWM Raw Interrupt Status          |
| 0x1C   | PWMISC        | PWM Interrupt Status and Clear    |
| 0x20   | PWMSTATUS     | PWM Status                        |
| 0x24   | PWMFAULTVAL   | PWM Fault Condition Value         |
| 0x28   | PWMENUPD      | PWM Enable Update                 |
| 0x40   | PWM0CTL       | PWM0 Control                      |
| 0x44   | PWM0INTEN     | PWM0 Interrupt and Trigger Enable |
| 0x48   | PWM0RIS       | PWM0 Raw Interrupt Status         |
| 0x4C   | PWM0ISC       | PWM0 Interrupt Status and Clear   |
| 0x50   | PWM0LOAD      | PWM0 Load                         |
| 0x54   | PWM0COUNT     | PWM0 Counter                      |
| 0x58   | PWM0CMPA      | PWM0 Compare A                    |
| 0x5C   | PWM0CMPB      | PWM0 Compare B                    |
| 0x60   | PWM0GENA      | PWM0 Generator A Control          |
| 0x64   | PWM0GENB      | PWM0 Generator B Control          |
| 0x68   | PWM0DBCTL     | PWM0 Dead-Band Control            |
| 0x6C   | PWM0DBRISE    | PWM0 Dead-Band Rising-Edge Delay  |
| 0x70   | PWM0DBFALL    | PWM0 Dead-Band Falling-Edge-Delay |
| 0x74   | PWM0FLTSRC0   | PWM0 Fault Source 0               |
| 0x78   | PWM0FLTSRC1   | PWM0 Fault Source 1               |
| 0x7C   | PWM0MINFLTPER | PWM0 Minimum Fault Period         |
| 0x080  | PWM1CTL       | PWM1 Control                      |
| 0x084  | PWM1INTEN     | PWM1 Interrupt and Trigger Enable |
| 0x088  | PWM1RIS       | PWM1 Raw Interrupt Status         |
| 0x08C  | PWM1ISC       | PWM1 Interrupt Status and Clear   |
| 0x090  | PWM1LOAD      | PWM1 Load                         |
| 0x094  | PWM1COUNT     | PWM1 Counter                      |
| 0x098  | PWM1CMPA      | PWM1 Compare A                    |
| 0x09C  | PWM1CMPB      | PWM1 Compare B                    |
| 0x0A0  | PWM1GENA      | PWM1 Generator A Control          |
| 0x0A4  | PWM1GENB      | PWM1 Generator B Control          |
| 0x0A8  | PWM1DBCTL     | PWM1 Dead-Band Control            |
| 0x0AC  | PWM1DBRISE    | PWM1 Dead-Band Rising-Edge Delay  |
| 0x0B0  | PWM1DBFALL    | PWM1 Dead-Band Falling-Edge-Delay |
| 0x0B4  | PWM1FLTSRC0   | PWM1 Fault Source 0               |
| 0x0B8  | PWM1FLTSRC1   | PWM1 Fault Source 1               |
| 0x0BC  | PWM1MINFLTPER | PWM1 Minimum Fault Period         |
| 0x0C0  | PWM2CTL       | PWM2 Control                      |
| 0x0C4  | PWM2INTEN     | PWM2 Interrupt and Trigger Enable |
| 0x0C8  | PWM2RIS       | PWM2 Raw Interrupt Status         |
| 0x0CC  | PWM2ISC       | PWM2 Interrupt Status and Clear   |

**表 6-23. PWM Registers (continued)**

| OFFSET | ACRONYM       | REGISTER NAME                     |
|--------|---------------|-----------------------------------|
| 0x0D0  | PWM2LOAD      | PWM2 Load                         |
| 0x0D4  | PWM2COUNT     | PWM2 Counter                      |
| 0x0D8  | PWM2CMPA      | PWM2 Compare A                    |
| 0x0DC  | PWM2CMPB      | PWM2 Compare B                    |
| 0x0E0  | PWM2GENA      | PWM2 Generator A Control          |
| 0x0E4  | PWM2GENB      | PWM2 Generator B Control          |
| 0x0E8  | PWM2DBCTL     | PWM2 Dead-Band Control            |
| 0x0EC  | PWM2DBRISE    | PWM2 Dead-Band Rising-Edge Delay  |
| 0x0F0  | PWM2DBFALL    | PWM2 Dead-Band Falling-Edge-Delay |
| 0x0F4  | PWM2FLTSRC0   | PWM2 Fault Source 0               |
| 0x0F8  | PWM2FLTSRC1   | PWM2 Fault Source 1               |
| 0x0FC  | PWM2MINFLTPER | PWM2 Minimum Fault Period         |
| 0x100  | PWM3CTL       | PWM3 Control                      |
| 0x104  | PWM3INTEN     | PWM3 Interrupt and Trigger Enable |
| 0x108  | PWM3RIS       | PWM3 Raw Interrupt Status         |
| 0x10C  | PWM3ISC       | PWM3 Interrupt Status and Clear   |
| 0x110  | PWM3LOAD      | PWM3 Load                         |
| 0x114  | PWM3COUNT     | PWM3 Counter                      |
| 0x118  | PWM3CMPA      | PWM3 Compare A                    |
| 0x11C  | PWM3CMPB      | PWM3 Compare B                    |
| 0x120  | PWM3GENA      | PWM3 Generator A Control          |
| 0x124  | PWM3GENB      | PWM3 Generator B Control          |
| 0x128  | PWM3DBCTL     | PWM3 Dead-Band Control            |
| 0x12C  | PWM3DBRISE    | PWM3 Dead-Band Rising-Edge Delay  |
| 0x130  | PWM3DBFALL    | PWM3 Dead-Band Falling-Edge-Delay |
| 0x134  | PWM3FLTSRC0   | PWM3 Fault Source 0               |
| 0x138  | PWM3FLTSRC1   | PWM3 Fault Source 1               |
| 0x13C  | PWM3MINFLTPER | PWM3 Minimum Fault Period         |
| 0x800  | PWM0FLTSEN    | PWM0 Fault Pin Logic Sense        |
| 0x804  | PWM0FLTSTAT0  | PWM0 Fault Status 0               |
| 0x808  | PWM0FLTSTAT1  | PWM0 Fault Status 1               |
| 0x880  | PWM1FLTSEN    | PWM1 Fault Pin Logic Sense        |
| 0x884  | PWM1FLTSTAT0  | PWM1 Fault Status 0               |
| 0x888  | PWM1FLTSTAT1  | PWM1 Fault Status 1               |
| 0x900  | PWM2FLTSEN    | PWM2 Fault Pin Logic Sense        |
| 0x904  | PWM2FLTSTAT0  | PWM2 Fault Status 0               |
| 0x908  | PWM2FLTSTAT1  | PWM2 Fault Status 1               |
| 0x980  | PWM3FLTSEN    | PWM3 Fault Pin Logic Sense        |
| 0x984  | PWM3FLTSTAT0  | PWM3 Fault Status 0               |
| 0x988  | PWM3FLTSTAT1  | PWM3 Fault Status 1               |
| 0xFC0  | PWMPP         | PWM Peripheral Properties         |
| 0xFC8  | PWMCC         | PWM Clock Configuration           |

**表 6-24. QEI Registers**

| OFFSET | ACRONYM | REGISTER NAME |
|--------|---------|---------------|
| 0x0    | QEICTL  | QEI Control   |
| 0x4    | QEISTAT | QEI Status    |

表 6-24. QEI Registers (continued)

| OFFSET | ACRONYM   | REGISTER NAME                  |
|--------|-----------|--------------------------------|
| 0x8    | QEIP0S    | QEI Position                   |
| 0xC    | QEIMAXPOS | QEI Maximum Position           |
| 0x10   | QEILOAD   | QEI Timer Load                 |
| 0x14   | QEITIME   | QEI Timer                      |
| 0x18   | QEICOUNT  | QEI Velocity Counter           |
| 0x1C   | QEISPEED  | QEI Velocity                   |
| 0x20   | QEINTEN   | QEI Interrupt Enable           |
| 0x24   | QEIRIS    | QEI Raw Interrupt Status       |
| 0x28   | QEISC     | QEI Interrupt Status and Clear |

表 6-25. QSSI Registers

| OFFSET | ACRONYM     | REGISTER NAME                    |
|--------|-------------|----------------------------------|
| 0x0    | SSICR0      | QSSI Control 0                   |
| 0x4    | SSICR1      | QSSI Control 1                   |
| 0x8    | SSIDR       | QSSI Data                        |
| 0xC    | SSISR       | QSSI Status                      |
| 0x10   | SSICPSR     | QSSI Clock Prescale              |
| 0x14   | SSIIM       | QSSI Interrupt Mask              |
| 0x18   | SSIRIS      | QSSI Raw Interrupt Status        |
| 0x1C   | SSIMIS      | QSSI Masked Interrupt Status     |
| 0x20   | SSIICR      | QSSI Interrupt Clear             |
| 0x24   | SSIDMACTL   | QSSI DMA Control                 |
| 0xFC0  | SSIPP       | QSSI Peripheral Properties       |
| 0xFC8  | SSICC       | QSSI Clock Configuration         |
| 0xFD0  | SSIPerphID4 | QSSI Peripheral Identification 4 |
| 0xFD4  | SSIPerphID5 | QSSI Peripheral Identification 5 |
| 0xFD8  | SSIPerphID6 | QSSI Peripheral Identification 6 |
| 0xFDC  | SSIPerphID7 | QSSI Peripheral Identification 7 |
| 0xFE0  | SSIPerphID0 | QSSI Peripheral Identification 0 |
| 0xFE4  | SSIPerphID1 | QSSI Peripheral Identification 1 |
| 0xFE8  | SSIPerphID2 | QSSI Peripheral Identification 2 |
| 0xFEC  | SSIPerphID3 | QSSI Peripheral Identification 3 |
| 0xFF0  | SSIPCellID0 | QSSI PrimeCell Identification 0  |
| 0xFF4  | SSIPCellID1 | QSSI PrimeCell Identification 1  |
| 0xFF8  | SSIPCellID2 | QSSI PrimeCell Identification 2  |
| 0xFFC  | SSIPCellID3 | QSSI PrimeCell Identification 3  |

表 6-26. SHA/MD5 Registers

| OFFSET | ACRONYM       | REGISTER NAME      |
|--------|---------------|--------------------|
| 0x000  | SHA_ODIGEST_A | SHA Outer Digest A |
| 0x004  | SHA_ODIGEST_B | SHA Outer Digest B |
| 0x008  | SHA_ODIGEST_C | SHA Outer Digest C |
| 0x00C  | SHA_ODIGEST_D | SHA Outer Digest D |
| 0x010  | SHA_ODIGEST_E | SHA Outer Digest E |
| 0x014  | SHA_ODIGEST_F | SHA Outer Digest F |
| 0x018  | SHA_ODIGEST_G | SHA Outer Digest G |
| 0x01C  | SHA_ODIGEST_H | SHA Outer Digest H |

**表 6-26. SHA/MD5 Registers (continued)**

| OFFSET | ACRONYM          | REGISTER NAME            |
|--------|------------------|--------------------------|
| 0x020  | SHA_IDIGEST_A    | SHA Inner Digest A       |
| 0x024  | SHA_IDIGEST_B    | SHA Inner Digest B       |
| 0x028  | SHA_IDIGEST_C    | SHA Inner Digest C       |
| 0x02C  | SHA_IDIGEST_D    | SHA Inner Digest D       |
| 0x030  | SHA_IDIGEST_E    | SHA Inner Digest E       |
| 0x034  | SHA_IDIGEST_F    | SHA Inner Digest F       |
| 0x038  | SHA_IDIGEST_G    | SHA Inner Digest G       |
| 0x03C  | SHA_IDIGEST_H    | SHA Inner Digest H       |
| 0x40   | SHA_DIGEST_COUNT | SHA Digest Count         |
| 0x44   | SHA_MODE         | SHA Mode                 |
| 0x48   | SHA_LENGTH       | SHA Length               |
| 0x080  | SHA_DATA_0_IN    | SHA Data 0 Input         |
| 0x084  | SHA_DATA_1_IN    | SHA Data 1 Input         |
| 0x088  | SHA_DATA_2_IN    | SHA Data 2 Input         |
| 0x08C  | SHA_DATA_3_IN    | SHA Data 3 Input         |
| 0x090  | SHA_DATA_4_IN    | SHA Data 4 Input         |
| 0x094  | SHA_DATA_5_IN    | SHA Data 5 Input         |
| 0x098  | SHA_DATA_6_IN    | SHA Data 6 Input         |
| 0x09C  | SHA_DATA_7_IN    | SHA Data 7 Input         |
| 0x0A0  | SHA_DATA_8_IN    | SHA Data 8 Input         |
| 0x0A4  | SHA_DATA_9_IN    | SHA Data 9 Input         |
| 0x0A8  | SHA_DATA_10_IN   | SHA Data 10 Input        |
| 0x0AC  | SHA_DATA_11_IN   | SHA Data 11 Input        |
| 0x0B0  | SHA_DATA_12_IN   | SHA Data 12 Input        |
| 0x0B4  | SHA_DATA_13_IN   | SHA Data 13 Input        |
| 0x0B8  | SHA_DATA_14_IN   | SHA Data 14 Input        |
| 0x0BC  | SHA_DATA_15_IN   | SHA Data 15 Input        |
| 0x100  | SHA_REVISION     | SHA Revision             |
| 0x110  | SHA_SYSCONFIG    | SHA System Configuration |
| 0x114  | SHA_SYSSTATUS    | SHA System Status        |
| 0x118  | SHA_IRQSTATUS    | SHA Interrupt Status     |
| 0x11C  | SHA_IRQENABLE    | SHA Interrupt Enable     |

**表 6-27. SHA/MD5  $\mu$ DMA Registers**

| OFFSET | ACRONYM    | REGISTER NAME                   |
|--------|------------|---------------------------------|
| 0x10   | SHA_DMAIM  | SHA DMA Interrupt Mask          |
| 0x14   | SHA_DMARIS | SHA DMA Raw Interrupt Status    |
| 0x18   | SHA_DMAMIS | SHA DMA Masked Interrupt Status |
| 0x1C   | SHA_DMAIC  | SHA DMA Interrupt Clear         |

**表 6-28. System Control Memory Registers**

| OFFSET         | ACRONYM                  | REGISTER NAME                                                                   |
|----------------|--------------------------|---------------------------------------------------------------------------------|
| 0xD4           | RVP                      | Reset Vector Pointer                                                            |
| 0x1D0          | BOOTCFG                  | Boot Configuration                                                              |
| 0x1E0 to 0x1EC | USER_REG_0 to USER_REG_3 | User Register 0 to User Register 3                                              |
| 0x200 to 0x23C | FMPRE_0 to FMPRE_15      | Flash Memory Protection Read Enable 0 to Flash Memory Protection Read Enable 15 |

表 6-28. System Control Memory Registers (continued)

| OFFSET         | ACRONYM             | REGISTER NAME                                                                         |
|----------------|---------------------|---------------------------------------------------------------------------------------|
| 0x400 to 0x43C | FMPPE_0 to FMPPE_15 | Flash Memory Protection Program Enable 0 to Flash Memory Protection Program Enable 15 |

表 6-29. System Exception Registers

| OFFSET | ACRONYM  | REGISTER NAME                            |
|--------|----------|------------------------------------------|
| 0x0    | SYSEXCRI | System Exception Raw Interrupt Status    |
| 0x4    | SYSEXCIM | System Exception Interrupt Mask          |
| 0x8    | SYSEXCMI | System Exception Masked Interrupt Status |
| 0xC    | SYSEXCIC | System Exception Interrupt Clear         |

表 6-30. UART Registers

| OFFSET | ACRONYM          | REGISTER NAME                     |
|--------|------------------|-----------------------------------|
| 0x0    | UARTDR           | UART Data                         |
| 0x4    | UARTSR/UARTCR    | UART Receive Status/Error Clear   |
| 0x18   | UARTFR           | UART Flag                         |
| 0x20   | UARTILPR         | UART IrDA Low-Power Register      |
| 0x24   | UARTIBRD         | UART Integer Baud-Rate Divisor    |
| 0x28   | UARTFBRD         | UART Fractional Baud-Rate Divisor |
| 0x2C   | UARTLCRH         | UART Line Control                 |
| 0x30   | UARTCTL          | UART Control                      |
| 0x34   | UARTIFLS         | UART Interrupt FIFO Level Select  |
| 0x38   | UARTIM           | UART Interrupt Mask               |
| 0x3C   | UARTIRIS         | UART Raw Interrupt Status         |
| 0x40   | UARTMIS          | UART Masked Interrupt Status      |
| 0x44   | UARTICR          | UART Interrupt Clear              |
| 0x48   | UARTDMACTL       | UART DMA Control                  |
| 0xA4   | UART9BITADDR     | UART 9-Bit Self Address           |
| 0xA8   | UART9BITAMASK    | UART 9-Bit Self Address Mask      |
| 0xFC0  | UARTPP           | UART Peripheral Properties        |
| 0xFC8  | UARTCC           | UART Clock Configuration          |
| 0xFD0  | UARTPeriphID4    | UART Peripheral Identification 4  |
| 0xFD4  | UARTPeriphID5    | UART Peripheral Identification 5  |
| 0xFD8  | UARTPeriphID6    | UART Peripheral Identification 6  |
| 0xFDC  | UARTPeriphID7    | UART Peripheral Identification 7  |
| 0xFE0  | UARTPeriphID0    | UART Peripheral Identification 0  |
| 0xFE4  | UARTPeriphID1    | UART Peripheral Identification 1  |
| 0xFE8  | UARTPeriphID2    | UART Peripheral Identification 2  |
| 0xFEC  | UARTPeriphID3    | UART Peripheral Identification 3  |
| 0xFF0  | UARTPrimeCellID0 | UART PrimeCell Identification 0   |
| 0xFF4  | UARTPrimeCellID1 | UART PrimeCell Identification 1   |
| 0xFF8  | UARTPrimeCellID2 | UART PrimeCell Identification 2   |
| 0xFFC  | UARTPrimeCellID3 | UART PrimeCell Identification 3   |

表 6-31. USB Registers

| OFFSET | ACRONYM  | REGISTER NAME                 |
|--------|----------|-------------------------------|
| 0x0    | USBFADDR | USB Device Functional Address |
| 0x1    | USBPOWER | USB Power                     |

**表 6-31. USB Registers (continued)**

| OFFSET | ACRONYM        | REGISTER NAME                                          |
|--------|----------------|--------------------------------------------------------|
| 0x2    | USBTXIS        | USB Transmit Interrupt Status                          |
| 0x4    | USBRXIS        | USB Receive Interrupt Status                           |
| 0x6    | USBTXIE        | USB Transmit Interrupt Enable                          |
| 0x8    | USBRXIE        | USB Receive Interrupt Enable                           |
| 0xA    | USBIS          | USB General Interrupt Status                           |
| 0xB    | USBIE          | USB Interrupt Enable                                   |
| 0xC    | USBFRAME       | USB Frame Value                                        |
| 0xE    | USBEPIDX       | USB Endpoint Index                                     |
| 0xF    | USBTEST        | USB Test Mode                                          |
| 0x20   | USBFIFO0       | USB FIFO Endpoint 0                                    |
| 0x24   | USBFIFO1       | USB FIFO Endpoint 1                                    |
| 0x28   | USBFIFO2       | USB FIFO Endpoint 2                                    |
| 0x2C   | USBFIFO3       | USB FIFO Endpoint 3                                    |
| 0x30   | USBFIFO4       | USB FIFO Endpoint 4                                    |
| 0x34   | USBFIFO5       | USB FIFO Endpoint 5                                    |
| 0x38   | USBFIFO6       | USB FIFO Endpoint 6                                    |
| 0x3C   | USBFIFO7       | USB FIFO Endpoint 7                                    |
| 0x60   | USBDEVCTL      | USB Device Control                                     |
| 0x61   | USBCCONF       | USB Common Configuration                               |
| 0x62   | USBTXFIFOSZ    | USB Transmit Dynamic FIFO Sizing                       |
| 0x63   | USBRXFIFOSZ    | USB Receive Dynamic FIFO Sizing                        |
| 0x64   | USBTXFIFOADD   | USB Transmit FIFO Start Address                        |
| 0x66   | USBRXFIFOADD   | USB Receive FIFO Start Address                         |
| 0x70   | ULPIVBUSCTL    | USB ULPI VBUS Control                                  |
| 0x74   | ULPIREGDATA    | USB ULPI Register Data                                 |
| 0x75   | ULPIREGADDR    | USB ULPI Register Address                              |
| 0x76   | ULPIREGCTL     | USB ULPI Register Control                              |
| 0x78   | USBEPINFO      | USB Endpoint Information                               |
| 0x79   | USBRAMINFO     | USB RAM Information                                    |
| 0x7A   | USBCONTIM      | USB Connect Timing                                     |
| 0x7B   | USBVPLEN       | USB OTG VBUS Pulse Timing                              |
| 0x7C   | USBHSEOF       | USB High-Speed Last Transaction to End of Frame Timing |
| 0x7D   | USBFSEOF       | USB Full-Speed Last Transaction to End of Frame Timing |
| 0x7E   | USBLSEOF       | USB Low-Speed Last Transaction to End of Frame Timing  |
| 0x80   | USBTXFUNCADDR0 | USB Transmit Functional Address Endpoint 0             |
| 0x82   | USBTXHUBADDR0  | USB Transmit Hub Address Endpoint 0                    |
| 0x83   | USBTXHUBPORT0  | USB Transmit Hub Port Endpoint 0                       |
| 0x88   | USBTXFUNCADDR1 | USB Transmit Functional Address Endpoint 1             |
| 0x8A   | USBTXHUBADDR1  | USB Transmit Hub Address Endpoint 1                    |
| 0x8B   | USBTXHUBPORT1  | USB Transmit Hub Port Endpoint 1                       |
| 0x8C   | USBRXFUNCADDR1 | USB Receive Functional Address Endpoint 1              |
| 0x8E   | USBRXHUBADDR1  | USB Receive Hub Address Endpoint 1                     |
| 0x8F   | USBRXHUBPORT1  | USB Receive Hub Port Endpoint 1                        |
| 0x90   | USBTXFUNCADDR2 | USB Transmit Functional Address Endpoint 2             |
| 0x92   | USBTXHUBADDR2  | USB Transmit Hub Address Endpoint 2                    |
| 0x93   | USBTXHUBPORT2  | USB Transmit Hub Port Endpoint 2                       |
| 0x94   | USBRXFUNCADDR2 | USB Receive Functional Address Endpoint 2              |

表 6-31. USB Registers (continued)

| OFFSET | ACRONYM        | REGISTER NAME                                   |
|--------|----------------|-------------------------------------------------|
| 0x96   | USBRXHUBADDR2  | USB Receive Hub Address Endpoint 2              |
| 0x97   | USBRXHUBPORT2  | USB Receive Hub Port Endpoint 2                 |
| 0x98   | USBTXFUNCADDR3 | USB Transmit Functional Address Endpoint 3      |
| 0x9A   | USBTXHUBADDR3  | USB Transmit Hub Address Endpoint 3             |
| 0x9B   | USBTXHUBPORT3  | USB Transmit Hub Port Endpoint 3                |
| 0x9C   | USBRXFUNCADDR3 | USB Receive Functional Address Endpoint 3       |
| 0x9E   | USBRXHUBADDR3  | USB Receive Hub Address Endpoint 3              |
| 0x9F   | USBRXHUBPORT3  | USB Receive Hub Port Endpoint 3                 |
| 0xA0   | USBTXFUNCADDR4 | USB Transmit Functional Address Endpoint 4      |
| 0xA2   | USBTXHUBADDR4  | USB Transmit Hub Address Endpoint 4             |
| 0xA3   | USBTXHUBPORT4  | USB Transmit Hub Port Endpoint 4                |
| 0xA4   | USBRXFUNCADDR4 | USB Receive Functional Address Endpoint 4       |
| 0xA6   | USBRXHUBADDR4  | USB Receive Hub Address Endpoint 4              |
| 0xA7   | USBRXHUBPORT4  | USB Receive Hub Port Endpoint 4                 |
| 0xA8   | USBTXFUNCADDR5 | USB Transmit Functional Address Endpoint 5      |
| 0xAA   | USBTXHUBADDR5  | USB Transmit Hub Address Endpoint 5             |
| 0xAB   | USBTXHUBPORT5  | USB Transmit Hub Port Endpoint 5                |
| 0xAC   | USBRXFUNCADDR5 | USB Receive Functional Address Endpoint 5       |
| 0xAE   | USBRXHUBADDR5  | USB Receive Hub Address Endpoint 5              |
| 0xAF   | USBRXHUBPORT5  | USB Receive Hub Port Endpoint 5                 |
| 0xB0   | USBTXFUNCADDR6 | USB Transmit Functional Address Endpoint 6      |
| 0xB2   | USBTXHUBADDR6  | USB Transmit Hub Address Endpoint 6             |
| 0xB3   | USBTXHUBPORT6  | USB Transmit Hub Port Endpoint 6                |
| 0xB4   | USBRXFUNCADDR6 | USB Receive Functional Address Endpoint 6       |
| 0xB6   | USBRXHUBADDR6  | USB Receive Hub Address Endpoint 6              |
| 0xB7   | USBRXHUBPORT6  | USB Receive Hub Port Endpoint 6                 |
| 0xB8   | USBTXFUNCADDR7 | USB Transmit Functional Address Endpoint 7      |
| 0xBA   | USBTXHUBADDR7  | USB Transmit Hub Address Endpoint 7             |
| 0xBB   | USBTXHUBPORT7  | USB Transmit Hub Port Endpoint 7                |
| 0xBC   | USBRXFUNCADDR7 | USB Receive Functional Address Endpoint 7       |
| 0xBE   | USBRXHUBADDR7  | USB Receive Hub Address Endpoint 7              |
| 0xBF   | USBRXHUBPORT7  | USB Receive Hub Port Endpoint 7                 |
| 0x102  | USBCSRL0       | USB Control and Status Endpoint 0 Low           |
| 0x103  | USBCSRH0       | USB Control and Status Endpoint 0 High          |
| 0x108  | USBCOUNT0      | USB Receive Byte Count Endpoint 0               |
| 0x10A  | USBTTYPE0      | USB Type Endpoint 0                             |
| 0x10B  | USBNAKLMT      | USB NAK Limit                                   |
| 0x110  | USBTXMAXP1     | USB Maximum Transmit Data Endpoint 1            |
| 0x112  | USBTXCSRL1     | USB Transmit Control and Status Endpoint 1 Low  |
| 0x113  | USBTXCSRH1     | USB Transmit Control and Status Endpoint 1 High |
| 0x114  | USBRXMAXP1     | USB Maximum Receive Data Endpoint 1             |
| 0x116  | USBRXCSRL1     | USB Receive Control and Status Endpoint 1 Low   |
| 0x117  | USBRXCSRH1     | USB Receive Control and Status Endpoint 1 High  |
| 0x118  | USBRXCOUNT1    | USB Receive Byte Count Endpoint 1               |
| 0x11A  | USBTXTYPE1     | USB Host Transmit Configure Type Endpoint 1     |
| 0x11B  | USBTXINTERVAL1 | USB Host Transmit Interval Endpoint 1           |
| 0x11C  | USBRXTYPE1     | USB Host Configure Receive Type Endpoint 1      |

**表 6-31. USB Registers (continued)**

| OFFSET | ACRONYM        | REGISTER NAME                                   |
|--------|----------------|-------------------------------------------------|
| 0x11D  | USBRXINTERVAL1 | USB Host Receive Polling Interval Endpoint 1    |
| 0x120  | USBTXMAXP2     | USB Maximum Transmit Data Endpoint 2            |
| 0x122  | USBTXCSRL2     | USB Transmit Control and Status Endpoint 2 Low  |
| 0x123  | USBTXCSRH2     | USB Transmit Control and Status Endpoint 2 High |
| 0x124  | USBRXMAXP2     | USB Maximum Receive Data Endpoint 2             |
| 0x126  | USBRXCSRL2     | USB Receive Control and Status Endpoint 2 Low   |
| 0x127  | USBRXCSRH2     | USB Receive Control and Status Endpoint 2 High  |
| 0x128  | USBRXCOUNT2    | USB Receive Byte Count Endpoint 2               |
| 0x12A  | USBTXTYPE2     | USB Host Transmit Configure Type Endpoint 2     |
| 0x12B  | USBTXINTERVAL2 | USB Host Transmit Interval Endpoint 2           |
| 0x12C  | USBRXTYPE2     | USB Host Configure Receive Type Endpoint 2      |
| 0x12D  | USBRXINTERVAL2 | USB Host Receive Polling Interval Endpoint 2    |
| 0x130  | USBTXMAXP3     | USB Maximum Transmit Data Endpoint 3            |
| 0x132  | USBTXCSRL3     | USB Transmit Control and Status Endpoint 3 Low  |
| 0x133  | USBTXCSRH3     | USB Transmit Control and Status Endpoint 3 High |
| 0x134  | USBRXMAXP3     | USB Maximum Receive Data Endpoint 3             |
| 0x136  | USBRXCSRL3     | USB Receive Control and Status Endpoint 3 Low   |
| 0x137  | USBRXCSRH3     | USB Receive Control and Status Endpoint 3 High  |
| 0x138  | USBRXCOUNT3    | USB Receive Byte Count Endpoint 3               |
| 0x13A  | USBTXTYPE3     | USB Host Transmit Configure Type Endpoint 3     |
| 0x13B  | USBTXINTERVAL3 | USB Host Transmit Interval Endpoint 3           |
| 0x13C  | USBRXTYPE3     | USB Host Configure Receive Type Endpoint 3      |
| 0x13D  | USBRXINTERVAL3 | USB Host Receive Polling Interval Endpoint 3    |
| 0x140  | USBTXMAXP4     | USB Maximum Transmit Data Endpoint 4            |
| 0x142  | USBTXCSRL4     | USB Transmit Control and Status Endpoint 4 Low  |
| 0x143  | USBTXCSRH4     | USB Transmit Control and Status Endpoint 4 High |
| 0x144  | USBRXMAXP4     | USB Maximum Receive Data Endpoint 4             |
| 0x146  | USBRXCSRL4     | USB Receive Control and Status Endpoint 4 Low   |
| 0x147  | USBRXCSRH4     | USB Receive Control and Status Endpoint 4 High  |
| 0x148  | USBRXCOUNT4    | USB Receive Byte Count Endpoint 4               |
| 0x14A  | USBTXTYPE4     | USB Host Transmit Configure Type Endpoint 4     |
| 0x14B  | USBTXINTERVAL4 | USB Host Transmit Interval Endpoint 4           |
| 0x14C  | USBRXTYPE4     | USB Host Configure Receive Type Endpoint 4      |
| 0x14D  | USBRXINTERVAL4 | USB Host Receive Polling Interval Endpoint 4    |
| 0x150  | USBTXMAXP5     | USB Maximum Transmit Data Endpoint 5            |
| 0x152  | USBTXCSRL5     | USB Transmit Control and Status Endpoint 5 Low  |
| 0x153  | USBTXCSRH5     | USB Transmit Control and Status Endpoint 5 High |
| 0x154  | USBRXMAXP5     | USB Maximum Receive Data Endpoint 5             |
| 0x156  | USBRXCSRL5     | USB Receive Control and Status Endpoint 5 Low   |
| 0x157  | USBRXCSRH5     | USB Receive Control and Status Endpoint 5 High  |
| 0x158  | USBRXCOUNT5    | USB Receive Byte Count Endpoint 5               |
| 0x15A  | USBTXTYPE5     | USB Host Transmit Configure Type Endpoint 5     |
| 0x15B  | USBTXINTERVAL5 | USB Host Transmit Interval Endpoint 5           |
| 0x15C  | USBRXTYPE5     | USB Host Configure Receive Type Endpoint 5      |
| 0x15D  | USBRXINTERVAL5 | USB Host Receive Polling Interval Endpoint 5    |
| 0x160  | USBTXMAXP6     | USB Maximum Transmit Data Endpoint 6            |
| 0x162  | USBTXCSRL6     | USB Transmit Control and Status Endpoint 6 Low  |

表 6-31. USB Registers (continued)

| OFFSET | ACRONYM        | REGISTER NAME                                         |
|--------|----------------|-------------------------------------------------------|
| 0x163  | USBTXCSRH6     | USB Transmit Control and Status Endpoint 6 High       |
| 0x164  | USBRXMAXP6     | USB Maximum Receive Data Endpoint 6                   |
| 0x166  | USBRXCSSL6     | USB Receive Control and Status Endpoint 6 Low         |
| 0x167  | USBRXCSRH6     | USB Receive Control and Status Endpoint 6 High        |
| 0x168  | USBRXCOUNT6    | USB Receive Byte Count Endpoint 6                     |
| 0x16A  | USBTXTYPE6     | USB Host Transmit Configure Type Endpoint 6           |
| 0x16B  | USBTXINTERVAL6 | USB Host Transmit Interval Endpoint 6                 |
| 0x16C  | USBRXTYPE6     | USB Host Configure Receive Type Endpoint 6            |
| 0x16D  | USBRXINTERVAL6 | USB Host Receive Polling Interval Endpoint 6          |
| 0x170  | USBTXMAXP7     | USB Maximum Transmit Data Endpoint 7                  |
| 0x172  | USBTXCSSL7     | USB Transmit Control and Status Endpoint 7 Low        |
| 0x173  | USBTXCSRH7     | USB Transmit Control and Status Endpoint 7 High       |
| 0x174  | USBRXMAXP7     | USB Maximum Receive Data Endpoint 7                   |
| 0x176  | USBRXCSSL7     | USB Receive Control and Status Endpoint 7 Low         |
| 0x177  | USBRXCSRH7     | USB Receive Control and Status Endpoint 7 High        |
| 0x178  | USBRXCOUNT7    | USB Receive Byte Count Endpoint 7                     |
| 0x17A  | USBTXTYPE7     | USB Host Transmit Configure Type Endpoint 7           |
| 0x17B  | USBTXINTERVAL7 | USB Host Transmit Interval Endpoint 7                 |
| 0x17C  | USBRXTYPE7     | USB Host Configure Receive Type Endpoint 7            |
| 0x17D  | USBRXINTERVAL7 | USB Host Receive Polling Interval Endpoint 7          |
| 0x200  | USBDMAINTR     | USB DMA Interrupt                                     |
| 0x204  | USBDMACTL0     | USB DMA Control 0                                     |
| 0x208  | USBDMAADDR0    | USB DMA Address 0                                     |
| 0x20C  | USBDMACOUNT0   | USB DMA Count 0                                       |
| 0x214  | USBDMACTL1     | USB DMA Control 1                                     |
| 0x218  | USBDMAADDR1    | USB DMA Address 1                                     |
| 0x21C  | USBDMACOUNT1   | USB DMA Count 1                                       |
| 0x224  | USBDMACTL2     | USB DMA Control 2                                     |
| 0x228  | USBDMAADDR2    | USB DMA Address 2                                     |
| 0x22C  | USBDMACOUNT2   | USB DMA Count 2                                       |
| 0x234  | USBDMACTL3     | USB DMA Control 3                                     |
| 0x238  | USBDMAADDR3    | USB DMA Address 3                                     |
| 0x23C  | USBDMACOUNT3   | USB DMA Count 3                                       |
| 0x244  | USBDMACTL4     | USB DMA Control 4                                     |
| 0x248  | USBDMAADDR4    | USB DMA Address 4                                     |
| 0x24C  | USBDMACOUNT4   | USB DMA Count 4                                       |
| 0x254  | USBDMACTL5     | USB DMA Control 5                                     |
| 0x258  | USBDMAADDR5    | USB DMA Address 5                                     |
| 0x25C  | USBDMACOUNT5   | USB DMA Count 5                                       |
| 0x264  | USBDMACTL6     | USB DMA Control 6                                     |
| 0x268  | USBDMAADDR6    | USB DMA Address 6                                     |
| 0x26C  | USBDMACOUNT6   | USB DMA Count 6                                       |
| 0x274  | USBDMACTL7     | USB DMA Control 7                                     |
| 0x278  | USBDMAADDR7    | USB DMA Address 7                                     |
| 0x27C  | USBDMACOUNT7   | USB DMA Count 7                                       |
| 0x304  | USBRQPKTCOUNT1 | USB Request Packet Count in Block Transfer Endpoint 1 |
| 0x308  | USBRQPKTCOUNT2 | USB Request Packet Count in Block Transfer Endpoint 2 |

**表 6-31. USB Registers (continued)**

| OFFSET | ACRONYM         | REGISTER NAME                                         |
|--------|-----------------|-------------------------------------------------------|
| 0x30C  | USBRQPKTCOUNT3  | USB Request Packet Count in Block Transfer Endpoint 3 |
| 0x310  | USBRQPKTCOUNT4  | USB Request Packet Count in Block Transfer Endpoint 4 |
| 0x314  | USBRQPKTCOUNT5  | USB Request Packet Count in Block Transfer Endpoint 5 |
| 0x318  | USBRQPKTCOUNT6  | USB Request Packet Count in Block Transfer Endpoint 6 |
| 0x31C  | USBRQPKTCOUNT7  | USB Request Packet Count in Block Transfer Endpoint 7 |
| 0x340  | USBRXDPKTBUFDIS | USB Receive Double Packet Buffer Disable              |
| 0x342  | USBTXDPKTBUFDIS | USB Transmit Double Packet Buffer Disable             |
| 0x344  | USBCTO          | USB Chirp Time-out                                    |
| 0x346  | USBHHSRTN       | USB High Speed to UTM Operating Delay                 |
| 0x348  | USBHSBT         | USB High Speed Time-out Adder                         |
| 0x360  | USBLPMATTR      | USB LPM Attributes                                    |
| 0x362  | USBLPMCNTL      | USB LPM Control                                       |
| 0x363  | USBLPMIM        | USB LPM Interrupt Mask                                |
| 0x364  | USBLPMRIS       | USB LPM Raw Interrupt Status                          |
| 0x365  | USBLPMFADDR     | USB LPM Function Address                              |
| 0x400  | USBEPIC         | USB External Power Control                            |
| 0x404  | USBEPICRIS      | USB External Power Control Raw Interrupt Status       |
| 0x408  | USBEPICIM       | USB External Power Control Interrupt Mask             |
| 0x40C  | USBEPICISC      | USB External Power Control Interrupt Status and Clear |
| 0x410  | USBDRRIS        | USB Device RESUME Raw Interrupt Status                |
| 0x414  | USBDRIM         | USB Device RESUME Interrupt Mask                      |
| 0x418  | USBDRISC        | USB Device RESUME Interrupt Status and Clear          |
| 0x41C  | USBGPCS         | USB General-Purpose Control and Status                |
| 0x430  | USBVDC          | USB VBUS Droop Control                                |
| 0x434  | USBVDCRIS       | USB VBUS Droop Control Raw Interrupt Status           |
| 0x438  | USBVDCIM        | USB VBUS Droop Control Interrupt Mask                 |
| 0x43C  | USBVDCISC       | USB VBUS Droop Control Interrupt Status and Clear     |
| 0xFC0  | USBPP           | USB Peripheral Properties                             |
| 0xFC4  | USBPC           | USB Peripheral Configuration                          |
| 0xFC8  | USBC            | USB Clock Configuration                               |

**表 6-32. WDT Registers**

| OFFSET | ACRONYM      | REGISTER NAME                        |
|--------|--------------|--------------------------------------|
| 0x0    | WDTLOAD      | Watchdog Load                        |
| 0x4    | WDTVALUE     | Watchdog Value                       |
| 0x8    | WDTCTL       | Watchdog Control                     |
| 0xC    | WDTICR       | Watchdog Interrupt Clear             |
| 0x10   | WDTISR       | Watchdog Raw Interrupt Status        |
| 0x14   | WDTMIS       | Watchdog Masked Interrupt Status     |
| 0x418  | WDTTEST      | Watchdog Test                        |
| 0xC00  | WDTLOCK      | Watchdog Lock                        |
| 0xFD0  | WDTPeriphID4 | Watchdog Peripheral Identification 4 |
| 0xFD4  | WDTPeriphID5 | Watchdog Peripheral Identification 5 |
| 0xFD8  | WDTPeriphID6 | Watchdog Peripheral Identification 6 |
| 0xFDC  | WDTPeriphID7 | Watchdog Peripheral Identification 7 |
| 0xFE0  | WDTPeriphID0 | Watchdog Peripheral Identification 0 |
| 0xFE4  | WDTPeriphID1 | Watchdog Peripheral Identification 1 |

表 6-32. WDT Registers (continued)

| OFFSET | ACRONYM      | REGISTER NAME                        |
|--------|--------------|--------------------------------------|
| 0xFE8  | WDTPeriphID2 | Watchdog Peripheral Identification 2 |
| 0xFEC  | WDTPeriphID3 | Watchdog Peripheral Identification 3 |
| 0xFF0  | WDTPCellID0  | Watchdog PrimeCell Identification 0  |
| 0xFF4  | WDTPCellID1  | Watchdog PrimeCell Identification 1  |
| 0xFF8  | WDTPCellID2  | Watchdog PrimeCell Identification 2  |
| 0xFFC  | WDTPCellID3  | Watchdog PrimeCell Identification 3  |

## 6.6 Identification

### Device Identification

Read-only registers in the system control module provide information about the MCU, such as version, part number, pin count, operating temperature range, and available peripherals on the device. The Device Identification 0 (DID0) and Device Identification 1 (DID1) registers provide details about the version, package, and temperature range of the device. The peripheral present registers starting at system control offset 0x300, such as the Watchdog Timer Peripheral Present (PPWD) register, provide information on how many of each type of module are included on the device. Finally, information about the capabilities of the on-chip peripherals are provided at offset 0xFC0 in the register space of each peripheral in the peripheral properties registers, such as the GPTM Peripheral Properties (GPTMPP). In addition, four unique identifier registers, Unique Identifier n (UNIQUEIDn), provide a 128-bit unique identifier that cannot be modified for each device.

### JTAG Identification

图 6-3 shows the format for the 32-bit IDCODE Data Register defined by the IEEE Standard 1149.1. The major uses of the JTAG port are for manufacturer testing of component assembly and program development and debug. To facilitate the use of auto-configuration debug tools, the IDCODE instruction outputs a value of 0x4BA0.0477. This value lets the debuggers automatically configure themselves to work correctly with the Cortex-M4F during debug.

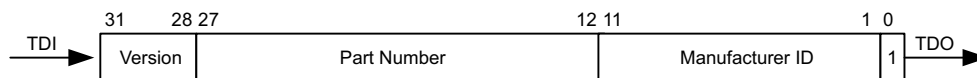


图 6-3. IDCODE Register Format

### ROM Version

The internal ROM is at address 0x0100.0000 of the device memory map.

## 6.7 Boot Modes

After POR and device initialization occurs, the hardware loads the stack pointer from either flash or ROM, based on the presence of an application in flash and the state of the EN bit in the BOOTCFG register.

If the flash address 0x0000.0004 contains an erased word (value 0xFFFF.FFFF) or the EN bit is of the BOOTCFG register is clear, the stack pointer and reset vector pointer are loaded from ROM at address 0x0100.0000 and 0x0100.0004, respectively. The bootloader executes and configures the available boot slave interfaces and waits for a programmer, host PC, or boot server to load its software. The bootloader uses a simple packet interface to provide synchronous communication with the device for I<sup>2</sup>C, SSI, and UART. The speed of the bootloader is determined by the frequency of the internal oscillator (PIOSC) or external crystal (if connected).

The ROM invokes the USB and Ethernet bootloader only when an external crystal is detected. Also, the Ethernet bootloader works only when a 25-MHz crystal is detected.

The following serial interfaces can be used:

- UART0
- SSI0
- I2C0
- USB
- Ethernet MAC and Integrated PHY

If the check of the flash at address 0x0000.0004 contains a valid reset vector value and the EN bit in the BOOTCFG register is set, the stack pointer and reset vector values are fetched from the beginning of flash. This application stack pointer and reset vector are loaded and the processor executes the application directly. Otherwise, the stack pointer and reset vector values are fetched from the beginning of ROM.

## 7 Applications, Implementation, and Layout

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### 注

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

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### 7.1 System Design Guidelines

The SimpleLink MSP432E4 microcontrollers are highly-integrated system-on-chip (SoC) devices with extensive interface and processing capabilities. Consequently, there are many factors to consider when creating a schematic and designing a circuit board. By following the recommendations in this design guide, your confidence will increase that the board will work successfully upon initial power up.

[System Design Guidelines for MSP432E4 SimpleLink™ Microcontrollers](#)

## 8 器件和文档支持

### 8.1 入门和后续步骤

TI 提供大量的开发工具。下面是用于评估器件性能、生成代码和开发解决方案的工具和软件。

### 8.2 器件命名规则

为了指出产品开发周期所处的阶段，TI 为所有微处理器 (MPU) 和支持工具的产品型号分配了前缀。每个器件都具有以下三个前缀中的其中一个：XMS、PMS 或 MSP。这些前缀代表了产品开发的发展阶段，即从工程原型直到完全合格的生产器件和工具。

器件开发进化流程：

**XMS** 试验器件不一定代表最终器件的电气规范标准，并且可能不使用生产组装流程。

**PMS** 原型器件不一定是最终器件模型，并且不一定符合最终电气标准规范。

**MSP** 完全合格的器件模型的生产版本。

试验器件和工具在供货时附带如下免责声明：

“开发中的产品用于内部评估用途。”

生产器件和开发支持工具已进行完全特性描述，并且器件的质量和可靠性已经完全论证。TI 的标准保修证书适用。

预测显示原型器件的故障率大于标准生产器件。由于这些器件的预计最终使用故障率仍未定义，德州仪器 (TI) 建议不要将它们用于任何生产系统。只有合格的产品器件将被使用。

TI 器件的命名规则也包括一个带有器件系列名称的后缀。这个后缀表示封装类型（例如，ZAD）和温度范围（例如，“空白”是默认的商业级温度范围）。图 8-1 显示了完整器件名称的解读图例。

有关器件的订购部件号，请参阅本文档的封装选项附录、[ti.com.cn](http://ti.com.cn) 或者与您的 TI 销售代表联系。

有关裸片器件命名规则标记的其他说明，请参阅具体器件的《器件勘误表》。

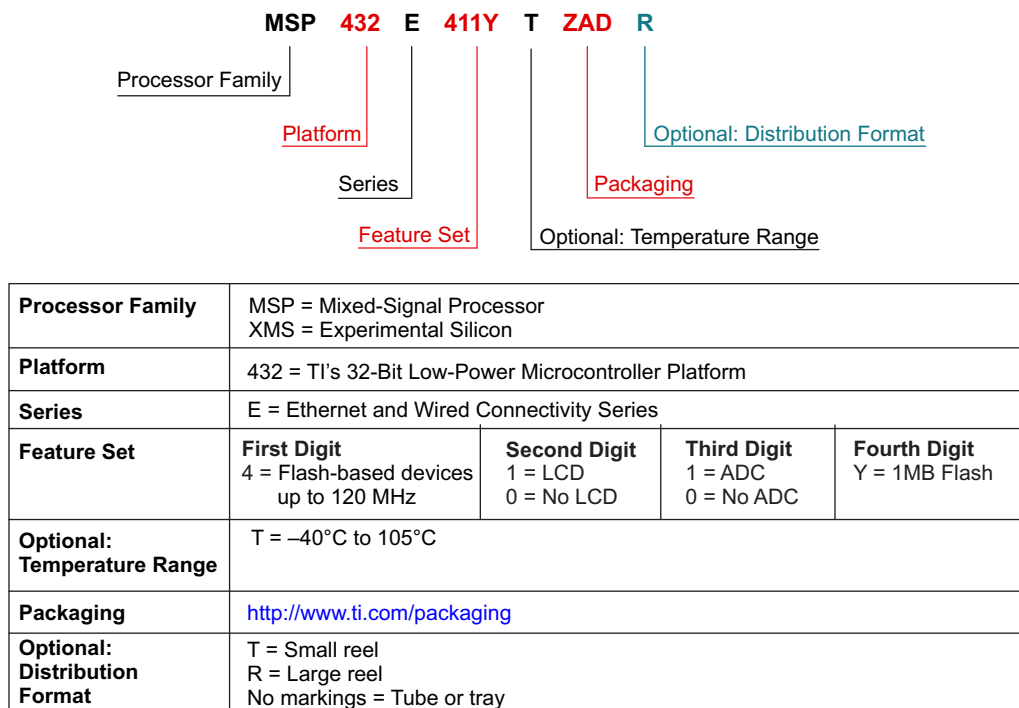


图 8-1. 器件命名规则

## 8.3 工具和软件

### 设计套件与评估模块

**MSP432E401Y SimpleLink 微控制器 LaunchPad 开发套件** SimpleLink 以太网 MSP432E401Y 微控制器 LaunchPad 开发套件是一款适用于基于 SimpleLink Arm Cortex-M4F 以太网微控制器的低成本评估平台。以太网 LaunchPad 开发套件设计的重点突出了 MSP432E401Y 微控制器及其片上 10/100 以太网 MAC 和 PHY、USB 2.0、休眠模块、运动控制脉宽调制以及大量同步串行连接。

### 软件

**SimpleLink MSP432E4 软件开发套件 (SDK)** MSP432E4 SDK 是一套综合性的软件包，可帮助工程师在德州仪器 (TI) MSP432E4 MCU 上快速开发功能强大的应用。MSP432E4 SDK 由多个兼容软件组件构成，其中包括 RTOS、驱动程序和中间件以及一些如何一起使用这些组件的示例。此外，还提供了各种示例来展示如何使用各功能区和各个受支持的器件，同时这些示例还可用作您自己的项目的起点。

### 开发工具

**适用于 MSP 微控制器的 Code Composer Studio™ 集成开发环境** Code Composer Studio 是一种集成开发环境 (IDE)，支持所有 MSP430 和 SimpleLink MSP432 微控制器器件。Code Composer Studio 包含一整套开发和调试嵌入式应用的嵌入式软件实用程序。它包含了优化的 C/C++ 编译器、源代码编辑器、项目构建环境、调试器、描述器以及其他多种功能。借助集成式 TI 资源浏览器，您可以访问适用于您的器件和开发板的更多示例、库、可执行代码和文档。有关更多信息，请参阅《适用于 SimpleLink™ MSP432™ 微控制器的 Code Composer Studio™ IDE 用户指南》。

**IAR 嵌入式工作平台 Kickstart** 适用于 MSP 的 IAR 嵌入式工作平台 Kickstart 是一套完整的调试器和 C/C++ 编译器工具链，可用于构建和调试基于 MSP430 和 SimpleLink MSP432 微控制器的嵌入式应用。MSP430 器件和 MSP432 器件的 C/C++ 编译器代码尺寸限制分别为 8KB 和 32KB。有关更多信息，请参阅《适用于 SimpleLink™ MSP432™ 微控制器的 IAR Embedded Workbench® for ARM® 用户指南》。

**Arm® Keil® MDK – 免费 32KB IDE** Arm Keil MDK 是一套完整的调试器和 C/C++ 编译器工具链，可用于构建和调试嵌入式应用。Keil MDK 支持低功耗和高性能 SimpleLink MSP432 MCU 系列，并且它还包括一个全集成调试器，适用于源代码级调试和反汇编级调试，支持复杂代码和数据断点。对于此 IDE，SimpleLink MSP432 软件开发套件 (SDK) 中仅支持非 RTOS 示例。有关更多信息，请参阅《适用于 SimpleLink™ MSP432™ 微控制器的 Arm® Keil® MDK 用户指南》。

**MSP432E CMSIS 器件系列软件包** TI 为 MSP432E 器件提供了符合 CMSIS 标准的器件系列软件包。该软件包将 MSP432E 器件支持添加到 IAR EWArm 8.x、Keil MDK 5.x 和 Atollic True Studio 7.x。在 IAR EWArm 中，该软件包是可选的，因为 IDE 本身便支持这些器件。

**适用于 MSP432 的调试器** 根据设计，SimpleLink MSP432E MCU 可与 TI 及第三方供应商的各种调试器结合使用。MSP-FET 不支持 MSP432E 器件系列。

## 8.4 文档支持

如需接收文档更新通知，请访问 [ti.com](http://ti.com) 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

以下文档描述了 MCU、相关外设和其他技术材料。

### 勘误表

《[MSP432E4 SimpleLink™ 微控制器器件勘误表](#)》介绍与已发布的规格不同的器件行为

### 应用报告

《[SimpleLink™ MSP432E4 微控制器的系统设计指南](#)》SimpleLink MSP432E4 微控制器是高度集成的片上系统 (SOC) 器件，具有扩展接口和处理功能。因此，在创建原理图和设计电路板时要考虑很多因素。通过采用本设计指南中的建议，您会更有信心，设计的电路板在首次加电时就可以有效工作。

《[在 SimpleLink MSP432E4 微控制器上使用 I²C 主机的功能集](#)》内部集成电路 (I²C) 是一个多主从单端总线，通常用于将速度较低的外设 IC 连接到处理器和微控制器。从器件涵盖从非易失性存储器到数据采集器件在内的各类型器件，如模数转换器 (ADC)、传感器等。本应用报告展示了如何在 SimpleLink MSP432E4 微控制器上使用功能丰富的 I²C 主机与系统中的多个从器件通信。

《[通过 JTAG 接口使用 SimpleLink MSP432E4 微控制器](#)》IEEE 标准 1149.1 - 1990、IEEE 标准测试访问端口和边界扫描架构 (JTAG) 是一种用于验证设计和测试组装后的印刷电路板的方法。它是将数据传输到嵌入式系统的非易失性存储器和调试嵌入式软件的主要手段。本应用报告介绍了 JTAG 的物理连接和设计自定义电路板时需要考虑的注意事项。它还说明了如何使用 SimpleLink MSP432E4 LaunchPad 开发套件上的 JTAG 接口，以通过外部调试器调试板载微控制器，或使用板载调试器调试非板载微控制器。

### 用户指南

《[MSP432E4 SimpleLink™ 微控制器技术参考手册](#)》介绍 MSP432E4 系列微控制器，包括围绕 Arm Cortex-M4F 内核设计的片上系统 (SoC) 器件的功能块。

《[MSP432E4 SimpleLink™ 微控制器引导加载程序用户指南](#)》引导加载程序是一小段代码，可以编程到闪存开始位置，以便用作应用加载程序。也可以用作在 SimpleLink MSP432E4 基于 Arm Cortex-M4 的微控制器上运行的应用的更新机制。引导加载程序可以搭建为使用 UART、SSI、I²C、CAN、以太网或 USB 端口来更新微控制器上的代码。通过源代码修改，或者简单地在编译时决定要包括的例程，可以定制引导加载程序。由于提供了完整源代码，因此引导加载程序可完全自定义。

## 8.5 Community Resources

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

**TI E2E™ 在线社区** 为了促进工程师之间的合作，我们创建了 TI 工程师对工程师 (E2E) 社区。在 [e2e.ti.com](http://e2e.ti.com) 中，您可以提问、分享知识、拓展思路并与同行工程师一道帮助解决问题。

**TI Embedded Processors Wiki** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

## 8.6 商标

SimpleLink, LaunchPad, MSP432, E2E are trademarks of Texas Instruments.  
ARM, Cortex, Thumb, Thumb-2, PrimeCell, Arm7 are registered trademarks of Arm Limited.  
Bluetooth is a registered trademark of Bluetooth SIG.  
Wi-Fi is a registered trademark of Wi-Fi Alliance.  
All other trademarks are the property of their respective owners.

## 8.7 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 8.8 出口管制提示

接收方同意：如果美国或其他适用法律限制或禁止将通过非披露义务的披露方获得的任何产品或技术数据（其中包括软件）（见美国、欧盟和其他出口管理条例之定义）、或者其他适用国家条例限制的任何受管制产品或此项技术的任何直接产品出口或再出口至任何目的地，那么在没有事先获得美国商务部和其他相关政府机构授权的情况下，接收方不得在知情的情况下，以直接或间接的方式将其出口。

## 8.9 术语表

**TI 术语表** 这份术语表列出并解释术语、缩写和定义。

## 9 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP432E401YTPDT  | ACTIVE        | TQFP         | PDT                | 128  | 90             | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 105   | MSP432<br>E401YT        | <a href="#">Samples</a> |
| MSP432E401YTPDTR | ACTIVE        | TQFP         | PDT                | 128  | 1000           | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 105   | MSP432<br>E401YT        | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

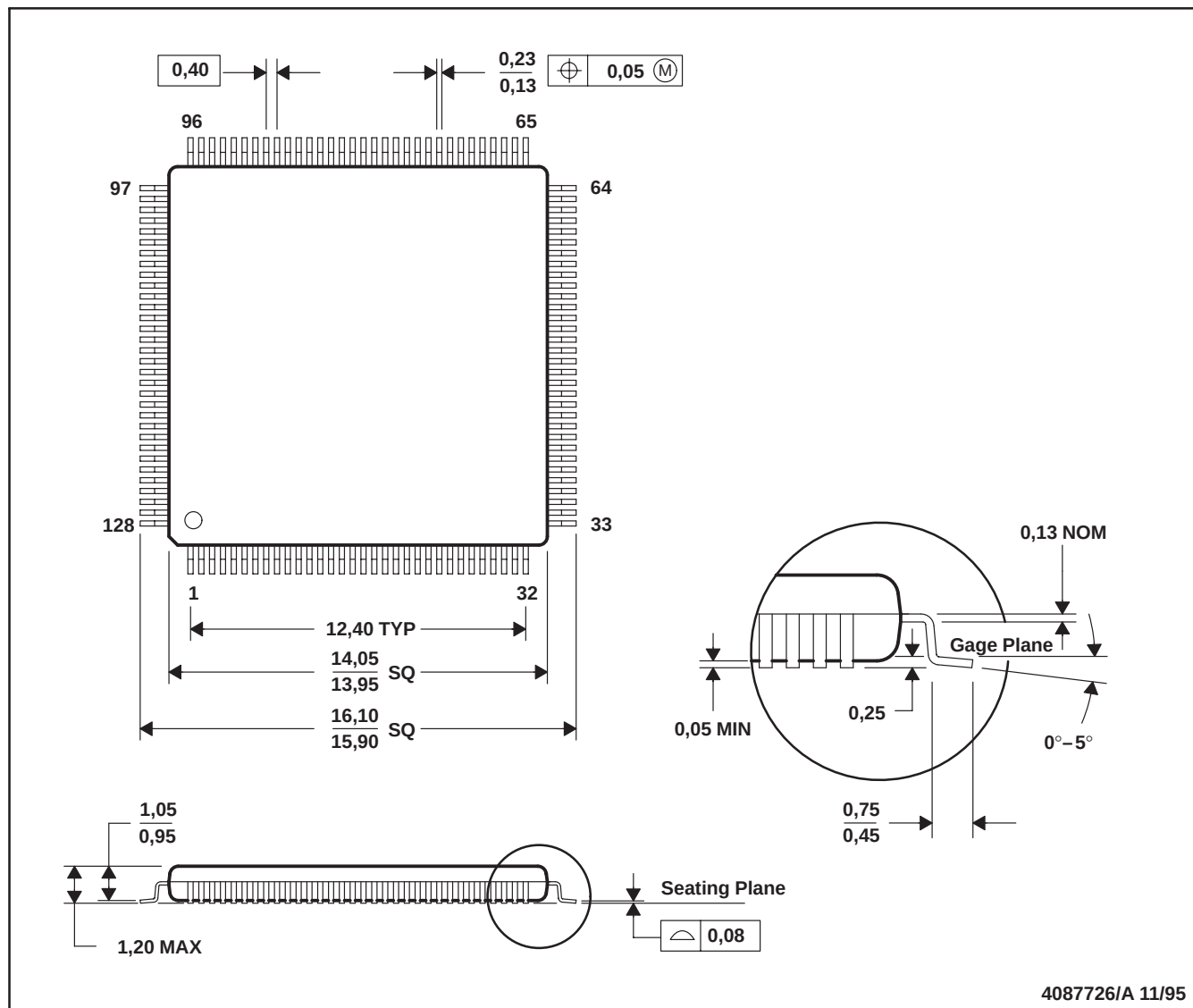
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PDT (S-PQFP-G128)

PLASTIC QUAD FLATPACK



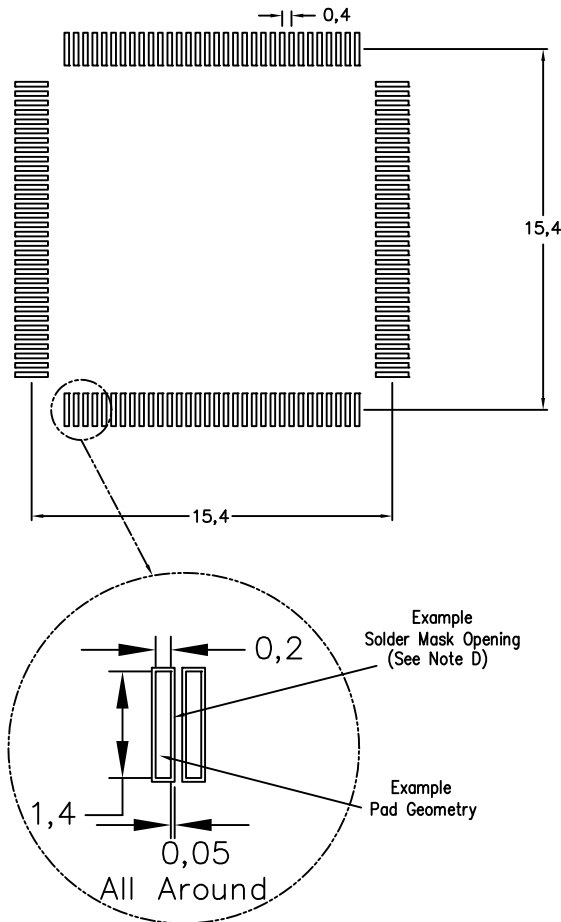
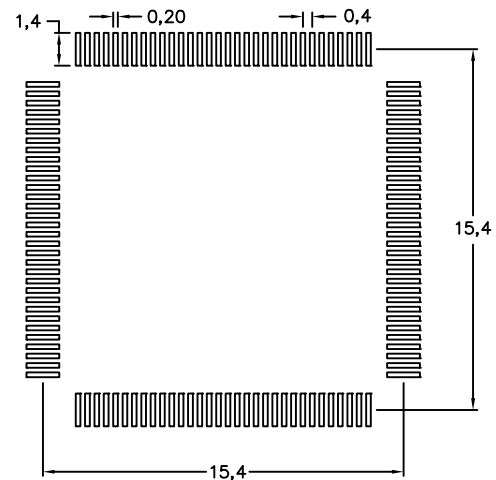
- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.

## PDT (S-PQFP-G128)

## PLASTIC QUAD FLAT PACK

Example Board Layout  
Via pattern and copper area under solder mask  
may vary depending on layout constraints

Stencil Openings based on a stencil  
thickness of .127mm (.005inch).



4215357/A 07/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## 重要声明和免责声明

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