TLC59211 8-Bit DMOS Sink Driver

1 Features

- DMOS Process
- High Voltage Output (V_{ds} = 30 V)
- Output Current on Each Channel (I_{ds} Max = 200 mA)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- ESD Protection Exceeds JESD 22
  - 2000-V Human Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged Device Model (C101)
- LED Driver Application
- Output Clamp Diode (Parasitic)

2 Applications

- Lamps and Display (LED)
- Hammers
- Relay

3 Description

The TLC59211 is an 8-bit LED and solenoid driver designed for 5-V V_{CC} operation.

The TLC59211 is characterized for operation from –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC59211	PDIP (20)	24.33 mm × 6.35 mm
	TSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Diagram

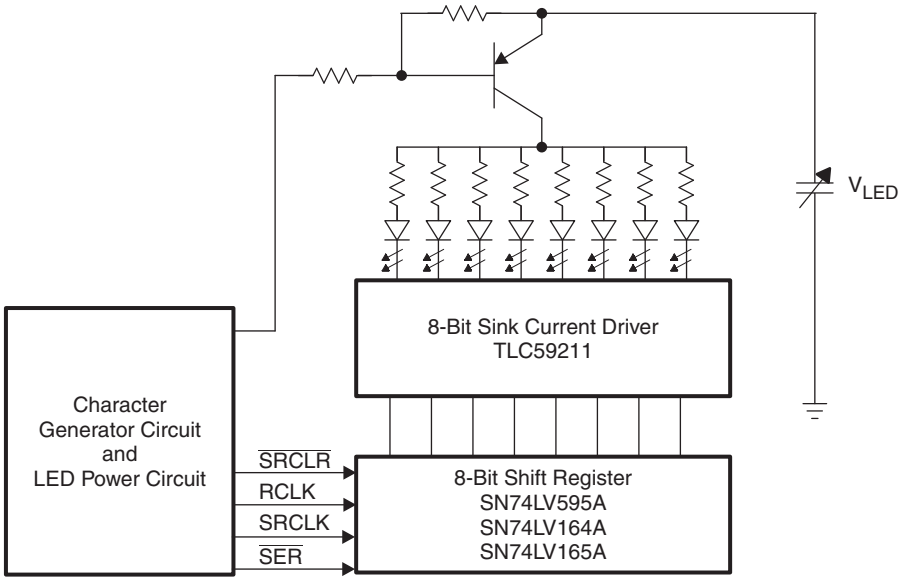


Table of Contents

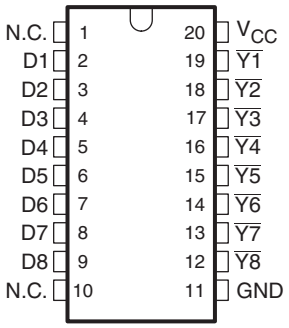
4 Revision History

Changes from Original (April 2009) to Revision A **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Removed *Ordering Information* table ... 1

5 Pin Configuration and Functions

N or PW Package
20-Pin PDIP or TSSOP
(Top View)



N.C. – Not internally connected

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
N.C.	1	—	No Connection
	10		
D1	2	I	Input control to the current sink driver
D2	3		
D3	4		
D4	5		
D5	6		
D6	7		
D7	8		
D8	9		
$\overline{Y1}$	19	O	Output to load
$\overline{Y2}$	18		
$\overline{Y3}$	17		
$\overline{Y4}$	16		
$\overline{Y5}$	15		
$\overline{Y6}$	14		
$\overline{Y7}$	13		
$\overline{Y8}$	12		
GND	11	—	Ground
VCC	20	I	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
D	Input voltage		–0.5	7	V
V_{ds}	Output voltage	H output	–0.5	32	V
I_{ds}	Output current	1 bit for output low		200	mA
I_{IK}	Input clamp current	V_I < 0 V		–20	mA
	Operating free-air temperature		–40	85	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

V_{CC} = 3 V to 5.5 V

				MIN	MAX	UNIT
V_{CC}	Supply voltage			3	5.5	V
V_{IH}	High-level input voltage			V_{CC} × 0.7	V_{CC}	V
V_{IL}	Low-level input voltage			0	V_{CC} × 0.3	V
V_{ds}	Output voltage				30	V
I_{ds}	Output current	N package	Duty cycle < 42%		200	mA
			Duty cycle < 100%		130	
		PW package	Duty cycle < 24%		200	
			Duty cycle < 100%		95	
T_A	Operating free-air temperature			–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLC59211		UNIT
		N (PDIP)	PW (TSSOP)	
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	54.4	94.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.6	28.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.4	45.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.0	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	35.3	45.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics V_{CC} = 3 V to 3.6 V

over recommended operating free-air temperature range, V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{t+}	Positive-going input threshold	D				2.52	V
V_{t-}	Negative-going input threshold	D		0.9			V
V_t	Hysteresis	D		0.33		1.32	V
I_{IH}	High-level input current	V_{CC} = 3.6 V, V_I = 3.6V			0	1	µA
I_{IL}	Low-level input current	V_{CC} = 3.6 V, V_I = 0 V			0	–1	µA
I_{OZ}	Leakage current	V_{ds}= 30 V				5	µA
I_{off}	Leakage current	V_I = 0 to 3.6 V, V_O = 0 to 30 V, V_{CC} = 0			0	5	µA
I_{CC}	Supply current	V_I = 0 to 3.6 V, V_{CC} = 3.6 V	Output = all OFF		0	5	µA
			Output = all ON		0	5	
V_{OL}	Low-level output voltage	V_{CC} = 3 V, I_{OL} = 100 mA			0.35	0.7	V
							V
r_{ON}	ON-state resistance	V_{CC} = 3 V, I_O = 100 mA			3.5	7	Ω
C_i	Input capacitance	V_I = V_{CC} or GND			5		pF

6.6 Electrical Characteristics V_{CC} = 4.5 V to 5.5 V

over recommended operating free-air temperature range, V_{CC} = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{t+}	Positive-going input threshold	D, $\overline{CLR}$, CLK				3.5	V
V_{t-}	Negative-going input threshold	D, $\overline{CLR}$, CLK		1.5			V
V_t	Hysteresis	D, $\overline{CLR}$, CLK		0.5		2	V
I_{IH}	High-level input current	V_{CC} = 5.5 V, V_I = 5.5 V			0	1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V, V_I = 0 V			0	–1	µA
I_{OZ}	Leakage current	V_{ds}= 30 V				5	µA
I_{off}	Leakage current	V_I = 0 to 5 V, V_O = 0 to 30 V, V_{CC} = 0			0	5	µA
I_{CC}	Supply current	V_I = 0 to 5 V, V_O = 0 to 30 V, V_{CC} = 0	Output = all OFF		0	5	µA
			Output = all ON		0	5	
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V, I_O = 100 mA			0.2	0.35	V
		V_{CC} = 4.5 V, I_O = 200 mA			0.5	0.7	V
r_{ON}	ON-state resistance	V_{CC} = 4.5 V, I_O = 100 mA			2	3.5	Ω
C_i	Input capacitance	V_I = V_{CC} or GND			5		pF

6.7 Switching Characteristics V_{CC} = 3 V to 3.6 V

over operating free-air temperature range, V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	LOAD CAPACITANCE	T_A = 25°C			T_A = –40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{TLH}	Output = low to high	C_L = 30 pF, R_L = 240 Ω, 24-V pullup		200	450		450	ns
t_{THL}	Output = high to low	C_L = 30 pF, R_L = 240 Ω, 24-V pullup		300	450		480	ns
t_{PLH}	Output = low to high	C_L = 30 pF, R_L = 240 Ω, 24-V pullup		450	650		800	ns
t_{PHL}	Output = high to low	C_L = 30 pF, R_L = 240 Ω, 24-V pullup		450	650		800	ns

6.8 Switching Characteristics V_{CC} = 4.5 V to 5.5 V

over operating free-air temperature range, V_{CC} = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	LOAD CAPACITANCE	T_A = 25°C			T_A = –40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{TLH}	Output = low to high	C_L = 30 pF, R_L = 240 Ω, 24-V pullup		180	220		260	ns
t_{THL}	Output = high to low	C_L = 30 pF, R_L = 240 Ω, 24-V pullup		290	430		460	ns
t_{PLH}	Output = low to high	C_L = 30 pF, R_L = 240 Ω, 24-V pullup		320	470		510	ns
t_{PHL}	Output = high to low	C_L = 30 pF, R_L = 240 Ω, 24-V pullup		320	470		510	ns

6.9 Typical Characteristics

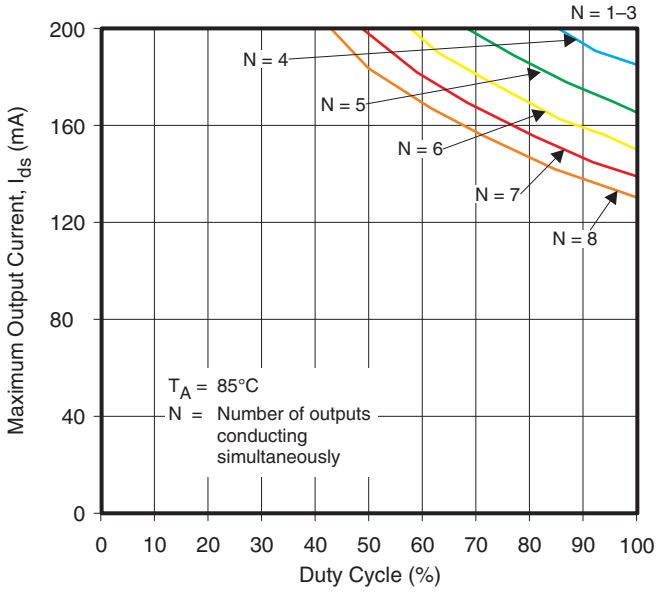
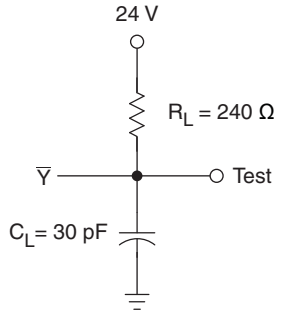
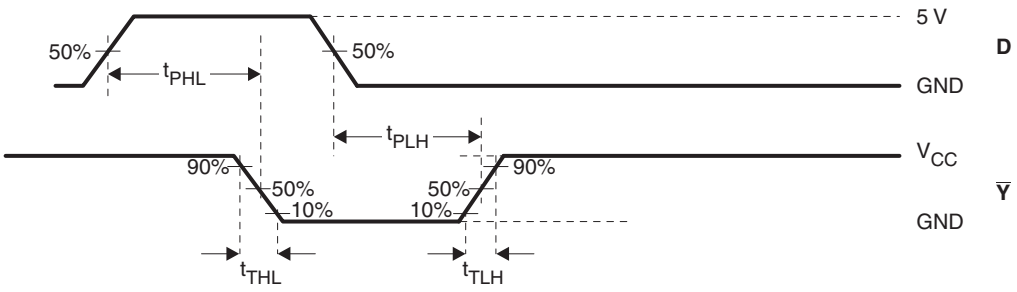


Figure 1. Maximum Output Currents vs Duty Cycle in PDIP (N) Package

7 Parameter Measurement Information



LOAD CIRCUIT FOR O/D OUTPUT



VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, and t_f ≤ 3 ns.

C. The outputs are measured one at a time with one transition per measurement.

D. t_{PLH} and t_{PHL} are the same as t_{pd}.

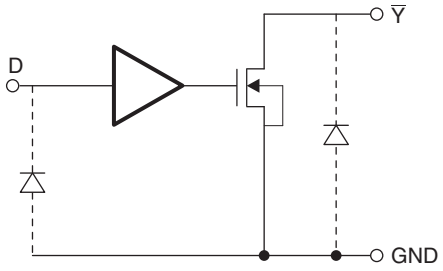
Figure 2. Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

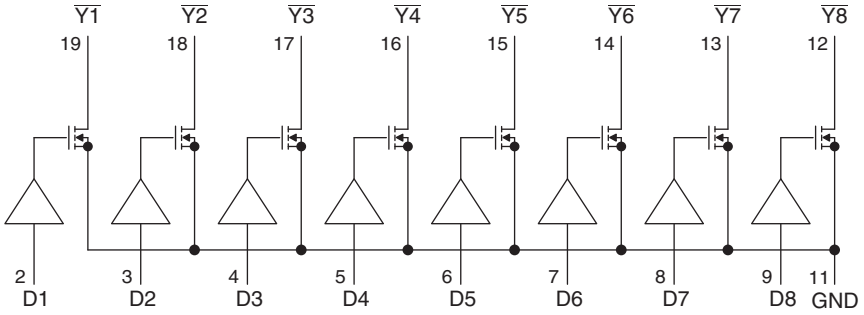
The TLC59211 is an 8-bit parallel LED and solenoid driver designed for 5-V V_{CC} operation. Each channel is individually controlled by its input.

8.2 Functional Block Diagram



8.3 Feature Description

Each of the 8 channels is controlled by its input Dn. When Dn is logic high, the current sink is enabled, output is low. When Dn is logic low, the current sink is disabled, output is pulled high.



(1) This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

Figure 3. Logic Symbol

8.4 Device Functional Modes

Table 1 lists the functional modes of the TLC59211.

Table 1. Function Table (Each Latch)(1)

INPUTS	OUTPUT
D	$\overline{Y}$
L	H*
H	L

(1) L: Low-level
H: High-level
H*: with pullup resistor

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

In LED display application, TLC59211 is used to drive the current sink for 8 LEDs in parallel. LED display pattern can be created by providing different bit pattern. LED can be duty cycled by either duty cycling the LED supply or the control bit.

9.2 Typical Application

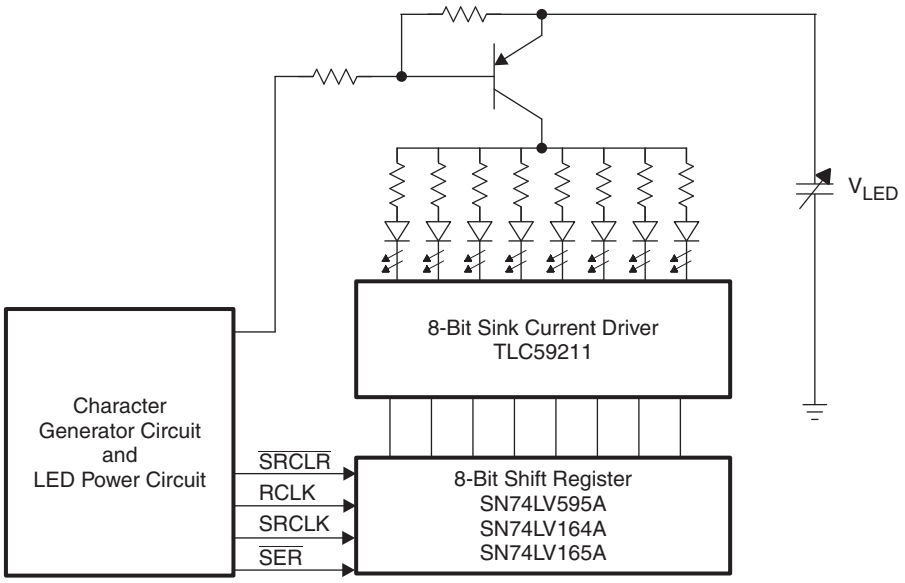


Figure 4. LED Display Implementation With TLC59211

9.2.1 Design Requirements

For LED display application, an 8-bit shift register is used to provide the input control for TLS59211. A character generator circuit and LED power circuit is used to generate the bit pattern written into the shift register and provide the power control for the entire LED array. The LED power circuit controls the total current into the array and can also power cycle the LED array. For simple implementation, LED power circuit could be eliminated. The VLED can be connected directly to the resistor and LED string.

9.2.2 Detailed Design Procedure

The combination of LED and resistor sets the current of the LED.

$$V_R + V_L = V_{LED},\ I = (V_{LED} - V_L)/R \quad (1)$$

The maximum current through each channel of TLC59211 is determined by the number of the LEDs that are on and the duty cycle according to Figure 5 for TSSOP package.

Typical Application (continued)

9.2.3 Application Curve

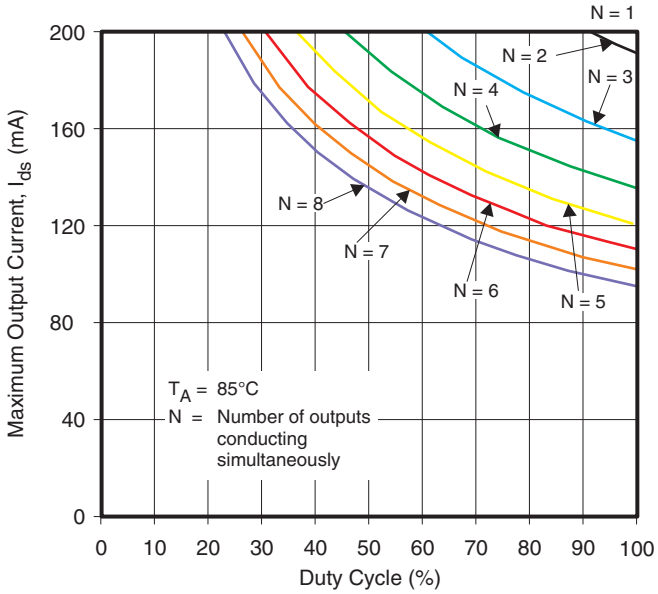


Figure 5. Maximum Output Currents vs Duty Cycle in TSSOP (PW) Package

10 Power Supply Recommendations

The supply voltage to TLC59211 is from 3.3 V to 5.5 V. The voltage at output can be up to 30 V.

11 Layout

11.1 Layout Guidelines

The traces that carry current from the LED cathodes to the OUTx pins must be wide enough to support the current (up to 200 mA).

11.2 Layout Example

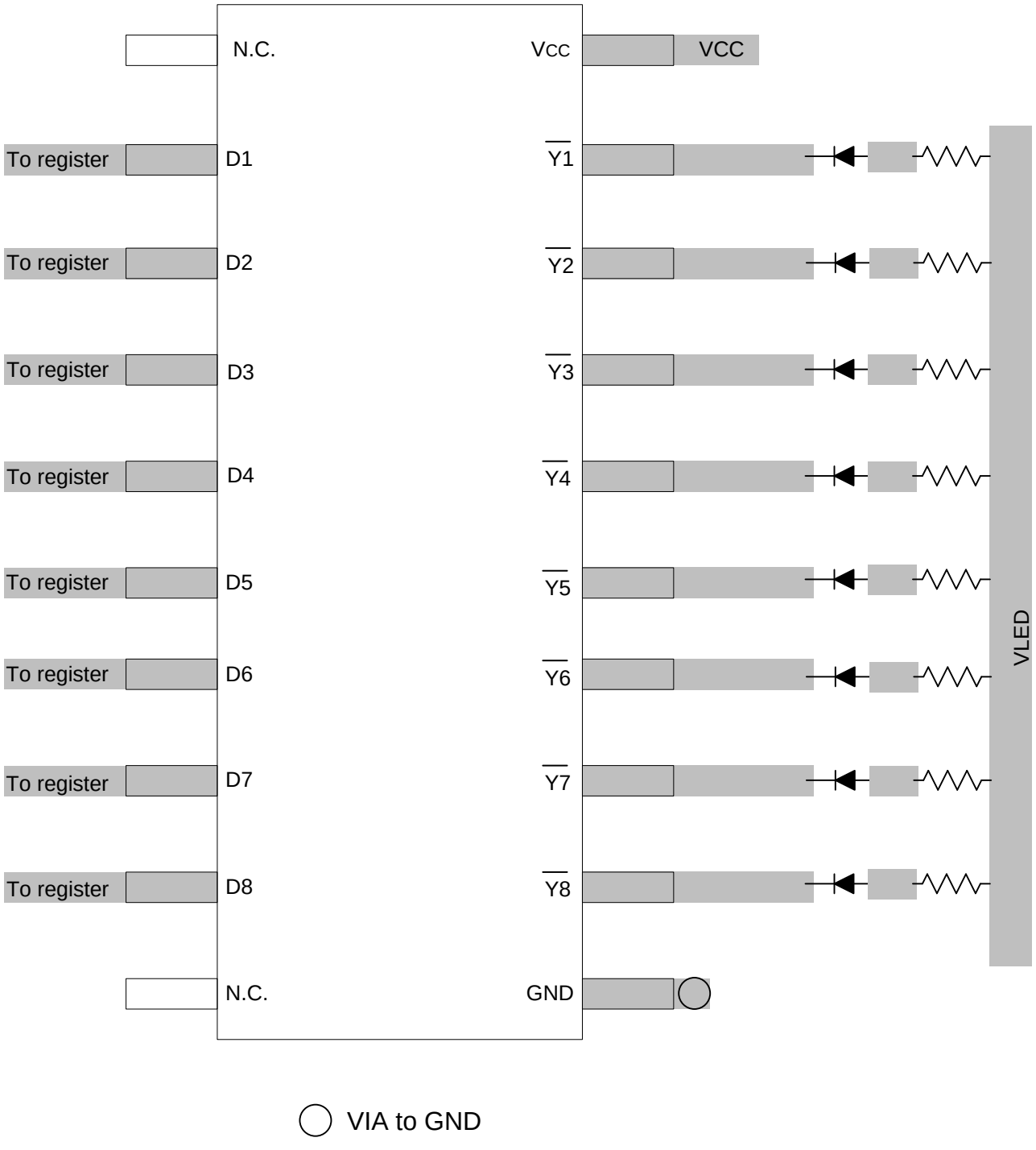


Figure 6. Layout Example Recommendation

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC59211IN	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLC59211IN	Samples
TLC59211IPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y59211	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

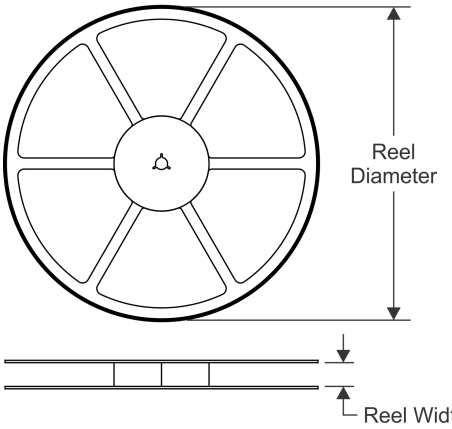
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

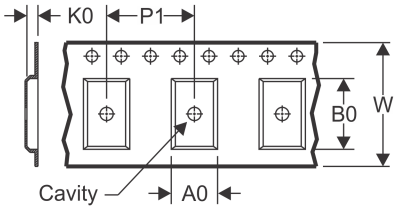
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

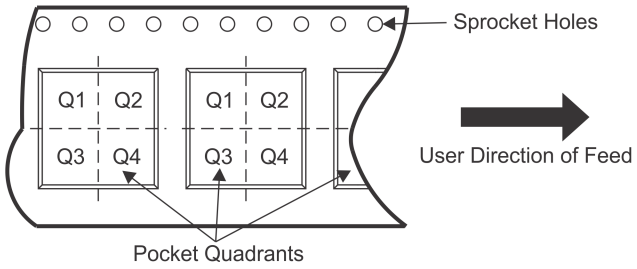


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

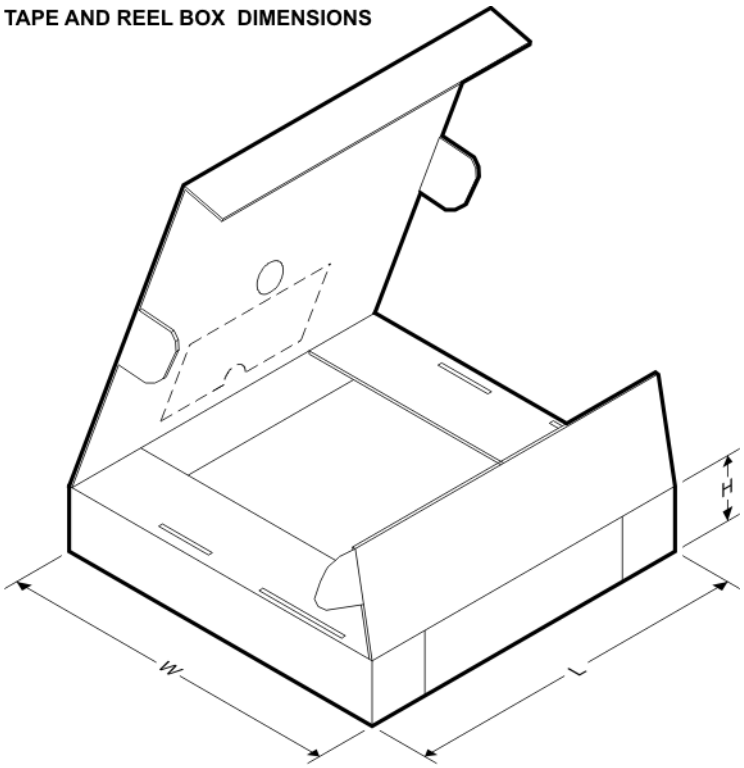
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC59211IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

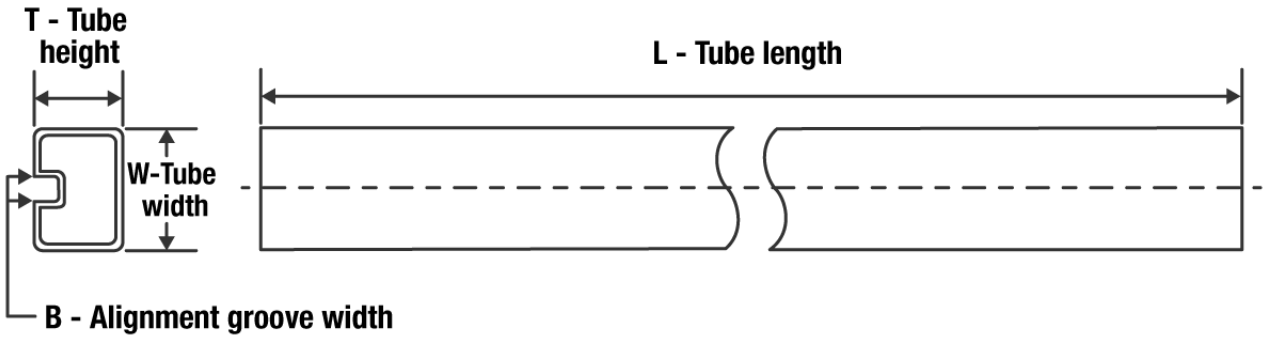
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC59211IPWR	TSSOP	PW	20	2000	853.0	449.0	35.0

TUBE



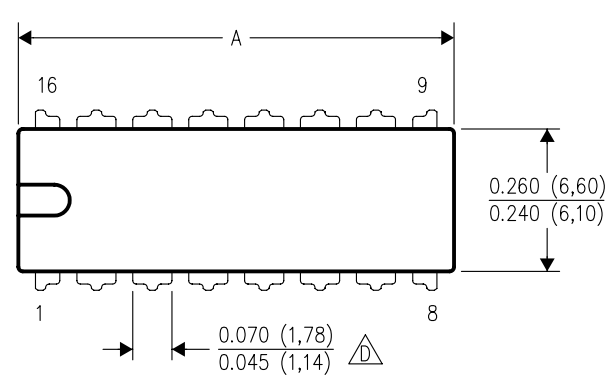
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC59211IN	N	PDIP	20	20	506	13.97	11230	4.32

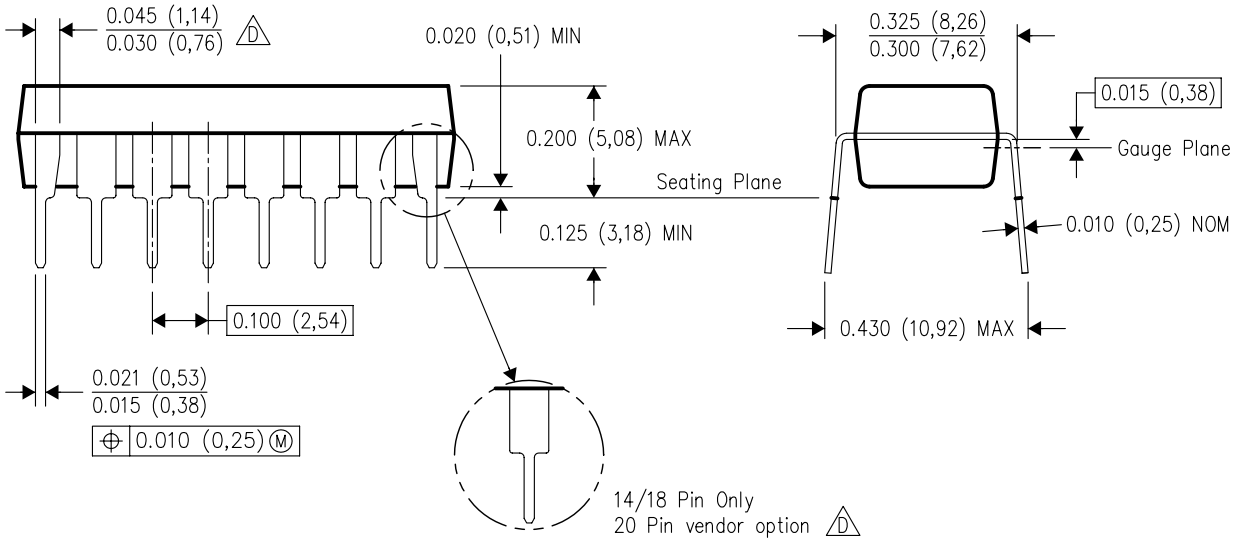
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

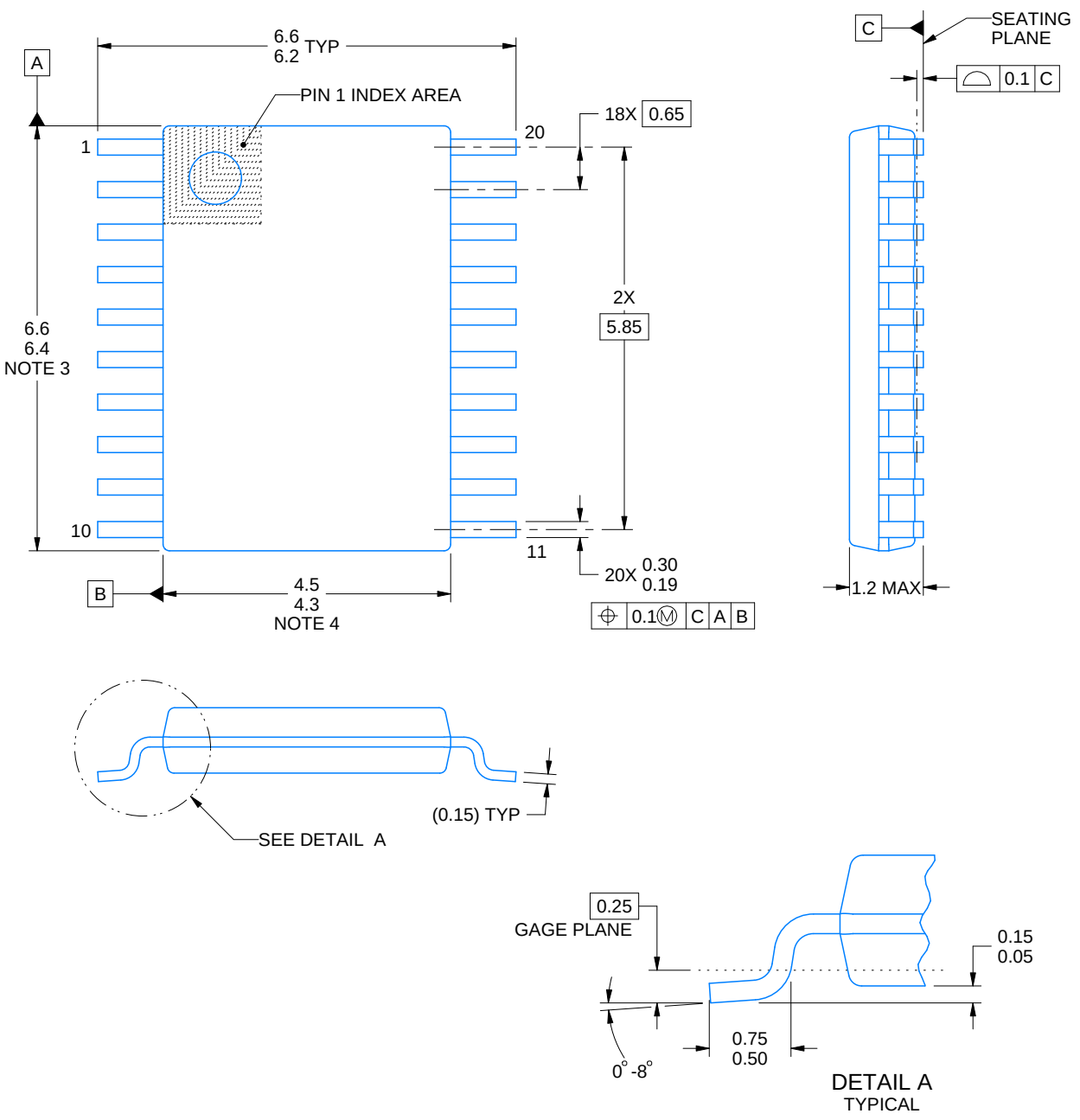
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0020A

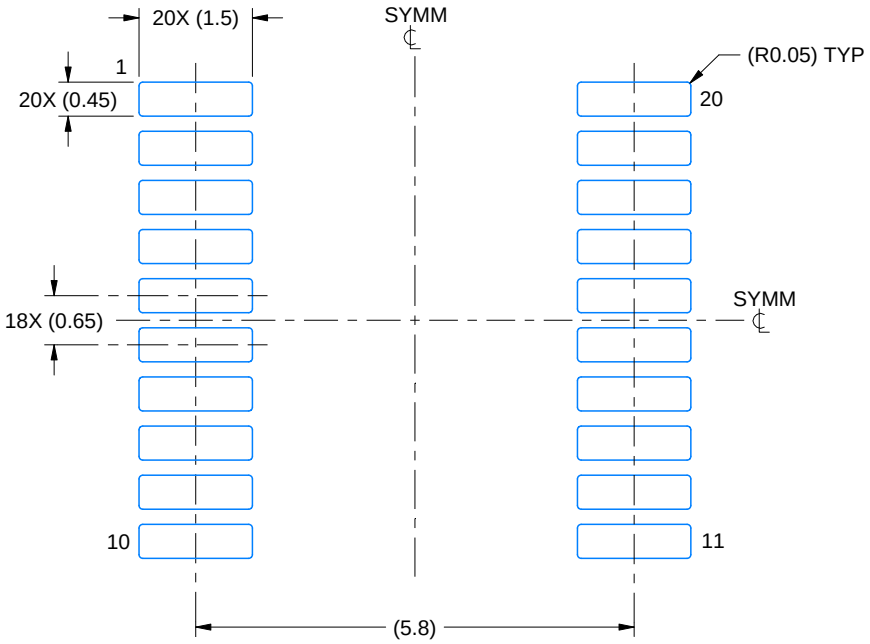
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



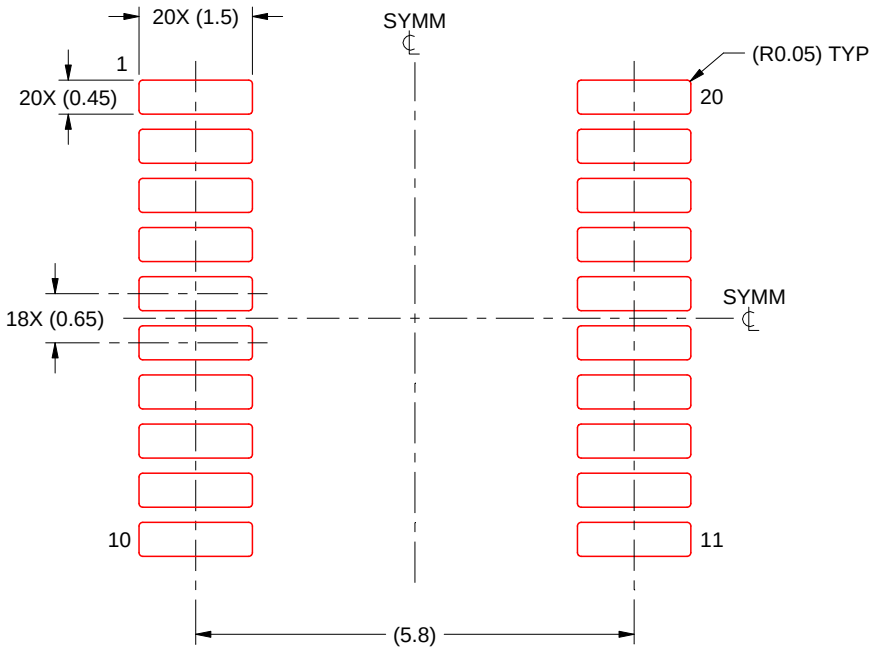
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



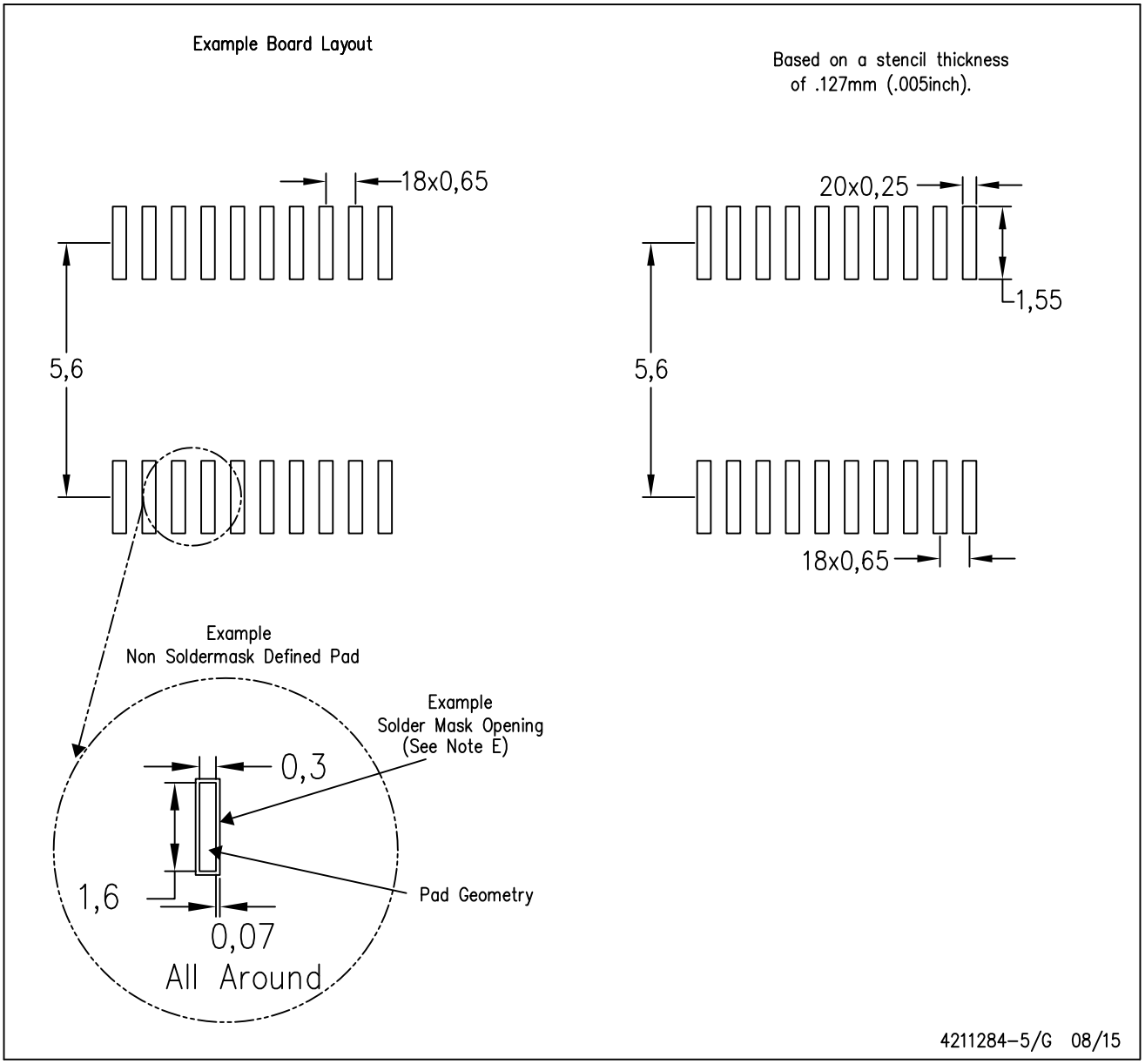
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265