

## SN75LVCP601 Two-Channel 6-Gbps SATA Redriver

### 1 Features

- 1.5-, 3-, or 6-Gbps Two-Channel Redriver
- Integrated Output Squelch
- Programmable RX and TX Equalization and De-Emphasis Width Control
- Power-Save Feature Lowers Power by >80% in Auto Low-Power Mode
- Low Power
  - <220 mW (Typ)
  - <50 mW (in Auto Low-Power Mode)
  - <5 mW (in Standby Mode)
- Excellent Jitter and Loss Compensation Capability to Over 24-Inch (61-cm) FR4 Trace
- 20-Pin 4-mm × 4-mm QFN Package
- High Protection Against ESD Transient
  - HBM: 10,000 V
  - CDM: 1,500 V
  - MM: 200 V
- Pin-Compatible With LVCP412A and MAX4951

### 2 Applications

- Notebooks
- Desktops
- Docking Stations
- Servers
- Workstations

### 3 Description

The SN75LVCP601 device is a dual-channel, single-lane SATA redriver and signal conditioner supporting data rates up to 6 Gbps. The device complies with SATA physical link 2m and 3i specifications. The SN75LVCP601 operates from one 3.3-V supply and has 100-Ω line termination with a self-biasing feature, making the device suitable for ac coupling. The inputs incorporate an out-of-band (OOB) detector, which automatically squelches the output while maintaining a stable common-mode voltage compliant to the SATA link. The device design also handles spread-spectrum clocking (SSC) transmission per the SATA specification.

The SN75LVCP601 device handles interconnect losses at both its input and output. The input stage of each channel offers selectable equalization settings that are programmable to match the loss in the channel. The differential outputs provide selectable de-emphasis to compensate for the expected distortion that the SATA signal experiences. The level of equalization and de-emphasis settings depends on the length of interconnect and its characteristics. The setting of signal control pins EQ1, EQ2, DE1, and DE2 controls both equalization and de-emphasis levels.

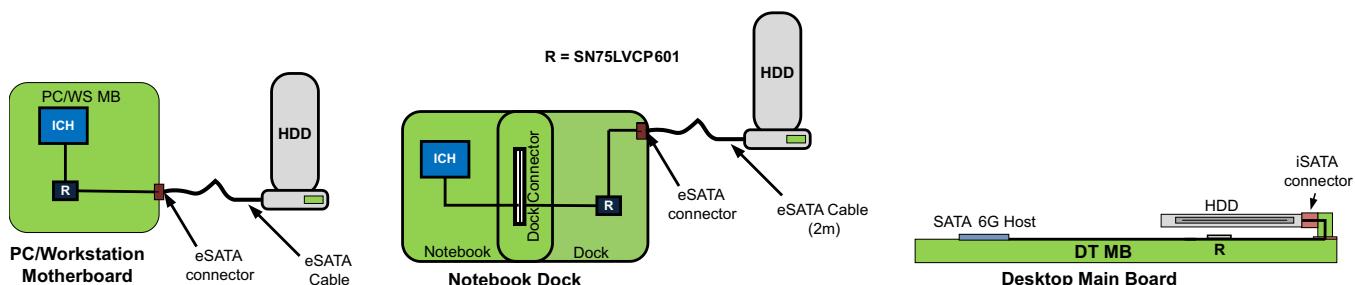
This device is hot-plug capable (requires the use of ac-coupling capacitors at differential inputs and outputs), thus preventing device damage under device hot-insertion, in such cases as: async signal plug or removal, unpowered plug or removal, powered plug or removal, surprise plug or removal

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN75LVCP601	WQFN (20)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

## Table of Contents

<b>1 Features</b> .....	<b>1</b>	<b>8 Detailed Description</b> .....	<b>17</b>
<b>2 Applications</b> .....	<b>1</b>	8.1 Overview .....	17
<b>3 Description</b> .....	<b>1</b>	8.2 Functional Block Diagram .....	17
<b>4 Revision History</b> .....	<b>2</b>	8.3 Feature Description .....	18
<b>5 Pin Configuration and Functions</b> .....	<b>4</b>	8.4 Device Functional Modes .....	18
<b>6 Specifications</b> .....	<b>5</b>	<b>9 Application and Implementation</b> .....	<b>19</b>
6.1 Absolute Maximum Ratings .....	5	9.1 Application Information .....	19
6.2 ESD Ratings .....	5	9.2 Typical Application .....	19
6.3 Recommended Operating Conditions .....	5	<b>10 Power Supply Recommendations</b> .....	<b>25</b>
6.4 Thermal Information .....	5	<b>11 Layout</b> .....	<b>25</b>
6.5 Electrical Characteristics .....	6	11.1 Layout Guidelines .....	25
6.6 Power Dissipation Characteristics .....	7	11.2 Layout Example .....	26
6.7 Timing Requirements .....	8	<b>12 Device and Documentation Support</b> .....	<b>27</b>
6.8 Switching Characteristics .....	8	12.1 Community Resources .....	27
6.9 Typical Characteristics .....	10	12.2 Trademarks .....	27
<b>7 Parameter Measurement Information</b> .....	<b>11</b>	12.3 Electrostatic Discharge Caution .....	27
7.1 Jitter and VOD Results: Case 1 at 6 Gbps .....	12	12.4 Glossary .....	27
7.2 Jitter and VOD Results: Case 2 at 3 Gbps .....	13	<b>13 Mechanical, Packaging, and Orderable</b> <b>Information</b> .....	<b>27</b>
7.3 Jitter and VOD Results: Case 3 at 1.5 Gbps .....	15		

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (January 2016) to Revision H	Page
• Changed pin DE1 number From: 8 To: 9 in the <i>Pin Functions</i> table .....	4
• Changed pin DE2 number From: 9 To: 8 in the <i>Pin Functions</i> table .....	4

Changes from Revision F (June 2015) to Revision G	Page
• Changed Pin 8 name To: DE2 and Pin 9 name To: DE1 in <a href="#">Figure 27</a> .....	20

Changes from Revision E (January 2014) to Revision F	Page
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
• Added Storage temperature to the <i>Absolute Maximum Ratings</i> table .....	5
• Moved timing parameters out of <i>Electrical Characteristics</i> and into <i>Timing Requirements</i> .....	8
• Moved switching parameters out of <i>Electrical Characteristics</i> and into <i>Switching Characteristics</i> .....	8

Changes from Revision D (January 2013) to Revision E	Page
• Changed $DJ_{TX}$ ( $UI = 333$ ps) From: Max = 0.19 To: Max = 0.07 .....	8
• Changed $DJ_{TX}$ ( $UI = 167$ ps) From: Max = 0.34 To: Max = 0.16 .....	8

Changes from Revision C (October 2012) to Revision D	Page
• Corrected formatting of the Differential output-voltage swing dc level section of the Electrical Characteristics table .....	7

<b>Changes from Revision B (February 2012) to Revision C</b>	<b>Page</b>
• Deleted Diff <sub>V<sub>pp</sub>TX</sub> row.....	7
• Inserted Diff <sub>V<sub>pp</sub>TX_DE</sub> row .....	7
• Changed <a href="#">Figure 5</a> caption .....	10
• Revised text of the Output Ed-Emphasis section .....	18
• Deleted setting recommendations on pulse durations for DEW1 and DEW2 .....	18

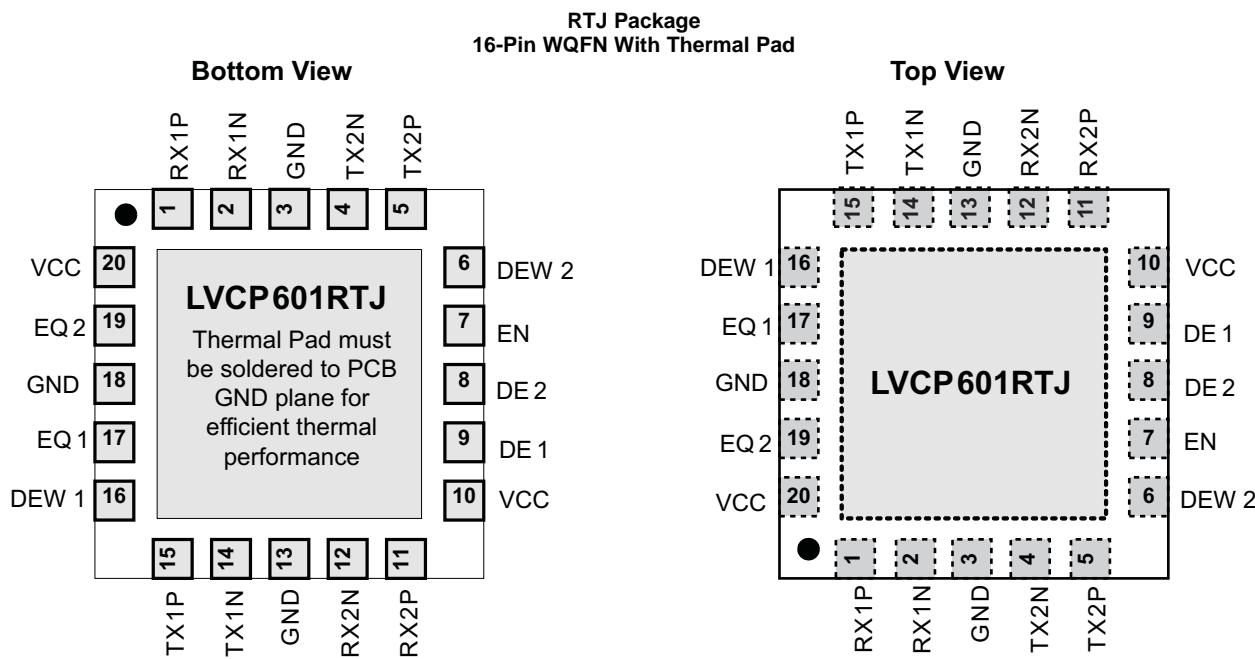
  

<b>Changes from Revision A (October 2011) to Revision B</b>	<b>Page</b>
• Changed pin type from CML to VML for pins 4, 5, 14, 15 in the <i>Pin Functions</i> table .....	4

<b>Changes from Original (June 2010) to Revision A</b>	<b>Page</b>
• Changed pin EN number From: 4 To: 7 in the <i>Pin Functions</i> table .....	4

## 5 Pin Configuration and Functions



### Pin Functions

PIN		PIN TYPE	DESCRIPTION
NAME	NO.		
<b>CONTROL PINS</b>			
DE1 <sup>(1)</sup>	9	I, LVCMOS	Selects de-emphasis settings for CH 1 and CH 2 per <a href="#">Table 1</a> . Internally tied to V <sub>CC</sub> / 2.
DE2 <sup>(1)</sup>	8	I, LVCMOS	De-emphasis width control for CH 1 and CH 2. 0 = De-emphasis pulse duration, short 1 = De-emphasis pulse duration, long (default)
DEW1	16	I, LVCMOS	Device enable and disable pin, internally pulled to V <sub>CC</sub> . 0 = Device in standby mode 1 = Device enabled (default)
DEW2	6	I, LVCMOS	
EN	7	I, LVCMOS	
EQ1 <sup>(1)</sup>	17	I, LVCMOS	Selects equalization settings for CH 1 and CH 2 per <a href="#">Table 1</a> . Internally tied to V <sub>CC</sub> / 2.
EQ2 <sup>(1)</sup>	19	I, LVCMOS	
<b>HIGH-SPEED DIFFERENTIAL I/O</b>			
RX1N	2	I, CML	Noninverting and inverting CML differential input for CH 1 and CH 2. These pins connect to an internal voltage bias via a dual-termination resistor circuit.
RX1P	1	I, CML	
RX2N	12	I, CML	
RX2P	11	I, CML	
TX1N	14	O, VML	Noninverting and inverting VML differential output for CH 1 and CH 2. These pins connect internally to voltage bias via termination resistors.
TX1P	15	O, VML	
TX2N	4	O, VML	
TX2P	5	O, VML	
<b>POWER</b>			
GND	3, 13, 18	Power	Supply ground
VCC	10, 20	Power	Positive supply must be 3.3 V ± 10%

(1) Internally biased to V<sub>CC</sub> / 2 with >200-k $\Omega$  pullup or pulldown. When 3-state pins are left as NC, board leakage at the pin pad must be <1  $\mu$ A; otherwise, drive to V<sub>CC</sub> / 2 to assert mid-level state.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range <sup>(2)</sup>	-0.5	4	V
Voltage range	Differential I/O	-0.5	4	V
	Control I/O	-0.5	V <sub>CC</sub> + 0.5	V
Continuous power dissipation		See <a href="#">Power Dissipation Characteristics</a>		
T <sub>stg</sub>	Storage temperature	150		°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential voltages, are with respect to the network ground terminal.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±10000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500
		Machine model <sup>(3)</sup>	±200

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

(3) Tested in accordance with JEDEC Standard 22, Test Method A115-A.

### 6.3 Recommended Operating Conditions

typical values for all parameters are V<sub>CC</sub> = 3.3 V and T<sub>A</sub> = 25°C; all temperature limits are specified by design

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	3	3.3	3.6	V
C <sub>COUPLING</sub>	Coupling capacitor	12		nF	
	Operating free-air temperature	0	85		°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN75LVCP601	UNIT
		RTJ (WQFN)	
		20 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	38	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	40	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	10	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.5	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	0.9	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	15.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DEVICE PARAMETERS</b>					
P <sub>D</sub>	Power dissipation in active mode DEW <sub>x</sub> = EN = V <sub>CC</sub> , EQ <sub>x</sub> = DEx = NC, K28.5 pattern at 6 Gbps, V <sub>ID</sub> = 700 mV <sub>p-p</sub>	215	288		mW
P <sub>SD</sub>	Power dissipation in standby mode EN = 0 V, DEW <sub>x</sub> = EQ <sub>x</sub> = DEx = NC, K28.5 pattern at 6 Gbps, V <sub>ID</sub> = 700 mV <sub>p-p</sub>		5		mW
I <sub>CC</sub>	Active-mode supply current EN = 3.3 V, DEW <sub>x</sub> = 0 V, EQ <sub>x</sub> = DEx = NC, K28.5 pattern at 6 Gbps, V <sub>ID</sub> = 700 mV <sub>p-p</sub>	65	80		mA
I <sub>CC_ALP</sub>	Active power-save mode I <sub>CC</sub> When device is enabled and auto low-power conditions are met		6.5	10	mA
I <sub>CC_STDBY</sub>	Standby mode supply current EN = 0 V		1		mA
	Maximum data rate	1	6		Gbps
<b>OUT-OF-BAND (OOB)</b>					
V <sub>OOB</sub>	Input OOB threshold f = 750 MHz	50	78	150	mV <sub>pp</sub>
D <sub>VdifoOB</sub>	OOB differential delta		25		mV
D <sub>VCMOOB</sub>	OOB common-mode delta		50		mV
<b>CONTROL LOGIC</b>					
V <sub>IH</sub>	Input high voltage For all control pins	1.4			V
V <sub>IL</sub>	Input low voltage		0.5		V
V <sub>INHYS</sub>	Input hysteresis	115			mV
I <sub>IH</sub>	High-level input current EQ <sub>x</sub> , DEx = V <sub>CC</sub>		30		μA
		EN, DEW <sub>x</sub> = V <sub>CC</sub>	1		
I <sub>IL</sub>	Low-level input current EQ <sub>x</sub> , DEx = GND	−30			μA
		EN, DEW <sub>x</sub> = GND	−10		
<b>RECEIVER AC/DC</b>					
Z <sub>DIFFRX</sub>	Differential-input impedance	85	100	115	Ω
Z <sub>SERX</sub>	Single-ended input impedance	40			Ω
V <sub>CMRX</sub>	Common-mode voltage		1.8		V
RL <sub>DiffRX</sub>	Differential-mode return loss (RL) f = 150 MHz to 300 MHz	18	28		dB
		14	17		
		10	12		
		8	9		
		3	9		
RX <sub>DiffRLSlope</sub>	Differential-mode RL slope f = 300 MHz to 6 GHz (see Figure 1)		−13		dB/dec
RL <sub>CMRX</sub>	Common-mode return loss f = 150 MHz to 300 MHz	5	10		dB
		5	17		
		2	23		
		1	16		
		1	12		
V <sub>diffRX</sub>	Differential input voltage PP f = 1.5 GHz and 3 GHz	120	1600		mV <sub>ppd</sub>
IB <sub>RX</sub>	Impedance balance f = 150 MHz to 300 MHz	30	41		dB
		30	38		
		20	32		
		10	26		
		10	25		
		4	20		
		4	17		

## Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TRANSMITTER AC/DC</b>					
$Z_{\text{diffTX}}$	Pair differential impedance	85	100	122	$\Omega$
$Z_{\text{SETX}}$	Single-ended impedance	40			$\Omega$
$V_{\text{TXtrans}}$	Sequencing transient voltage	Transient voltages on the serial data bus during power sequencing (lab load)	-1.2	1.2	V
$RL_{\text{DiffTX}}$	Differential-mode return loss	$f = 150 \text{ MHz to } 300 \text{ MHz}$	14	24	dB
		$f = 300 \text{ MHz to } 600 \text{ MHz}$	8	19	
		$f = 600 \text{ MHz to } 1.2 \text{ GHz}$	6	14	
		$f = 1.2 \text{ GHz to } 2.4 \text{ GHz}$	6	10	
		$f = 2.4 \text{ GHz to } 3 \text{ GHz}$	3	10	
$TX_{\text{DiffRLSlope}}$	Differential-mode RL slope	$f = 300 \text{ MHz to } 3 \text{ GHz}$ (see <a href="#">Figure 1</a> )		-13	dB/dec
$RL_{\text{CMTX}}$	Common-mode return loss	$f = 150 \text{ MHz to } 300 \text{ MHz}$	5	20	dB
		$f = 300 \text{ MHz to } 600 \text{ MHz}$	5	19	
		$f = 600 \text{ MHz to } 1.2 \text{ GHz}$	2	17	
		$f = 1.2 \text{ GHz to } 2.4 \text{ GHz}$	1	12	
		$f = 2.4 \text{ GHz to } 3.0 \text{ GHz}$	1	11	
$IB_{\text{TX}}$	Impedance balance	$f = 150 \text{ MHz to } 300 \text{ MHz}$	30	41	dB
		$f = 300 \text{ MHz to } 600 \text{ MHz}$	30	38	
		$f = 600 \text{ MHz to } 1.2 \text{ GHz}$	20	33	
		$f = 1.2 \text{ GHz to } 2.4 \text{ GHz}$	10	24	
		$f = 2.4 \text{ GHz to } 3 \text{ GHz}$	10	26	
		$f = 3 \text{ GHz to } 5 \text{ GHz}$	4	22	
		$f = 5 \text{ GHz to } 6.5 \text{ GHz}$	4	21	
DE	Output de-emphasis (relative to transition bit)	$f = 3 \text{ GHz, DE1 or DE2 = 0}$	0		dB
		$f = 3 \text{ GHz, DE1 or DE2 = 1}$	-2		
		$f = 3 \text{ GHz, DE1 or DE2 = NC}$	-4		
$Diff_{V_{\text{ppTX\_DE}}}$	Differential output-voltage swing dc level	$f = 3 \text{ GHz, DE1 or DE2 = 0}$	550		mV
		$f = 3 \text{ GHz, DE1 or DE2 = 1}$	830		
		$f = 3 \text{ GHz, DE1 or DE2 = NC}$	630		
$VCM_{\text{AC\_TX}}$	TX AC CM voltage	At 1.5 GHz	20	50	$\text{mVppd}$
		At 3 GHz	12	26	$\text{dBmV}$ (rms)
		At 6 GHz	13	30	
$VCM_{\text{TX}}$	Common-mode voltage			1.8	V
$TxR/F_{\text{imb}}$	TX rise-fall imbalance	At 3 Gbps		6%	20%
$TxAmp_{\text{imb}}$	TX amplitude imbalance			2%	10%

## 6.6 Power Dissipation Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	MAX	UNIT
$P_D$	215	288	mW
$P_{\text{SD}}$		5	mW

## 6.7 Timing Requirements

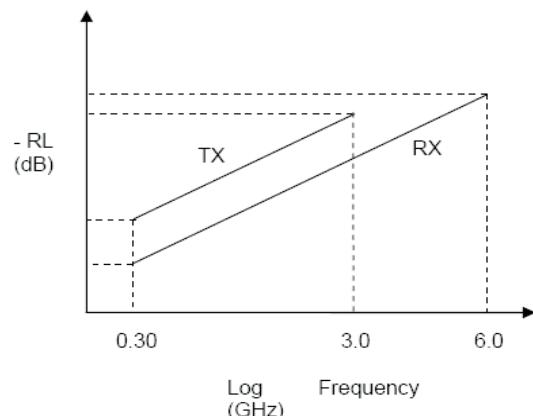
			MIN	NOM	MAX	UNIT
<b>DEVICE PARAMETERS</b>						
AutoLP <sub>ENTRY</sub>	Auto low-power entry time	Electrical idle at input (see <a href="#">Figure 4</a> )	80	105	130	μs
AutoLP <sub>EXIT</sub>	Auto low-power exit time	After first signal activity (see <a href="#">Figure 4</a> )	42	50	ns	
<b>TRANSMITTER AC/DC</b>						
t <sub>DE</sub>	De-emphasis duration	DEW1 or DEW2 = 0	94	ps		
		DEW1 or DEW2 = 1	215			
<b>OUT-OF-BAND (OOB)</b>						
t <sub>OOB1</sub>	OOB mode enter	See <a href="#">Figure 4</a>	3	5	ns	
t <sub>OOB2</sub>	OOB mode exit	See <a href="#">Figure 4</a>	3	5	ns	

## 6.8 Switching Characteristics

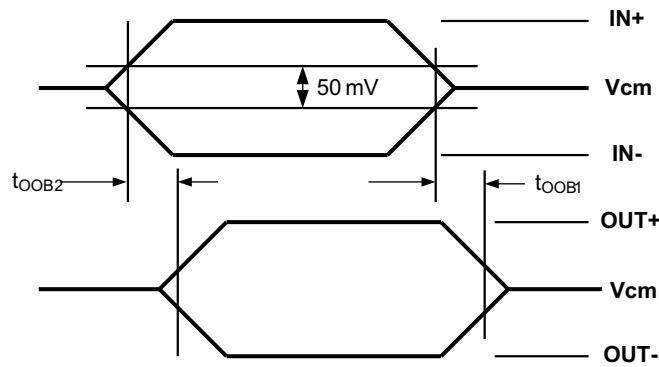
over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>DEVICE PARAMETERS</b>						
t <sub>pDelay</sub>	Propagation delay	Measured using K28.5 pattern (see <a href="#">Figure 2</a> )	323	400	ps	
t <sub>ENB</sub>	Device enable time	EN 0 → 1		5	μs	
t <sub>DIS</sub>	Device disable time	EN 1 → 0		2	μs	
<b>RECEIVER AC/DC</b>						
t <sub>20-80RX</sub>	Rise/fall time	Rise times and fall times measured between 20% and 80% of the signal. SATA 6-Gbps speed measured 1 in. (2.5 cm) from device pin.	62	75	ps	
t <sub>skewRX</sub>	Differential skew	Difference between the single-ended midpoint of the RX+ signal rising or falling edge, and the single-ended midpoint of the RX– signal falling or rising edge.		30	ps	
<b>TRANSMITTER AC/DC</b>						
t <sub>20-80TX</sub>	Rise/fall time	Rise times and fall times measured between 20% and 80% of the signal. At 6 Gbps under no load conditions.	42	55	75	ps
t <sub>skewTX</sub>	Differential skew	Difference between the single-ended mid-point of the TX+ signal rising or falling edge, and the single-ended mid-point of the TX– signal falling or rising edge.	6	20	ps	
<b>TRANSMITTER JITTER</b>						
DJ <sub>TX</sub>	Deterministic jitter <sup>(1)</sup> at CP in <a href="#">Figure 9</a>	VID = 500 mVpp, UI = 333 ps, K28.5 control character	0.06	0.07	UIp-p	
RJ <sub>TX</sub>	Residual random jitter <sup>(1)</sup>	VID = 500 mVpp, UI = 333 ps, K28.7 control character	0.01	2	ps-rms	
DJ <sub>TX</sub>	Deterministic jitter <sup>(1)</sup> at CP in <a href="#">Figure 9</a>	VID = 500 mVpp, UI = 167 ps, K28.5 control character	0.08	0.16	UIp-p	
RJ <sub>TX</sub>	Residual random jitter <sup>(1)</sup>	VID = 500 mVpp, UI = 167 ps, K28.7 control character	0.09	2	ps-rms	

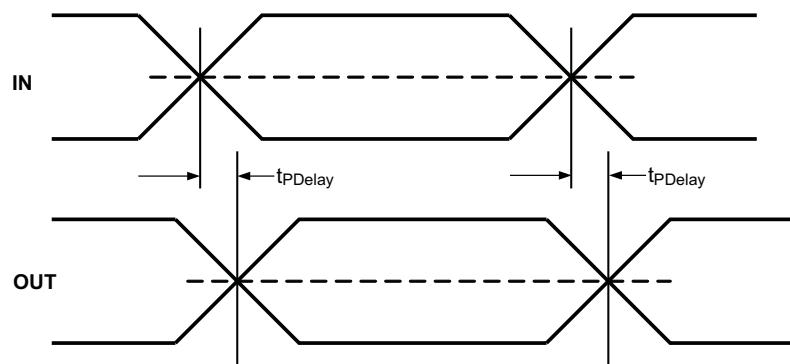
(1)  $TJ = (14.1 \times RJ_{SD} + DJ)$ , where  $RJ_{SD}$  is one standard deviation value of RJ Gaussian distribution. Jitter measurement is at the SATA connector and includes jitter generated at the package connection on the printed circuit board, and at the board interconnect as shown in [Figure 9](#).



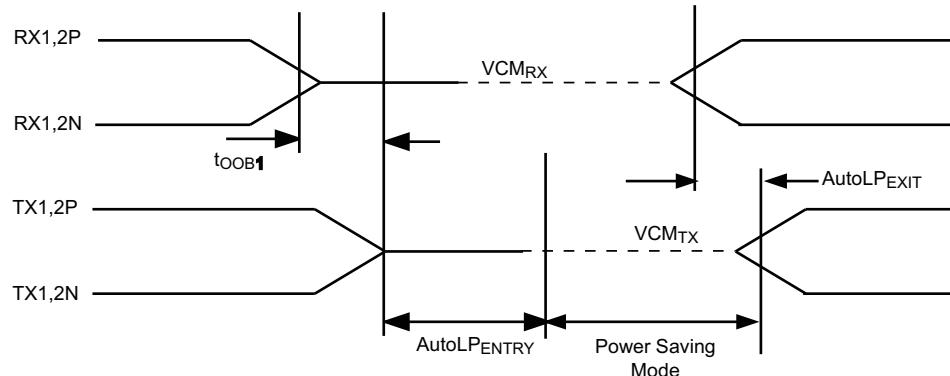
**Figure 1. TX, RX Differential Return Loss Limits**



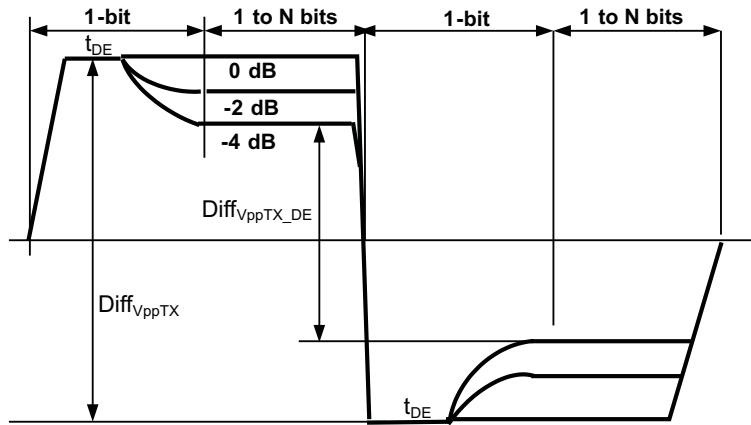
**Figure 2. OOB Enter and Exit Timing**



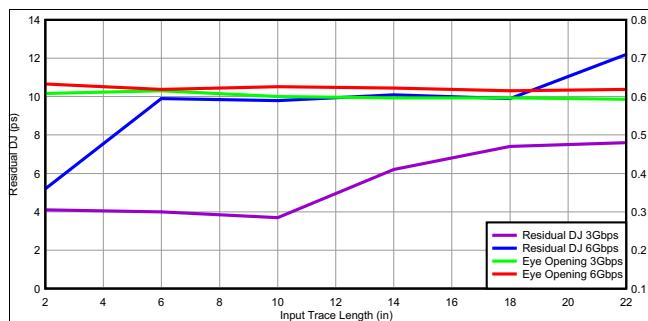
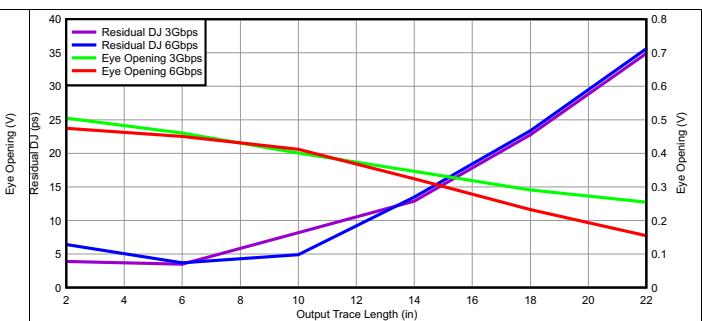
**Figure 3. Propagation Delay Timing Diagram**



**Figure 4. Auto Low-Power Mode Enter and Exit Timing**


**Figure 5. TX Differential Output**

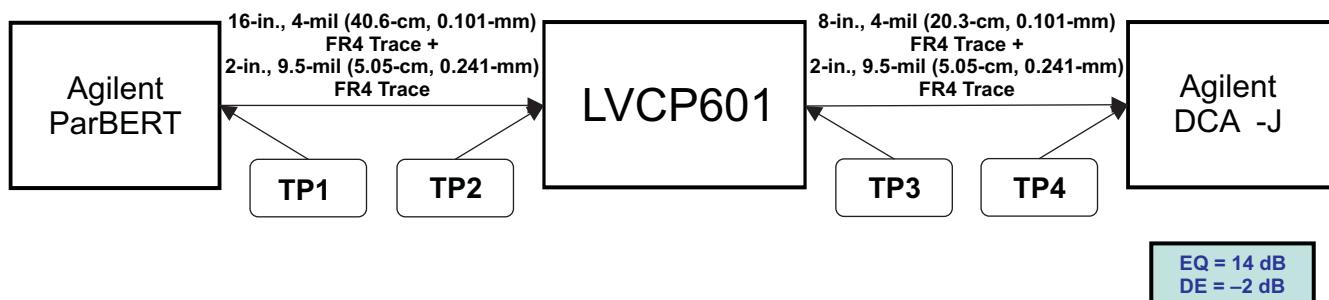
## 6.9 Typical Characteristics


**Figure 6. Residual DJ and Eye Opening  
vs Input Trace Length**

**Figure 7. Residual DJ and Eye Opening  
vs Output Trace Length**

## 7 Parameter Measurement Information

- Input signal characteristics
  - Data rate = 6 Gbps, 3 Gbps, 1.5 Gbps
  - Amplitude = 500 mVp-p
  - Data pattern = K28.5
- SN75LVCP601 device setup
  - Temperature = 25°C
  - Voltage = 3.3 V
  - De-emphasis duration = 117 ps (short)
  - Equalization and de-emphasis set to optimize performance at 6 Gbps

## With LVCP601



## Without LVCP601

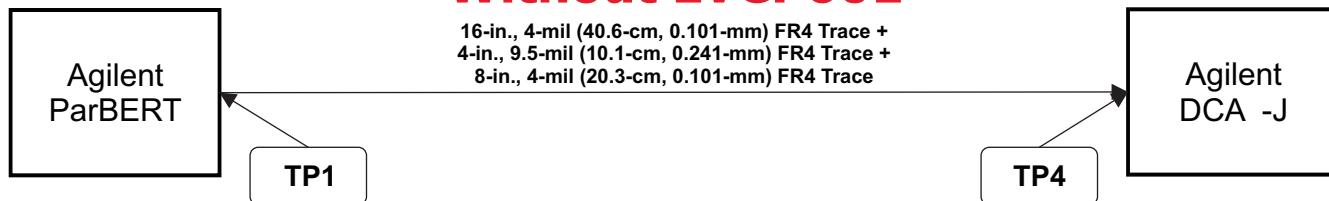


Figure 8. Performance Curve Measurement Setup

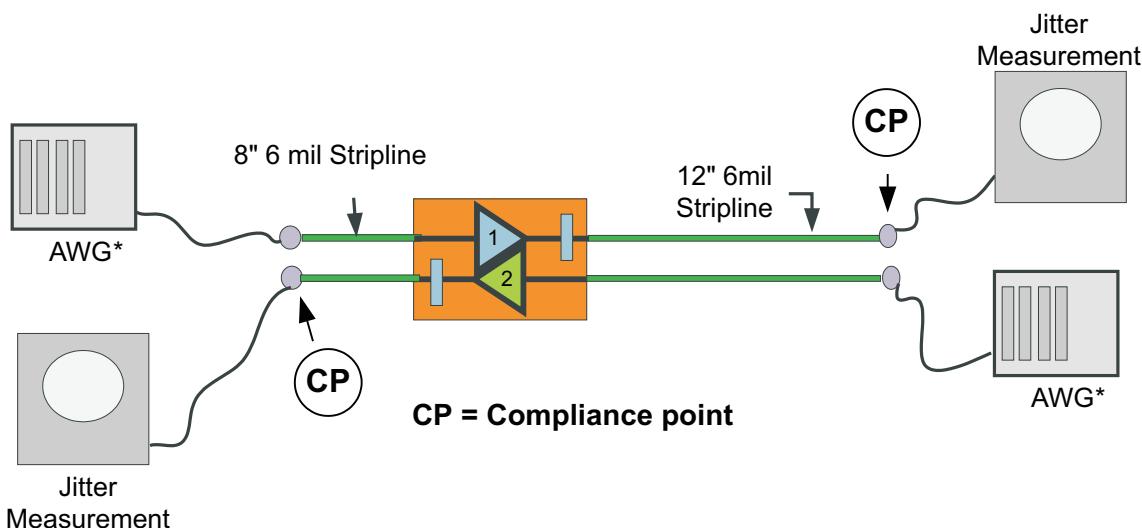
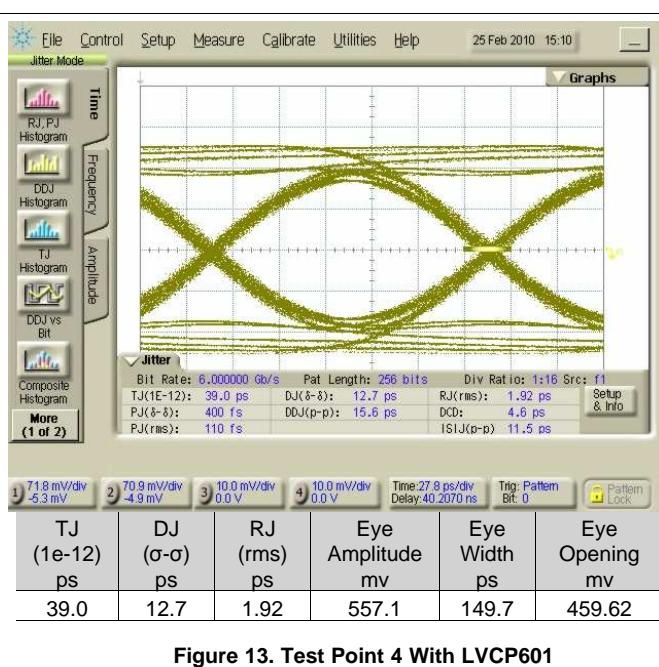
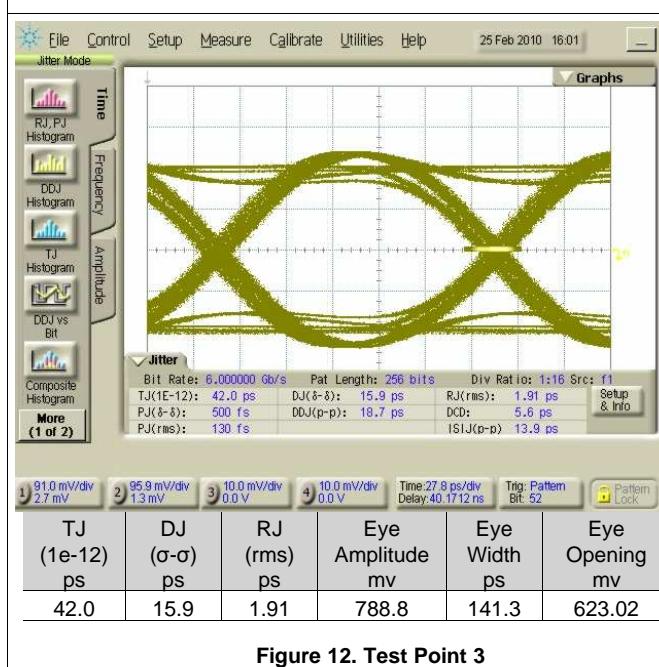
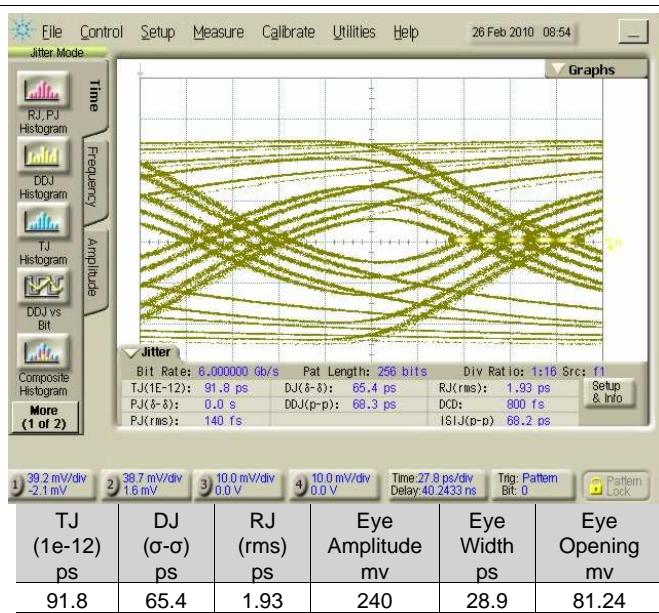
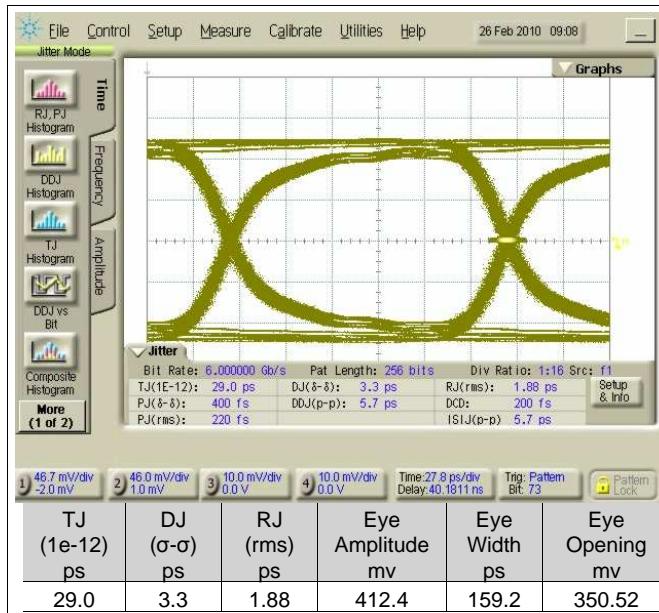
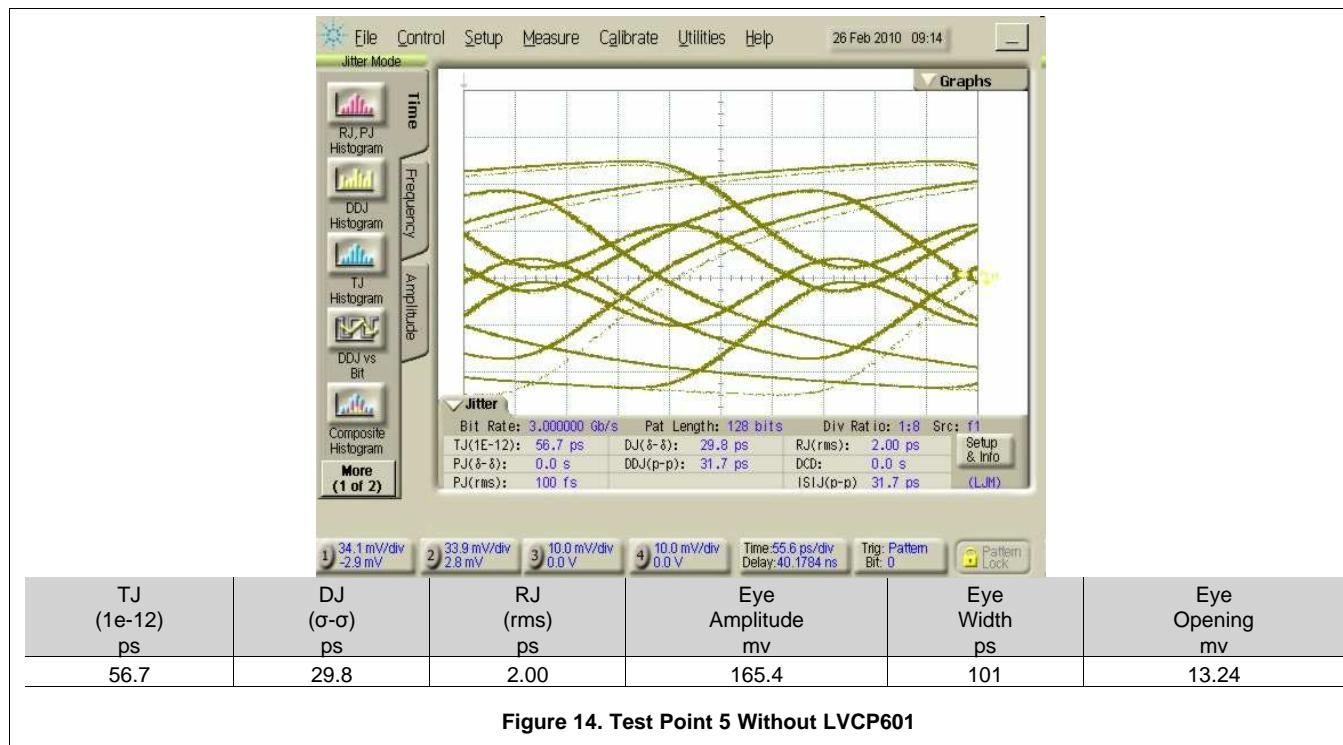
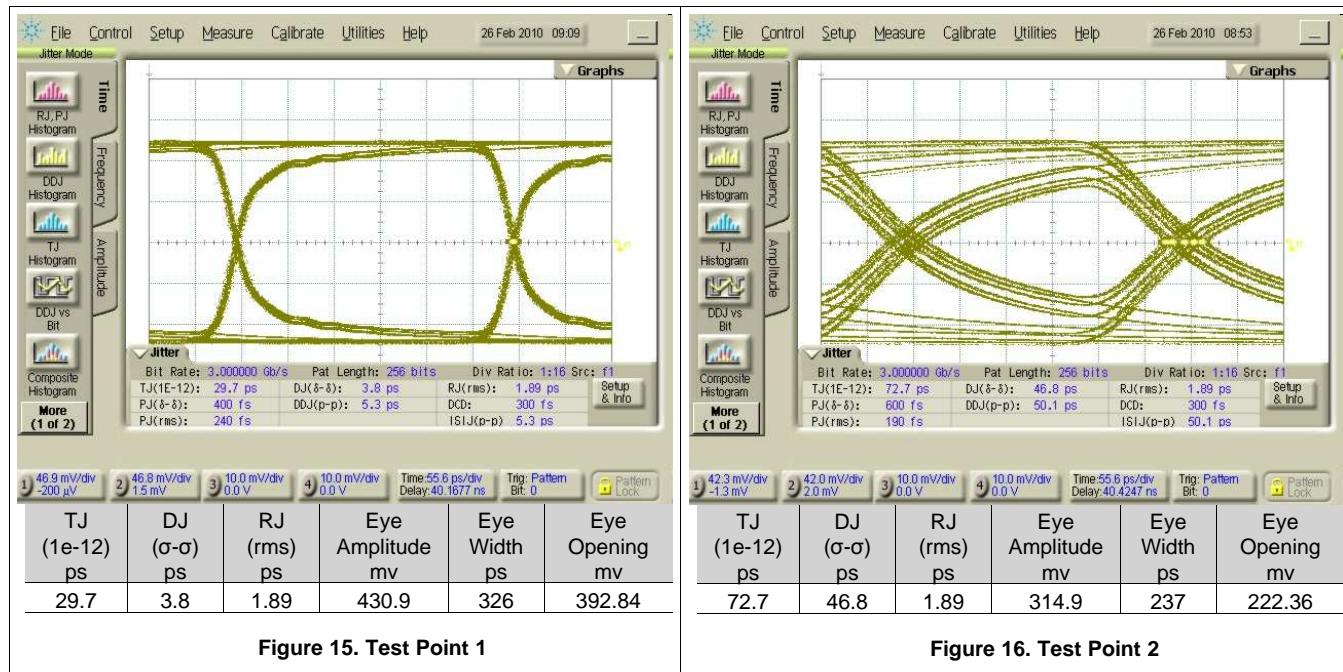
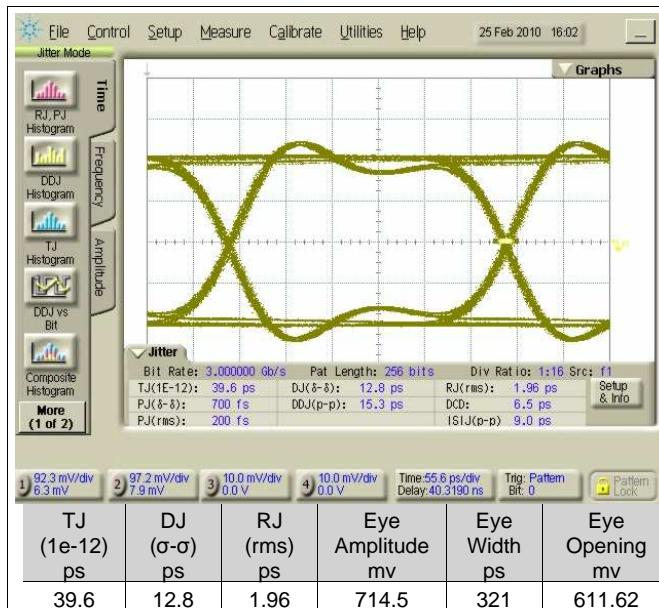
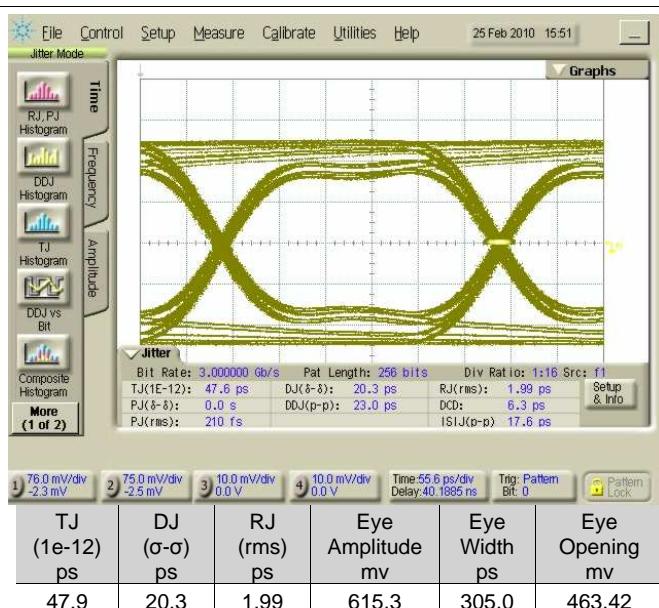
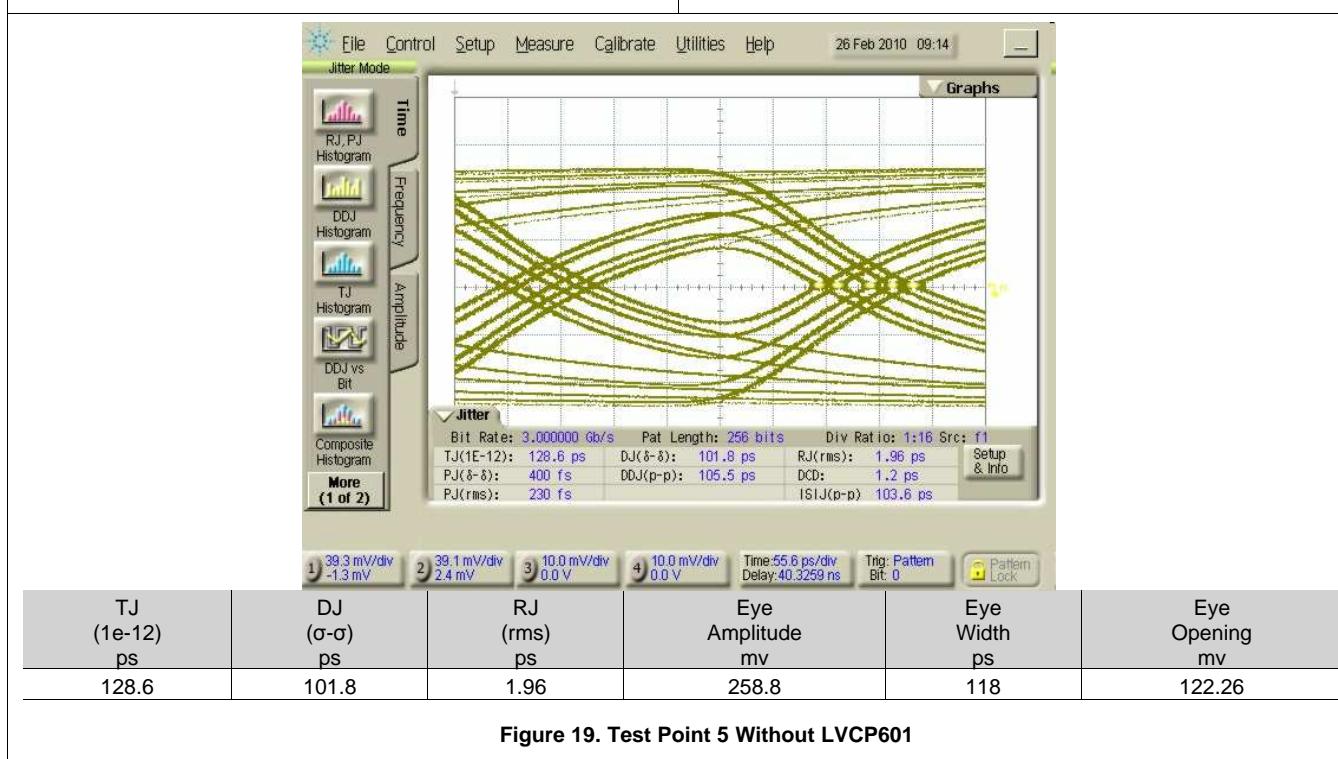


Figure 9. Jitter Measurement Test Condition

## 7.1 Jitter and VOD Results: Case 1 at 6 Gbps



**Jitter and VOD Results: Case 1 at 6 Gbps (continued)**

**Figure 14. Test Point 5 Without LVCP601**
**7.2 Jitter and VOD Results: Case 2 at 3 Gbps**

**Figure 15. Test Point 1**
**Figure 16. Test Point 2**

**Jitter and VOD Results: Case 2 at 3 Gbps (continued)**

**Figure 17. Test Point 3**

**Figure 18. Test Point 4 With LVCP601**

**Figure 19. Test Point 5 Without LVCP601**

### 7.3 Jitter and VOD Results: Case 3 at 1.5 Gbps

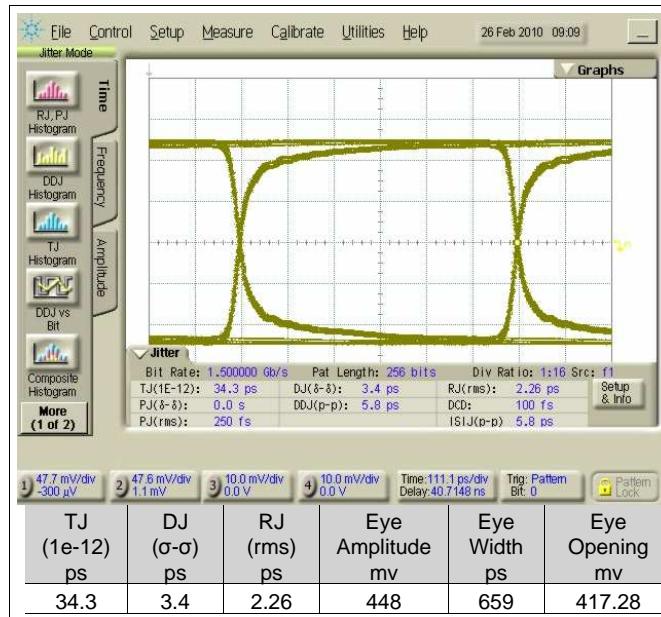


Figure 20. Test Point 1

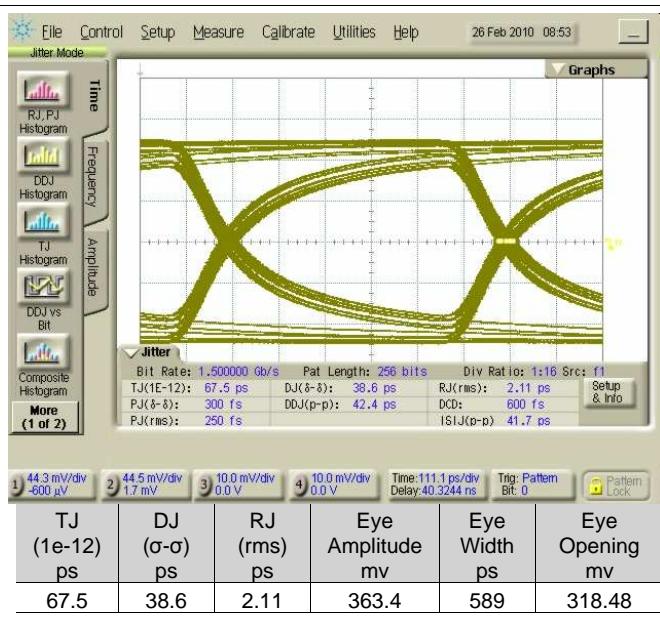


Figure 21. Test Point 2

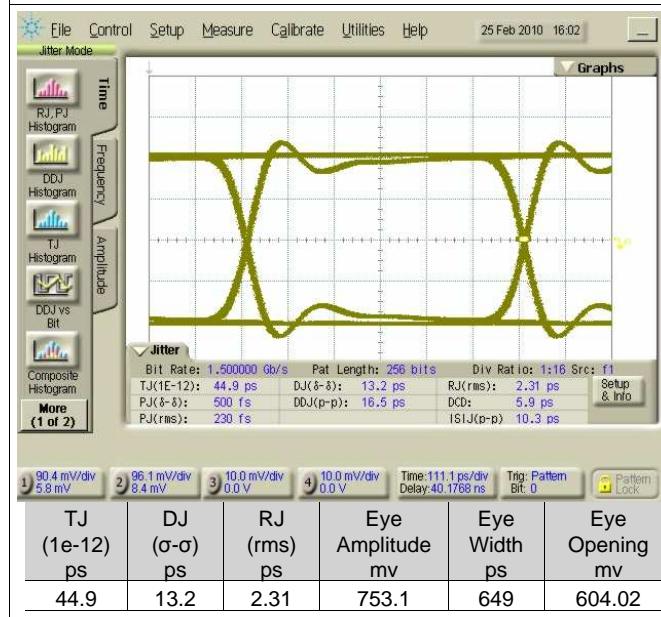


Figure 22. Test Point 3

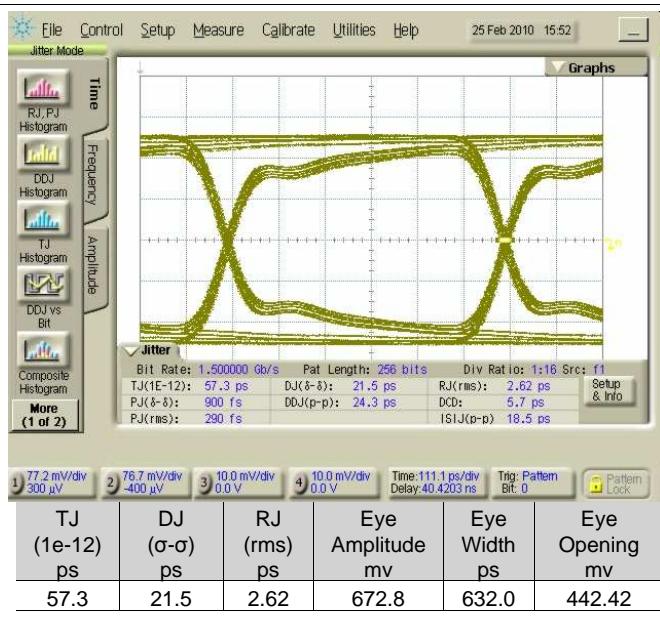
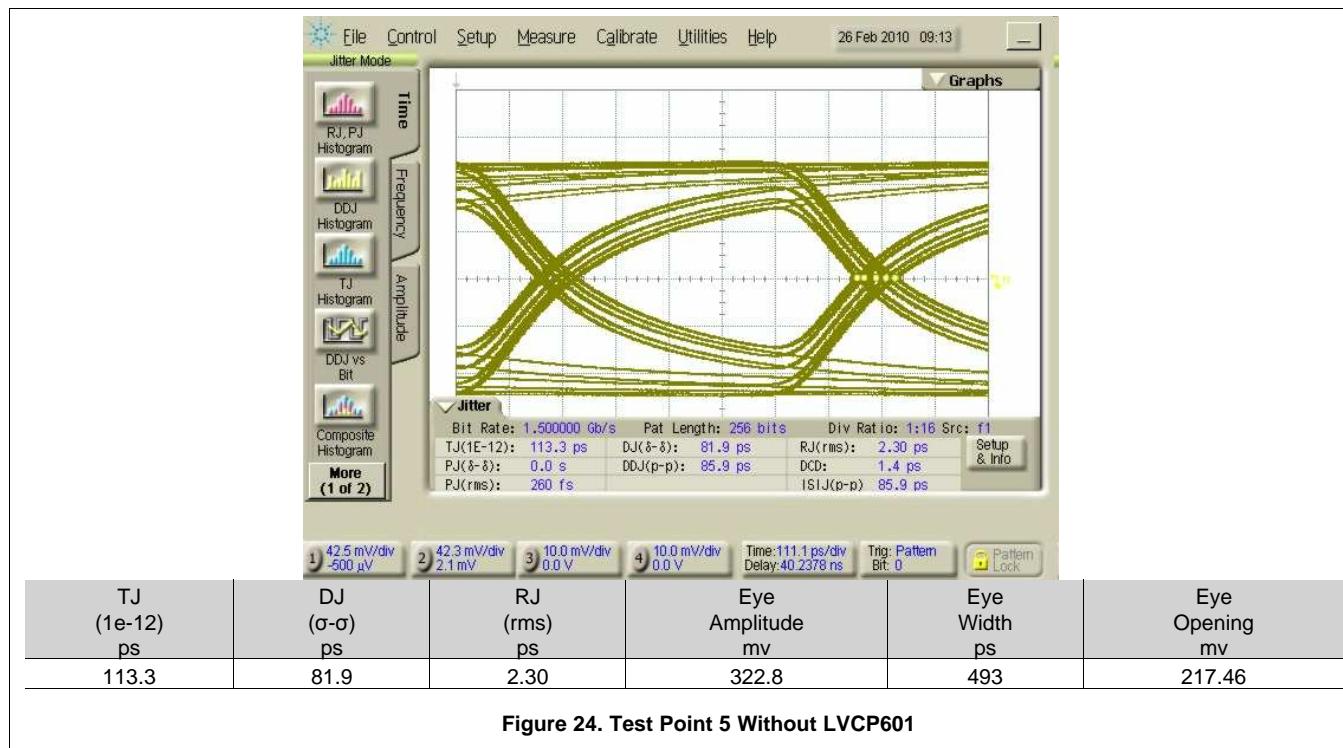


Figure 23. Test Point 4 With LVCP601

## Jitter and VOD Results: Case 3 at 1.5 Gbps (continued)



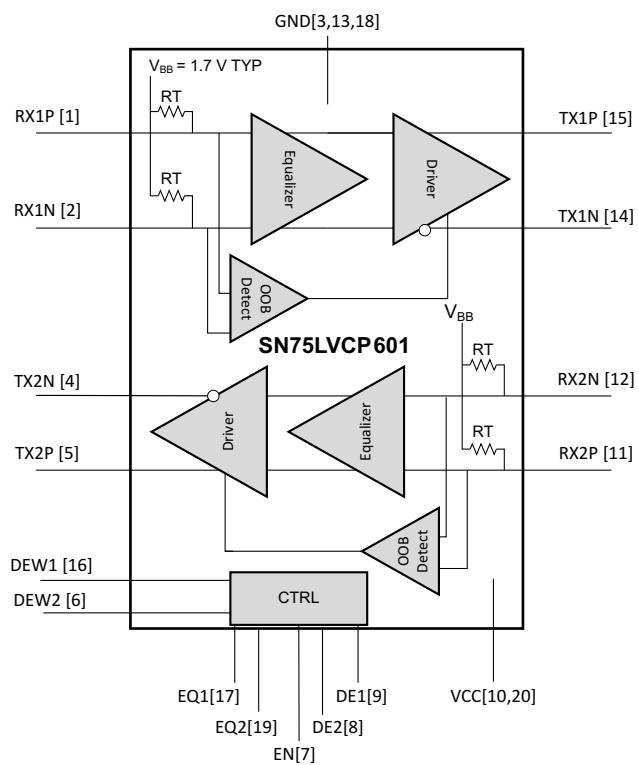
## 8 Detailed Description

### 8.1 Overview

The SN75LVCP601 device is a dual-channel, single-lane SATA redriver and signal conditioner supporting data rates up to 6 Gbps.

This device complies with SATA physical link 2m and 3i specifications. The SN75LVCP601 device is designed to handle interconnect losses at both its input and output. The input stage of each channel offers selectable equalization settings that can be programmed to match the loss of the channel. The outputs provide selectable de-emphasis to compensate for the distortion the SATA signal is expected to experience. The level of equalization and de-emphasis settings depend on the length of interconnect and its characteristics. Equalization for input trace and output trace are individually controlled by the setting of EQ1 and EQ2. De-emphasis levels for input and output trace are individually controlled by the setting of DE1, DE2, DEW1 and DEW2 pins.

### 8.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

**Figure 25. Data Flow Block Diagram**

## 8.3 Feature Description

### 8.3.1 Input Equalization

Each differential input of the SN75LVCP601 device has programmable equalization in its front stage. [Table 1](#) lists the equalization. The input equalizer design recovers a signal even when no eye is present at the receiver, and effectively supports FR4 trace at the input anywhere from 4 in. (10.2 cm) to 20 in. (50.8 cm) at SATA 6G speed.

### 8.3.2 Output De-Emphasis

The SN75LVCP601 device provides the de-emphasis settings shown in [Table 1](#). De-emphasis control is independent for each channel, controlled by the DE1 and DE2 pin settings as shown in [Table 1](#). The reference for the de-emphasis settings available in the device is the transition bit amplitude for each given configuration; this transition bit amplitude is different at 0 dB than the -2-dB and -4-dB settings by design. DEW1 and DEW2 control the DE durations for channels one and two, respectively. [Table 1](#) lists the recommended settings for these control pins. Output de-emphasis is capable of supporting FR4 trace at the output anywhere from 2 in. (5.1 cm) to 12 in. (30.5 cm) at SATA 3G/6G speed.

**Table 1. TX and RX EQ and DE Pulse-Duration Settings**

DE1 OR DE2	CH1 OR CH2 DE-EMPHASIS dB (at 6 Gbps)	EQ1 OR EQ2	CH1 OR CH2 Equalization dB (at 6 Gbps)
NC ( <b>default</b> )	-4	NC ( <b>default</b> )	0
0	0	0	7
1	-2	1	14
DEW1 OR DEW2	DEVICE FUNCTION → DE WIDTH FOR CH1/CH2		
0	De-emphasis pulse duration, short		
1 ( <b>default</b> )	De-emphasis pulse duration, long		

### 8.3.3 Out-of-Band (OOB) Support

The squelch detector circuit within the device enables full detection of OOB signaling as specified in the SATA specification. The device does not detect differential signal amplitude at the receiver input of 50 mVpp or less as an activity, and hence does not pass it to the output. The device detects differential signal amplitude of 150 mVp-p or more as an activity and therefore passes it to the output, providing an indication of the activity. Squelch circuit ON or OFF time is 5 ns, maximum. While in squelch mode, outputs are held to VCM.

## 8.4 Device Functional Modes

### 8.4.1 Low-Power Mode

There are two low-power modes supported by the SN75LVCP601 device, listed as follows:

1. Standby mode (triggered by the EN pin, EN = 0 V)
  - The enable (EN) pin controls the low-power mode. Pulling this pin LOW puts the device in standby mode within 2  $\mu$ s (max). In this mode, the device drives all its active components to their quiescent level, and differential outputs Hi-Z (open). Maximum power dissipation in this mode is 5 mW. Exiting from this mode to normal operation requires a maximum latency of 5  $\mu$ s.
2. Auto low-power mode (triggered when a given channel is in the electrically idle state for more than 100  $\mu$ s and EN = VCC)
  - The device enters and exits low-power mode by actively monitoring the input signal (VIDp-p) level on each of its channels independently. When the input signal on either or both channels is in the electrically idle state, that is, VIDp-p < 50 mV and stays in this state for >100  $\mu$ s, the associated channel enters into the low-power state. In this state, output of the associated channel goes to VCM and the device selectively shuts off some circuitry to lower power by >80% of its normal operating power. Exit time from the auto low-power mode is <50 ns.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SN75LVCP601 is a dual-channel SATA redriver and signal conditioner supporting data rates of 6 Gbps. The inputs incorporate an OOB (out-of-band) detector, which automatically squelches the output while maintaining a stable common-mode voltage compliant to the SATA link.

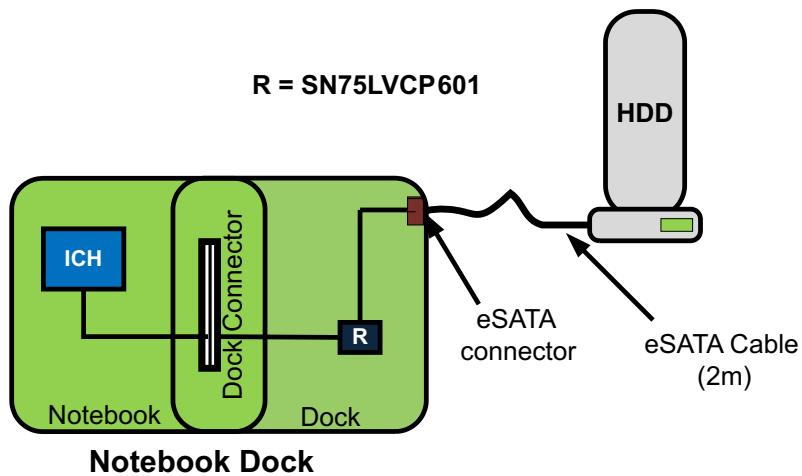
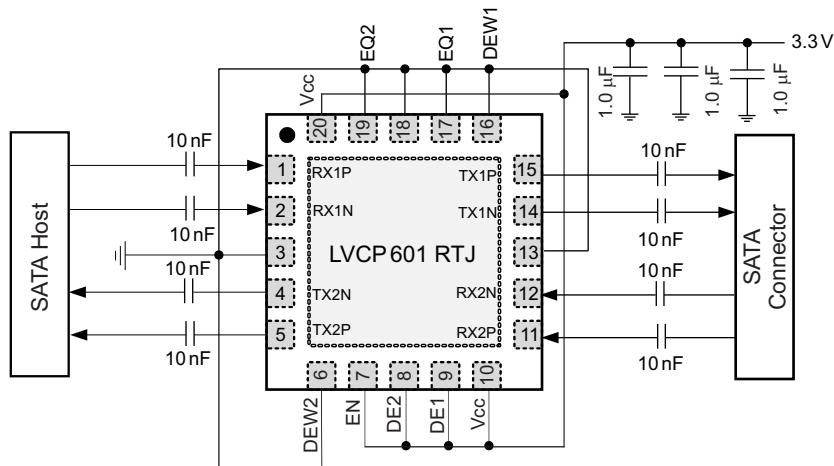


Figure 26. Typical SN75LVCP601 Placement in the System

### 9.2 Typical Application

This typical application describes how to configure the EQ, DE, and DEW configuration pins of the SN75LVCP601 device based on board trace length between the SATA Host and the SN75LVCP601 and the SN75LVCP601 and SATA Device. Actual configuration settings may differ due to additional factors such as board layout, trace widths, and connectors used in the signal path.

## Typical Application (continued)



Copyright © 2016, Texas Instruments Incorporated

- (1) Place supply capacitors close to device pin.
- (2) With no external control is implemented, one can leave EN open or tie it to the supply .
- (3) Output de-emphasis setting is for –2 dB, EQ for 7 dB, and DE duration for SATA I/II/III operation for both channels.
- (4) Actual EQ/DE duration settings depend on device placement relative to host and SATA connector.

**Figure 27. Typical Device Implementation**

### 9.2.1 Design Requirements

Typically, system trace length from the SATA host to the SN75LVCP601 device and trace length from the SN75LVCP601 device to a SATA device differ and require different equalization and de-emphasis settings for the host side and device side.

For example:

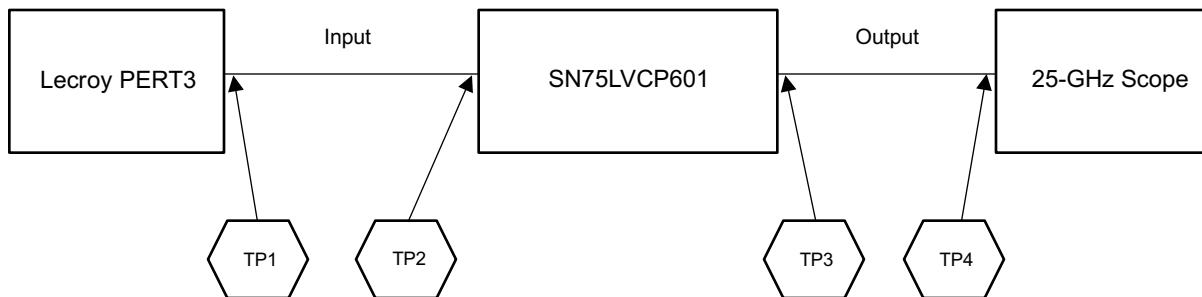
- A system with a 6-inch trace from the SN75LVCP601 device to a SATA host may set EQ1 (Rx1 $\pm$ ) to 7 dB, and DE2 (Tx2 $\pm$ ) to –2 dB and DEW2 (Tx2 $\pm$ ) to long pulse duration.
- The same system with a 1-inch trace from the SN75LVCP601 device to a SATA HDD may set EQ2 (Rx2 $\pm$ ) to 0 dB, and DE1 (Tx1 $\pm$ ) to 0 dB and DEW1 (Tx1 $\pm$ ) to short pulse duration.

Refer to [Application Curves](#) for recommended EQ, DE and DEW settings based on trace length. It is highly recommended to add both pullup- and pulldown-resistor options in the layout to fine-tune the settings if needed.

Input Signal Characteristics:

- Data Rate: 6 Gbps
- Pattern: PRBS7
- No pre-emphasis
- Signal amplitude: 500 mVp-p
- 18-inch SMA cable from test equipment to input and output trace

## Typical Application (continued)



**Figure 28. Measurement Set-up**

### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 Equalization Configuration

Each differential input of the SN75LVCP601 device has programmable equalization in the front stage. The equalization setting is shown in [Table 2](#). The input equalizer is designed to recover a signal even when no eye is present at the receiver and effectively supports FR4 trace input from 3 inches to greater than 24 inches at SATA 6 Gbps speed.

**Table 2. Equalization Settings**

EQ1, EQ2	CH1, CH2 EQUALIZATION dB (AT 6 Gbps)
NC	0
0	7
1	14

#### 9.2.2.2 De-emphasis Configuration

The SN75LVCP601 device provides the de-emphasis settings shown in [Table 3](#). De-emphasis is controlled independently for each channel and is set by the DE1, DE2, DEW1 and DEW2 pins of the SN75LVCP601 device. The recommended settings for these pins are listed in [Application Curves](#). Output de-emphasis is capable of supporting FR4 trace lengths at the output from 3 inches to 12+ inches at SATA 6 Gbps speed.

**Table 3. De-emphasis Settings**

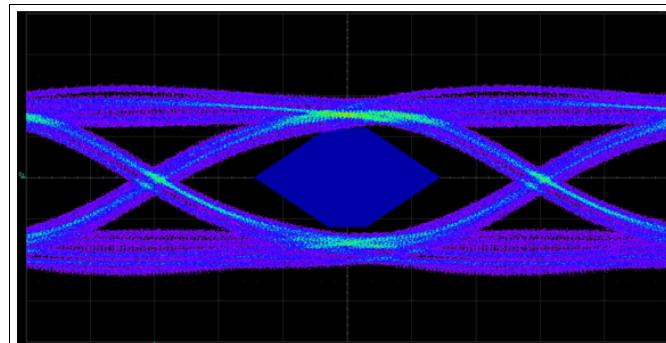
DE1, DE2	CH1, CH2 DE-EMPHASIS dB (AT 6 Gbps)
0	0
1	-2
NC	-4

**Table 4. DE Width Control**

DEW1, DEW2	DE-EMPHASIS WIDTH FOR CH1, CH2
0	Short de-emphasis pulse duration
1	Long de-emphasis pulse duration

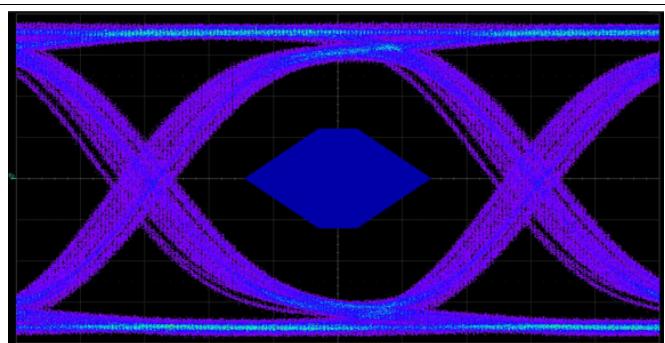
## 9.2.3 Application Curves

### 9.2.3.1 SN75LVCP601 Equalization Settings For Various Input Trace Lengths



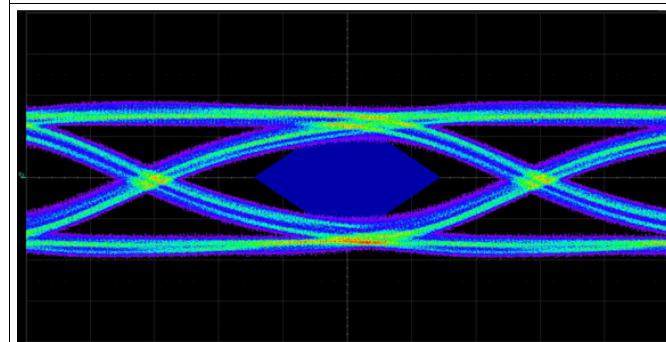
Input Trace Length = 3 in.  
EQ1, EQ2 Setting = NC (0 dB)

Figure 29. Input Eye (TP2)



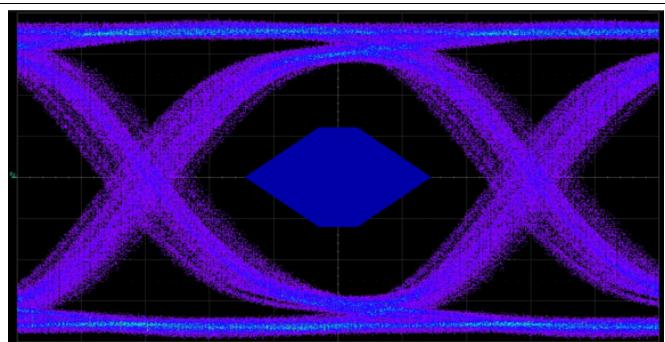
Input Trace Length = 3 in.  
EQ1, EQ2 Setting = NC (0 dB)

Figure 30. Output Eye (TP4)



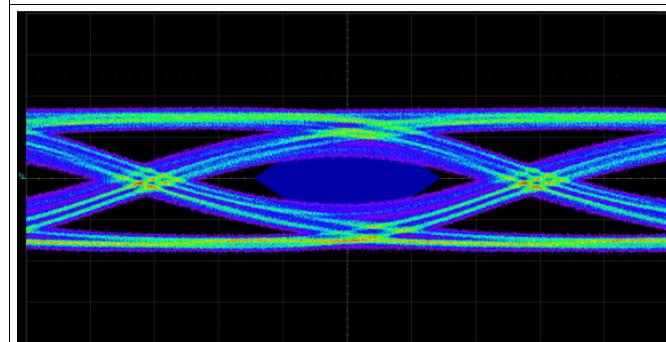
Input Trace Length = 6 in.  
EQ1, EQ2 Setting = 0 (7 dB)

Figure 31. Input Eye (TP2)



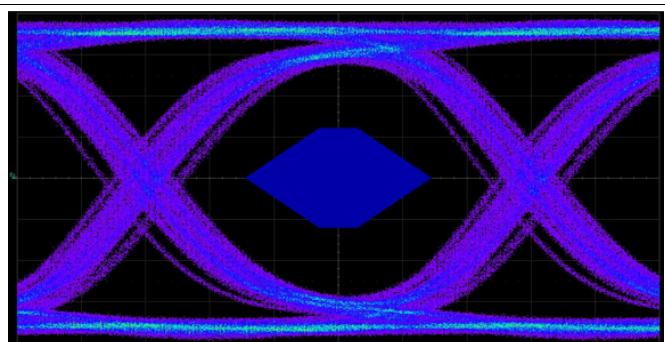
Input Trace Length = 6 in.  
EQ1, EQ2 Setting = 0 (7 dB)

Figure 32. Output Eye (TP2)



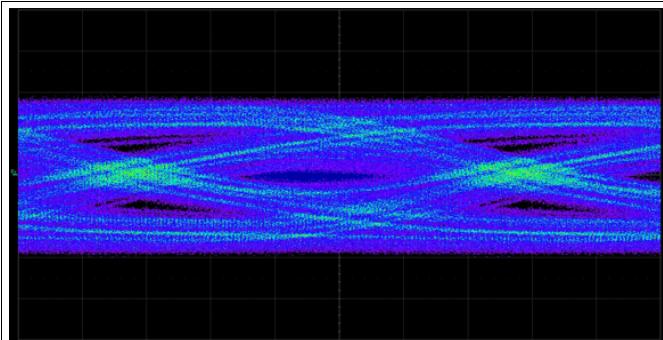
Input Trace Length = 12 in.  
EQ1, EQ2 Setting = 0 (7 dB)

Figure 33. Input Eye (TP2)



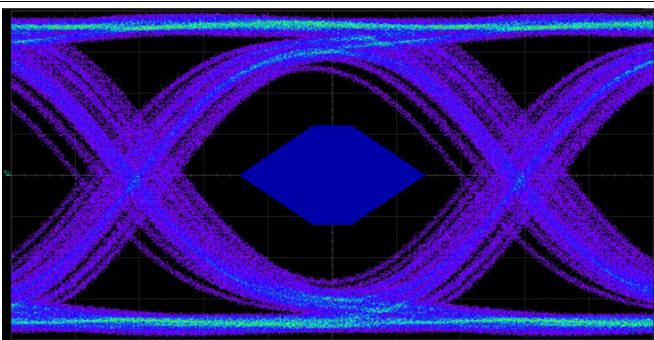
Input Trace Length = 12 in.  
EQ1, EQ2 Setting = 0 (7 dB)

Figure 34. Output Eye (TP2)



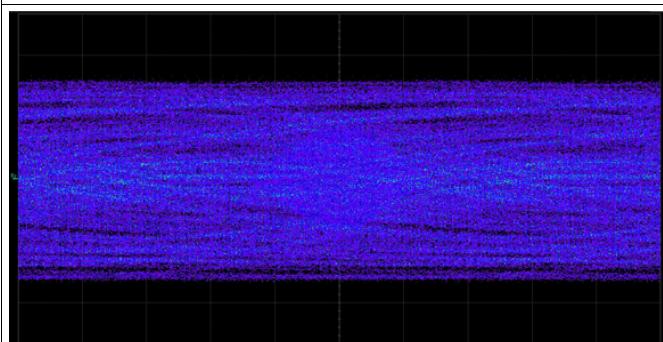
Input Trace Length = 24 in.  
EQ1, EQ2 Setting = 0 (7 dB)

Figure 35. Input Eye (TP2)



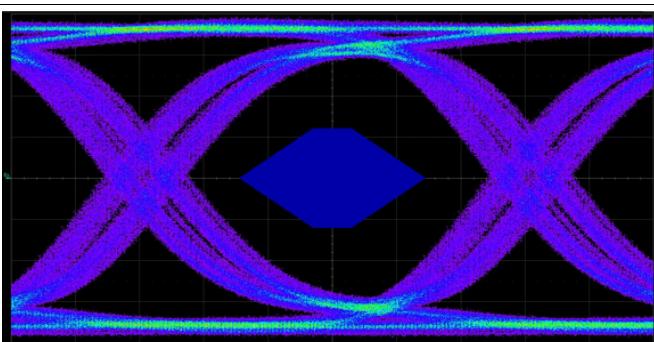
Input Trace Length = 24 in.  
EQ1, EQ2 Setting = 0 (7 dB)

Figure 36. Output Eye (TP2)



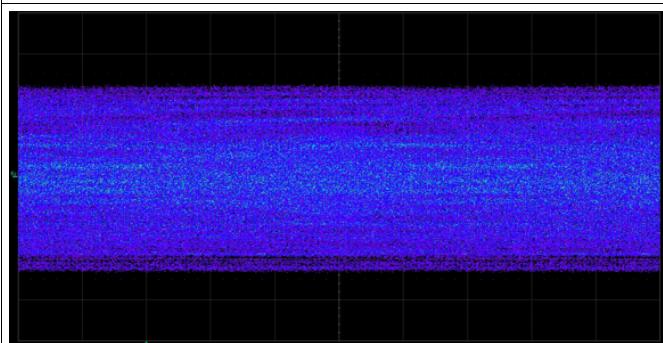
Input Trace Length = 36 in.  
EQ1, EQ2 Setting = 1 (14 dB)

Figure 37. Input Eye (TP2)



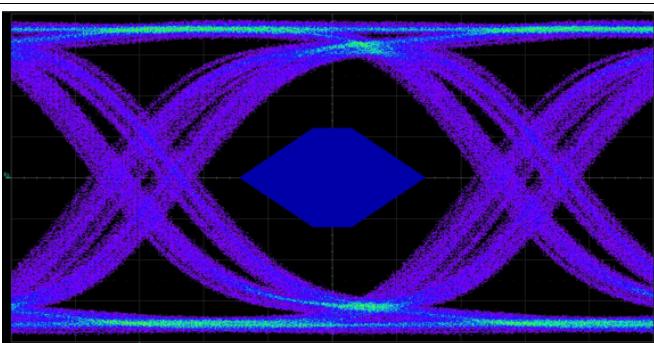
Input Trace Length = 36 in.  
EQ1, EQ2 Setting = 1 (14 dB)

Figure 38. Output Eye (TP2)



Input Trace Length = 48 in.  
EQ1, EQ2 Setting = 1 (14 dB)

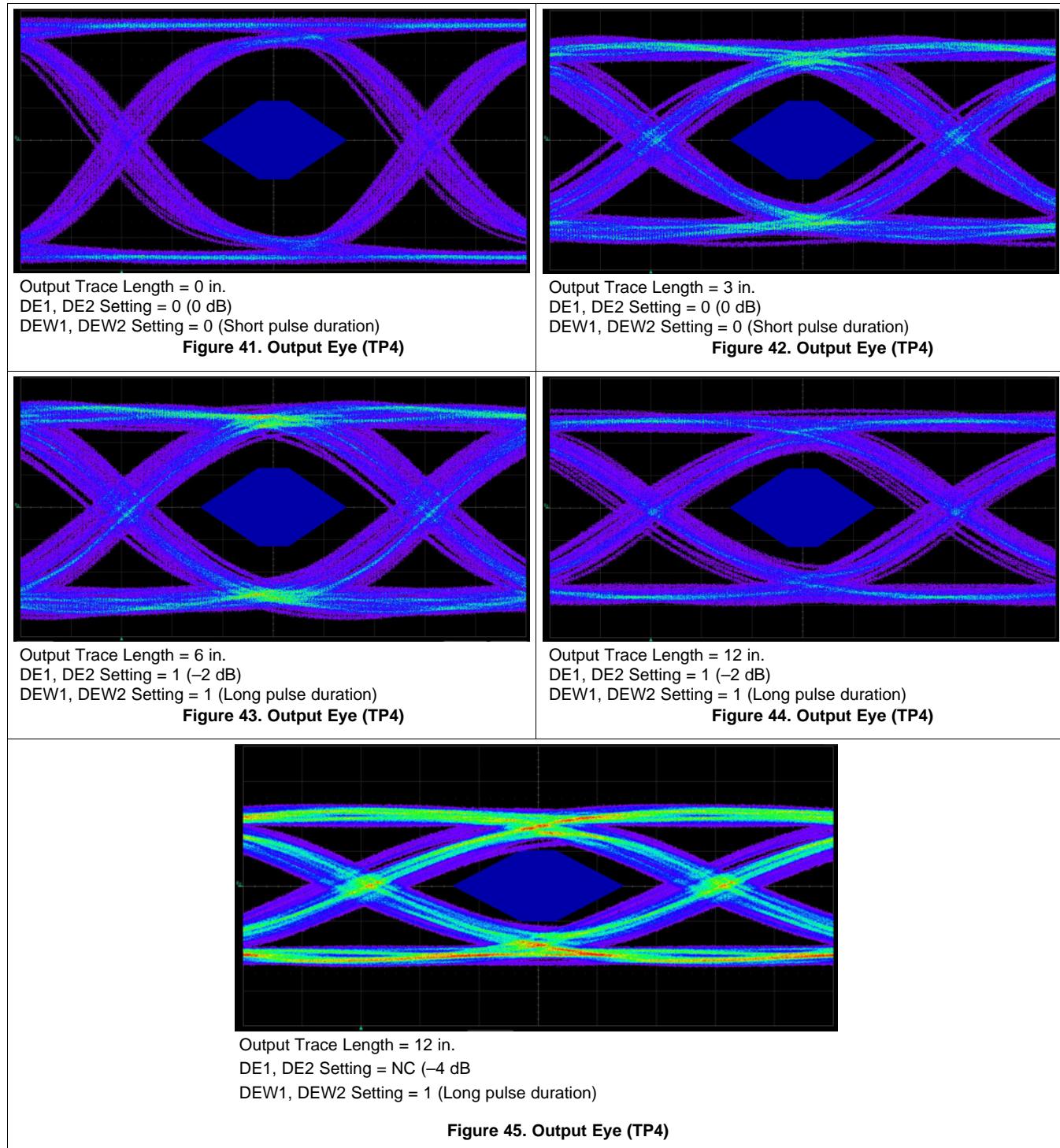
Figure 39. Input Eye (TP2)



Input Trace Length = 36 in.  
EQ1, EQ2 Setting = 1 (14 dB)

Figure 40. Output Eye (TP2)

### 9.2.3.2 SN75LVCP601 De-emphasis Settings For Various Output Trace Lengths

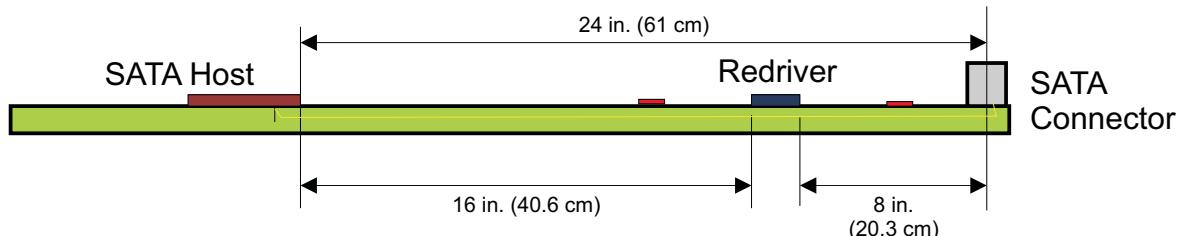


## 10 Power Supply Recommendations

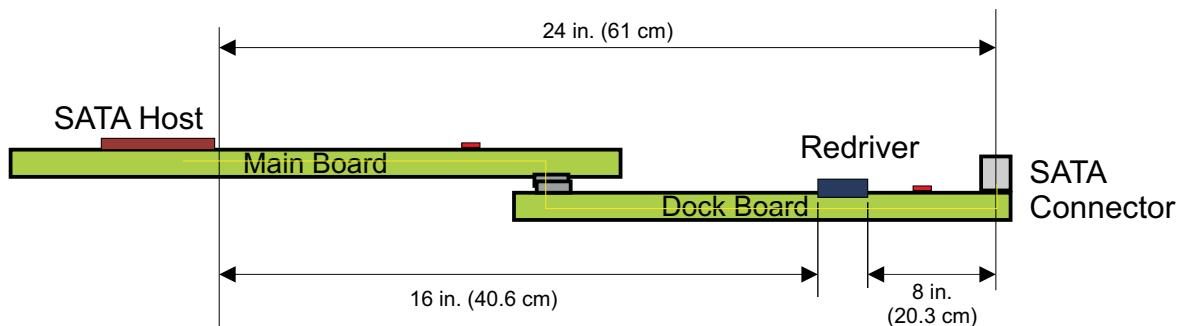
The design of SN75LVCP601 device is for operation from one 3.3-V supply. Always practice proper power-supply sequencing procedure. Apply VCC first, before application of any input signals to the device. The power-down sequence is in reverse order.

## 11 Layout

### 11.1 Layout Guidelines



**Redriver on Motherboard**



**Redriver on Dock Board**

Example: Suggested trace-length values are values based on TI spice simulations (done over programmable limits of input EQ and output de-emphasis) to meet SATA loss and jitter specification.

Actual trace length supported by the LVCP601 may be more or less than suggested values and depends on board layout, trace widths, and number of connectors used in the SATA signal path.

**Figure 46. Trace Length Example for LVCP601**

## 11.2 Layout Example

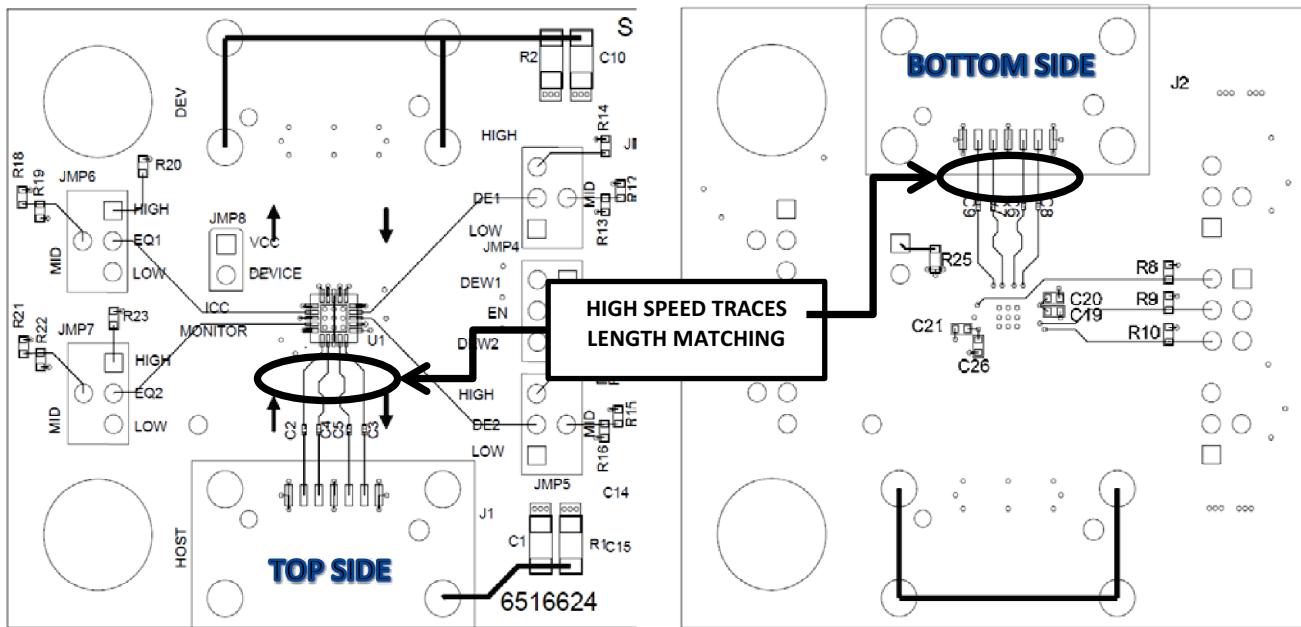


Figure 47. SN65LVCP601 EVM

## 12 Device and Documentation Support

### 12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.2 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.4 Glossary

[SLYZ022](#) — *TI Glossary.*

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75LVCP601RTJR	ACTIVE	QFN	RTJ	20	3000	RoHS & Green	Call TI   NIPDAU	Level-2-260C-1 YEAR	0 to 85	LVC601	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75LVCP601RTJT	ACTIVE	QFN	RTJ	20	250	RoHS & Green	Call TI   NIPDAU	Level-2-260C-1 YEAR	0 to 85	LVC601	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

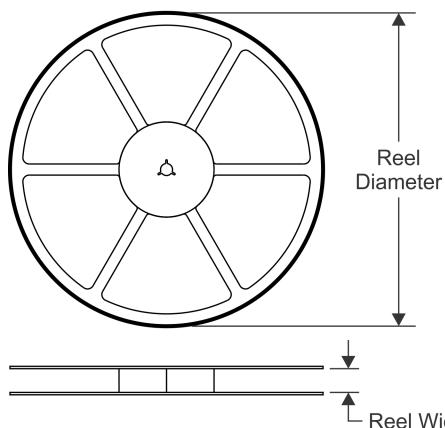
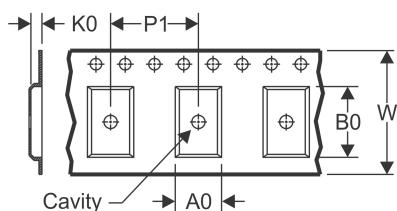


www.ti.com

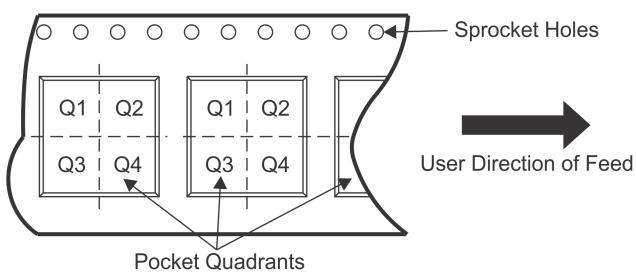
## PACKAGE OPTION ADDENDUM

10-Dec-2020

---

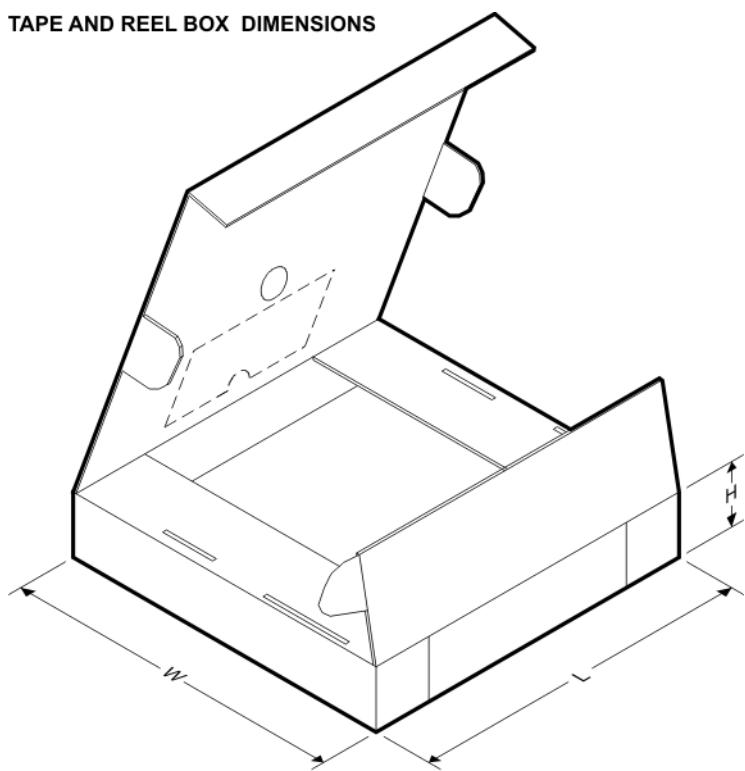
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVCP601RTJR	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN75LVCP601RTJT	QFN	RTJ	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVCP601RTJR	QFN	RTJ	20	3000	367.0	367.0	35.0
SN75LVCP601RTJT	QFN	RTJ	20	250	210.0	185.0	35.0

## GENERIC PACKAGE VIEW

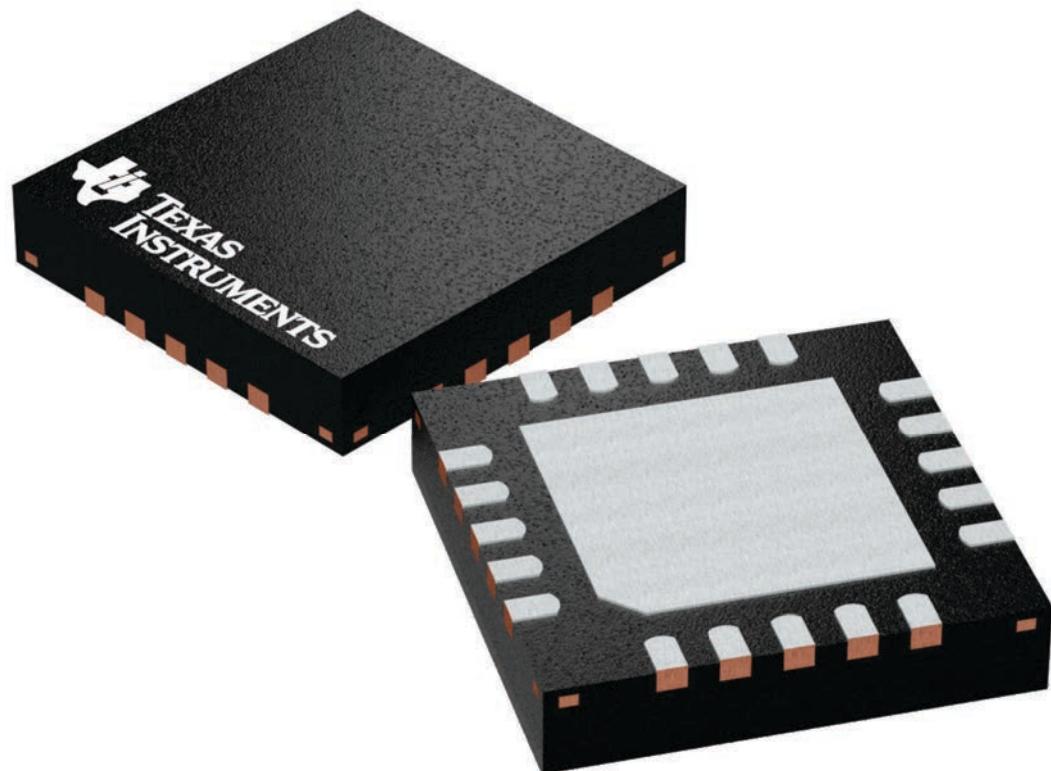
**RTJ 20**

**WQFN - 0.8 mm max height**

**4 x 4, 0.5 mm pitch**

**PLASTIC QUAD FLATPACK - NO LEAD**

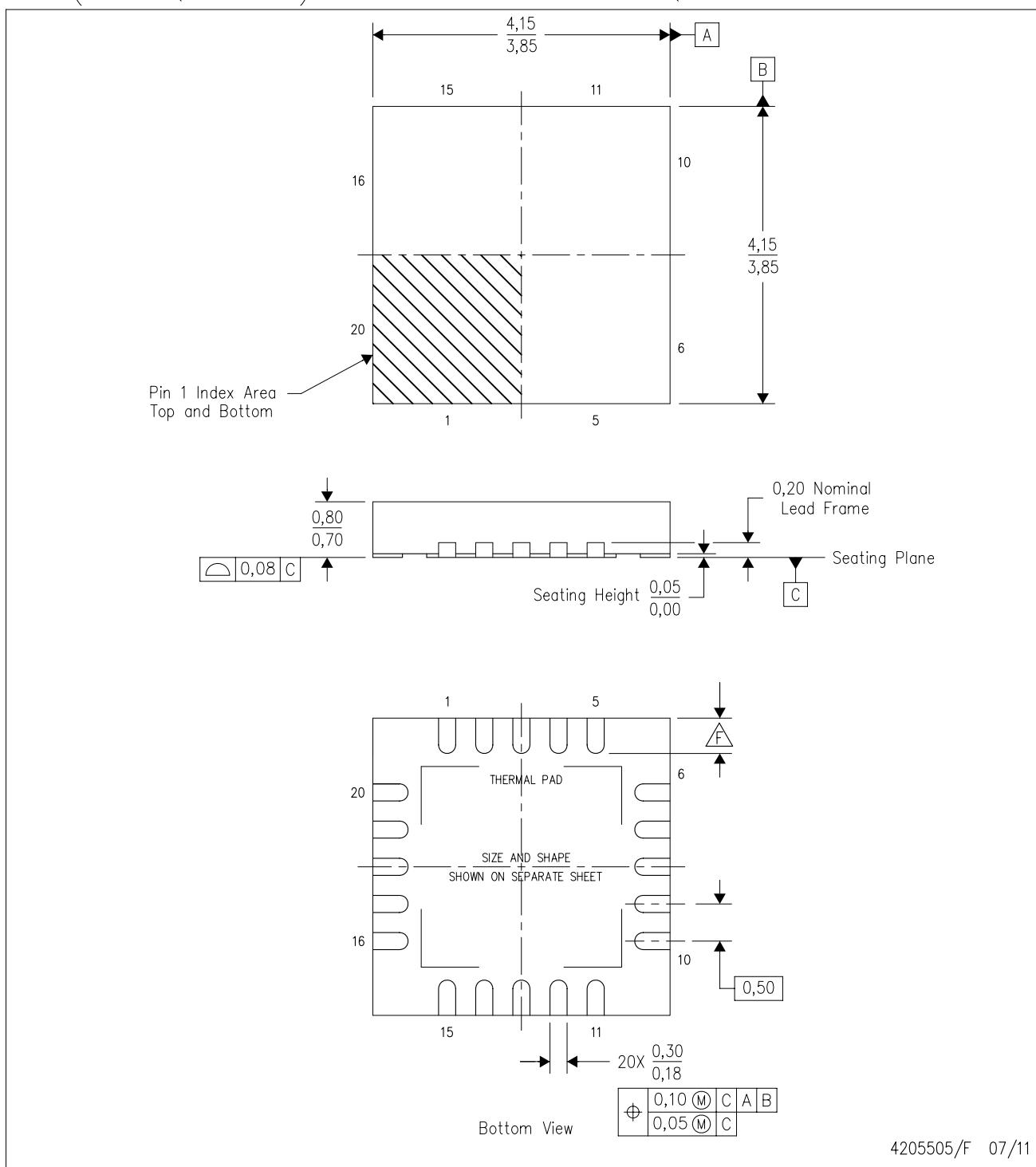
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224842/A

RTJ (S-PWQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
- This drawing is subject to change without notice.
- QFN (Quad Flatpack No-Lead) package configuration.
- The package thermal pad must be soldered to the board for thermal and mechanical performance.
- See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

## THERMAL PAD MECHANICAL DATA

RTJ (S-PWQFN-N20)

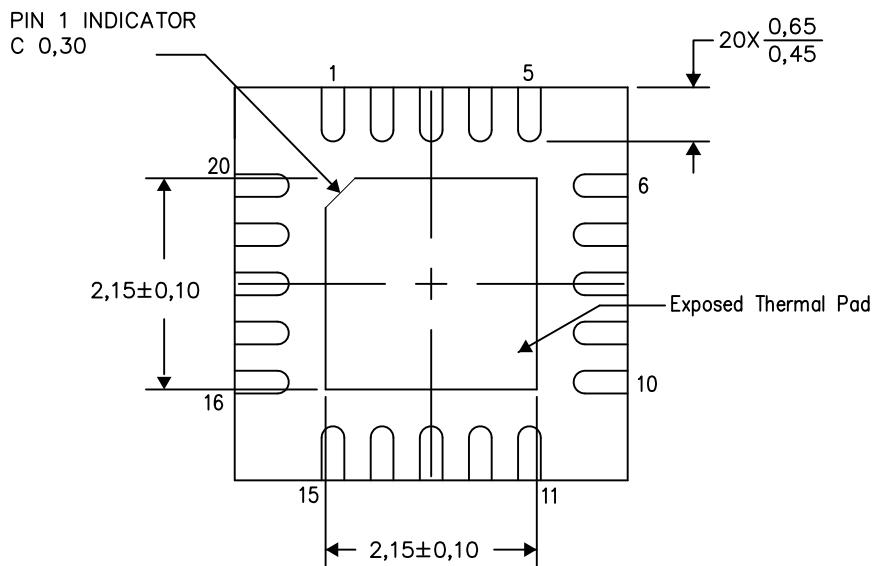
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206256-3/V 05/15

NOTE: All linear dimensions are in millimeters

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2021, Texas Instruments Incorporated