SNx4HC138 3 线路至 8 线路解码器/多路信号分离器

1 特性

- 专门针对高速存储器解码器和数据传输系统
- 宽工作电压范围（2V 至 6V）
- 输出可驱动多达 10 个低功耗肖特基晶体管逻辑电路 (LSTTL) 负载
- 低功耗，I_{CC} 最大值为 80μA
- t_{pd} 典型值 = 15ns
- ±4mA 输出驱动（在 5V 时）
- 低输入电流，最大值为 1μA
- 低电平有效输出（所选输出为低电平）
- 纳入三个使能输入以简化级联或数据接收

2 应用

- 发光二极管 (LED) 显示屏
- 服务器
- 大型家电
- 电力基础设施
- 楼宇自动化
- 工厂自动化

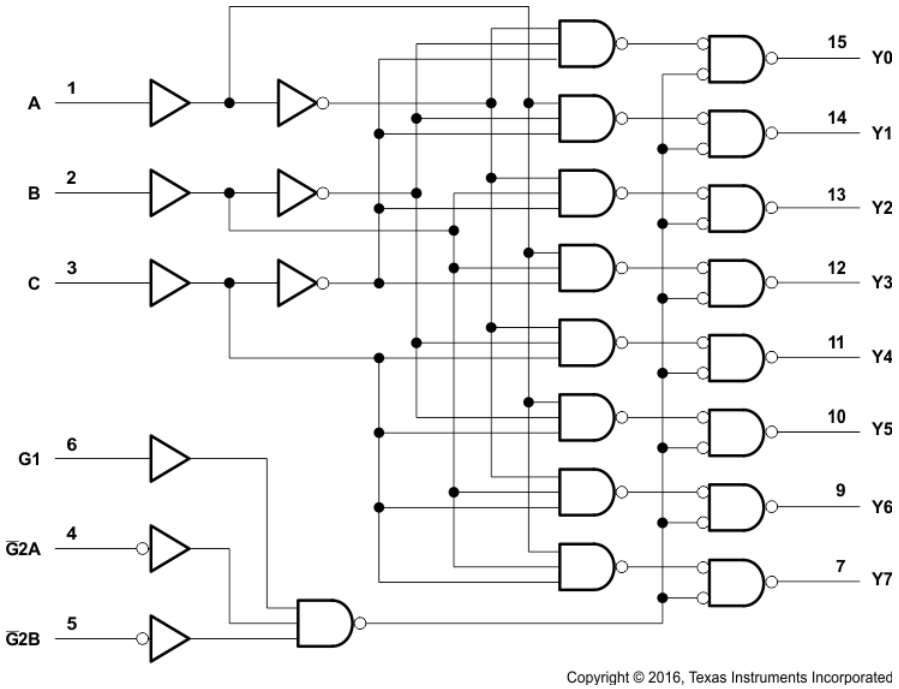
3 说明

SNx4HC138 器件设计用于需要极短传播延迟时间的高性能存储器解码或数据路由应用。在高性能存储系统中，可使用此类解码器来尽可能地消除系统解码的影响。与使用高速使能电路的高速存储器一起使用时，这些解码器的延迟时间和存储器的使能时间通常小于存储器的典型存取时间。这意味着解码器引起的有效系统延迟可以忽略不计。

器件信息

器件型号	封装[1]	封装尺寸（标称值）
SN74HC138D	SOIC (16)	9.90mm x 3.90mm
SN74HC138DB	SSOP (16)	6.20mm x 5.30mm
SN74HC138N	PDIP (16)	19.32 mm x 6.35 mm
SN74HC138NS	SO (16)	10.20mm x 5.30mm
SN74HC138PW	TSSOP (16)	5.00mm x 4.40mm
SN54HC138J	陶瓷双列直插封装 (CDIP) (16)	21.34 mm x 6.92 mm
SN54HC138W	CFP (16)	10.16 mm x 6.73 mm
SN54HC138FK	LCCC (20)	8.89 mm x 8.89 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



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所示引脚编号用于 D、DB、J、N、NS、PW 和 W 封装。

功能方框图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

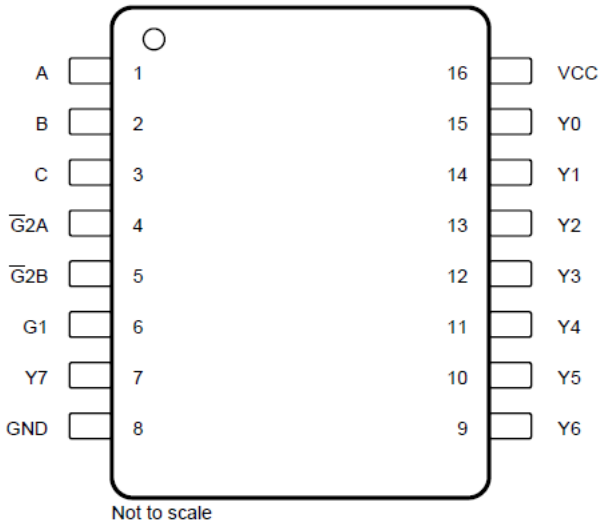
注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (September 2003) to Revision F (September 2016)	Page
• 添加了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分	1
• 删除了“订购信息”表；请参阅数据表末尾的 POA	1
• Changed $R_{\theta JA}$ values from 73 to 87.3 (D), from 82 to 104.3 (DB), from 67 to 54.8 (N), from 64 to 91.1 (NS), and from 108 to 114.6 (PW)	5

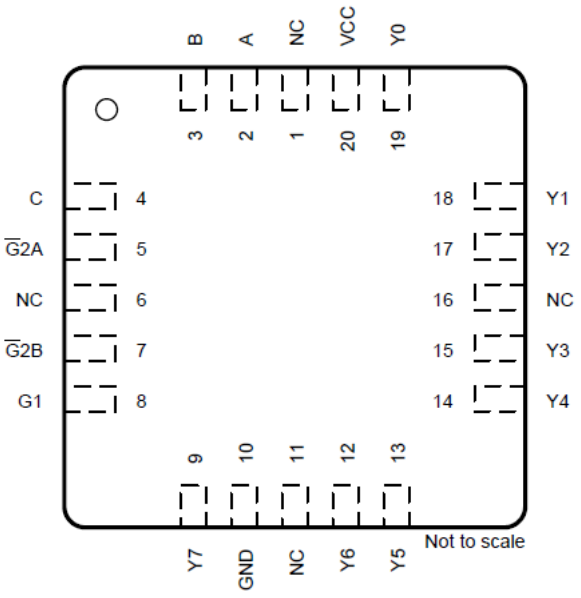
Changes from Revision F (September 2016) to Revision G (October 2021)	Page
• Updated the ESD ratings table to fit modern data sheet standards	4

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5 Pin Configuration and Functions



SOIC, SSOP, PDIP, SO, TSSOP, CDIP, or CFP Package
16-Pin D, DB, N, NS, PW, J or W
Top View



NC: No internal connection

LCCC Package
20-Pin FK
Top View

Pin Functions

PIN			I/O[1]	DESCRIPTION
NAME	SOIC, SSOP, PDIP, SO, TSSOP, CDIP, CFP	LCCC		
A	1	2	I	Select input A (least significant bit)
B	2	3	I	Select input B
C	3	4	I	Select input C (most significant bit)
$\overline{G}$2A	4	5	I	Active low enable A
$\overline{G}$2B	5	7	I	Active low enable B
G1	6	8	I	Active high enable
GND	8	10	—	Ground
NC	—	1, 6, 11, 16	—	No internal connection
V_{CC}	16	20	—	Supply voltage
Y0	15	19	O	Output 0 (least significant bit)
Y1	14	18	O	Output 1
Y2	13	17	O	Output 2
Y3	12	15	O	Output 3
Y4	11	14	O	Output 4
Y5	10	13	O	Output 5
Y6	9	12	O	Output 6
Y7	7	9	O	Output 7 (most significant bit)

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current(2)	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings: SN74HC138

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 6 V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 6 V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall time	V_{CC} = 2 V			1000	ns
		V_{CC} = 4.5 V			500	
		V_{CC}= 6 V			400	
C_{pd}	Power dissipation capacitance (no load)			85		pF
T_A	Operating free-air temperature	SN54HC138	–55		125	°C
		SN74HC138	–40		85	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

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6.4 Thermal Information: SN74HC138

THERMAL METRIC[1]		SN74HC138					UNIT
		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87.3	104.3	54.8	91.1	141.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.8	54.7	42.1	49.5	49.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.8	54.9	34.8	51.5	59.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.2	17.7	27	17.8	6.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44.5	54.4	34.7	51.2	59.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: SN54HC138

THERMAL METRIC[1]		SN54HC138[2]			UNIT
		J (CDIP)	W (CFP)	FK (LCCC)	
		16 PINS	16 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	—	—	—	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.4	68.1	49	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	—	118.4	47.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	—	—	7.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.5	—	—	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	17.7	9	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) $R_{\theta JC}$ follows MIL-STD-883, and $R_{\theta JB}$ follows JESD51.

6.6 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = – 20 µA	V_{CC} = 2 V	1.9	1.998		V
			V_{CC} = 4.5 V	4.4	4.499		
			V_{CC} = 6 V	5.9	5.999		
		I_{OH} = – 4 mA, V_{CC} = 4.5 V		3.98	4.3		
		I_{OH}= – 5.2 mA, V_{CC} = 6 V		5.48	5.8		
V_{OL}	V_I= V_{IH} or V_{IL}	I_{OL} = 20 µA	V_{CC} = 2 V		0.002	0.1	V
			V_{CC} = 4.5 V		0.001	0.1	
			V_{CC} = 6 V		0.001	0.1	
		I_{OL} = 4 mA, V_{CC} = 4.5 V			0.17	0.26	
		I_{OL} = 5.2 mA, V_{CC} = 6 V			0.15	0.26	
I_I	V_I = V_{CC} or 0, V_{CC} = 6 V				±0.1	±100	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0, V_{CC} = 6 V					8	µA
C_i	V_{CC} = 2 V to 6 V				3	10	pF

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6.7 Electrical Characteristics: SN74HC138

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 μA	V_{CC} = 2 V	1.9			V
			V_{CC} = 4.5 V	4.4			
			V_{CC} = 6 V	5.9			
		I_{OH} = –4 mA, V_{CC} = 4.5 V		3.84			
		I_{OH}= –5.2 mA, V_{CC} = 6 V		5.34			
V_{OL}	V_I= V_{IH} or V_{IL}	I_{OL} = 20 μA	V_{CC} = 2 V			0.1	V
			V_{CC} = 4.5 V			0.1	
			V_{CC} = 6 V			0.1	
		I_{OL} = 4 mA, V_{CC} = 4.5 V				0.33	
		I_{OL} = 5.2 mA, V_{CC} = 6 V				0.33	
I_I	$V_I = V_{CC}$ or 0, V_{CC} = 6 V					±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0, V_{CC} = 6 V					80	μA
C_i	V_{CC} = 2 V to 6 V					10	pF

6.8 Electrical Characteristics: SN54HC138

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 μA	V_{CC} = 2 V	1.9			V
			V_{CC} = 4.5 V	4.4			
			V_{CC} = 6 V	5.9			
		I_{OH} = –4 mA, V_{CC} = 4.5 V		3.7			
		I_{OH}= –5.2 mA, V_{CC} = 6 V		5.2			
V_{OL}	V_I= V_{IH} or V_{IL}	I_{OL} = 20 μA	V_{CC} = 2 V			0.1	V
			V_{CC} = 4.5 V			0.1	
			V_{CC} = 6 V			0.1	
		I_{OL} = 4 mA, V_{CC} = 4.5 V				0.4	
		I_{OL} = 5.2 mA, V_{CC} = 6 V				0.4	
I_I	$V_I = V_{CC}$ or 0, V_{CC} = 6 V					±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0, V_{CC} = 6 V					160	μA
C_i	V_{CC} = 2 V to 6 V					10	pF

6.9 Switching Characteristics

T_A = 25°C and C_L = 50 pF (unless otherwise noted; see 节 7)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	From A, B, or C (input) to any Y (output)	V_{CC} = 2 V		67	180	ns
		V_{CC} = 4.5 V		18	36	
		V_{CC} = 6 V		15	31	
	From enable (input) to any Y (output)	V_{CC} = 2 V		66	155	
		V_{CC} = 4.5 V		18	31	
		V_{CC} = 6 V		15	26	
t_t	To any output	V_{CC} = 2 V		38	75	ns
		V_{CC} = 4.5 V		8	15	
		V_{CC} = 6 V		6	13	

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6.10 Switching Characteristics: SN74HC138

over recommended operating free-air temperature range and C_L = 50 pF (unless otherwise noted; see 节 7)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	From A, B, or C (input) to any Y (output)	V_{CC} = 2 V			225	ns
		V_{CC} = 4.5 V			45	
		V_{CC} = 6 V			38	
	From enable (input) to any Y (output)	V_{CC} = 2 V			195	
		V_{CC} = 4.5 V			39	
		V_{CC} = 6 V			33	
t_t	To any output	V_{CC} = 2 V			95	ns
		V_{CC} = 4.5 V			19	
		V_{CC} = 6 V			16	

6.11 Switching Characteristics: SN54HC138

over recommended operating free-air temperature range and C_L = 50 pF (unless otherwise noted; see 节 7)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	From A, B, or C (input) to any Y (output)	V_{CC} = 2 V			270	ns
		V_{CC} = 4.5 V			54	
		V_{CC} = 6 V			46	
	From enable (input) to any Y (output)	V_{CC} = 2 V			235	
		V_{CC} = 4.5 V			47	
		V_{CC} = 6 V			40	
t_t	To any output	V_{CC} = 2 V			110	ns
		V_{CC} = 4.5 V			22	
		V_{CC} = 6 V			19	

6.12 Typical Characteristic

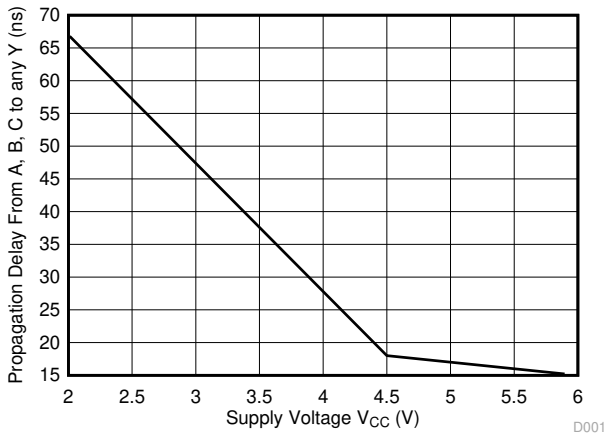
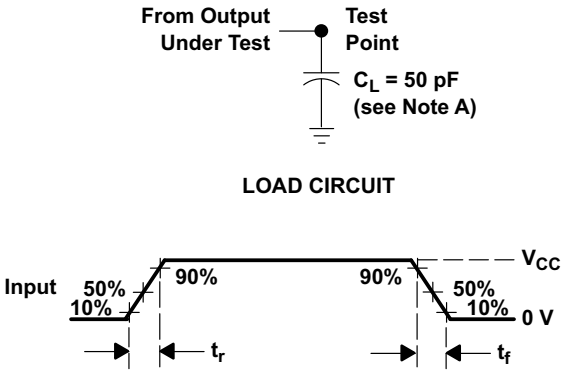


图 6-1. Typical Propagation Delay vs Supply Voltage

7 Parameter Measurement Information



NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

图 7-1. Load Circuit and Voltage Waveforms

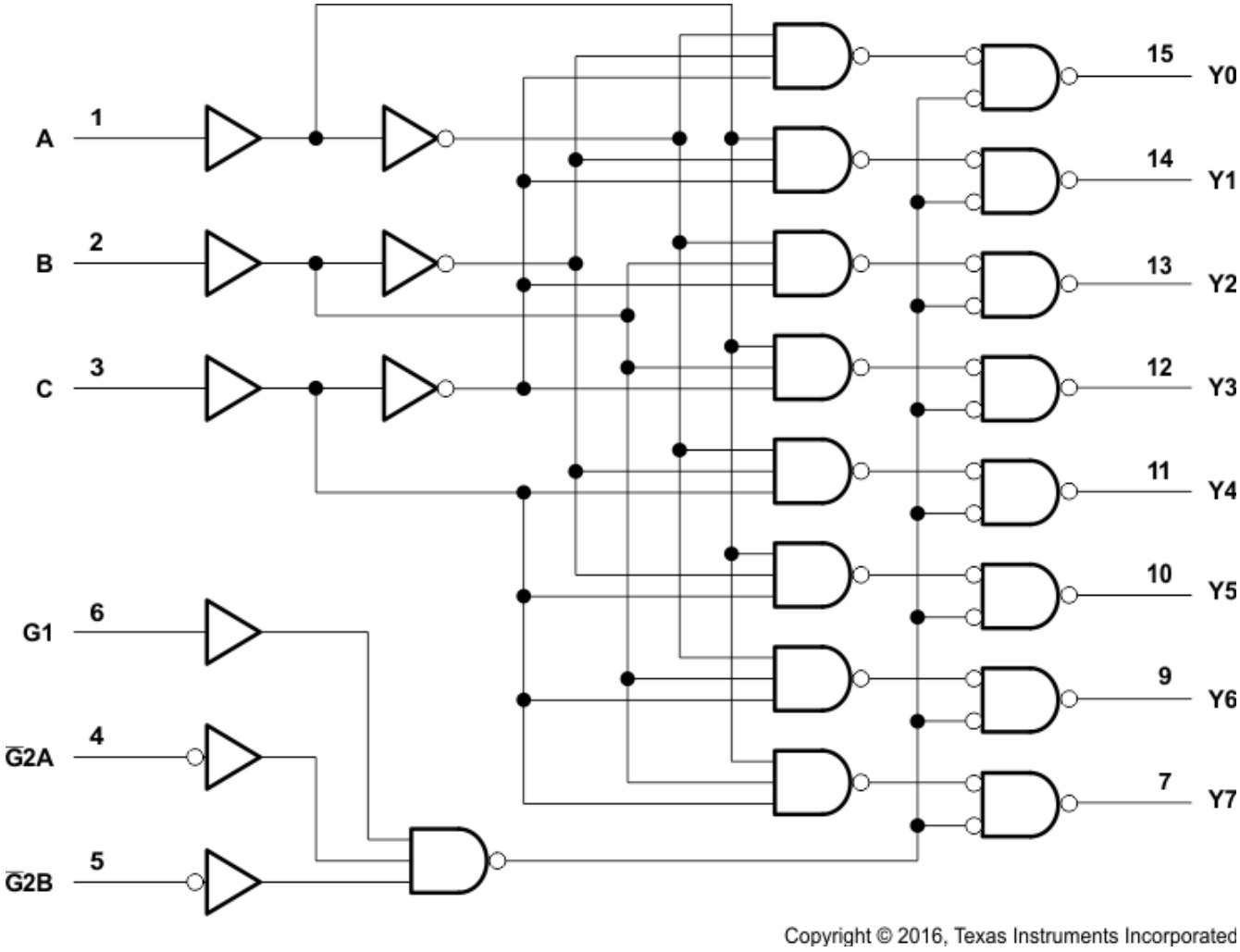
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8 Detailed Description

8.1 Overview

The SNx4HC138 devices are 3-to-8 decoders and demultiplexers. The three input pins, A, B, and C, select which output is active. The selected output is pulled LOW, while the remaining outputs are all HIGH. The conditions at the binary-select inputs at the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the requirement for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

8.2 Functional Block Diagram



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Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

8.3 Feature Description

This device features three binary inputs to select a single active-low output. Three enable pins are also available to enable or disable the outputs. One active high enable and two active low enable pins are available, and any enable pin can be deactivated to force all outputs high. All three enable pins must be active for the output to be enabled.

8.4 Device Functional Modes

表 8-1 lists the functions of the SNx4HC138 devices.

表 8-1. Function Table

INPUTS						OUTPUTS							
ENABLE			SELECT										
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

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9 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The SN74HC138 is useful as a scanning column selector for an LED Matrix display as it can be used for the low side drive of the LED string. The decoder functionality ensures that no more than one output is pulled to a low-level logic voltage so that only a single column is enabled at any point in time.

9.2 Typical Application

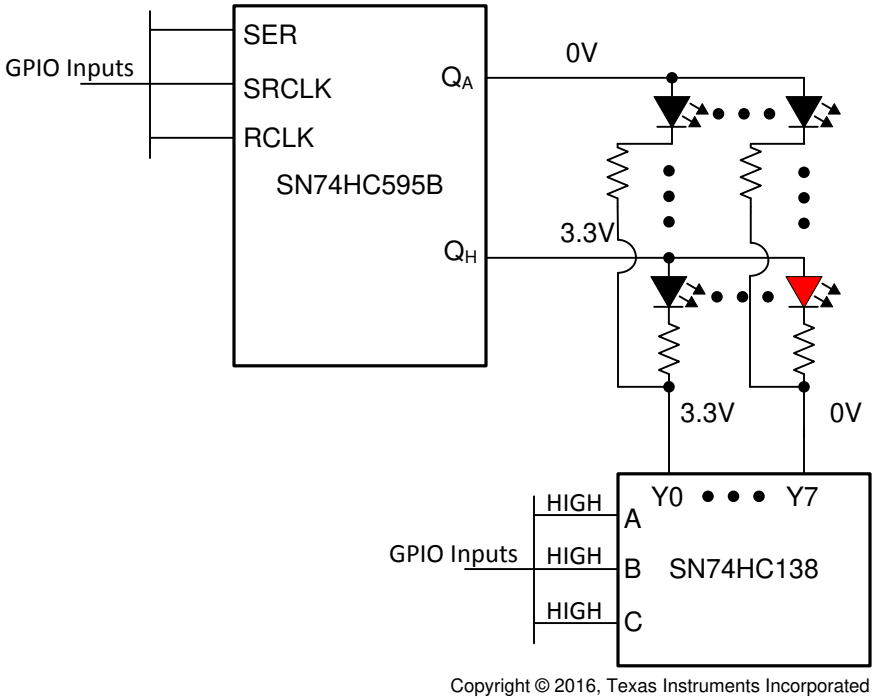


图 9-1. LED Matrix Driver Application

9.2.1 Design Requirements

These devices use CMOS technology and have balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - For switch time specifications, see propagation delay times in 节 6.9.
   - For input voltage level specifications for control inputs, see V_{IH} and V_{IL} in 节 6.6.
2. Recommended Output Conditions
   - Outputs must not be pulled above V_{CC} or below GND.

9.2.3 Application Curve

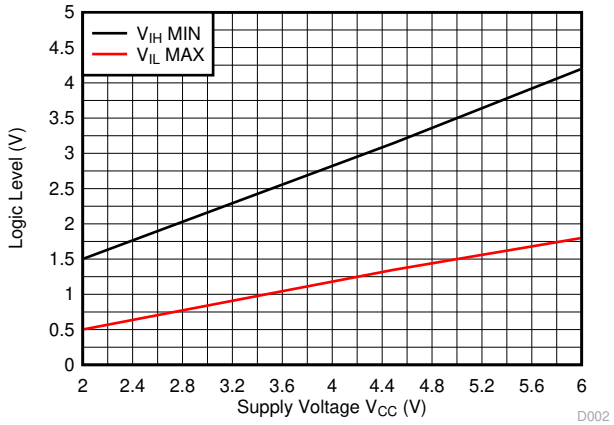


图 9-2. Input High and Input Low Thresholds vs Supply Voltage

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *节 6.3*.

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. A 0.1-μF bypass capacitor is recommended to be placed close to the V_{CC} terminal. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise; 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self‐inductance of the trace (resulting in the reflection). It is a given that not all PCB traces can be straight, and so they have to turn corners. 图 11-1 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

11.2 Layout Example

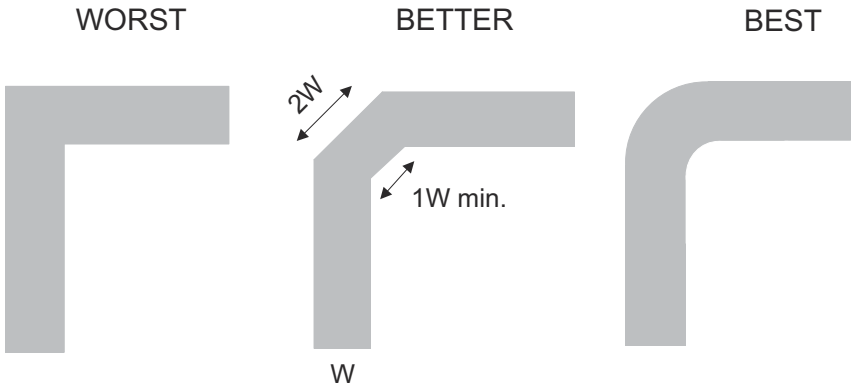


图 11-1. Trace Example

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs (SCBA004)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HC138	Click here	Click here	Click here	Click here	Click here
SN74HC138	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

12.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8406201VEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8406201VE A SNV54HC138J	Samples
5962-8406201VFA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8406201VF A SNV54HC138W	Samples
84062012A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84062012A SNJ54HC 138FK	Samples
8406201EA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8406201EA SNJ54HC138J	Samples
8406201FA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8406201FA SNJ54HC138W	Samples
JM38510/65802B2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65802B2A	Samples
JM38510/65802BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65802BEA	Samples
M38510/65802B2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65802B2A	Samples
M38510/65802BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65802BEA	Samples
SN54HC138J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HC138J	Samples
SN74HC138D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC138	Samples
SN74HC138DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC138	Samples
SN74HC138DE4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC138	Samples
SN74HC138DG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC138	Samples
SN74HC138DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HC138	Samples
SN74HC138DRE4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC138	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC138DRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC138	Samples
SN74HC138DT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC138	Samples
SN74HC138N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU | SN	N / A for Pkg Type	-40 to 85	SN74HC138N	Samples
SN74HC138NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC138N	Samples
SN74HC138NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC138	Samples
SN74HC138PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC138	Samples
SN74HC138PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HC138	Samples
SN74HC138PWRE4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC138	Samples
SN74HC138PWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC138	Samples
SN74HC138PWT	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC138	Samples
SNJ54HC138FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84062012A SNJ54HC 138FK	Samples
SNJ54HC138J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8406201EA SNJ54HC138J	Samples
SNJ54HC138W	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8406201FA SNJ54HC138W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC138, SN54HC138-SP, SN74HC138 :

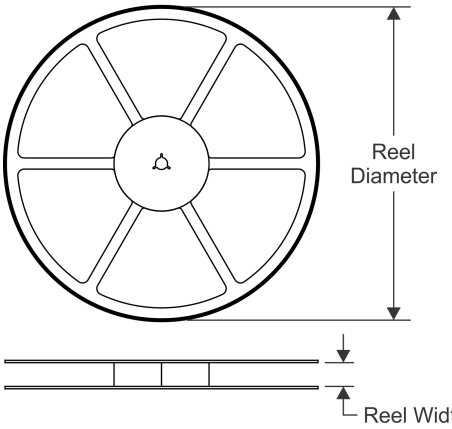
- Catalog : SN74HC138, SN54HC138
- Automotive : SN74HC138-Q1, SN74HC138-Q1
- Military : SN54HC138
- Space : SN54HC138-SP

NOTE: Qualified Version Definitions:

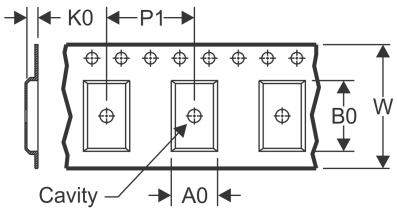
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

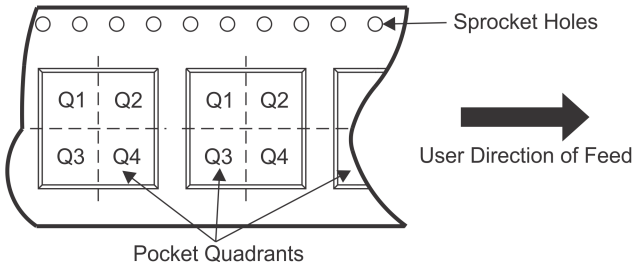


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

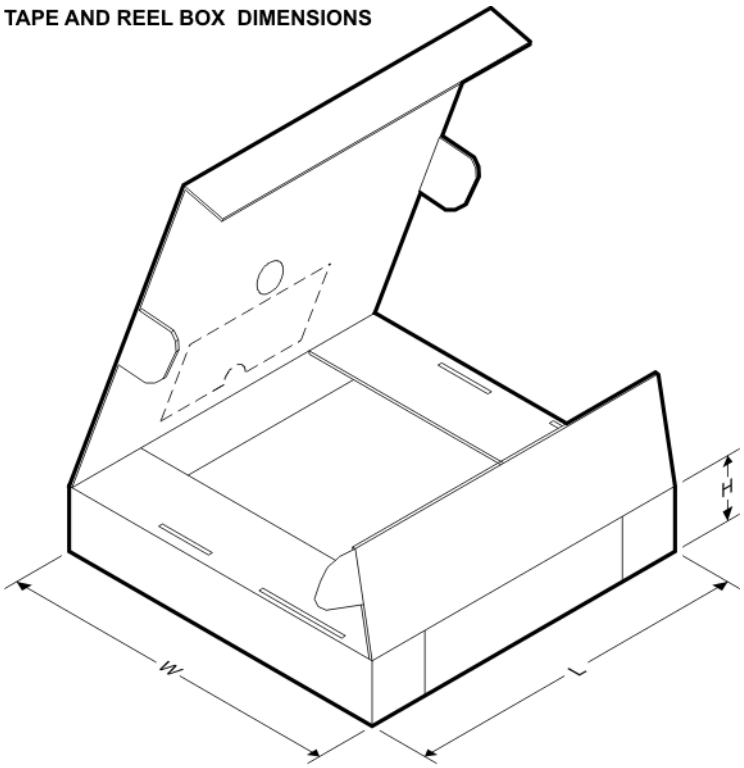
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC138DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74HC138DR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC138DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC138DRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC138NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC138PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC138PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC138PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC138PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

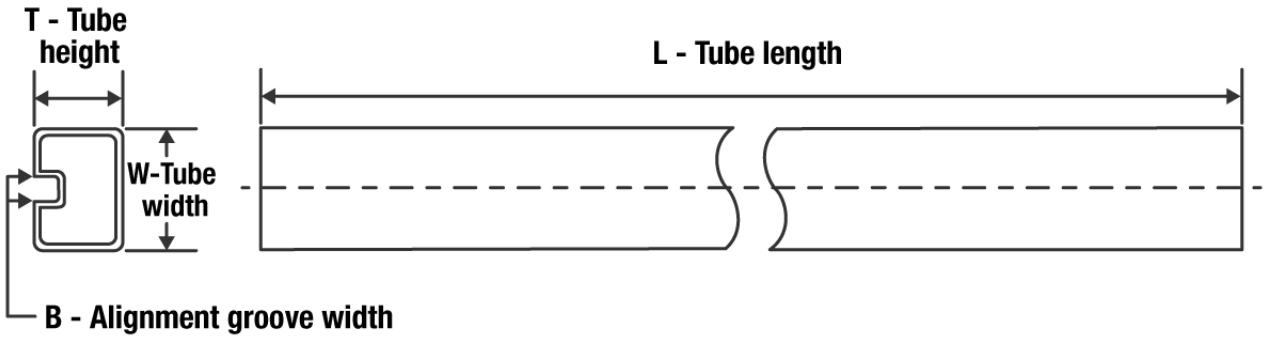
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

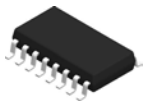
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC138DBR	SSOP	DB	16	2000	853.0	449.0	35.0
SN74HC138DR	SOIC	D	16	2500	364.0	364.0	27.0
SN74HC138DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74HC138DRG4	SOIC	D	16	2500	340.5	336.1	32.0
SN74HC138NSR	SO	NS	16	2000	853.0	449.0	35.0
SN74HC138PWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74HC138PWR	TSSOP	PW	16	2000	853.0	449.0	35.0
SN74HC138PWRG4	TSSOP	PW	16	2000	853.0	449.0	35.0
SN74HC138PWT	TSSOP	PW	16	250	853.0	449.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-8406201VFA	W	CFP	16	1	506.98	26.16	6220	NA
84062012A	FK	LCCC	20	1	506.98	12.06	2030	NA
JM38510/65802B2A	FK	LCCC	20	1	506.98	12.06	2030	NA
M38510/65802B2A	FK	LCCC	20	1	506.98	12.06	2030	NA
SN74HC138D	D	SOIC	16	40	507	8	3940	4.32
SN74HC138DE4	D	SOIC	16	40	507	8	3940	4.32
SN74HC138DG4	D	SOIC	16	40	507	8	3940	4.32
SN74HC138N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC138N	N	PDIP	16	25	506.1	9	600	5.4
SN74HC138N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC138NE4	N	PDIP	16	25	506.1	9	600	5.4
SN74HC138NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC138NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC138PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SNJ54HC138FK	FK	LCCC	20	1	506.98	12.06	2030	NA

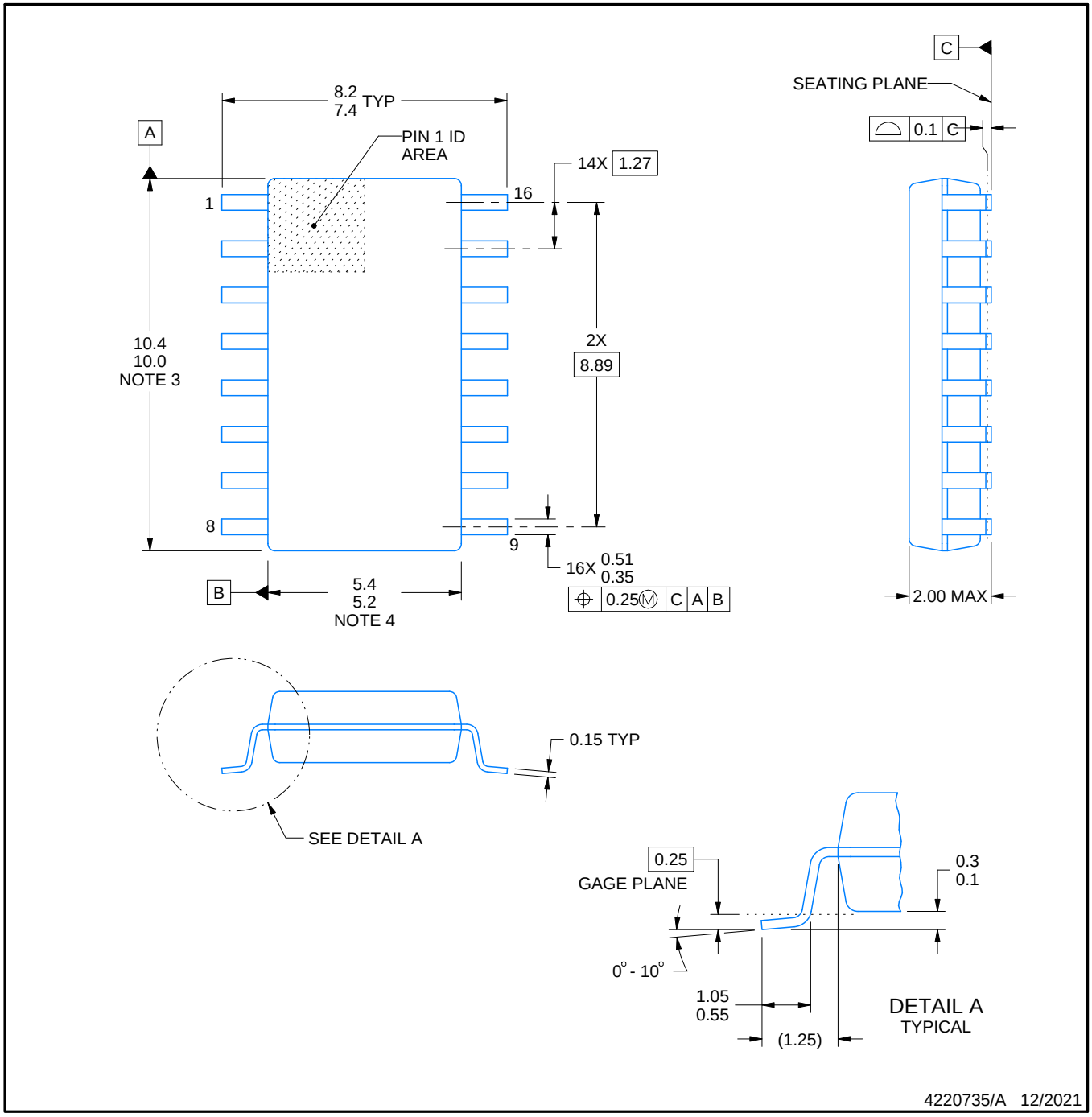


PACKAGE OUTLINE

NS0016A

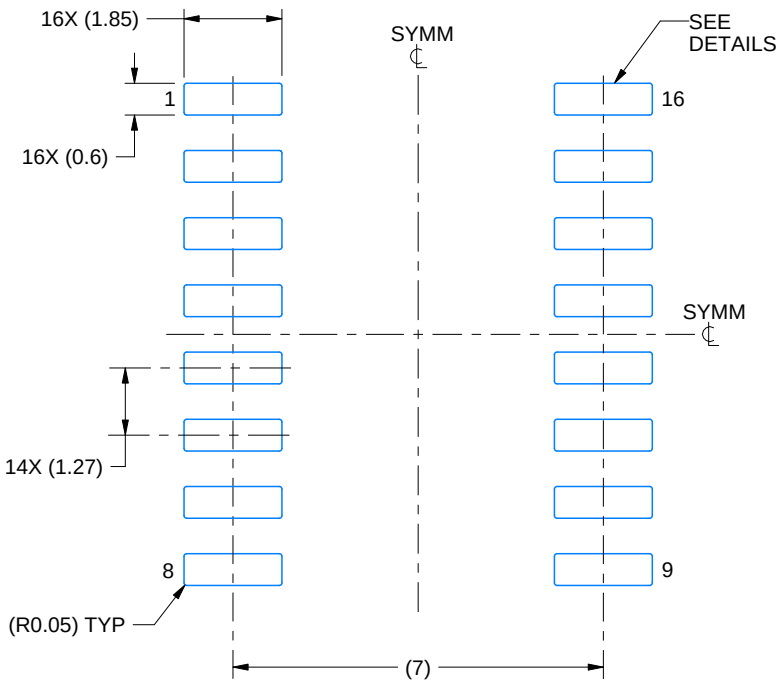
SOP - 2.00 mm max height

SOP

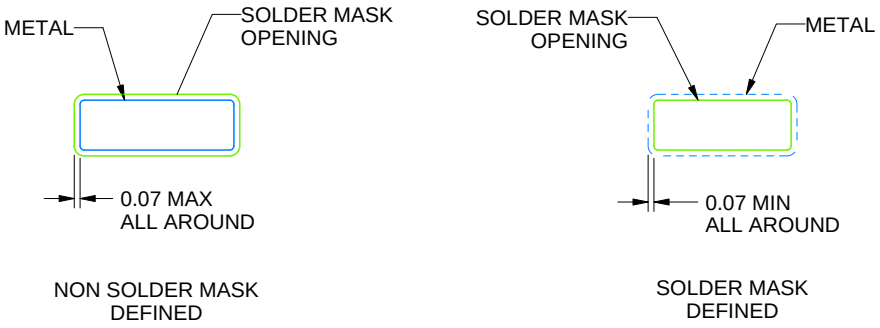


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

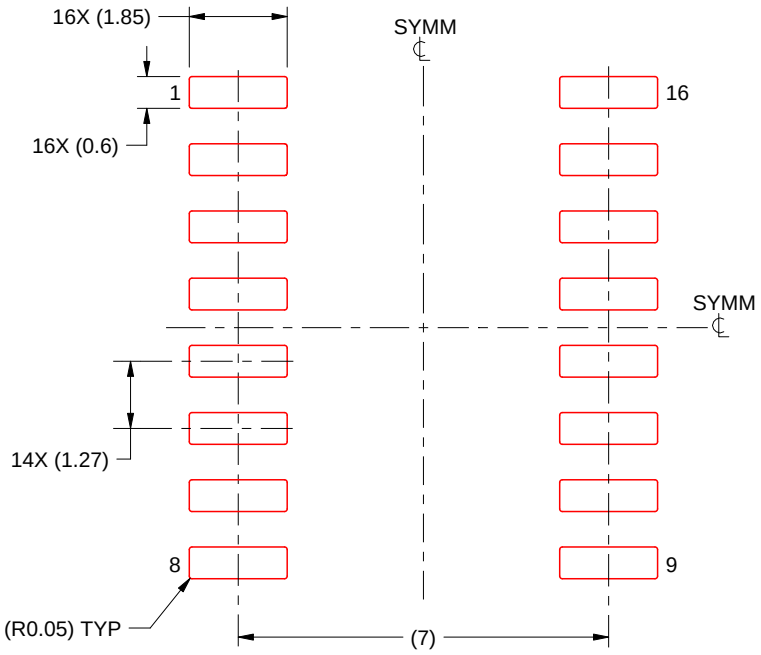
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

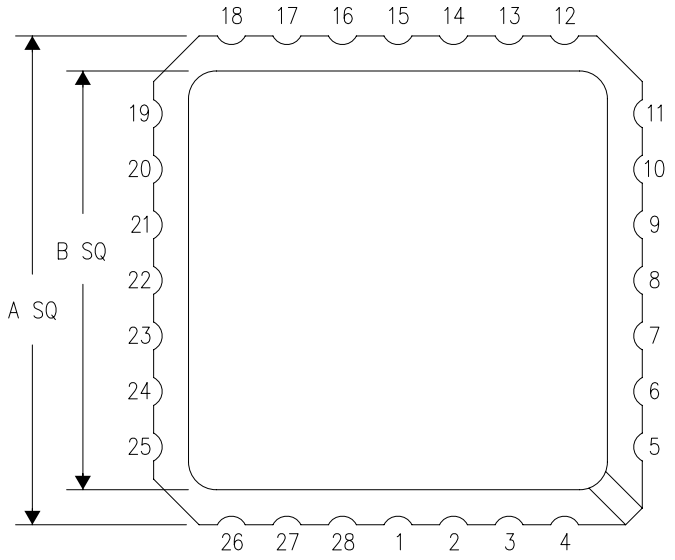
4220735/A 12/2021

NOTES: (continued)

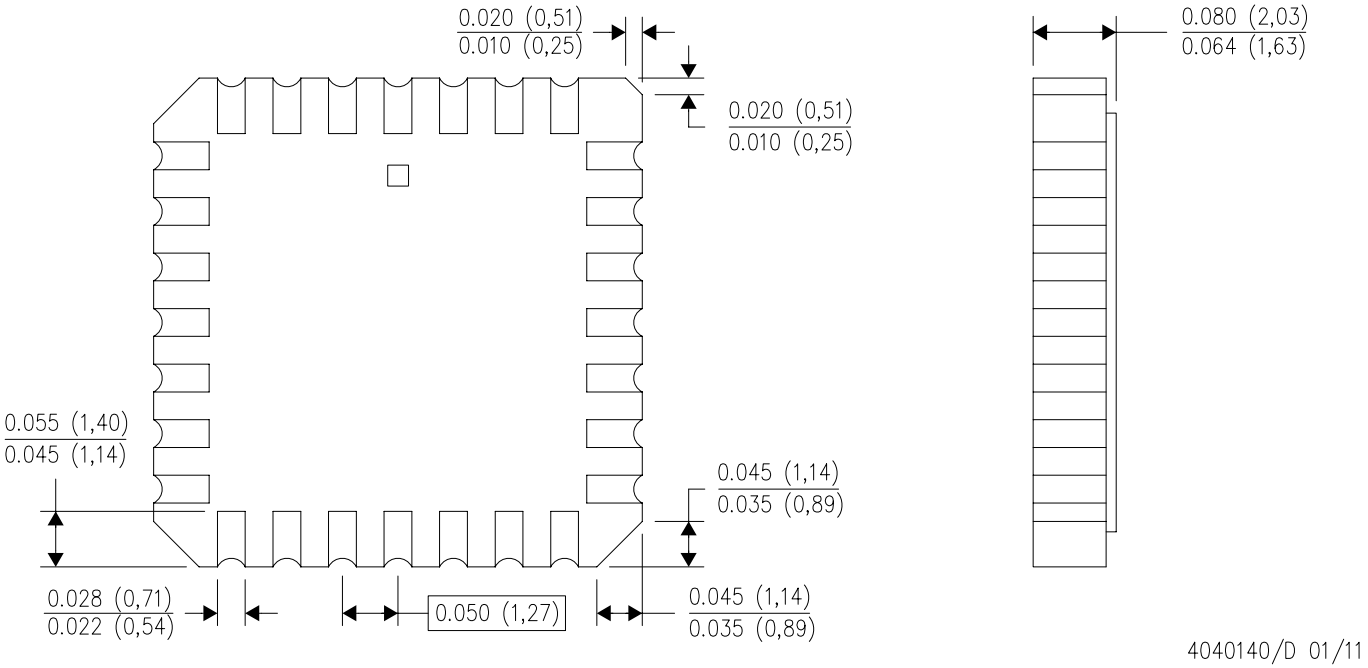
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



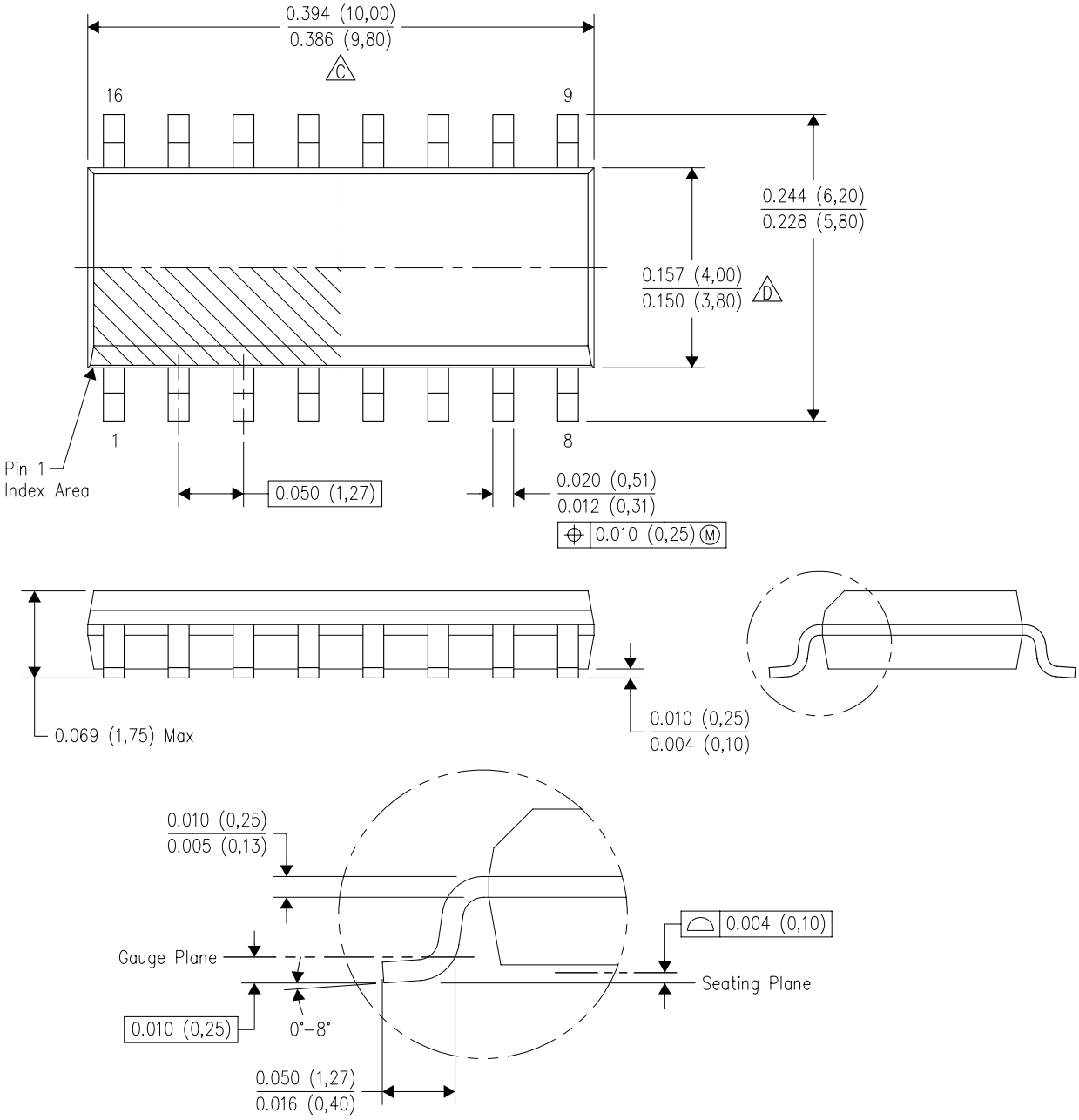
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

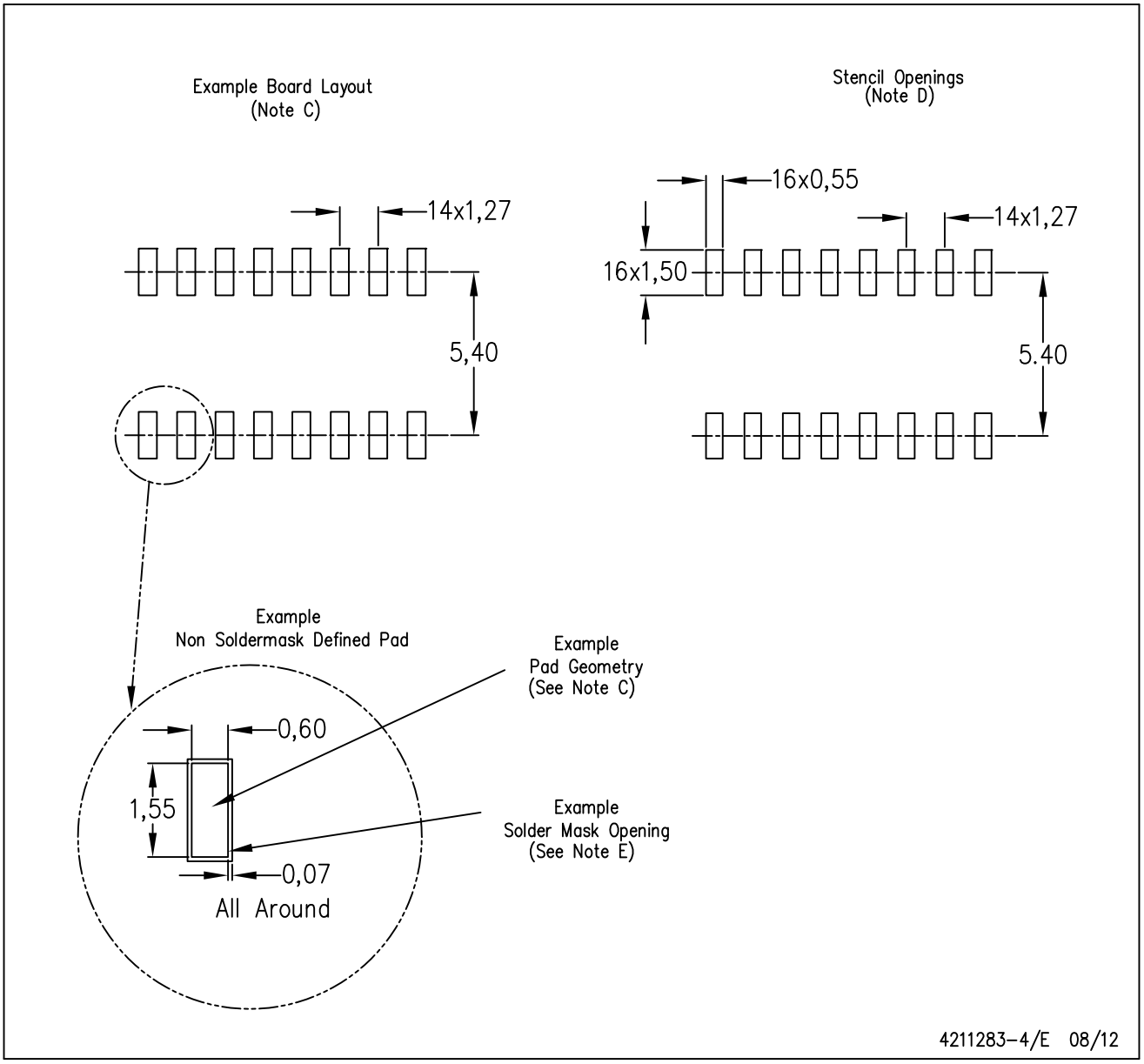
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



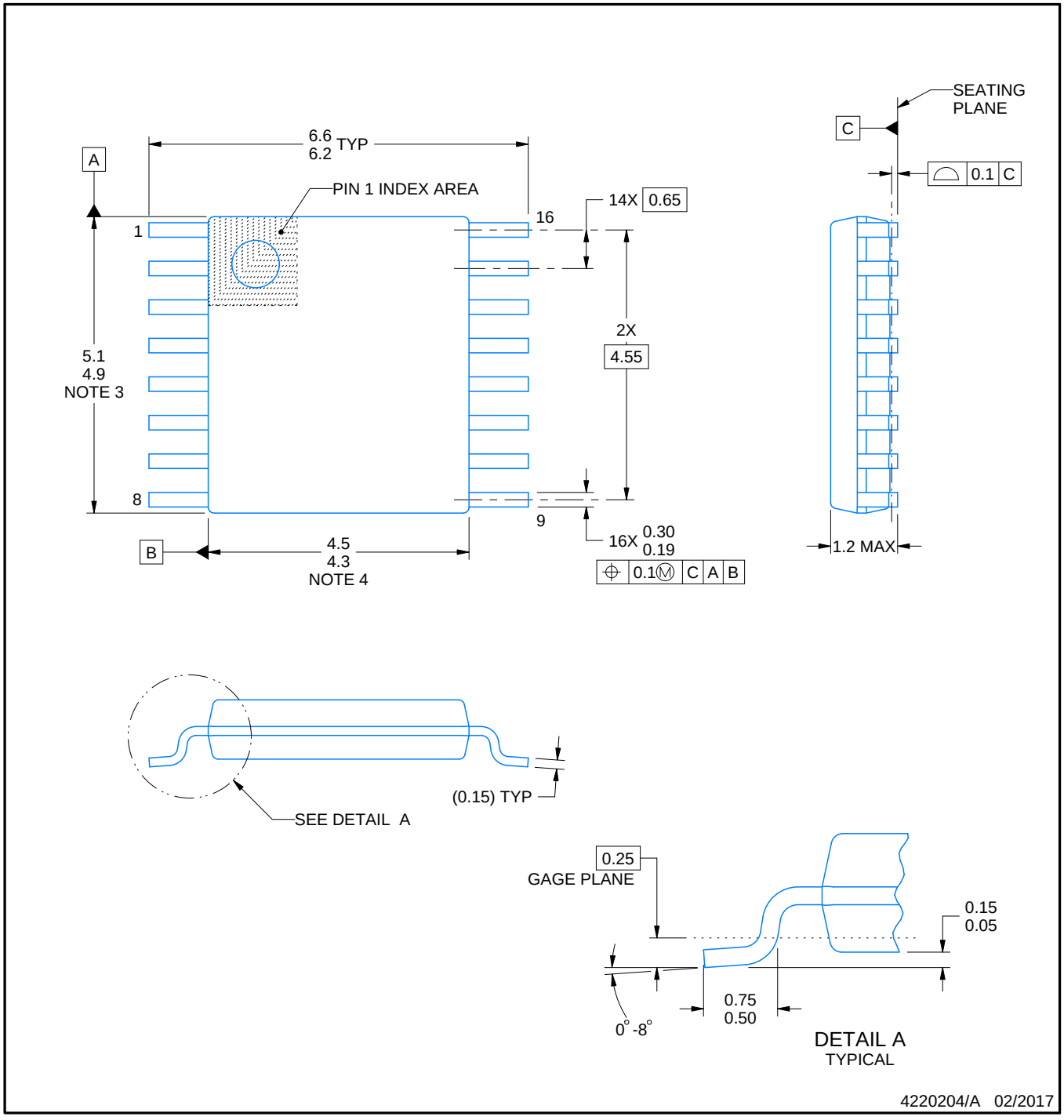
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

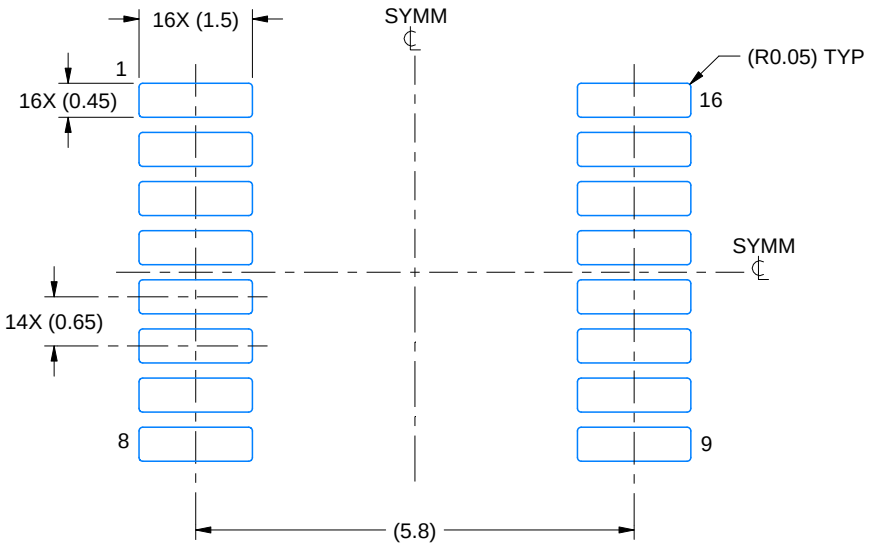
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

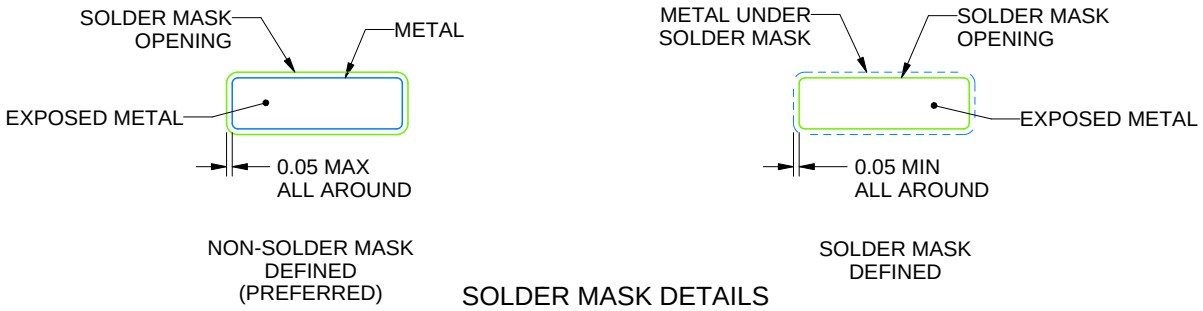


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

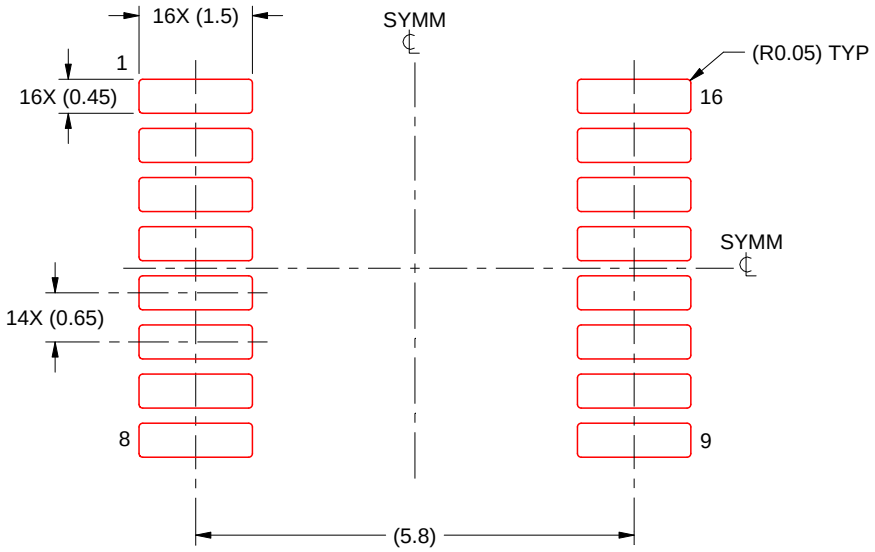


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

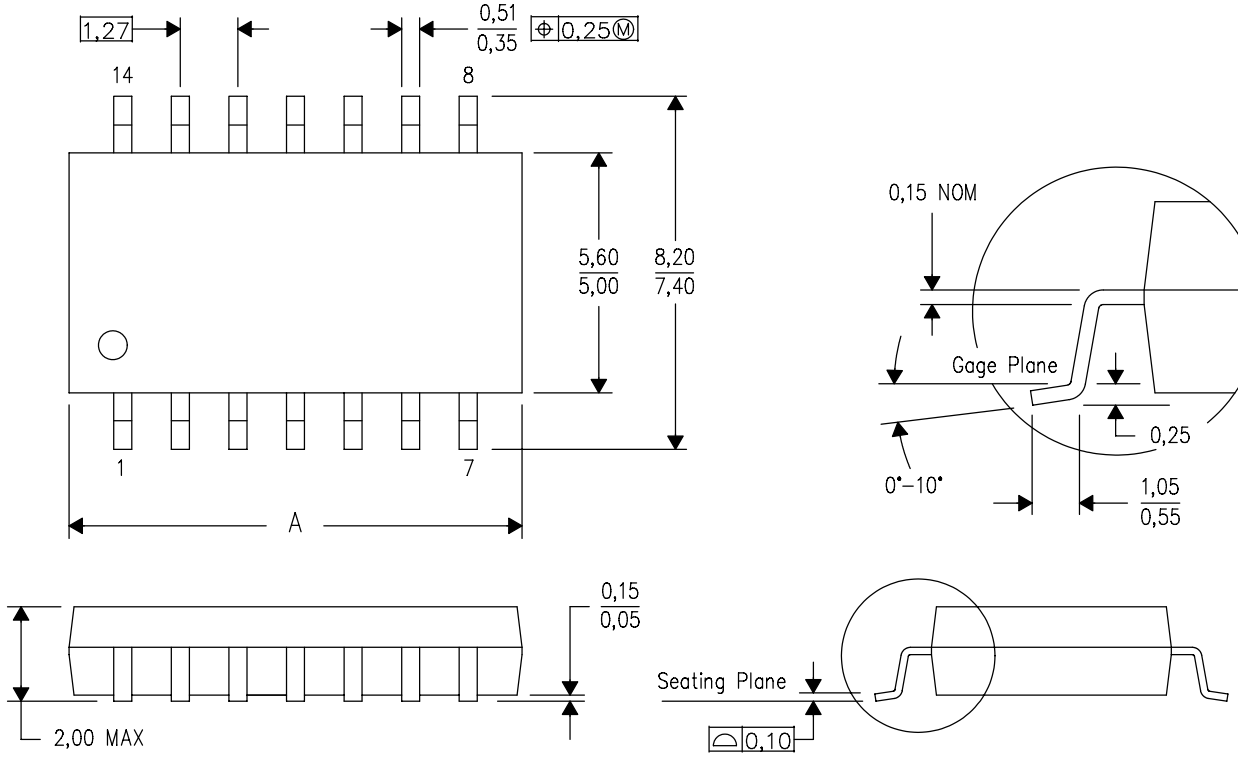
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

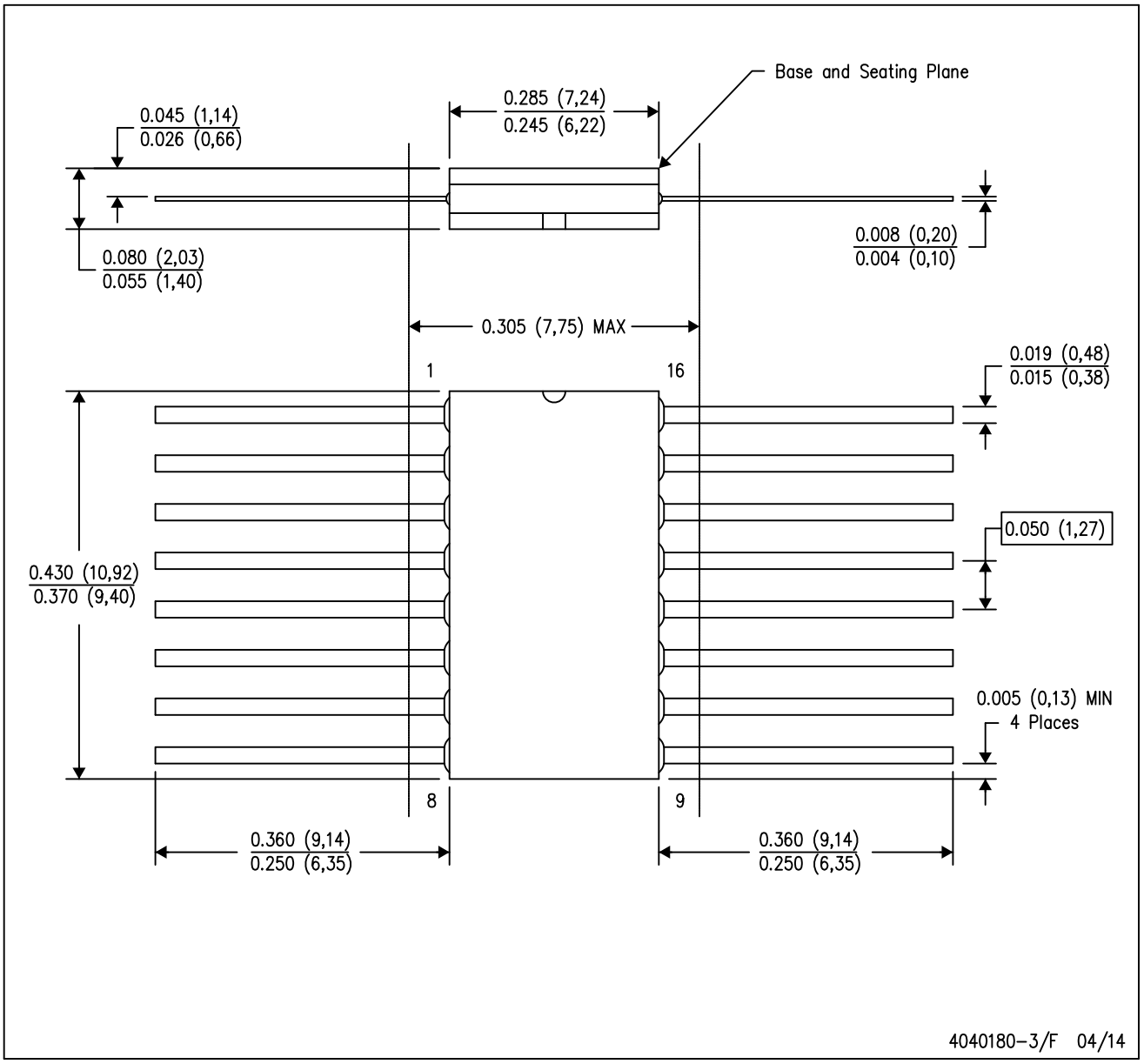


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F16) CERAMIC DUAL FLATPACK

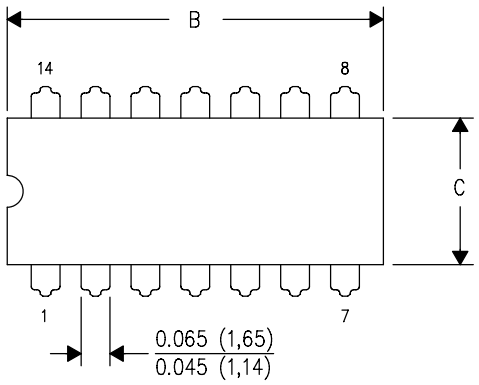


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

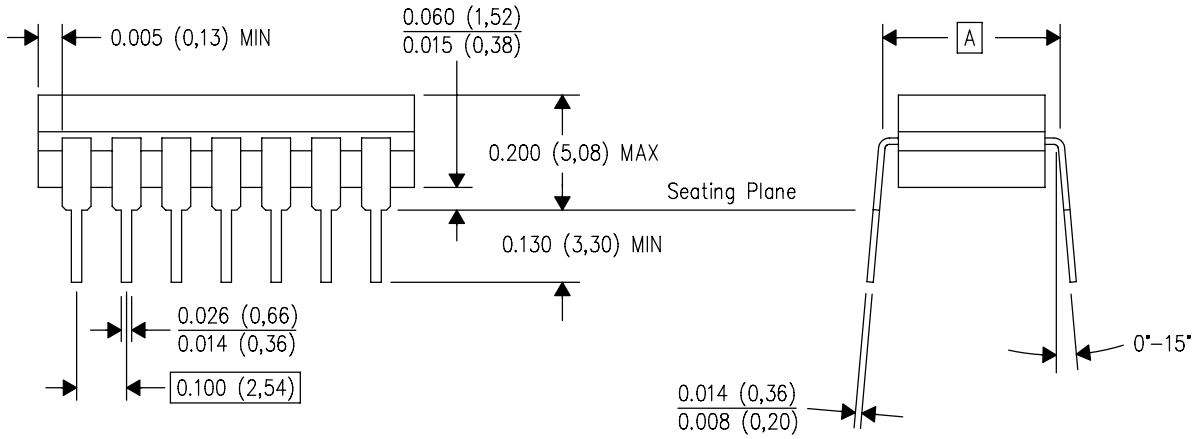
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



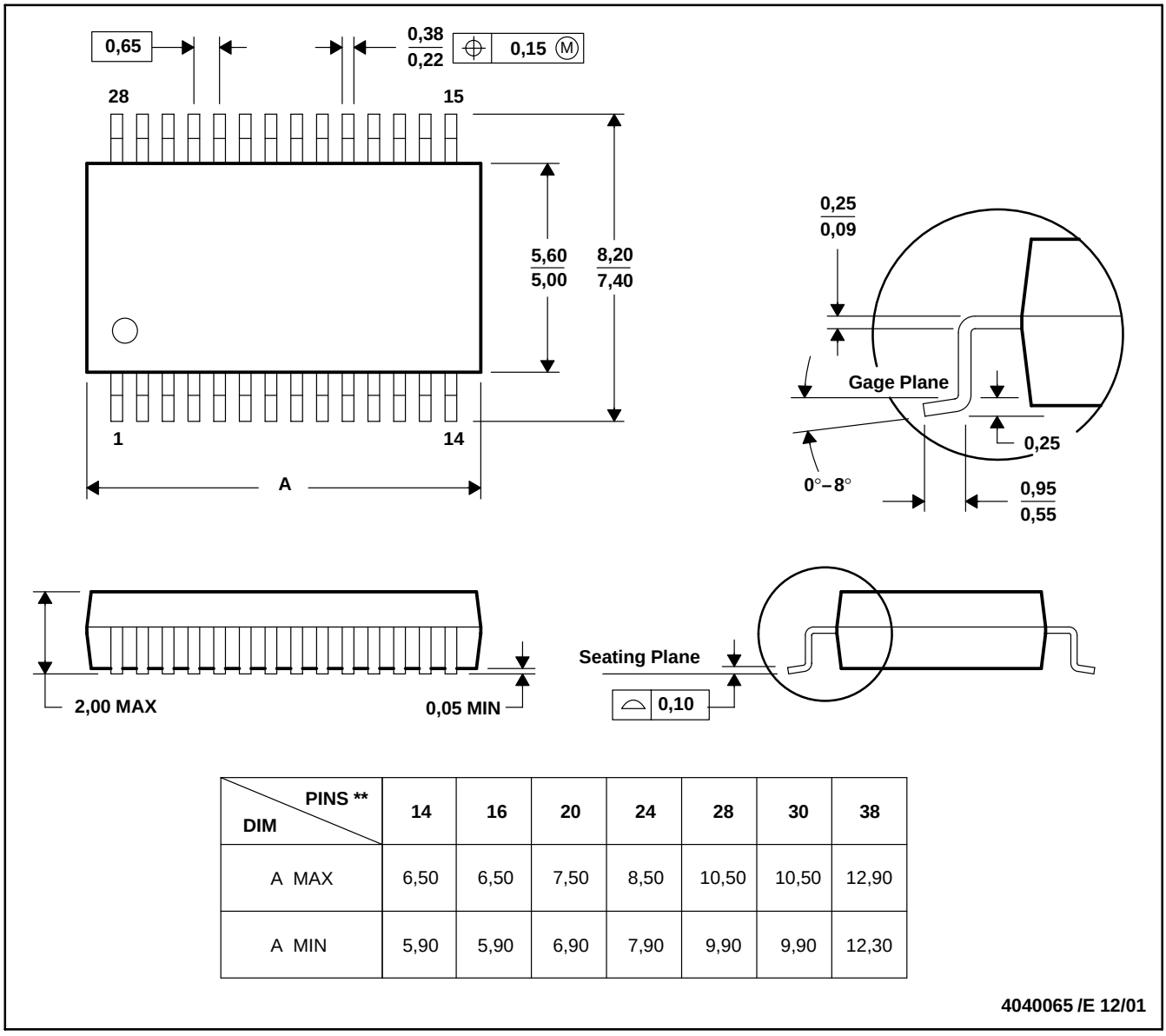
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

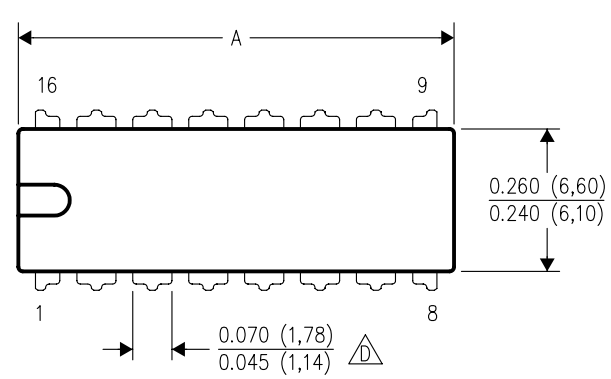
4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

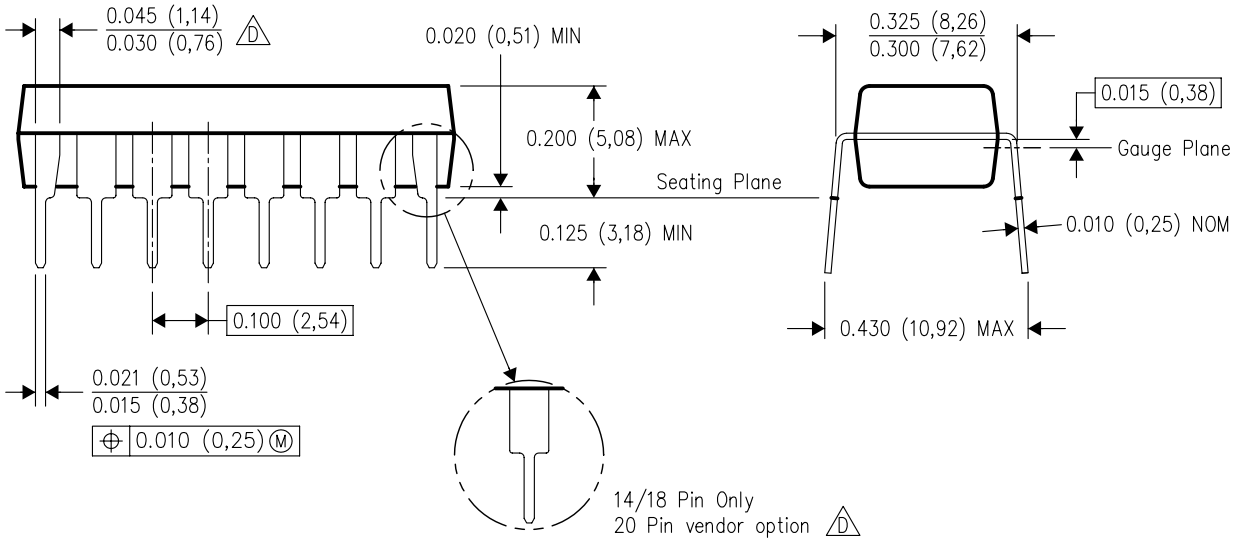
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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