具有可编程延迟和 1% 复位阈值的 LP3470A 超低功耗电压监控器

1 特性

- 与 LP3470 引脚对引脚兼容
- 5 引脚 SOT-23 封装
- 漏极开路复位输出
- 使用外部电容器的可编程复位超时周期
- 不受 VCC 短时瞬变干扰
- ±1% 复位阈值精度（典型值）
- 超低静态电流（0.3µA 典型值）
- 复位有效低至 VCC = 0.95V

2 应用

- 关键 µP 和 µC 电源监视
- 智能仪表
- 计算机
- 便携式和电池供电类设备
- 楼宇自动化：楼宇安全系统、视频监控
- 工厂自动化：现场发送器、位置和接近传感器
- 电机驱动器

3 说明

微功耗电压监控电路 LP3470A 器件设计用于在 1% 的过热复位阈值内监测电压，与 TI 现有的 LP3470 器件引脚对引脚兼容。LP3470A 器件提供精确的毫微功耗电压监控，具有可编程延迟功能。

当 VCC 电源电压低于复位阈值时，LP3470A 将发出复位信号。使用外部电容器可调节复位超时周期。VCC 升至阈值电压以上且加一定迟滞后，在某一间隔（可通过外部电容器编程）复位保持有效。

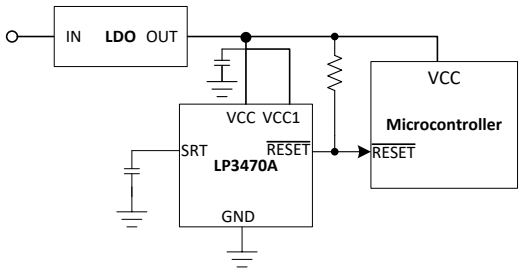
有关可用复位阈值电压选项的信息，请参阅*机械、封装和可订购信息*。

器件信息(1)

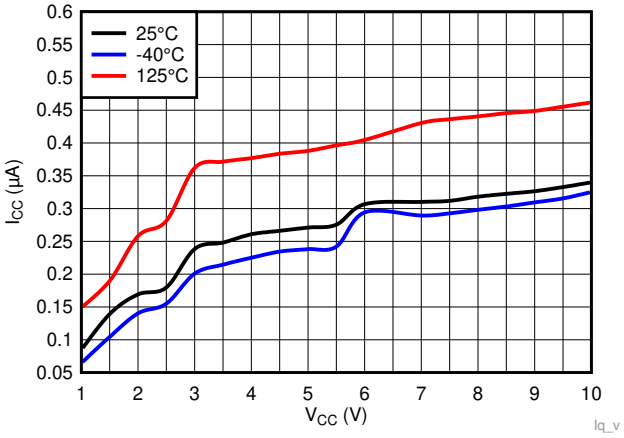
器件型号	封装	封装尺寸（标称值）
LP3470A	SOT-23 (5)	1.60mm × 2.90mm

(1) 要了解所有可用封装，请参阅数据表末尾的“封装选项附录”。

基本工作电路



LP3470A 典型电源电流



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (October 2019) to Revision B — **Page**

- 已更改 将超低静态电流从 0.35 更改为 0.3 以与“电气特性”表保持一致 ... 1
- Changed the typical value of I_{CC} in the Electrical Characteristics table from 300 to 0.3 to match with the units of µA ... 6

Changes from Original (July 2019) to Revision A — **Page**

- 首次公开发布 ... 1

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5 Device Comparison Table

PART NUMBER	V_{IT-} (typ) (VCC RAMPING DOWN)	V_{IT+} (typ) (VCC RAMPING UP)
LP3470A263	2.63 V	2.73 V
LP3470A275	2.75 V	2.85 V
LP3470A293	2.93 V	3.03 V
LP3470A308	3.08 V	3.28 V
LP3470A365	3.65 V	3.85 V
LP3470A400	4.0 V	4.2 V
LP3470A438	4.38 V	4.58 V
LP3470A463	4.63 V	4.83 V

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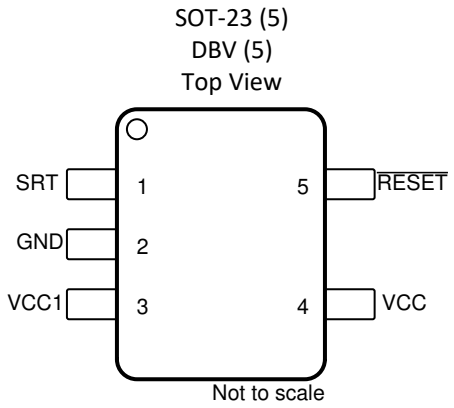
6 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SRT	I	Set reset time-out. Connect a capacitor between this pin and ground to select the reset time-out period (t_D). $t_D = 619 \times C_1$ (C_{SRT} in µF and t_D in ms). If no capacitor is connected, leave this pin floating.
2	GND	—	Ground pin.
3	VCC1	I	Can be connected to VCC or left floating. DO NOT CONNECT TO GND.
4	VCC	I	Supply voltage, and reset threshold monitor input.
5	$\overline{\text{RESET}}$	O	Open-drain, active-low reset output. Connect to an external pullup resistor. $\overline{\text{RESET}}$ changes from high to low whenever the monitored voltage (VCC) drops below the reset threshold voltage (V_{IT-}). Once VCC exceeds the reset threshold (V_{IT-}) + hysteresis (V_{HYS}), $\overline{\text{RESET}}$ remains low for the reset time-out period (t_D) and then deasserts to logic high.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted[(1)]

		MIN	MAX	UNIT
Voltage	VCC	–0.3	12	V
	$\overline{\text{RESET}}$	–0.3	12	
	SRT	–0.3	5.5	
Current	$\overline{\text{RESET}}$		±70	mA
Temperature[(2)]	Operating junction temperature, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	± 2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[(2)]	± 750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Input supply voltage	0.95		10	V
$V_{\overline{RESET}}$, V_{RESET}	$\overline{\text{RESET}}$ pin voltage	0		10	V
$I_{\overline{RESET}}$, I_{RESET}	$\overline{\text{RESET}}$ pin current	0		±5	mA
T_J	Junction temperature (free air temperature)	–40		125	°C

7.4 Thermal Information

THERMAL METRIC[(1)]		LP3470A DBV (SOT23-5) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	109.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	92.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	35.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	92.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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7.5 Electrical Characteristics

At 0.95 V ≤ V_{CC} ≤ 10 V, SRT = Open, $\overline{RESET}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to VCC, output reset load (C_{LOAD}) = 10 pF and over the operating free-air temperature range – 40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Input supply voltage		0.95		10	V
V_{IT-}	Negative-going input threshold accuracy	-40°C to 125°C	–1.5	1	1.5	%
V_{HYS}	Hysteresis on V_{IT-} pin	V_{IT-} = 3.08 V to 4.63 V	175	200	225	mV
V_{HYS}	Hysteresis on V_{IT-} pin	V_{IT-} = 2.64 V to 2.93 V	75	100	125	mV
I_{CC}	Supply current into VCC pin	VCC = 0.95 V < V_{CC} < 10 V VCC > V_{IT+} (1) T_A = -40°C to 125°C		0.3	1	µA
R_{SRT}	SRT pin internal resistance (2)		350	500	650	kΩ
V_{POR}	Power on Reset Voltage (3)	$V_{OL(max)}$ = 0.2 V $I_{OUT\ (Sink)}$ = 5.6 uA			950	mV
V_{OL}	Low level output voltage	1.5 V < V_{CC} < 5 V V_{CC} < V_{IT-} $I_{OUT(Sink)}$ = 2 mA			200	mV
$I_{lkg(OD)}$	Open-Drain output leakage current	$\overline{RESET}$ pin in High Impedance, V_{CC} = V_{RESET} = 5.5 V V_{IT+} < V_{CC}			90	nA

(1) V_{IT+} = V_{HYS} + V_{IT-}
(2) This parameter is guranteed by design and characterization
(3) V_{POR} is the minimum V_{DD} voltage level for a controlled output state. V_{DD} slew rate ≤ 100mV/µs

7.6 Timing Requirements

At 0.95 V ≤ V_{CC} ≤ 10 V, SRT = Open, $\overline{RESET}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to VCC, output reset load (C_{LOAD}) = 10 pF and over the operating free-air temperature range – 40°C to 125°C, VCC slew rate < 100mV / us, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{P_HL}	Propagation detect delay for VCC falling below V_{IT-}	V_{CC} = V_{IT+} to (V_{IT-}) - 10% (1)		15	30	µs
t_D	Reset time delay	SRT pin = open V_{CC} = (V_{IT-} -1V) to (V_{IT+} + 1V)			50	µs
		SRT pin = 10 nF (2)(3)		6.2		ms
		SRT pin = 1 µF (2)(3)		619		ms
t_{GI_VIT-}	Glitch immunity V_{IT-}	5% V_{IT-} overdrive (3)(4)		10		µs

(1) t_{P_HL} measured from threhold trip point (V_{IT-}) to V_{OL}
(2) Ideal capacitor
(3) Parameter is guranteed by design.
(4) Overdrive % = [(V_{CC}/ V_{IT-}) - 1] × 100%

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7.7 Typical Characteristics

Typical characteristics show the typical performance of the LP3470A device. Test conditions are at $T_A = T_J = 25°C$ (unless otherwise noted).

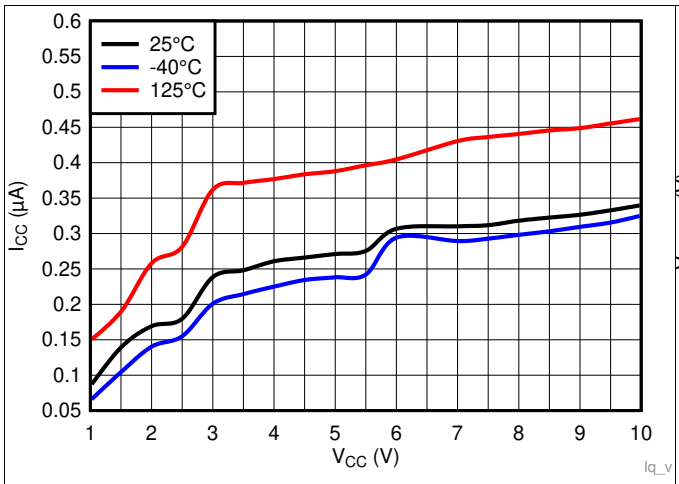

图 1. Supply Current vs Supply Voltage

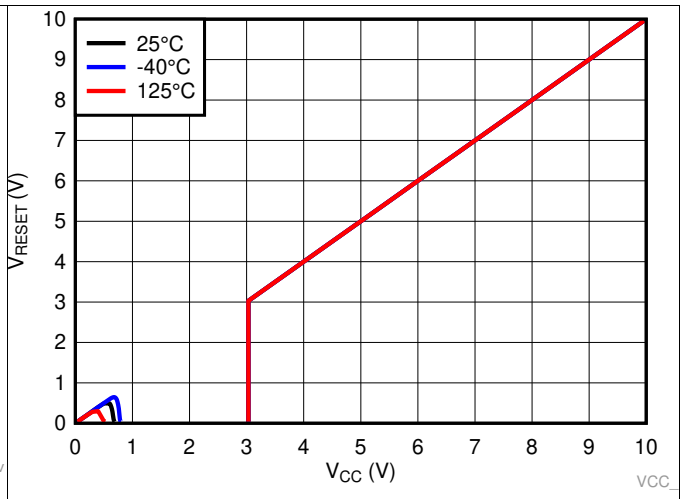

图 2. Output Voltage vs Supply Voltage for LP3470A293

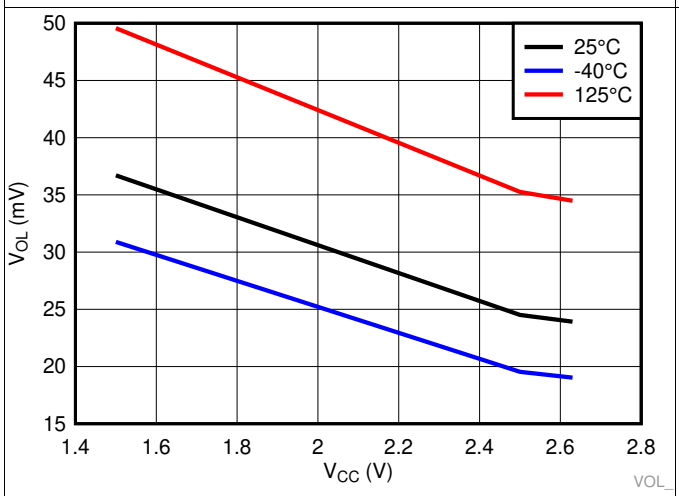

图 3. Low Level Output Voltage vs Supply Voltage

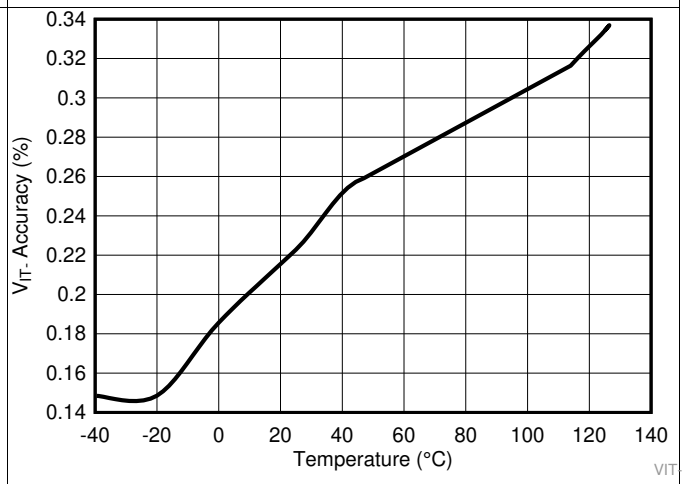

图 4. Negative-going Input Threshold V_{IT-} Accuracy vs Temperature

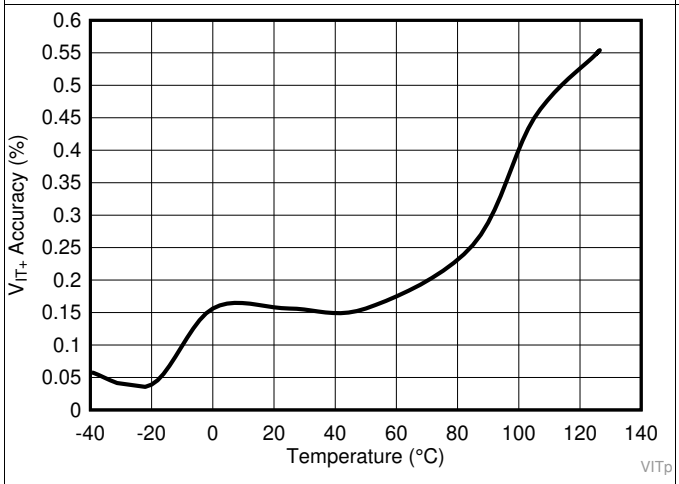

图 5. Positive-going Input Threshold V_{IT+} Accuracy vs Temperature

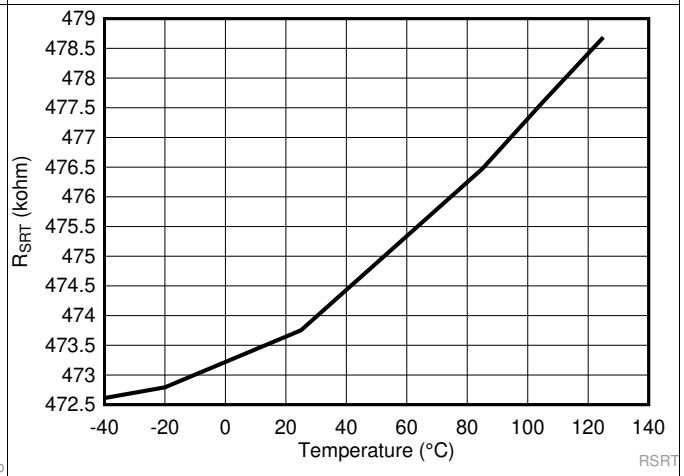

图 6. SRT Pin Internal Resistance Overtemperature

Typical Characteristics（接下页）

Typical characteristics show the typical performance of the LP3470A device. Test conditions are at $T_A = T_J = 25°C$ (unless otherwise noted).

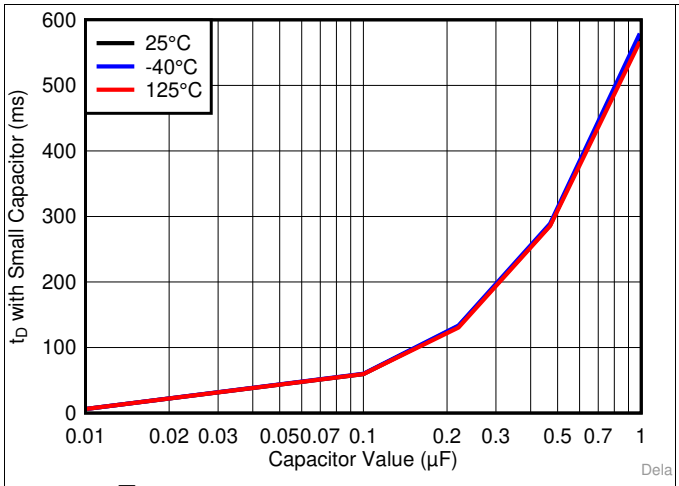

图 7. Reset Time Delay vs Small Capacitor Values

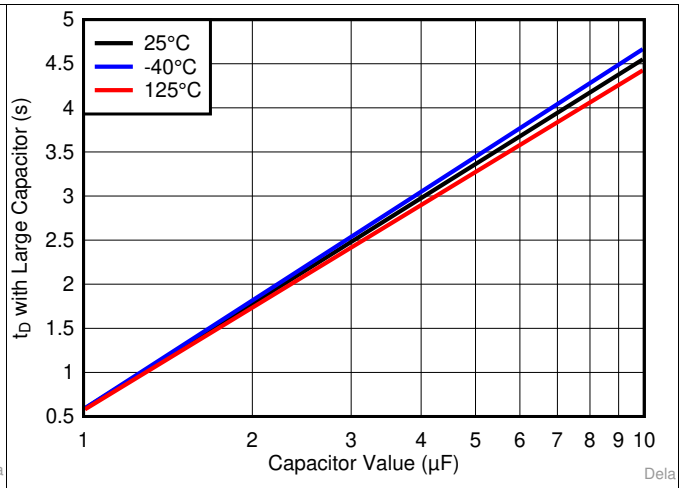

图 8. Reset Time Delay vs Large Capacitor Values

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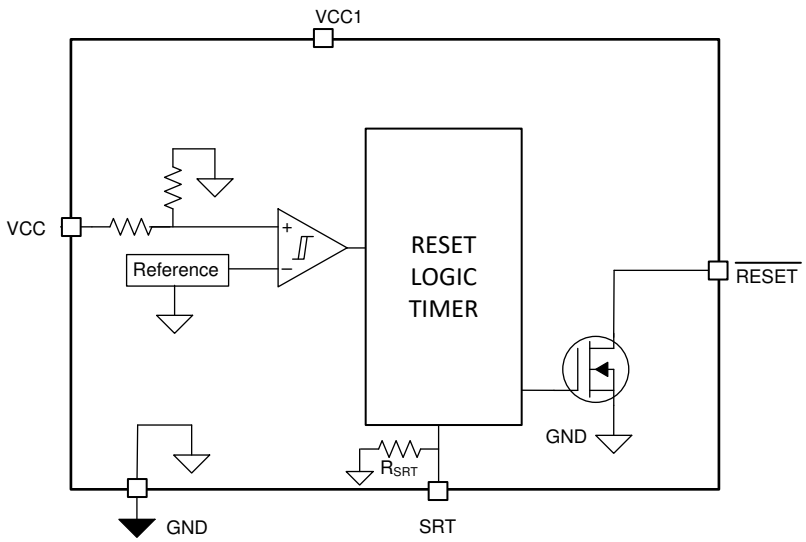
8 Detailed Description

8.1 Overview

The LP3470A micropower voltage supervisory circuit provides a simple solution to monitor the power supplies in microprocessor and digital systems and provides a reset controlled by the factory-programmed reset threshold on the VCC supply voltage pin. When the voltage declines below the reset threshold, the reset signal is asserted and remains asserted for an interval programmed by an external capacitor after VCC has risen above the threshold voltage. The reset threshold options are 2.63 V, 2.75 V, 2.93 V, 3.08 V, 3.65 V, 4 V, 4.38 V, 4.63 V.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 $\overline{\text{RESET}}$ Time-Out Period

The reset time delay can be set to a minimum value of 50 µs by leaving the SRT pin floating, or a maximum value of approximately 6.2 seconds by connecting 10 µF delay capacitor. The reset time delay (t_D) can be programmed by connecting a capacitor no larger than 10 µF between SRT pin and GND.

The relationship between external capacitor (C_{SRT}) in Farads at SRT pin and the time delay (t_D) in seconds is given by 公式 1.

$$t_D = -\ln(0.29) \times R_{SRT} \times C_{SRT} + t_D \text{ (no cap)} \quad (1)$$

公式 1 is simplified to 公式 2 by plugging R_{SRT} and $t_{D(no\ cap)}$ given in *Electrical Characteristics* section:

$$t_D = 618937 \times C_{SRT} + 50\ \mu s \quad (2)$$

公式 3 solves for external capacitor value (C_{SRT}) in units of Farads where t_D is in units of seconds

$$C_{SRT} = (t_D - 50\ \mu s) \div 618937 \quad (3)$$

The reset delay varies according to three variables: the external capacitor variance (C_{SRT}), SRT pin internal resistance (R_{SRT}) provided in the Electrical Characteristics table, and a constant. The minimum and maximum variance due to the constant is shown in Equation 5 and Equation 6.

$$t_{D\ (minimum)} = -\ln(0.36) \times R_{SRT\ (min)} \times C_{SRT\ (min)} + t_{D\ (no\ cap,\ min)} \quad (4)$$

$$t_{D\ (maximum)} = -\ln(0.26) \times R_{SRT\ (max)} \times C_{SRT\ (max)} + t_{D\ (no\ cap,\ max)} \quad (5)$$

Feature Description (接下页)

The recommended maximum delay capacitor for the LP3470A is limited to 10 µF as this ensures there is enough time for the capacitor to fully discharge when the reset condition occurs. When a voltage fault occurs, the previously charged up capacitor discharges, and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the delay capacitor will begin charging from a voltage above zero and the reset delay will be shorter than expected. Larger delay capacitors can be used so long as the capacitor has enough time to fully discharge during the duration of the voltage fault.

8.3.2 $\overline{\text{RESET}}$ Output

In applications like microprocessor (µP) systems, errors might occur in system operation during power up, power down, or brownout conditions. It is imperative to monitor the power supply voltage to prevent these errors from occurring.

The LP3470A asserts a reset signal whenever the VCC supply voltage is below a threshold (V_{IT-}) voltage. $\overline{\text{RESET}}$ is ensured to be a logic low for VCC > 0.95 V. Once VCC exceeds the reset threshold plus a hysteresis voltage, the reset is kept asserted for a time period (t_D) programmed by an external capacitor (C_{SRT}); after this interval $\overline{\text{RESET}}$ goes to logic high. If a brownout condition occurs (monitored voltage falls below the reset threshold), $\overline{\text{RESET}}$ goes low. When VCC returns above the reset threshold plus a hysteresis voltage, $\overline{\text{RESET}}$ remains low for a time period t_D before going to logic high. 图 9 shows this behavior.

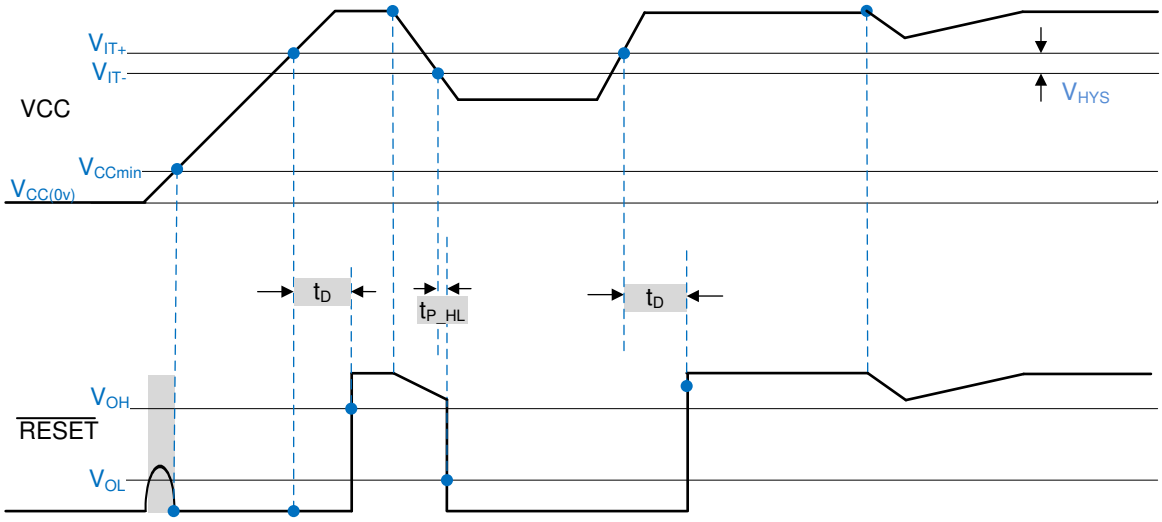


图 9. $\overline{\text{RESET}}$ Output Timing Diagram

8.3.3 Pull-up Resistor Selection

The $\overline{\text{RESET}}$ output structure of the LP3470A is an open-drain N-channel MOSFET switch. A pull-up resistor ($R_{pull-up}$) must be connected to VCC to keep the output logic high when $\overline{\text{RESET}}$ is not asserted.

Connect the pull-up resistor to the desired pull-up voltage source and $\overline{\text{RESET}}$ can be pulled up to any voltage up to 10 V independent of the VCC voltage. To ensure proper voltage levels, give some consideration when choosing the pull-up resistor values. $R_{pull-up}$ must be large enough to limit the current through the output within the recommended operating conditions. The pull-up resistor value determines the actual VOL, the output capacitive loading, and the output leakage current ($I_{LKG(OD)}$). A typical pull-up resistor value of 20 kΩ is sufficient in most applications.

8.3.4 VCC Transient Immunity

The LP3470A is immune to quick voltage transients or excursions on VCC. Sensitivity to transients depends on both pulse duration and overdrive. Overdrive is defined by how much VCC deviates from the specified threshold. Threshold overdrive is calculated as a percent of the threshold in question, as shown in 公式 6. A 0.1-µF bypass capacitor mounted close to VCC provides additional transient immunity.

$$\text{Overdrive} = |\,(V_{CC} / V_{IT-} - 1) \times 100\%\,| \quad (6)$$

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Feature Description (接下页)

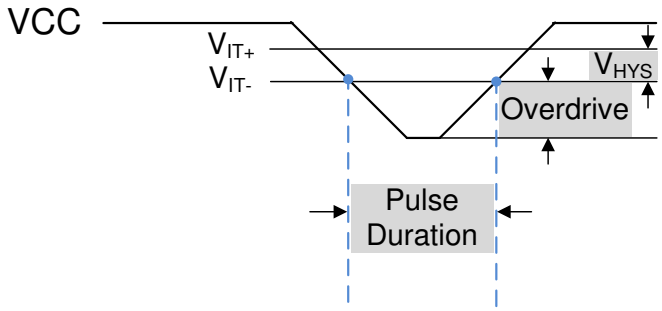

图 10. Overdrive vs Pulse Duration

8.4 Device Functional Modes

8.4.1 $\overline{\text{RESET}}$ Output Low

When the VCC supply voltage is below the reset threshold (V_{IT-}), the $\overline{\text{RESET}}$ pin will output logic low. $\overline{\text{RESET}}$ is ensured to be a logic low for VCC > 0.95 V.

8.4.2 $\overline{\text{RESET}}$ Output High

When the VCC supply voltage exceeds the reset threshold (V_{IT-}) plus the hysteresis voltage (V_{HYS}), the $\overline{\text{RESET}}$ remains asserted for a time period (t_D) programmed by an external capacitor (C_{SRT}); after this interval $\overline{\text{RESET}}$ goes to logic high.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LP3470A is a micropower CMOS voltage supervisor that is ideal for use in battery-powered microprocessor and other digital systems. It is small in size and provides voltage monitoring and supervisory functions with nano-Iq and programmable delay, making it a good solution in a variety of applications. The LP3470A is available in six standard reset threshold voltage options, and the reset time-out period is adjustable using an external capacitor providing maximum flexibility in any application. This device can ensure system reliability and ensures that a connected microprocessor will operate only when a minimum voltage supply is satisfied.

9.2 Typical Application

The LP3470A can be used as a simple supervisor circuit to monitor the input supply to a microprocessor as shown in 图 11.

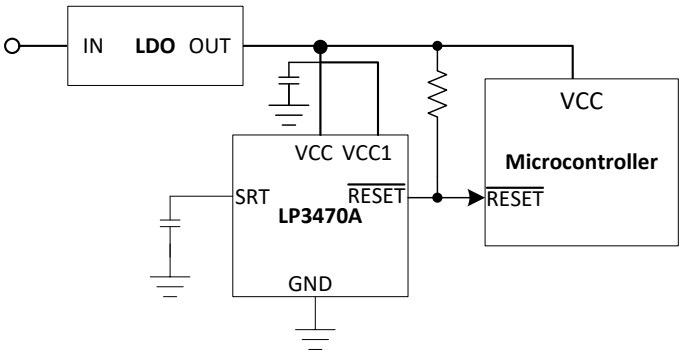

图 11. Power-On Reset Circuit

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 1 as the input parameters.

表 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input supply voltage	0.95 to 10 V
Reset threshold voltage	2.63 V, 2.75 V, 2.93 V, 3.08 V, 3.65 V, 4 V, 4.38 V, 4.63 V
External pullup resistor	0.68 to 68 kΩ
External reset time-out period capacitor	C_{SRT} = 1 nF
Reset time-out period	619 µs

9.2.2 Detailed Design Procedure

The minimum application circuit requires the LP3470A Power-On Reset Circuit IC and a pullup resistor connecting the reset pin to VCC. The reset delay can be programmed with an additional capacitor connected from the SRT pin to GND. See *RESET Time-Out Period* and *Pull-up Resistor Selection* for information on choosing specific values for components.

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9.2.3 Application Curves

Two capacitor values for C_{SRT} (0.1 µF and 1 µF) are used as examples to show the programmability of the output time delay as shown in 图 12 and 图 13.

图 12. Reset Delay Time with 0.1-µF Capacitor at SRT

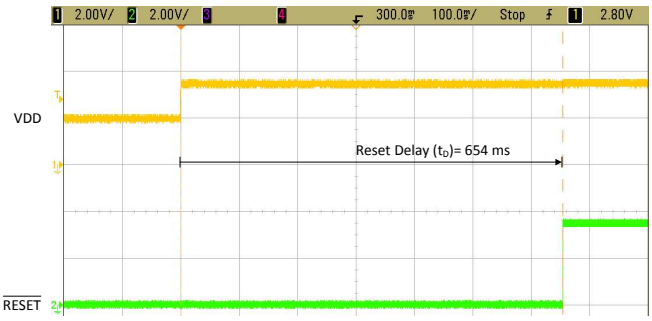

图 13. Reset Delay Time with 1-µF Capacitor at SRT

10 Power Supply Recommendations

The input of the LP3470A is designed to handle up to the supply voltage absolute maximum rating of 12 V. If the input supply is susceptible to any large transients above the maximum rating, then take extra precautions. An input capacitor is optional but not required to help avoid false reset output triggers due to noise.

11 Layout

11.1 Layout Guidelines

- Good analog design practice recommends placing a minimum of 0.1-µF ceramic capacitor as near as possible to the VCC pin.
- Place components as close as possible to the IC
- Keep traces short between the IC and the C_{SRT} capacitor to ensure the timing delay is as accurate as possible.
- For VCC slew rate > 100 mV/µs, increase input capacitance and pull-up resistor value

11.2 Layout Example

图 14 shows a layout example.

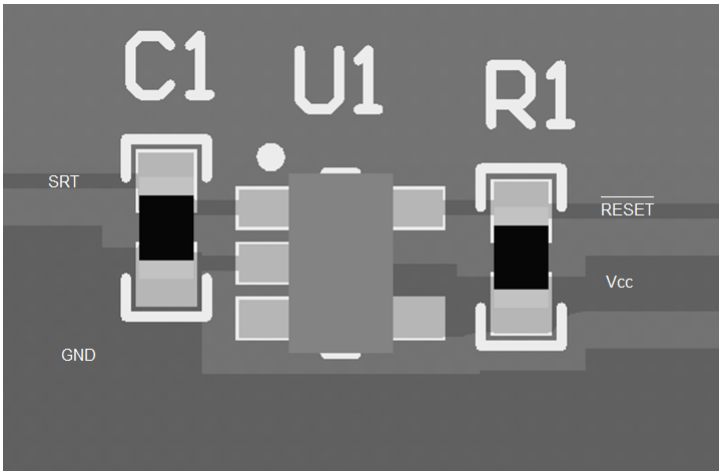

图 14. LP3470A Layout Example

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12 器件和文档支持

12.1 接收文档更新通知

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12.3 商标

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12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3470A263DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D263	Samples
LP3470A275DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D275	Samples
LP3470A293DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D293	Samples
LP3470A308DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D308	Samples
LP3470A365DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D365	Samples
LP3470A400DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D400	Samples
LP3470A438DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D438	Samples
LP3470A463DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D463	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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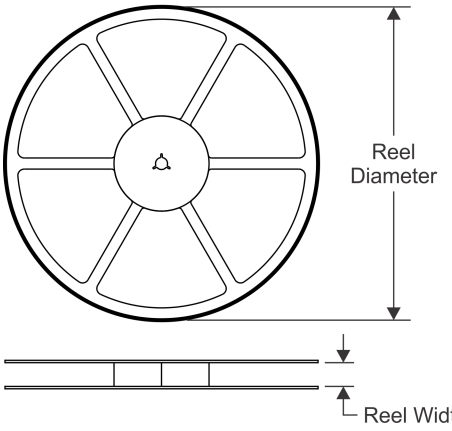
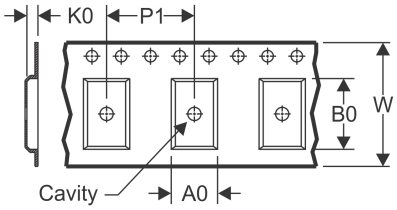
TAPE AND REEL INFORMATION

REEL DIMENSIONS

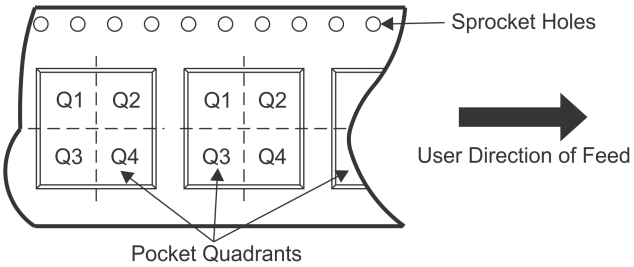


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

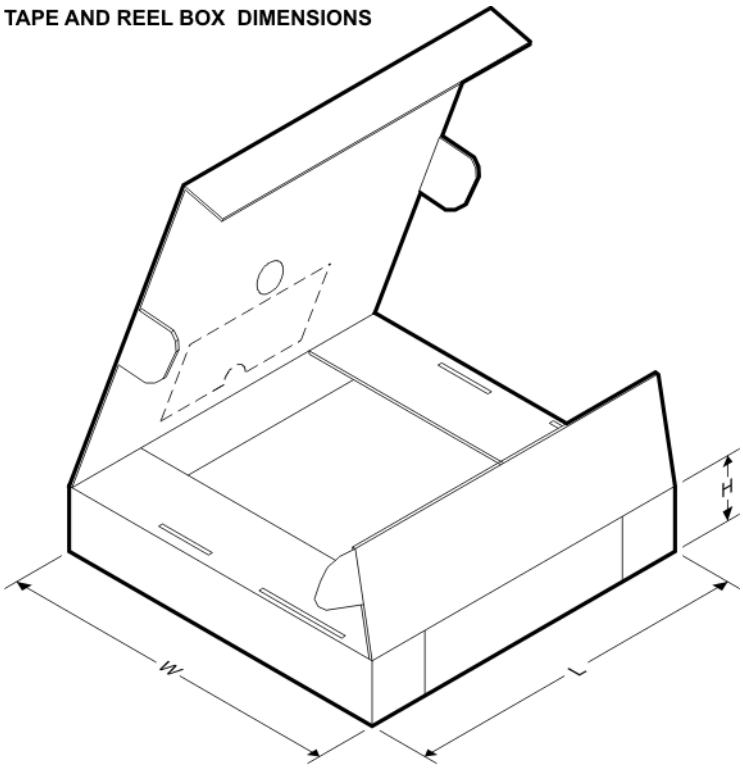
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

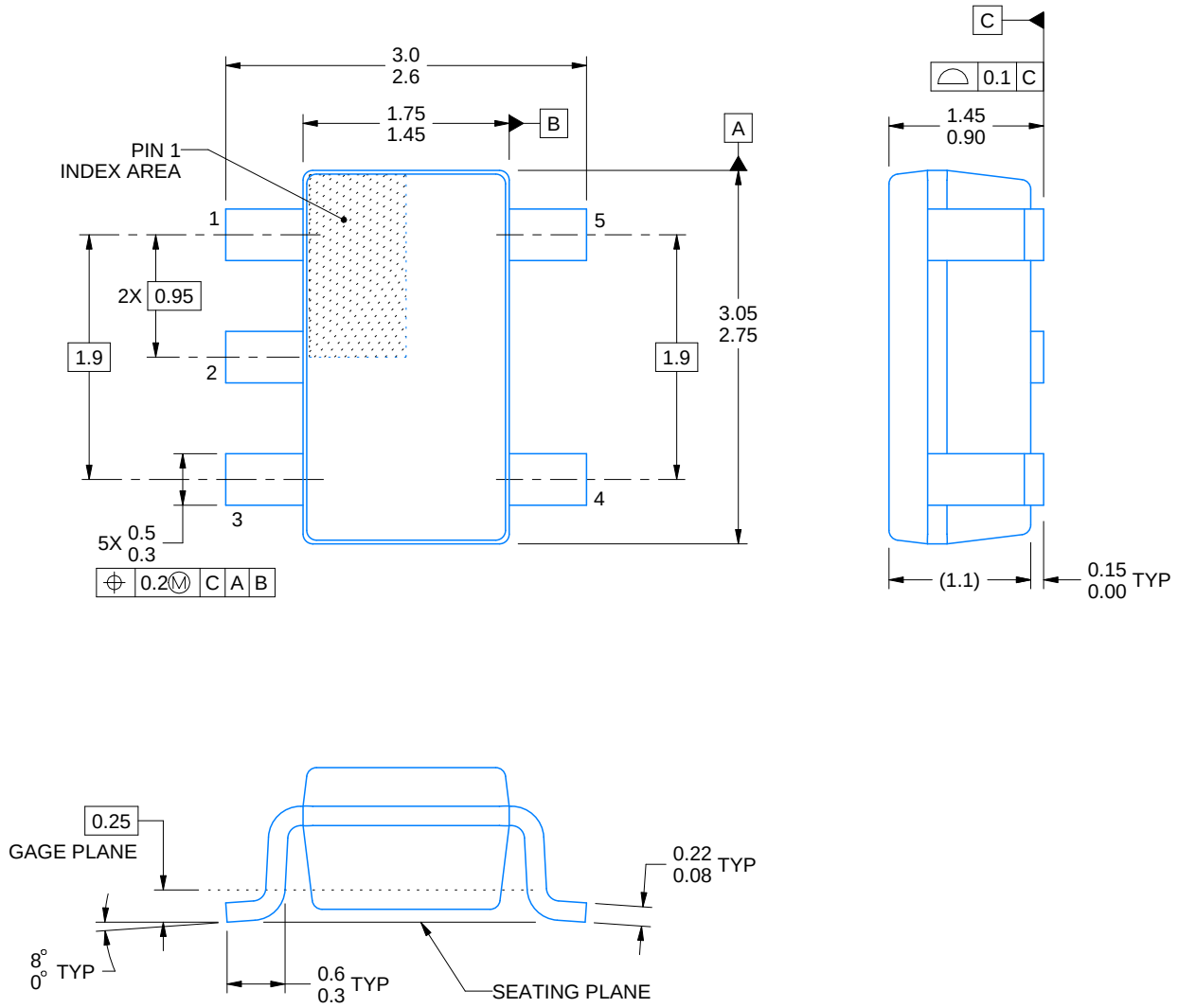
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3470A263DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470A275DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470A293DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470A308DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470A365DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470A400DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470A438DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470A463DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3470A263DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470A275DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470A293DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470A308DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470A365DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470A400DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470A438DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470A463DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0



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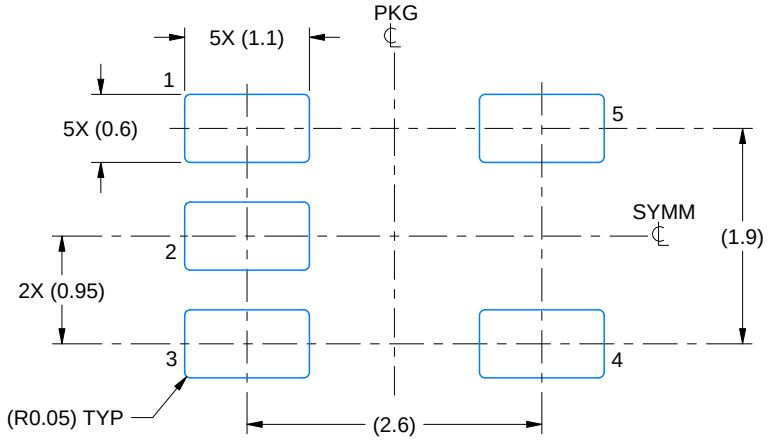
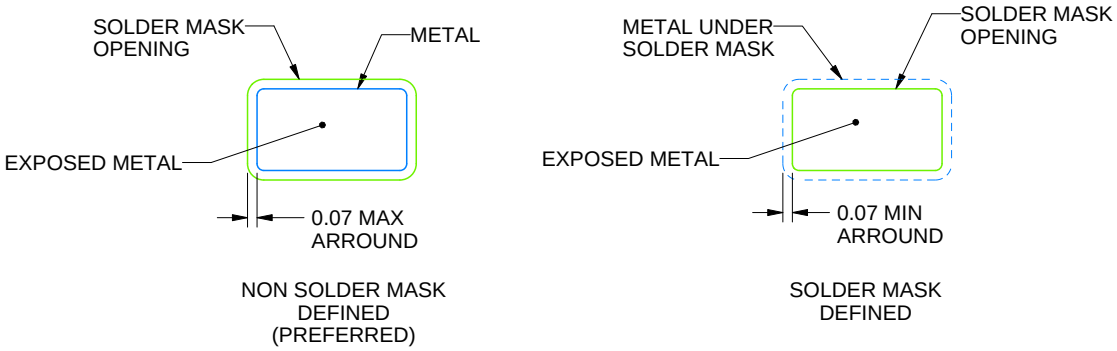
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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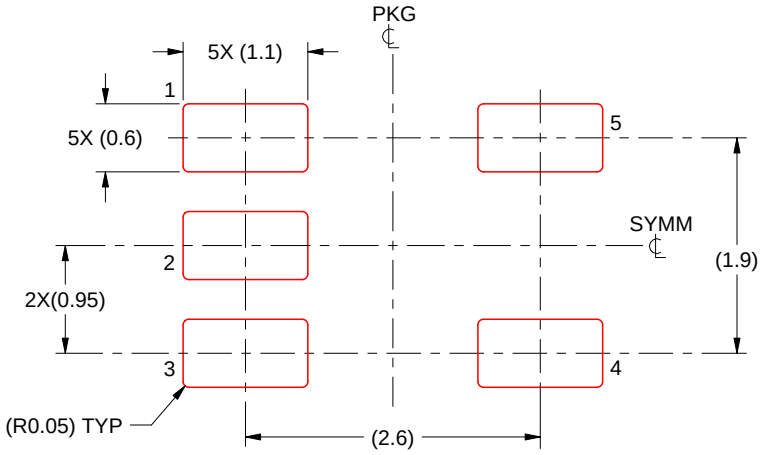
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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