

# SN74GTLP22033

## 8-BIT LVTTTL-TO-GTLP ADJUSTABLE-EDGE-RATE REGISTERED TRANSCEIVER WITH SPLIT LVTTTL PORT AND FEEDBACK PATH

SCES354C – JUNE 2001 – REVISED SEPTEMBER 2001

- **Member of the Texas Instruments Widebus™ Family**
- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTTL Logic Levels**
- **Split LVTTTL Port Provides a Feedback Path for Control and Diagnostics Monitoring**
- **AO Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **LVTTTL Interfaces Are 5-V Tolerant**
- **High-Drive GTLP Open-Drain Outputs (100 mA)**
- **Reduced LVTTTL Outputs (–12 mA/12 mA)**
- **Variable Edge-Rate Control (ERC) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I<sub>off</sub>, Power-Up 3-State, and BIAS V<sub>CC</sub> Support Live Insertion**
- **Distributed V<sub>CC</sub> and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

**DGG OR DGV PACKAGE  
(TOP VIEW)**

IMODE1	1	48	IMODE0
AI1	2	47	BIAS V <sub>CC</sub>
AO1	3	46	B1
GND	4	45	GND
AI2	5	44	OEAB
AO2	6	43	B2
V <sub>CC</sub>	7	42	ERC
AI3	8	41	OEAB
AO3	9	40	B3
GND	10	39	GND
AI4	11	38	CLKAB/LEAB
AO4	12	37	B4
AO5	13	36	B5
AI5	14	35	CLKBA/LEBA
GND	15	34	GND
AO6	16	33	B6
AI6	17	32	OEBA
V <sub>CC</sub>	18	31	V <sub>CC</sub>
AO7	19	30	B7
AI7	20	29	LOOPBACK
GND	21	28	GND
AO8	22	27	B8
AI8	23	26	V <sub>REF</sub>
OMODE0	24	25	OMODE1

### description

The SN74GTLP22033 is a high-drive, 8-bit, three-wire registered transceiver that provides inverted LVTTTL-to-GTLP and GTLP-to-LVTTTL signal-level translation. The device allows for transparent, latched, and flip-flop modes of data transfer with separate LVTTTL input and LVTTTL output pins, which provides a feedback path for control and diagnostics monitoring, the same functionality as the SN74FB2033. The device provides a high-speed interface between cards operating at LVTTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard LVTTTL or TTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The high drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 11 Ω.

The AO outputs, which are designed to sink up to 12 mA, include equivalent 26-Ω resistors to reduce overshoot and undershoot.



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## description (continued)

GTLP is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLP22033 is given only at the preferred higher noise margin GTLP, but the user has the flexibility of using this device at either GTL ( $V_{TT} = 1.2\text{ V}$  and  $V_{REF} = 0.8\text{ V}$ ) or GTLP ( $V_{TT} = 1.5\text{ V}$  and  $V_{REF} = 1\text{ V}$ ) signal levels. For information on using GTLP devices in FB+/BTL applications, refer to TI application reports, *Texas Instruments GTLP Frequently Asked Questions*, literature number SCEA019, and *GTLP in BTL Applications*, literature number SCEA017.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTTL logic levels, but are 5-V tolerant and can be directly driven by TTL or 5-V CMOS devices.  $V_{REF}$  is the B-port differential input reference voltage.

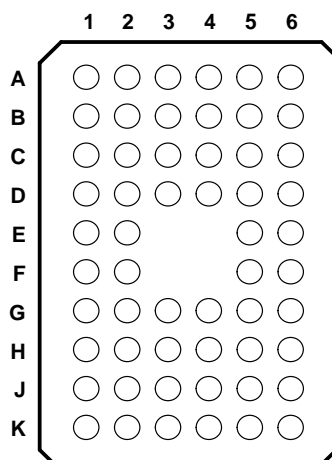
This device is fully specified for live-insertion applications using  $I_{off}$ , power-up 3-state, and BIAS  $V_{CC}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS  $V_{CC}$  circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

High-drive GTLP backplane interface devices feature adjustable edge-rate control (ERC). Changing the ERC input voltage between low and high adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

When  $V_{CC}$  is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OEAB}$  should be tied to  $V_{CC}$  through a pullup resistor and OEAB and OEBA should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

**QGL PACKAGE  
(TOP VIEW)**



## terminal assignments

	1	2	3	4	5	6
A	IMODE1	NC	NC	NC	NC	IMODE0
B	AO1	AI1	GND	GND	BIAS $V_{CC}$	B1
C	AO2	AI2	$V_{CC}$	ERC	OEAB	B2
D	AO3	AI3	GND	GND	$\overline{OEAB}$	B3
E	AO4	AI4			CLKAB/LEAB	B4
F	AO5	AI5			CLKBA/LEBA	B5
G	AO6	AI6	GND	GND	OEBA	B6
H	AO7	AI7	$V_{CC}$	$V_{CC}$	LOOPBACK	B7
J	AO8	AI8	GND	GND	$V_{REF}$	B8
K	OMODE0	NC	NC	NC	NC	OMODE1

NC = No internal connection

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### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTLP22033DGGR	GTLP22033
	TVSOP – DGV	Tape and reel	SN74GTLP22033DGVR	GT22033
	VFBGA – GQL	Tape and reel	SN74GTLP22033GQLR	GS033

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### functional description

The SN74GTLP22033 is a high-drive (100 mA), 8-bit, three-wire registered transceiver containing D-type latches and D-type flip-flops for data-path operation in the transparent, latched, or flip-flop modes. Data transmission is complementary, with inverted AI data going to the B port and inverted B data going to AO. The split LVTTTL AI and AO provides a feedback path for control and diagnostics monitoring.

The logic element for data flow in each direction is configured by two mode (IMODE1 and IMODE0 for B to A, OMODE1 and OMODE0 for A to B) inputs as a buffer, a D-type flip-flop, or a D-type latch. When configured in the buffer mode, the inverted input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock (CLKAB/LEAB or CLKBA/LEBA) input. In the latch mode, the clock inputs serve as active-high transparent latch enables.

Data flow in the B-to-A direction, regardless of the logic element selected, is further controlled by the LOOPBACK input. When LOOPBACK is low, B-port data is the B-to-A input. When LOOPBACK is high, the output of the selected A-to-B logic element (prior to inversion) is the B-to-A input.

The AO enable/disable control is provided by OEBA. When OEBA is low or when V<sub>CC</sub> is less than 1.5 V, AO is in the high-impedance state. When OEBA is high, AO is active (high or low logic levels).

The B port is controlled by OEAB and  $\overline{\text{OEAB}}$ . If OEAB is low,  $\overline{\text{OEAB}}$  is high, or V<sub>CC</sub> is less than 1.5 V, the B port is inactive. If OEAB is high and  $\overline{\text{OEAB}}$  is low, the B port is active.

The A-to-B and B-to-A logic elements are active, regardless of the state of their associated outputs. The logic elements can enter new data (in flip-flop and latch modes) or retain previously stored data while the associated outputs are in the high-impedance (AO) or inactive (B port) states.



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## Function Tables

FUNCTION/MODE

INPUTS								OUTPUT	MODE
OEBA	OEAB	$\overline{\text{OEAB}}$	OMODE1	OMODE0	IMODE1	IMODE0	LOOPBACK		
L	L	X	X	X	X	X	X	Z	Isolation
L	X	H	X	X	X	X	X		
X	H	L	L	L	X	X	X	Inverted AI to B	Buffer
X	H	L	L	H	X	X	X		Flip-flop
X	H	L	H	X	X	X	X		Latch
H	L	X	X	X	L	L	L	Inverted B to AO	Buffer
H	X	H	X	X	L	L	L		
H	L	X	X	X	L	H	L	Inverted B to AO	Flip-flop
H	X	H	X	X	L	H	L		
H	L	X	X	X	H	X	L	Inverted B to AO	Latch
H	X	H	X	X	H	X	L		
H	L	X	X	X	L	L	H	AI to AO	Buffer
H	X	H	X	X	L	L	H		
H	L	X	X	X	L	H	H	AI to AO	Flip-flop
H	X	H	X	X	L	H	H		
H	L	X	X	X	H	X	H	AI to AO	Latch
H	X	H	X	X	H	X	H		
H	H	L	X	X	X	X	L	Inverted AI to B, Inverted B to AO	Transparent with feedback path

ENABLE/DISABLE

INPUTS			OUTPUTS	
OEBA	OEAB	$\overline{\text{OEAB}}$	AO	B
L	X	X	Z	Active
H	X	X		
X	L	L	Z	Active
X	L	H		
X	H	L	Z	Active
X	H	H		

BUFFER

INPUT	OUTPUT
L	H
H	L

LATCH

INPUTS		OUTPUT
CLK/LE	DATA	
H	L	H
H	H	L
L	X	Q <sub>0</sub>

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## Function Tables (Continued)

### LOOPBACK

LOOPBACK	Q <sup>†</sup>
L	B port
H	Point P <sup>‡</sup>

<sup>†</sup>Q is the input to the B-to-A logic element.

<sup>‡</sup>P is the output of the A-to-B logic element (see functional block diagram).

### SELECT

INPUTS		SELECTED LOGIC ELEMENT
MODE1	MODE0	
L	L	Buffer
L	H	Flip-flop
H	X	Latch

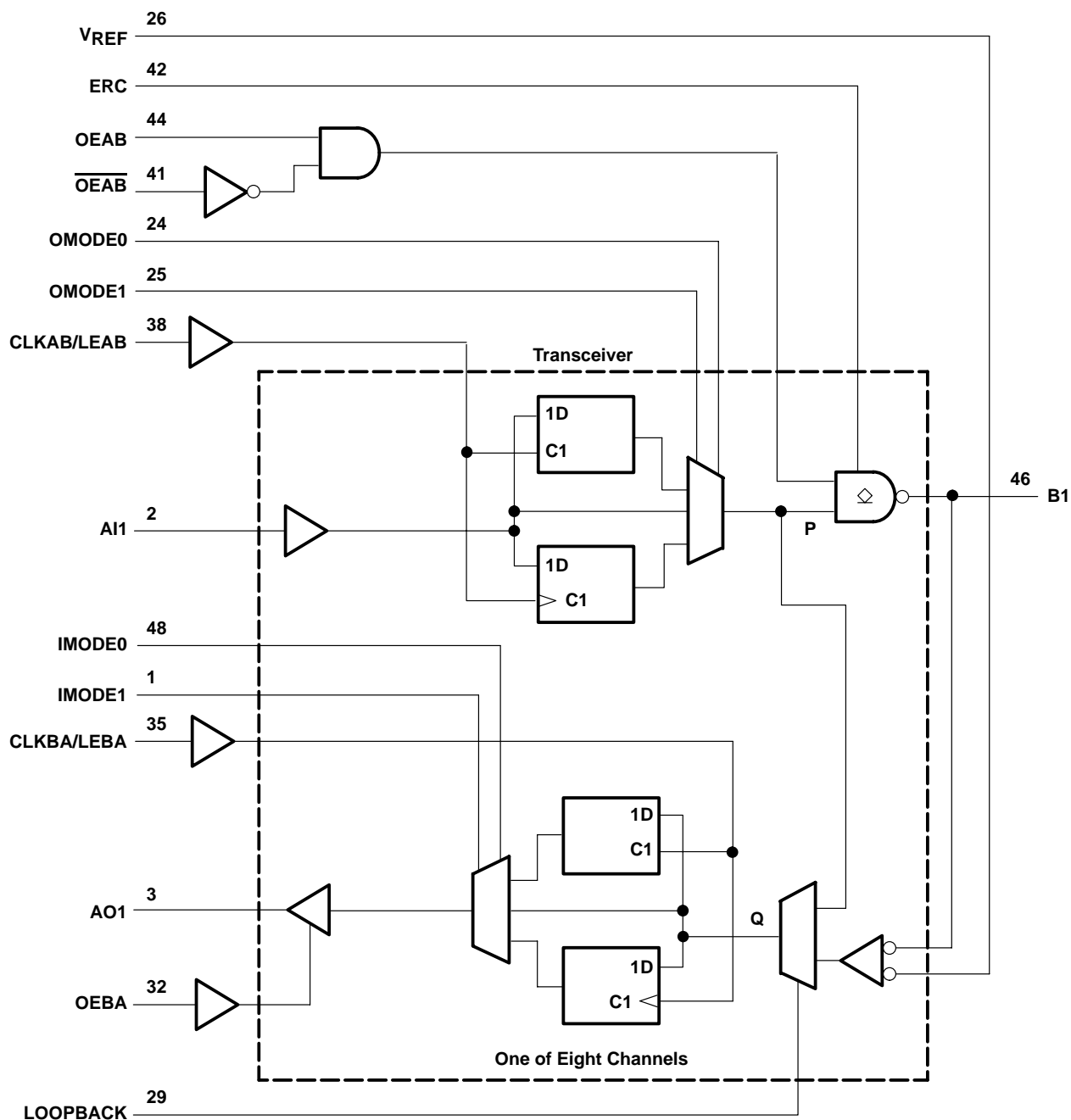
### FLIP-FLOP

INPUTS		OUTPUT
CLK/LE	DATA	
L	X	Q <sub>0</sub>
↑	L	H
↑	H	L

### B-PORT EDGE-RATE CONTROL (ERC)

INPUT ERC	OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	
H	Slow
L	Fast

## functional block diagram



Pin numbers shown are for the DGG and DGV packages.

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CC}$ and BIAS $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1): AI port, ERC, and control inputs	–0.5 V to 7 V
B port and $V_{REF}$	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$	
(see Note 1): AO port	–0.5 V to 7 V
B port	–0.5 V to 4.6 V
Current into any output in the low state, $I_O$ : AO port	24 mA
B port	200 mA
Current into any A-port output in the high state, $I_O$ (see Note 2)	24 mA
Continuous current through each $V_{CC}$ or GND	±100 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package	70°C/W
DGV package	58°C/W
GQL package	42°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
  3. The package thermal impedance is calculated in accordance with JESD 51-7.



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## recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V <sub>CC</sub> , BIAS V <sub>CC</sub>	Supply voltage		3.15	3.3	3.45	V
V <sub>TT</sub>	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V <sub>REF</sub>	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V <sub>I</sub>	Input voltage	B port	V <sub>TT</sub>			V
		Except B port and V <sub>REF</sub>	V <sub>CC</sub> 5.5			
V <sub>IH</sub>	High-level input voltage	B port	V <sub>REF</sub> +0.05			V
		Except B port	2			
V <sub>IL</sub>	Low-level input voltage	B port	V <sub>REF</sub> −0.05			V
		Except B port	0.8			
I <sub>IK</sub>	Input clamp current		−18			mA
I <sub>OH</sub>	High-level output current	AO	−12			mA
I <sub>OL</sub>	Low-level output current	AO	12			mA
		B port	100			
Δt/Δv	Input transition rise or fall rate	Outputs enabled	10			ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate		20			μs/V
T <sub>A</sub>	Operating free-air temperature		−40 85			°C

- NOTES: 4. All unused control and B-port inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS  $V_{CC} = 3.3$  V first, I/O second, and  $V_{CC} = 3.3$  V last, because the BIAS  $V_{CC}$  precharge circuitry is disabled when any  $V_{CC}$  pin is connected. The control and  $V_{REF}$  inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable but, generally, GND is connected first.
6.  $V_{TT}$  and  $R_{TT}$  can be adjusted to accommodate backplane impedances if the dc recommended  $I_{OL}$  ratings are not exceeded.
7.  $V_{REF}$  can be adjusted to optimize noise margins, but normally is two-thirds  $V_{TT}$ . TI-OPC circuitry is enabled in the A-to-B direction and is activated when  $V_{TT} > 0.7$  V above  $V_{REF}$ . If operated in the A-to-B direction,  $V_{REF}$  should be set to within 0.6 V of  $V_{TT}$  to minimize current drain.

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**electrical characteristics over recommended operating free-air temperature range for GTLP  
(unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{IK}$		$V_{CC} = 3.15\text{ V}$ , $I_I = -18\text{ mA}$			-1.2	V
$V_{OH}$	AO	$V_{CC} = 3.15\text{ V to } 3.45\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			V
		$V_{CC} = 3.15\text{ V}$ , $I_{OH} = -6\text{ mA}$	2.4			
		$V_{CC} = 3.15\text{ V}$ , $I_{OH} = -12\text{ mA}$	2			
$V_{OL}$	AO	$V_{CC} = 3.15\text{ V to } 3.45\text{ V}$ , $I_{OL} = 100\text{ }\mu\text{A}$			0.2	V
		$V_{CC} = 3.15\text{ V}$ , $I_{OL} = 6\text{ mA}$			0.55	
		$V_{CC} = 3.15\text{ V}$ , $I_{OL} = 12\text{ mA}$			0.8	
	B port	$V_{CC} = 3.15\text{ V}$ , $I_{OL} = 10\text{ mA}$			0.2	
		$V_{CC} = 3.15\text{ V}$ , $I_{OL} = 64\text{ mA}$			0.4	
		$V_{CC} = 3.15\text{ V}$ , $I_{OL} = 100\text{ mA}$			0.55	
$I_I^\ddagger$	AI and control inputs	$V_{CC} = 3.45\text{ V}$ , $V_I = 0\text{ or } 5.5\text{ V}$			$\pm 10$	$\mu\text{A}$
$I_{OZ}^\ddagger$	AO	$V_{CC} = 3.45\text{ V}$ , $V_O = 0\text{ to } 5.5\text{ V}$			$\pm 10$	$\mu\text{A}$
	B port	$V_{CC} = 3.45\text{ V}$ , $V_{REF}$ within 0.6 V of $V_{TT}$ , $V_O = 0\text{ to } 2.3\text{ V}$			$\pm 10$	
$I_{CC}$	AO or B port	$V_{CC} = 3.45\text{ V}$ , $I_O = 0$ , $V_I$ (A-port or control input) = $V_{CC}$ or GND, $V_I$ (B port) = $V_{TT}$ or GND	Outputs high		40	mA
			Outputs low		40	
			Outputs disabled		40	
$\Delta I_{CC}^\S$		$V_{CC} = 3.45\text{ V}$ , One AI or control input at $V_{CC} - 0.6\text{ V}$ , Other AI or control inputs at $V_{CC}$ or GND			1.5	mA
$C_i$	AI	$V_I = 3.15\text{ V or } 0$		3.5	4.5	pF
	Control inputs			3.5	5.5	
$C_o$	AO	$V_O = 3.15\text{ V or } 0$		5	6	pF
$C_{io}$	B port	$V_O = 1.5\text{ V or } 0$		8.5	10	pF

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

**hot-insertion specifications for A port over recommended operating free-air temperature range**

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$I_{off}$	$V_{CC} = 0$ , $V_I$ or $V_O = 0\text{ to } 5.5\text{ V}$		10	$\mu\text{A}$
$I_{OZPU}$	$V_{CC} = 0\text{ to } 1.5\text{ V}$ , $V_O = 0.5\text{ V to } 3\text{ V}$ , $OEBA = V_{CC}$		$\pm 30$	$\mu\text{A}$
$I_{OZPD}$	$V_{CC} = 1.5\text{ V to } 0$ , $V_O = 0.5\text{ V to } 3\text{ V}$ , $OEBA = V_{CC}$		$\pm 30$	$\mu\text{A}$

**live-insertion specifications for B port over recommended operating free-air temperature range**

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$I_{off}$	$V_{CC} = 0$ , BIAS $V_{CC} = 0$ , $V_I$ or $V_O = 0\text{ to } 1.5\text{ V}$		10	$\mu\text{A}$
$I_{OZPU}$	$V_{CC} = 0\text{ to } 1.5\text{ V}$ , BIAS $V_{CC} = 0$ , $V_O = 0.5\text{ V to } 1.5\text{ V}$ , $\overline{OEAB} = 0$ and $OEAB = V_{CC}$		$\pm 30$	$\mu\text{A}$
$I_{OZPD}$	$V_{CC} = 1.5\text{ V to } 0$ , BIAS $V_{CC} = 0$ , $V_O = 0.5\text{ V to } 1.5\text{ V}$ , $\overline{OEAB} = 0$ and $OEAB = V_{CC}$		$\pm 30$	$\mu\text{A}$
$I_{CC}$ (BIAS $V_{CC}$ )	$V_{CC} = 0\text{ to } 3.15\text{ V}$		5	mA
	$V_{CC} = 3.15\text{ V to } 3.45\text{ V}$ , BIAS $V_{CC} = 3.15\text{ V to } 3.45\text{ V}$ , $V_O$ (B port) = $0\text{ to } 1.5\text{ V}$		10	
$V_O$	$V_{CC} = 0$ , BIAS $V_{CC} = 3.3\text{ V}$ , $I_O = 0$	0.95	1.05	V
$I_O$	$V_{CC} = 0$ , BIAS $V_{CC} = 3.15\text{ V to } 3.45\text{ V}$ , $V_O$ (B port) = $0.6\text{ V}$	-1		$\mu\text{A}$



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timing requirements over recommended ranges of supply voltage and operating free-air temperature,  $V_{TT} = 1.5\text{ V}$  and  $V_{REF} = 1\text{ V}$  for GTLP (unless otherwise noted)

			MIN	MAX	UNIT
$f_{\text{clock}}$	Clock frequency			175	MHz
$t_w$	Pulse duration	CLKAB/LEAB or CLKBA/LEBA	2.8		ns
$t_{\text{su}}$	Setup time	AI before CLKAB $\uparrow$	1.1		ns
		AI before CLKBA $\uparrow$	1.4		
		B before CLKBA $\uparrow$	1		
		AI before LEAB $\downarrow$	1.6		
		AI before LEBA $\downarrow$	2.1		
		B before LEBA $\downarrow$	2.2		
$t_h$	Hold time	AI after CLKAB $\uparrow$	0.3		ns
		AI after CLKBA $\uparrow$	0.2		
		B after CLKBA $\uparrow$	0.6		
		AI after LEAB $\downarrow$	0.3		
		AI after LEBA $\downarrow$	0		
		B after LEBA $\downarrow$	0		

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $V_{TT} = 1.5\text{ V}$  and  $V_{REF} = 1\text{ V}$  for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
$f_{max}$				175			MHz
$t_{PLH}$	AI (buffer)	B	Slow	3	7.4		ns
$t_{PHL}$				3	7.1		
$t_{PLH}$	AI (buffer)	B	Fast	2	5.9		ns
$t_{PHL}$				2	5.8		
$t_{PLH}$	B (buffer)	AO	–	1	6.1		ns
$t_{PHL}$				1	5.4		
$t_{PLH}$	LEAB (latch mode)	B	Slow	4.2	8.6		ns
$t_{PHL}$				3.2	7.7		
$t_{PLH}$	LEAB (latch mode)	B	Fast	3.2	7.6		ns
$t_{PHL}$				2.8	6.7		
$t_{PLH}$	LEAB (latch mode)	AO	–	2	7.3		ns
$t_{PHL}$				1.8	6.6		
$t_{PLH}$	LEBA (latch mode)	AO	–	1	6		ns
$t_{PHL}$				1	5.2		
$t_{PLH}$	OEAB	B	Slow	3.8	7.5		ns
$t_{PHL}$				3.1	7		
$t_{PLH}$	OEAB	B	Fast	2.5	6		ns
$t_{PHL}$				2.5	6		
$t_{PLH}$	$\overline{OEAB}$	B	Slow	3.5	7.5		ns
$t_{PHL}$				3	7.2		
$t_{PLH}$	$\overline{OEAB}$	B	Fast	2.5	6		ns
$t_{PHL}$				2.5	6		
$t_{PZH}$	OEBA	AO	–	1	5.3		ns
$t_{PZL}$				1	4.2		
$t_{PHZ}$	OEBA	AO	–	1	5.5		ns
$t_{PLZ}$				1	5.2		
$t_{PLH}$	CLKAB (flip-flop mode)	B	Slow	4.4	8.8		ns
$t_{PHL}$				3.6	8.1		
$t_{PLH}$	CLKAB (flip-flop mode)	B	Fast	3.2	7.2		ns
$t_{PHL}$				3.1	6.9		
$t_{PLH}$	CLKAB (flip-flop mode)	AO	–	2	7.5		ns
$t_{PHL}$				1.8	7		
$t_{PLH}$	CLKBA (flip-flop mode)	AO	–	1	6		ns
$t_{PHL}$				1	5.6		
$t_{PLH}$	OMODE	B	Slow	3.8	8.7		ns
$t_{PHL}$				3.2	8.2		
$t_{PLH}$	OMODE	B	Fast	2.7	7.2		ns
$t_{PHL}$				2.7	7.2		
$t_{PLH}$	IMODE	AO	–	1	6		ns
$t_{PHL}$				1	5.1		

† Slow (ERC = H) and Fast (ERC = L)

‡ All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .



# 8-BIT LVTTTL-TO-GTLP ADJUSTABLE-EDGE-RATE REGISTERED TRANSCEIVER WITH SPLIT LVTTTL PORT AND FEEDBACK PATH

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $V_{TT} = 1.5\text{ V}$  and  $V_{REF} = 1\text{ V}$  for GTLP (see Figure 1) (continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
tPLH	LOOPBACK	AO	–	2.5		6.8	ns
tPHL				2		5.4	
tPLH	AI (loopback high)	AO	–	1		6	ns
tPHL				1		5.5	
tr	Rise time, B-port outputs (20% to 80%)		Slow	2.8		ns	
			Fast	1.5			
	Rise time, AO (10% to 90%)			5.5			
tf	Fall time, B-port outputs (80% to 20%)		Slow	3		ns	
			Fast	1.8			
	Fall time, AO (90% to 10%)			4.5			

† Slow (ERC = H) and Fast (ERC = L)

‡ All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

skew characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)§

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
$t_{sk(LH)}^{\parallel}$	AI	B	Slow	0.5		1	ns
$t_{sk(HL)}^{\parallel}$				0.5		1	
$t_{sk(LH)}^{\parallel}$	AI	B	Fast	0.4		0.9	ns
$t_{sk(HL)}^{\parallel}$				0.4		0.9	
$t_{sk(LH)}^{\parallel}$	CLKAB/LEAB	B	Slow	0.5		1	ns
$t_{sk(HL)}^{\parallel}$				0.5		1	
$t_{sk(LH)}^{\parallel}$	CLKAB/LEAB	B	Fast	0.4		0.9	ns
$t_{sk(HL)}^{\parallel}$				0.4		0.9	
$t_{sk(t)}^{\parallel}$	AI	B	Slow	1.4		2	ns
			Fast	0.6		1.4	
	CLKAB/LEAB	B	Slow	1.8		2.5	
			Fast	0.9		1.8	

† Slow (ERC = L) and Fast (ERC = H)

‡ All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§ Actual skew values between the GTLP outputs could vary on the backplane due to the loading and impedance seen by the device.

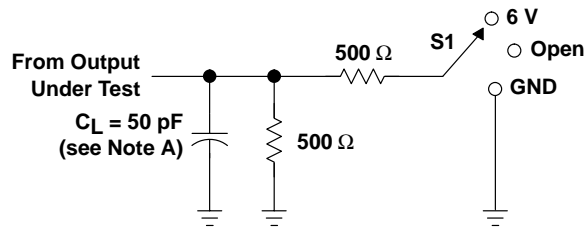
$t_{sk(LH)}/t_{sk(HL)}$  and  $t_{sk(t)}$  – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs with the same packaged device. The specifications are given for specific worst-case  $V_{CC}$  and temperature and apply to any outputs switching in the same direction either high to low [ $t_{sk(HL)}$ ] or low to high [ $t_{sk(LH)}$ ] or in opposite directions, both low to high and high to low [ $t_{sk(t)}$ ].

# SN74GTLP22033

## 8-BIT LVTTTL-TO-GTLP ADJUSTABLE-EDGE-RATE REGISTERED TRANSCEIVER WITH SPLIT LVTTTL PORT AND FEEDBACK PATH

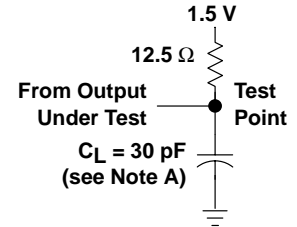
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### PARAMETER MEASUREMENT INFORMATION

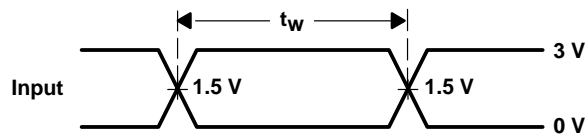


LOAD CIRCUIT FOR A OUTPUTS

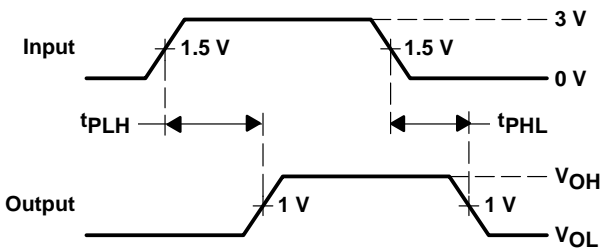
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



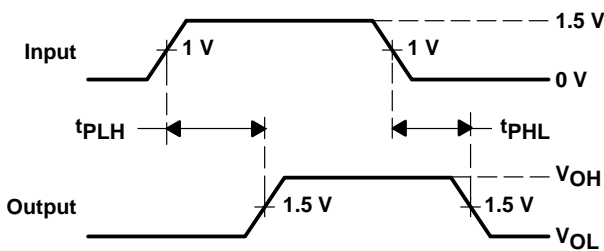
LOAD CIRCUIT FOR B OUTPUTS



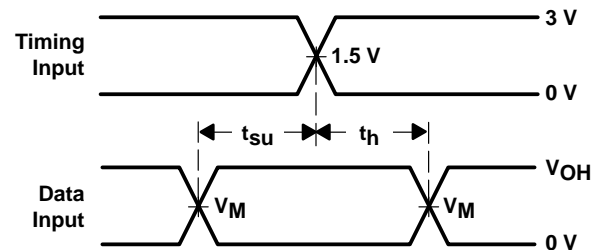
VOLTAGE WAVEFORMS  
PULSE DURATION



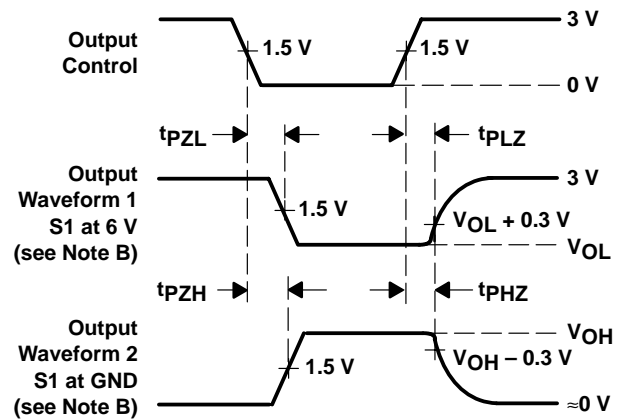
VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
(A1 to B port)



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
(B port to AO)



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES  
( $V_M = 1.5 \text{ V}$  for A port and  $1 \text{ V}$  for B port)  
( $V_{OH} = 3 \text{ V}$  for A port and  $1.5 \text{ V}$  for B port)



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
(AO)

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \approx 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \approx 2 \text{ ns}$ ,  $t_f \approx 2 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

## DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application is probably a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be closely approximated to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer to better understand the performance of the GTLP device in this typical backplane. See [www.ti.com/sc/gtlp](http://www.ti.com/sc/gtlp) for more information.

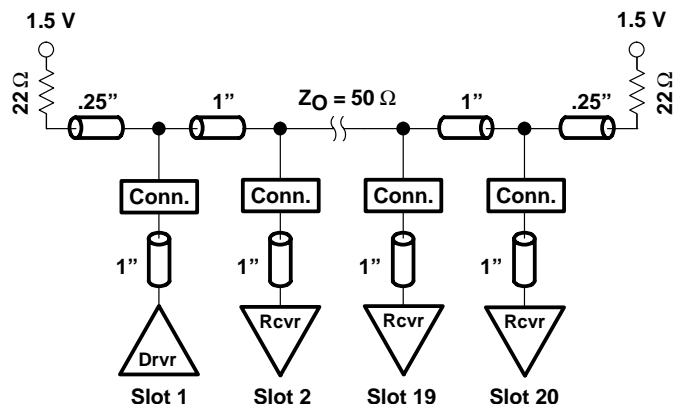


Figure 2. High-Drive Test Backplane

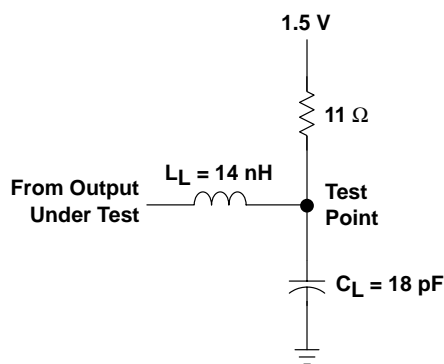


Figure 3. High-Drive RLC Network

**SN74GTLP22033**

**8-BIT LVTTTL-TO-GTLP ADJUSTABLE-EDGE-RATE REGISTERED TRANSCEIVER  
WITH SPLIT LVTTTL PORT AND FEEDBACK PATH**

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**switching characteristics over recommended operating conditions for the bus transceiver function (unless otherwise noted) (see Figure 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	TYP‡	UNIT
tPLH	AI (buffer)	B	Slow	4.7	ns
tPHL				5	
tPLH	AI (buffer)	B	Fast	3.7	ns
tPHL				4	
tPLH	LEAB (latch mode)	B	Slow	5.5	ns
tPHL				5.8	
tPLH	LEAB (latch mode)	B	Fast	4.6	ns
tPHL				4.8	
tPLH	CLKAB (flip-flop mode)	B	Slow	5.8	ns
tPHL				6	
tPLH	CLKAB (flip-flop mode)	B	Fast	4.9	ns
tPHL				4.9	
tPLH	OMODE	B	Slow	5.5	ns
tPHL				5.7	
tPLH	OMODE	B	Fast	4.5	ns
tPHL				4.7	
tr	Rise time, B-port outputs (20% to 80%)		Slow	1.8	ns
			Fast	1.1	
tf	Fall time, B-port outputs (80% to 20%)		Slow	3.4	ns
			Fast	2.6	

† Slow (ERC = H) and Fast (ERC = L)

‡ All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C. All values are derived from TI-SPICE models.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74GTLP22033DGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GTLP22033	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

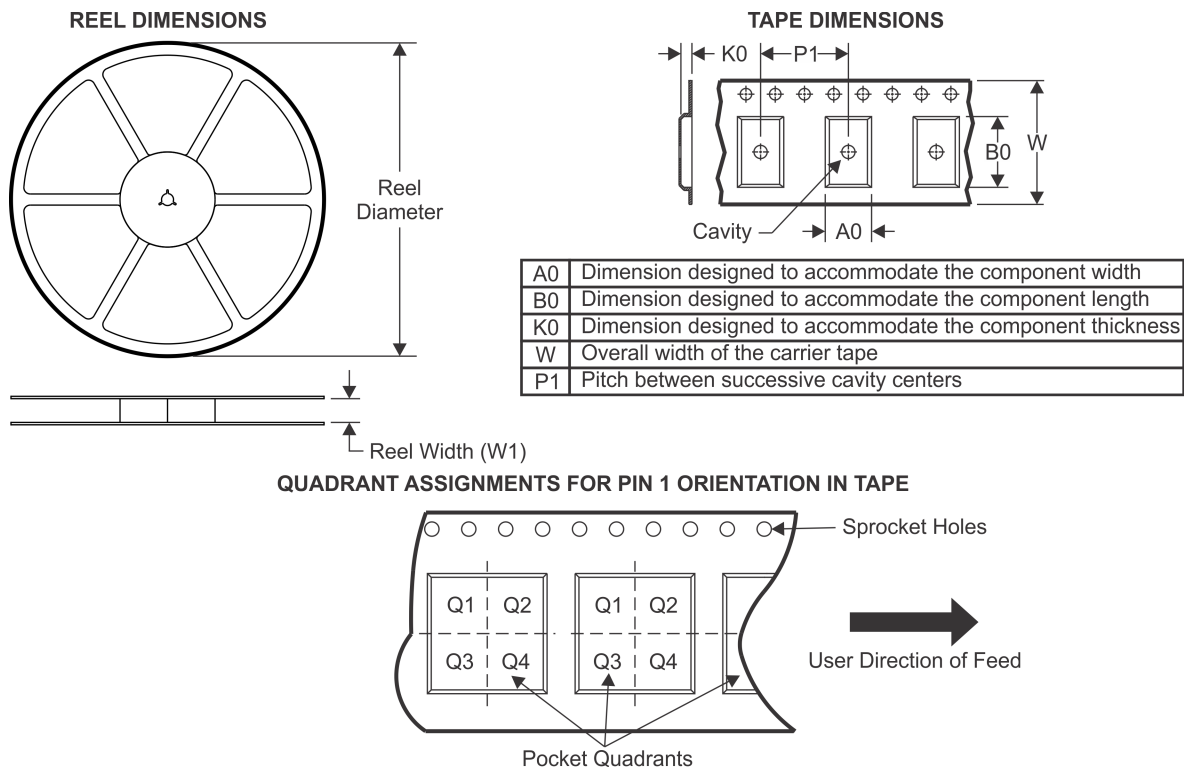
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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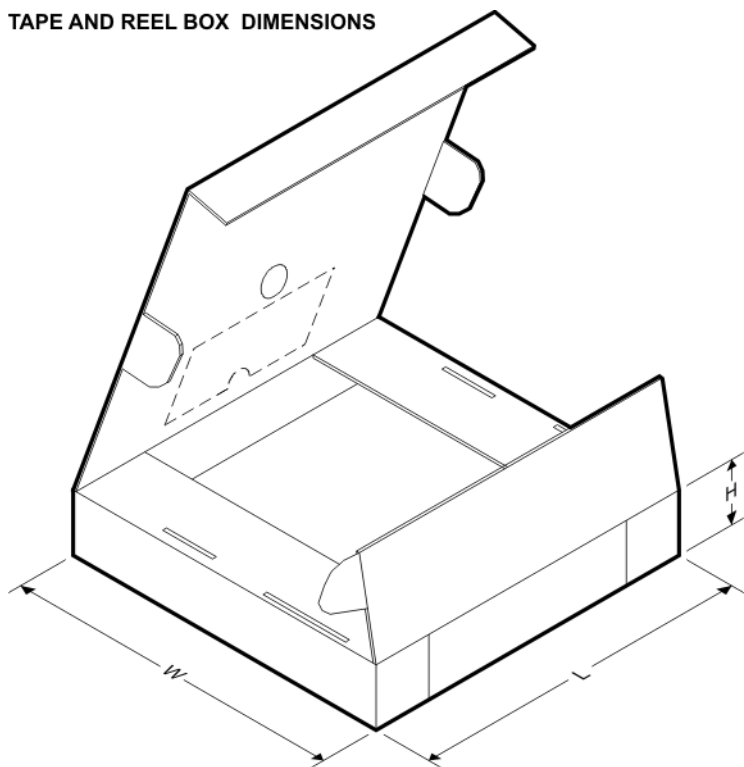
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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

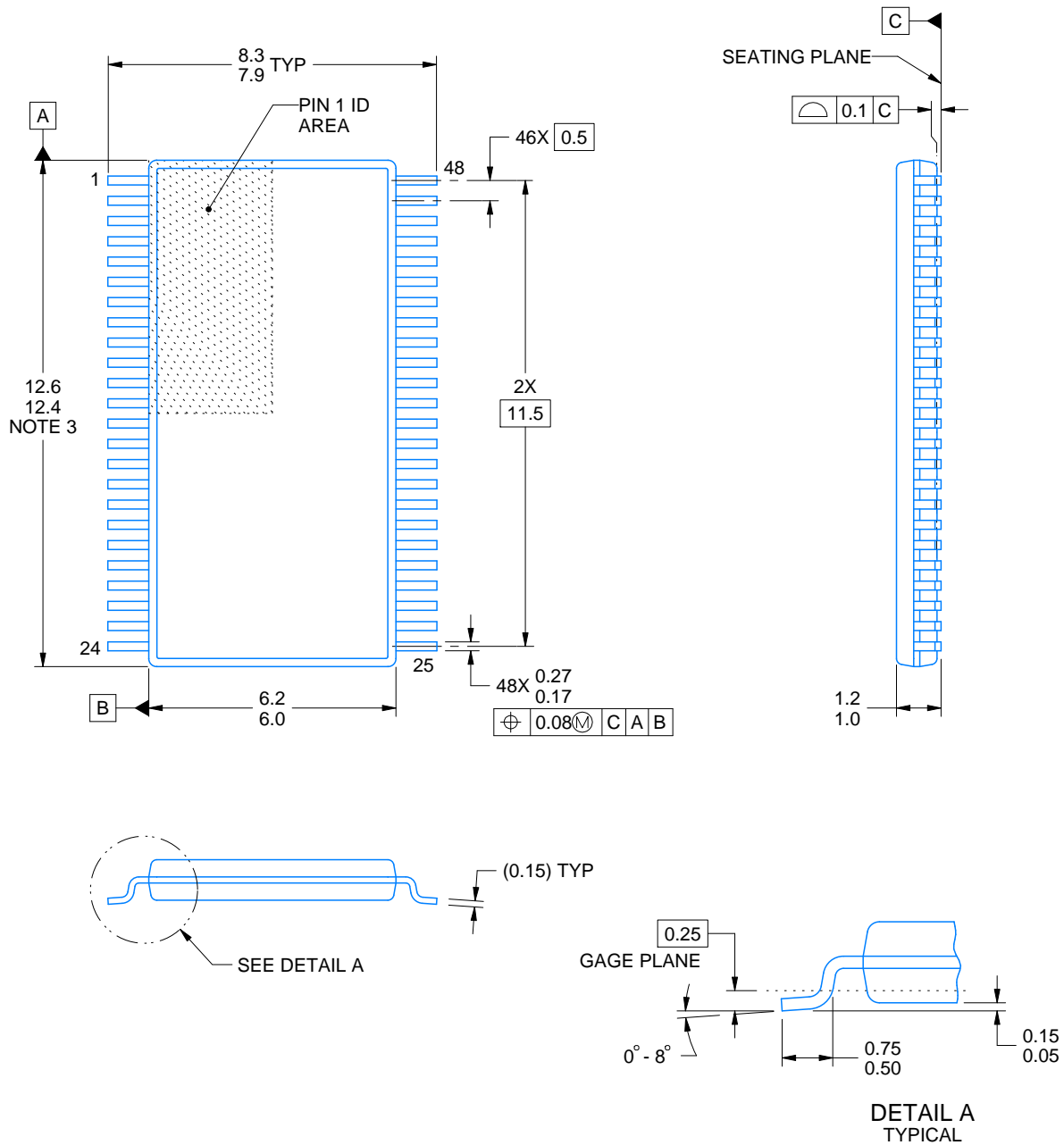
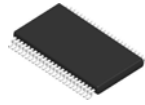
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTLP22033DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTL22033DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0



4214859/B 11/2020

## NOTES:

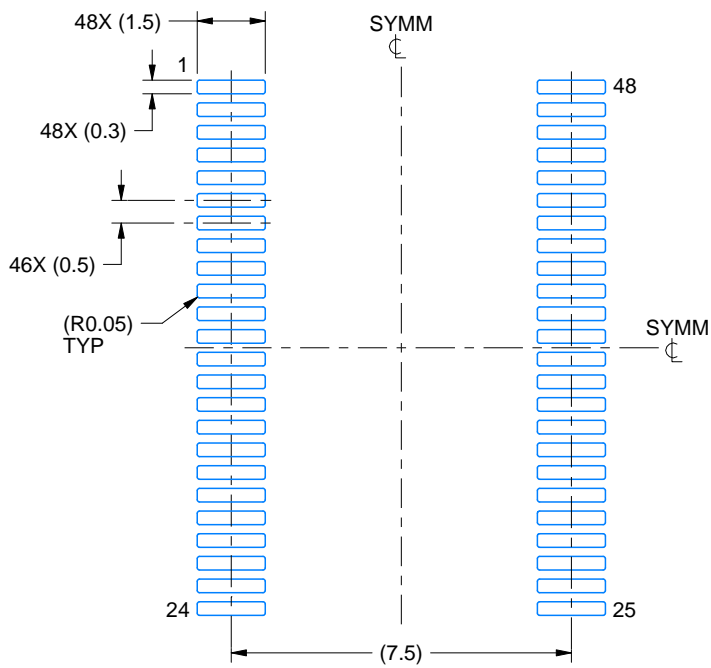
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

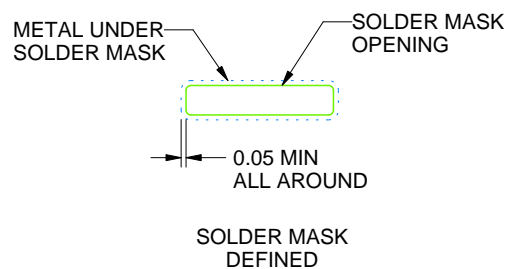
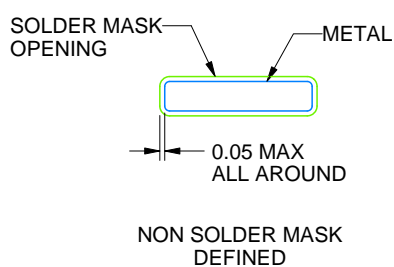
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

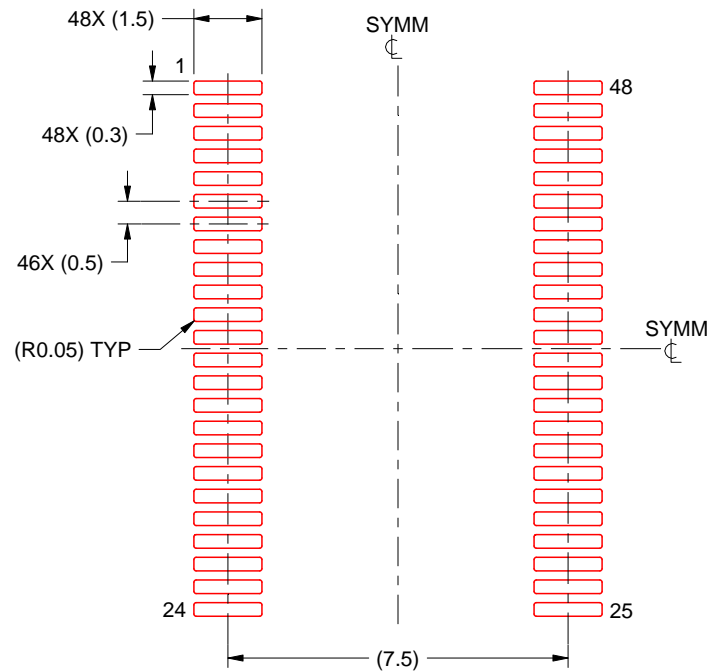
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4214859/B 11/2020

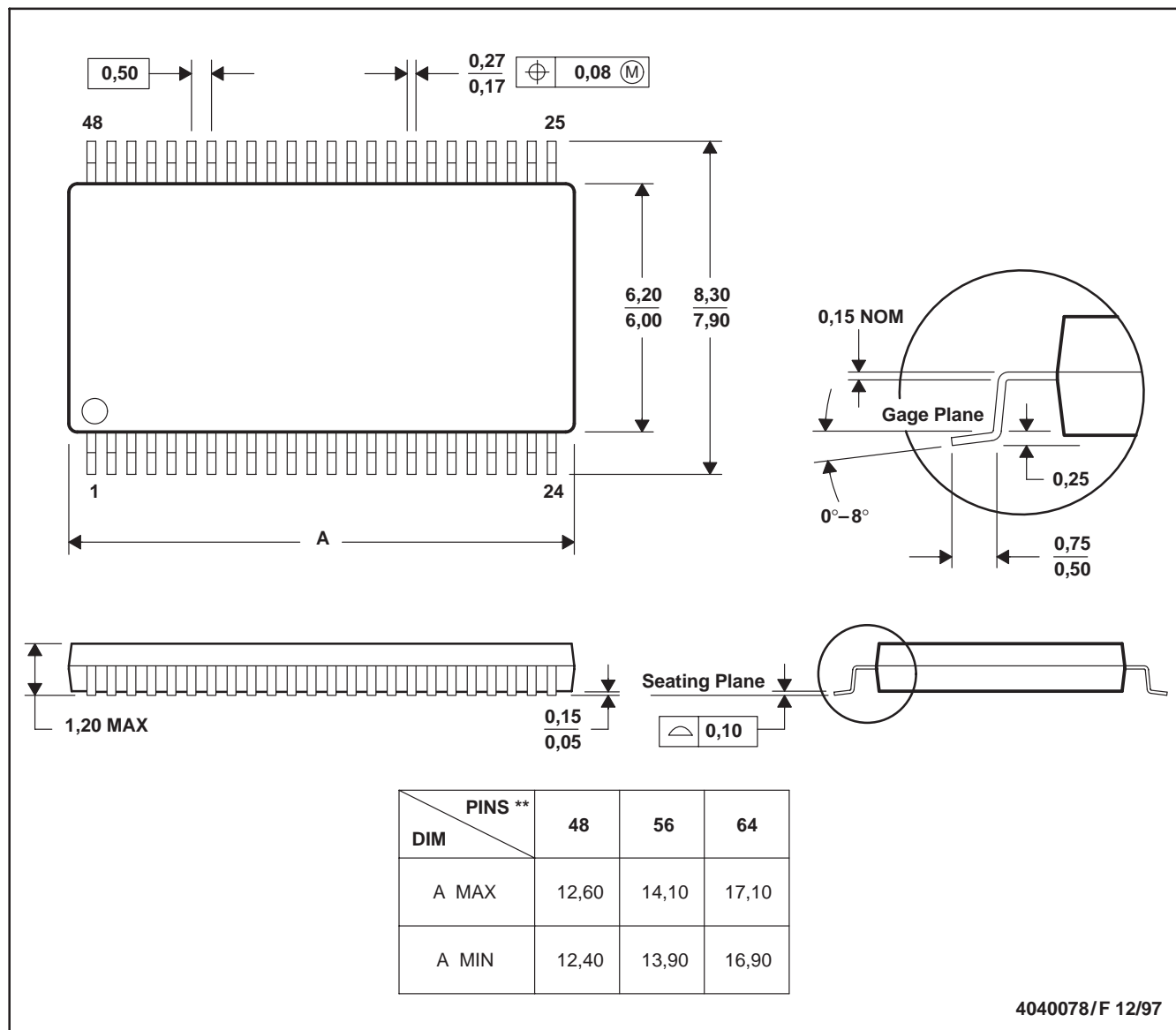
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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