

TLVH431B-EP Enhanced Plastic 0.5% Low-Voltage Wide-Operating Current Adjustable Precision Shunt Regulator

1 Features

- Low-voltage operation: down to 1.24 V
- Reference voltage tolerances 0.5% at 25°C
- Adjustable output voltage, $V_O = V_{REF}$ to 18 V
- Wide operating cathode current range: 200 μ A to 70 mA
- 0.25- Ω typical output impedance
- Supports defense and aerospace applications:
 - Controlled baseline
 - Available in extended (–55°C to 125°C) temperature range
 - Extended product life cycle
 - Extended product-change notification
 - Product traceability

2 Applications

- Adjustable voltage and current referencing
- Secondary side regulation in flyback SMPSs
- Zener replacement
- Voltage monitoring
- Comparator with integrated reference

3 Description

The TLVH431B-EP device is a low-voltage, 3-terminal, adjustable voltage reference with specified thermal stability over applicable industrial and commercial temperature ranges. Output voltage can be set to any value between V_{REF} (1.24 V) and 18 V with two external resistors (see [Figure 24](#)). This device operates from a lower voltage (1.24 V) than the widely used TL431 and TL1431 shunt-regulator references.

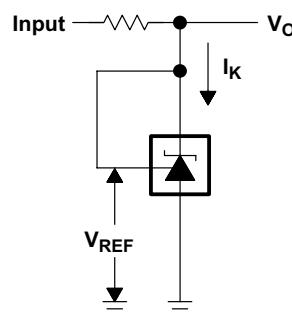
When used with an optocoupler, the TLVH431B-EP device is ideal for voltage references in isolated feedback circuits designed for 3-V to 3.3-V switching-mode power supplies. It has a typical output impedance of 0.25 Ω . Active output circuitry provides a very sharp turn-on characteristic, making the TLVH431B-EP device an excellent replacement for low-voltage Zener diodes in many applications, including on-board regulation and adjustable power supplies.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLVH431BMDBZREP	SOT-23 (3)	2.92 mm x 1.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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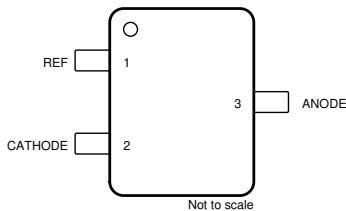
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2019	*	Initial release.

5 Pin Configuration and Functions

**TLVH431B-EP DBZ Package
3-Pin SOT-23
Top View**



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
CATHODE	2	I/O	Shunt current/voltage input
REF	1	I	Threshold relative to common anode
ANODE	3	O	Common pin, normally connected to ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{KA}	Cathode voltage ⁽²⁾		20	V
I_K	Cathode current	-25	80	mA
I_{ref}	Reference current	-0.05	3	mA
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Voltage values are with respect to the anode terminal, unless otherwise noted.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 2000
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	± 1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See⁽¹⁾

		MIN	MAX	UNIT
V_{KA}	Cathode voltage	V_{REF}	18	V
I_K	Cathode current (continuous)	0.2	70	mA
T_A	Operating free-air temperature	-55	125	°C

(1) Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A) / \theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	TLVH431B-EP	UNIT	
	DBZ (SOT-23)		
	3 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	226.5	°C/W
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	91.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44.7	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

at -55°C to 125°C free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF} Reference voltage	$V_{\text{KA}} = V_{\text{REF}}$, $I_K = 10 \text{ mA}$, see Figure 23	$T_A = 25^{\circ}\text{C}$	1.234	1.24	1.246
		$T_A = \text{full range}^{(1)}$	1.221		1.265
$V_{\text{REF(dev)}}$ V_{REF} deviation ⁽²⁾	$V_{\text{KA}} = V_{\text{REF}}$, $I_K = 10 \text{ mA}$, see Figure 23		11	31	mV
$\frac{\Delta V_{\text{REF}}}{\Delta V_{\text{KA}}}$ Ratio of V_{REF} change to cathode voltage change	$I_K = 10 \text{ mA}$, $V_K = V_{\text{REF}}$ to 18 V, see Figure 24	$T_A = 25^{\circ}\text{C}$		-1.5	-2.7
I_{ref} Reference terminal current	$I_K = 10 \text{ mA}$, $R1 = 10 \text{ k}\Omega$, $R2 = \text{open}$, see Figure 24	$T_A = 25^{\circ}\text{C}$		0.1	0.5
$I_{\text{ref(dev)}}$ I_{ref} deviation ⁽²⁾	$I_K = 10 \text{ mA}$, $R1 = 10 \text{ k}\Omega$, $R2 = \text{open}$, see Figure 24 ⁽¹⁾			0.15	0.5
$I_{K(\text{min})}$ Minimum cathode current for regulation	$V_{\text{KA}} = V_{\text{REF}}$, see Figure 23	$T_A = 25^{\circ}\text{C}$	60	100	μA
		$T_A = \text{full range}^{(1)}$		200	
$I_{K(\text{off})}$ Off-state cathode current	$V_{\text{REF}} = 0$, $V_{\text{KA}} = 18 \text{ V}$, see Figure 25	$T_A = 25^{\circ}\text{C}$		0.02	0.1
		$T_A = \text{full range}^{(1)}$			0.7
$ z_{\text{KA}} $ Dynamic impedance ⁽³⁾	$V_{\text{KA}} = V_{\text{REF}}$, $f \leq 1 \text{ kHz}$, $I_K = 0.2 \text{ mA}$ to 70 mA, see Figure 23	$T_A = 25^{\circ}\text{C}$		0.25	0.4

(1) Full temperature range is -55°C to 125°C .

(2) The deviation parameters $V_{\text{REF(dev)}}$ and $I_{\text{ref(dev)}}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, αV_{REF} , is defined as:

$$|\alpha V_{\text{REF}}| \left(\frac{\text{ppm}}{^{\circ}\text{C}} \right) = \frac{\left(\frac{V_{\text{REF(dev)}}}{V_{\text{REF}} (T_A = 25^{\circ}\text{C})} \right) \times 10^6}{\Delta T_A}$$

where ΔT_A is the rated operating free-air temperature range of the device.

αV_{REF} can be positive or negative, depending on whether minimum V_{REF} or maximum V_{REF} , respectively, occurs at the lower temperature.

(3) The dynamic impedance is defined as:

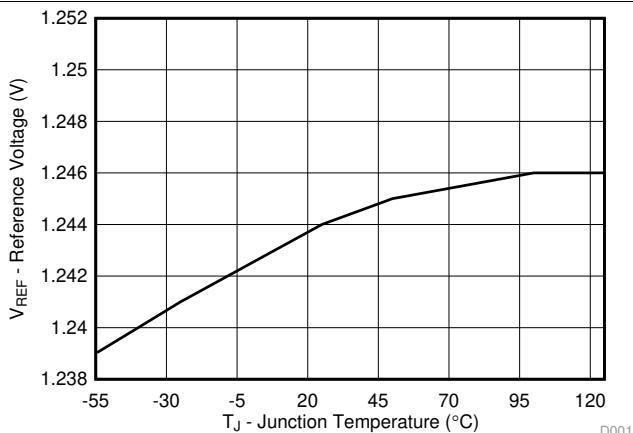
$$|z_{\text{ka}}| = \frac{\Delta V_{\text{KA}}}{\Delta I_K}$$

When the device is operating with two external resistors (see [Figure 24](#)), the total dynamic impedance of the circuit is defined as:

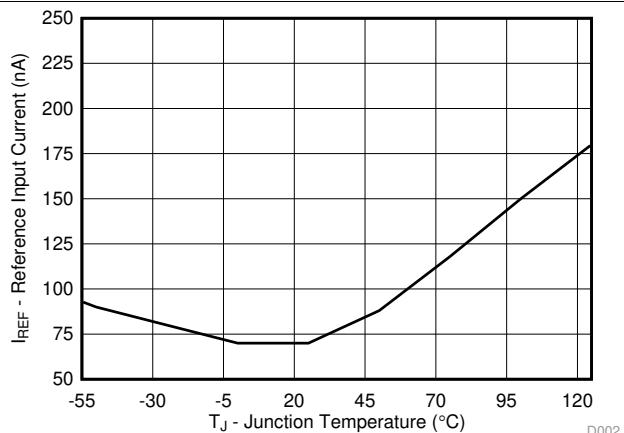
$$|z_{\text{ka}}|' = \frac{\Delta V}{\Delta I} \approx |z_{\text{ka}}| \times \left(1 + \frac{R1}{R2} \right)$$

6.6 Typical Characteristics

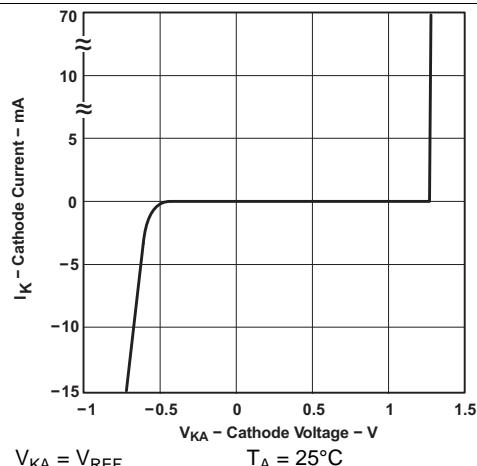
Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.



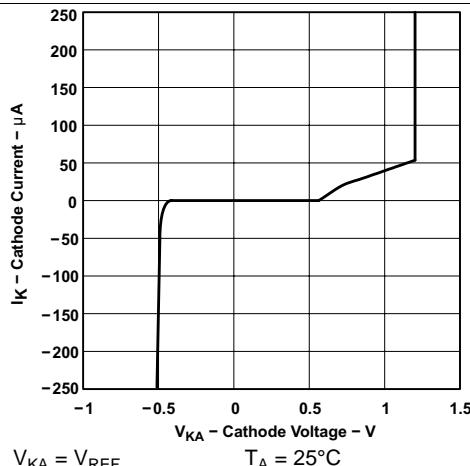
**Figure 1. Reference Voltage
vs Junction Temperature**



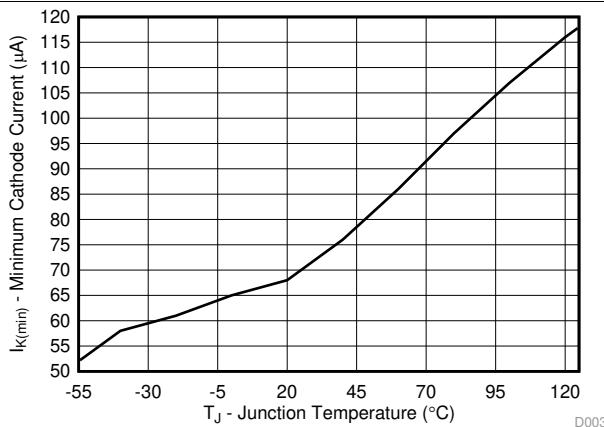
**Figure 2. Reference Input Current
vs Junction Temperature**



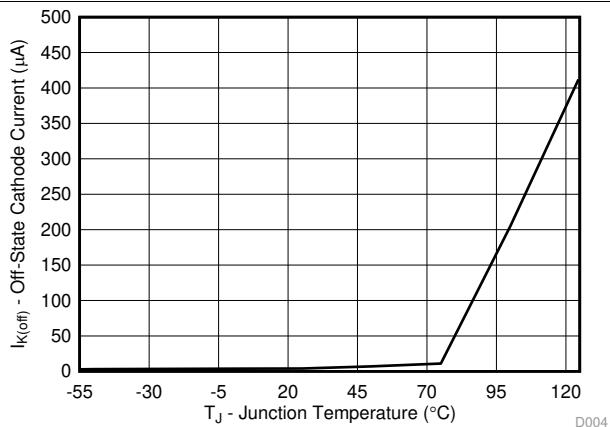
**Figure 3. Cathode Current
vs Cathode Voltage**



**Figure 4. Cathode Current
vs Cathode Voltage**



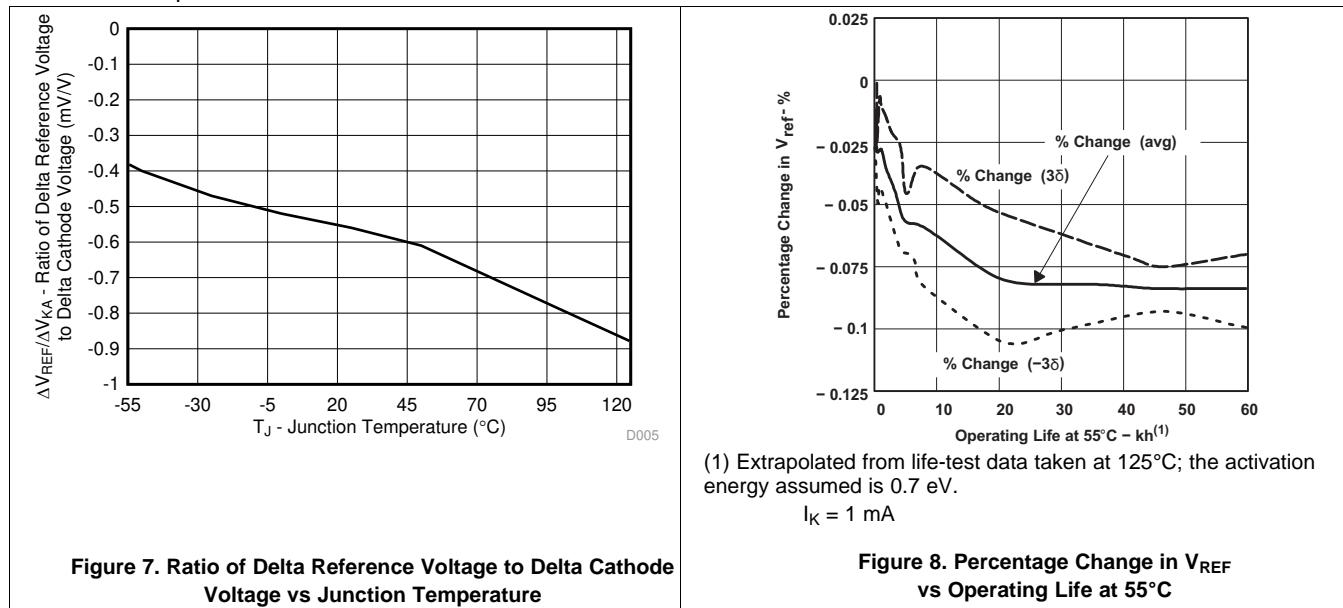
**Figure 5. Minimum Cathode Current
vs Junction Temperature**



**Figure 6. Off-State Cathode Current
vs Junction Temperature**

Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.



Typical Characteristics (continued)

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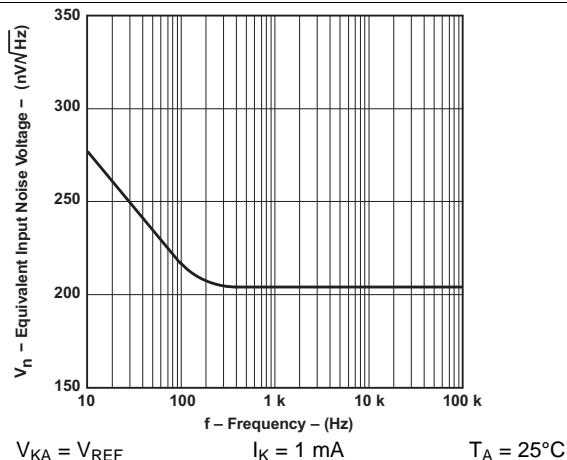


Figure 9. Equivalent Input Noise Voltage vs Frequency

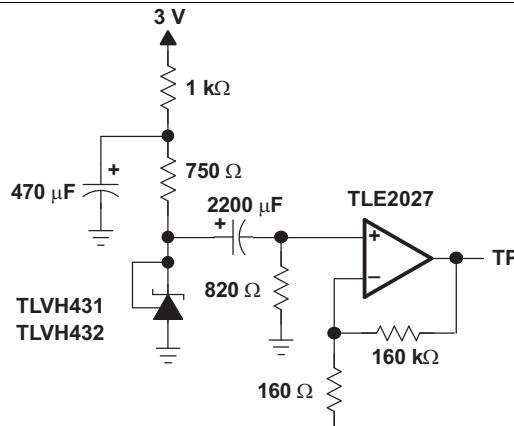


Figure 10. Test Circuit for Equivalent Noise Voltage

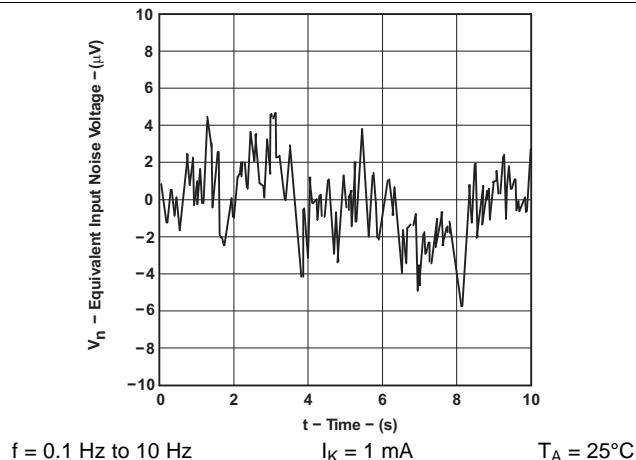


Figure 11. Equivalent Input Noise Voltage Over a 10-s Period

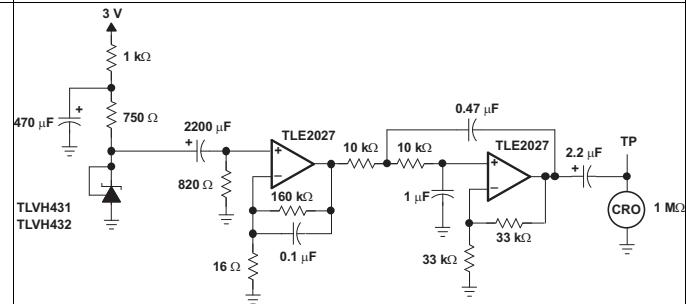


Figure 12. Test Circuit for 0.1-Hz to 10-Hz Equivalent Noise Voltage

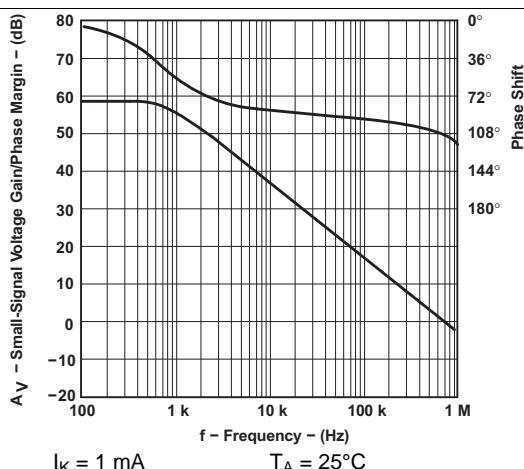


Figure 13. Voltage Gain and Phase Margin vs Frequency

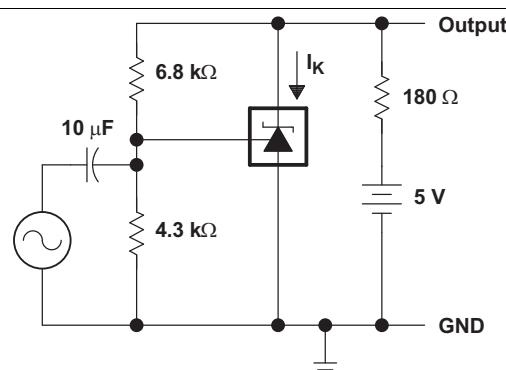
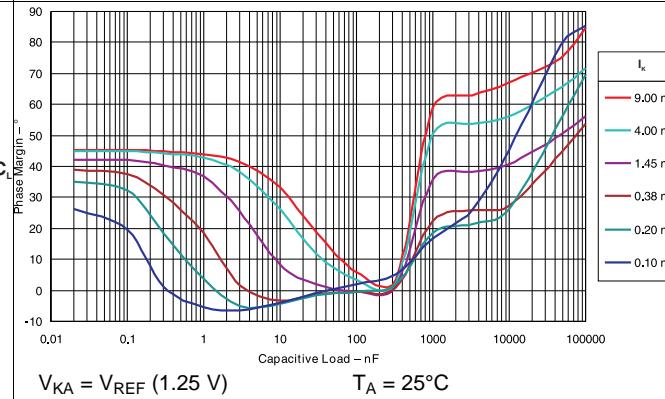
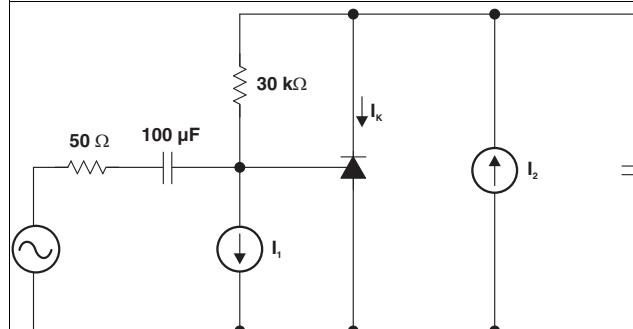
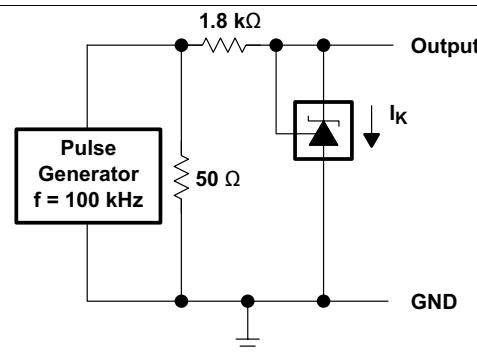
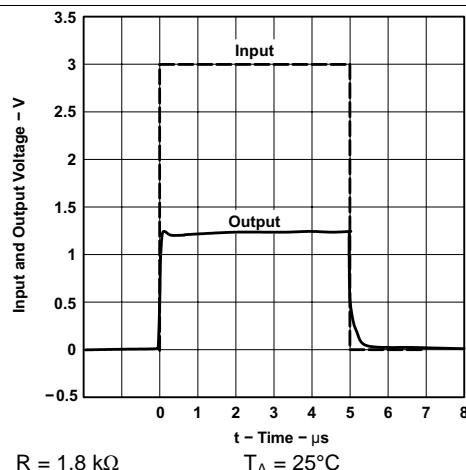
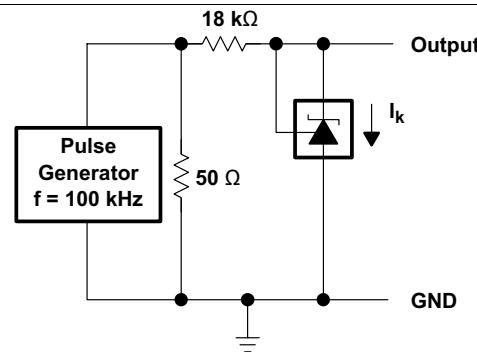
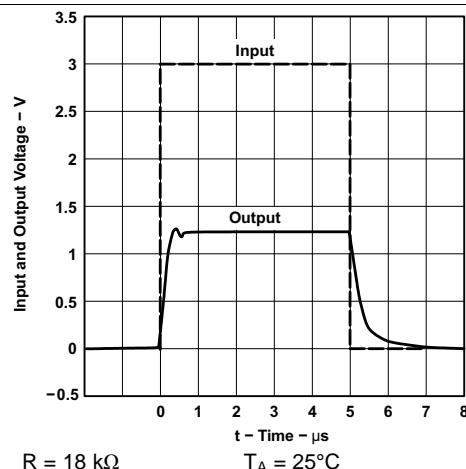


Figure 14. Test Circuit for Voltage Gain and Phase Margin

Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.



Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

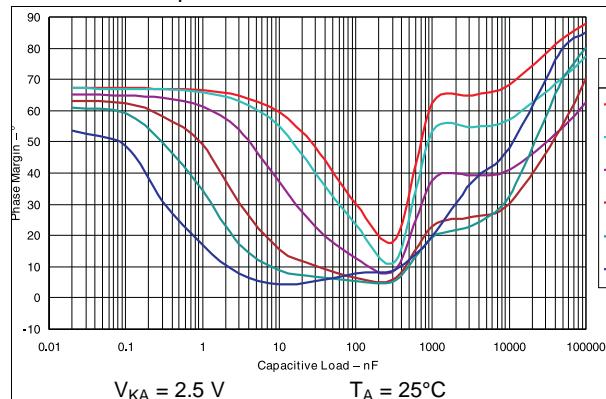


Figure 21. Phase Margin vs Capacitive Load

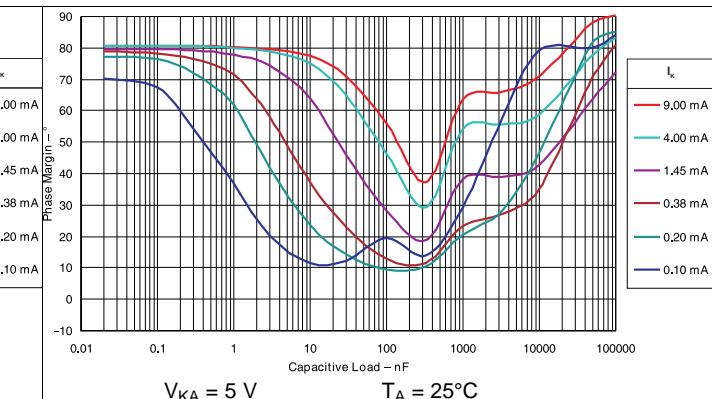


Figure 22. Phase Margin vs Capacitive Load

7 Parameter Measurement Information

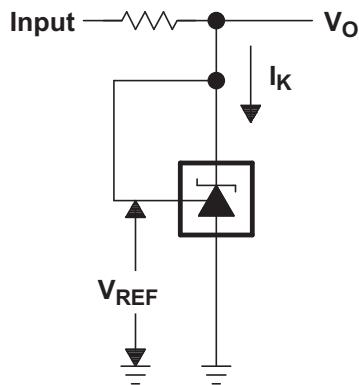


Figure 23. Test Circuit for $V_{KA} = V_{REF}$, $V_O = V_{KA} = V_{REF}$

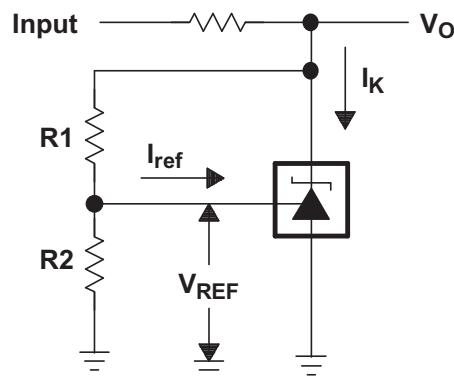


Figure 24. Test Circuit for $V_{KA} > V_{REF}$, $V_O = V_{KA} = V_{REF} \times (1 + R1 / R2) + I_{ref} \times R1$

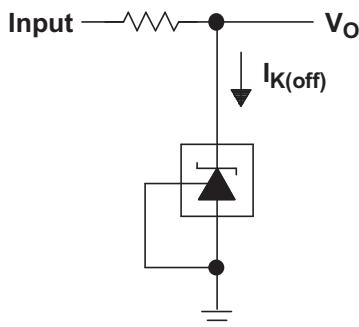


Figure 25. Test Circuit for $I_{K(off)}$

8 Detailed Description

8.1 Overview

TLVH431B-EP is a low power counterpart to TL431, having lower reference voltage (1.24 V versus 2.5 V) for lower voltage adjustability and lower minimum cathode current ($I_{K(min)} = 200 \mu A$ versus 1 mA). Like TL431, TLVH431B-EP is used in conjunction with its key components to behave as a single voltage reference, error amplifier, voltage clamp or comparator with integrated reference.

TLVH431B-EP is also a higher voltage counterpart to TLV431, with cathode voltage adjustability from 1.24 V to 18 V, making this part optimum for a wide range of end equipments in industrial, auto, telecom and computing. In order for this device to behave as a shunt regulator or error amplifier, $> 200 \mu A$ ($I_{min(max)}$) must be supplied to the cathode pin. Under this condition, feedback can be applied from the Cathode and Ref pins to create a replica of the internal reference voltage.

The reference voltage initial tolerance (at 25°C) is 0.5% and these devices are characterized for operation from $-55^{\circ}C$ to $125^{\circ}C$.

8.2 Functional Block Diagram

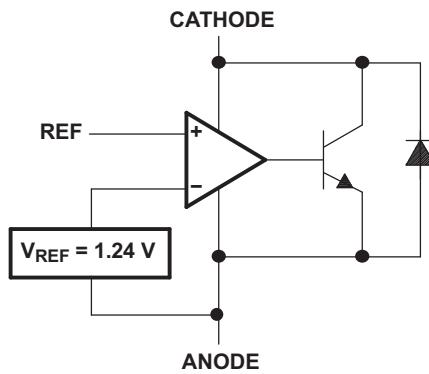


Figure 26. Equivalent Schematic

Functional Block Diagram (continued)

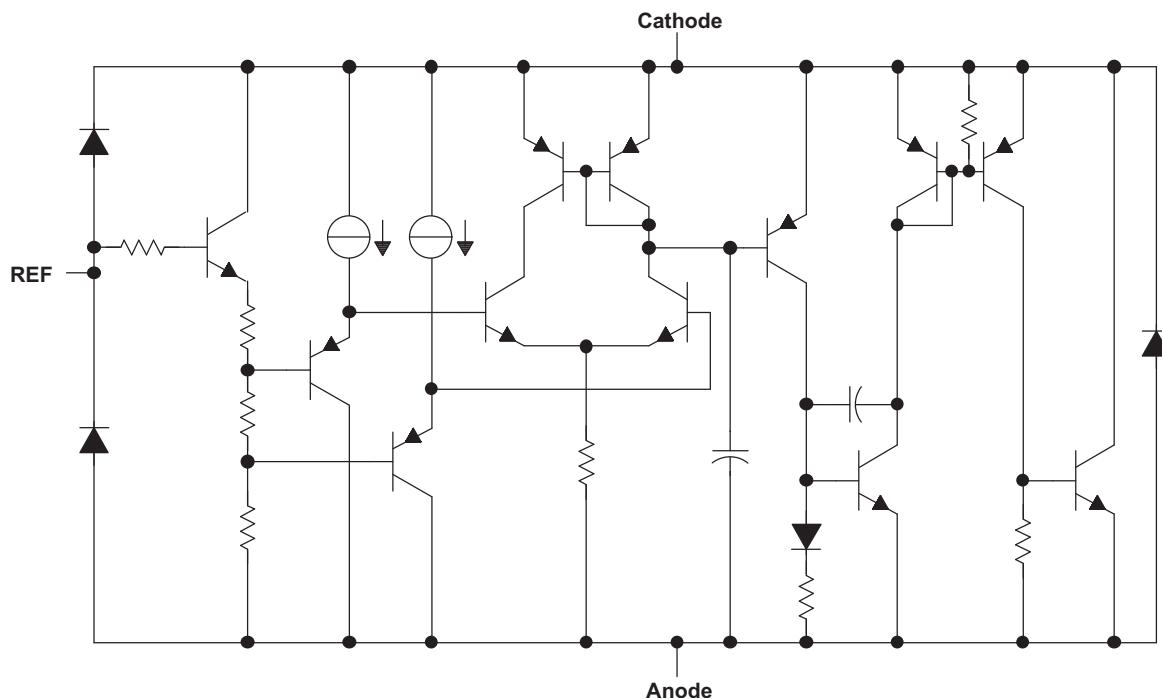


Figure 27. Detailed Schematic

8.3 Feature Description

TLVH431B-EP consists of an internal reference and amplifier that outputs a sink current base on the difference between the reference pin and the virtual internal pin. The sink current is produced by an internal Darlington pair.

When operated with enough voltage headroom (≥ 1.24 V) and cathode current (I_{ka}), TLVH431B-EP forces the reference pin to 1.24 V. However, the reference pin can not be left floating, as it needs $I_{ref} \geq 0.5$ μ A (see the [Specifications](#) section). This is because the reference pin is driven into an NPN, which needs base current in order operate properly.

When feedback is applied from the Cathode and Reference pins, TLVH431B-EP behaves as a Zener diode, regulating to a constant voltage dependent on current being supplied into the cathode. This is due to the internal amplifier and reference entering the proper operating regions. The same amount of current needed in the above feedback situation must be applied to this device in open loop, servo, or error amplifying implementations in order for it to be in the proper linear region giving TLVH431B-EP enough gain.

Unlike many linear regulators, TLVH431B-EP is internally compensated to be stable without an output capacitor between the cathode and anode. If instead it is desired to use an output capacitor, [Figure 20](#), [Figure 21](#), and [Figure 22](#) can be used as a guide to assist in choosing the correct capacitor to maintain stability.

8.4 Device Functional Modes

8.4.1 Open Loop (Comparator)

When the cathode/output voltage or current of TLVH431B-EP is not being fed back to the reference/input pin in any form, this device is operating in open loop. With proper cathode current (I_{ka}) applied to this device, TLVH431B-EP has the characteristics shown in [Figure 4](#). With such high gain in this configuration, the TLVH431B-EP device is typically used as a comparator. With the reference integrated makes TLVH431B-EP the preferred choice when users are trying to monitor a certain level of a single signal.

8.4.2 Closed Loop

When the cathode/output voltage or current of TLVH431B-EP is being fed back to the reference/input pin in any form, this device is operating in closed loop. The majority of applications involving TLVH431B-EP use it in this manner to regulate a fixed voltage or current. The feedback enables this device to behave as an error amplifier, computing a portion of the output voltage and adjusting it to maintain the desired regulation. This is done by relating the output voltage back to the reference pin in a manner to make it equal to the internal reference voltage, which can be accomplished through resistive or direct feedback.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Figure 28 shows the TLVH431B-EP used in a 3.3-V isolated flyback supply. Output voltage V_O can be as low as reference voltage V_{REF} ($1.24 \text{ V} \pm 1\%$). The output of the regulator, plus the forward voltage drop of the optocoupler LED ($1.24 + 1.4 = 2.64 \text{ V}$), determine the minimum voltage that can be regulated in an isolated supply configuration. Regulated voltage as low as 2.7 Vdc is possible in the topology shown in Figure 28.

The TLVH431B-EP family of devices are prevalent in these applications, being designers go to choice for secondary side regulation. Due to this prevalence, this section explains operation and design in both states of TLVH431B-EP that this application will see, open loop (Comparator + V_{REF}) and closed loop (Shunt Regulator).

Further information about system stability and using a TLVH431B-EP device for compensation see *Compensation Design With TL431 for UCC28600*, [SLUA671](#).

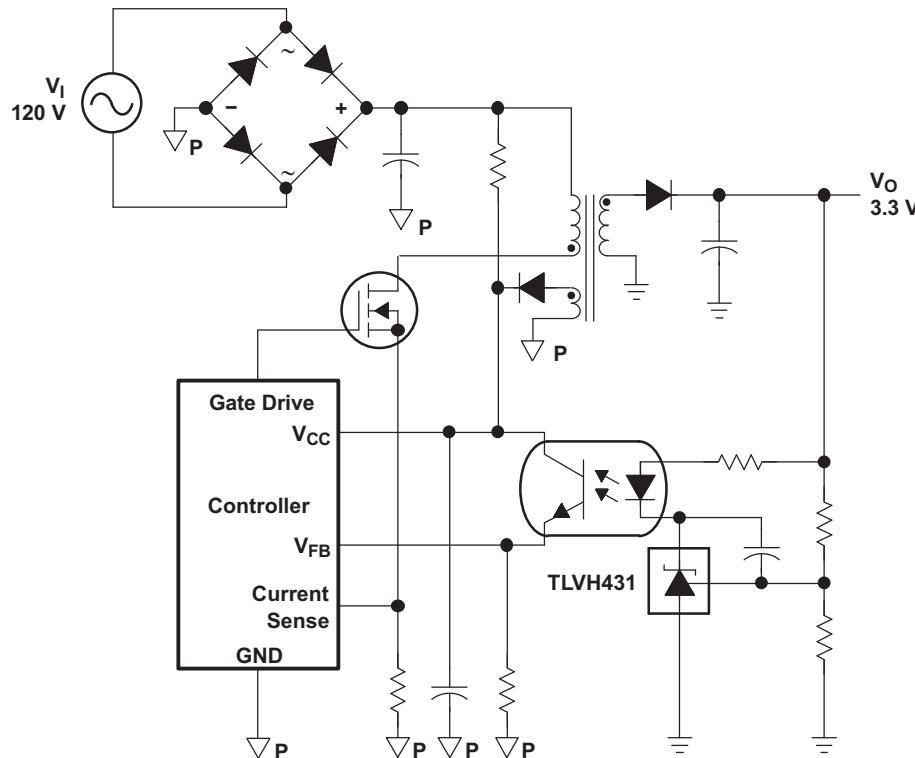


Figure 28. Flyback With Isolation Using TLVH431B-EP as Voltage Reference and Error Amplifier

9.2 Typical Applications

9.2.1 Comparator With Integrated Reference (Open Loop)

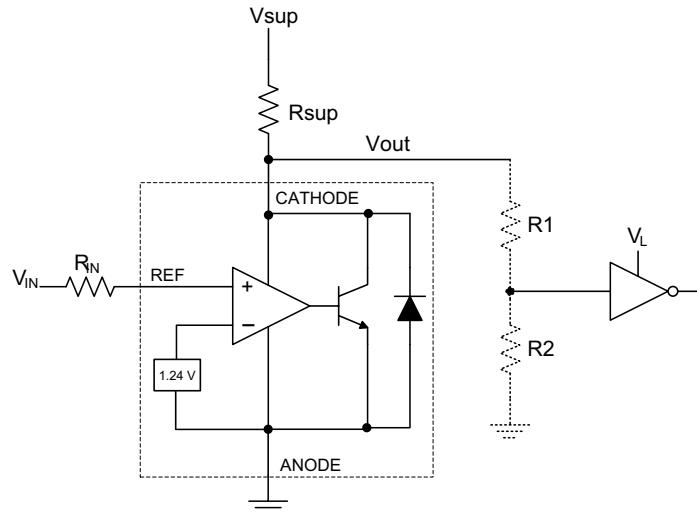


Figure 29. Comparator Application Schematic

9.2.1.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#) as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0 V to 5 V
Input Resistance	10 k Ω
Supply Voltage	9 V
Cathode Current (I_k)	500 μ A
Output Voltage Level	\sim 1 V – V_{sup}
Logic Input Thresholds V_{IH}/V_{IL}	V_L

9.2.1.2 Detailed Design Procedure

When using TLVH431B-EP as a comparator with reference, determine the following:

- Input voltage range
- Reference voltage accuracy
- Output logic input high and low level thresholds
- Current source resistance

9.2.1.2.1 Basic Operation

In the configuration shown in [Figure 29](#), TLVH431B-EP behaves as a comparator, comparing the V_{ref} pin voltage to the internal virtual reference voltage. When provided a proper cathode current (I_k), TLVH431B-EP will have enough open loop gain to provide a quick response. With the TLVH431B-EP's max Operating Current (I_{min}) being 100 μ A and up to 150 μ A over temperature, operation below that could result in low gain, leading to a slow response.

9.2.1.2.2 Overdrive

Slow or inaccurate responses can also occur when the reference pin is not provided enough overdrive voltage. This is the amount of voltage that is higher than the internal virtual reference. The internal virtual reference voltage will be within the range of $1.24\text{ V} \pm(0.5\%, 1.0\% \text{ or } 1.5\%)$ depending on which version is being used.

The more overdrive voltage provided, the faster the TLVH431B-EP will respond. See [Figure 30](#) and [Figure 31](#) for the output responses to various input voltages.

For applications where TLVH431B-EP is being used as a comparator, it is best to set the trip point greater than the positive expected error (that is, $+1.0\%$ for the A version). For fast response, setting the trip point to $> 10\%$ of the internal V_{ref} should suffice.

For minimal voltage drop or difference from V_{in} to the ref pin, it is recommended to use an input resistor $< 10\text{ k}\Omega$ to provide I_{ref} .

9.2.1.2.3 Output Voltage and Logic Input Level

In order for TLVH431B-EP to properly be used as a comparator, the logic output must be readable by the receiving logic device. This is accomplished by knowing the input high and low level threshold voltage levels, typically denoted by V_{IH} and V_{IL} .

As shown in [Figure 30](#) and [Figure 31](#), TLVH431B-EP's output low level voltage in open-loop/comparator mode is approximately 1 V, which is sufficient for some 3.3-V supplied logic. However, would not work for 2.5-V and 1.8-V supplied logic. To accommodate this a resistive divider can be tied to the output to attenuate the output voltage to a voltage legible to the receiving low-voltage logic device.

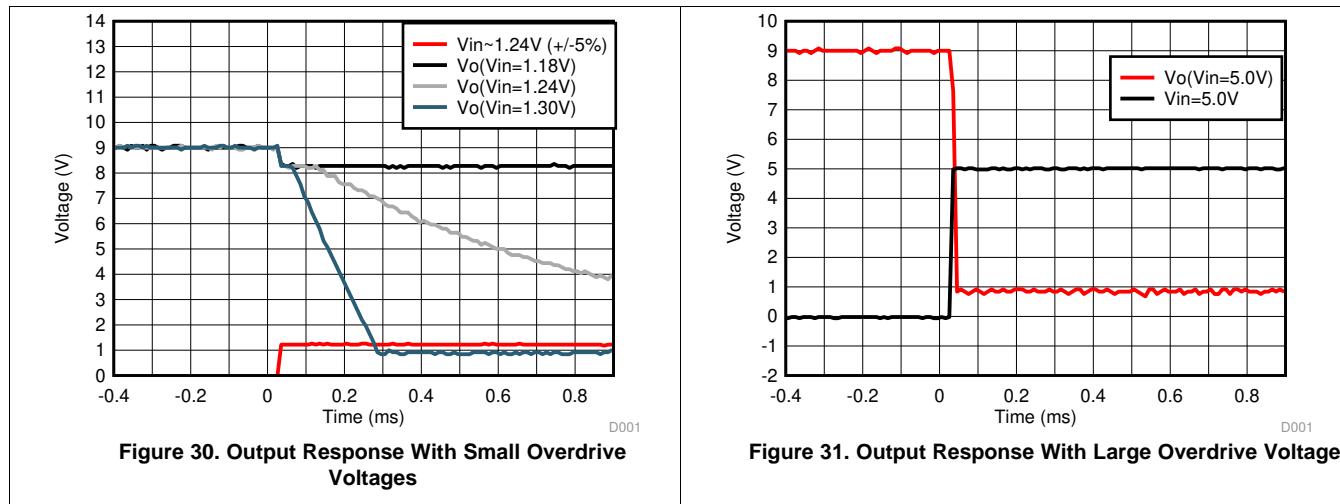
TLVH431B-EP's output high voltage is approximately V_{SUP} due to TLVH431B-EP being open-collector. If V_{SUP} is much higher than the receiving logic's maximum input voltage tolerance, the output must be attenuated to accommodate the outgoing logic's reliability.

When using a resistive divider on the output, be sure to make the sum of the resistive divider (R_1 and R_2 in [Figure 29](#)) is much greater than R_{SUP} in order to not interfere with TLVH431B-EP's ability to pull close to V_{SUP} when turning off.

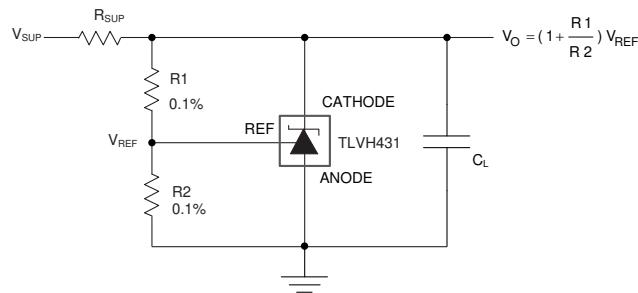
9.2.1.2.3.1 Input Resistance

TLVH431B-EP requires an input resistance in this application in order to source the reference current (I_{REF}) needed from this device to be in the proper operating regions while turning on. The actual voltage seen at the ref pin will be $V_{\text{REF}} = V_{\text{IN}} - I_{\text{REF}} \times R_{\text{IN}}$. Because I_{REF} can be as high as $0.5\text{ }\mu\text{A}$, TI recommends to use a resistance small enough that will mitigate the error that I_{REF} creates from V_{IN} .

9.2.1.3 Application Curves



9.2.2 Shunt Regulator/Reference



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Figure 32. Shunt Regulator Schematic

9.2.2.1 Design Requirements

For this design example, use the parameters listed in [Table 2](#) as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Reference Initial Accuracy	1.0%
Supply Voltage	6 V
Cathode Current (Ik)	500 μ A
Output Voltage Level	1.24 V - 18 V
Load Capacitance	100 nF
Feedback Resistor Values and Accuracy (R1 and R2)	10 k Ω

9.2.2.2 Detailed Design Procedure

When using TLVH431B-EP as a Shunt Regulator, determine the following:

- Input voltage range
- Temperature range
- Total accuracy
- Cathode current
- Reference initial accuracy
- Output capacitance

9.2.2.2.1 Programming Output/Cathode Voltage

To program the cathode voltage to a regulated voltage a resistive bridge must be shunted between the cathode and anode pins with the mid point tied to the reference pin. This can be seen in [Figure 32](#), with R1 and R2 being the resistive bridge. The cathode/output voltage in the shunt regulator configuration can be approximated by the equation shown in [Figure 32](#). The cathode voltage can be more accurately determined by taking in to account the cathode current:

$$V_O = (1 + R1 / R2) \times V_{REF} - I_{REF} \times R1$$

In order for this equation to be valid, TLVH431B-EP must be fully biased so that it has enough open loop gain to mitigate any gain error. This can be done by meeting the I_{min} spec denoted in the [Specifications](#) section.

9.2.2.2.2 Total Accuracy

When programming the output above unity gain ($V_{KA} = V_{REF}$), TLVH431B-EP is susceptible to other errors that may effect the overall accuracy beyond V_{REF} . These errors include:

- R1 and R2 accuracies
- $V_{I(\text{dev})}$ - Change in reference voltage over temperature
- $\Delta V_{\text{ref}} / \Delta V_{KA}$ - Change in reference voltage to the change in cathode voltage
- $|Z_{KA}|$ - Dynamic impedance, causing a change in cathode voltage with cathode current

Worst case, cathode voltage can be determined taking all of the variables in to account. The application note *Setting the Shunt Voltage on an Adjustable Shunt Regulator*, [SLVA445](#), assists designers in setting the shunt voltage to achieve optimum accuracy for this device.

9.2.2.2.3 Stability

Though TLVH431B-EP is stable with no capacitive load, the device that receives the shunt regulator's output voltage could present a capacitive load that is within the TLVH431B-EP region of stability, shown in [Figure 20](#), [Figure 21](#) and [Figure 22](#). Also, designers may use capacitive loads to improve the transient response or for power supply decoupling.

TI recommends to choose capacitors that will give a phase margin $> 5^\circ$ to assure stability of the TLVH431B-EP.

9.2.2.3 Application Curve

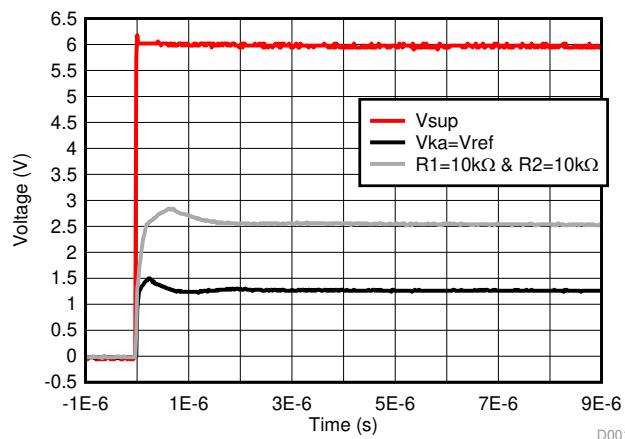


Figure 33. TLVH431B-EP Start-Up Response

10 Power Supply Recommendations

When using TLVH431B-EP as a Linear Regulator to supply a load, designers will typically use a bypass capacitor on the output/cathode pin. When doing this, be sure that the capacitance is within the stability criteria shown in [Figure 20](#), [Figure 21](#), and [Figure 22](#).

To not exceed the maximum cathode current, be sure that the supply voltage is current limited. Also, limit the current being driven into the Ref pin, as not to exceed its absolute maximum rating.

For applications shunting high currents, pay attention to the cathode and anode trace lengths, adjusting the width of the traces to have the proper current density.

11 Layout

11.1 Layout Guidelines

Place decoupling capacitors as close to the device as possible. Use appropriate widths for traces when shunting high currents to avoid excessive voltage drops.

11.2 Layout Example

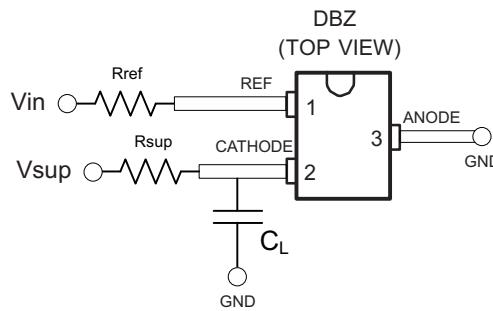


Figure 34. DBZ Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Compensation Design With TL431 for UCC28600*, [SLUA671](#)
- *Setting the Shunt Voltage on an Adjustable Shunt Regulator*, [SLVA445](#)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.4 Trademarks

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12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

[SLYZ022 — TI Glossary](#).

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLVH431BMDBZREP	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125		Samples
V62/19622-01XE	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

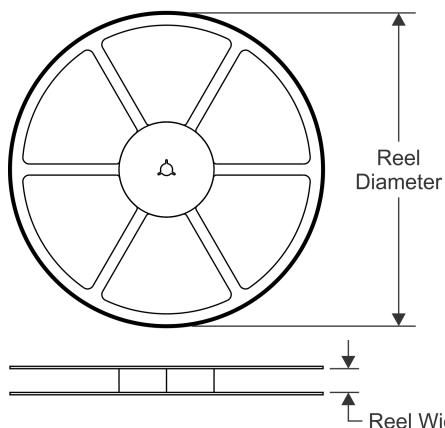
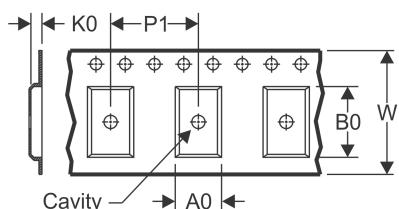
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLVH431B-EP :

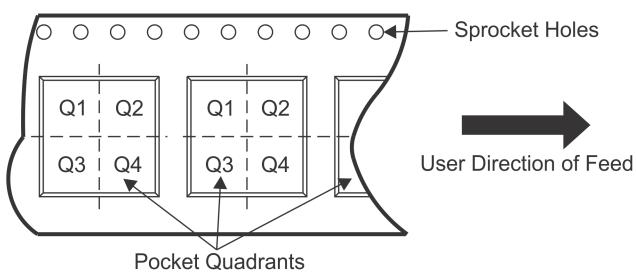
- Catalog: [TLVH431B](#)
- Automotive: [TLVH431B-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

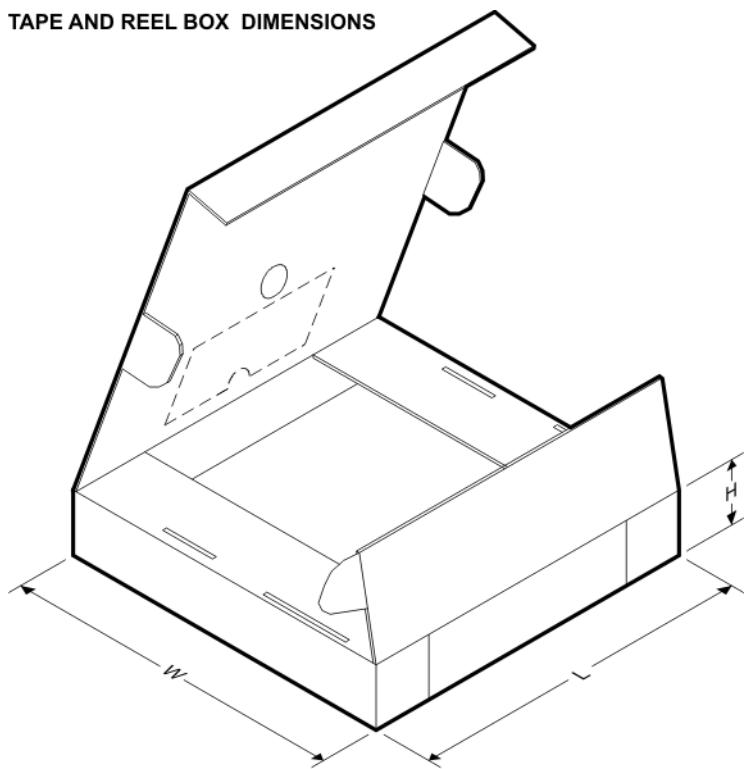
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLVH431BMDBZREP	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

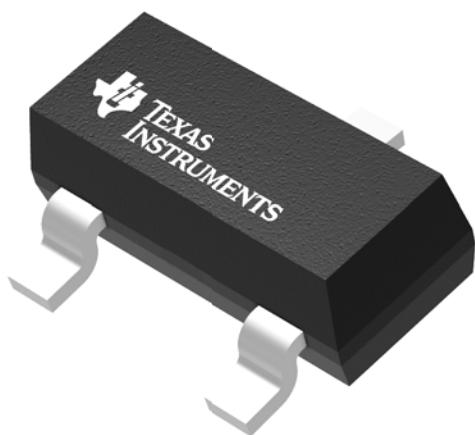
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLVH431BMDBZREP	SOT-23	DBZ	3	3000	213.0	191.0	35.0

GENERIC PACKAGE VIEW

DBZ 3

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203227/C

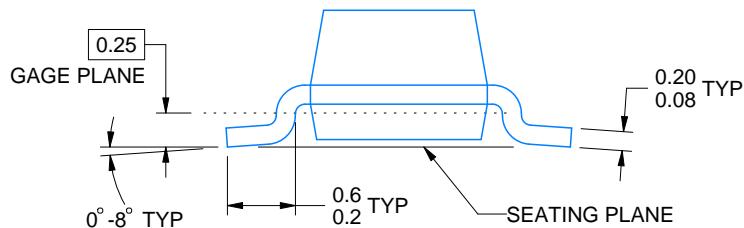
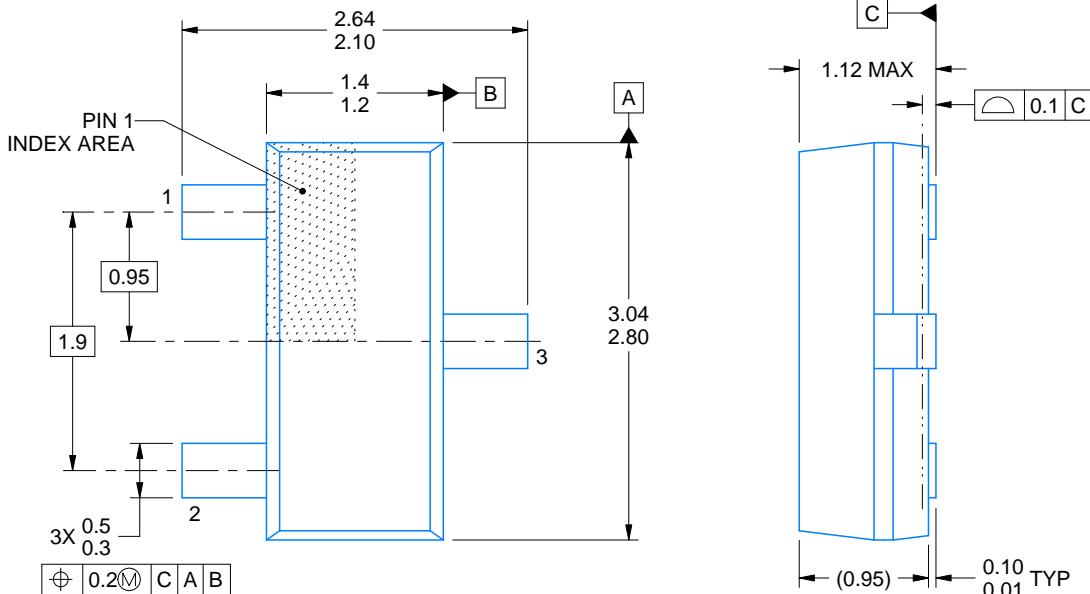
PACKAGE OUTLINE

DBZ0003A



SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



4214838/C 04/2017

NOTES:

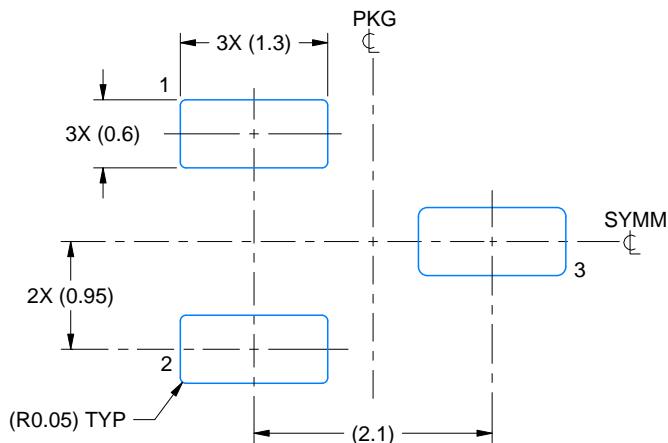
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.

EXAMPLE BOARD LAYOUT

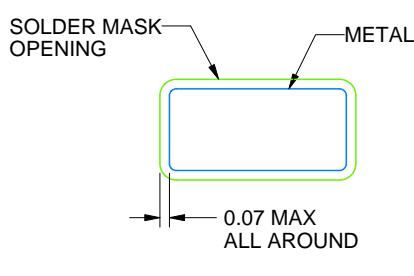
DBZ0003A

SOT-23 - 1.12 mm max height

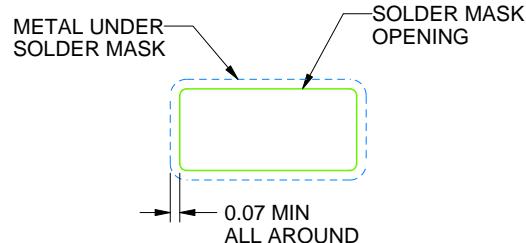
SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)



SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214838/C 04/2017

NOTES: (continued)

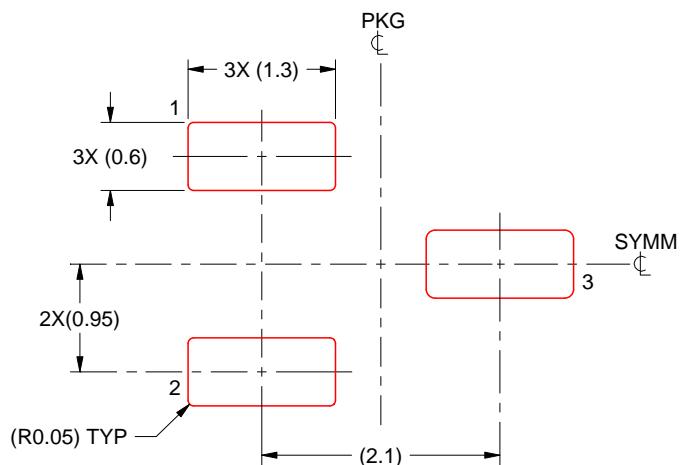
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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