具有 I²C 接口的 TPS55288-Q1 36V、16A 降压/升压转换器

1 特性

- 符合 AEC-Q100 标准：
  - 器件温度等级 1：–40°C 至 +125°C 环境工作温度范围
- 可编程电源 (PPS) 支持 USB 供电 (USB PD)
  - 宽输入电压范围：2.7V 至 36V
  - 可编程输出电压范围：0.8V 至 22V，步长为 20mV
  - ±1% 基准电压精度
  - 电缆上压降的可调输出电压补偿
  - 可编程输出电流限制高达 6.35A，步长为 50mA
  - ±5% 精密输出电流监测
  - I²C 接口
- 在整个负载范围内具有高效率
  - V_{IN} = 12V、V_{OUT} = 20V 且 I_{OUT} = 3A 时效率为 97%
  - 轻负载状态下的可编程 PFM 和 FPWM 模式
- 避免频率干扰和串扰
  - 可选的时钟同步
  - 可编程开关频率范围为 200kHz 至 2.2MHz
- 降低 EMI
  - 可选可编程扩展频谱
  - 无引线封装
- 丰富的保护特性
  - 输出过压保护
  - 利用断续模式实现输出短路保护
  - 热关断保护
  - 可编程平均电感器电流限制高达 16A
- 小解决方案尺寸
  - 开关频率高达 2.2MHz（最大值）
  - 具有可湿性侧面选项的 4.0mm × 3.5mm HotRod™ QFN 封装
- 使用 TPS55288-Q1 并借助 WEBENCH® Power Designer 创建定制设计方案

2 应用

- USB PD
- 汽车信息娱乐系统与仪表组
- 汽车充电器

3 说明

TPS55288-Q1 是一款同步四开关降压/升压转换器，能够将输出电压稳定在等于、高于或低于输入电压的某一电压值上。TPS55288-Q1 在 2.7V 至 36V 的宽输入电压范围内工作，可输出 0.8V 至 22V 电压以支持各种不同的应用。

TPS55288-Q1 集成了两个 16A MOSFET，其中的升压桥臂可实现解决方案尺寸和效率间的平衡。通过 I²C 接口对输出电压和输出电流限制进行编程，TPS55288-Q1 完全符合 USB PD 规范。TPS55288-Q1 能够通过 12V 输入电压提供 100W 的功率。

TPS55288-Q1 采用平均电流模式控制方案。开关频率可通过外部电阻在 200kHz 至 2.2MHz 之间进行编程，并且可与外部时钟同步。TPS55288-Q1 还提供可选的扩频，从而更大限度地减少峰值 EMI。

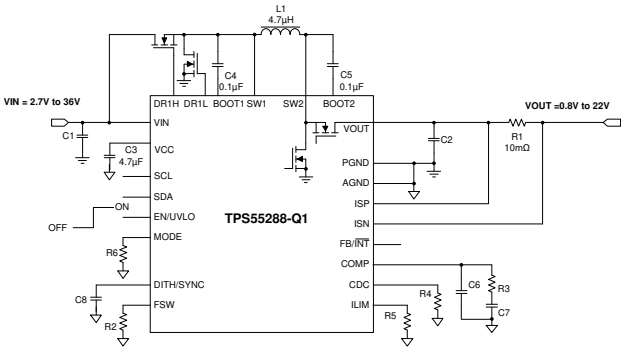
TPS55288-Q1 提供输出过压保护、平均电感器电流限制、逐周期峰值电流限制和输出短路保护。TPS55288-Q1 还使用持续过载情况下的可选输出电流限制和断续模式保护来确保安全运行。

TPS55288-Q1 可以使用具有高开关频率的小型电感器和电容器。此器件采用 4.0mm × 3.5mm QFN 封装。

器件信息

器件型号	封装(1)	封装尺寸
TPS55288-Q1	VQFN-HR	4.00mm × 3.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用电路

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Changes from Revision * (December 2020) to Revision A (December 2021)	Page
• 添加了可湿性侧面选项	1

5 Pin Configuration and Functions

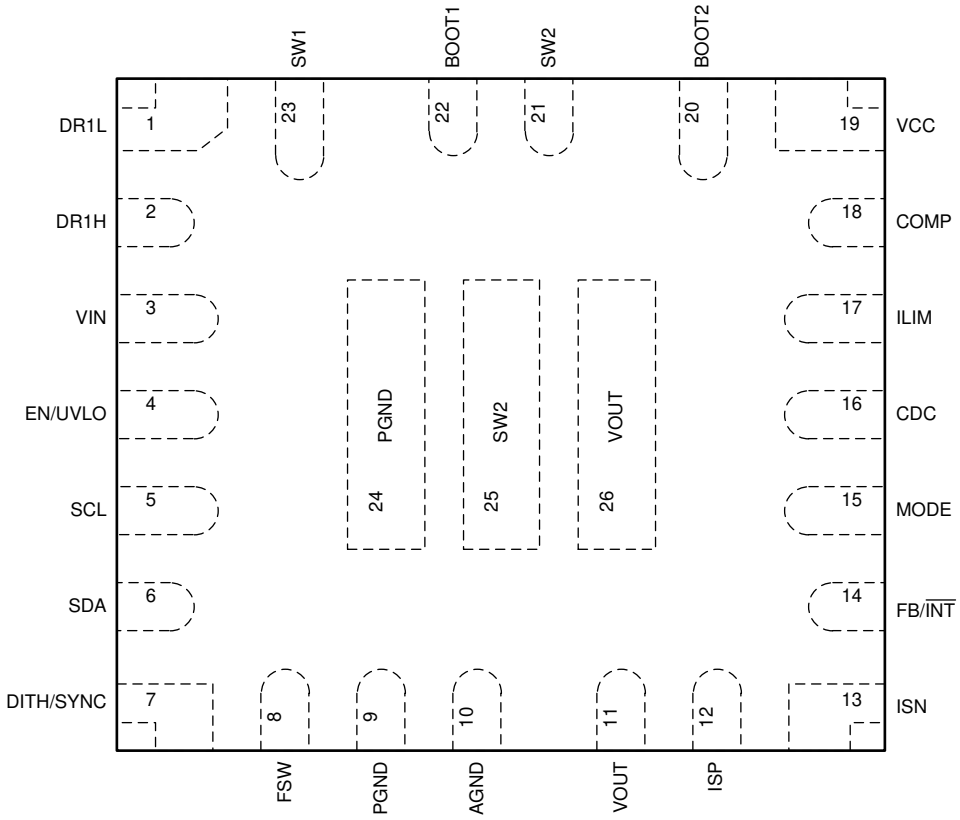


图 5-1. 26-pin VQFN-HR, RPM Package (Transparent Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	DR1L	O	Gate driver output for low-side MOSFET in buck side
2	DR1H	O	Gate driver output for high-side MOSFET in buck side
3	VIN	PWR	Input power supply for the IC
4	EN/UVLO	I	Enable logic input and programmable input voltage undervoltage lockout (UVLO) input. Logic high level enables the device. Logic low level disables the device and turns it into shutdown mode. After the voltage at the EN/UVLO pin is above the logic high voltage of 1.15 V, this pin acts as programmable UVLO input with 1.23-V internal reference.
5	SCL	I	Clock of I^2C interface
6	SDA	I/O	Data of I^2C interface
7	DITH/SYNC	I	Dithering frequency setting and synchronous clock input. Use a capacitor between this pin and ground to set the dithering frequency. When this pin is short to ground or pulled above 1.2 V, there is no dithering function. An external clock can be applied at this pin to synchronize the switching frequency.
8	FSW	O	The switching frequency is programmed by a resistor between this pin and the AGND pin.
9, 24	PGND	PWR	Power ground of the IC. It is connected to the source of the low-side MOSFET.
10	AGND	PWR	Signal ground of the IC
11, 26	VOUT	PWR	Output of the buck-boost converter
12	ISP	I	Positive input of the current sense amplifier. An optional current sense resistor connected between the ISP pin and the ISN pin can limit the output current. If the sensed voltage reaches the current limit setting value in the register, a slow constant current control loop becomes active and starts to regulate the voltage between the ISP pin and the ISN pin. Connecting the ISP pin and the ISN pin together with the VOUT pin can disable the output current limit function.

表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
13	ISN	I	Negative input of the current sense amplifier. An optional current sense resistor connected between the ISP pin and the ISN pin can limit the output current. If the sensed voltage reaches the current limit setting value in the register, a slow constant current control loop becomes active and starts to regulate the voltage between the ISP pin and the ISN pin. Connecting the ISP pin and the ISN pin together with the VOUT pin can disable the output current limit function.
14	FB/$\overline{\text{INT}}$	I/O	When the device is set to use external output voltage feedback, connect to the center tap of a resistor divider to program the output voltage. When the device is set to use internal feedback, this pin is a fault indicator output. When there is an internal fault happening, this pin outputs logic low level.
15	MODE	I	Set the operation modes of the TPS55288-Q1 by a resistor between this pin and AGND to select PFM mode, forced PWM mode in light load condition to select the internal LDO, or external 5 V for VCC, and to select different I^2C address.
16	CDC	O	Voltage output proportional to the sensed voltage between the ISP pin and the ISN pin. Use a resistor between this pin and AGND to increase the output voltage to compensate voltage droop across the cable caused by the cable resistance.
17	ILIM	O	Average inductor current limit setting pin. Connect an external resistor between this pin and the AGND pin.
18	COMP	I	Output of the internal error amplifier. Connect the loop compensation network between this pin and the AGND pin.
19	VCC	O	Output of the internal regulator. A ceramic capacitor of more than 4.7 μF is required between this pin and the AGND pin.
20	BOOT2	O	Power supply for high-side MOSFET gate driver in boost side. A ceramic capacitor of 0.1 μF must be connected between this pin and the SW2 pin.
21, 25	SW2	I	The switching node pin of the boost side. It is connected to the drain of the internal low-side power MOSFET and the source of internal high-side power MOSFET.
22	BOOT1	I	Power supply for high-side MOSFET gate driver in buck side. A ceramic capacitor of 0.1 μF must be connected between this pin and the SW1 pin.
23	SW1	I	The switching node pin of the buck side. It is connected to the drain of the external low-side power MOSFET and the source of external high-side power MOSFET.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range at terminals(2)	VIN, SW1	– 0.3	40	V
	DRH1, BOOT1	SW1 – 0.3	SW1+6	V
	VCC, DRL1, SCL, SDA, ILIM, FSW, COMP, FB/$\overline{\text{INT}}$, MODE, CDC, DITH/SYNC	– 0.3	6	V
	VOUT, SW2, ISP, ISN	– 0.3	25	V
	ISP, ISN	VOUT-6	VOUT+6	V
	EN	-0.3	20	V
	BOOT2	SW2 – 0.3	SW2+6	V
	DRL1, SCL, SDA, ILIM, FSW, COMP, FB/$\overline{\text{INT}}$, MODE, CDC, DITH/SYNC	– 0.3	VCC+0.3	V
T_J	Operating Junction, T_J (3)	– 40	150	°C
T_{stg}	Storage temperature	– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(2)	±2000	V
		Charged-device model (CDM), per AEC Q100-011, all pins(3)	±500	
$V_{(ESD)}$ (1)	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-011, corner pins(3)	±750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.7		36	V
V_{OUT}	Output voltage range	0.8		22	V
L	Effective inductance range	0.7	4.7	13	µH
C_{IN}	Effective input capacitance range	4.7	22		µF
C_{OUT}	Effective output capacitance range	10	100	1000	µF
T_J	Operating junction temperature	– 40		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS55288-Q1 VQFN-HR (RPM)-26 PINS Standard	TPS55288-Q1 VQFN-HR (RPM)-26 PINS EVM(2)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.5	25.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.8	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.8	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	12.7	11.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.8	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Measured on TPS55288-Q1EVM-045, 4-layer, 2-oz/2-oz/2-oz/2-oz copper 112-mm×71-mm PCB.

6.5 Electrical Characteristics

T_J = -40°C to 125°C, V_{IN} = 12 V and V_{OUT} = 20 V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2.7		36	V
V_{VIN_UVLO}	Under voltage lockout threshold	V_{IN} rising	2.8	2.9	3.0	V
		V_{IN} falling	2.6	2.65	2.7	V
I_Q	Quiescent current into the VIN pin	IC enabled, no load, no switching. V_{IN} = 3 V to 24 V, V_{OUT} = 0.8 V, V_{FB} = V_{REF} + 0.1 V, R_{FSW} = 100 kΩ, T_J up to 125°C		760	860	μA
	Quiescent current into the VOUT pin	IC enabled, no load, no switching, V_{IN} = 2.9 V, V_{OUT} = 3 V to 20 V, V_{FB} = V_{REF} + 0.1 V, R_{FSW} = 100 kΩ, T_J up to 125°C		760	860	μA
I_{SD}	Shutdown current into the VIN pin	IC disabled, V_{IN} = 2.9 V to 14 V, T_J up to 125°C		6.8	10	μA
V_{CC}	Internal regulator output	I_{VCC} = 50 mA, V_{IN} = 8 V, V_{OUT} = 20 V	5.0	5.2	5.4	V
V_{CC_DO}	VCC dropout	V_{IN} = 5.0 V, V_{OUT} = 20 V, I_{VCC} = 60 mA		200	320	mV
		V_{IN} = 14 V, V_{OUT} = 5.0 V, I_{VCC} = 60 mA		110	170	mV
EN/UVLO						
V_{EN_H}	EN Logic high threshold	V_{CC} = 2.7 V to 5.5 V			1.15	V
V_{EN_L}	EN Logic low threshold	V_{CC} = 2.7 V to 5.5 V	0.4			V
V_{EN_HYS}	Enable threshold hysteresis	V_{CC} = 2.7 V to 5.5 V	0.05	0.12		V
V_{UVLO}	UVLO rising threshold at the EN/UVLO pin	V_{CC} = 3.0 V to 5.5 V	1.20	1.23	1.26	V
V_{UVLO_HYS}	UVLO threshold hysteresis	V_{CC} = 3.0 V to 5.5 V	8	14	20	mV
I_{UVLO}	Sourcing current at the EN/UVLO pin	$V_{EN/UVLO}$ = 1.3 V	4.5	5	5.5	μA
OUTPUT						
V_{OUT}	Output voltage range		0.8		22	V
V_{OVP}	Output overvoltage protection threshold		22.5	23.5	24.5	V
V_{OVP_HYS}	Over voltage protection hysteresis			1		V
I_{FB_LKG}	Leakage current at the FB pin	T_J up to 125°C			100	nA
I_{VOUT_LKG}	Leakage current into the VOUT pin	IC disabled, V_{OUT} = 20 V, V_{SW2} = 0 V, T_J up to 125°C		1	20	μA

6.5 Electrical Characteristics (continued)

T_J = -40°C to 125°C, V_{IN} = 12 V and V_{OUT} = 20 V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DISCHG}	Output discharge current	V_{OUT} = 20 V, V_{CC} = 5.2 V	40	100	170	mA
INTERNAL REFERENCE DAC						
	Resolution of reference voltage DAC			10		bits
INL	Integral non-linearity		-4		4	LSB
DNL	Differential non-linearity		-1		2	LSB
V_{OUT_FULL}	Output voltage when V_{REF} is set to 1.129V	VOUT_FS=03h, REF=03C0h, V_{REF} = 1.129 V	19.7	20	20.3	V
		VOUT_FS=02h, REF=03C0h, V_{REF}=1.129V	14.78	15	15.22	V
		VOUT_FS=01h, REF=03C0h, V_{REF} = 1.129 V	9.85	10	10.15	V
		VOUT_FS=00h, REF=03C0h, V_{REF} = 1.129 V	4.93	5	5.07	V
V_{OUT_ZERO}	Output voltage when V_{REF} is set to 45mV	VOUT_FS=03h, REF=0000h, V_{REF} = 45 mV	0.74	0.8	0.86	V
		VOUT_FS=02h, REF=0000h, V_{REF} = 45 mV	0.56	0.6	0.64	V
		VOUT_FS=01h, REF=0000h, V_{REF} = 45 mV	0.37	0.4	0.43	V
		VOUT_FS=00h, REF=0000h, V_{REF} = 45 mV	0.18	0.2	0.22	V
REFERENCE VOLTAGE						
V_{REF}	Reference voltage at the FB/$\overline{INT}$ pin when using external feedback	External feedback with REF=03C0h	1.117	1.129	1.141	V
		External feedback with REF=02C6h	0.837	0.846	0.855	V
		External feedback with REF=019Ah	0.502	0.508	0.514	V
		External feedback with REF=00D2h	0.276	0.282	0.288	V
POWER SWITCH						
$R_{DS(on)}$	Low-side MOSFET on resistance on boost side	V_{OUT} = 20 V, V_{CC}= 5.2 V		7.1		mΩ
	High-side MOSFET on resistance on boost side	V_{OUT} = 20 V, V_{CC}= 5.2 V		7.6		mΩ
INTERNAL CLOCK						
f_{SW}	Switching frequency	R_{FSW} = 100 kΩ	180	200	220	kHz
		R_{FSW} = 9.09 kΩ	2000	2200	2400	kHz
t_{OFF_min}	Min. off time	Boost mode		100	145	ns
t_{ON_min}	Min. on time	Buck mode		90	130	ns
V_{FSW}	Voltage at the FSW pin			1		V
CURRENT LIMIT						
I_{LIM_AVG}	Average inductor current limit	R_{ILIM} = 20 kΩ, V_{IN} = 8 V, V_{OUT} = 20 V, f_{SW} = 400 kHz, FPWM	14	16.5	19	A
		R_{ILIM} = 20 kΩ, V_{IN} = 8 V, V_{OUT} = 20 V, f_{SW} = 400 kHz, PFM	14	16.5	19	A
		R_{ILIM} = 60 kΩ, V_{IN} = 5 V, V_{OUT} = 14 V, f_{SW} = 2.2 MHz, FPWM	4	5.5		A
		R_{ILIM} = 60 kΩ, V_{IN} = 5 V, V_{OUT} = 14 V, f_{SW} = 2.2 MHz, PFM	4	5.5		A

6.5 Electrical Characteristics (continued)

T_J = -40°C to 125°C, V_{IN} = 12 V and V_{OUT} = 20 V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LIM_PK}	Peak inductor current limit at high side	R_{ILIM} = 20 kΩ, V_{IN} = 8 V, V_{OUT} = 20 V, f_{SW} = 400 kHz, FPWM		25		A
		R_{ILIM} = 20 kΩ, V_{IN} = 8 V, V_{OUT} = 20 V, f_{SW} = 400 kHz, PFM		25		A
V_{ILIM}	Voltage at the ILIM pin	VOUT = 3 V		0.6		V
V_{SNS}	Current loop regulation voltage between the ISP and ISN pins	V_{ISN} = 2 V to 21 V,IOUT_LIMIT Register = 11100100b	48	50	52	mV
		V_{ISN} = 2 V to 21 V,IOUT_LIMIT Register = 10111100b	28	30	32	mV
CABLE VOLTAGE DROOP COMPENSATION						
V_{CDC}	Voltage at the CDC pin	R_{CDC} = 20 kΩ or floating, V_{ISP} – V_{ISN} = 50 mV	0.95	1	1.05	V
		R_{CDC} = 20 kΩ or floating, V_{ISP} – V_{ISN} = 2 mV		40	75	mV
V_{OUT_CDC}	VOUT increase for cable droop compensation	Internal output feedback, CDC[2:0]=111, V_{ISP} – V_{ISN} = 50 mV	650	700	750	mV
		Internal output feedback, CDC[2:0]=111, V_{ISP} – V_{ISN} = 2 mV		30	60	mV
		Internal output feedback, CDC[2:0]=001, V_{ISP} – V_{ISN} = 50 mV	70	100	130	mV
		Internal output feedback, CDC[2:0]=001, V_{ISP} – V_{ISN} = 10 mV		20	40	mV
I_{FB_CDC}	FB/$\overline{INT}$ pin sinking current	External output feedback, R_{CDC} = 20kΩ, V_{ISP} – V_{ISN} = 50 mV	7.23	7.5	7.87	µA
		External output feedback, R_{CDC} = 20 kΩ, V_{ISP} – V_{ISN} = 0 mV		0.05	0.32	µA
		External output feedback, R_{CDC} = floating, V_{ISP} – V_{ISN} = 50 mV		0	0.3	µA
ERROR AMPLIFIER						
I_{SINK}	COMP pin sink current	V_{FB} = V_{REF} + 400 mV, V_{COMP} = 1.5 V, V_{CC} = 5 V		20		µA
I_{SOURCE}	COMP pin source current	V_{FB} = V_{REF} - 400 mV, V_{COMP} = 1.5 V, V_{CC} = 5 V		60		µA
V_{CCLPH}	High clamp voltage at the COMP pin			1.8		V
V_{CCLPL}	Low clamp voltage at the COMP pin			0.7		V
G_{EA}	Error amplifier transconductance			190		µA/V
SOFT START						
t_{SS}	Soft-start time		3	4	5	ms
DR1H GATE DRIVER						
V_{DR1H_L}	Low-state voltage drop	V_{DR1H} – V_{SW1}, 100-mA sinking		0.1		V
V_{DR1H_H}	High-state voltage drop	V_{BOOT1} – V_{DR1H}, 100-mA sourcing		0.2		V
DR1L GATE DRIVER						
V_{DR1L_L}	Low-state voltage drop	100-mA sinking		0.1		V
V_{DR1L_H}	High-state voltage drop	V_{CC} – V_{DR1L}, 100-mA sourcing		0.2		V
SPREAD SPECTRUM						
I_{DITH_CHG}	Dithering charge current	$V_{DITH/SYNC}$ = 1.0 V, R_{FSW} = 49.9 kΩ, voltage rising from 0.85 V		2		µA
I_{DITH_DIS}	Dithering discharge current	$V_{DITH/SYNC}$ = 1.0 V, R_{FSW} = 49.9 kΩ, voltage falling from 1.15 V		2		µA

6.5 Electrical Characteristics (continued)

T_J = -40°C to 125°C, V_{IN} = 12 V and V_{OUT} = 20 V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DITH_H}	Dither high threshold			1.07		V
V_{DITH_L}	Dither low threshold			0.93		V
SYNCHRONOUS CLOCK						
V_{SNYC_H}	Sync clock high voltage threshold				1.2	V
V_{SYNC_L}	Sync clock low voltage threshold		0.4			V
t_{SYNC_MIN}	Minimum sync clock pulse width		50			ns
HICCUP						
t_{HICCUP}	Hiccup off time			76		ms
MODE RESISTANCE DETECTION						
I_{MODE}	Sourcing current from the MODE pin	V_{MODE} = 2.5 V	9	10	11	µA
V_{MODE_DT1}	Detection threshold voltage at the MODE pin		1.147	1.220	1.293	V
V_{MODE_DT2}			0.824	0.88	0.936	V
V_{MODE_DT3}			0.571	0.614	0.657	V
V_{MODE_DT4}			0.321	0.351	0.381	V
V_{MODE_DT5}			0.168	0.189	0.210	V
V_{MODE_DT6}			0.080	0.097	0.114	V
V_{MODE_DT7}			0.014	0.027	0.040	V
LOGIC INTERFACE						
V_{I2C_IO}	IO voltage range for I^2C		1.7		5.5	V
V_{I2C_H}	I^2C input high threshold	V_{CC} = 2.7 V to 5.5 V			1.2	V
V_{I2C_L}	I^2C input low threshold	V_{CC} = 2.7 V to 5.5 V	0.4			V
$I_{FB/\overline{INT}\_H}$	Leakage current into FB/$\overline{INT}$ pin when outputting high impedance	$V_{FB/\overline{INT}}$ = 5 V			100	nA
$V_{FB/\overline{INT}\_L}$	Output low voltage range of the FB/$\overline{INT}$ pin	Sinking 4-mA current		0.03	0.1	V
PROTECTION						
T_{SD}	Thermal shutdown threshold	T_J rising		175		°C
T_{SD_HYS}	Thermal shutdown hysteresis	T_J falling below TSD		20		°C

6.6 I^2C Timing Characteristics

T_J = -40°C to 125°C, V_{IN} = 12 V and V_{OUT} = 20 V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I^2C TIMING						
f_{SCL}	SCL clock frequency		100		1000	kHz
t_{BUF}	Bus free time between a STOP and START condition	Fast mode plus	0.5			µs
$t_{HD(STA)}$	Hold time (repeated) START condition		260			ns
t_{LOW}	Low period of the SCL clock		0.5			µs
t_{HIGH}	High period of the SCL clock		260			ns
$t_{SU(STA)}$	Setup time for a repeated START condition		260			ns
$t_{SU(DAT)}$	Data setup time		50			ns
$t_{HD(DAT)}$	Data hold time		0			µs
t_{RCL}	Rise time of SCL signal				120	ns

T_J = -40°C to 125°C, V_{IN} = 12 V and V_{OUT} = 20 V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an ACK bit				120	ns
t_{FCL}	Fall time of SCL signal				120	ns
t_{RDA}	Rise time of SDA signal				120	ns
t_{FDA}	Fall time of SDA signal				120	ns
$t_{SU(STO)}$	Setup time of STOP condition		260			ns
C_B	Capacitive load for SDA and SCL				200	pF

6.7 Typical Characteristics

V_{IN} = 12 V, T_A = 25°C, f_{SW} = 400 kHz, unless otherwise noted.

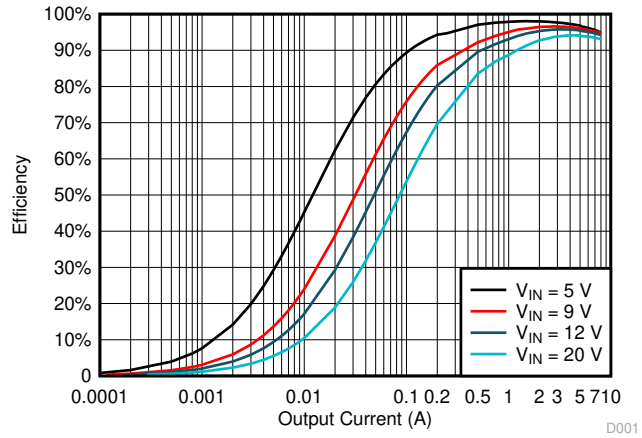


图 6-1. Efficiency vs Output Current, V_{OUT} = 5 V, FPWM

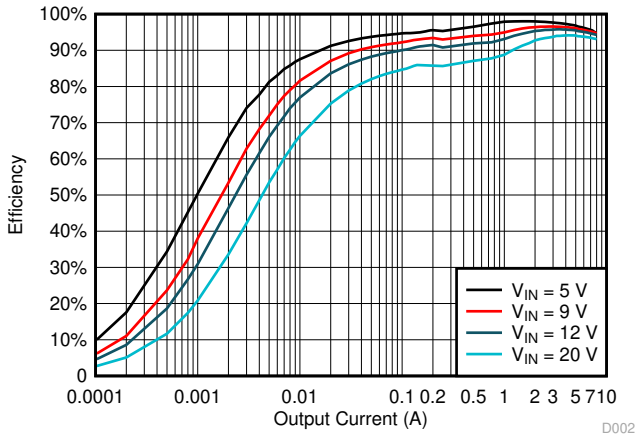


图 6-2. Efficiency vs Output Current, V_{OUT} = 5 V, PFM

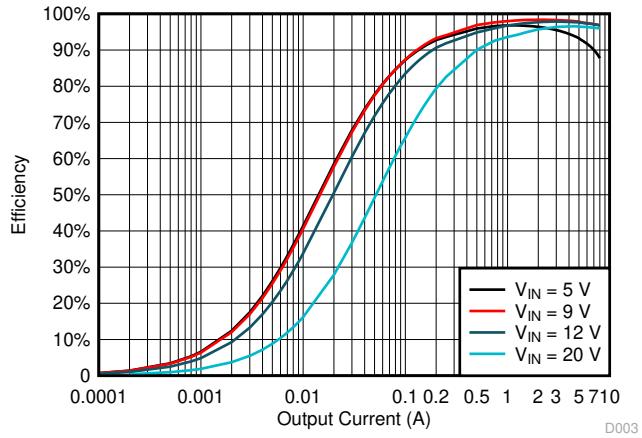


图 6-3. Efficiency vs Output Current, V_{OUT} = 9 V, FPWM

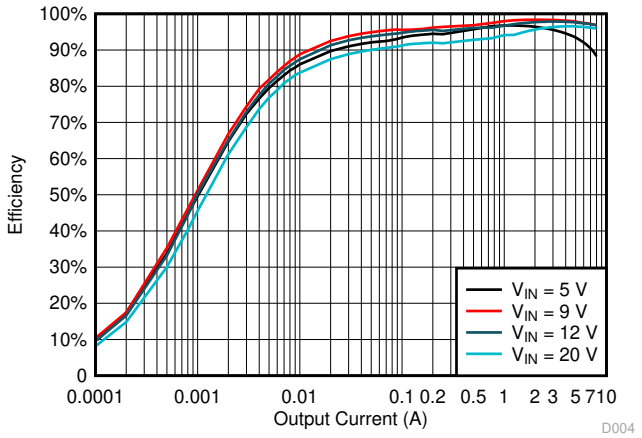


图 6-4. Efficiency vs Output Current, V_{OUT} = 9 V, PFM

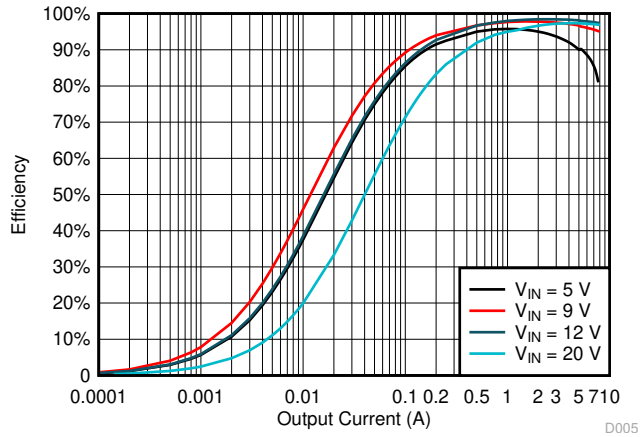


图 6-5. Efficiency vs Output Current, V_{OUT} = 12 V, FPWM

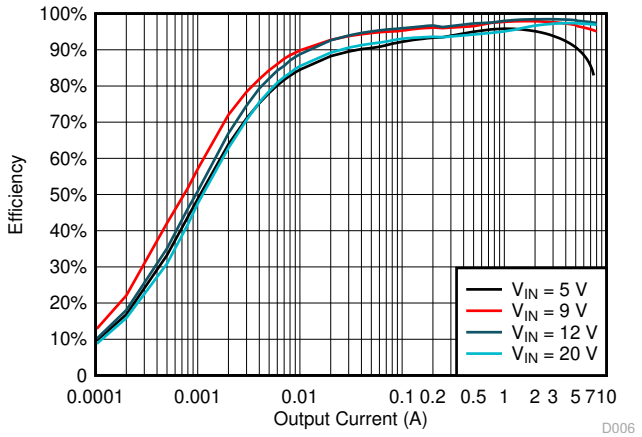


图 6-6. Efficiency vs Output Current, V_{OUT} = 12 V, PFM

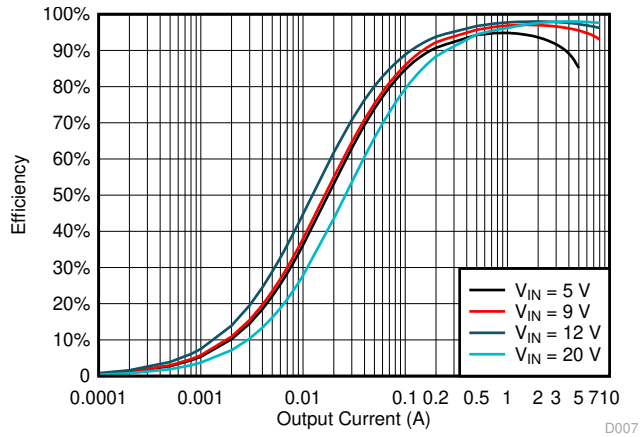


图 6-7. Efficiency vs Output Current, V_{OUT} = 15 V, FPWM

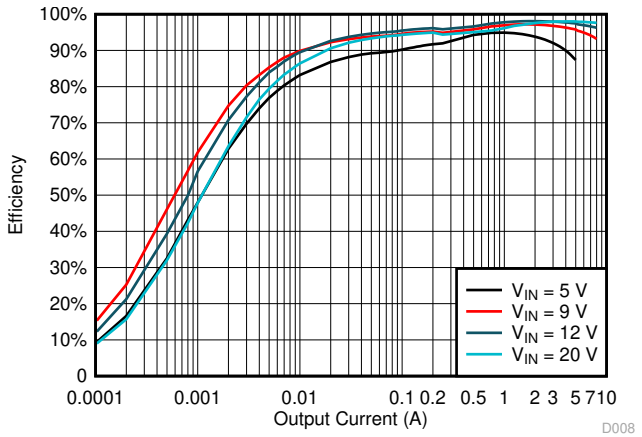


图 6-8. Efficiency vs Output Current, V_{OUT} = 15 V, PFM

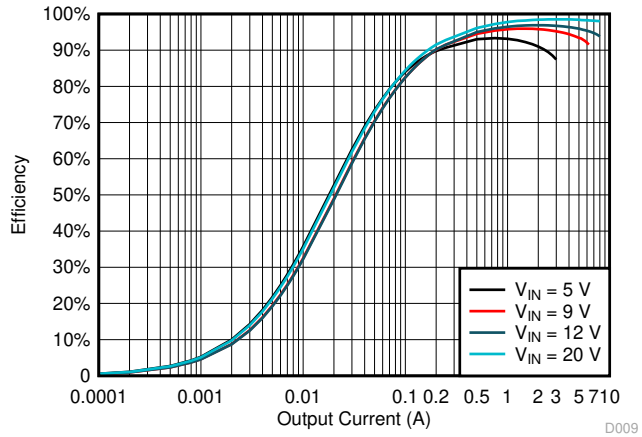


图 6-9. Efficiency vs Output Current, V_{OUT} = 20 V, FPWM

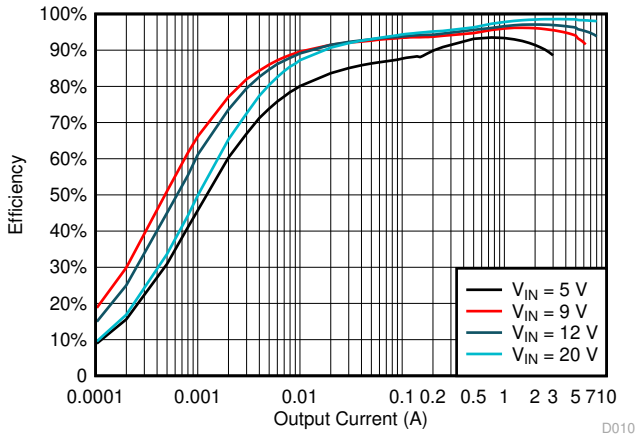


图 6-10. Efficiency vs Output Current, V_{OUT} = 20 V, PFM

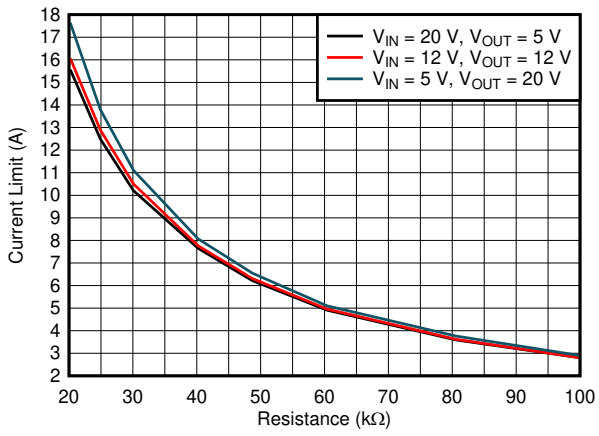


图 6-11. Average Inductor Current Limit vs Setting Resistance

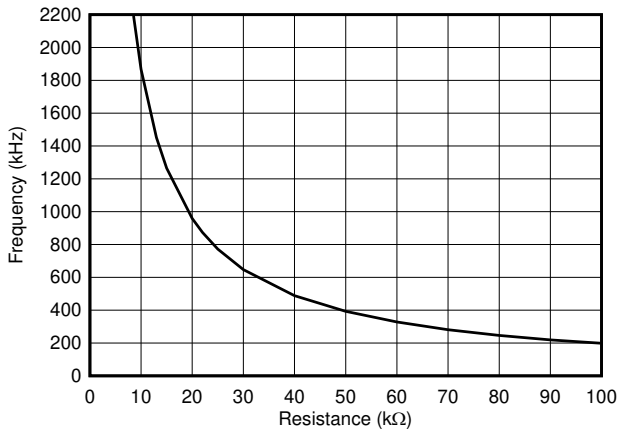


图 6-12. Switching Frequency vs Setting Resistance

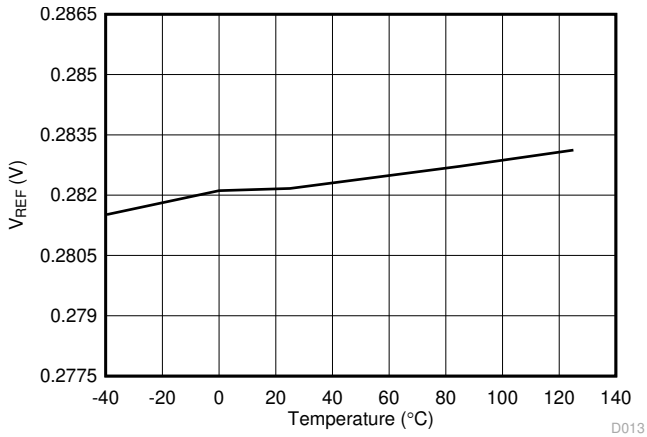


图 6-13. Reference Voltage vs Temperature (V_{REF} = 0.282 V)

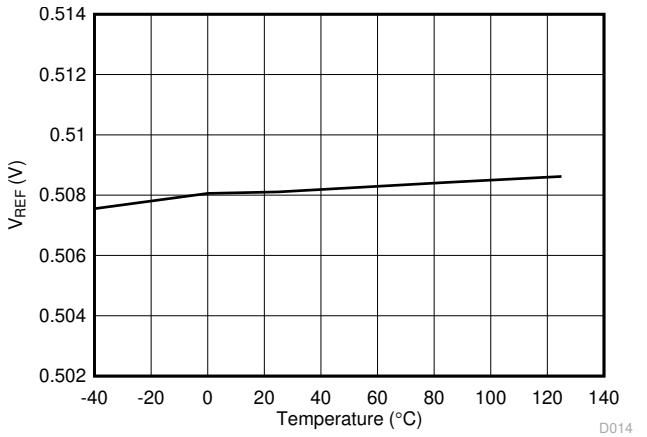


图 6-14. Reference Voltage vs Temperature (V_{REF} = 0.508 V)

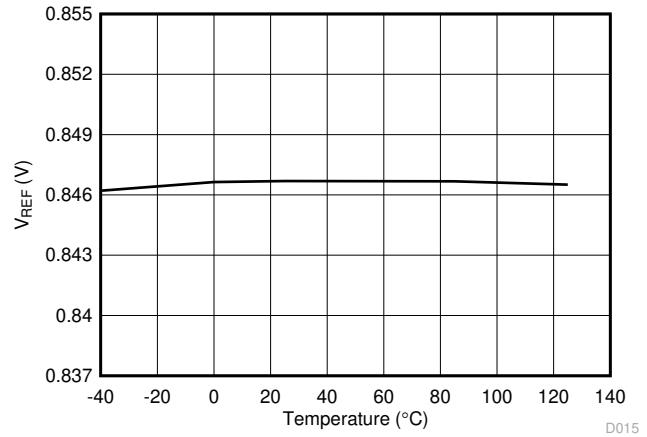


图 6-15. Reference Voltage vs Temperature (V_{REF} = 0.846 V)

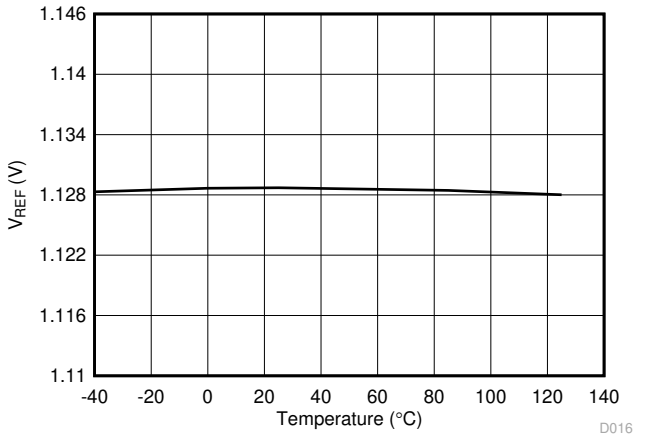


图 6-16. Reference Voltage vs Temperature (V_{REF} = 1.129 V)

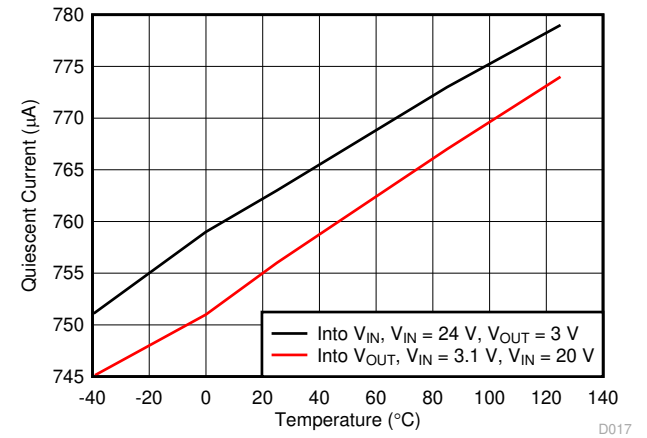


图 6-17. Quiescent Current vs Temperature

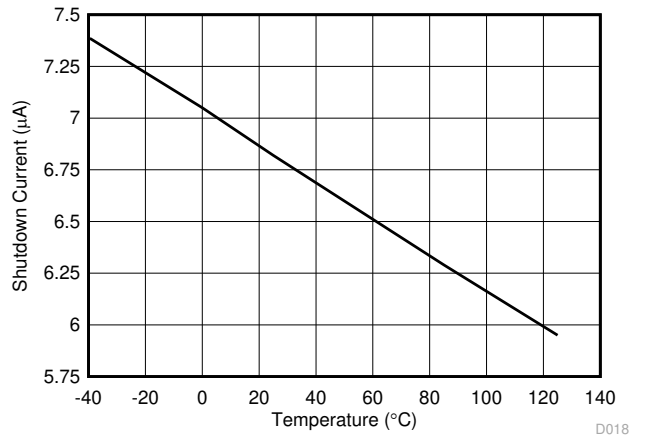


图 6-18. Shutdown Current vs Temperature

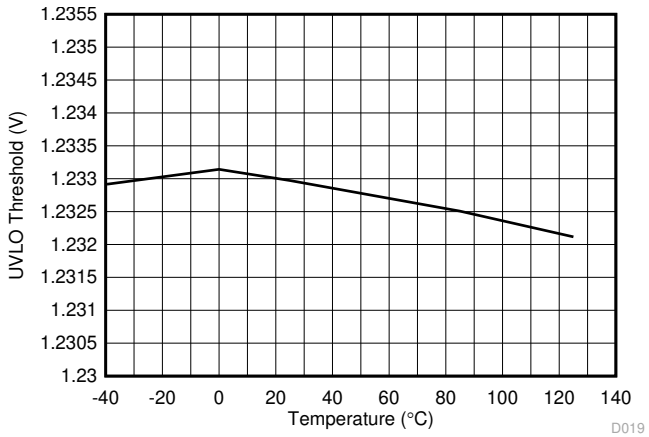


图 6-19. ENABLE/UVLO Rising Threshold vs Temperature

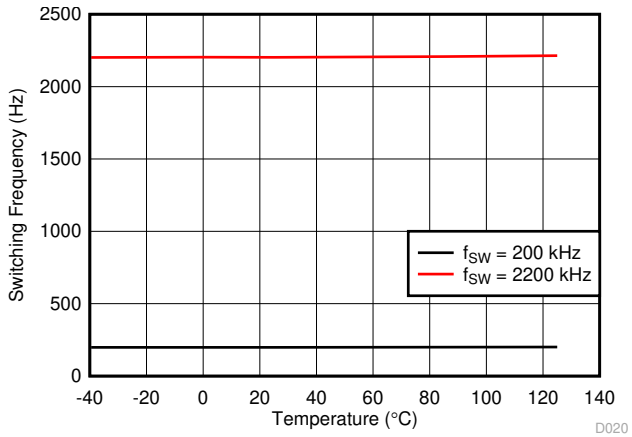


图 6-20. Switching Frequency vs Temperature

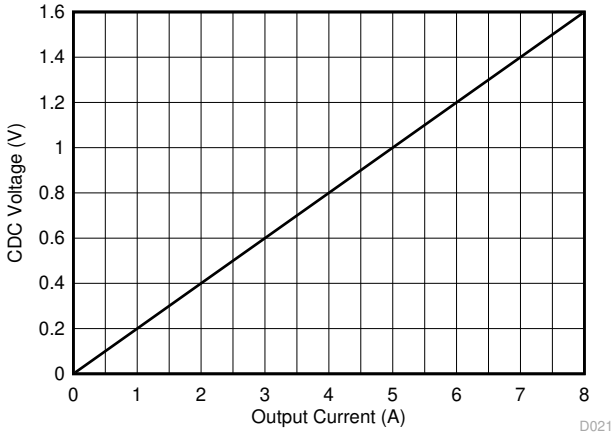


图 6-21. CDC Voltage vs Output Current with R_{SENSE} = 10 mΩ

7 Detailed Description

7.1 Overview

The TPS55288-Q1 is a 16-A buck-boost DC-to-DC converter with the two boost MOSFETs integrated. The TPS55288-Q1 can operate over a wide range of 2.7-V to 36-V input voltage and an output voltage of 0.8 V to 22 V. It can transition among buck mode, buck-boost mode, and boost mode smoothly according to the input voltage and the set output voltage. The TPS55288-Q1 operates in buck mode when the input voltage is greater than the output voltage and in boost mode when the input voltage is less than the output voltage. When the input voltage is close to the output voltage, the TPS55288-Q1 operates in one-cycle buck and one-cycle boost mode alternately.

The TPS55288-Q1 uses an average current mode control scheme. Current mode control provides simplified loop compensation, rapid response to the load transients, and inherent line voltage rejection. An error amplifier compares the feedback voltage with the internal reference voltage. The output of the error amplifier determines the average inductor current.

An internal oscillator can be configured to operate over a wide range of frequency from 200 kHz to 2.2 MHz. The internal oscillator can also synchronize to an external clock applied to the DITH/SYNC pin. To minimize EMI, the TPS55288-Q1 can dither the switching frequency at ±7% of the set frequency.

The TPS55288-Q1 works in fixed-frequency PWM mode at moderate to heavy load currents. In light load condition, the TPS55288-Q1 can be configured to automatically transition to PFM mode or be forced in PWM mode by either connecting a resistor at the MODE pin or setting the corresponding bit in an internal register.

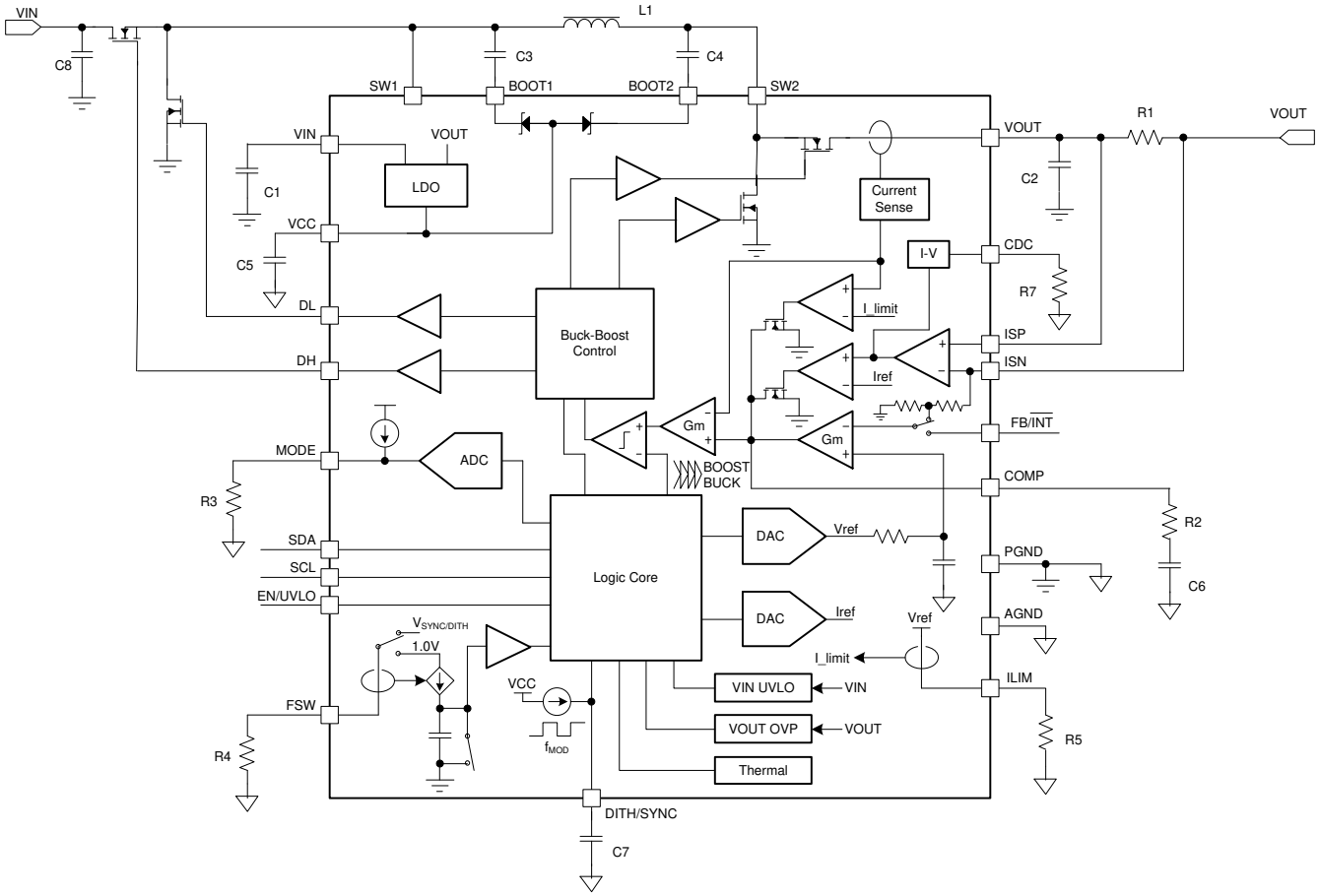
The output voltage of the TPS55288-Q1 is adjustable by setting the internal register through I^2C interface. An internal 10-bit DAC adjusts the reference voltage related to the value written into the REF register. The device can also limit the output current by placing a current sense resistor in the output path. These two functions support the programmable power supply (PPS) feature of the USB PD.

The TPS55288-Q1 provides average inductor current limit set by a resistor at the ILIM pin. In addition, it provides cycle-by-cycle peak inductor current limit during transient to protect the device against overcurrent condition beyond the capability of the device.

A precision voltage threshold of 1.23 V with 5-µA sourcing current at the EN/UVLO pin supports programmable input undervoltage lockout (UVLO) with hysteresis. The output overvoltage protection (OVP) feature turns off the high-side FETs to prevent damage to the devices powered by the TPS55288-Q1.

The device provides hiccup mode option to reduce the heating in the power components when output short circuit happens. When the hiccup mode is enabled, the TPS55288-Q1 turns off for 76 ms and restarts at soft start-up.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 VCC Power Supply

An internal LDO to supply the TPS55288-Q1 outputs regulated 5.2-V voltage at the VCC pin with 60-mA output current capability. When V_{IN} is less than V_{OUT}, the internal LDO selects the power supply source by comparing V_{IN} to a rising threshold of 6.2 V with 0.3-V hysteresis. When V_{IN} is higher than 6.2 V, the supply for LDO is V_{IN}. When V_{IN} is lower than 5.9 V, the supply for LDO is V_{OUT}. When V_{OUT} is less than V_{IN}, the internal LDO selects the power supply source by comparing V_{OUT} to a rising threshold of 6.2 V with 0.3-V hysteresis. When V_{OUT} is higher than 6.2 V, the supply for LDO is V_{OUT}. When V_{OUT} is lower than 5.9 V, the supply for LDO is V_{IN}. 表 7-1 shows the supply source selection for the internal LDO.

表 7-1. V_{CC} Power Supply Logic

V_{IN}	V_{OUT}	INPUT for V_{CC} LDO
V_{IN} > 6.2 V	V_{OUT} > V_{IN}	V_{IN}
V_{IN} < 5.9 V	V_{OUT} > V_{IN}	V_{OUT}
V_{IN} > V_{OUT}	V_{OUT} > 6.2 V	V_{OUT}
V_{IN} > V_{OUT}	V_{OUT} < 5.9 V	V_{IN}

To minimize the power dissipation of the internal LDO when both input voltage and output voltage are high, an external 5-V power source can be applied at the VCC pin to supply the TPS55288-Q1. The external 5-V power supply must have at least 100-mA output current capability and must be within the 4.75-V to 5.5-V regulation range. To use an external power supply for V_{CC}, a resistor with proper resistance must be connected to the MODE pin.

7.3.2 Operation Mode Setting

By placing different resistors between the MODE pin and AGND pin, the TPS55288-Q1 selects the internal power supply or external power supply for V_{CC}, selects one of two different I^2C addresses, and selects the PFM mode or the forced PWM mode in light load conditions. 表 7-2 shows the resistance values for each selection. After the TPS55288-Q1 is enabled, an I^2C master device can control these three operating modes by writing the corresponding value into the internal registers regardless the resistance settings at the MODE pin. See details in 节 7.6.

表 7-2. V_{CC} Source, I^2C Slave Address and PFM/PWM Programming

RESISTOR VALUE (kΩ)	V_{CC} SOURCE	I^2C SLAVE ADDRESS	OPERATING MODE AT LIGHT LOAD
0	Internal	74h	PWM
6.19	Internal	74h	PFM
14.3	Internal	75h	PWM
24.9	Internal	75h	PFM
51.1	External	74h	PWM
75.0	External	74h	PFM
105	External	75h	PWM
Open	External	75h	PFM

7.3.3 Input Undervoltage Lockout

When the input voltage is below 2.6 V, the TPS55288-Q1 is disabled. When the input voltage is above 3 V, the TPS55288-Q1 can be enabled by pulling the EN pin to a high voltage above 1.3 V.

7.3.4 Enable and Programmable UVLO

The TPS55288-Q1 has a dual function enable and undervoltage lockout (UVLO) circuit. When the input voltage at the VIN pin is above the input UVLO rising threshold of 3 V and the EN/UVLO pin is pulled above 1.15 V but less than the enable UVLO threshold of 1.23 V, the TPS55288-Q1 is enabled but still in standby mode. The TPS55288-Q1 starts to detect the resistance between the MODE pin and ground. After that, the TPS55288-Q1 selects the power supply for V_{CC}, the I^2C slave address, and the PFM or FPWM mode for light load condition accordingly.

The EN/UVLO pin has an accurate UVLO voltage threshold to support programmable input undervoltage lockout with hysteresis. When the EN/UVLO pin voltage is greater than the UVLO threshold of 1.23 V, the TPS55288-Q1 is enabled for I^2C communication and switching operation. A hysteresis current I_{UVLO_HYS} is sourced out of the EN/UVLO pin to provide hysteresis that prevents on/off chattering in the presence of noise with a slowly changing input voltage.

By using resistor divider as shown in 图 7-1, the turnon threshold is calculated using 方程式 1.

$$V_{IN(UVLO\_ON)} = V_{UVLO} \times (1 + \frac{R1}{R2}) \quad (1)$$

where

- V_{UVLO} is the UVLO threshold of 1.23 V at the EN/UVLO pin

The hysteresis between the UVLO turnon threshold and turnoff threshold is set by the upper resistor in the EN/UVLO resistor divider and is given by the Equation 2.

$$\Delta V_{IN(UVLO)} = I_{UVLO\_HYS} \times R1 \quad (2)$$

where

- I_{UVLO_HYS} is the sourcing current from the EN/UVLO pin when the voltage at the EN/UVLO pin is above V_{UVLO}

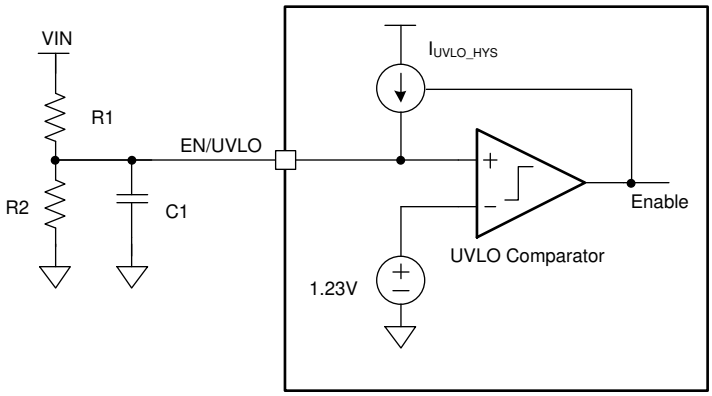


图 7-1. Programmable UVLO With Resistor Divider at the EN/UVLO Pin

Using an NMOSFET together with a resistor divider can implement both logic enable and programmable UVLO as shown in 图 7-2. The EN logic high level must be greater than enable threshold plus the V_{th} of the NMOSFET Q1. The Q1 also eliminates the leakage current from VIN to ground through the UVLO resistor divider during shutdown mode.

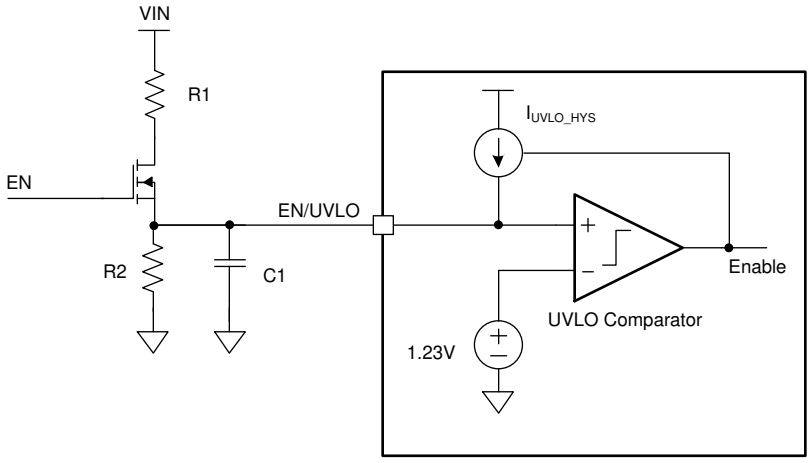


图 7-2. Logic Enable and Programmable UVLO

7.3.5 Soft Start

When the input voltage is above the UVLO threshold and the voltage at the EN/UVLO pin is above the enable UVLO threshold, the TPS55288-Q1 is ready to accept the command from I^2C master device. An I^2C master device can configure the internal registers of the TPS55288-Q1 before setting the OE bit of the register 06h. Once an I^2C master device sets the OE bit to 1, the TPS55288-Q1 starts to ramp up the output voltage by ramping an internal reference voltage from 0 V to a voltage set in the internal registers 00h and 01h within typical 4 ms.

7.3.6 Shutdown and Load Discharge

When the EN/UVLO pin voltage is pulled below 0.4 V, the TPS55288-Q1 is in shutdown mode, and all functions are disabled. All internal registers are reset to default values.

When the EN/UVLO pin is at high logic level and the OE bit is cleared to 0, the TPS55288-Q1 turns off the switching operation but keeps the I^2C interface active. Simultaneously, if the DISCHG bit in the register 06h is set to 1, the TPS55288-Q1 discharges the output voltage below 0.8 V by an internal constant current.

7.3.7 Switching Frequency

The TPS55288-Q1 uses a fixed frequency average current control scheme. The switching frequency is between 200 kHz and 2.2 MHz set by placing a resistor at the FSW pin. An internal amplifier holds this pin at a fixed voltage of 1 V. The setting resistance is between maximum of 100 kΩ and minimum of 9.09 kΩ. Use Equation 3 to calculate the resistance by a given switching frequency.

$$f_{SW} = \frac{1000}{0.05 \times R_{FSW} + 20} \text{ (MHz)} \quad (3)$$

where

- R_{FSW} is the resistance at the FSW pin

For noise-sensitive applications, the TPS55288-Q1 can be synchronized to an external clock signal applied to the DITH/SYNC pin. The duty cycle of the external clock is recommended in the range of 30% to 70%. A resistor also must be connected to the FSW pin when the TPS55288-Q1 is switching by the external clock. The external clock frequency at the DITH/SYNC pin must have lower than 0.4-V low level voltage and must be within ±30% of the corresponding frequency set by the resistor. 图 7-3 is a recommended configuration.

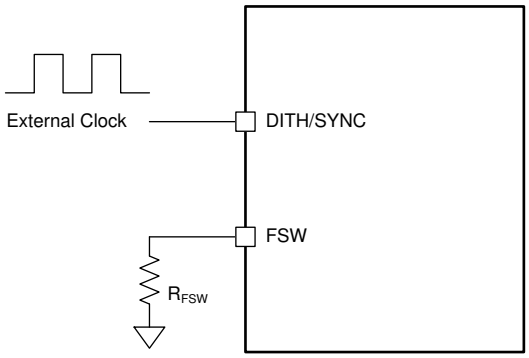


图 7-3. External Clock Configuration

7.3.8 Switching Frequency Dithering

The TPS55288-Q1 provides an optional switching frequency dithering that is enabled by connecting a capacitor from the DITH/SYNC pin to ground. 图 7-4 illustrates the dithering circuit. By charging and discharging the capacitor, a triangular waveform centered at 1 V is generated at the DITH/SYNC pin. The triangular waveform modulates the oscillator frequency by ±7% of the nominal frequency set by the resistance at the FSW pin. The capacitance at the DITH/SYNC pin sets the modulation frequency. A small capacitance modulates the oscillator frequency at a fast rate than a large capacitance. For the dithering circuit to effectively reduce peak EMI, the modulation rate normally is below 1 kHz. Equation 4 calculates the capacitance required to set the modulation frequency, F_{MOD}.

$$C_{DITH} = \frac{1}{2.8 \times R_{FSW} \times F_{MOD}} (F) \quad (4)$$

where

- R_{FSW} is the switching frequency setting resistance (Ω) at the FSW pin
- F_{MOD} is the modulation frequency (Hz) of the dithering

Connecting the DITH/SYNC pin below 0.4 V or above 1.2 V disables switching frequency dithering. The dithering function also is disabled when an external synchronous clock is used.

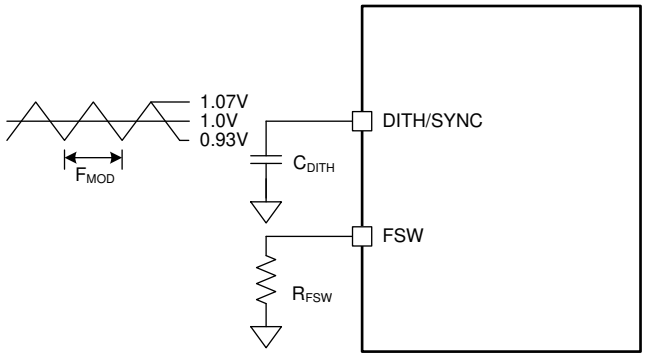


图 7-4. Switching Frequency Dithering

7.3.9 Inductor Current Limit

The TPS55288-Q1 implements both peak current and average inductor current limit by a resistor connected to the ILIM pin. The average current mode control loop uses the current sense information at the high-side MOSFET of the boost leg to clamp the maximum average inductor current to 16.5 A (typical) when the resistor is 20 kΩ. Use large resistance to get smaller average inductor current limit. Use Equation 5 to calculate the resistance for a desired average inductor current limit.

$$I_{AVG\_LIMIT} = \frac{\min(1, 0.6 \times V_{OUT}) \times 330000}{R_{ILIM}} (A) \quad (5)$$

where

- I_{AVG_LIMIT} is the average inductor current limit
- R_{ILIM} is the resistance (Ω) between the ILIM pin and analog ground

Besides the average current limit, a peak current limit protection is implemented during transient to protect the device against over current condition beyond the capability of the device.

7.3.10 Internal Charge Path

Each of the two high-side MOSFET drivers is biased from its floating bootstrap capacitor, which is normally re-charged by V_{CC} through both the external and internal bootstrap diodes when the low-side MOSFET is turned on. When the TPS55288-Q1 operates exclusively in the buck or boost regions, one of the high-side MOSFETs is constantly on. An internal charge path, from VOUT and BOOT2 to BOOT1 or from VIN and BOOT1 to BOOT2, charges the bootstrap capacitor to V_{CC} so that the high-side MOSFET remains on.

7.3.11 Output Voltage Setting

There are two ways to set the output voltage: changing the feedback ratio and changing the reference voltage. The TPS55288-Q1 has a 10-bit DAC to program the reference voltage from 45 mV to 1.2 V. The TPS55288-Q1 also can select an internal feedback resistor divider or an external resistor divider by setting the FB bit in register 04h. When the FB bit is set to 0, the output voltage feedback ratio is set in internal register 04h. When the FB bit is set to 1, the output voltage feedback ratio is set by an external resistor divider.

When using internal output voltage feedback settings, there are four feedback ratios programmable by writing the INTFB[1:0] bits of register 04h. With this function, the TPS55288-Q1 can limit the maximum output voltage to different values. In addition, the minimum step of the output voltage change is also programmed to 20 mV, 15 mV, 10 mV, and 5 mV, accordingly.

When using an external output voltage feedback resistor divider as shown in 图 7-5, use Equation 6 to calculate the output voltage with the reference voltage at the FB/$\overline{INT}$ pin.

$$V_{OUT} = V_{REF} \times (1 + \frac{R_{FB\_UP}}{R_{FB\_BT}}) \quad (6)$$

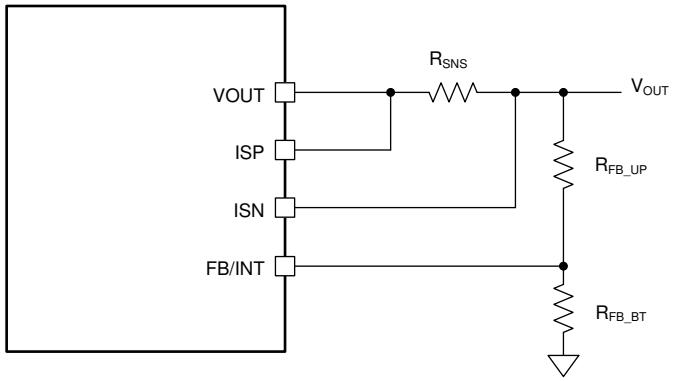


图 7-5. Output Voltage Setting by External Resistor Divider

TI recommends using 100 kΩ for the up resistor R_{FB_UP}. The reference voltage V_{REF} at the FB/$\overline{INT}$ pin is programmable from 45 mV to 1.2 V by writing a 10-bit data into register 00h and 01h.

7.3.12 Output Current Monitoring and Cable Voltage Droop Compensation

The TPS55288-Q1 outputs a voltage at the CDC pin proportional to the sensed voltage across a output current sensing resistor between the ISP pin and the ISN pin. Equation 7 shows the exact voltage at the CDC pin related to the sensed output current.

$$V_{CDC} = 20 \times (V_{ISP} - V_{ISN}) \quad (7)$$

To compensate the voltage droop across a cable from the output of the USB port to its powered device, the TPS55288-Q1 can lift its output voltage in proportion to the load current. There are two methods in the TPS55288-Q1 to implement the compensation: by setting internal register 05h or by placing a resistor between the CDC pin and AGND pin.

When using internal output voltage feedback, it is recommended to use the internal compensation setting. When using an external resistor divider at the FB/$\overline{INT}$ pin to set the output voltage, it is recommended to use the external compensation setting by placing a resistor at the CDC pin.

By default, the internal cable voltage droop compensation function is enabled with 0 V added to the output voltage. Write the value into the bit CDC [2:0] in register 05h to get the desired voltage compensation.

When using external output voltage feedback, external compensation is better than the internal register for its high accuracy. The output voltage rises in proportion to the current sourcing from the CDC pin through the resistor at the CDC pin. It is recommended to use 100-kΩ resistance for the up resistor of the feedback resistor divider. Equation 8 shows the output voltage rise related to the sensed output current, the resistance at the CDC pin, and the up resistor of the output voltage feedback resistor divider.

$$V_{OUT\_CDC} = 3 \times R_{FB\_UP} \times \left(\frac{V_{ISP} - V_{ISN}}{R_{CDC}}\right) \quad (8)$$

where

- R_{FB_UP} is the up resistor of the resistor divider between the output and the FB/INT pin
- R_{CDC} is the resistor at the CDC pin

When RFB_UP is 100 kΩ, the output voltage rise versus the sensed output current and the resistor at the CDC pin is shown in 图 7-6.

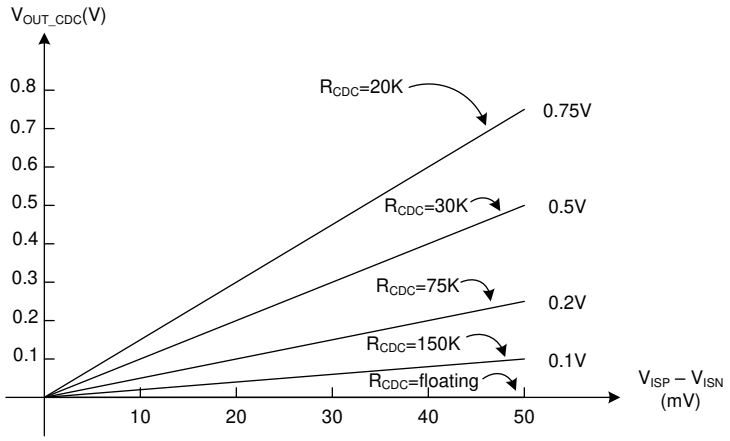


图 7-6. Output Voltage Rise versus Output Current

7.3.13 Integrated Gate Drivers

The TPS55288-Q1 provides two N-channel MOSFET gate drivers for buck side. Each driver is capable of sourcing 1-A and sinking 1.8-A peak current. In buck operation, the DR1H pin and the DR1L pin are switched by the PWM controller. In boost mode, the DR1H pin remains at continuously high voltage to turn on the high-side MOSFET of the buck side, and the DR1L pin remains at continuously low voltage to turn off the low-side MOSFET of the buck side.

In DCM buck mode operation, the DR1L turns off the low-side FET when the inductor current drops to zero.

The low-side gate driver is powered from the VCC pin, and the high-side gate driver is powered from the bootstrap capacitor C_{BOOT1}, which is between the BOOT1 pin and the SW1 pin.

7.3.14 Output Current Limit

The output current limit is programmable from 0 A to 6.35 A by placing a 10-mΩ current sensing resistor between the ISP pin and the ISN pin. Smaller resistance results in a higher current limit and bigger resistance results in a lower current limit. An internal register sets the current sense voltage across the ISP pin and the ISN pin. The programmable voltage step between the ISP pin and the ISN pin is 0.5 mV.

Connecting the ISP and the ISN pin together to the VOUT pin disables the output current limit because the sensed voltage is always zero. The output current limit can also be disabled by reset the Current_Limit_EN bit in the Current_Limit register to 0.

When the OE bit or the Current_Limit_EN bit is changed from 0 to 1, the OCP_MASK must be 0. After the OE bit and the Current_Limit_EN bit are set, set the OCP_MASK to 1 to enable the OCP fault indication output.

7.3.15 Overvoltage Protection

The TPS55288-Q1 has output overvoltage protection. When the output voltage at the VOUT pin is detected above 23.5 V typically, the TPS55288-Q1 turns off two high-side FETs and turns on two low-side FETs until its output voltage drops the hysteresis value lower than the output overvoltage protection threshold. This function prevents overvoltage on the output and secures the circuits connected to the output from excessive overvoltage.

7.3.16 Output Short Circuit Protection

In addition to the average inductor current limit, the TPS55288-Q1 implements the output short-circuit protection by entering hiccup mode. To enable hiccup mode, the HICCUP bit in register 06h must be set. After soft start-up time of 4 ms, the TPS55288-Q1 monitors the average inductor current and output voltage. Whenever the output short circuit happens, causing the average inductor current hitting the set limit and the output voltage below 0.8 V, the TPS55288-Q1 shuts down the switching for 76 ms (typical) and then repeats the soft start for 4 ms. The hiccup mode helps reduce the total power dissipation on the TPS55288-Q1 in the output short-circuit or overcurrent condition.

7.3.17 Thermal Shutdown

The TPS55288-Q1 is protected by a thermal shutdown circuit that shuts down the device when the internal junction temperature exceeds 175°C (typical). The internal soft-start circuit is reset but all internal registers values remain unchanged when thermal shutdown is triggered. The converter automatically restarts when the junction temperature drops below the thermal shutdown hysteresis of 20°C below the thermal shutdown threshold.

7.4 Device Functional Modes

In light load condition, the TPS55288-Q1 can work in PFM or forced PWM mode to meet different application requirements. PFM mode decreases switching frequency to reduce the switching loss thus it gets high efficiency at light load condition. The FPWM mode keeps the switching frequency unchanged to avoid undesired low switching frequency but the efficiency becomes lower than that of PFM mode.

7.4.1 PWM Mode

In FPWM mode, the TPS55288-Q1 keeps the switching frequency unchanged in light load condition. When the load current decreases, the output of the internal error amplifier decreases as well to reduce the average inductor current down to deliver less power from input to output. When the output current further reduces, the current through the inductor decreases to zero during the switch-off time. The high-side N-MOSFET is not turned off even if the current through the MOSFET is zero. Thus, the inductor current changes its direction after it runs to zero. The power flow is from output side to input side. The efficiency is low in this condition. However, with the fixed switching frequency, there is no audible noise or other problems that might be caused by low switching frequency in light load condition.

7.4.2 Power Save Mode

The TPS55288-Q1 improves the efficiency at light load condition with PFM mode. By connecting an appropriate resistor at the MODE pin or enabling the PFM function in the internal register, the TPS55288-Q1 can work in PFM mode at light load condition. When the TPS55288-Q1 operates at light load condition, the output of the internal error amplifier decreases to make the inductor peak current down to deliver less power to the load. When the output current further reduces, the current through the inductor will decrease to zero during the switch-off time. When the TPS55288-Q1 works in buck mode, once the inductor current becomes zero, the low-side switch of the buck side is turned off to prevent the reverse current from output to ground. When the TPS55288-Q1 works in boost mode, once the inductor current becomes zero, the high side-switch of the boost side is turned off to prevent the reverse current from output to input. The TPS55288-Q1 resumes switching until the output voltage drops. Thus PFM mode reduces switching cycles and eliminates the power loss by the reverse inductor current to get high efficiency in light load condition.

7.5 Programming

The TPS55288-Q1 uses I^2C interface for flexible converter parameter programming. I^2C is a bi-directional 2-wire serial interface. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). I^2C devices can be considered as masters or slaves when performing data transfers. A master is the device that initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The TPS55288-Q1 operates as a slave device with address 74h and 75h set by a different resistor at the MODE pin. Receiving control inputs from the master device like a microcontroller or a digital signal processor reads and writes the internal registers 00h through 07h. The I^2C interface of the TPS55288-Q1 supports both standard mode (up to 100 kbit/s) and fast mode plus (up to 1000 kbit/s). Both SDA and SCL must be connected to the positive supply voltage through current sources or pullup resistors. When the bus is free, both lines are in high voltage.

7.5.1 Data Validity

The data on the SDA line must be stable during the high level period of the clock. The high level or low level state of the data line can only change when the clock signal on the SCL line is low level. One clock pulse is generated for each data bit transferred.

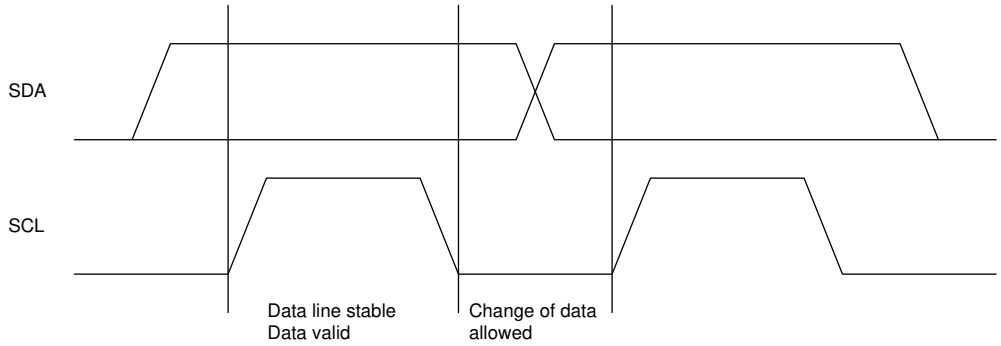


图 7-7. I²C Data Validity

7.5.2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A high level to low level transition on the SDA line while SCL is at high level defines a START condition. A low level to high level transition on the SDA line when the SCL is at high level defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

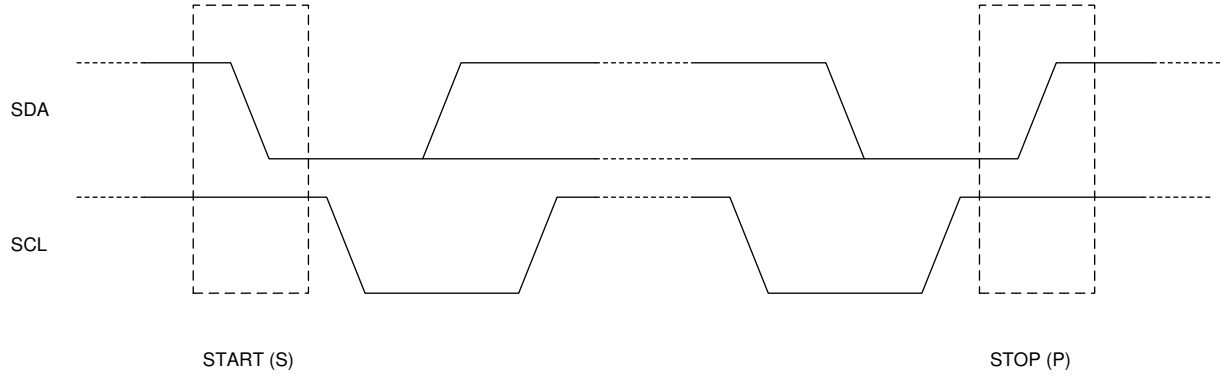


图 7-8. I²C START and STOP Conditions

7.5.3 Byte Format

Every byte on the SDA line must be eight bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

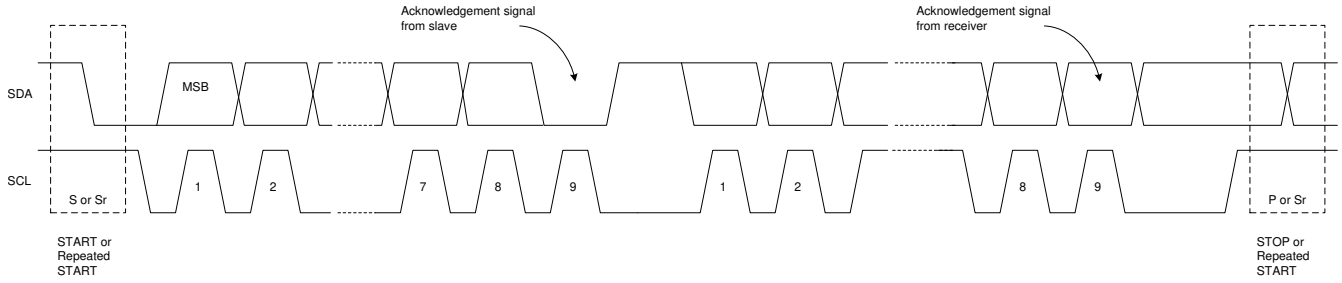


图 7-9. Byte Format

7.5.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line to low level and it remains stable low level during the high level period of this clock pulse.

The Not Acknowledge signal is when SDA remains high level during the 9th clock pulse. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

7.5.5 Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is seven bits long followed by the eighth bit as a data direction bit (bit R/$\overline{W}$). A zero indicates a transmission (WRITE) and a one indicates a request for data (READE).

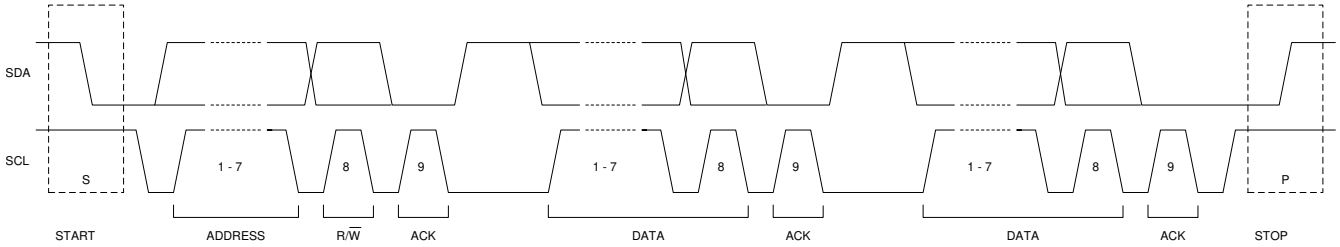


图 7-10. Slave Address and Data Direction

7.5.6 Single Read and Write

图 7-11 and 图 7-12 show the single-byte write and single-byte read format of the I^{2}C communication.

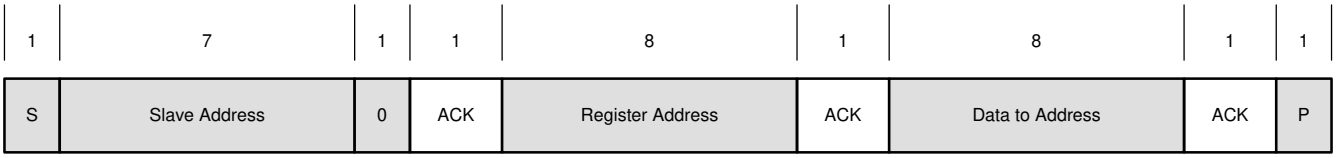


图 7-11. Single-byte Write

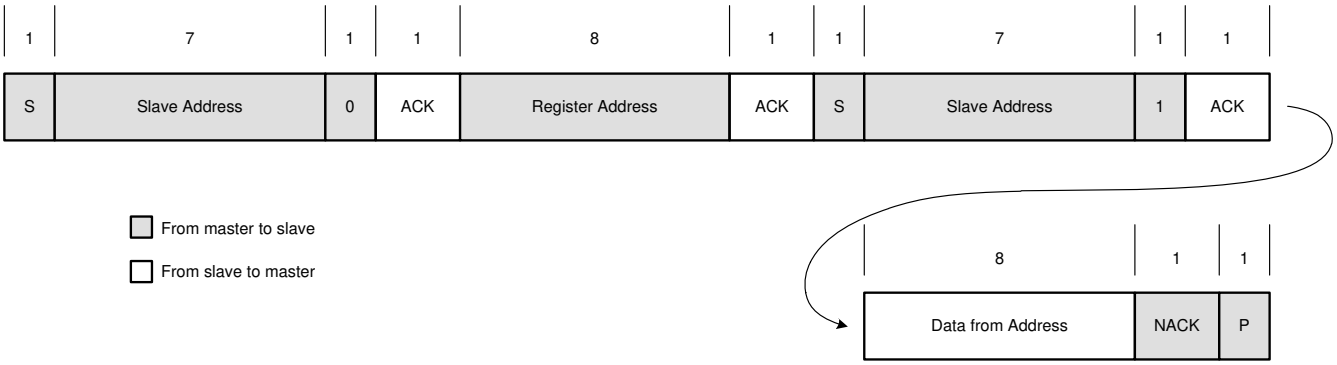


图 7-12. Single-byte Read

If the register address is not defined, the TPS55288-Q1 sends back NACK and goes back to the idle state.

7.5.7 Multi-Read and Multi-Write

The TPS55288-Q1 supports multi-read and multi-write.

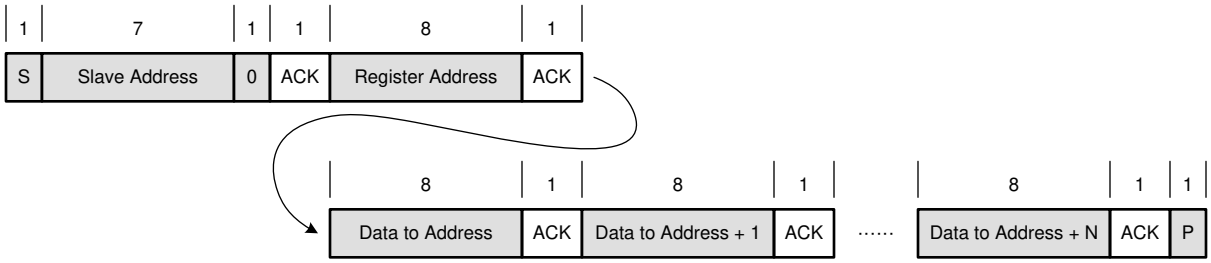


图 7-13. Multi-byte Write

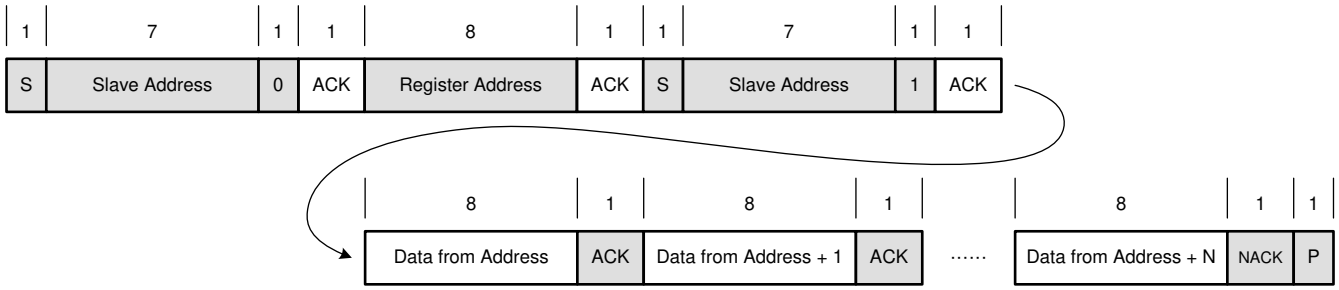


图 7-14. Multi-byte Read

7.6 Register Maps

表 7-3 lists the memory-mapped registers for the device registers. All register offset addresses not listed in 表 7-3 should be considered as reserved locations, and the register contents should not be modified.

表 7-3. Device Registers

Address	Acronym	Register Name	Section
0h, 1h	REF	Reference Voltage	Go
2h	IOUT_LIMIT	Current Limit Setting	Go
3h	VOUT_SR	Slew Rate	Go
4h	VOUT_FS	Feedback Selection	Go
5h	CDC	Cable Compensation	Go
6h	MODE	Mode Control	Go
7h	STATUS	Operating Status	Go

7.6.1 REF Register (Address = 0h, 1h) [reset = 11010010h, 00000000h]

REF is shown in 图 7-15 and 图 7-16 described in 表 7-4.

Return to Summary Table.

REF sets the internal reference voltage of the TPS55288-Q1. The 01h register is the high byte and the 00h register is the low byte. One LSB of register 00h stands for 1.129 mV of the internal reference voltage. The default register value is 00000000 11010010b of 282 mV. When the register value is 00000000 00000000b, the reference voltage is 45 mV. When the register value is 00000011 11000000b, the reference voltage is 1.129 V. The output voltage of the TPS55288-Q1 also depends on the output feedback ratio, which is either set in register 04h or set by an external resistor divider.

Writing register 01h enables the TPS55288-Q1 to load the 01h and 00h data into the internal 10-bit DAC. Writing the register 00h does not impact the internal reference voltage.

图 7-15. REF_LSB

7	6	5	4	3	2	1	0
VREF							
R/W-11010010b							

图 7-16. REF_MSB

15	14	13	12	11	10	9	8
Reserved						VREF	
R/W-000000b						R/W-00b	

表 7-4. REF Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	Reserved	R/W	000000b	Reserved
9-0	VREF	R/W	00 11010010b	Sets the internal reference voltage 00 00000000b = 45-mV reference voltage 00 00000001b = 46.129-mV reference voltage 00 00000010b = 47.258-mV reference voltage ..... = ... 00 11010010b = 282-mV reference voltage (Default) ..... = ... 01 10011010b = 508-mV reference voltage ..... = ... 10 11000110b = 846-mV reference voltage ..... = ... 11 11000000b = 1129-mV reference voltage ..... = ... 11 11111111b = 1200-mV reference voltage

7.6.2 IOUT_LIMIT Register (Address = 2h) [reset = 11100100h]

IOUT_LIMIT is shown in 图 7-17 and described in 表 7-5.

Return to Summary Table.

IOUT_LIMIT sets the current limit target voltage between the ISP pin and the ISN pin. The default value in the current limit register is 11100100b standing for 50 mV. 1 LSB stands for 0.5 mV. The bit7 enables the current limit or disables the current limit.

图 7-17. IOUT_LIMIT Register

7	6	5	4	3	2	1	0
Current_Limit_EN	Current_Limit_Setting						
R/W-1b	R/W-1100100b						

表 7-5. IOUT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Current_Limit_EN	R/W	1b	Enable or disable current limit. 0b = Current limit disabled 1b = Current limit enabled (Default)
6-0	Current_Limit_Setting	R/W	1100100b	Sets the current limit target voltage between the ISP pin and the ISN pin 0000000b = V_{ISP}-V_{ISN} = 0 (mV) 0000001b = V_{ISP}-V_{ISN} = 0.5 (mV) 0000010b = V_{ISP}-V_{ISN} = 1 (mV) 0000011b = V_{ISP}-V_{ISN} = 1.5 (mV) 0000100b = V_{ISP}-V_{ISN} = 2.0 (mV) 1100100b = V_{ISP}-V_{ISN} = 50.0 (mV) (Default) 1111111b = V_{ISP}-V_{ISN} = 63.5 (mV)

7.6.3 VOUT_SR Register (Address = 3h) [reset = 00000001h]

VOUT_SR is shown in 图 7-18 and described in 表 7-6.

Return to Summary Table.

Register 03h sets the slew rate of the output voltage change and the response delay time after the output current exceeds the setting output current limit.

The OCP_DELAY [1:0] bits set the response time of the TPS55288-Q1 when the output overcurrent limit is hit. This allows the TPS55288-Q1 to output high current in a relative short duration time. The default setting is 128 µs so that the TPS55288-Q1 immediately limits the output current.

The SR [1:0] bits set 1.25 mV/µs, 2.5 mV/µs, 5 mV/µs, and 10 mV/µs slew rate for output voltage change.

图 7-18. VOUT_SR Register

7	6	5	4	3	2	1	0
RESERVED		OCP_DELAY		RESERVED		SR	
R/W-0b		R/W-00b		R/W-00b		R/W-01b	

表 7-6. VOUT_SR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00b	Reserved
5-4	OCP_DELAY	R/W	00b	Sets the response time of the device when the output overcurrent limit is reached. 00b = 128 µs (Default) 01b = Delay 1.024 x 3 ms 10b = Delay 1.024 x 6 ms 11b = Delay 1.024 x 12 ms
3-2	RESERVED	R/W	00b	Reserved
1-0	SR	R/W	01b	Sets slew rate for output voltage change. 00b = 1.25 mV/µs output change slew rate 01b = 2.5 mV/µs output change slew rate (Default) 10b = 5 mV/µs output change slew rate 11b = 10 mV/µs output change slew rate

7.6.4 VOUT_FS Register (Address = 4h) [reset = 00000011h]

VOUT_FS is shown in 图 7-19 and described in 表 7-7.

Return to Summary Table.

Register 04h sets the selection for the output feedback voltage, either by an internal resistor divider or external resistor divider, and sets the internal feedback ratio when using internal feedback resistor divider.

图 7-19. VOUT_FS Register

7	6	5	4	3	2	1	0
FB	RESERVED					INTFB	
R/W-0b	R/W-00000b					R/W-11b	

表 7-7. VOUT_FS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FB	R/W	0b	Output feedback voltage 0b = Use internal output voltage feedback. The FB/$\overline{INT}$ pin is the indicator for output short circuit protection, overcurrent status, and overvoltage status (Default). 1b = Use external output voltage feedback. The FB/$\overline{INT}$ pin is the feedback input of the output voltage.
6-2	RESERVED	R	00000b	Reserved
1-0	INTFB	R/W	11b	Internal feedback ratio 00b = Set internal feedback ratio to 0.2256 01b = Set internal feedback ratio to 0.1128 10b = Set internal feedback ratio to 0.0752 11b = Set internal feedback ratio to 0.0564(Default)

表 7-8. Output Voltage vs Internal Reference

INTFB1	INTFB0	REF=0000h	REF=000Dh	REF=0028h	REF=0078h	REF=03C0h	Output Voltage Step
0	0				0.8 V	5 V	5 mV
0	1			0.8 V		10 V	10 mV
1	0		0.8 V			15 V	15 mV
1	1	0.8 V				20 V	20 mV

7.6.5 CDC Register (Address = 5h) [reset = 11100000h]

CDC is shown in 图 7-20 and described in 表 7-9.

Return to Summary Table.

Register 05h sets masks for SC bit, OCP bit, and OVP bit in register 07h. In addition, register 05h sets the voltage rise added to the setting output voltage with respect to the sensed differential voltage between the ISP pin and the ISN pin.

The OCP_MASK must be 0 when the OE bit or the Current_Limit_EN bit is changed from 0 to 1. After the OE bit and the Current_Limit_EN bit are set, set the OCP_MASK to 1 to enable the OCP fault indication output.

图 7-20. CDC Register

7	6	5	4	3	2	1	0
SC_MASK	OCP_MASK	OVP_MASK	RESERVED	CDC_OPTION	CDC		
R/W-1b	R/W-1b	R/W-1b	R/W-0b	R/W-0b	R/W-000b		

表 7-9. CDC Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SC_MASK	R/W	1b	Short circuit mask 0b = Disabled SC indication 1b = Enable SC indication (Default)
6	OCP_MASK	R/W	1b	Over current mask 0b = Disabled OCP indication 1b = Enable OCP indication (Default)
5	OVP_MASK	R/W	1b	Over voltage mask 0b = Disabled OVP indication 1b = Enable OVP indication (Default)
4	RESERVED	R/W	0b	Reserved
3	CDC_OPTION	R/W	0b	Select the cable voltage droop compensation approach. 0b = Internal CDC compensation by the register 05H (Default) 1b = External CDC compensation by a resistor at the CDC pin
2-0	CDC	R/W	000b	Compensation for voltage droop over the cable 000b = 0-V output voltage rise with 50 mV at V_{ISP} - V_{ISN} (Default) 001b = 0.1-V output voltage rise with 50 mV at V_{ISP} - V_{ISN} 010b = 0.2-V output voltage rise with 50 mV at V_{ISP} - V_{ISN} 011b = 0.3-V output voltage rise with 50 mV at V_{ISP} - V_{ISN} 100b = 0.4-V output voltage rise with 50 mV at V_{ISP} - V_{ISN} 101b = 0.5-V output voltage rise with 50 mV at V_{ISP} - V_{ISN} 110b = 0.6-V output voltage rise with 50 mV at V_{ISP} - V_{ISN} 111b = 0.7-V output voltage rise with 50 mV at V_{ISP} - V_{ISN}

7.6.6 MODE Register (Address = 6h) [reset = 00100000h]

MODE is shown in 图 7-21 and described in 表 7-10.

Return to Summary Table.

MODE controls the operating mode of the TPS55288-Q1.

图 7-21. MODE Register

7	6	5	4	3	2	1	0
OE	FSW	HICCUP	DISCHG	VCC	I2CADD	PFM	MODE
R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 7-10. MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OE	R/W	0b	Output enable 0b = Output disabled (Default) 1b = Output enable
6	FSWDBL	R/W	0b	Switching frequency doubling in buck-boost mode TI does not recommend using double frequency function at switching frequency above 1.6 MHz. 0b = Keep the switching frequency unchanged during buck-boost mode (Default) 1b = Double the switching frequency during buck-boost mode
5	HICCUP	R/W	1b	Hiccup mode 0b = Disable the hiccup during output short circuit protection. 1b = Enable the hiccup during output short circuit protection (Default)
4	DISCHG	R/W	0b	Output discharge 0b = Disabled VOUT discharge when the device is in shutdown mode (Default) 1b = Enable VOUT discharge. VOUT is discharged to ground by an internal 100-mA current sink
3	VCC	R/W	0b	V_{CC} option 0b = Select internal LDO for V_{CC} (Default) 1b = Select external 5-V power supply for V_{CC}
2	I2CADD	R/W	0b	I^2C address 0b = Set I^2C slave address to 74h (Default) 1b = Set I^2C slave address to 75h
1	PFM	R/W	0b	Select operating mode at light load condition 0b = PFM operating mode at light load condition (Default) 1b = FPWM operating mode at light load condition
0	MODE	R/W	0b	Mode control approach 0b = Set VCC, I2CADD, and PFM controlled by external resistor (Default) 1b = Set VCC, I2CADD, and PFM controlled by internal register

7.6.7 STATUS Register (Address = 7h) [reset = 00000011h]

STATUS is shown in 图 7-22 and described in 表 7-11.

Return to Summary Table.

The STATUS register stores the operating status of the TPS55288-Q1. When any of the SCP bit, the OCP bit, or the OVP bit are set, and the corresponding mask bit in register 05h is set as well, the FB/$\overline{INT}$ pin outputs low logic level to indicate the situation. Reading register 07h clears the SCP bit, OCP bit, and OVP bit. After the SCP bit, OCP bit, or OVP bit is set, it does not reset until the register is read. If the situation still exists, the corresponding bit is set again.

图 7-22. STATUS Register

7	6	5	4	3	2	1	0
SCP	OCP	OVP	Reserved	Reserved	Reserved	STATUS	
R-0b	R-0b	R-0b	R/W-0b	R/W-0b	R/W-0b	R-11b	

表 7-11. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SCP	R	0b	Short circuit protection 0b = No short circuit 1b = Short circuit happens. Does not reset until it is read.
6	OCP	R	0b	Overcurrent protection 0b = No output overcurrent 1b = Output current hits the current limit sensed at the ISP and the ISN pin. Does not reset until it is read.
5	OVP	R	0b	Overvoltage protection 0b = No OVP 1b = Output voltage exceeds the OVP threshold. Does not reset until it is read.
4	RESERVED	R	0b	Reserved
3	RESERVED	R	0b	Reserved
2	RESERVED	R	0b	Reserved
1-0	STATUS	R	11b	Operating status 00b = Boost 01b = Buck 10b = Buck-Boost 11b = Reserved

7.6.8 Register Summary

The 表 7-12 summarizes the default settings of the registers in the TPS55288-Q1.

表 7-12. Default Settings of Registers

Register Address	Register Name	R/W	Default Values
00h	VREF_LSB	R/W	11010010
01h	VREF_MSB	R/W	00000000
02h	IOUT_LIMIT	R/W	11100100
03h	VOUT_SR	R/W	00000001
04h	VOUT_FS	R/W	00000011
05h	CDC	R/W	11100000
06h	MODE	R/W	00100000
07h	STATUS	R	00000011

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TPS55288-Q1 can operate over a wide range of 2.7-V to 36-V input voltage and output 0.8 V to 22 V. It can transition among buck mode, buck-boost mode, and boost mode smoothly according to the input voltage and the setting output voltage. The TPS55288-Q1 operates in buck mode when the input voltage is greater than the output voltage and in boost mode when the input voltage is less than the output voltage. When the input voltage is close to the output voltage, the TPS55288-Q1 operates in one-cycle buck and one-cycle boost mode alternately. The switching frequency is set by an external resistor. To reduce the switching power loss in high power conditions, it is recommended to set the switching frequency below 500 kHz. If a system requires higher switching frequency above 500 kHz, it is recommended to set the lower switch current limit for better thermal performance.

8.2 Typical Application

The TPS55288-Q1 provides a small size solution for USB PD power supply application with the input voltage ranging from 9 V to 36 V.

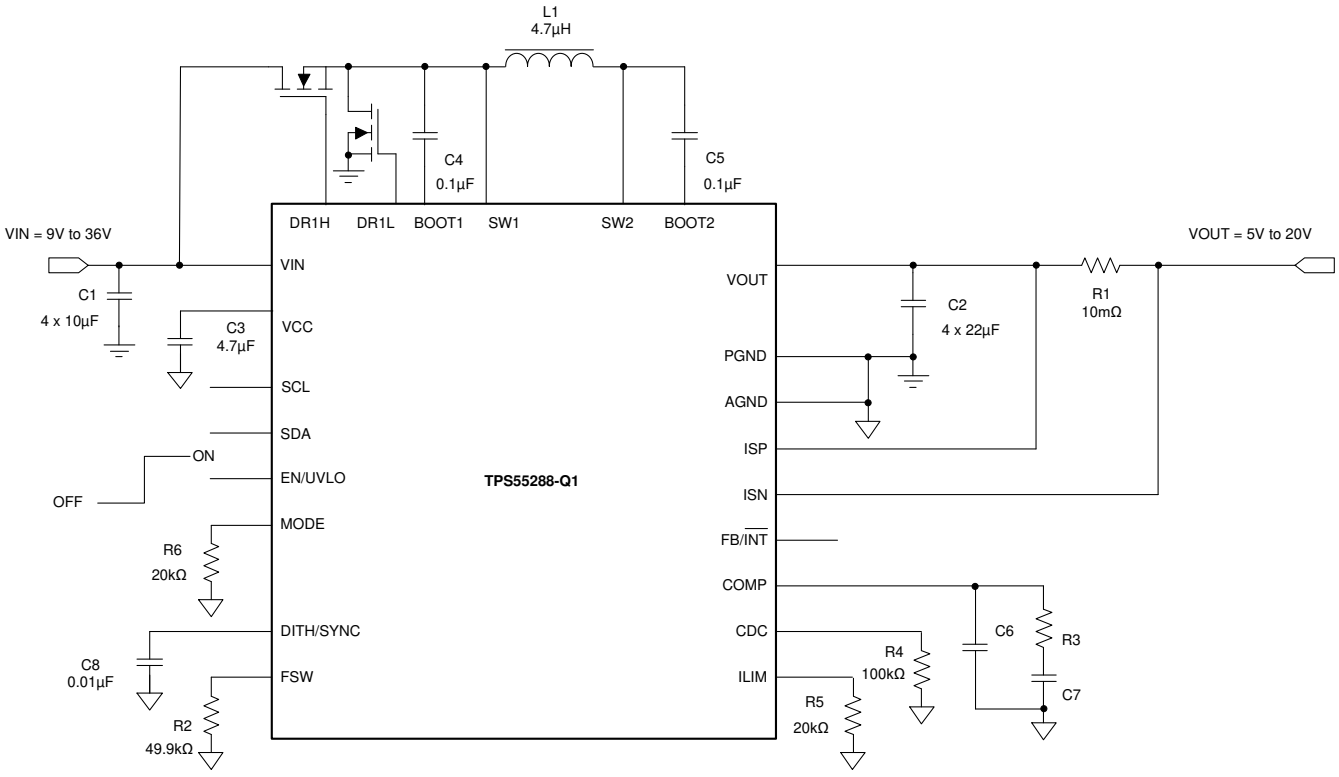


图 8-1. USB PD Power Supply With 9-V to 36-V Input Voltage

8.2.1 Design Requirements

The design parameters are listed in 表 8-1:

表 8-1. Design Parameters

PARAMETERS	VALUES
Input voltage	9 V to 36 V
Output voltage	5 V to 20 V
Output current limit	5 A
Output voltage ripple	±50 mV
Operating mode at light load	PFM

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS55288-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Switching Frequency

The switching frequency of the TPS55288-Q1 is set by a resistor at the FSW pin. Use Equation 3 to calculate the resistance for the desired frequency. To reduce the switching power loss with such a high current application, a 1% standard resistor of 49.9 kΩ is selected for 400-kHz switching frequency for this application.

8.2.2.3 Output Voltage Setting

The TPS55288-Q1 has I^2C interface to set the internal reference voltage. A microcontroller can easily set the desired output voltage by writing the proper data into the reference voltage registers through I^2C bus.

8.2.2.4 Inductor Selection

Since the selection of the inductor affects steady state operation, transient behavior, and loop stability, the inductor is the most important component in power regulator design. There are three important inductor specifications: inductance, saturation current, and DC resistance.

The TPS55288-Q1 is designed to work with inductor values between 1 µH and 10 µH. The inductor selection is based on consideration of both buck and boost modes of operation.

For buck mode, the inductor selection is based on limiting the peak-to-peak current ripple to the maximum inductor current at the maximum input voltage. In CCM, Equation 9 shows the relationship between the inductance and the inductor ripple current.

$$L = \frac{(V_{IN(MAX)} - V_{OUT}) \times V_{OUT}}{\Delta I_{L(P-P)} \times f_{SW} \times V_{IN(MAX)}} \quad (9)$$

where

- $V_{IN(MAX)}$ is the maximum input voltage
- V_{OUT} is the output voltage
- $\Delta I_{L(P-P)}$ is the peak to peak ripple current of the inductor
- f_{SW} is the switching frequency

For a certain inductor, the inductor ripple current achieves maximum value when VOUT equals half of the maximum input voltage. Choosing higher inductance gets smaller inductor current ripple while smaller inductance gets larger inductor current ripple.

For boost mode, the inductor selection is based on limiting the peak-to-peak current ripple to the maximum inductor current at the maximum output voltage. In CCM, Equation 10 shows the relationship between the inductance and the inductor ripple current.

$$L = \frac{V_{IN} \times (V_{OUT(MAX)} - V_{IN})}{\Delta I_{L(P-P)} \times f_{SW} \times V_{OUT(MAX)}} \quad (10)$$

where

- V_{IN} is the input voltage
- $V_{OUT(MAX)}$ is the maximum output voltage
- $\Delta I_{L(P-P)}$ is the peak to peak ripple current of the inductor
- f_{SW} is the switching frequency

For a certain inductor, the inductor ripple current achieves maximum value when V_{IN} equals to the half of the maximum output voltage. Choosing higher inductance gets smaller inductor current ripple while smaller inductance gets larger inductor current ripple.

For this application example, a 4.7-µH inductor is selected, which produces approximate maximum inductor current ripple of 50% of the highest average inductor current in buck mode and 50% of the highest average inductor current in boost mode.

In buck mode, the inductor DC current equals to the output current. In boost mode, the inductor DC current can be calculated with Equation 11.

$$I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (11)$$

where

- V_{OUT} is the output voltage
- I_{OUT} is the output current
- V_{IN} is the input voltage
- η is the power conversion efficiency

For a given maximum output current of the buck-boost converter TPS55288-Q1, the maximum inductor DC current happens at the minimum input voltage and maximum output voltage. Set the inductor current limit of the TPS55288-Q1 higher than the calculated maximum inductor DC current to make sure the TPS55288-Q1 has the desired output current capability.

In boost mode, the inductor ripple current is calculated with Equation 12.

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{L \times f_{SW} \times V_{OUT}} \quad (12)$$

where

- $\Delta I_{L(P-P)}$ is the inductor ripple current
- L is the inductor value

- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Therefore, the inductor peak current is calculated with Equation 13.

$$I_{L(P)} = I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2} \quad (13)$$

Normally, it is advisable to work with an inductor peak-to-peak current of less than 40% of the average inductor current for maximum output current. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI, but in the same way, load transient response time is increased. The selected inductor must have higher saturation current than the calculated peak current.

The conversion efficiency is dependent on the resistance of its current path. The switching loss associated with the switching MOSFETs, and the inductor core loss. Therefore, the overall efficiency is affected by the inductor DC resistance (DCR), equivalent series resistance (ESR) at the switching frequency, and the core loss. 表 8-2 lists recommended inductors for the TPS55288-Q1. In this application example, the Coilcraft inductor XAL1010-472 is selected for its small size, high saturation current, and small DCR.

表 8-2. Recommended Inductors

PART NUMBER	L (µH)	DCR (MAXIMUM) (mΩ)	SATURATION CURRENT / HEAT RATING CURRENT (A)	SIZE (L x W x H mm)	VENDOR(1)
XAL1010-472ME	4.7	10	25.4/17.5	11.3 × 10 × 10	Coilcraft
IHLP5050EZER4R7	4.7	10.1	17.8/15.3	13.5 × 12.9 × 5	Vishay
125CDMCCDS-4R7MC	4.7	10	22/14	13.5 × 12.6 × 5	Sumida

(1) See the *Third-party Products* disclaimer.

8.2.2.5 Input Capacitor

In buck mode, the input capacitor supplies high ripple current. The RMS current in the input capacitors is given by Equation 14.

$$I_{CIN(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times V_{IN}}} \quad (14)$$

where

- $I_{CIN(RMS)}$ is the RMS current through the input capacitor
- I_{OUT} is the output current

The maximum RMS current occurs at the output voltage is half of the input voltage, which gives $I_{CIN(RMS)} = I_{OUT} / 2$. Ceramic capacitors are recommended for their low ESR and high ripple current capability. A total of 20 µF effective capacitance is a good starting point for this application.

8.2.2.6 Output Capacitor

In boost mode, the output capacitor conducts high ripple current. The output capacitor RMS ripple current is given by Equation 15, where the minimum input voltage and the maximum output voltage correspond to the maximum capacitor current.

$$I_{COUT(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} - 1} \quad (15)$$

where

- $I_{COUT(RMS)}$ is the RMS current through the output capacitor
- I_{OUT} is the output current

In this example, the maximum output ripple RMS current is 5.5 A.

The ESR of the output capacitor causes an output voltage ripple given by Equation 16 in boost mode.

$$V_{RIPPLE(ESR)} = \frac{I_{OUT} \times V_{OUT}}{V_{IN}} \times R_{COUT} \quad (16)$$

where

- R_{COUT} is the ESR of the output capacitance

The capacitance also causes a capacitive output voltage ripple given by Equation 17 in boost mode. When input voltage reaches the minimum value and the output voltage reaches the maximum value, there is the largest output voltage ripple caused by the capacitance.

$$V_{RIPPLE(CAP)} = \frac{I_{OUT} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right)}{C_{OUT} \times f_{SW}} \quad (17)$$

Typically, a combination of ceramic capacitors and bulk electrolytic capacitors is needed to provide low ESR, high ripple current, and small output voltage ripple. From the required output voltage ripple, use Equation 16 and Equation 17 to calculate the minimum required effective capacitance of the C_{OUT}.

8.2.2.7 Output Current Limit

The output current limit is implemented by putting a current sense resistor between the ISP and ISN pins along with setting a limit voltage between the ISP pin and the ISN pin through register 02h. The maximum value of the limit voltage between the ISP and ISN pins is 63.5 mV. The default limit voltage is 50 mV. The current sense resistor between the ISP and ISN pins should be selected to ensure that the output current limit is set high enough for output. The output current limit setting resistor is given by Equation 18.

$$R_{SNS} = \frac{V_{SNS}}{I_{OUT\_LIMIT}} \quad (18)$$

where

- V_{SNS} is the current limit setting voltage between the ISP and ISN pins
- I_{OUT_LIMIT} is the desired output current limit

Because the power dissipation is large, make sure the current sense resistor has enough power dissipation capability with large package.

8.2.2.8 Loop Stability

The TPS55288-Q1 uses average current control scheme. The inner current loop uses internal compensation and requires the inductor value must be larger than $1.2/f_{SW}$. The outer voltage loop requires an external compensation. The COMP pin is the output of the internal voltage error amplifier. An external compensation network comprised of resistor and ceramic capacitors is connected to the COMP pin.

The TPS55288-Q1 operates in buck mode or boost mode. Therefore, both buck and boost operating modes require loop compensations. The restrictive one of both compensations is selected as the overall compensation from a loop stability point of view. Typically for a converter designed either work in buck mode or boost mode, the boost mode compensation design is more restrictive due to the presence of a right half plane zero (RHPZ).

The power stage in boost mode can be modeled by Equation 19.

$$G_{PS}(s) = \frac{R_{LOAD} \times (1-D)}{2 \times R_{SENSE}} \times \frac{\left(1 + \frac{s}{2\pi \times f_{ESRZ}}\right) \times \left(1 - \frac{s}{2\pi \times f_{RHPZ}}\right)}{1 + \frac{s}{2\pi \times f_P}} \quad (19)$$

where

- R_{LOAD} is the output load resistance
- D is the switching duty cycle in boost mode
- R_{SENSE} is the equivalent internal current sense resistor, which is 0.055 Ω

The power stage has two zeros and one pole generated by the output capacitor and load resistance. Use 方程式 20 to Equation 22 to calculate them.

$$f_P = \frac{2}{2\pi \times R_{LOAD} \times C_{OUT}} \quad (20)$$

$$f_{ESRZ} = \frac{1}{2\pi \times R_{COUT} \times C_{OUT}} \quad (21)$$

$$f_{RHPZ} = \frac{R_{LOAD} \times (1-D)^2}{2\pi \times L} \quad (22)$$

The internal transconductance amplifier together with the compensation network at the COMP pin constitutes the control portion of the loop. The transfer function of the control portion is shown by Equation 23.

$$G_C(s) = \frac{G_{EA} \times R_{EA} \times V_{REF}}{V_{OUT}} \times \frac{\left(1 + \frac{s}{2\pi \times f_{COMZ}}\right)}{\left(1 + \frac{s}{2\pi \times f_{COMP1}}\right) \times \left(1 + \frac{s}{2\pi \times f_{COMP2}}\right)} \quad (23)$$

where

- G_{EA} is the transconductance of the error amplifier
- R_{EA} is the output resistance of the error amplifier
- V_{REF} is the reference voltage input to the error amplifier
- V_{OUT} is the output voltage
- f_{COMP1} and f_{COMP2} are the pole’s frequency of the compensation network
- f_{COMZ} is the zero’s frequency of the compensation network

The total open-loop gain is the product of $G_{PS}(s)$ and $G_C(s)$. The next step is to choose the loop crossover frequency, f_C, at which the total open-loop gain is 1, namely 0 dB. The higher in frequency that the loop gain stays above 0 dB before crossing over, the faster the loop response. It is generally accepted that the loop gain cross over 0 dB at the frequency no higher than the lower of either 1/10 of the switching frequency, f_{SW} or 1/5 of the RHPZ frequency, f_{RHPZ}.

Then, set the value of R_C, C_C, and C_P by Equation 24 to Equation 26.

$$R_C = \frac{2\pi \times V_{OUT} \times R_{SENSE} \times C_{OUT} \times f_C}{(1-D) \times V_{REF} \times G_{EA}} \quad (24)$$

where

- f_C is the selected crossover frequency

$$C_C = \frac{R_{LOAD} \times C_{OUT}}{2 \times R_C} \quad (25)$$

$$C_P = \frac{R_{COUT} \times C_{OUT}}{R_C} \quad (26)$$

If the calculated C_P is less than 10 pF, it can be left open.

Designing the loop for greater than 45° of phase margin and greater than 10-dB gain margin eliminates output voltage ringing during the line and load transient.

8.2.3 Application Curves

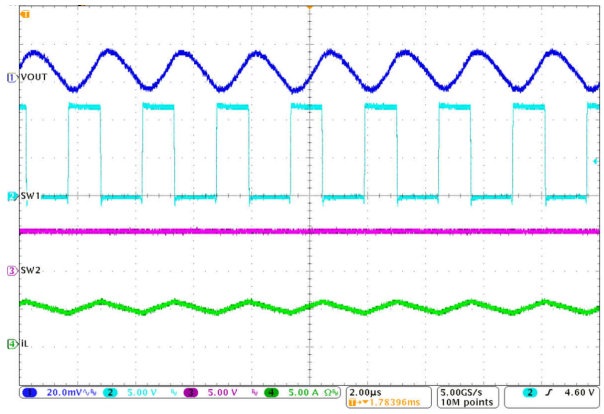


图 8-2. Switching Waveforms in V_{IN} = 12 V, V_{OUT} = 5 V, I_O = 5 A, FPWM

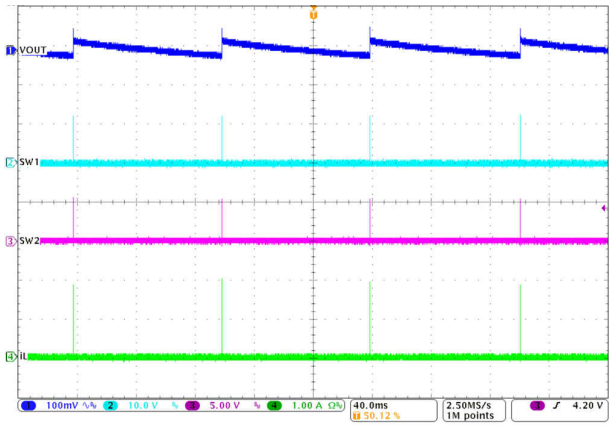


图 8-3. Switching Waveforms in V_{IN} = 12 V, V_{OUT} = 5 V, I_O = 0 A, PFM

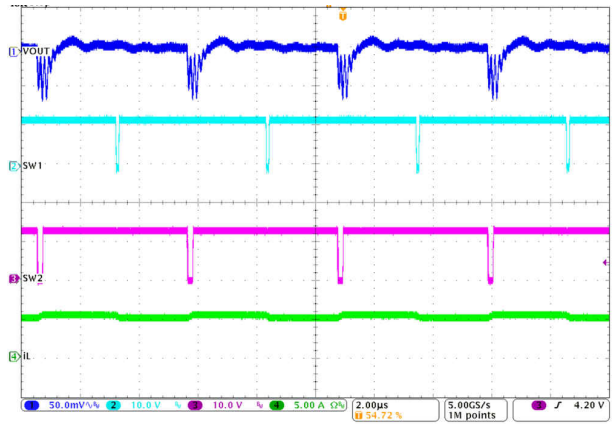


图 8-4. Switching Waveforms in V_{IN} = 12 V, V_{OUT} = 12 V, I_O = 5 A, FPWM

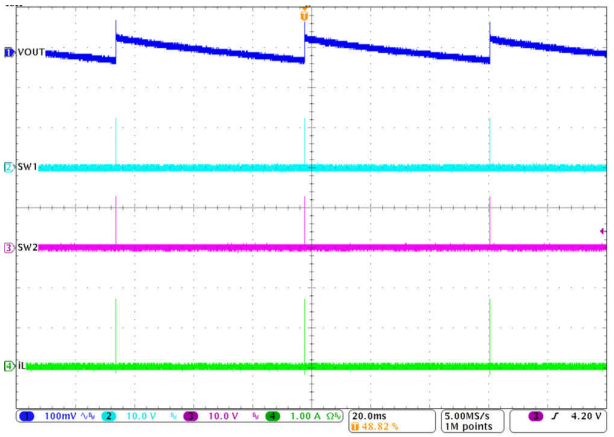


图 8-5. Switching Waveforms in V_{IN} = 12 V, V_{OUT} = 12 V, I_O = 0 A, PFM

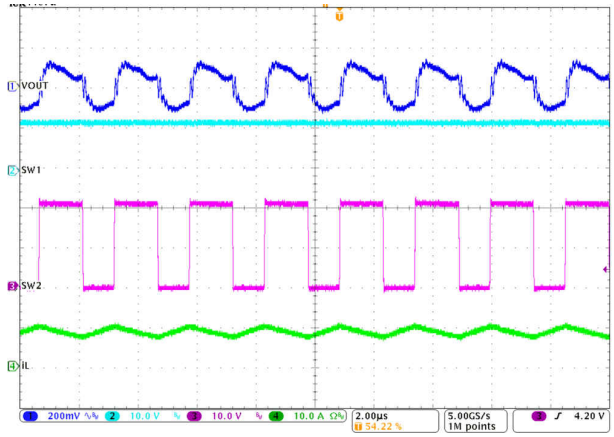


图 8-6. Switching Waveforms in V_{IN} = 12 V, V_{OUT} = 20 V, I_O = 5 A, FPWM

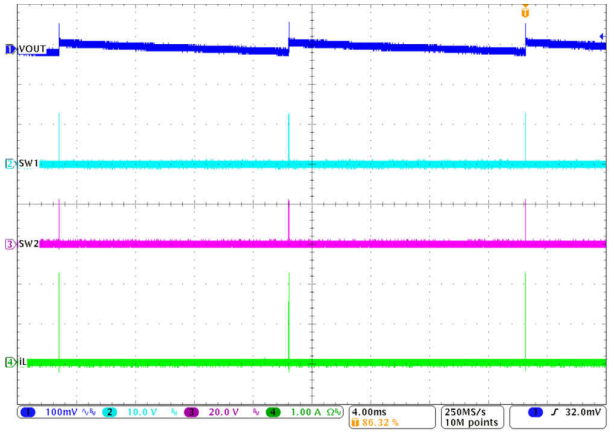


图 8-7. Switching Waveforms in V_{IN} = 12 V, V_{OUT} = 20 V, I_O = 0 A, PFM

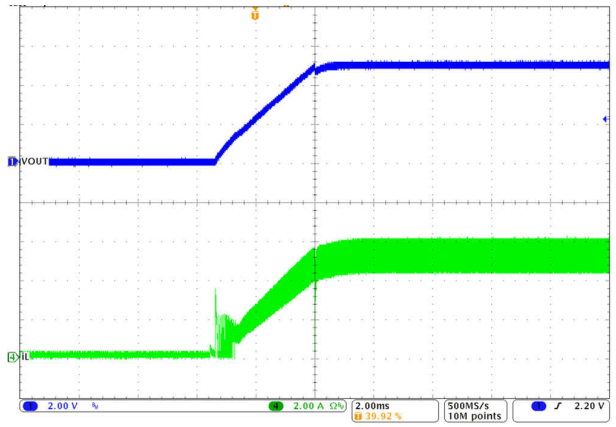


图 8-8. Start-up Waveforms in V_{IN} = 12 V, V_{OUT} = 5 V, I_O = 5 A, FPWM

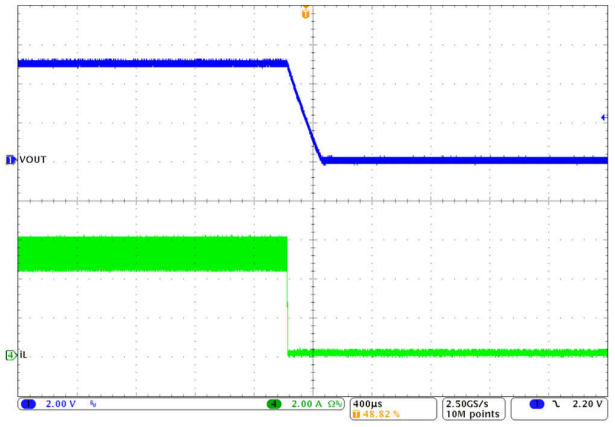


图 8-9. Shutdown Waveforms in V_{IN} = 12 V, V_{OUT} = 5 V, I_O = 5 A, FPWM

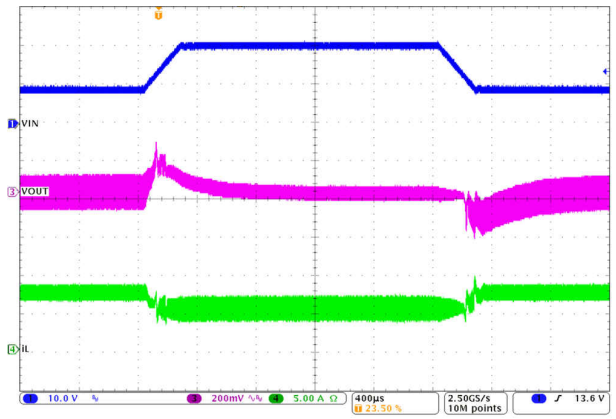


图 8-10. Line Transient Waveforms in V_{IN} = 9 V to 20 V, V_{OUT} = 12 V, I_O = 5 A with 200-µs Slew Rate, FPWM

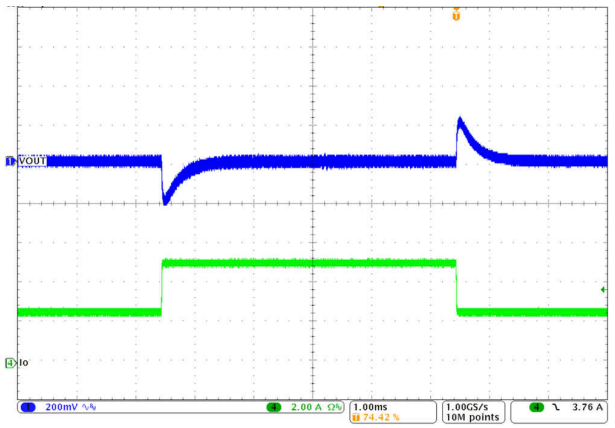


图 8-11. Load Transient Waveforms in V_{IN} = 12 V, V_{OUT} = 5 V, I_O = 2.5 A to 5 A with 20-µs Slew Rate, FPWM

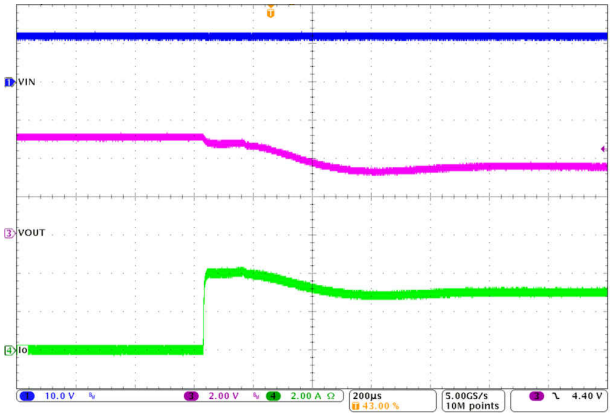


图 8-12. 3-A Output Current Limit Waveforms in V_{IN} = 12 V, V_{OUT} = 5 V, R_{LOAD} = 1.2 Ω, FPWM

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.7 V to 36 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. A typical choice is an aluminum electrolytic capacitor with a value of 100 μF.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If layout is not carefully done, the regulator can suffer from instability and noise problems. To maximize efficiency, switching rise time and fall time are very fast. To prevent radiation of high-frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW1 and SW2 pins, and always use a ground plane under the switching regulator to minimize interplane coupling. The input capacitor needs to be close to the VIN pin and the PGND to reduce the input supply current ripple.

The most critical current path for buck converter portion is from the switching FET at the buck side, through the rectifier FET at the buck side to the PGND, then the input capacitors, and back to the input of the switching FET. This high current path contains nanosecond rise time and fall time, and should be kept as short as possible. Therefore, the input capacitor for power stage must be close to the input of the switching FET and the PGND terminal of the rectifier FET.

The most critical current path for boost converter portion is from the switching FET at the boost side, through the rectifier FET at boost side, then the output capacitors, and back to ground of the switching FET. This high current path contains nanosecond rise time and fall time, and should be kept as short as possible. Therefore, the output capacitor needs not only to be close to the VOUT pin, but also to the PGND pin to reduce the overshoot at the SW2 pin and the VOUT pin.

The traces from the output current sensing resistor to the ISP pin and the ISN pin must be in parallel and close to each other to avoid noise coupling.

The PGND plane and the AGND plane are connected at the terminal of the capacitor at the VCC pin. Thus the noise caused by the MOSFET driver and parasitic inductance does not interfere with the AGND and internal control circuit.

To get good thermal performance, it is recommended to use thermal vias beneath the TPS55288-Q1 connecting the PGND pin to the PGND plane, and the VOUT pin to a large VOUT area separately.

10.2 Layout Example

trace on bottom layer

AGND plane on an inner layer

The first inner layer is the PGND plane

AGND plane connects to PGND plane at the terminal of the capacitor at the VCC pin

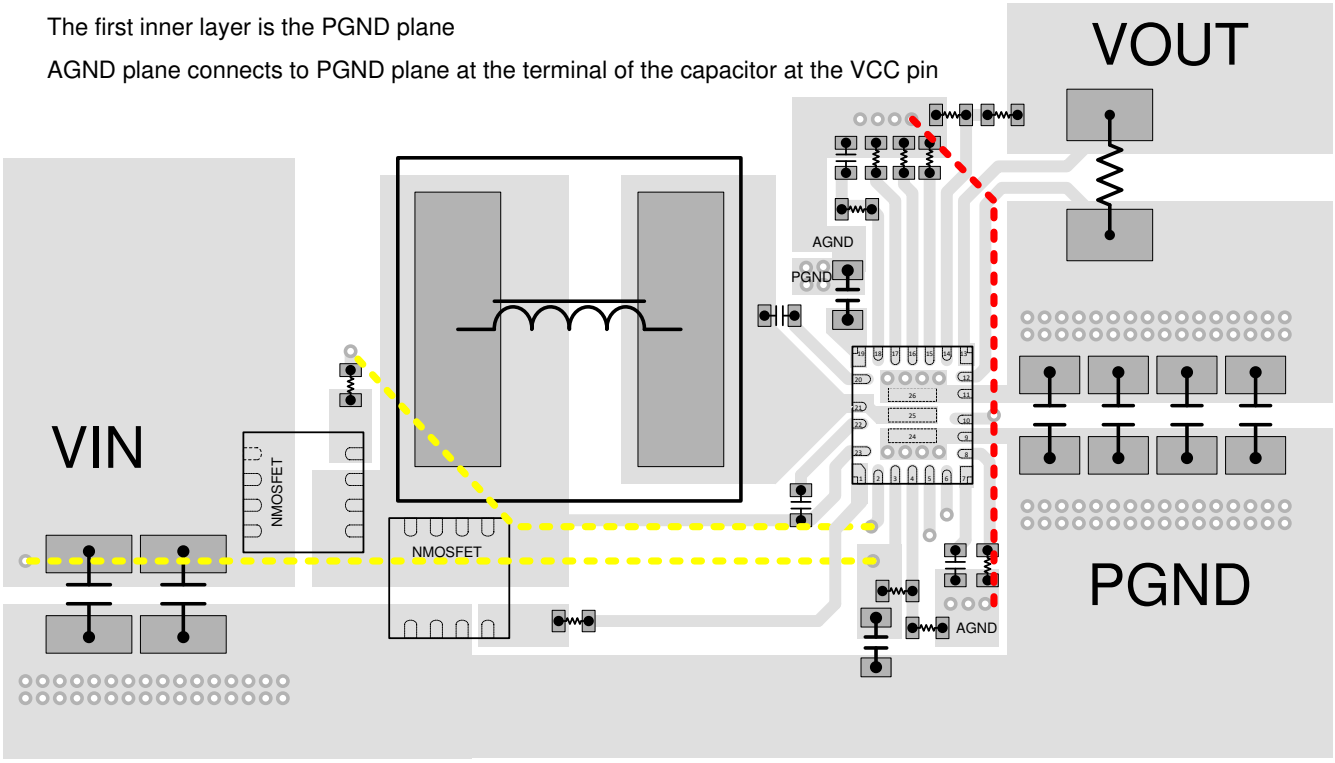


图 10-1. Layout Example

11 Device and Documentation Support

11.1 Device Support

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11.1.2 Development Support

11.1.2.1 Custom Design With WEBENCH® Tools

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1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
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- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

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所有商标均为其各自所有者的财产。

11.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS55288QRPMRQ1	ACTIVE	VQFN-HR	RPM	26	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	55288Q	Samples
TPS55288QWRPMRQ1	ACTIVE	VQFN-HR	RPM	26	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	55288W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS55288-Q1 :

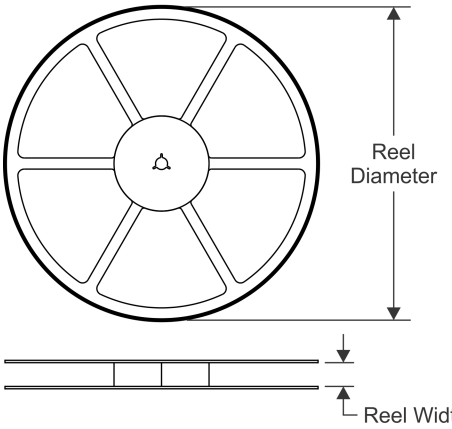
- Catalog : TPS55288

NOTE: Qualified Version Definitions:

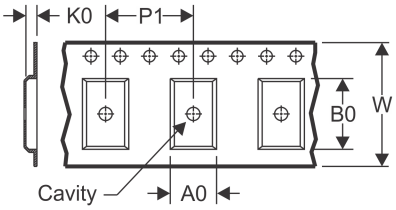
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

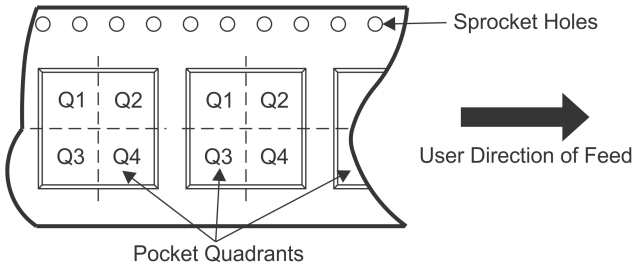


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

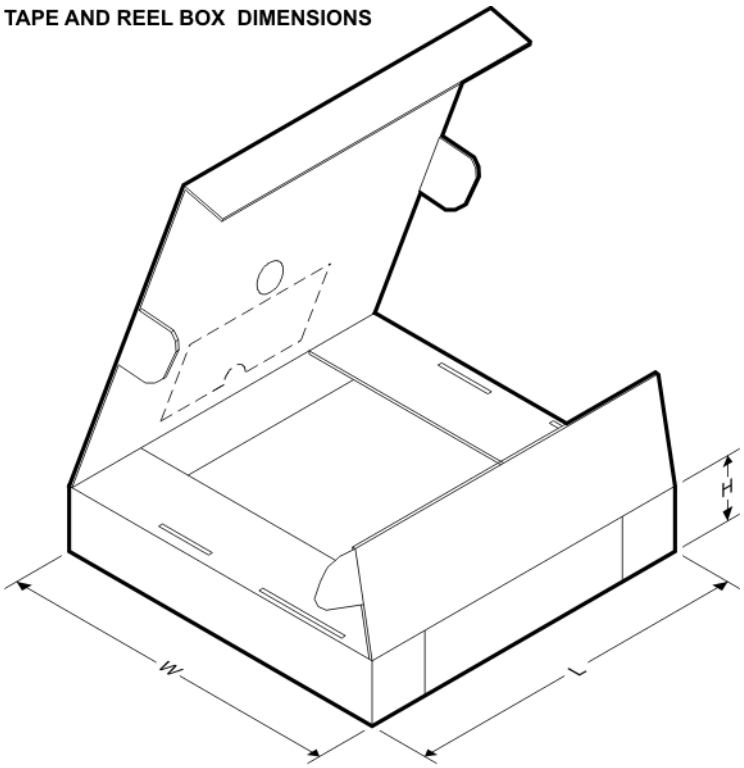
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS55288QRPMRQ1	VQFN-HR	RPM	26	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q2
TPS55288QWRPMRQ1	VQFN-HR	RPM	26	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS55288QRPMRQ1	VQFN-HR	RPM	26	3000	367.0	367.0	35.0
TPS55288QWRPMRQ1	VQFN-HR	RPM	26	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

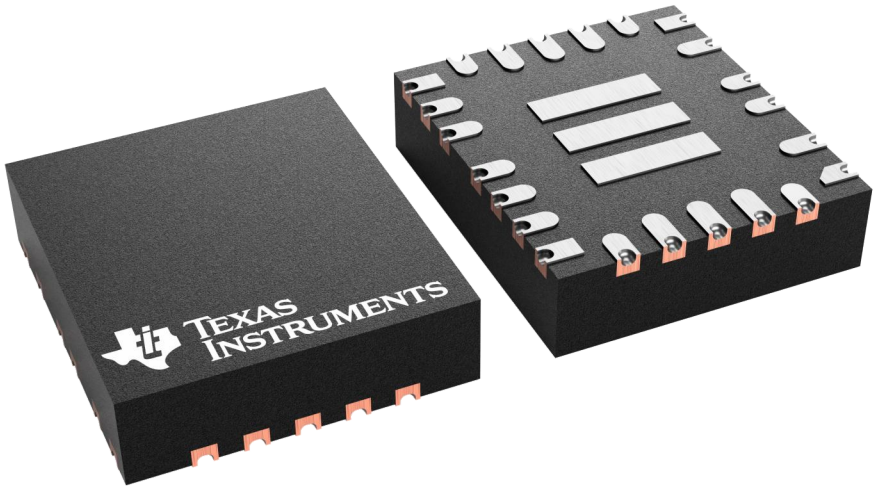
RPM 26

VQFN-HR - 1 mm max height

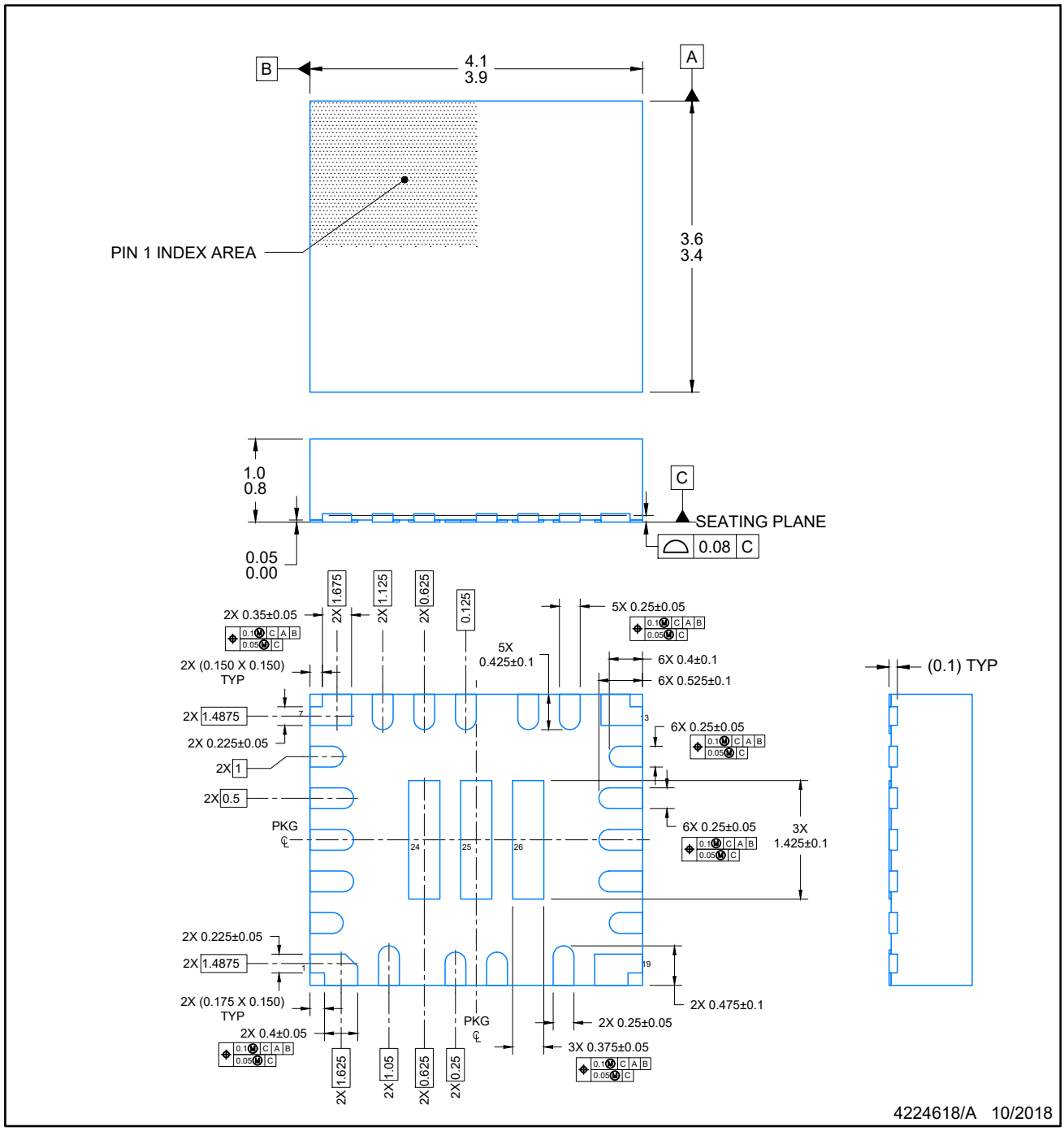
3.5 x 4, 0.5 mm pitch

VERY THIN QUAD FLATPACK-HotRod

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

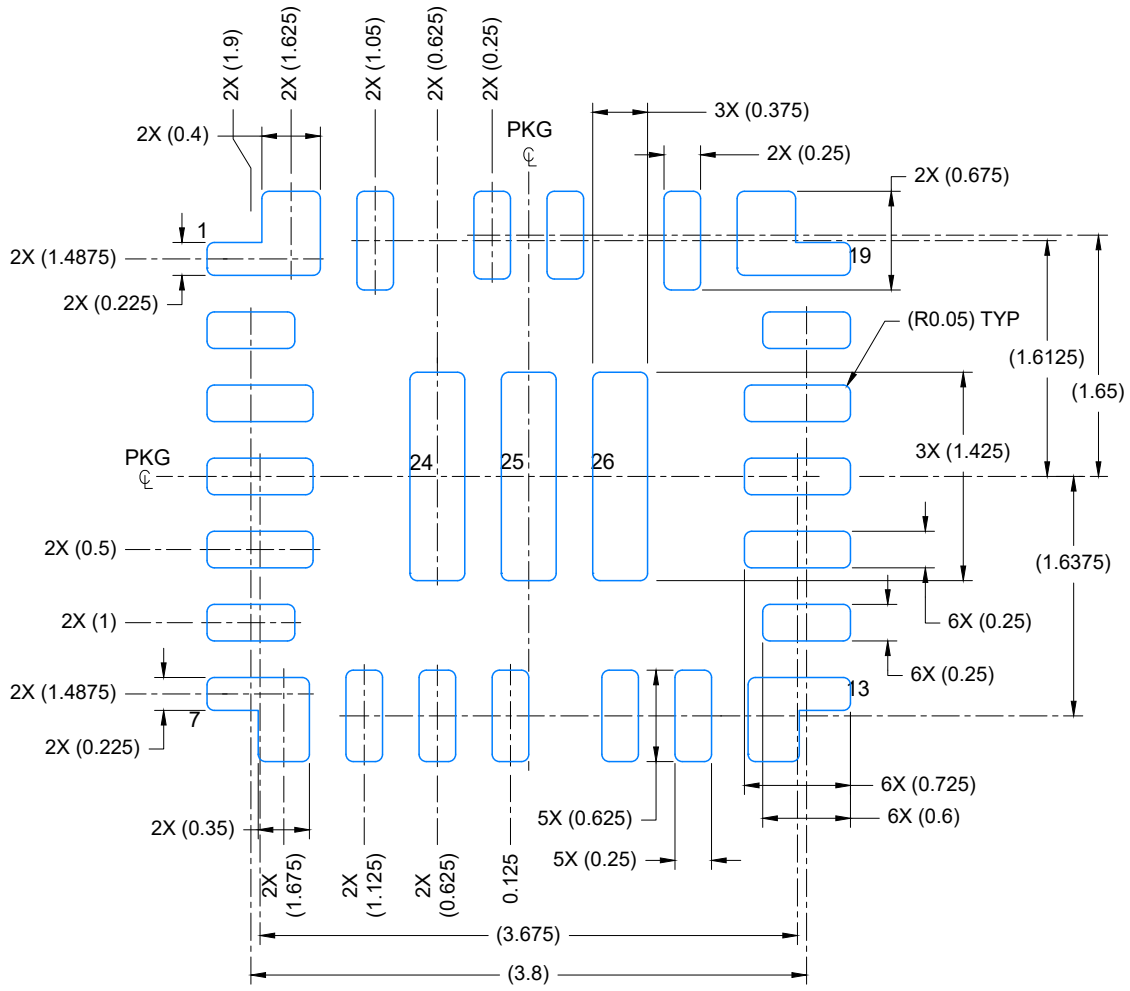


4226451/A

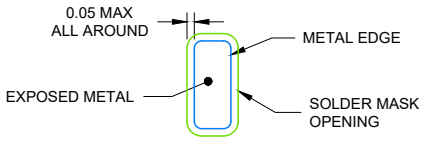


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



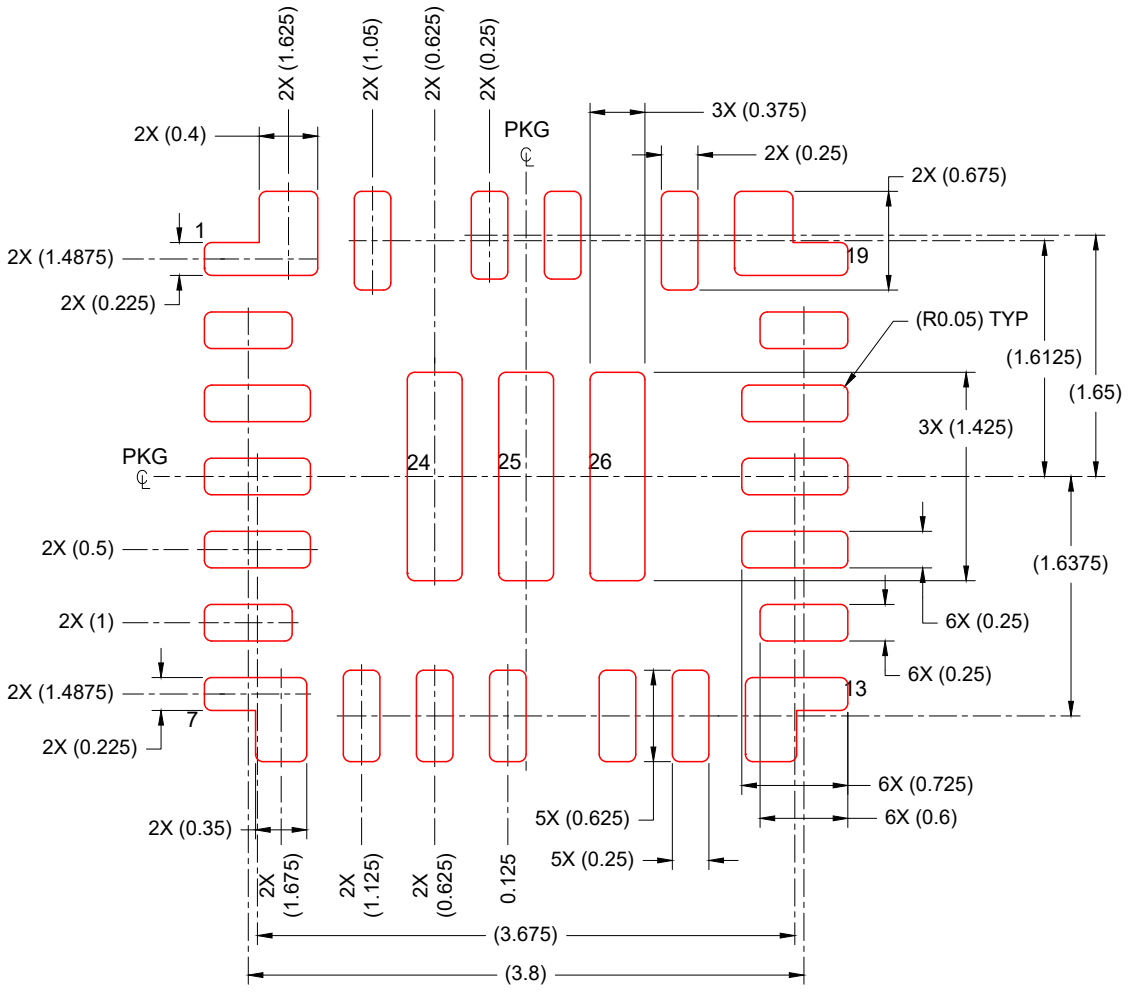
NON SOLDER MASK
DEFINED

SOLDER MASK DETAIL

4224618/A 10/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 20X

4224618/A 10/2018

NOTES: (continued)

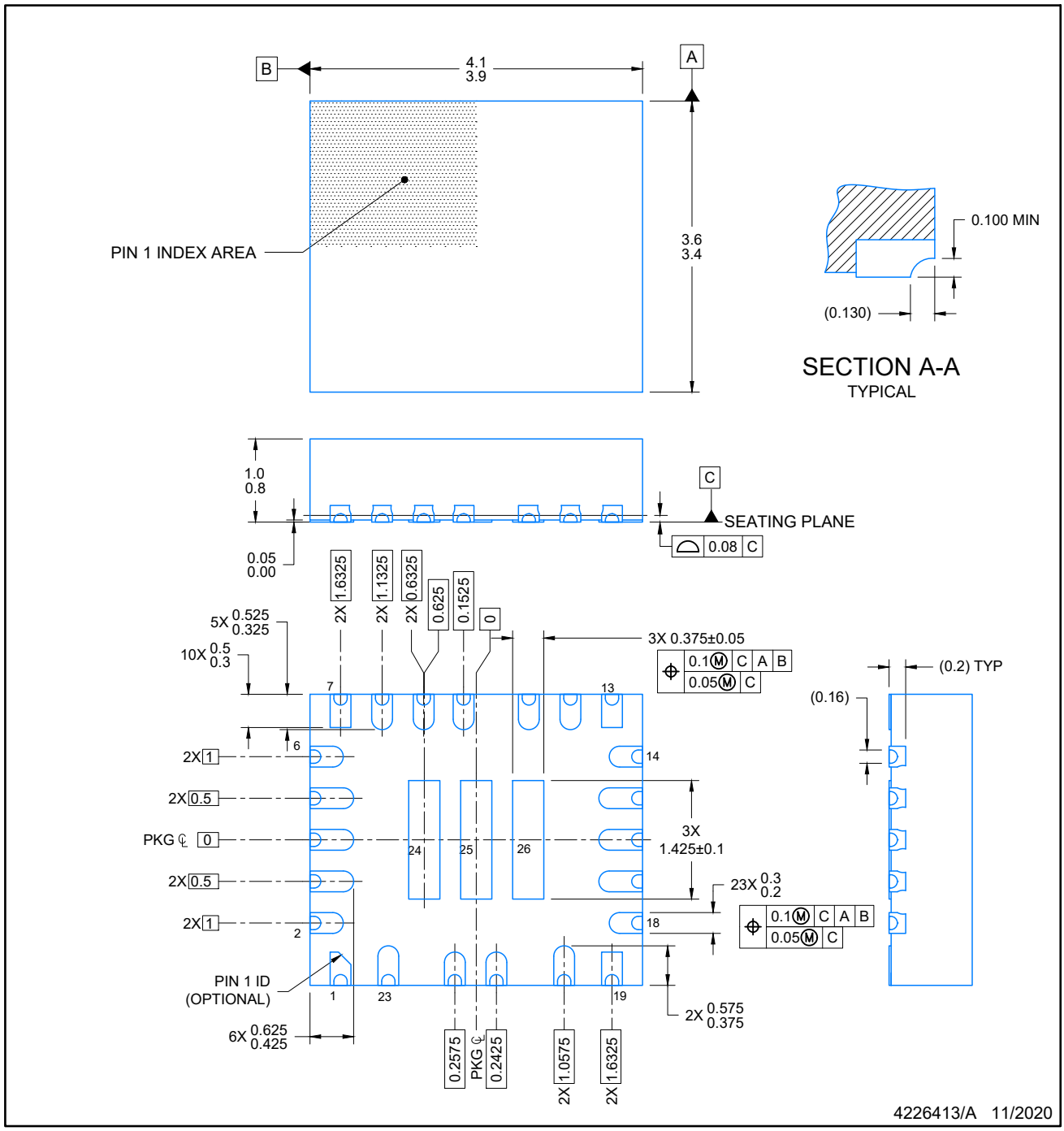
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

RPM0026B

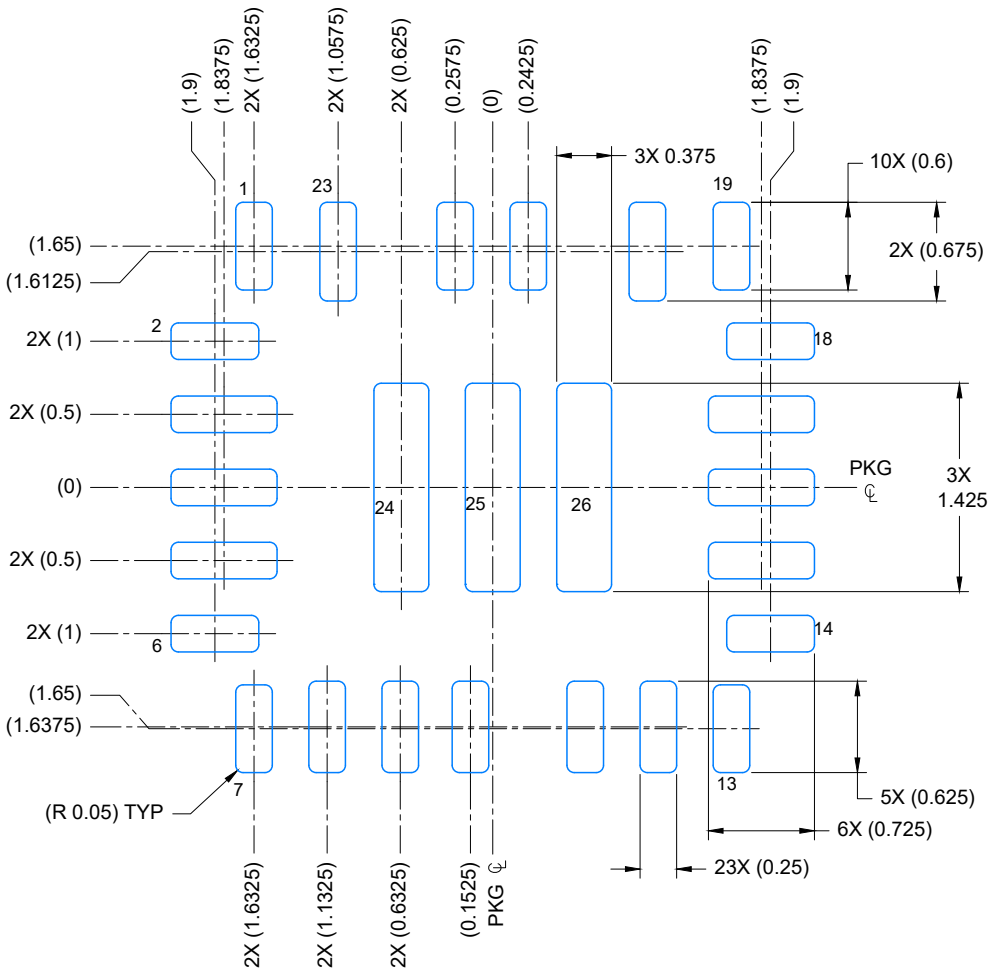
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

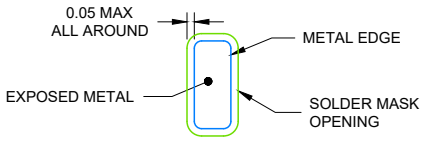


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



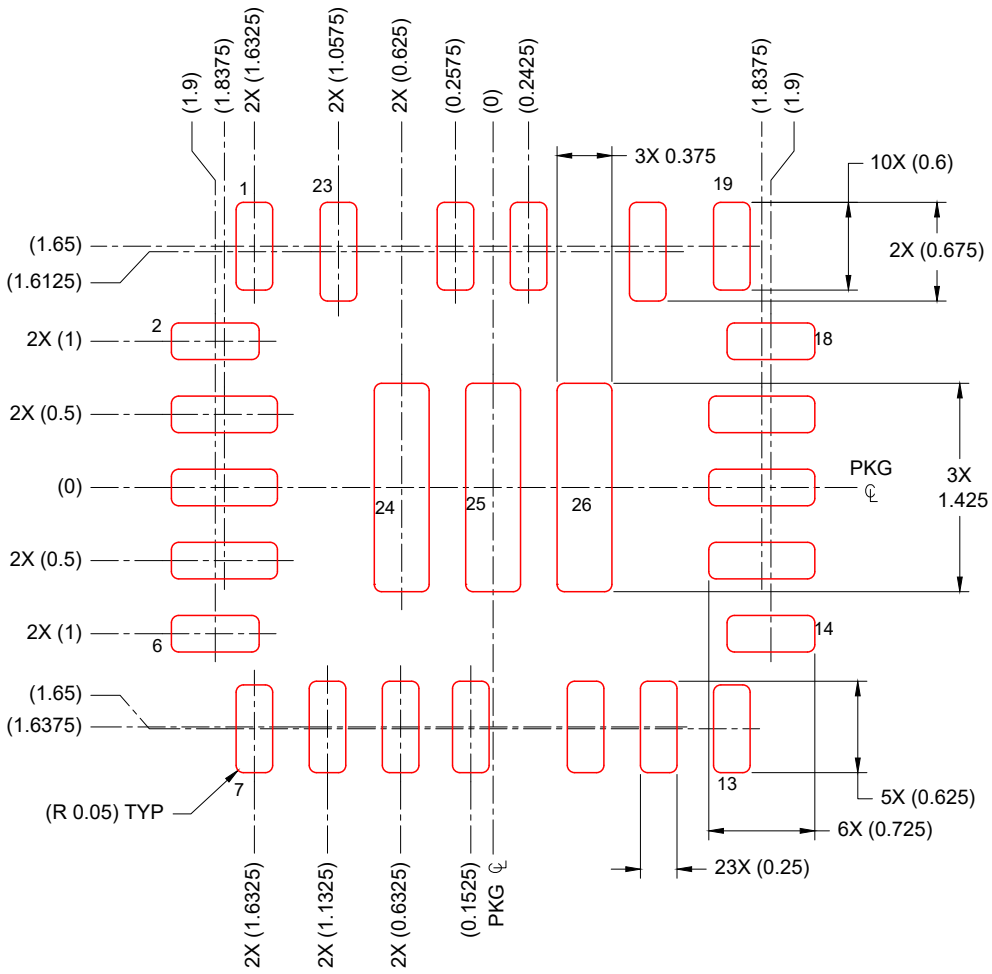
NON SOLDER MASK
DEFINED

SOLDER MASK DETAIL

4226413/A 11/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 20X

4226413/A 11/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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