UCC2813-x-Q1 Low-Power Economy BiCMOS Current-Mode PWM

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C T_A
  - Device HBM classification level 2: ±2 kV
  - Device CDM classification level C5: >1000 V
- 100-µA typical starting supply current
- 500-µA typical operating supply current
- Operation to 1 MHz
- Internal soft start
- Internal fault soft start
- Internal leading-edge blanking of the current-sense signal
- 1-A totem-pole output
- 70-ns typical response from current-sense to gate-drive output
- 1.5% tolerance voltage reference
- Same pinout as the UCC3802 device, UC3842 device, and UC3842A device families

2 Applications

- Automotive power supplies
- Auxiliary power supply for automotive hybrid and electric vehicles
- AC and DC power supplies

3 Description

The UCC2813-x-Q1 device family of high-speed, low-power integrated circuits contains all of the control and drive components required for off-line and DC-to-DC fixed-frequency current-mode switching power supplies with minimal parts count.

These devices have the same pin configuration as the UC284x device family, and also offer the added features of internal full-cycle soft start and internal leading-edge blanking of the current-sense input.

The UCC2813-x-Q1 device family offers a variety of package options, choice of maximum duty cycle, and choice of critical voltage levels. Devices with lower reference voltage such as the UCC2813-3-Q1 and UCC2813-5-Q1 fit best into battery operated systems, while the higher reference and the higher UVLO hysteresis of the UCC2813-2-Q1 device and UCC2813-4-Q1 device make these ideal choices for use in off-line power supplies.

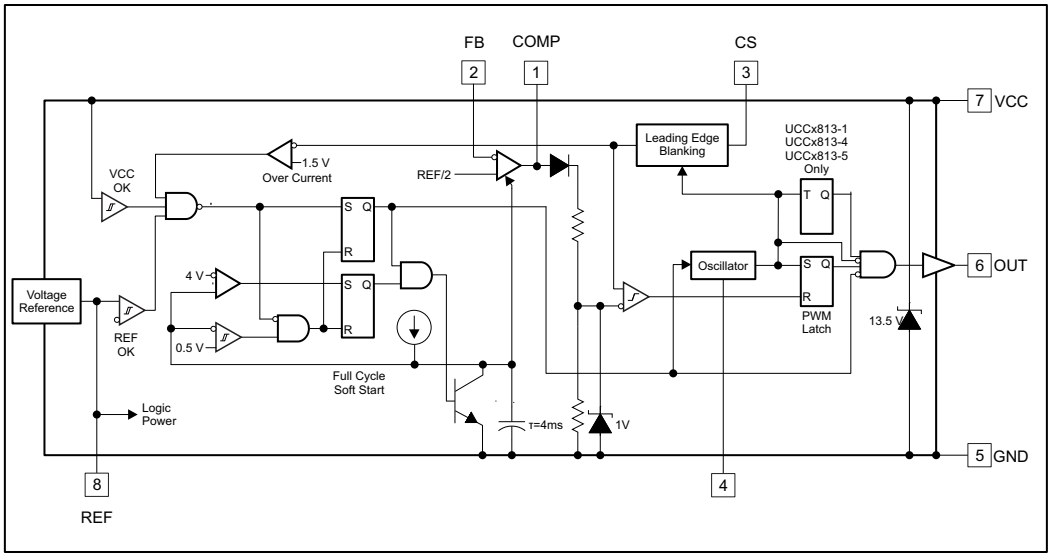
The UCC2813-x-Q1 device series is specified for operation from –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC2813-x-Q1	SOIC (8)	3.91 mm × 4.90 mm
	TSSOP (8)	4.40 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (October 2019) to Revision E	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1
• Changed Updated notes under Abs Max table	4
• Changed Additional information to Power Supply Recommendation section	33

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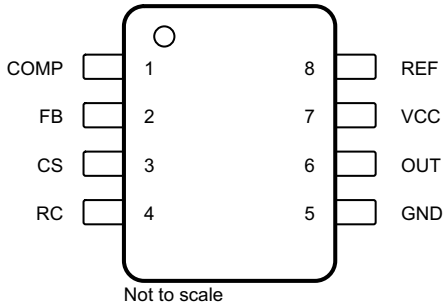
5 Device Comparison Table

PART NUMBER(1)	MAXIMUM DUTY CYCLE	REFERENCE VOLTAGE	TURNON THRESHOLD	TURNOFF THRESHOLD	UNIT
UCC2813-0-Q1	100%	5	7.2	6.9	V
UCC2813-1-Q1	50%	5	9.4	7.4	V
UCC2813-2-Q1	100%	5	12.5	8.3	V
UCC2813-3-Q1	100%	4	4.1	3.6	V
UCC2813-4-Q1	50%	5	12.5	8.3	V
UCC2813-5-Q1	50%	4	4.1	3.6	V

(1) The *x* in the part number refers to the operating temperature range difference between the UCC2813 devices and the UCC2813 devices.

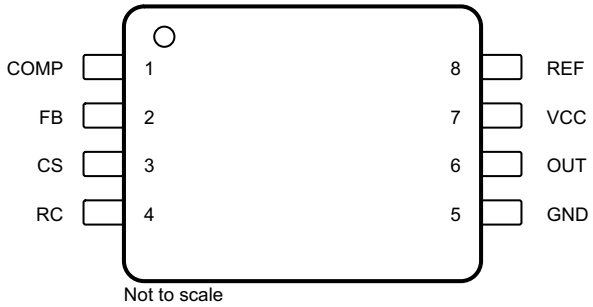
6 Pin Configuration and Functions

N and D Packages
8-Pin PDIP and SOIC
Top View



Not to scale

PW Package
8-Pin TSSOP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COMP	1	O	COMP is the output of the error amplifier and the input of the PWM comparator. Feedback loop compensation is applied between this pin and the FB pin.
CS	3	I	CS is the input to the current-sense comparators: the PWM comparator and the overcurrent comparator.
FB	2	I	FB is the inverting input of the error amplifier.
GND	5	—	GND is the reference ground and power ground for all functions of this device.
OUT	6	O	OUT is the output of a high-current power driver capable of driving the gate of a power MOSFET.
RC	4	I	RC is the oscillator timing programming pin. An external resistor and capacitor are applied to this input to program the switching frequency and maximum duty-cycle.
REF	8	O	REF is the voltage reference for the error amplifier and many other functions, and is the bias source for logic functions of this device.
VCC	7	I	VCC is the bias-power input for this device. In normal operation, VCC is connected to a voltage source through a current-limiting resistor.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
VCC voltage(3)			12	V
VCC current			30	mA
OUT current			±1	A
OUT energy (capacitive load)			20	µJ
Analog inputs	FB, CS, RC, COMP	–0.3	6.3 or V_{VCC} + 0.3(4)	V
Power dissipation at T_A < 25°C	N package		1	W
	D package		0.65	
Lead temperature, soldering (10 s)			300	°C
Junction temperature		–55	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) All voltages are with respect to GND. All currents are positive into the specified terminal.
(2) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(3) In normal operation Vcc is powered through a current limit resistor. The resistor must be sized so that the VCC voltage under all operating conditions is below 12 V but above the turnoff threshold. Absolute maximum of 12 V applies when VCC is driven from a low impedance source such that ICC does not exceed 30mA. Failure to limit VCC and ICC to these limits may result in permanent damage of the device.This is further discussed in the *Power Supply Recommendations*
(4) Whichever is smaller.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011(1)	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specifications.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{VCC}	VCC bias supply voltage from a low impedance source			11	V
I_{VCC}	Supply bias current			25	mA
V_{OUT}	Gate driver output voltage		–0.1	V_{VCC}	V
I_{OUT}	Average OUT pin current			20	mA
I_{REF}	REF pin output current			5	mA
	Voltage on analog pins	FB, CS, RC, COMP	–0.1	6 or V_{VCC}(1)	V
f_{OSC}	Oscillator frequency			1	MHz

(1) Whichever is smaller.

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7.4 Thermal Information

THERMAL METRIC(1)		UCC2813-x-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.5	153.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.3	38.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.7	83.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.6	2.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48	82	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and device Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Unless otherwise stated, these specifications apply for –40°C ≤ T_A ≤ 125°C , T_J = T_A; V_{VCC} = 10 V(1); R_T = 100 kΩ from REF to RC; C_T = 330 pF from RC to GND; 0.1-µF capacitor from VCC to GND; 0.1-µF capacitor from VREF to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE						
	Output voltage	T_J = 25°C, I = 0.2 mA, UCC2813-[0,1,2,4]-Q1	4.925	5	5.075	V
		T_J = 25°C, I = 0.2 mA, UCC2813-[3,5]-Q1	3.94	4	4.06	
	Load regulation	0.2 mA < I < 5 mA		10	30	mV
	Total variation	UCC2813-[0,1,2,4]-Q1 (2)	4.84	5	5.1	V
		UCC2813-[3,5]-Q1 (2)	3.84	4	4.08	
	Output noise voltage	10 Hz ≤ f ≤ 10 kHz, T_J = 25°C (3)		70		µV
	Long term stability	T_A = 125°C, 1000 hours (3)		5		mV
	Output short circuit current		–5		–35	mA
OSCILLATOR						
	Oscillator frequency	UCC2813-[0,1,2,4]-Q1 (4)	40	46	52	kHz
		UCC2813-[3,5]-Q1 (4)	26	31	36	
	Temperature stability	See note (3)		2.5%		
	Amplitude peak-to-peak		2.25	2.4	2.55	V
	Oscillator peak voltage			2.45		V
ERROR AMPLIFIER						
	Input voltage	V_{COMP} = 2.5 V; UCC2813-[0,1,2,4]-Q1	2.42	2.5	2.56	V
		V_{COMP} = 2 V; UCC2813-[3,5]-Q1	1.92	2	2.05	
	Input bias current		–2		2	µA
	Open loop voltage gain		60	80		dB
	COMP sink current	V_{FB} = 2.7 V, V_{COMP} = 1.1 V	0.3		3.5	mA
	COMP source current	V_{FB} = 1.8 V, V_{COMP} = V_{REF} – 1.2 V	–0.2	–0.5	–0.8	mA
	Gain-bandwidth product	See note (3)		2		MHz
PWM						
	Maximum duty cycle	UCC2813-[0,2,3]-Q1	97%	99%	100%	
		UCC2813-[1,4,5]-Q1	48%	49%	50%	
	Minimum duty cycle	V_{COMP} = 0 V			0%	

(1) Adjust VCC above the start threshold before setting at 10 V.
(2) Total variation includes temperature stability and load regulation.
(3) Ensured by design. Not 100% tested in production.
(4) Output frequency for the UCC2813-[0,2,3]-Q1 device is the oscillator frequency. Output frequency for the UCC2813-[1,4,5]-Q1 device is one-half the oscillator frequency.

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Electrical Characteristics (continued)

Unless otherwise stated, these specifications apply for –40°C ≤ T_A ≤ 125°C , T_J = T_A; V_{VCC} = 10 V(1); R_T = 100 kΩ from REF to RC; C_T = 330 pF from RC to GND; 0.1-µF capacitor from VCC to GND; 0.1-µF capacitor from VREF to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE						
	Gain	See note (5)	1.1	1.65	1.8	V/V
	Maximum input signal	V_{COMP} = 5 V(6)	0.9	1	1.1	V
	Input bias current		–200		200	nA
	CS blank time		50	100	150	ns
	Over-current threshold		1.32	1.55	1.7	V
	COMP to CS offset	V_{CS} = 0 V	0.45	0.9	1.35	V
OUTPUT						
	OUT low level	I = 20 mA, all parts		0.1	0.4	V
		I = 200 mA, all parts		0.35	0.9	
		I = 50 mA, V_{VCC} = 5 V, UCC2813-[3,5]-Q1		0.15	0.4	
		I = 20 mA, VCC = 0 V, all parts		0.7	1.2	
V_{VCC} – OUT	OUT high V_{sat}	I = –20 mA, all parts		0.15	0.4	V
		I = –200 mA, all parts		1	1.9	
		I = –50 mA, V_{VCC} = 5 V, UCC2813-[3,5]-Q1		0.4	0.9	
	Rise time	C_L = 1 nF		41	70	ns
	Fall time	C_L = 1 nF		44	75	ns
UNDERVOLTAGE LOCKOUT						
	Start threshold (7)	UCC2813-0-Q1	6.6	7.2	7.8	V
		UCC2813-1-Q1	8.6	9.4	10.2	
		UCC2813-[2,4]-Q1	11.5	12.5	13.5	
		UCC2813-[3,5]-Q1	3.7	4.1	4.5	
	Stop threshold (7)	UCC2813-0-Q1	6.3	6.9	7.5	V
		UCC2813-1-Q1	6.8	7.4	8	
		UCC2813-[2,4]-Q1	7.6	8.3	9	
		UCC2813-[3,5]-Q1	3.2	3.6	4	
	Start to stop hysteresis	UCC2813-0-Q1	0.12	0.3	0.48	V
		UCC2813-1-Q1	1.6	2	2.4	
		UCC2813-[2,4]-Q1	3.5	4.2	5.1	
		UCC2813-[3,5]-Q1	0.2	0.5	0.8	
SOFT START						
	COMP rise time	V_{FB} = 1.8 V, Rise from 0.5 V to REF – 1 V		4	10	ms
OVERALL						
	Start-up current	V_{VCC} < start threshold		0.1	0.23	mA
	Operating supply current	V_{FB} = 0 V, V_{CS} = 0 V, V_{RC} = 0 V		0.5	1.2	mA
	VCC internal Zener voltage(7)(8)	I_{VCC} = 10 mA	12	13.5	15	V
	VCC internal Zener voltage minus start-threshold voltage (7)	UCC2813-[2,4]-Q1	0.5	1		V

$$A = \frac{\Delta V_{COMP}}{\Delta V_{CS}} \quad 0 \le V_{CS} \le 0.8\ V$$

(5) Gain is defined by: .
(6) Parameter measured at trip point of latch with FB at 0 V.
(7) Start threshold, stop threshold, and Zener-shunt thresholds track one another.
(8) The device is fully operating in clamp mode as the forcing current is higher than the normal operating supply current.

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7.6 Typical Characteristics

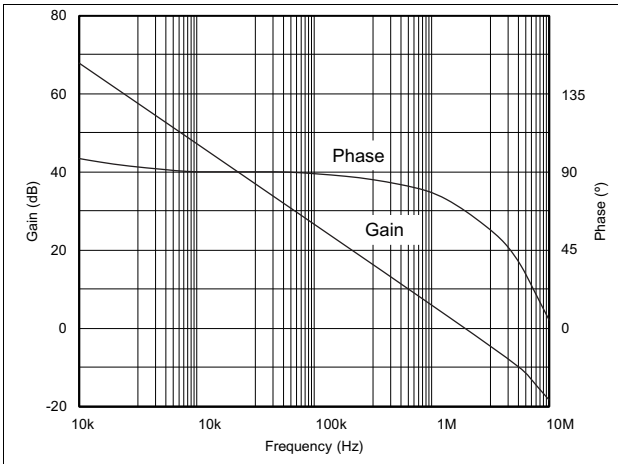


Figure 1. Error Amplifier Gain and Phase Response

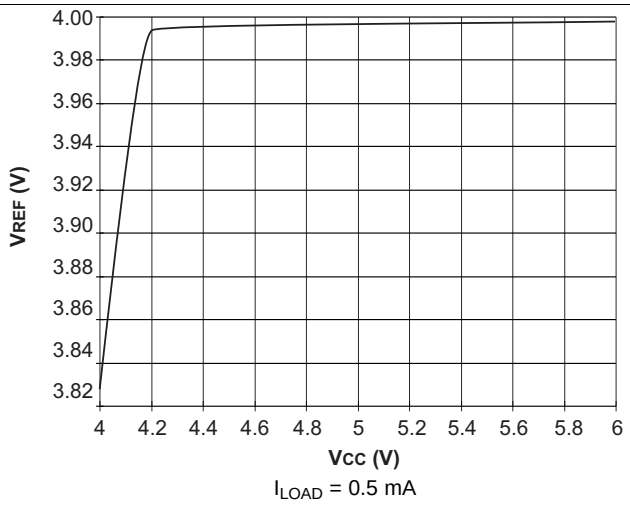


Figure 2. UCC2813-[3,5]-Q1: V_{REF} vs VCC

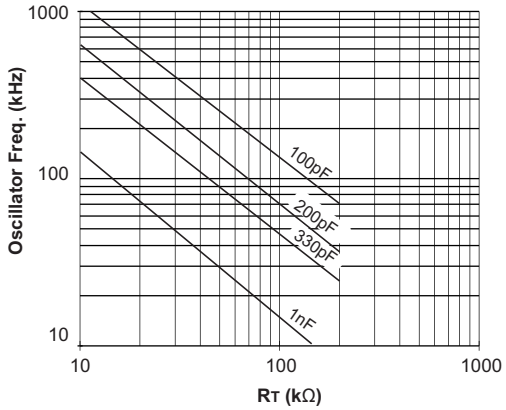


Figure 3. UCC2813-[0,1,2,4]-Q1: Oscillator Frequency vs R_T and C_T

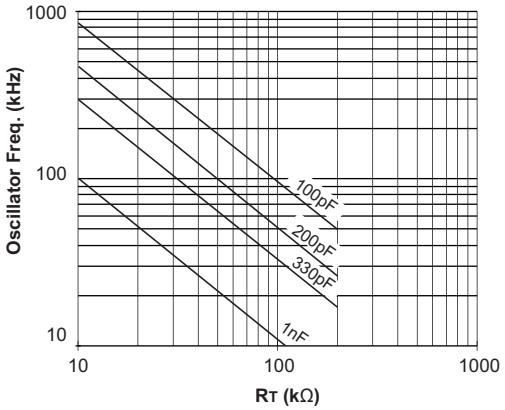


Figure 4. UCC2813-[3,5]-Q1: Oscillator Frequency vs R_T and C_T

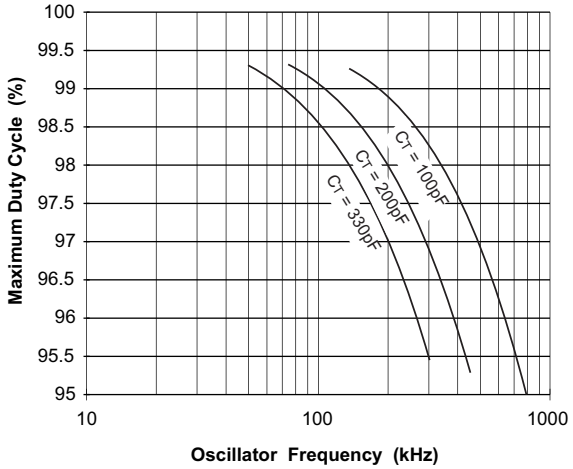


Figure 5. UCC2813-[0,2,3]-Q1: Maximum Duty Cycle vs Oscillator Frequency

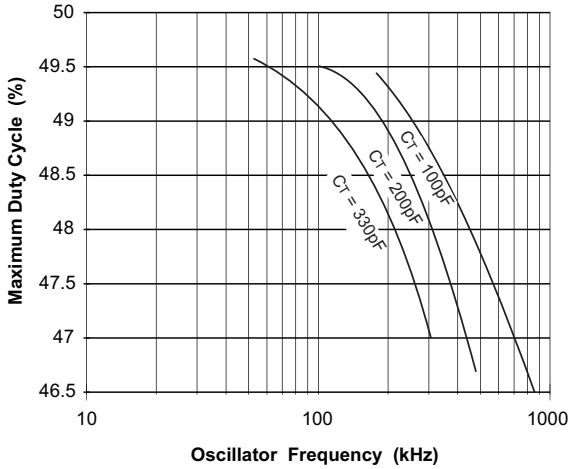


Figure 6. UCC2813-[1,4,5]-Q1: Maximum Duty Cycle vs Oscillator Frequency

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Typical Characteristics (continued)

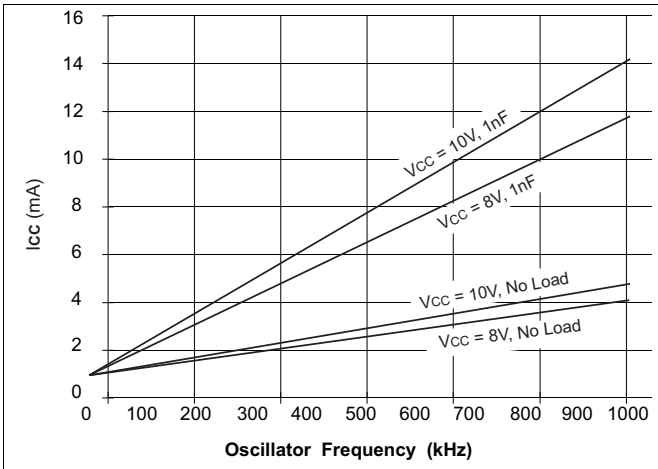


Figure 7. UCC2813-0-Q1: I_{CC} vs Oscillator Frequency

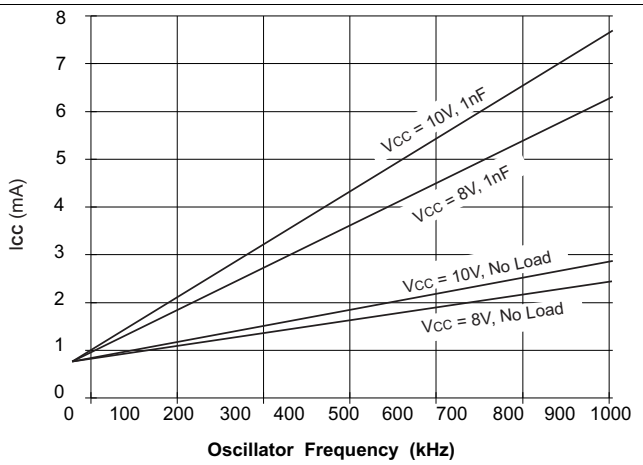


Figure 8. UCC2813-5-Q1: I_{CC} vs Oscillator Frequency

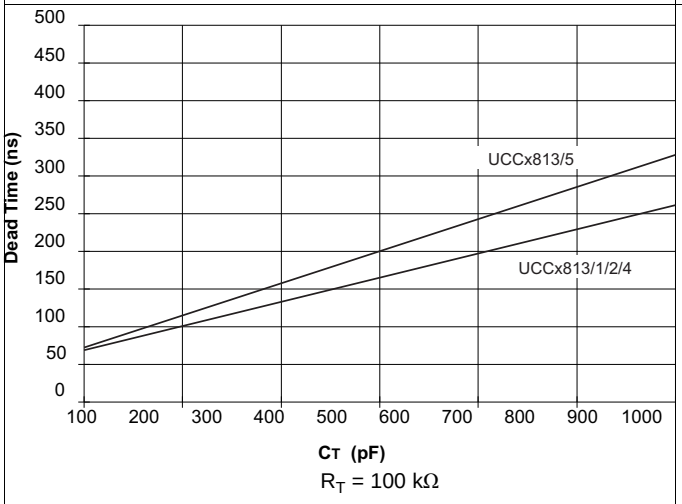


Figure 9. Dead Time vs C_T

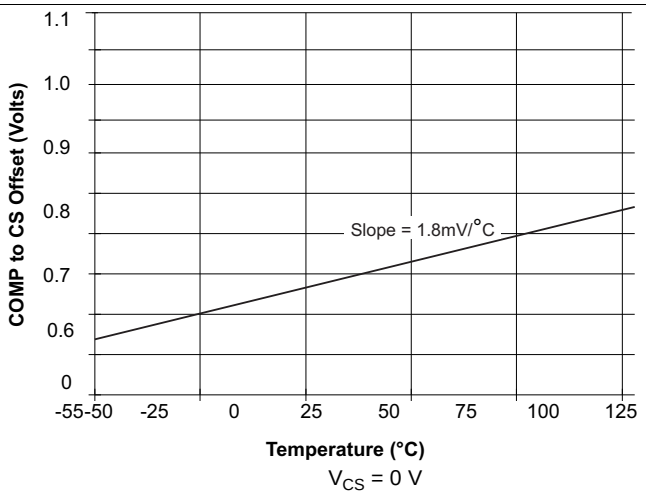


Figure 10. COMP To CS Offset vs Temperature

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8 Detailed Description

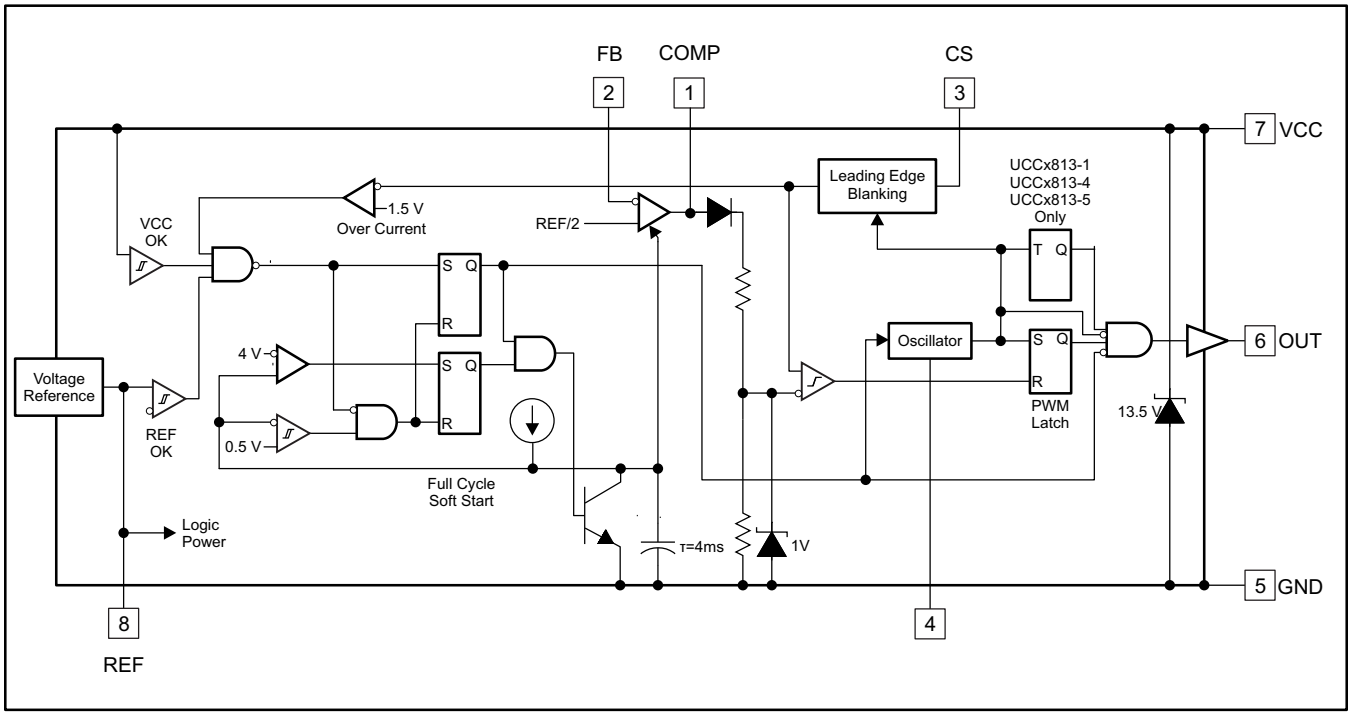
8.1 Overview

The UCC2813-x-Q1 family of high-speed, low-power integrated circuits contain all of the control and drive functions required for off-line and DC-to-DC fixed-frequency current-mode switched-mode power supplies having minimal external parts count. The UCC2813-x-Q1 family is a cost-reduced version of the UCCx80x family, with some relaxation of certain parameter limits. See *Differences Between the UCC3813 and UCC3800 PWM Families* for more information.

These devices have the same pin configuration as the UC284x and UC284xA families, and also offer the added features of internal full-cycle soft start and internal leading-edge blanking of the current-sense input. The UCC2813-x-Q1 devices are pin-out compatible with the UC284x and UC284xA families, however they are not plug-in compatible. In general, the UCC2813-x-Q1 requires fewer external components and consumes less operating current.

The UCC2813-x-Q1 series is specified for the automotive temperature range of −40°C to 125°C.

8.2 Functional Block Diagram



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8.3 Feature Description

The UCC2813-x-Q1 family offers numerous advantages that allow the power supply design engineer to meet their challenging requirements.

Features include:

- Bi-CMOS process
- Low starting supply current: typically 100 µA
- Low operating supply current: typically 500 µA
- Pinout compatible with UC2842 and UC2842A families
- 5-V operation (UCC2813-[3,5]-Q1)
- Leading-edge blanking of current-sense signal
- On-chip soft start for start-up and fault recovery

Feature Description (continued)

- Internal full cycle restart delay
- 1.5% voltage reference
- Up to 1-MHz oscillator
- Low self-biasing output during UVLO
- 70-ns response from current sense to output
- Very few external components required
- Available in surface-mount and PDIP packages

8.3.1 Detailed Pin Descriptions

8.3.1.1 COMP

COMP is the output of the error amplifier and the input of the PWM comparator. Unlike earlier-generation devices, the error amplifier in the UCC2813-x-Q1 device family is a true low-output-impedance 2-MHz operational amplifier. As such, the COMP terminal both sources and sinks current. However, the error amplifier is internally current limited, so zero duty cycle may be commanded by externally forcing COMP to GND.

The UCC2813-x-Q1 device family features built-in full cycle soft start at power up and after fault recovery, and no external components are necessary. Soft start is implemented as a rising clamp on the COMP voltage, increasing from 0 V to 5 V in 4 ms.

8.3.1.2 CS

CS is the input to the current-sense comparators. The UCC2813-x-Q1 current sense is significantly different from its predecessor. The UCC2813-x-Q1 device family has two different current-sense comparators: the PWM comparator and an overcurrent comparator. The overcurrent comparator is intended only for fault sensing, and exceeding the overcurrent threshold causes a soft-start cycle. The earlier UC3842 family current-sense input connects to only the PWM comparator.

The UCC2813-x-Q1 device family contains digital current-sense filtering, which disconnects the CS terminal from the current sense comparator during the 100-ns interval immediately following the rising edge of the OUT pin. This digital filtering, also called leading-edge blanking, prevents false triggering due to leading edge noises which means that in most applications, no analog filtering (external R-C filter) is required on CS. Compared to an external RC filter technique, the leading-edge blanking provides a smaller effective CS-to-OUT delay. However, the minimum non-zero on-time of the OUT signal is determined by the leading-edge-blanking time and the CS-to-OUT propagation delay. The gain of the current sense amplifier is typically 1.65 V/V in the UCC2813-x-Q1 family versus typically 3 V/V in the UC3842 family. Connect CS directly to MOSFET source current sense resistor.

8.3.1.3 FB

FB is the inverting input of the error amplifier. For best stability, keep the FB lead length as short as possible and FB stray capacitance as small as possible. At 2 MHz, the gain-bandwidth of the error amplifier is twice that of earlier UC3842 family devices, and feedback design techniques are identical.

8.3.1.4 GND

GND is the signal reference ground and power ground for all functions on this part. TI recommends separating the signal return paths and the high current gate driver path so that signals are not affected by the switching current.

8.3.1.5 OUT

OUT is the output of a high-current power driver capable of driving the gate of a power MOSFET with peak currents exceeding ±750 mA (up to ±1 A). OUT is actively held low when VCC is below the UVLO threshold. This feature eliminates the need for a gate-to-source *bleeder* resistor associated with the MOSFET gate drive.

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Feature Description (continued)

The high-current power driver consists of CMOS FET output devices, which can switch all of the way to GND and all of the way to VCC. The output provides very smooth rising and falling waveforms, providing very low impedances to overshoot and undershoot which means that in many cases, external Schottky clamp diodes may not be necessary on the output. Finally, no external gate voltage clamp is necessary with the UCC2813-x-Q1 as the on-chip Zener diode automatically clamps the output to VCC.

8.3.1.6 RC

RC is the oscillator timing pin. For fixed frequency operation, set the timing-capacitor charging current by connecting a resistor from REF to RC. Set frequency by connecting a timing capacitor from RC to GND. For best performance, keep the timing capacitor lead to GND as short and direct as possible. If possible, use separate ground traces for the timing capacitor and all other functions.

The UCC2813-x-Q1's oscillator allows for operation to 1 MHz versus 500 kHz with the UC3842 family. Both devices make use of an external resistor to set the charging current for the capacitor, which determines the oscillator frequency. For the UCC2813-[0,1,2,4]-Q1, use Equation 1.

$$f = \frac{1.5}{R \times C} \quad (1)$$

where

- f is the oscillator frequency in hertz (Hz)
- R is the timining resistance in ohms (Ω)
- C is the timing capacitance in farads (F)

For the UCC2813-[3,5]-Q1, use Equation 2.

$$f = \frac{1.0}{R \times C} \quad (2)$$

The recommended timing resistance is from 10 kΩ to 200 kΩ and timing capacitance is from 100 pF to 1000 pF. Never use a timing resistor less than 10 kΩ.

The two equations are different due to different reference voltages. The peak-to-peak amplitude of the oscillator waveform is 2.45 V versus 1.7 V in UC3842 family. For best performance, keep the timing capacitor lead to GND as short as possible. TI recommends separate ground traces for the timing capacitor and all other pins. The maximum duty cycle for the UCC2813-[0,2,3]-Q1 is approximately 99%; the maximum duty cycle for the UCC2813-[1,4,5]-Q1 is approximately 49%. The duty cycle cannot be easily modified by adjusting R_T and C_T, unlike the UC3842A family. The maximum duty cycle limit is set by the ratio of the external oscillator charging resistor R_T and the internal oscillator discharge transistor on-resistance, like the UC3842. However, maximum duty cycle limits less than 90% (for the UCC2813-[0,2,3]-Q1) and less than 45% (for the UCC2813-[1,4,5]-Q1) can not reliably be set in this manner. For better control of maximum duty cycle, consider using the UCCx807.

8.3.1.7 REF

REF is the voltage reference for the error amplifier and also for many other functions on the IC. REF is also used as the logic power supply for high speed switching logic on the IC. The UCC2813-[0,1,2,4]-Q1 have a 5-V reference and the UCC2813-[3,5]-Q1 have a 4-V reference. Both have ±1.5% accuracy at 25°C versus ±2% in the UC3842 family. The REF output short-circuit current is lower at 5 mA, compared to 30 mA in the UC3842 family.

For reference stability and to prevent noise problems with high speed switching transients, it is important to bypass REF to GND with a ceramic capacitor as close to the pins as possible. A minimum of 0.1-µF ceramic is required. Additional REF bypassing is required for external loads greater than 2.5 mA on the reference. An electrolytic capacitor can also be used in addition to the ceramic capacitor.

When VCC is greater than 1 V and less than the UVLO on-threshold, REF is internally pulled to ground through a 5-kΩ resistor which means that REF can be used as a logic output indicating power-system status.

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Feature Description (continued)

8.3.1.8 VCC

VCC is the power input connection for this device. In normal operation, VCC is powered through a current limiting resistor to a low-impedance source. To prevent noise problems, bypass VCC to GND with a 0.1-µF ceramic capacitor in parallel as close to the VCC pin as possible. An electrolytic capacitor can also be used in addition to the ceramic capacitor.

Although quiescent VCC current is very low, total supply current is higher, depending on the OUT current. Total VCC current is the sum of quiescent VCC current and the average OUT current. Knowing the switching frequency f and the MOSFET gate charge (Qg), average OUT current can be calculated from Equation 3.

$$I_{OUT} = Q_g \times f \tag{3}$$

The UCC2813-x-Q1 has a lower VCC (supply voltage) clamp of 13.5 V typical versus 30 V on the UC3842. For applications that require a higher VCC voltage, a resistor must be placed in series with VCC to increase the source impedance. The maximum value of this resistor is calculated with Equation 4.

$$R_{max} = \frac{V_{IN(min)} - V_{VCC(max)}}{I_{VCC} + Q_g \times f} \tag{4}$$

where

- $V_{IN(min)}$ is the minimum voltage that is used to supply VCC
- $V_{VCC(max)}$ is the maximum VCC clamp voltage of the controller
- I_{VCC} is the device supply current without considering the gate driver current
- Q_g is the external power MOSFET gate charge, and f is the switching frequency

Additionally, the UCC2813-x-Q1 has an on-chip Zener diode to limit VCC to 13.5 V, which also limits the maximum OUT voltage. If the bias-supply source is always lower than 12 V, it may be connected directly to VCC. With UVLO thresholds at 4.1 V and 3.6 V for the UCC2813-3-Q1 and UCC2813-5-Q1, respectively, 5-V PWM operation is now possible.

8.3.2 Undervoltage Lockout (UVLO)

The UCC2813-x-Q1 devices feature undervoltage lockout protection circuits for controlled operation during power-up and power-down sequences. Both the supply voltage (V_{VCC}) and the reference voltage (V_{REF}) are monitored by the UVLO circuitry. During UVLO, an active-low, self-biasing totem-pole output structure is also incorporated for enhanced power switch protection.

Undervoltage lockout thresholds for the UCC2813-[2,3,4,5]-Q1 devices are different from the previous generation of UCx84[2,3,4,5]-Q1 PWM controllers. The thresholds are optimized for two groups of applications: off-line power supplies and DC-DC converters. See Table 1 for the specific thresholds for each device.

Table 1. UVLO Level Comparison Table

DEVICE	V_{ON} (V)	V_{OFF} (V)
UCC2813-0-Q1	7.2	6.9
UCC2813-1-Q1	9.4	7.4
UCC2813-[2,4]-Q1	12.5	8.3
UCC2813-[3,5]-Q1	4.1	3.6

The UCC2813-[2,4]-Q1 feature typical UVLO thresholds of 12.5 V for turnon and 8.3 V for turnoff, providing 4.3 V of hysteresis.

For low voltage inputs, which include battery and 5-V applications, the UCC2813-[3,5]-Q1 turn on at 4.1 V and turn off at 3.6 V with 0.5 V of hysteresis.

The UCC2813-[0,1]-Q1 have UVLO thresholds optimized for automotive and battery applications.

During UVLO, the device draws approximately 100 µA of supply current. Once VCC crosses the turnon threshold, the device supply current increases typically to about 500 µA, over an order of magnitude lower than bipolar counterparts. Figure 11 indicates the supply current behavior at the relative UVLO turnon and turnoff thresholds, not including average OUT current.

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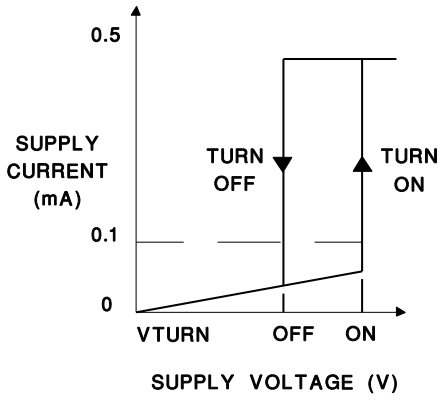


Figure 11. Device Supply Current at UVLO

8.3.3 Self-Biasing, Active Low Output

The self-biasing, active-low clamp circuit shown in Figure 12 eliminates the potential for problematic MOSFET turnon. As the PWM output voltage rises while in UVLO, the P-channel device drives the larger N-channel switch ON, which clamps the output voltage low. Power to this circuit is supplied by the externally rising gate voltage, so full protection is available regardless of the device's supply voltage during undervoltage lockout.

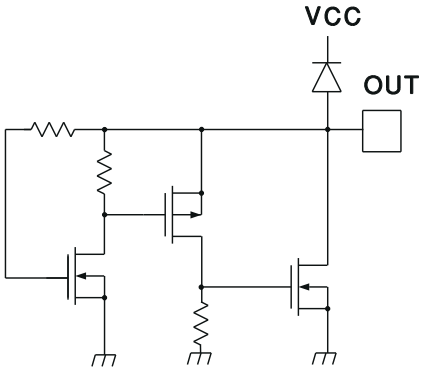


Figure 12. Internal Circuit Holding OUT Low During UVLO

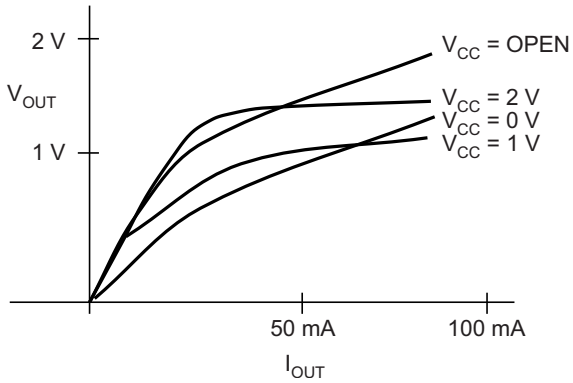


Figure 13. OUT Voltage vs OUT Current During UVLO

8.3.4 Reference Voltage

The traditional 5-V band-gap-derived reference voltage of the UC3842 family can be also found on the UCC2813-[0,1,2,4]-Q1 devices. However, the reference voltage of the UCC2813-[3,5]-Q1 devices is 4 V. This change was necessary to facilitate operation with input supply voltages below 5 V. Many of the reference voltage specifications are similar to the UC3842 devices although the test conditions have been changed, indicative of lower-current PWM applications. Similar to their bipolar counterparts, the BiCMOS devices internally pull the reference voltage low during UVLO, which can be used as a logic status indication.

The 4-V reference voltage on the UCC2813-[3,5]-Q1 is derived from the supply voltage (V_{VCC}) and requires about 0.5 V of headroom to maintain regulation. Whenever V_{VCC} is below approximately 4.5 V, the reference voltage also drops outside of its specified range for normal operation. The relationship between V_{VCC} and V_{REF} during this excursion is shown in Figure 14.

The noninverting input to the error amplifier is tied to one-half of the controller's reference voltage (V_{REF}). This input is 2 V on the UCC2813-[3,5]-Q1 and 2.5 V on the higher reference voltage parts: the UCC2813-[0,1,2,4]-Q1.

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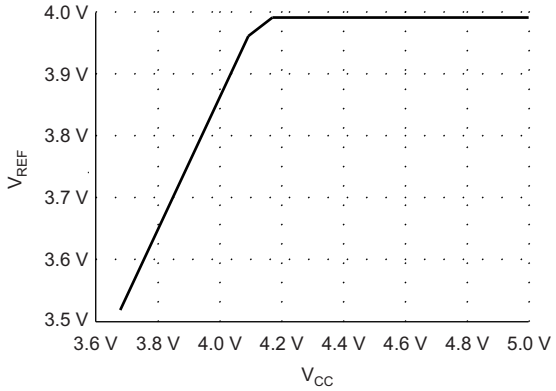


Figure 14. UCC2813-3-Q1 REF Output vs V_{VCC}

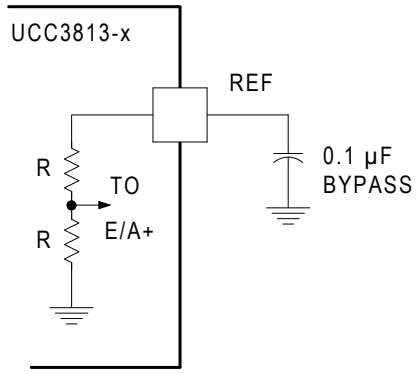


Figure 15. Required Reference Bypass Minimum Capacitance

8.3.5 Oscillator

The UCC2813-x-Q1 oscillator generates a sawtooth waveform on RC. The rise time is set by the time constant of R_T and C_T. The fall time is set by C_T and an internal transistor on-resistance of approximately 130 Ω. During the fall time, the output is OFF and the maximum duty cycle is reduced below 50% or 100%, depending on the part number. Larger values for the timing capacitor increase the discharge time and reduce the maximum duty cycle and frequency slightly, as seen in Figure 5 and Figure 6 .

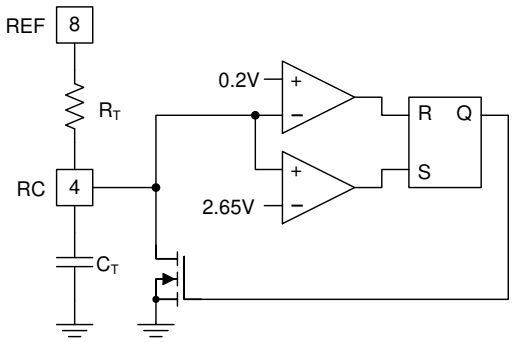


Figure 16. Oscillator Equivalent Circuit

The oscillator section of the UCC2813-x-Q1 BiCMOS family has few similarities to the UC3842 type — other than single-pin programming. It does still use a resistor to the reference voltage and capacitor to ground to program the oscillator frequency up to 1 MHz. Timing component values must be changed because a much lower charging current is desirable for low-power operation. Several characteristics of the oscillator have been optimized for high-speed, noise-immune operation. The oscillator peak-to-peak amplitude has been increased to 2.45 V typical versus 1.7 V on the UC3842 family. The lower oscillator threshold has been dropped to approximately 0.2 V while the upper threshold remains fairly close to the original 2.8 V at approximately 2.65 V.

Discharge current of the timing capacitor has been increased to nearly 20-mA peak as opposed to roughly 8 mA. This can be represented by approximately 130 Ω in series with the discharge switch to ground. The higher current is necessary to achieve brief dead times and high duty cycles with high-frequency operation. Practical applications can use these devices to a 1-MHz switching frequency.

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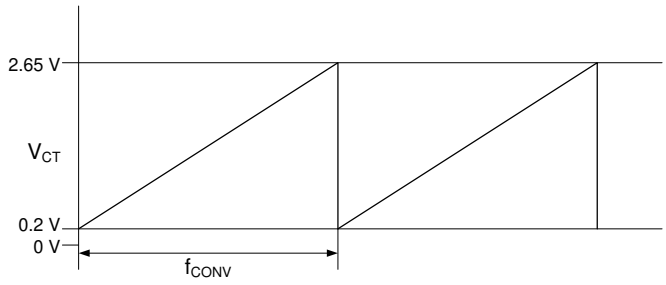


Figure 17. Oscillator Waveform at RC

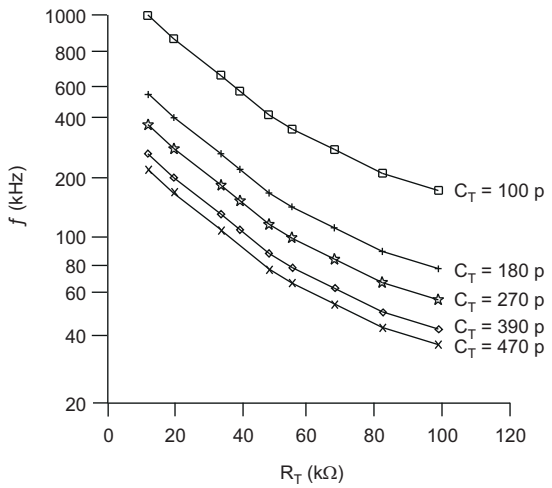


Figure 18. Oscillator Frequency vs R_T For Several C_T

8.3.6 Synchronization

Synchronization of these PWM controllers is best obtained by the universal technique shown in Figure 19. The device oscillator is programmed to free-run at a frequency about 20% lower than that of the synchronizing frequency. A brief positive pulse is applied across the 50-Ω resistor to force synchronization. Typically, a 1-V amplitude pulse of 100-ns width is sufficient for most applications.

The controller can also be synchronized to a pulse-train applied directly to the oscillator RC pin. The device internally pulls low at this node once the upper oscillator threshold is crossed. This 130-Ω impedance to ground remains active until the voltage on RC is lowered below 0.2 V. External synchronization circuits must accommodate these conditions.

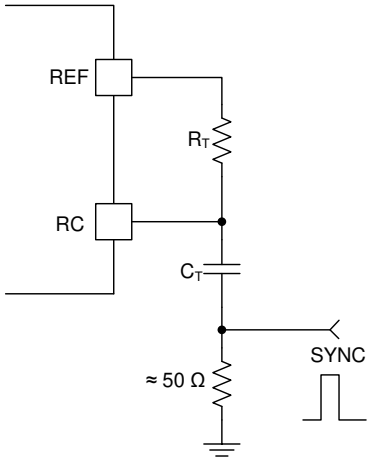


Figure 19. Synchronizing the Oscillator

8.3.7 PWM Generator

Maximum duty cycle is higher for these devices than for their UC384x predecessors. This is primarily due to the higher ratio of timing capacitor discharge-to-charge current, which can exceed one hundred-to-one in a typical BiCMOS application. Attempts to program the oscillator maximum duty cycle much below the specified range, by adjusting the timing component values of R_T and C_T, must be avoided. There are two reasons to refrain from this design practice. First, the device's high discharge current would necessitate higher charging current than necessary for programming, defeating the purpose of low power operation. Second, a low-value timing resistor may prevent the capacitor from discharging to the lower threshold and initiating the next switching cycle.

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8.3.8 Minimum Off-Time Adjustment (Dead-Time Control)

Dead time is the term used to describe the ensured OFF time of the PWM output during each oscillator cycle. It is used to ensure that even at maximum duty cycle, there is enough time to reset the magnetic circuit elements, and prevent saturation. The dead time of the UCC2813-x-Q1 PWM family is determined by the internal 130-Ω discharge impedance and the timing capacitor value. Larger capacitance values extend the dead time whereas smaller values results in higher maximum duty cycles for the same operating frequency. A curve for dead time versus timing capacitor values is provided in Figure 20. Further increasing the dead time is possible by adding a low-value resistor between the RC pin and the timing components, as shown in Figure 21. The dead time increases with increasing discharge resistor value to about 470 Ω as indicated from the curve in Figure 22. Higher resistances must be avoided as they can decrease the dead time and reduce the oscillator peak-to-peak amplitude. Sinking too much current (1 mA) by reducing R_T will *freeze* the oscillator OFF by preventing discharge to the lower comparator threshold voltage of 0.2 V. Adding this discharge control resistor has several impacts on the oscillator programming. First, it introduces a DC offset to the capacitor during the discharge interval – but not the charging interval of the timing cycle, thus lowering the usable peak-to-peak timing capacitor amplitude. Because of the reduced peak-to-peak amplitude, the exact value of C_T may require adjustment to obtain the correct oscillator frequency. One alternative is keep the same value timing capacitor and adjust both the timing and discharge resistor values because these are readily available in finer numerical increments.

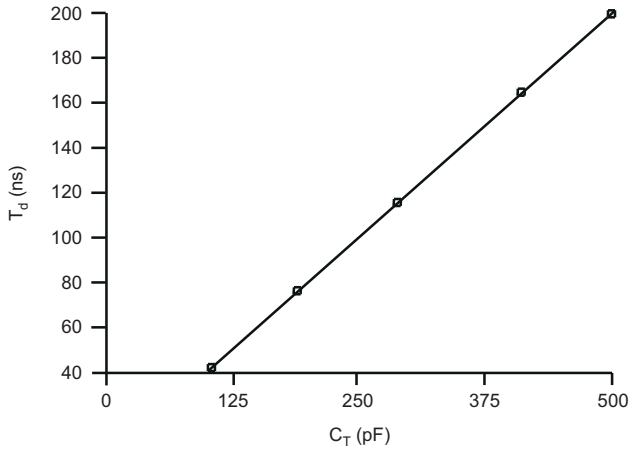
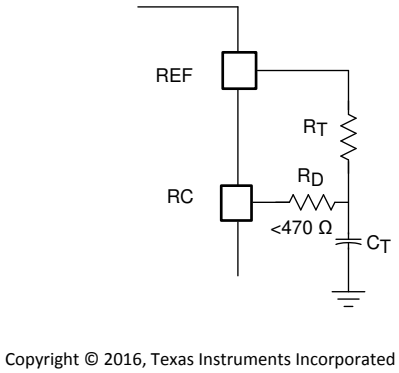
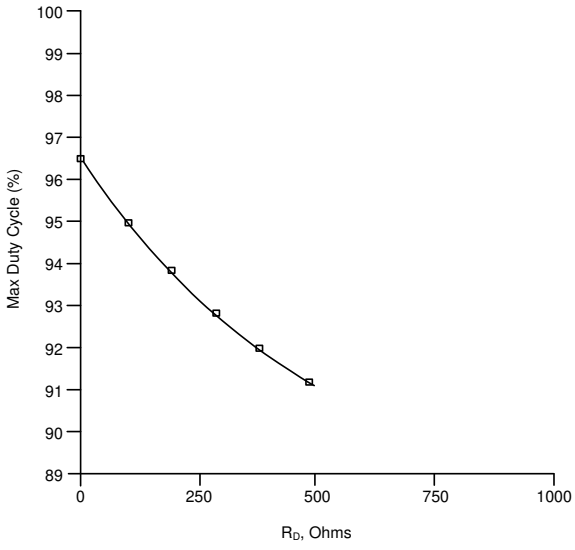


Figure 20. Minimum Dead Time vs C_T



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Figure 21. Circuit to Produce Controlled Maximum Duty Cycle



R_T = 20 kΩ

Figure 22. Maximum Duty Cycle vs R_D

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8.3.9 Leading Edge Blanking

A 100-ns leading-edge-blanking interval is applied to the current-sense input circuitry of the UCC2813-x-Q1 devices. This internal feature eliminates the requirement for an external resistor-capacitor filter network to suppress the switching spike associated with turnon of the power MOSFET. This 100-ns period should be adequate for most switch-mode designs but can be lengthened by adding an external R/C filter. The 100-ns leading edge blanking is also applied to the overcurrent fault comparator in addition to the cycle-by-cycle current-limiting PWM function.

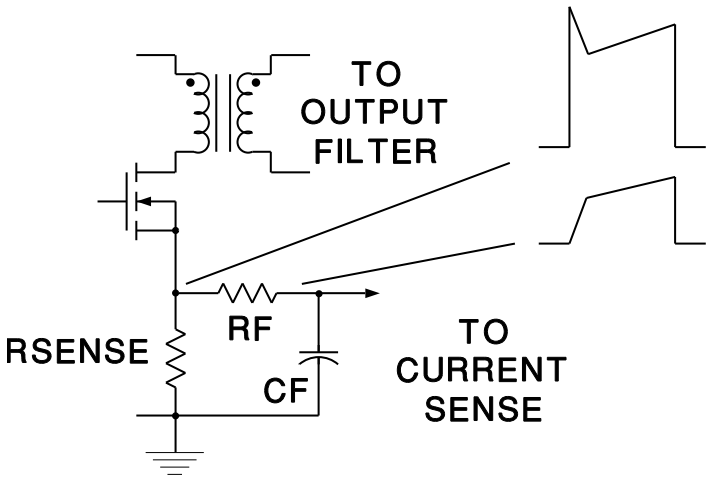


Figure 23. Current-Sense Filter Required With Older PWM Devices

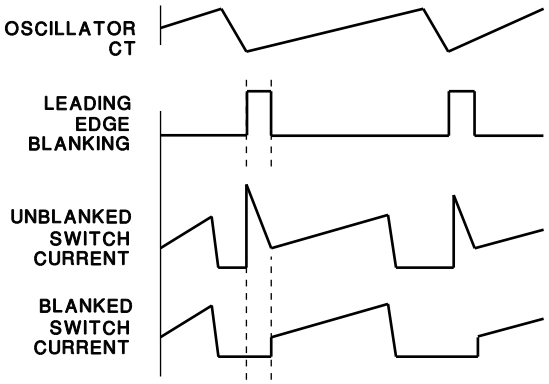


Figure 24. UCC2813-x-Q1 Current-Sense Waveforms With Leading Edge Blanking

8.3.10 Minimum Pulse Width

The PWM comparator has two inputs; one is from the current sense input, the other input is the attenuated error-amplifier output (COMP) that has a diode and two resistors in series to ground. The diode in this network is used to ensure that zero duty-cycle can be reached. Whenever the E/A output falls below a diode forward voltage drop, no current flows in the resistor divider and the PWM input goes to zero, resulting in zero pulse width.

Under certain conditions, the leading-edge-blanking circuitry can lead to an output pulse of minimum width equal to the blanking interval. This occurs when the COMP is slightly higher than a diode forward voltage drop of about 0.5 V, such that the attenuated COMP input to the PWM comparator allows an output pulse to start. If the attenuated COMP level commands a peak current whose pulse width would fall within the leading-edge-blanking interval, the output will remain ON until the blanking interval is finished and the peak current will be higher than desired by the COMP level. The usual result is that the converter output voltage rises, increasing the error, and COMP is driven lower than the diode drop which then produces zero pulse width. Cycle-skipping may result as the output voltage rises and falls around this minimum pulse-width condition.

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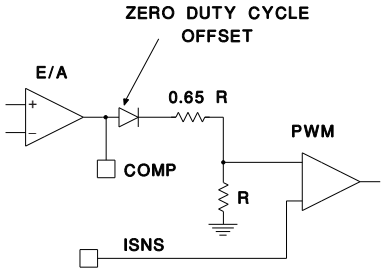
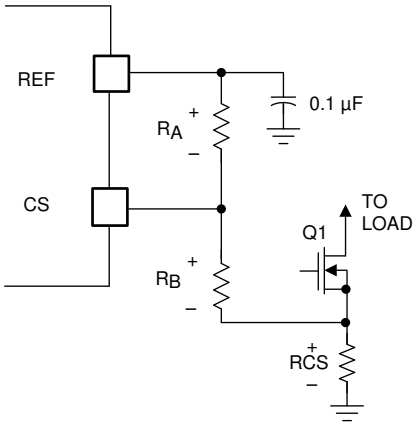


Figure 25. Zero Duty-Cycle Offset

8.3.11 Current Limiting

A 1-V (typical) cycle-by-cycle current limit threshold is incorporated into the UCC2813-x-Q1 family. The 100-ns leading-edge-blanking interval is applied to this current-limiting circuitry. The blanking overrides the current-limit comparator output to prevent the leading-edge switch noise from triggering a current-limit function. Propagation delay from the current-limit comparator to the output is typically 70 ns. This high-speed path minimizes power semiconductor dissipation during an overload by abbreviating the ON time.

For increased efficiency in the current-sense circuitry, the circuit shown in Figure 26 can be used. Resistors R_A and R_B bias the actual current-sense resistor voltage up, allowing a smaller current sense amplitude to be used. This circuitry provides current-limiting protection with lower power-loss current sensing.



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Figure 26. Biasing CS For Lower Current-Sense Voltage

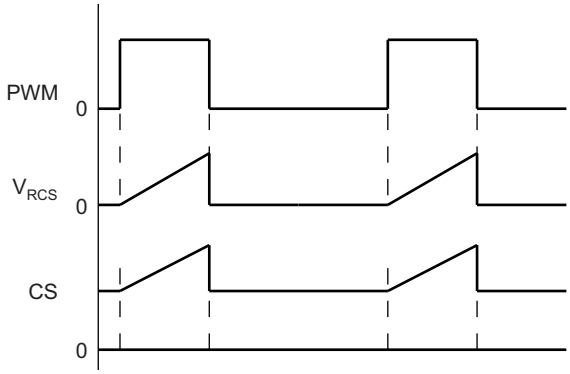


Figure 27. CS Pin Voltage with Biasing

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The example shown uses a 200-mV full-scale signal at the current sense resistor. Resistor R_B biases this up by approximately 700 mV to match the 0.9-V minimum specification of the current-limit comparator of the IC. The value of resistor R_A changes with the specific device used, due to the different reference voltages. The resistor values should be selected for minimal power loss. For example, a 50-µA bias current sets R_B = 13 kΩ, and R_A = 75 kΩ for UCC2813-[0,1,2,4]-Q1 or R_A = 56 kΩ for UCC2813-[3,5]-Q1 devices.

8.3.12 Overcurrent Protection and Full-Cycle Restart

A separate overcurrent comparator within the UCC2813-x-Q1 devices handles operation into a short-circuited or severely overloaded power supply output. This overcurrent comparator has a 1.5-V threshold and is also gated by the leading edge blanking signal to prevent false triggering. Once triggered, the overcurrent comparator uses the internal soft-start capacitor to generate a delay before retry is attempted. Often referred to as *hiccup*, this delay time is used to significantly reduce the input and dissipated power of the main converter and switching components. Full-cycle soft start ensures that there is a predictable delay of greater than 3 ms between successive attempts to operate during fault conditions. The circuit shown in Figure 28 and the timing diagram in Figure 29 show how the device responds to a severe fault, such as a saturated inductor. When the peak current fault is first detected, the internal soft-start capacitor instantly discharges and stays discharged until the fault clears. At the same time, the PWM output is turned off and held off. When the fault clears, the capacitor slowly charges and allows the error amp output (COMP) to rise. When COMP gets high enough to enable the output, another fault occurs, latching off the PWM output, but the soft-start capacitor still continues to rise to 4 V before being discharged and permitting start of a new cycle. This means that for a severe fault, successive retries is spaced by the time required to fully charge the soft-start capacitor. TI recommends low leakage transformer designs in high-frequency applications to activate the overcurrent protection feature. Otherwise, the switch current may not ramp up sufficiently to trigger the overcurrent comparator within the leading edge blanking duration. This condition would cause continual cyclical triggering of the cycle-by-cycle current limit comparator but not the overcurrent comparator. This would result in brief high power dissipation durations in the main converter at the switching frequency. The intent of the overcurrent comparator is to reduce the effective retry rate under these conditions to a few milliseconds, thus significantly lowering the short-circuit power dissipation of the converter.

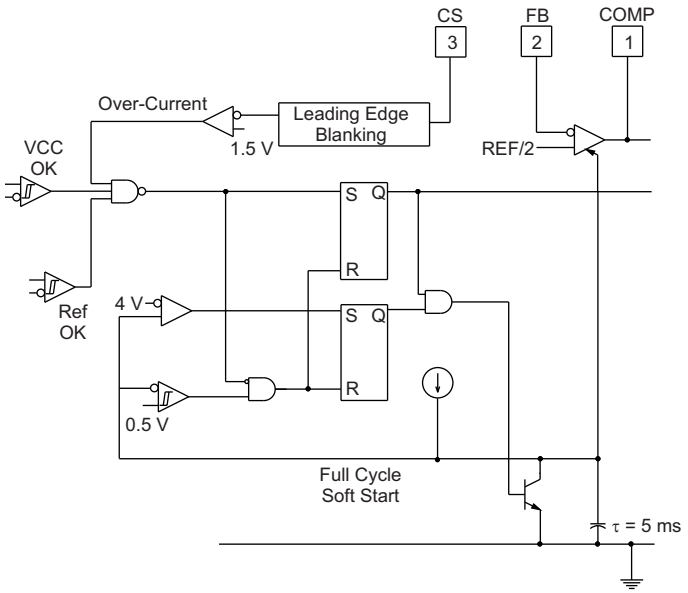


Figure 28. Detailed Block Diagram for Overcurrent Protection

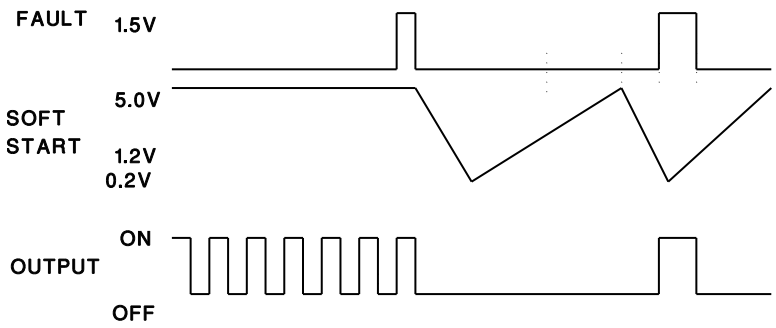


Figure 29. Device Behavior with Repetitive Fault at CS

8.3.13 Soft Start

Internal soft starting of the PWM output is accomplished by gradually increasing the error amplifier (E/A) output voltage at COMP. When used in current-mode control, this implementation slowly raises the peak switch current each PWM cycle in succession, forcing a controlled start-up. In voltage-mode (duty-cycle) control, this feature continually widens the pulse width.

Soft-start is performed within the UCC2813-x-Q1 devices by clamping the E/A amplifier output (COMP) to the voltage on an internal soft-start capacitor (C_{SS}), which is charged by a current source. C_{SS} is discharged following an undervoltage lockout transition or if the reference voltage is below a minimum value for normal operation. Additionally, discharge of C_{SS} occurs whenever the overcurrent protection comparator is triggered by a fault. The soft-start clamp circuitry is overridden once C_{SS} charges above the voltage commanded by the error amplifier for normal PWM operation.

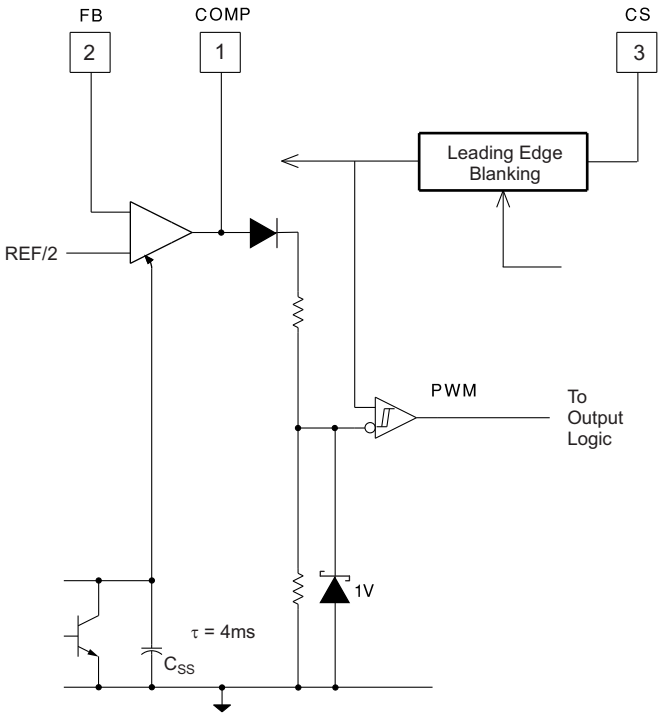


Figure 30. Detailed Block Diagram for Soft-Start

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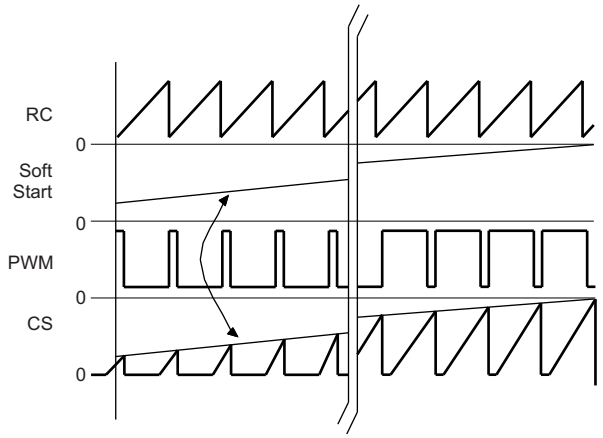


Figure 31. Device Soft-Start Behavior

8.3.14 Slope Compensation

Slope compensation can be added in all current-mode control applications to cancel the peak-to-average current error. Slope compensation is necessary in applications with duty-cycles exceeding 50%, but also improves performance in those below 50%. Primary current is sensed using resistor R_{CS} in series with the converter switch. The timing resistor can be broken up into two series resistors to bias up an NPN voltage-follower, as shown in Figure 32. This is required to provide ample compliance for slope compensation at the beginning of a switching cycle, especially with continuous-current converters. The voltage follower drives the slope compensating programming resistor (R_{SC}) to provide a slope-compensating current into C_F.

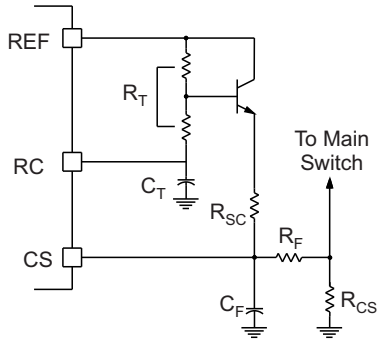


Figure 32. Adding Slope Compensation

8.4 Device Functional Modes

The UCC2813-x-Q1 family of high-speed, low-power current-mode PWM controllers has the following functional modes.

8.4.1 Normal Operation

During this operation mode, the device controls the power converter into the voltage-mode or current-mode control, regulates the output voltage or current through the converter duty cycle. The regulation can be achieve through the integrated error amplifier or external feedback circuitry.

8.4.2 UVLO Mode

During the system start-up, V_{VCC} voltage starts to rise from 0 V. Before the VCC voltage reaches its corresponding turn-on threshold, the device operates in UVLO mode. In this mode, REF pin voltage is not generated. When V_{VCC} is above 1 V and below the turnon threshold, the REF pin is actively pulled low through a 5-kΩ resistor. This way, V_{REF} can be used as a logic signal to indicate UVLO mode.

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Device Functional Modes (continued)

8.4.3 Soft-Start Mode

Once VCC voltage rises above the UVLO level, or the device comes out of a fault mode, it enters the soft-start mode. During soft-start, the internal soft-start capacitor C_{SS} clamps the error amplifier output voltage, forcing it to rise slowly. This in turn controls the power converter peak current to rise slowly, reducing the voltage and current stress to the system. The UCC2813-x-Q1 family has a fixed built-in soft-start time at 4 ms.

8.4.4 Fault Mode

A separate overcurrent comparator within the UCC2813-x-Q1 devices handles operation into a short-circuited or severely overloaded power supply output. This overcurrent comparator has a 1.5-V threshold and is also gated by the leading-edge-blanking signal to prevent false triggering. When the fault is first detected, the internal soft-start capacitor instantly discharges and stays discharged until the fault clears. At the same time, the PWM output is turned off and held off. This is often referred to as *hiccup*. This delay time is used to significantly reduce the input and dissipated power of the main converter and switching components. Full-cycle soft-start insures that there is a predictable delay of greater than 3 milliseconds between successive attempts to operate during fault. When the fault clears, the capacitor slowly charges and allows the error amp output (COMP) to rise. When COMP gets high enough to enable the output, another fault occurs, latching off the PWM output, but the soft-start capacitor still continues to rise to 4 V before being discharged and permitting start of a new cycle. This means that for a severe fault, successive retries are spaced by the time required to fully charge the soft-start capacitor.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The UCC2813-x-Q1 controllers are peak-current-mode (PCM) pulse-width modulators (PWM). These controllers have an onboard amplifier and can be used in isolated and nonisolated power supply design. There is an onboard totem-pole gate driver capable of delivering up to ±1 A of peak current. These controllers are capable of operating at switching frequencies up to 1 MHz.

9.2 Typical Application

Figure 33 illustrates a typical circuit diagram for an AC-DC converter using the UCC2813-0-Q1 in a peak-current-mode-controlled flyback application.

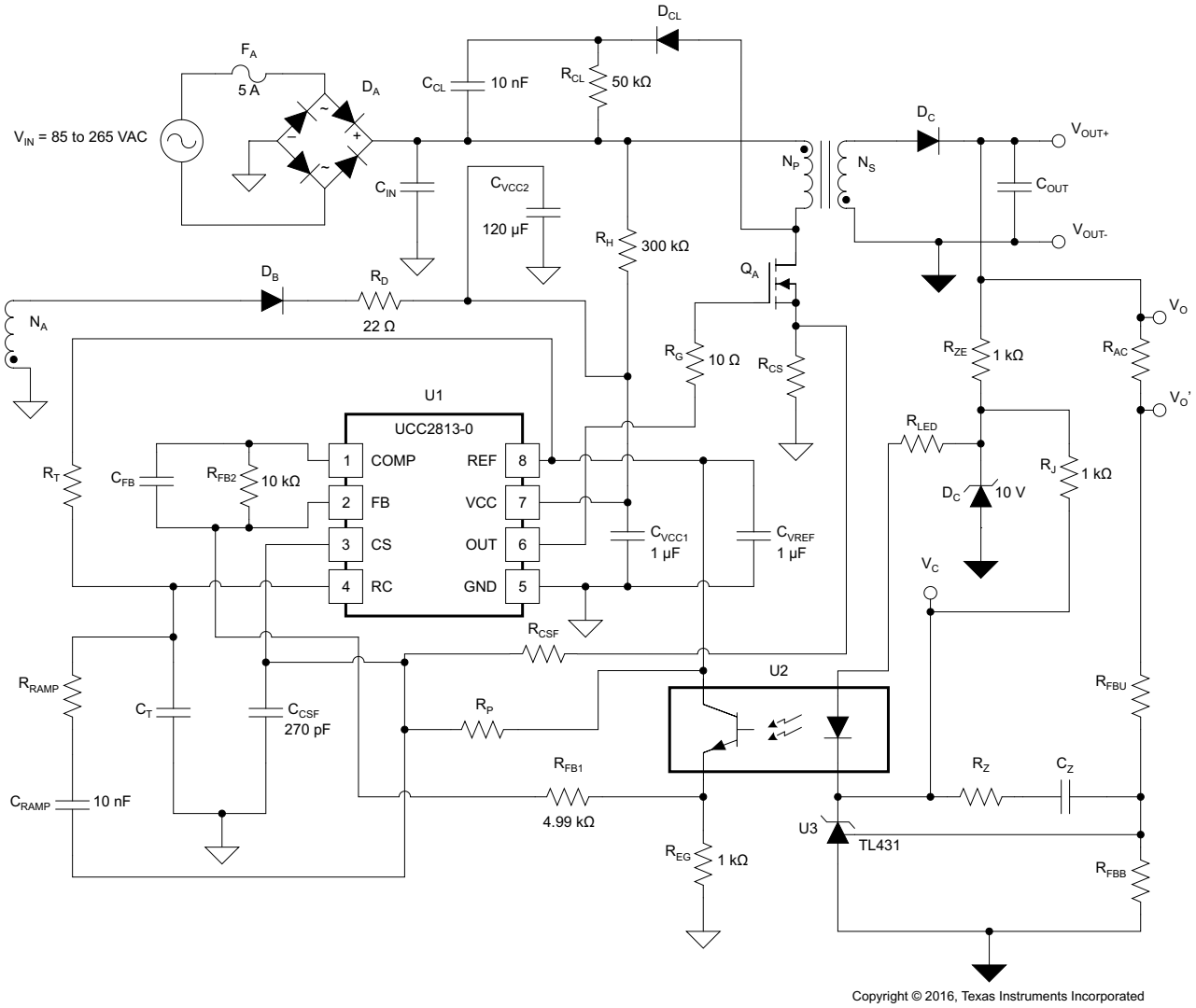


Figure 33. Typical Application Circuit Diagram

Typical Application (continued)

9.2.1 Design Requirements

Use the parameters in Table 2 to review the design of a 12-V, 48-W offline flyback converter using the UCC2813-0-Q1 PWM controller.

Table 2. Design Parameters

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERSTICS						
V_{IN}	Input voltage (RMS)		85		265	V
f_{LINE}	Line frequency		47		63	Hz
OUTPUT CHARACTRSTICS						
V_{OUT}	Output voltage		11.75	12	12.25	V
V_{ripple}	Output ripple voltage				120	mV_{PP}
I_{OUT}	Output current			4	4.33	A
V_{tran}	Output transient	Output voltage measured under 0-A to 4-A load step	11.75		12.25	V
SYSTEM CHARACTRSTICS						
η	Max load efficiency		85%			

9.2.2 Detailed Design Procedure

9.2.2.1 Bulk Capacitor Calculation

The design starts with selecting an appropriate bulk capacitor.

The primary-side bulk capacitor is selected based on the input power level and on the desired minimum bulk voltage level. The bulk capacitor value can be calculated by Equation 5.

$$C_{BULK} = \frac{2P_{IN} \times \left[0.25 + \frac{1}{\pi} \times \arcsin\left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}}\right)\right]}{\left(2V^2_{IN(min)} - V^2_{BULK(min)}\right) \times f_{LINE}}$$

where

- P_{IN} is the maximum output power divided by the target efficiency at maximum load
- $V_{IN(min)}$ is the minimum AC input voltage RMS value
- $V_{BULK(min)}$ is the target minimum bulk voltage
- f_{LINE} is the line frequency (5)

Based on this equation, to achieve 75-V minimum bulk voltage, assuming 85% converter efficiency and 47-Hz minimum line frequency, the bulk capacitor must be larger than 127 µF. 180 µF was chosen in the design, considering the typical tolerance of bulk capacitors.

9.2.2.2 Transformer Design

The transformer design starts with selecting a suitable switching frequency. Generally the switching frequency selection is based on a tradeoff between the converter size and efficiency, based on the simple Flyback topology. Normally, higher switching frequency results in smaller transformer size. However, the switching loss is increased and hurts the efficiency. Sometimes, the switching frequency is selected to avoid certain communication bands to prevent noise interference with the communication. The frequency selection is beyond the scope of this data sheet.

The switching frequency is targeted for 110 kHz, to minimize the transformer size. At the same time, because EMI regulations start to limit conducted noise at 150 kHz, choosing 110-kHz switching frequency can help to reduce the EMI filter size.

The transformer turns ratio can be selected based on the desired MOSFET voltage rating and diode voltage rating. Because maximum input voltage is 265 V AC, the peak bulk voltage can be calculated by Equation 6.

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$$V_{BULK(max)} = \sqrt{2} \times V_{IN(max)} \approx 375\ V \tag{6}$$

To minimize the cost of the system, a popular 650-V MOSFET is selected. Considering the design margin and extra voltage ringing on the MOSFET drain, the reflected output voltage must be less than 120 V. The transformer turns ratio can be selected by Equation 7.

$$n_{ps} = \frac{120V}{12V} = 10 \tag{7}$$

The transformer inductance selection is based on the continuous conduction mode (CCM) condition. Higher inductance would allow the converter to stay in CCM longer. However, it tends to increase the transformer size. Normally, the transformer magnetizing inductance is selected so that the converter enters CCM operation at about 50% load at minimum line voltage. This would be a tradeoff between the transformer size and the efficiency. In this particular design, due to the higher output current, it is desired to keep the converter deeper in CCM and minimize the conduction loss and output ripple. The converter enters CCM operation at about 10% load at minimum bulk voltage.

The inductor can be calculated as Equation 8.

$$L_m = \frac{1}{2} \frac{V^2_{BULK(min)} \times \left(\frac{n_{PS} V_{OUT}}{V_{BULK(min)} + n_{PS} V_{OUT}} \right)^2}{10\ \% \times P_{IN} \times f_{SW}} \tag{8}$$

In this equation, the switching frequency is 110 kHz. Therefore, the transformer inductance must be about 1.7 mH. 1.5 mH is chosen as the magnetizing inductance value.

The auxiliary winding provides the bias power for UCC2813-0-Q1 normal operation. The auxiliary winding voltage is the output voltage reflected to the primary side. It is desired to have higher reflected voltage so that the device can quickly get energy from the transformer and make start-up under heavy load easier. However, higher reflected voltage makes the device consume more power. Therefore, a tradeoff is required.

In this design, the auxiliary winding voltage is selected to be the same as the output voltage so that it is above the UVLO level but keeps the device and driving loss low. Therefore, the auxiliary winding to the output winding turns ratio is selected by Equation 9.

$$n_{as} = \frac{12\ V}{12\ V} = 1 \tag{9}$$

Based on calculated primary inductance value and the switching frequency, the current stress of the MOSFET and diode can be calculated.

9.2.2.3 MOSFET and Output Diode Selection

The peak current of the MOSFET is calculated by Equation 10.

$$I_{PK_{MOS}} = \frac{P_{IN}}{V_{BULK(min)} \times \frac{n_{PS} V_{OUT}}{V_{BULK(min)} + n_{PS} V_{OUT}}} + \frac{1}{2} \frac{V_{BULK(min)}}{L_m} \times \frac{\frac{n_{PS} V_{OUT}}{V_{BULK(min)} + n_{PS} V_{OUT}}}{f_{sw}} \tag{10}$$

The MOSFET peak current is 1.425 A.

The RMS current of the MOSFET can be calculated as Equation 11.

$$I_{RMS_{MOS}} = \sqrt{\frac{1}{3} D^3 \times \left(\frac{V_{BULK(min)}}{L_m \times f_{sw}} \right)^2 - \frac{D^2 I_{PK_{MOS}} V_{BULK(min)}}{L_m \times f_{sw}} + D \times I^2_{PK_{MOS}}} \tag{11}$$

where

- D is the MOSFET duty cycle at minimum bulk voltage and it can be calculated as Equation 12

$$D = \frac{n_{ps} V_{OUT}}{V_{BULK(min)} + n_{ps} V_{OUT}} \tag{12}$$

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The MOSFET RMS current is 0.75 A. With less than 0.9-Ω on-resistance, IRFB9N65A is selected as the primary-side MOSFET.

The diode peak current is the reflected MOSFET peak current on the secondary side.

$$I_{PK_{DIODE}} = n_{ps} \times I_{PK_{MOS}} = 14.25\ A \tag{13}$$

The diode voltage stress is the output voltage plus the reflected input voltage. The voltage stress on the diode can be calculated by Equation 14.

$$V_{DIODE} = \frac{V_{BULK(max)}}{n_{ps}} + V_{OUT} = \frac{375V}{10} + 12V \approx 50V \tag{14}$$

Considering the ringing voltage spikes and voltage derating, the diode voltage rating must be higher than 50 V.

The diode average current is the output current (4 A), so 48CTQ060-1, with 60-V rating and 40-A average current capability, is selected.

9.2.2.4 Output Capacitor Calculation

The output capacitor is selected based on the output voltage ripple requirement. In this design, 0.1% voltage ripple is assumed. Based on the 0.1% ripple requirement, the capacitor value can be selected based on Equation 15.

$$C_{OUT} \geq \frac{I_{OUT} \times \frac{n_{ps} V_{OUT}}{V_{BULK(min)} + n_{ps} V_{OUT}}}{0.1\% \times V_{OUT} \times f_{sw}} = 2105\mu F \tag{15}$$

Considering the tolerance and temperature effect, together the ripple current rating of the capacitors, 3 parallel 680-µF capacitors are selected for the output.

After the basic power stage is designed, the surrounding controller components can be selected.

9.2.2.5 Current Sensing Network

The current sensing network consists of R_{CS}, R_{CSF}, C_{CSF}, and optional R_P. Typically, the direct current sense signal contains a large-amplitude leading-edge spike associated with the turn-on of the main power MOSFET, reverse recovery of the output rectifier, and other factors including charging and discharging of parasitic capacitances. Therefore, C_{CSF} and R_{CSF} form a low-pass filter that provides additional immunity beyond the internal blanking time to suppress the leading edge spike. For this converter, C_{CSF} is chosen to be 270 pF to provide enough filtering.

Without R_P, R_{CS} sets the maximum peak current in the transformer primary based on the maximum amplitude of CS pin, 1 V. To achieve 1.425-A primary side peak current, a 0.75-Ω resistor is chosen for R_{CS}.

The high current-sense threshold helps to provide better noise immunity but the current-sense loss is increased. The current-sense loss can be minimized by injecting an offset voltage into the current-sense signal. R_P and R_{CSF} form a resistor-divider network from the current-sense signal to the device's reference voltage to offset the current-sense voltage. This technique still achieves current-mode control with cycle-by-cycle overcurrent protection. To calculate required offset value (Voffset), use Equation 16.

$$V_{offset} = \frac{R_{CSF}}{R_{CSF} + R_P} V_{REF} \tag{16}$$

9.2.2.6 Gate Drive Resistor

R_G is the gate driver resistor for the power switch, Q_A. The selection of this resistor value must be done in conjunction with EMI compliance testing and efficiency testing. Larger R_G slows down the turn-on and turn-off of the MOSFET. Slower switching speed reduces EMI but also increases the switching loss. A tradeoff between switching loss and EMI performance must be carefully performed. For this design, 10 Ω was chosen as the gate driver resistor.

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9.2.2.7 REF Bypass Capacitor

The precision 5-V reference voltage at REF is designed to perform several important functions. The reference voltage is divided down internally to 2.5 V and connected to the error amplifier's noninverting input for accurate output voltage regulation. Other duties of the reference voltage are to set internal bias currents and thresholds for functions such as the oscillator upper and lower thresholds along with the overcurrent limiting threshold. Therefore, the reference voltage must be bypassed with a ceramic capacitor (C_{VREF}), and 1-µF, 16-V ceramic capacitor was selected for this converter. Placement of this capacitor on the physical printed-circuit board layout must be as close as possible to the respective REF and GND pins.

9.2.2.8 R_T and C_T

The internal oscillator uses a timing capacitor (C_T) and a timing resistor (R_T) to program operating frequency and maximum duty cycle. The operating frequency can be programmed based the curves in Figure 3, where the timing resistor can be found once the timing capacitor is selected. The selection of timing capacitor also affects the maximum duty cycle provided in Figure 5. It is best for the timing capacitor to have a flat temperature coefficient, typical of most COG or NPO type capacitors. For this converter, 1000 pF and 13.6 kΩ were selected for C_T and R_T to operate at 110-kHz switching frequency.

9.2.2.9 Start-Up Circuit

At start-up, the device gets its power directly from the high voltage bulk, through a high-voltage resistor R_H. The selection of start-up resistor is the tradeoff between power loss and start-up time. The current flowing through R_H at minimum input voltage must be higher than the VCC current under UVLO condition (0.2 mA at its maximum value). A 300-kΩ resistor is chosen as the result of the tradeoff.

After VCC is charged up above the UVLO turnon threshold, UCC2813-0-Q1 starts to operate and consumes full operating current. At the beginning, because the output voltage is low, VCC cannot get energy from the auxiliary winding. The VCC capacitor is required to hold enough energy to prevent its voltage drop below UVLO during the start-up time, until the output reaches high enough. A larger capacitor holds more energy but slows down the start-up time. In this design, a 120-µF capacitor is chosen to provide enough energy for the start-up purpose.

9.2.2.10 Voltage Feedback Compensation Procedure

Feedback compensation, also called closed-loop control, reduces or eliminates steady-state output voltage error, reduces the sensitivity to parametric changes, changes the gain or phase of a system over some desired frequency range, reduces the effects of small-signal load disturbances and noise on system performance, and creates a stable system. This section describes how to compensate an isolated Flyback converter with the peak-current-mode control.

9.2.2.10.1 Power Stage Gain, Zeroes, and Poles

The first step in compensating a fixed-frequency flyback is to verify if the converter operates in continuous conduction mode (CCM) or discontinuous conduction mode (DCM). If the primary inductance (L_P) is greater than the inductance for DCM-CCM boundary mode operation, called the critical inductance (L_{Pcrit}), then the converter operates in CCM. L_{Pcrit} is calculated with Equation 17.

$$L_{Pcrit} = \frac{R_{OUT} \times N_{PS}^2}{2 \times f_{SW}} \times \left(\frac{V_{IN}}{V_{IN} + V_{OUT} \times N_{PS}} \right)^2 \quad (17)$$

For loads greater than 10% of P_{MAX} over the entire input voltage range, the selected primary inductance has value larger than the critical inductance. Therefore, the converter operates in CCM and the compensation loop requires design based on CCM flyback equations.

The current-to-voltage conversion is done externally with the ground-referenced current-sense resistor (R_{CS}) and the internal resistor divider sets up the internal current-sense gain, A_{CS} = 1.65. The device technology allows tight control of the resistor-divider ratio, regardless of the actual resistor value variations.

The DC open-loop gain (G_O) of the fixed-frequency voltage control loop of a peak-current-mode control CCM flyback converter shown in Figure 33 is approximated by first using the output load (R_{OUT}), the primary to secondary turns ratio (N_{PS}), and the maximum duty cycle (D) as shown in Equation 18.

$$G_O = \frac{R_{OUT} \times N_{PS}}{R_{CS} \times A_{CS}} \times \frac{1}{\frac{(1-D)^2}{\tau_L} + (2 \times M) + 1}$$

where

- $R_{OUT} = V_{OUT} / I_{OUT}$
- D is calculated with Equation 19
- τ_L is calculated with Equation 20
- M is calculated with Equation 21

(18)

$$D = \frac{N_{PS} \times V_{OUT}}{V_{IN} + (N_{PS} \times V_{OUT})}$$ (19)

$$\tau_L = \frac{2 \times L_P \times f_{SW}}{R_{OUT} \times N_{PS}^2}$$ (20)

$$M = \frac{V_{OUT} \times N_{PS}}{V_{IN}}$$ (21)

For this design, a converter with an output voltage (V_{OUT}) of 12 V, and 48 W relates to an output load (R_{OUT}) equal to 3 Ω at full load.

At minimum input bulk voltage of 75 V DC, the duty cycle reaches its maximum value of 0.615. The current sense resistance (R_{CS}) is 0.75 Ω and a primary to secondary turns-ratio (N_{PS}) is 10. The open-loop gain calculates to 14.95 dB.

A CCM flyback transfer function has two zeroes that are of interest. The ESR and the output capacitance contribute a left-half plane zero to the power stage, and the frequency of this zero (f_{ESRz}) is calculated with Equation 22.

$$\omega_{ESRz} = \frac{1}{R_{ESR} \times C_{OUT}}$$ (22)

The f_{ESRz} zero for a capacitance bank of three 680-µF capacitors (for a total output capacitance of 2040 µF) and a total ESR of 13 mΩ is located at 6 kHz.

CCM flyback converters have a zero in the right-half plane (RHP) of their transfer function. RHP zero has the same 20 dB/decade rising gain magnitude with increasing frequency just like a left-half plane zero, but it adds phase lag instead of lead. This phase lag tends to limit the overall loop bandwidth. The frequency location (f_{RHPz}) in Equation 23 is a function of the output load, the duty cycle, the primary inductance (L_P), and the primary to secondary side turns ratio (N_{PS}).

$$f_{RHPz} = \frac{R_{OUT} \times (1-D)^2 \times N_{PS}^2}{2 \times \pi \times L_P \times D}$$ (23)

RHP zero frequency increases with higher input voltage and lighter load. Generally, the design requires consideration of the worst case of the lowest RHP zero frequency and the converter must be compensated at the minimum input and maximum load condition. With a primary inductance of 1.5 mH, at 75-V DC input, the RHP zero frequency (f_{RHPz}) is equal to 7.65 kHz at maximum duty cycle (full load).

The power stage has one dominant pole (ω_{P1}) which is in the region of interest, located at a lower frequency (f_{P1}) which is related to the duty cycle (D), the output load, and the output capacitance. There is also a double pole (f_{P2}) located at half the switching frequency of the converter. These poles are frequencies calculated with Equation 24 and Equation 25.

$$f_{P1} = \frac{\frac{(1-D)^3}{\tau_L} + 1 + D}{2 \times \pi \times R_{OUT} \times C_{OUT}}$$ (24)

$$f_{P2} = \frac{f_{SW}}{2}$$ (25)

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Subharmonic oscillation is the large signal instability that can occur in CCM flyback converters when duty cycles extend beyond 50%. The subharmonic oscillation increases the output voltage ripple and sometimes it even limits the power handling capability of the converter. Slope compensation to the CS signal is a technique used to eliminate the instability.

Ideally, the target of slope compensation is to achieve quality coefficient (Q_P = 1) at half of the switching frequency. The Q_P is calculated by Equation 26.

$$Q_P = \frac{1}{\pi \times \left[M_C \times (1-D) - 0.5\right]} \tag{26}$$

where

- D is the primary side switch duty cycle
- M_C is the slope compensation factor, which is defined by Equation 27

$$M_C = 1 + \frac{S_e}{S_n} \tag{27}$$

where

- S_e is the compensation ramp slope
- S_n represents the rising current slope of the transformer primary inductance

The optimal goal of the slope compensation is to achieve Q_P equal to 1, which means M_C must be 2.128 when D reaches it maximum value of 0.615.

The inductance current slope at the CS pin is calculated by Equation 28.

$$S_n = \frac{V_{BULK(min)} \times R_{CS}}{L_P} = \frac{75V \times 0.75\Omega}{1.5mH} = 38mV/\mu s \tag{28}$$

The compensation slope is calculated by Equation 29.

$$S_e = (M_C - 1) \times S_n = (2.128 - 1) \times 38\ mV/\mu s = 46.3\ mV/\mu s \tag{29}$$

The compensation slope is added into the system through R_{RAMP} and R_{CSF}. A series capacitor (C_{RAMP}) is selected to approximate a high-frequency short circuit. Choose C_{RAMP} as 10 nF as the starting point, and make adjustments if required. R_{RAMP} and R_{CSF} form a voltage divider to scale the RC pin ramp voltage and inject the slope compensation into CS pin. Choose R_{RAMP} much larger than the R_T resistor so that it does not affect the frequency setting very much. In this design, R_{RAMP} is selected as 24.9 kΩ. The RC pin ramp slope is calculated with Equation 30.

$$S_{RC} = 2.4\ V \times 100\ kHz = 240\ mV/\mu s \tag{30}$$

To achieve 46.3 mV/µs compensation slope, R_{CSF} resistor is calculated with Equation 31.

$$R_{CSF} = \frac{R_{RAMP}}{\frac{S_{RC}}{S_e} - 1} = \frac{24.9\ k\Omega}{\frac{240\ mV/\mu s}{46.3\ mV/\mu s} - 1} = 5.95\ k\Omega \tag{31}$$

The power stage open-loop gain and phase can be plotted as a function of frequency. The total open-loop transfer function, as a function of frequency, can be characterized by Equation 32.

$$H_0(S) = G_0 \times \frac{\left(1 + \frac{S}{\omega_{ESRz}}\right) \times \left(1 - \frac{S}{\omega_{RHPz}}\right)}{1 + \frac{S}{\omega_{P1}}} \times \frac{1}{1 + \frac{S}{\omega_{P2} \times Q_P} + \frac{S^2}{\omega_{P2}^2}} \tag{32}$$

where

- ω_{P1} and ω_{P2} are based on the frequencies calculated by Equation 24 and Equation 25

The open-loop gain and phase Bode plots are graphed accordingly (see Figure 34 and Figure 35).

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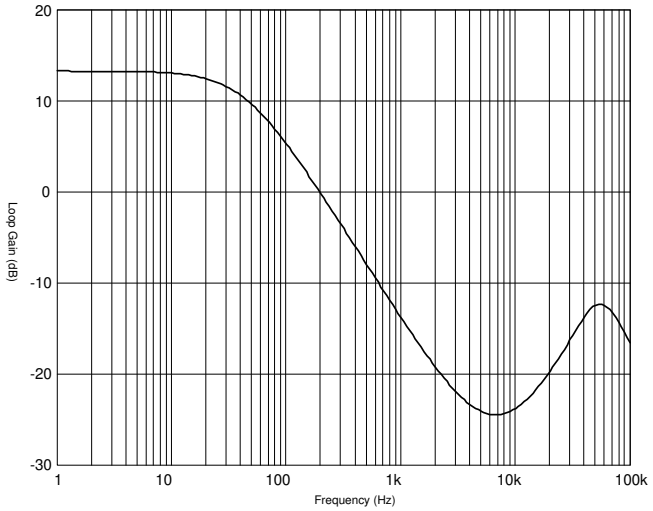


Figure 34. Converter Open-Loop Bode Plot: Gain

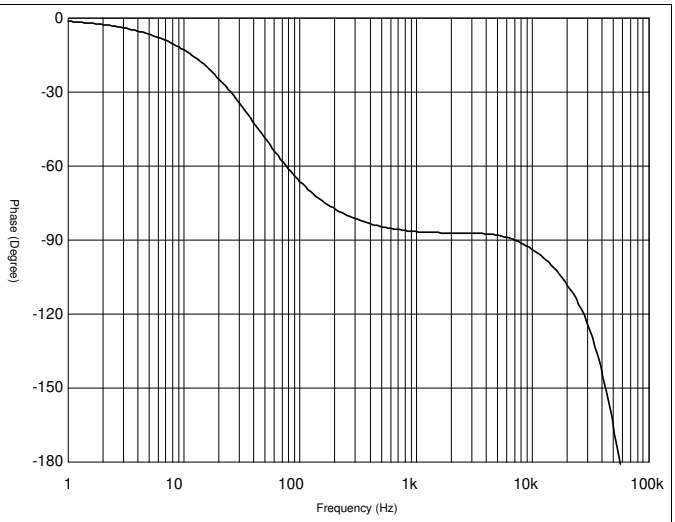


Figure 35. Converter Open-Loop Bode Plot: Phase

9.2.2.10.2 Compensating the Loop

For good transient response, the bandwidth of the finalized design must be as wide as possible. The bandwidth of a CCM flyback (f_{BW}) is limited to ¼ of the RHP-zero frequency, or approximately 1.9 kHz using Equation 33.

$$f_{BW} = \frac{f_{RHPz}}{4} \tag{33}$$

The gain of the open-loop power stage at f_{BW} is equal to –22.4 dB and the phase at f_{BW} is equal to –87°. First step is to choose the output voltage-sensing resistor values. The output sensing resistors are selected based on the allowed power consumption and in this case, 1 mA of sensing current is assumed.

The TL431 is used as the feedback amplifier. Given its 2.5-V reference voltage, the voltage-sensing dividers R_{FBU} and R_{FBB} can be selected with Equation 34 and Equation 35.

$$R_{FBU} = \frac{V_{OUT} - 2.5\ V}{1\,mA} = 9.5\ k\Omega \tag{34}$$

$$R_{FBB} = \frac{2.5\ V}{1\,mA} = 2.5\ k\Omega \tag{35}$$

Next step is to put the compensator zero f_{CZ} at 190 Hz, which is 1/10 of the target crossover frequency. Choose C_Z as a fixed value of 10 nF and choose the zero resistor value according to Equation 36.

$$R_Z = \frac{1}{2\pi \times f_{CZ} \times C_Z} = \frac{1}{2\pi \times 190\ Hz \times 10\ nF} = 83.77\ k\Omega \tag{36}$$

Next, place a pole at the lower of RHP-zero or the ESR-zero frequencies. Based previous analysis, the RHP zero is at 7.65 kHz and the ESR zero is at 6 kHz, so the pole of the compensation loop should be put at 6 kHz. This pole can be added through the primary side error amplifier. R_{FB} and C_{FB} provide the necessary pole. Choosing R_{FB} as 10 kΩ, C_{FB} is calculated by Equation 37.

$$C_{FB} = \frac{1}{2\pi \times 10\ k\Omega \times 6\ kHz} = 2.65\ nF \tag{37}$$

Based on the compensation loop structure, the entire compensation loop transfer function is written as Equation 38.

$$G(S) = \frac{1}{R_{FBU} \cdot R_{LED}} \cdot \frac{1 + S \cdot C_Z \cdot R_Z}{S \cdot C_Z} \cdot \frac{R_{FB2}}{R_{FB1}} \cdot \frac{1}{S \cdot C_{FB} \cdot R_{FB2} + 1} \cdot CTR \cdot R_{EG}$$

where

- CTR is the current transfer ratio of the opto-coupler. Choose 1 as the nominal value for CTR.
- R_{EG} is the opto-emitter pulldown resistor and 1 kΩ is chosen as a default value

(38)

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The only remaining unknown value required in this equation is R_{LED}. The entire loop gain must be equal to 1 at the crossover frequency. R_{LED} is calculated accordingly as 1.62 kΩ.

The final closed-loop Bode plots are shown in Figure 36 and Figure 37. The converter achieves approximately 2-kHz crossover frequency and approximately 70° of phase margin.

TI recommends checking the loop stability across all the corner cases, including component tolerances, to ensure system stability.

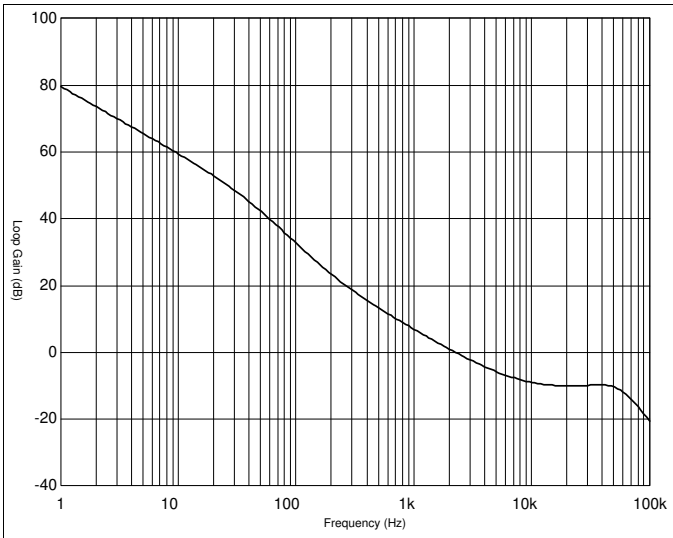


Figure 36. Converter Closed-Loop Bode Plot: Gain

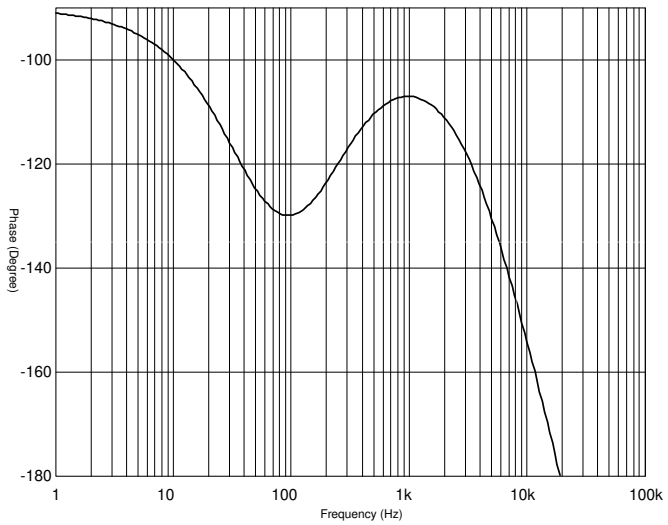


Figure 37. Converter Closed-Loop Bode Plot: Phase

9.2.3 Application Curves

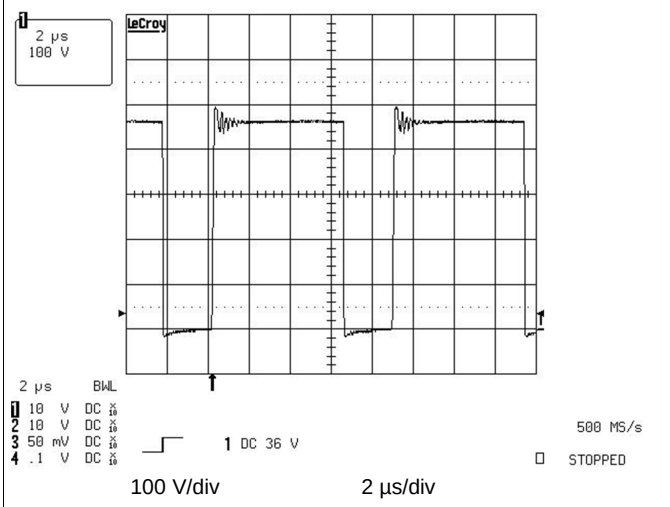


Figure 38. Primary Side MOSFET Drain to Source Voltage at 240-V AC Input

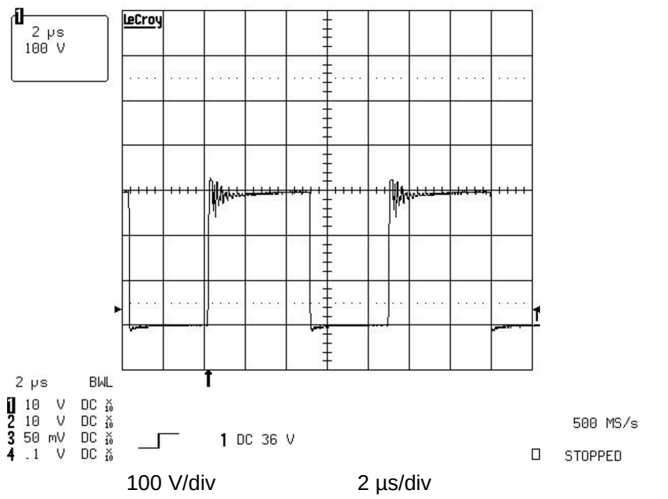
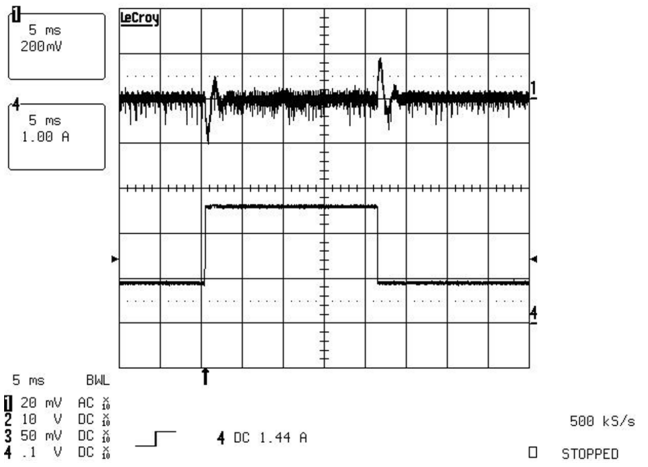


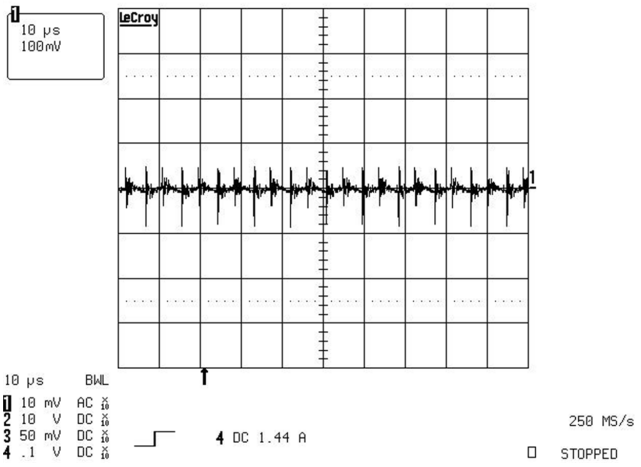
Figure 39. Primary Side MOSFET Drain to Source Voltage at 120-V AC Input

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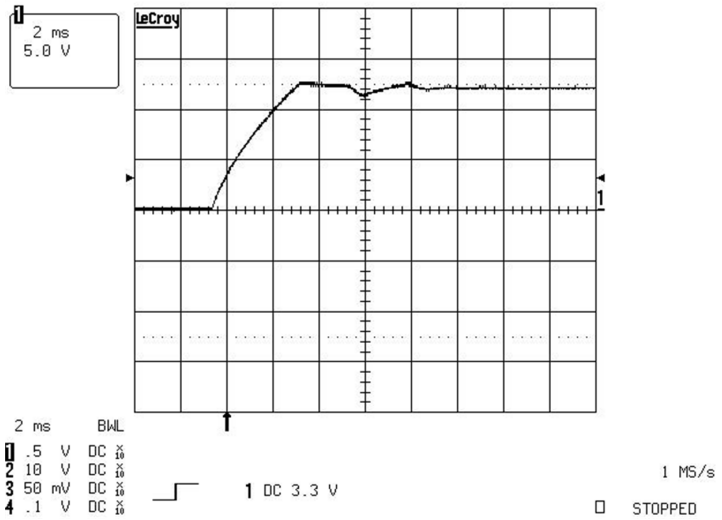
CH1: output voltage AC coupled 200 mV/div
CH4: output current 1 A/div 5 ms/div

Figure 40. Output Voltage During 0.9-A to 2.7-A Load Transient



100 mV/div 10 µs/div

Figure 41. Output Voltage Ripple at Full Load



5 V/div 2 ms/div

Figure 42. Output Voltage Behavior at Full Load Start-Up

10 Power Supply Recommendations

An internal VCC shunt regulator is incorporated into each member of the UCC2813-x-Q1 family to limit the supply voltage to approximately 13.5 V. A series resistor from VCC to the input supply source is required with inputs above 12 V to limit the shunt regulator current. A maximum of 10 mA can be shunted to ground by the internal regulator. The internal regulator in conjunction with the device's low start-up and operating current can greatly simplify powering the device and may eliminate the requirement for a regulated bootstrap auxiliary supply and winding in many applications. The supply voltage is MOSFET gate level compatible and requires no external Zener diode or regulator protection with a current-limited input supply. The UVLO start-up threshold is 1 V below the shunt regulator level on the UCC2813-[2,4]-Q1 devices to ensure start-up. It is important to bypass the device's supply (VCC) and reference voltage (REF) pins each with a 0.1-µF to 1-µF ceramic capacitor to ground. The capacitors must be placed as close to the actual pin connections as possible for optimal noise filtering. A second, larger filter capacitor may also be required in offline applications to hold the supply voltage (V_{VCC}) above the UVLO turnoff threshold during start-up.

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The UVLO start threshold of the UCC2813-[2,4]-Q1 devices has a range of 11.5 V to 13.5 V, while the protection zener voltage can vary from 12 V to 15 V. However, the absolute maximum supply voltage of the IC is specified at 12 V. This absolute maximum is defined as the lowest possible Zener voltage when driven from a low impedance (voltage) source. The zener voltage is always higher than the UVLO start voltage. These two parameters track each other and the chip is tested to guarantee that the Zener voltage will never be below that of the start voltage. To limit the current flowing in the internal clamp zener, a series resistor must be added. Failure to provide a series resistance between the auxiliary voltage source and the Vcc pin of the controller, to limit the current and voltage stress within rated levels on the Vcc pin may result in permanent damage to the controller. In automotive or industrial applications where there is a risk of high power load transients which may cause transients or voltage excursions on the Vcc rail supplying the PWM controller it is recommended to add an external Zener diode across the Vcc pin. The external Zener acts as an additional protection to the impedance provided by the series resistor between the Vcc source and Vcc pin.

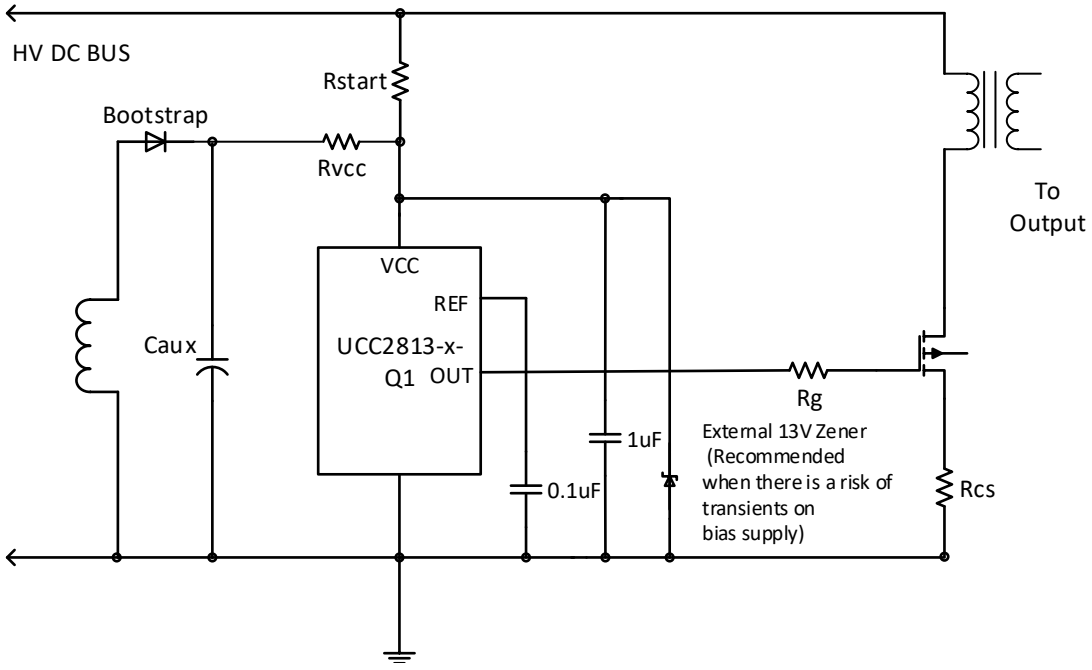


Figure 43. Power-Up Recommendation

Placing a resistor, Rg, in series with the gate of the mosfet allows the mosfet switching speed to be adjusted and also can be used to keep the peak gate drive currents within the specified limits of the controller.

11 Layout

11.1 Layout Guidelines

In addition to following general power management device layout guidelines (star grounding, minimal current loops, reasonable impedance levels, and so on) layout for the UCC2813-x-Q1 family must consider the following:

- If possible, a ground plane should be used to minimize the voltage drop on the ground circuit and the noise introduced by parasitic inductances in individual traces.
- A decoupling capacitor is required for each the VCC pin and REF pin and both must be returned to GND as close to the device as possible.
- For the best performance, keep the timing capacitor lead to GND as short and direct as possible. If possible, use separate ground traces for the timing capacitor and all other functions.
- The CS pin filter capacitor must be as close to the device possible and grounded right at the device ground pin. This ensures the best filtering effect and minimizes the chance of current sense pin malfunction.
- Gate-drive loop area must be minimized to reduce the EMI noise generated by the high di/dt of the current in the loop.

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11.2 Layout Example

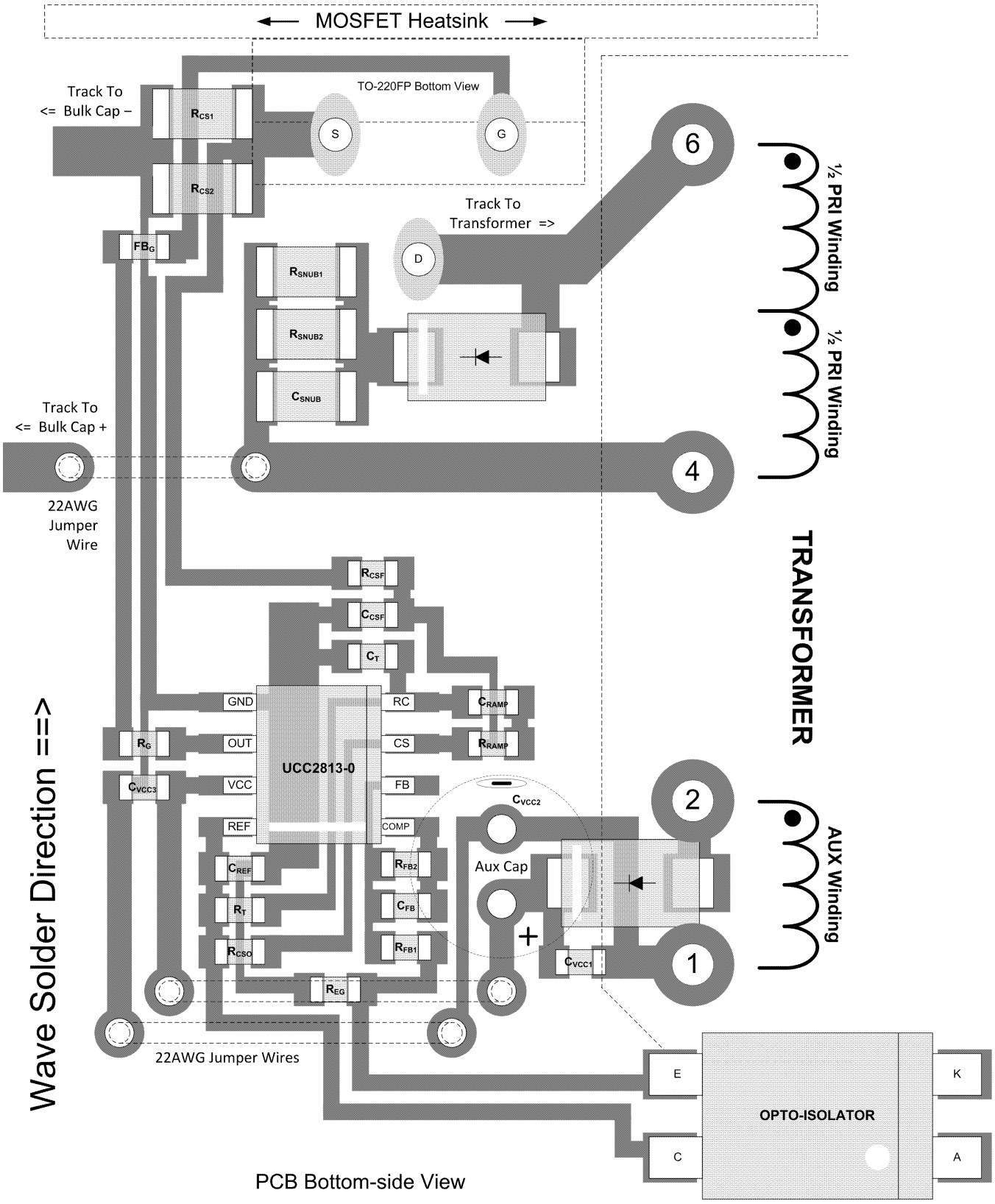


Figure 44. UCC2813-0-Q1 Layout Example for Single-Layer PCB

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Differences Between the UCC3813 and UCC3800 PWM Families (SLUA247)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC2813-0-Q1	Click here	Click here	Click here	Click here	Click here
UCC2813-1-Q1	Click here	Click here	Click here	Click here	Click here
UCC2813-2-Q1	Click here	Click here	Click here	Click here	Click here
UCC2813-3-Q1	Click here	Click here	Click here	Click here	Click here
UCC2813-4-Q1	Click here	Click here	Click here	Click here	Click here
UCC2813-5-Q1	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 Trademarks

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12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC2813QDR-0Q1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2813-0, 2813-0Q1)	Samples
UCC2813QDR-1Q1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2813-1, 2813-1Q1)	Samples
UCC2813QDR-2Q1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2813-2, 2813-2Q1)	Samples
UCC2813QDR-3Q1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2813-3, 2813-3Q1)	Samples
UCC2813QDR-4Q1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2813-4, 2813-4Q1)	Samples
UCC2813QDR-5Q1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2813-5, 2813-5Q1)	Samples
UCC2813QPWR-3Q1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28133Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC2813-0-Q1, UCC2813-1-Q1, UCC2813-2-Q1, UCC2813-3-Q1, UCC2813-4-Q1, UCC2813-5-Q1 :

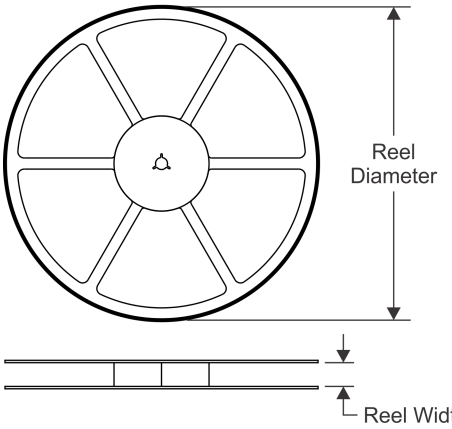
- Catalog: UCC2813-0, UCC2813-1, UCC2813-2, UCC2813-3, UCC2813-4, UCC2813-5

NOTE: Qualified Version Definitions:

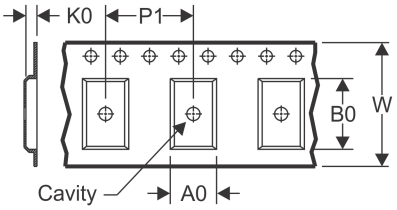
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

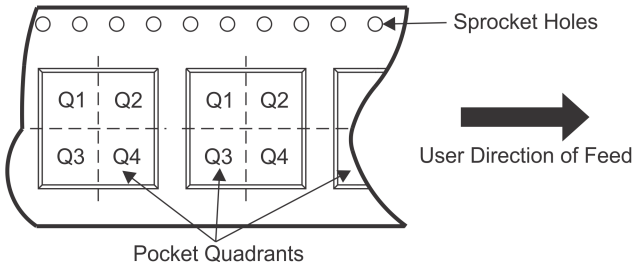


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

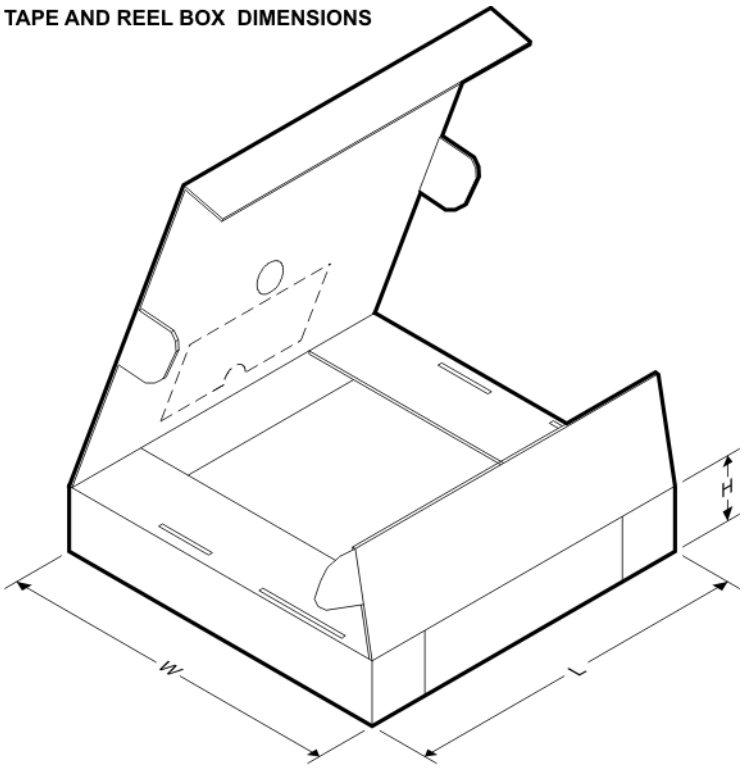
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

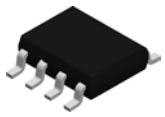
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2813QDR-0Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2813QDR-1Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2813QDR-2Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2813QDR-3Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2813QDR-4Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2813QDR-5Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2813QPWR-3Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2813QDR-0Q1	SOIC	D	8	2500	853.0	449.0	35.0
UCC2813QDR-1Q1	SOIC	D	8	2500	853.0	449.0	35.0
UCC2813QDR-2Q1	SOIC	D	8	2500	853.0	449.0	35.0
UCC2813QDR-3Q1	SOIC	D	8	2500	853.0	449.0	35.0
UCC2813QDR-4Q1	SOIC	D	8	2500	853.0	449.0	35.0
UCC2813QDR-5Q1	SOIC	D	8	2500	853.0	449.0	35.0
UCC2813QPWR-3Q1	TSSOP	PW	8	2000	367.0	367.0	35.0

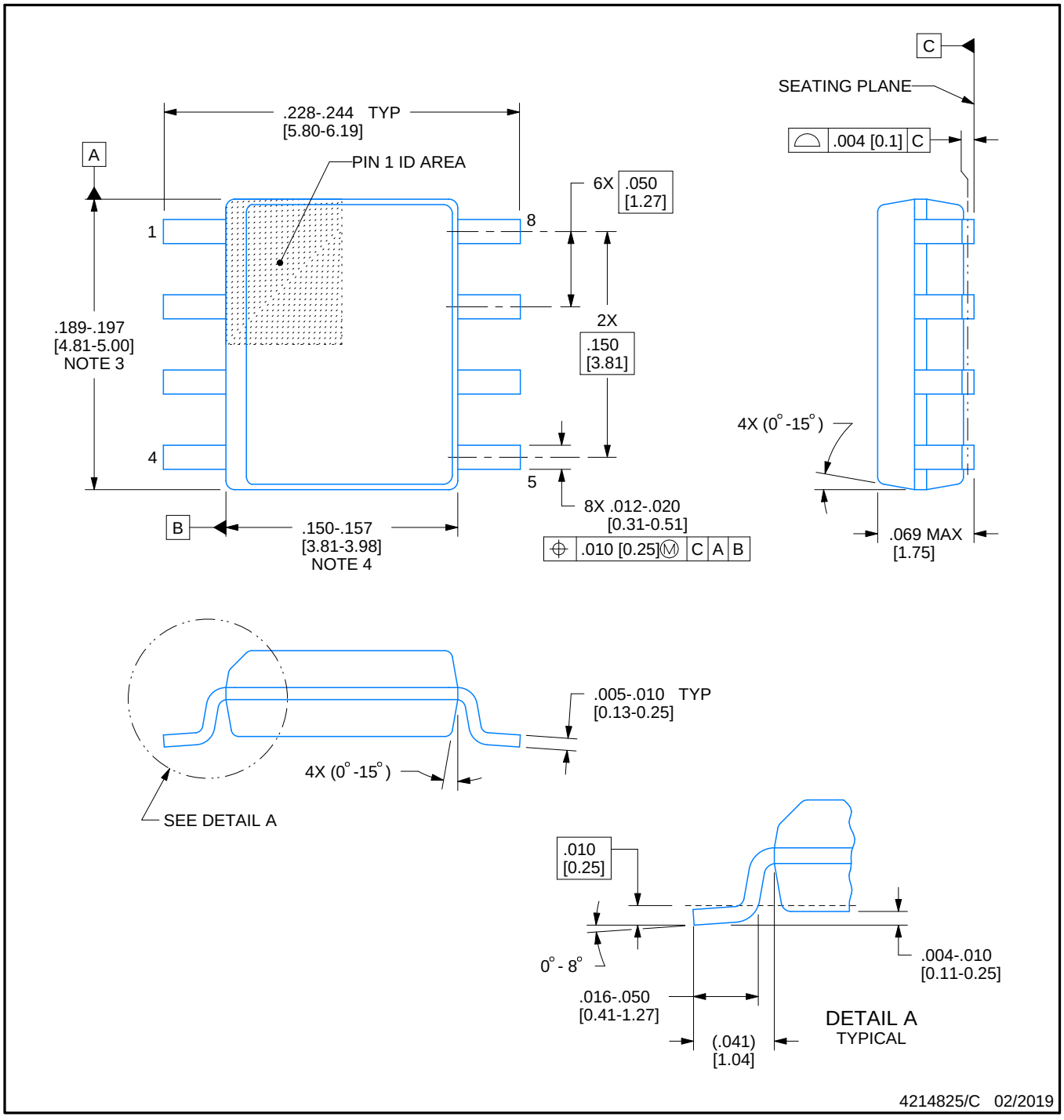


PACKAGE OUTLINE

D0008A

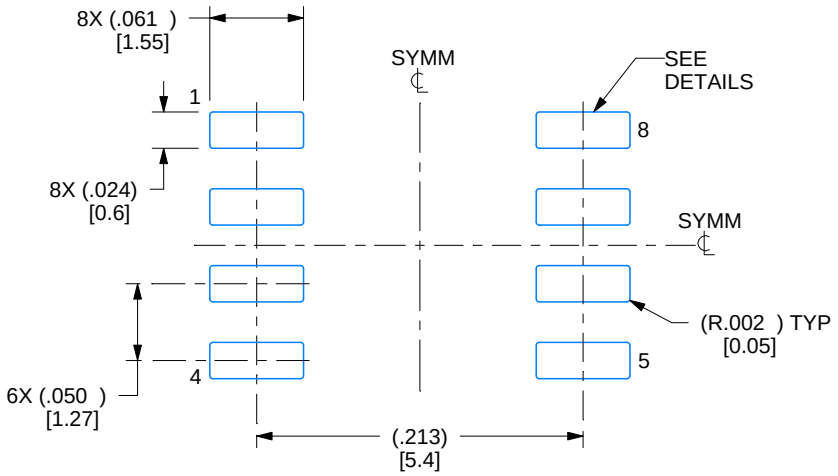
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

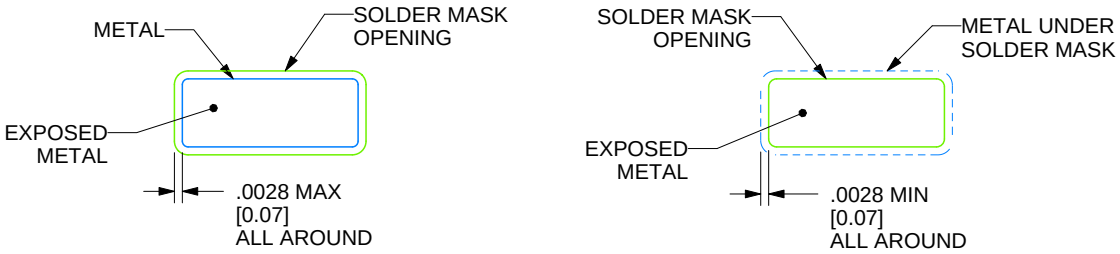


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

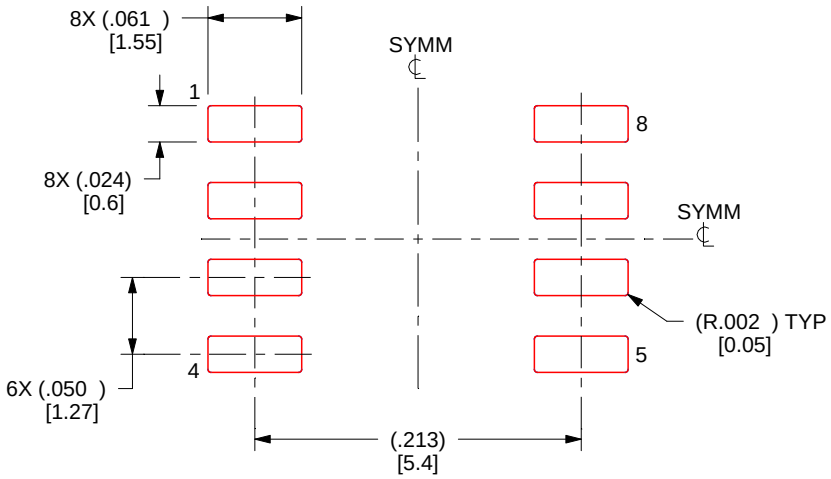
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

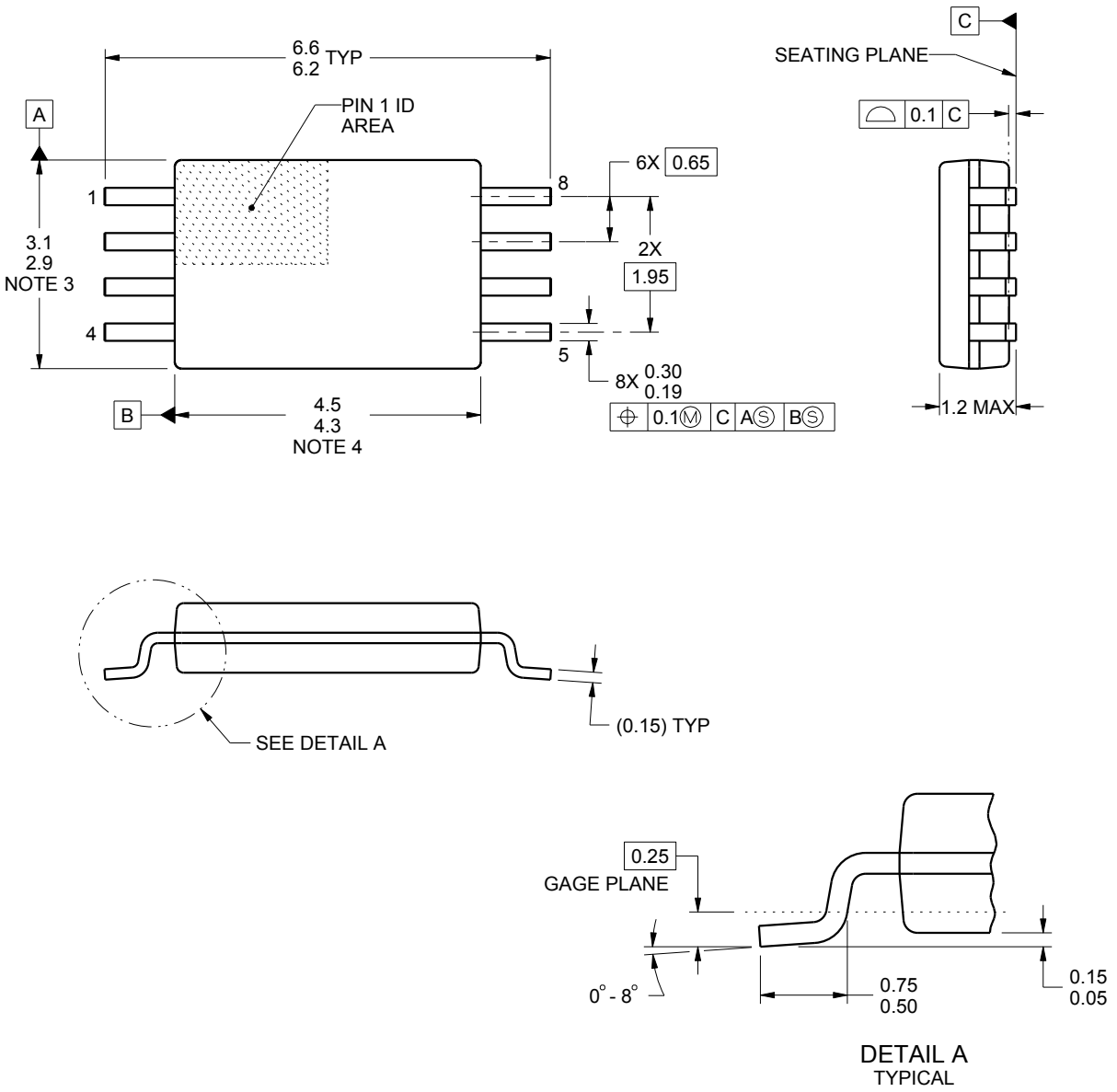
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

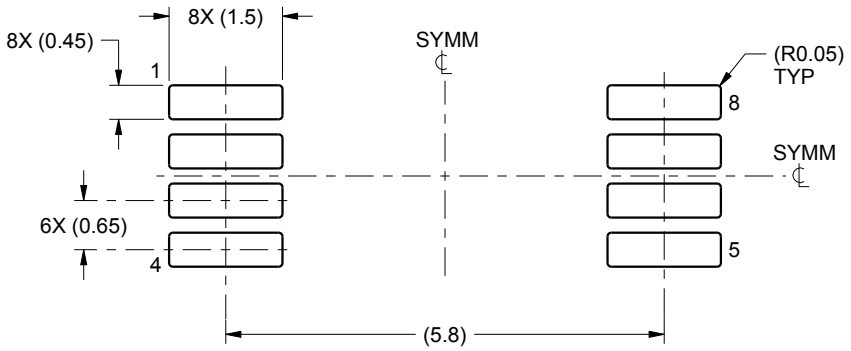
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

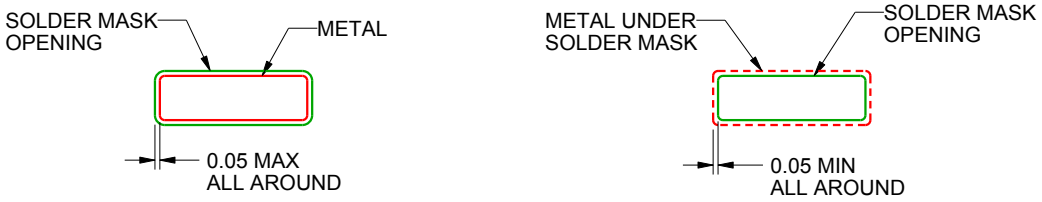


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

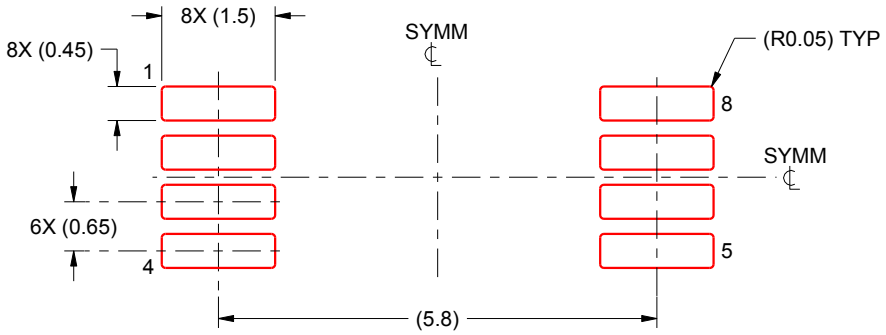


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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