OPAx991 40-V 轨至轨输入/输出、低失调电压、低噪声运算放大器

1 特性

- 低失调电压：±125µV
- 低失调电压温漂：±0.3µV/°C
- 低噪声：1kHz 时为 10.5nV/√Hz
- 高共模抑制：130dB
- 低偏置电流：±10pA
- 轨至轨输入和输出
- 宽带宽：4.5MHz GBW
- 高压摆率：21V/µs
- 高容性负载驱动：1nF
- 支持多路复用器/比较器的输入
  - 放大器以最高达到电源轨的差分输入工作
  - 放大器可用于开环中，也可用作比较器
- 低静态电流：每个放大器 560µA
- 宽电源电压范围：±1.35V 至 ±20V，2.7V 至 40V
- 强大的 EMIRR 性能：输入引脚和电源引脚上采用 EMI/RFI 滤波器
- 电源轨的差分和共模输入电压范围

2 应用

- 低功率音频前置放大器
- 多路复用数据采集系统
- 测试和测量设备
- ADC 驱动器放大器
- SAR ADC 基准缓冲器
- 可编程逻辑控制器
- 高侧和低侧电流感应
- 高精度比较器

3 说明

OPAx991 系列（OPA991、OPA2991 和 OPA4991）是高电压 (40V) 通用运算放大器系列。这些器件具有出色的直流精度和交流性能，包括轨至轨输入/输出、低失调电压（典型值为 ±125µV）、低温漂（典型值为 ±0.3µV/°C）、低噪声（10.5nV/√Hz 和 1.8µV_{PP}）和 4.5MHz 带宽。

OPAx991 拥有独特 特性，例如电源轨的差分和共模输入电压范围、高输出电流 (±75mA)、高压摆率 (21V/µs)、高容性负载驱动 (1nF) 和关断功能，是一款稳定可靠的高性能运算放大器，适用于高电压工业 应用。

OPAx991 运算放大器系列采用*微型*封装（例如 X2QFN、WSON 和 SOT-553）以及标准封装（例如 SOT-23、SOIC 和 TSSOP），额定工作温度范围为 -40°C 至 125°C。

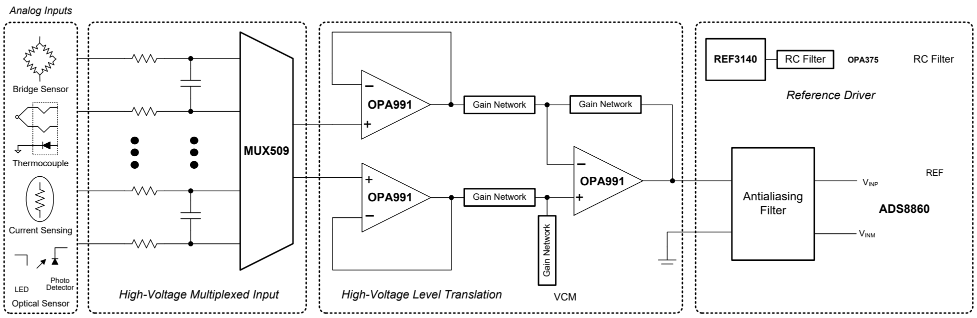
器件信息(1)

器件型号	封装	封装尺寸（标称值）
OPA991	SOT-23 (5)(2)	2.90mm × 1.60mm
	SOT-23 (6)(2)	2.90mm × 1.60mm
	SC70 (5)(2)	2.00mm × 1.25mm
OPA2991	SOIC (8)	4.90mm × 3.90mm
	SOT-23-8 (8)(2)	2.90mm × 1.60mm
	TSSOP (8)	3.00mm × 4.40mm
	VSSOP (8)(2)	3.00mm × 3.00mm
	WSON (8)(2)	2.00mm × 2.00mm
	X2QFN (10)(2)	1.50mm × 1.50mm
OPA4991	SOIC (14)(2)	8.65mm × 3.90mm
	TSSOP (14)(2)	5.00mm × 4.40mm
	WQFN (16)(2)	3.00mm × 3.00mm
	X2QFN (14)(2)	2.00mm × 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装仅为预览版。

OPAx991 应用于高压多路复用数据采集系统



English Data Sheet: SBOS969

目录

1 特性 1
2 应用 1
3 说明 1
4 修订历史记录 2
5 **Pin Configuration and Functions** 3
6 **Specifications** 10
  6.1 Absolute Maximum Ratings 10
  6.2 ESD Ratings 10
  6.3 Recommended Operating Conditions 10
  6.4 Thermal Information for Single Channel 10
  6.5 Thermal Information for Dual Channel 11
  6.6 Thermal Information for Quad Channel 11
  6.7 Electrical Characteristics 12
  6.8 Typical Characteristics 15
7 **Detailed Description** 22
  7.1 Overview 22
  7.2 Functional Block Diagram 22
  7.3 Feature Description 23
  7.4 Device Functional Modes 31
8 **Application and Implementation** 32
  8.1 Application Information 32
  8.2 Typical Applications 32
9 **Power Supply Recommendations** 34
10 **Layout** 34
  10.1 Layout Guidelines 34
  10.2 Layout Example 35
11 器件和文档支持 36
  11.1 器件支持 36
  11.2 文档支持 36
  11.3 接收文档更新通知 36
  11.4 社区资源 36
  11.5 商标 36
  11.6 静电放电警告 37
  11.7 Glossary 37
12 机械、封装和可订购信息 38

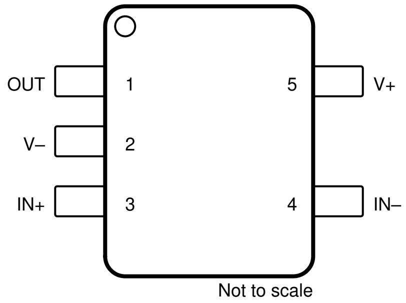
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (October 2019) to Revision A	Page
• 已更改 将 OPA2991 器件状态从*预告信息* 更改为*生产数据*	1
• 在*器件信息* 中删除了 SOIC (D) 封装的预发布符号	1
• Removed preview notation from SOIC (D) package in *Pin Configuration and Functions* section	5
• 已添加 *Typical Characteristics* section in *Specifications* section	15
• 已添加 在*相关文档* 部分添加了其他参考	36

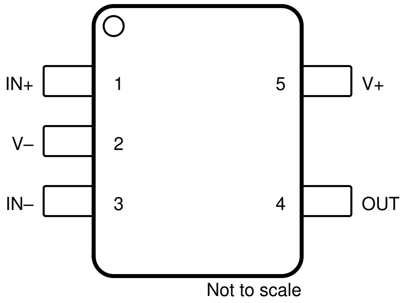
5 Pin Configuration and Functions

OPA991 DBV and DRL Package(1)
5-Pin SOT-23 and SOT-553
Top View



(1) Package is preview only.

OPA991 DCK Package(1)
5-Pin SC70
Top View

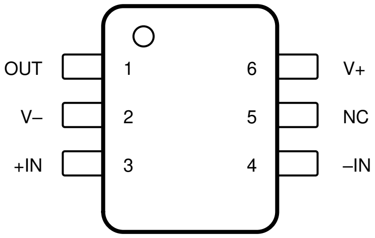


(1) Package is preview only.

Pin Functions: OPA991

PIN			I/O	DESCRIPTION
NAME	DBV, DCK, DRL	DCK		
+IN	3	1	I	Noninverting input
–IN	4	3	I	Inverting input
OUT	1	4	O	Output
V+	5	5	—	Positive (highest) power supply
V–	2	2	—	Negative (lowest) power supply

OPA991S DBV and DRL Package[1]
6-Pin SOT-23 and SOT-563
Top View



Not to scale

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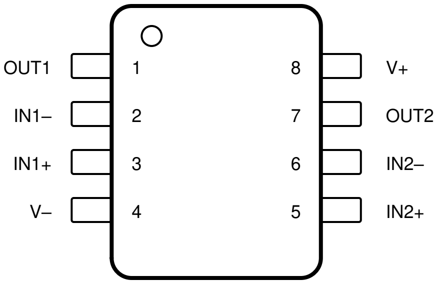
(1) Package is preview only.

Pin Functions: OPA991S

PIN		I/O	DESCRIPTION
NAME	DBV, DRL		
+IN	3	I	Noninverting input
–IN	4	I	Inverting input
OUT	1	O	Output
$\overline{\text{SHDN}}$	5	I	Shutdown (active low) logic input
V+	6	—	Positive (highest) power supply
V–	2	—	Negative (lowest) power supply

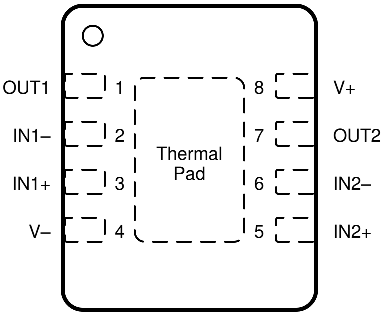
OPA2991 D, DDF, DGK, and PW Packages[1]
8-Pin SOIC, SOT-23-8, TSSOP, and VSSOP
Top View



Not to scale

(1) DDF, DGK, and PW packages are preview only.

OPA2991 DSG Package[1][2]
8-Pin WSON With Exposed Thermal Pad
Top View



Not to scale

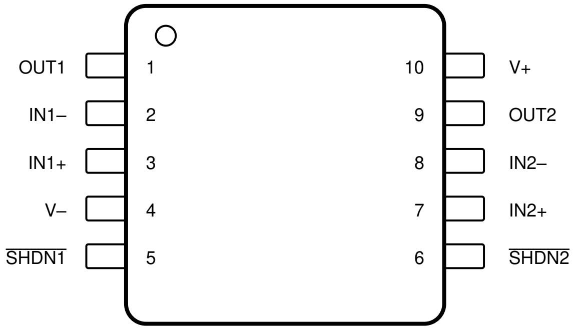
(1) Connect thermal pad to V–.

(2) Package is preview only. See *Packages With an Exposed Thermal Pad* section for more information.

Pin Functions: OPA2991

PIN		I/O	DESCRIPTION
NAME	SOIC, TSSOP, VSSOP, WSON		
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

OPA2991S DGS Package[(1)]
10-Pin VSSOP
Top View



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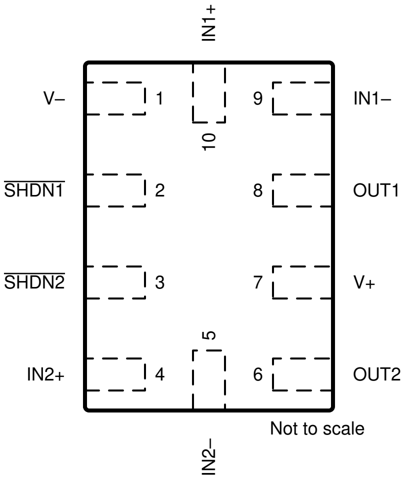
(1) Package is preview only.

OPA2991S RUG Package[(1)]
10-Pin X2QFN
Top View



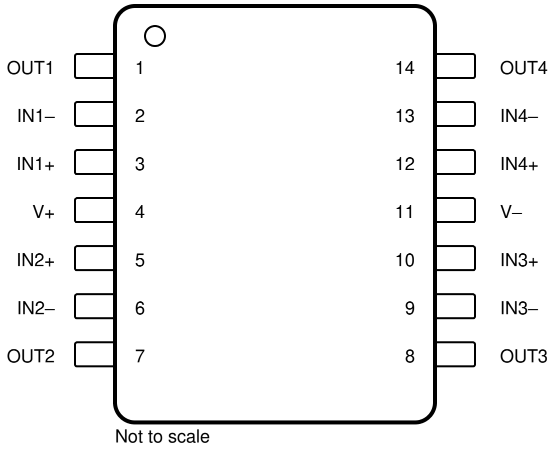
Not to scale

(1) Package is preview only.

Pin Functions: OPA2991S

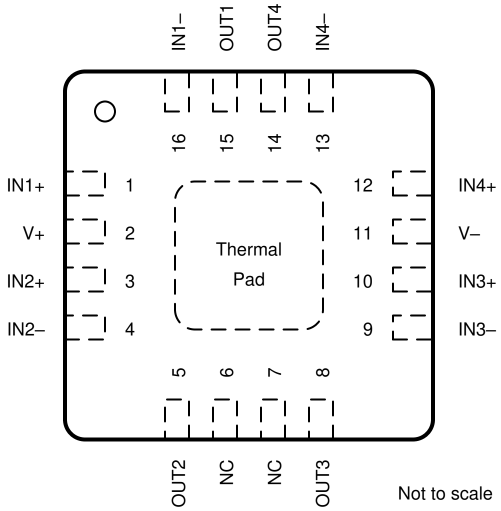
PIN			I/O	DESCRIPTION
NAME	VSSOP	X2QFN		
+IN A	3	10	I	Noninverting input, channel A
+IN B	7	4	I	Noninverting input, channel B
–IN A	2	9	I	Inverting input, channel A
–IN B	8	5	I	Inverting input, channel B
OUT A	1	8	O	Output, channel A
OUT B	9	6	O	Output, channel B
$\overline{\text{SHDN 1}}$	5	2	I	Shutdown, channel 1: low = amplifier enabled, high = amplifier disabled. See *Shutdown* section for more information.
$\overline{\text{SHDN 2}}$	6	3	I	Shutdown, channel 2: low = amplifier enabled, high = amplifier disabled. See *Shutdown* section for more information.
V+	10	7	—	Positive (highest) power supply
V–	4	1	—	Negative (lowest) power supply

OPA4991 D and PW Packages(1)
14-Pin SOIC and TSSOP
Top View



(1) Package is preview only.

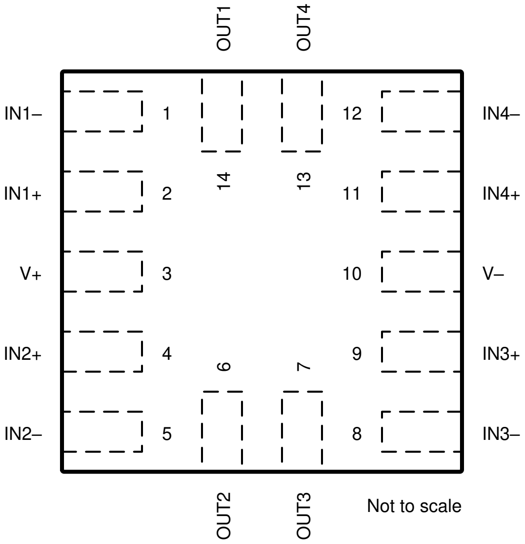
OPA4991 RTE Package(1)(2)
16-Pin WQFN With Exposed Thermal Pad
Top View



(1) Connect thermal pad to V–. See *Packages With an Exposed Thermal Pad* section for more information.

(2) Package is preview only.

OPA4991 RUC Packages(1)
14-Pin WQFN With Exposed Thermal Pad
Top View

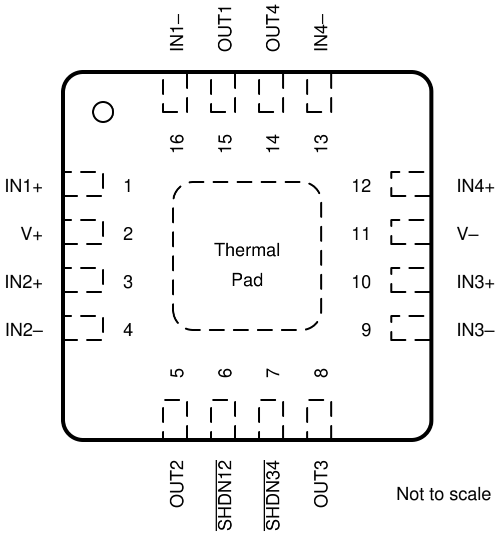


(1) Package is preview only.

Pin Functions: OPA4991

PIN			I/O	DESCRIPTION
NAME	SOIC, TSSOP	WQFN		
IN1+	3	1	I	Noninverting input, channel 1
IN1–	2	16	I	Inverting input, channel 1
IN2+	5	3	I	Noninverting input, channel 2
IN2–	6	4	I	Inverting input, channel 2
IN3+	10	10	I	Noninverting input, channel 3
IN3–	9	9	I	Inverting input, channel 3
IN4+	12	12	I	Noninverting input, channel 4
IN4–	13	13	I	Inverting input, channel 4
NC	—	6, 7	—	Do not connect
OUT1	1	15	O	Output, channel 1
OUT2	7	5	O	Output, channel 2
OUT3	8	8	O	Output, channel 3
OUT4	14	14	O	Output, channel 4
V+	4	2	—	Positive (highest) power supply
V–	11	11	—	Negative (lowest) power supply

OPA4991S RTE Package[1]
16-Pin WQFN With Exposed Thermal Pad
Top View



[1] Package is preview only.

Pin Functions: OPA4991S

PIN		I/O	DESCRIPTION
NAME	RTE		
IN1+	1	I	Noninverting input, channel 1
IN1-	16	I	Inverting input, channel 1
IN2+	3	I	Noninverting input, channel 2
IN2-	4	I	Inverting input, channel 2
IN3+	10	I	Noninverting input, channel 3
IN3-	9	I	Inverting input, channel 3
IN4+	12	I	Noninverting input, channel 4
IN4-	13	I	Inverting input, channel 4
OUT1	15	O	Output, channel 1
OUT2	5	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
$\overline{\text{SHDN12}}$	6	I	Shutdown (active low), channel 1 & 2, logic input
$\overline{\text{SHDN34}}$	7	I	Shutdown (active low), channel 3 & 4, logic input
VCC+	2	—	Positive (highest) power supply
VCC-	11	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	42	V
Signal input pins	Common-mode voltage (2)	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage (2)		V_S + 0.2	V
	Current (2)	–10	10	mA
Output short-circuit (3)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operating the device beyond the ratings listed under *Absolute Maximum Ratings* will cause permanent damage to the device. These are stress ratings only, based on process and design limitations, and this device has not been designed to function outside the conditions indicated under *Recommended Operating Conditions*. Exposure to any condition outside *Recommended Operating Conditions* for extended periods, including absolute-maximum-rated conditions, may affect device reliability and performance.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package. This device has been designed to limit *electrical* damage due to excessive output current, but extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual *thermal* destruction. See the Thermal Protection section for more information.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	2.7	40	V
V_I	Input voltage range	(V–) – 0.1	(V+) + 0.1	V
T_A	Specified temperature	–40	125	°C

6.4 Thermal Information for Single Channel

THERMAL METRIC (1)		OPA991, OPA991S					UNIT
		DBV (2) (SOT-23)		DCK (2) (SC70)	DRL (2) (SOT-553)		
		5 PINS	6 PINS	5 PINS	5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	TBD	TBD	TBD	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	TBD	TBD	TBD	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	TBD	TBD	TBD	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	TBD	TBD	TBD	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	TBD	TBD	TBD	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	TBD	TBD	TBD	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) This package option is preview for OPA991.

6.5 Thermal Information for Dual Channel

THERMAL METRIC (1)		OPA2991, OPA2991S							UNIT
		D (2) (SOIC)	DDF (2) (SOT-23-8)	DGK (2) (VSSOP)	DGS (2) (VSSOP)	DSG (2) (WSON)	PW (2) (TSSOP)	RUG (2) (X2QFN)	
		8 PINS	8 PINS	8 PINS	10 PINS	8 PINS	8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	130.7	TBD	TBD	TBD	TBD	TBD	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.8	TBD	TBD	TBD	TBD	TBD	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	74.0	TBD	TBD	TBD	TBD	TBD	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	24.0	TBD	TBD	TBD	TBD	TBD	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	73.3	TBD	TBD	TBD	TBD	TBD	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	TBD	TBD	TBD	TBD	TBD	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) This package option is preview for OPA2991.

6.6 Thermal Information for Quad Channel

THERMAL METRIC (1)		OPA4991, OPA4991S					UNIT
		D (2) (SOIC)	PW (2) (TSSOP)		RTE (2) (WQFN)	RUC (2) (WQFN)	
		14 PINS	14 PINS	16 PINS	16 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	TBD	TBD	TBD	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	TBD	TBD	TBD	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	TBD	TBD	TBD	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	TBD	TBD	TBD	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	TBD	TBD	TBD	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	TBD	TBD	TBD	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) This package option is preview for OPA4991.

6.7 Electrical Characteristics

For V_S = (V+) – (V–) = 2.7 V to 40 V (±1.35 V to ±20 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = V–			±125	±750	µV
			T_A = –40°C to 125°C			±780	
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to 125°C		±0.3		µV/°C
PSRR	Input offset voltage versus power supply	V_{CM} = V–, V_S = 4 V to 40 V	T_A = –40°C to 125°C		±0.3	±1	µV/V
		V_{CM} = V–, V_S = 2.7 V to 40 V(1)			±1	±5	
	Channel separation	f = 0 Hz			5		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±10		pA
I_{OS}	Input offset current				±10		pA
NOISE							
E_N	Input voltage noise	f = 0.1 Hz to 10 Hz			1.8		$µV_{PP}$
					0.3		$µV_{RMS}$
e_N	Input voltage noise density	f = 1 kHz			10.8		nV/√Hz
		f = 10 kHz			9.4		
i_N	Input current noise	f = 1 kHz			2		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 40 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V (Main input pair)	T_A = –40°C to 125°C	109	130		dB
		V_S = 4 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V (Main input pair)		84	100		
		V_S = 2.7 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V (Main input pair)(1)		75	95		
		V_S = 2.7 V to 40 V, (V+) – 1 V < V_{CM} < (V+) + 0.1 V (Aux input pair)			85		
INPUT CAPACITANCE							
Z_{ID}	Differential				100 || 9		MΩ || pF
Z_{ICM}	Common-mode				6 || 1		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 40 V, V_{CM} = V– (V–) + 0.1 V < V_O < (V+) – 0.1 V		120	145		dB
			T_A = –40°C to 125°C		142		
		V_S = 4 V, V_{CM} = V– (V–) + 0.1 V < V_O < (V+) – 0.1 V		104	130		
			T_A = –40°C to 125°C		125		
		V_S = 2.7 V, V_{CM} = V– (V–) + 0.1 V < V_O < (V+) – 0.1 V(1)		101	120		
			T_A = –40°C to 125°C		118		

(1) Specified by characterization only.

Electrical Characteristics (continued)

For V_S = (V+) – (V–) = 2.7 V to 40 V (±1.35 V to ±20 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

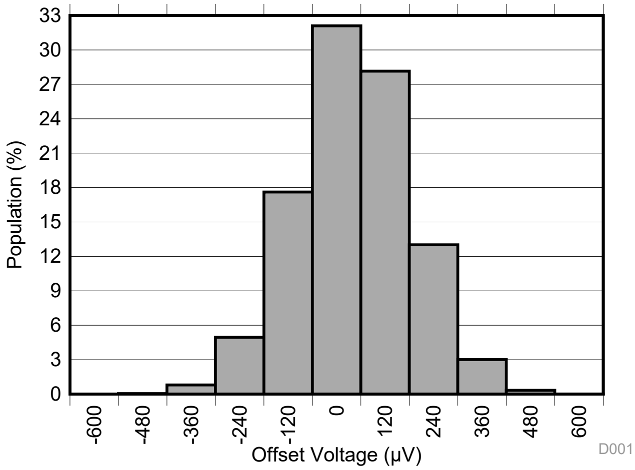
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				4.5		MHz
SR	Slew rate	V_S = 40 V, G = +1, C_L = 20 pF			21		V/µs
t_S	Settling time	To 0.01%, V_S = 40 V, V_{STEP} = 10 V , G = +1, CL = 20 pF			2.5		µs
		To 0.01%, V_S = 40 V, V_{STEP} = 2 V , G = +1, CL = 20 pF			1.5		
		To 0.1%, V_S = 40 V, V_{STEP} = 10 V , G = +1, CL = 20 pF			2		
		To 0.1%, V_S = 40 V, V_{STEP} = 2 V , G = +1, CL = 20 pF			1		
	Phase margin	G = +1, R_L = 10 kΩ			60		°
	Overload recovery time	V_{IN} × gain > V_S			400		ns
THD+N	Total harmonic distortion + noise	V_S = 40 V, V_O = 3 V_{RMS}, G = 1, f = 1 kHz			0.00021%		
OUTPUT							
	Voltage output swing from rail	Positive and negative rail headroom	V_S = 40 V, R_L = no load(1)		5	10	mV
			V_S = 40 V, R_L = 10 kΩ		50	55	
			V_S = 40 V, R_L = 2 kΩ		200	250	
			V_S = 2.7 V, R_L = no load(1)		1	6	
			V_S = 2.7 V, R_L = 10 kΩ		5	12	
			V_S = 2.7 V, R_L = 2 kΩ		25	40	
I_{SC}	Short-circuit current				±75		mA
C_{LOAD}	Capacitive load drive				1000		pF
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A			525		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_{CM} = V–, I_O = 0 A			560	685	µA
			T_A = –40°C to 125°C			750	

表 1. Table of Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	图 1
Offset Voltage Drift Distribution	图 2
Offset Voltage vs Temperature	图 3, 图 4
Offset Voltage vs Common-Mode Voltage	图 5, 图 6, 图 7, 图 8
Offset Voltage vs Power Supply	图 9
Open-Loop Gain and Phase vs Frequency	图 10
Closed-Loop Gain and Phase vs Frequency	图 11
Input Bias Current vs Common-Mode Voltage	图 12
Input Bias Current vs Temperature	图 13
Output Voltage Swing vs Output Current	图 14, 图 15,
CMRR and PSRR vs Frequency	图 16
CMRR vs Temperature	图 17
PSRR vs Temperature	图 18
0.1-Hz to 10-Hz Noise	图 19
Input Voltage Noise Spectral Density vs Frequency	图 20
THD+N Ratio vs Frequency	图 21
THD+N vs Output Amplitude	图 22
Quiescent Current vs Supply Voltage	图 23
Quiescent Current vs Temperature	图 24
Open Loop Voltage Gain vs Temperature	图 25
Open Loop Output Impedance vs Frequency	图 26
Small Signal Overshoot vs Capacitive Load (100-mV Output Step)	图 27, 图 28
Phase Margin vs Capacitive Load	图 29
No Phase Reversal	图 30
Positive Overload Recovery	图 31
Negative Overload Recovery	图 32
Small-Signal Step Response (100 mV)	图 33, 图 34
Large-Signal Step Response	图 35, 图 36, 图 37
Short-Circuit Current vs Temperature	图 38
Maximum Output Voltage vs Frequency	图 39
Channel Separation vs Frequency	图 40
EMIRR vs Frequency	图 41

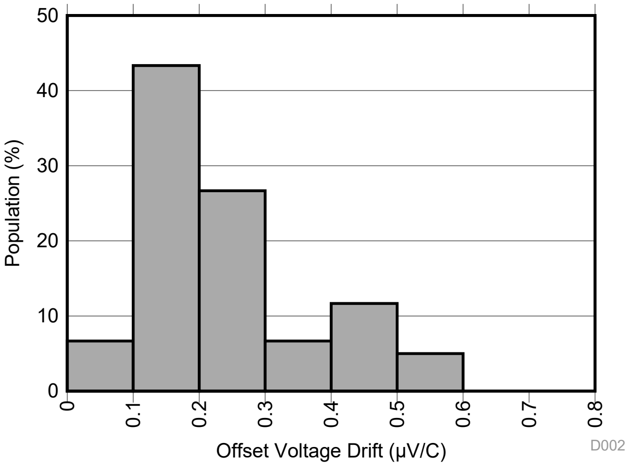
6.8 Typical Characteristics

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)



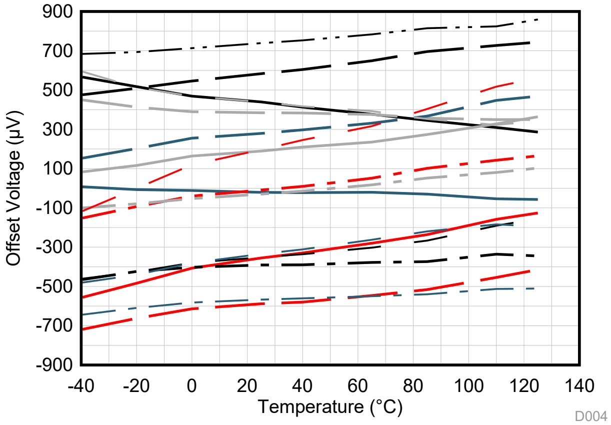
Distribution from 15462 amplifiers, T_A = 25°C

图 1. Offset Voltage Production Distribution



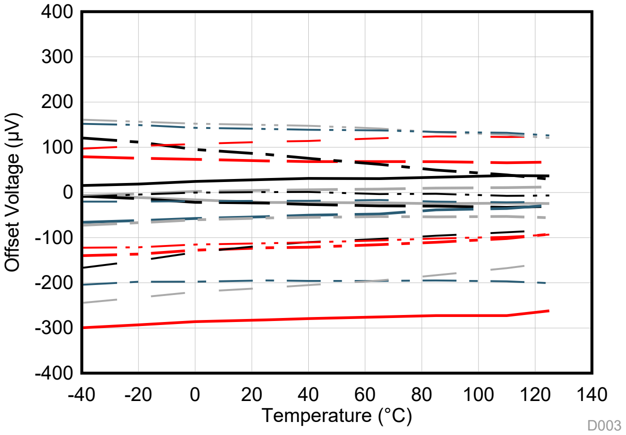
Distribution from 60 amplifiers

图 2. Offset Voltage Drift Distribution



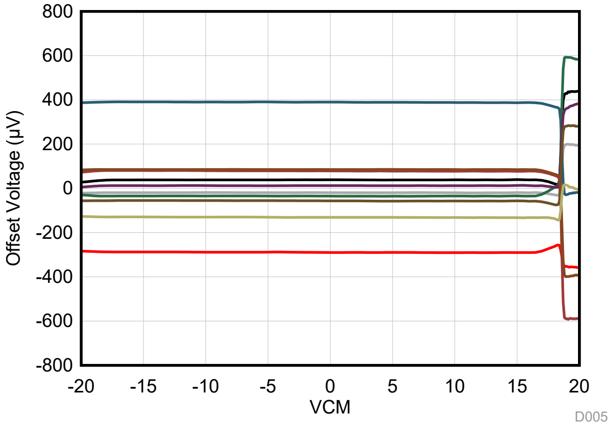
V_{CM} = V+

图 3. Offset Voltage vs Temperature



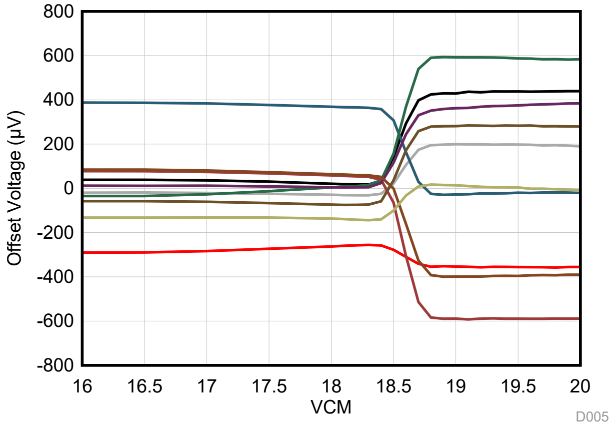
V_{CM} = V–

图 4. Offset Voltage vs Temperature



T_A = 25°C

图 5. Offset Voltage vs Common-Mode Voltage

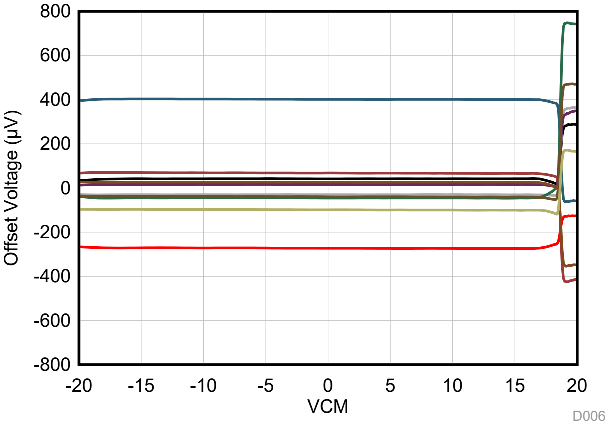


T_A = 25°C

图 6. Offset Voltage vs Common-Mode Voltage (Transition Region)

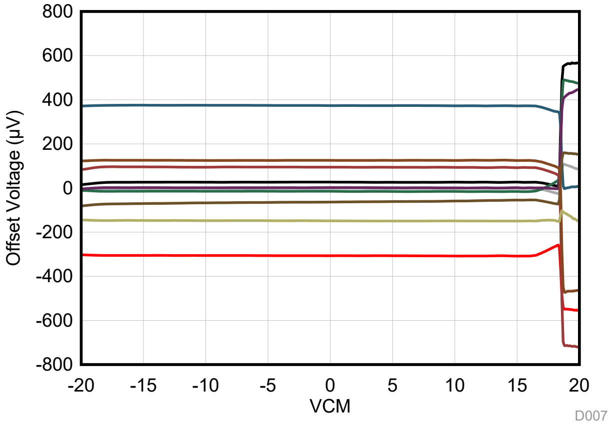
Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)



T_A = 125°C

图 7. Offset Voltage vs Common-Mode Voltage



T_A = –40°C

图 8. Offset Voltage vs Common-Mode Voltage

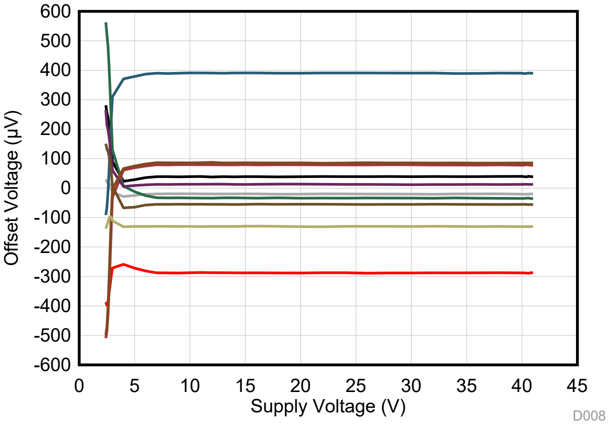
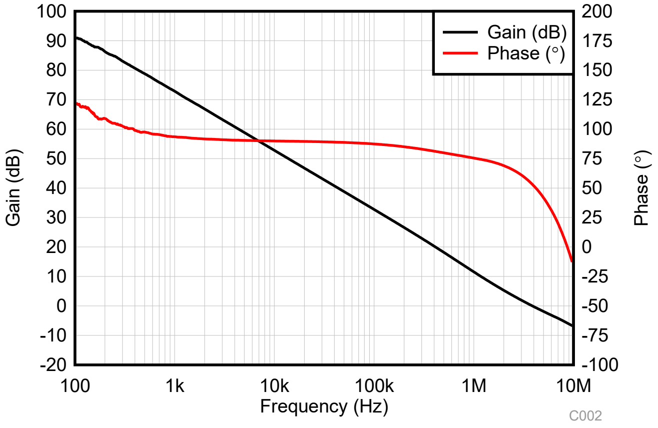


图 9. Offset Voltage vs Power Supply



C_L = 20 pF

图 10. Open-Loop Gain and Phase vs Frequency

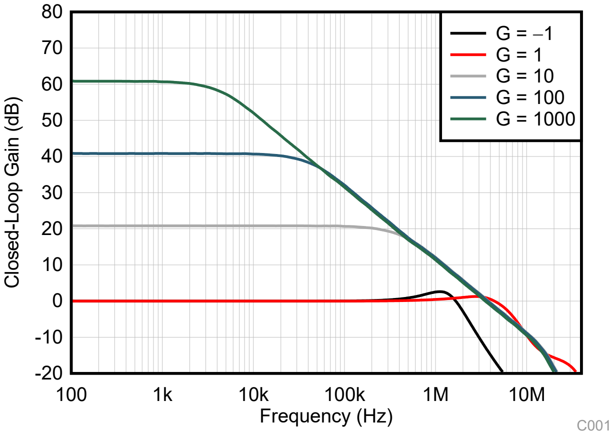


图 11. Closed-Loop Gain vs Frequency

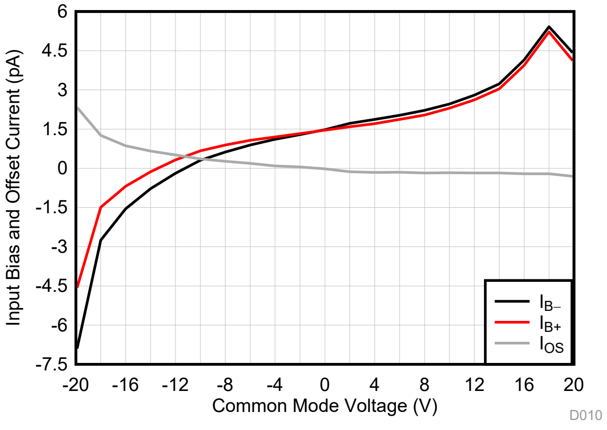


图 12. Input Bias Current vs Common-Mode Voltage

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)

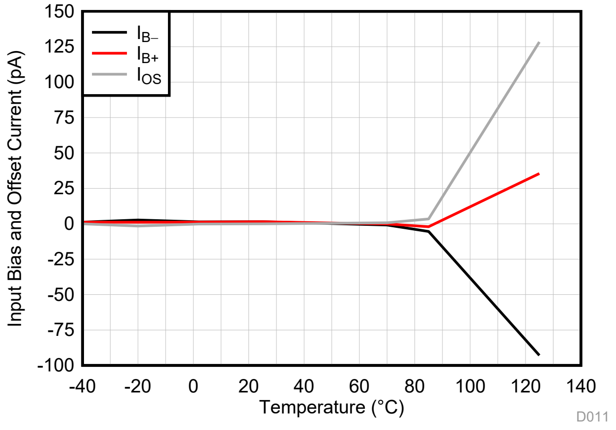


图 13. Input Bias Current vs Temperature

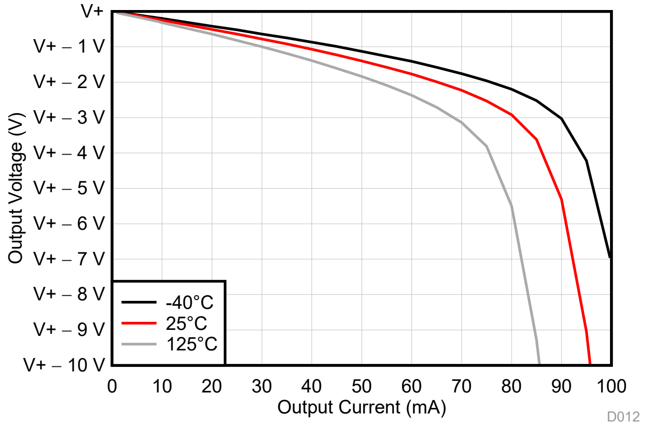


图 14. Output Voltage Swing vs Output Current (Sourcing)

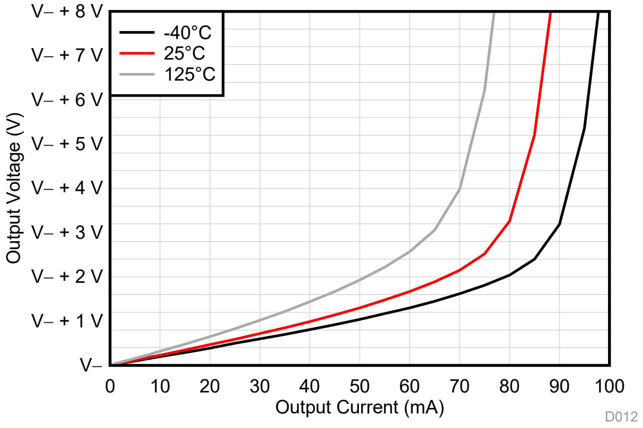


图 15. Output Voltage Swing vs Output Current (Sinking)

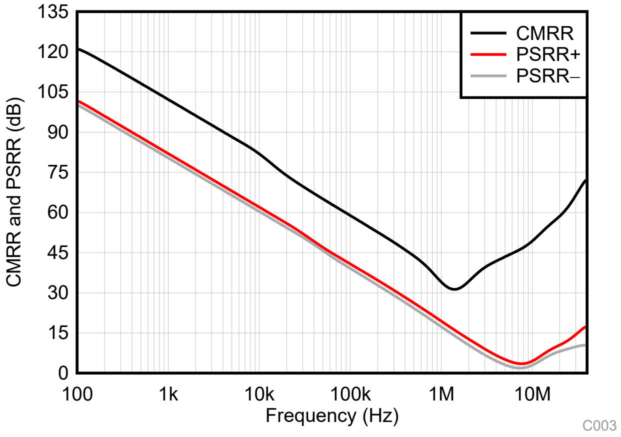
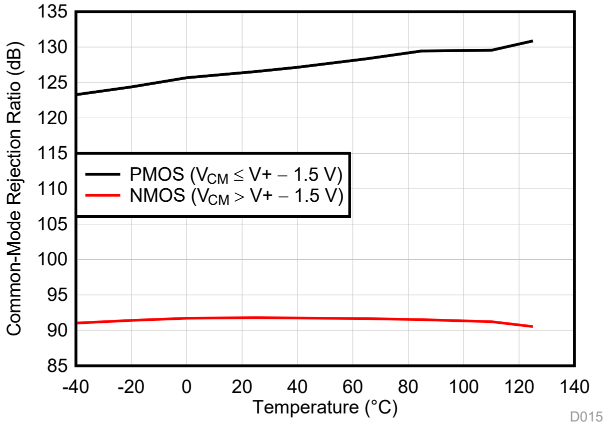
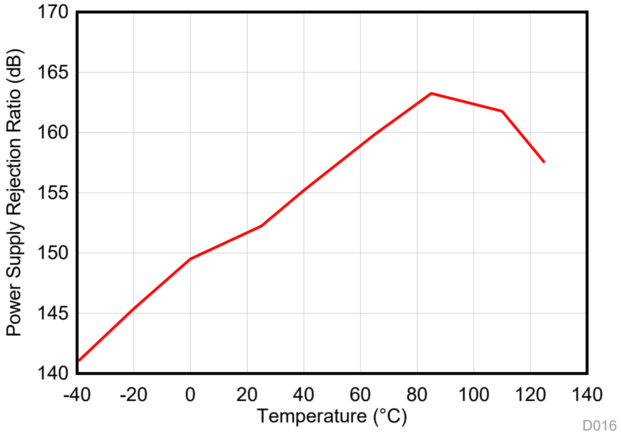


图 16. CMRR and PSRR vs Frequency



f = 0 Hz

图 17. CMRR vs Temperature (dB)



f = 0 Hz

图 18. PSRR vs Temperature (dB)

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)

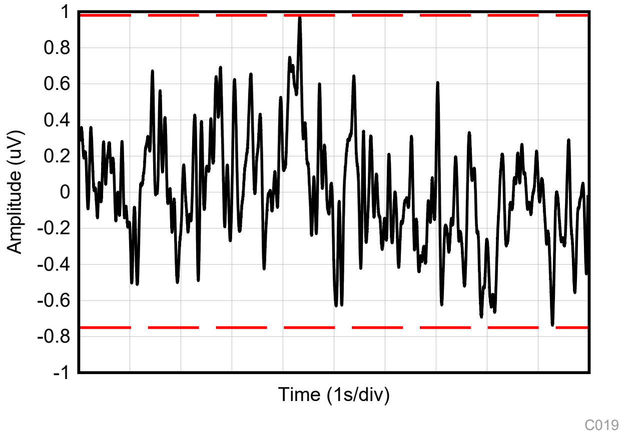


图 19. 0.1-Hz to 10-Hz Noise

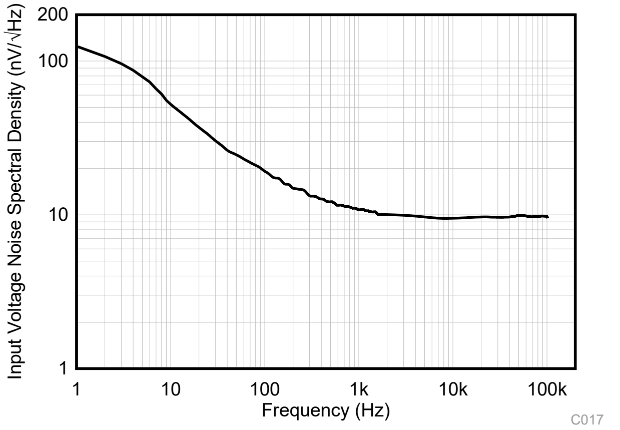
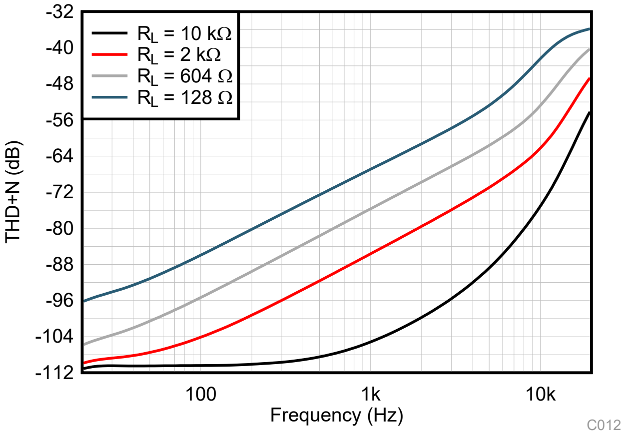
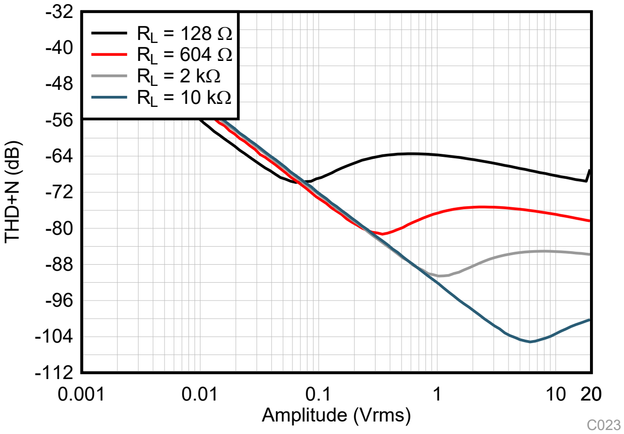


图 20. Input Voltage Noise Spectral Density vs Frequency



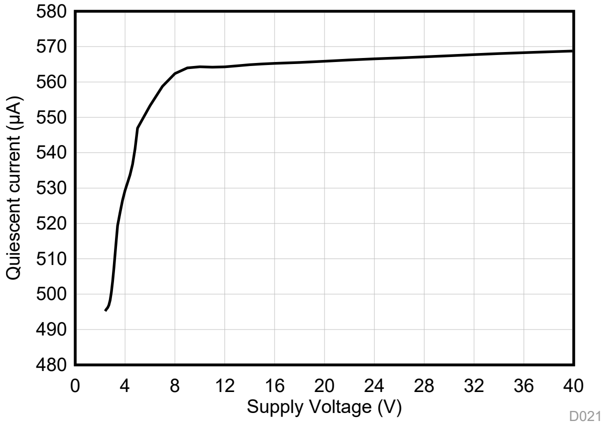
BW = 80 kHz, V_{OUT} = 1 V_{RMS}

图 21. THD+N Ratio vs Frequency



BW = 80 kHz, f = 1 kHz

图 22. THD+N vs Output Amplitude



V_{CM} = V–

图 23. Quiescent Current vs Supply Voltage

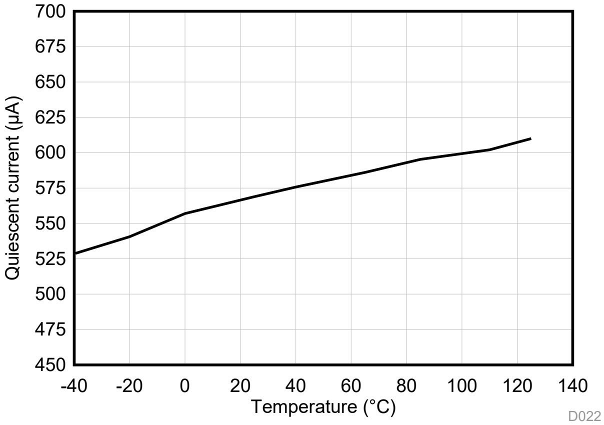


图 24. Quiescent Current vs Temperature

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)

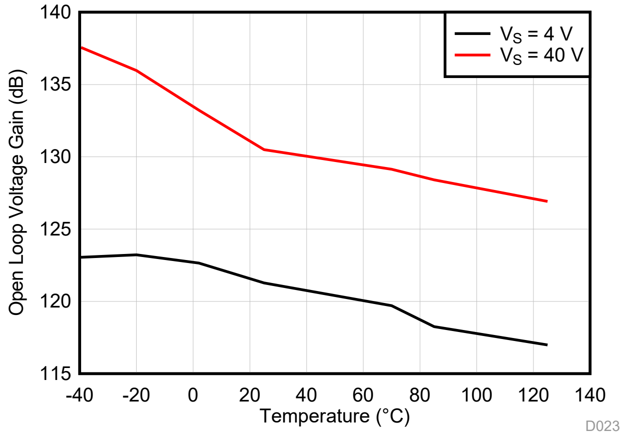


图 25. Open-Loop Voltage Gain vs Temperature (dB)

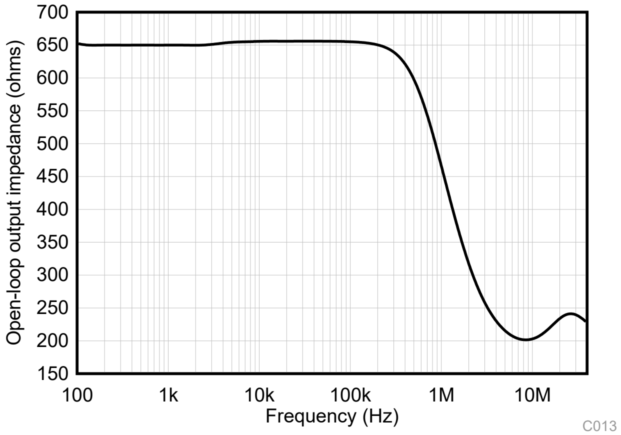
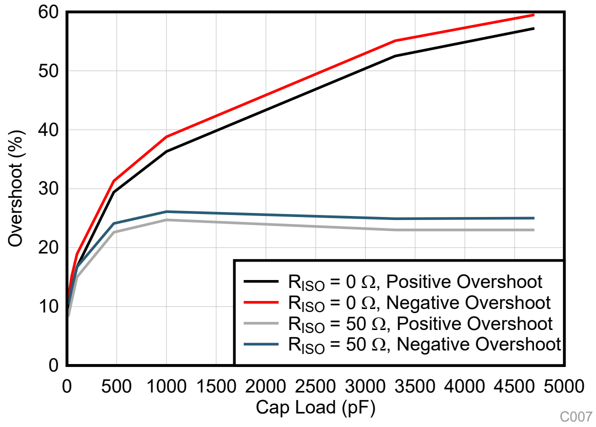
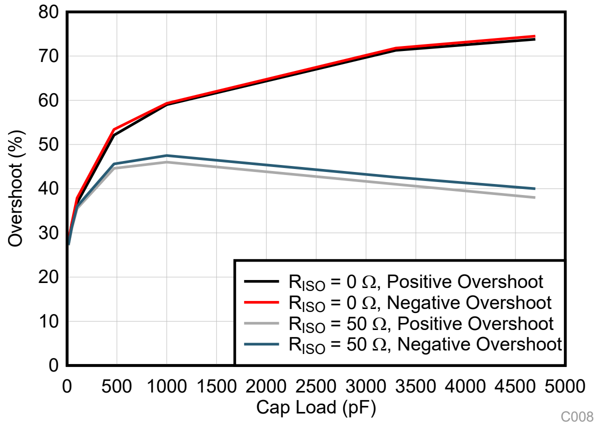


图 26. Open-Loop Output Impedance vs Frequency



G = –1, 10-mV output step

图 27. Small-Signal Overshoot vs Capacitive Load



G = 1, 10-mV output step

图 28. Small-Signal Overshoot vs Capacitive Load

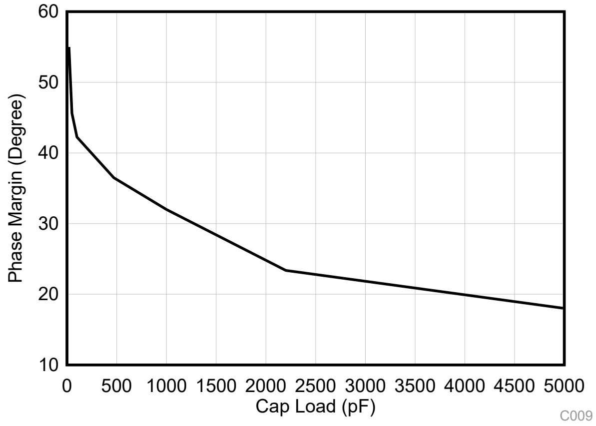
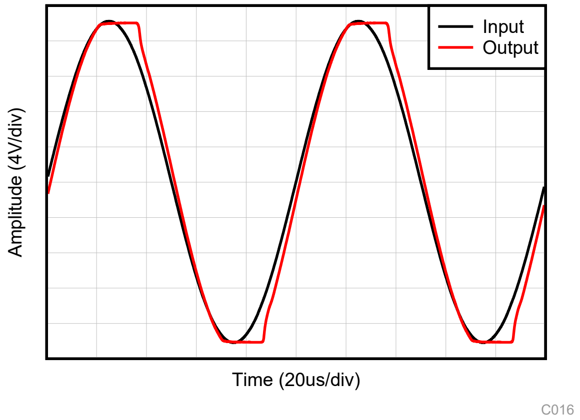


图 29. Phase Margin vs Capacitive Load

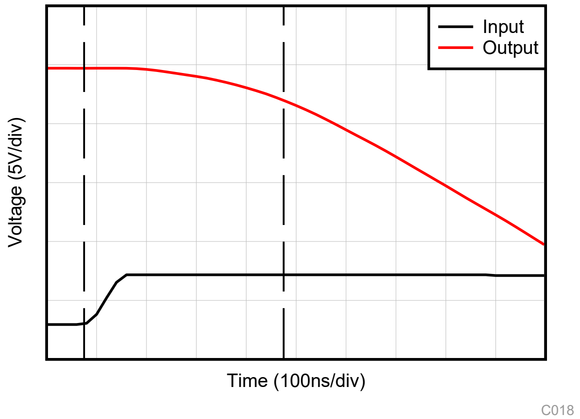


V_{IN} = ±20 V; V_S = V_{OUT} = ±17 V

图 30. No Phase Reversal

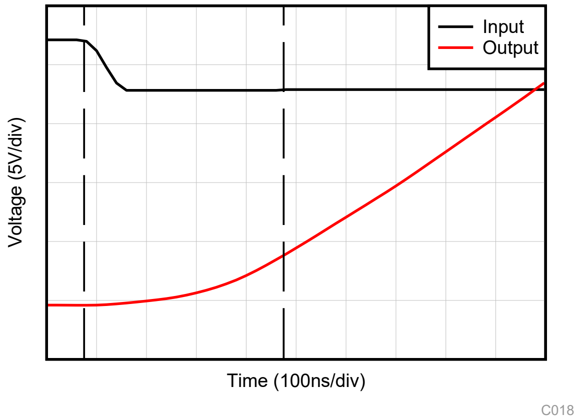
Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)



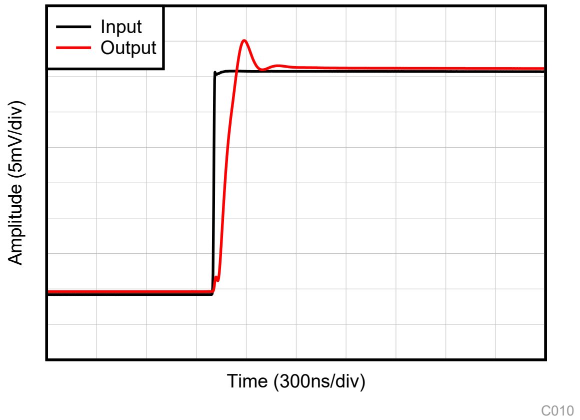
G = –10

图 31. Positive Overload Recovery



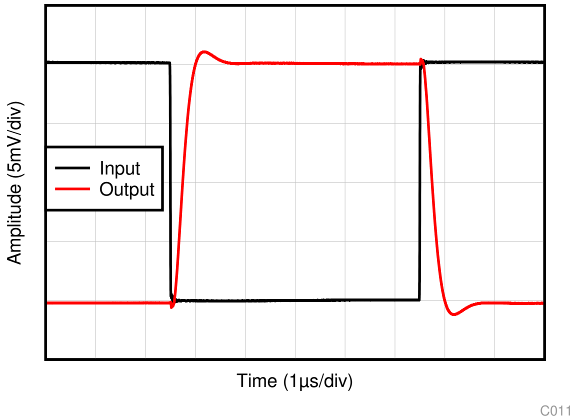
G = –10

图 32. Negative Overload Recovery



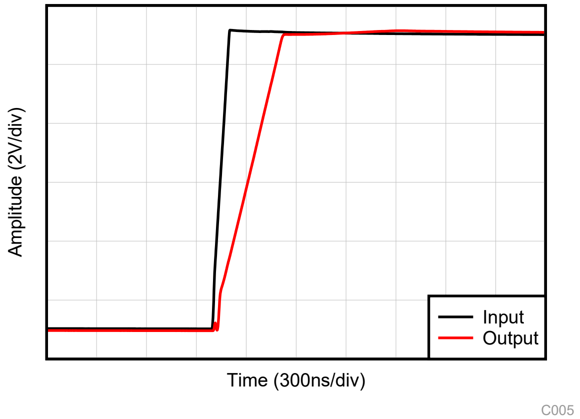
C_L = 20 pF, G = 1, 20-mV step response

图 33. Small-Signal Step Response, Rising



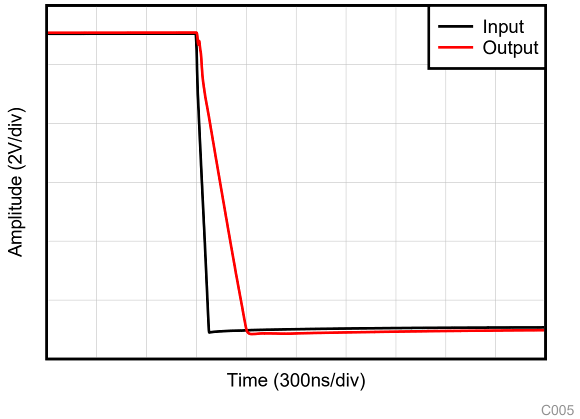
C_L = 20 pF, G = 1, 20-mV step response

图 34. Small-Signal Step Response, Falling



C_L = 20 pF, G = 1

图 35. Large-Signal Step Response (Rising)

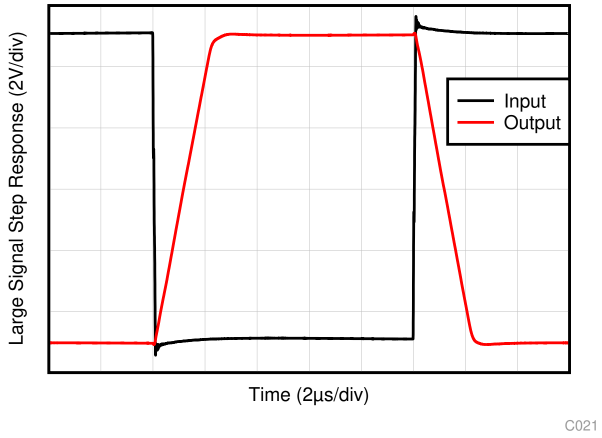


C_L = 20 pF, G = 1

图 36. Large-Signal Step Response (Falling)

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)



C_L = 20 pF, G = –1

图 37. Large-Signal Step Response

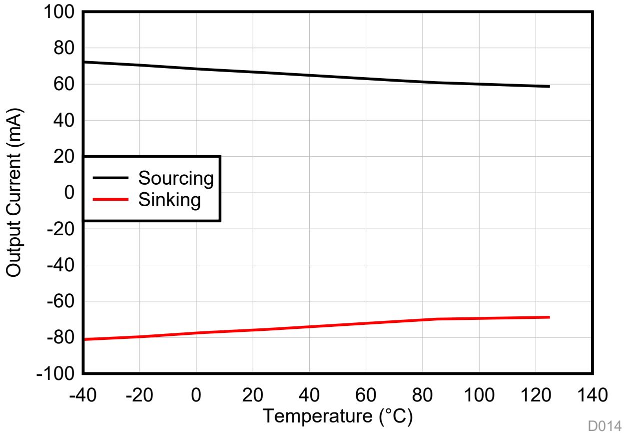


图 38. Short-Circuit Current vs Temperature

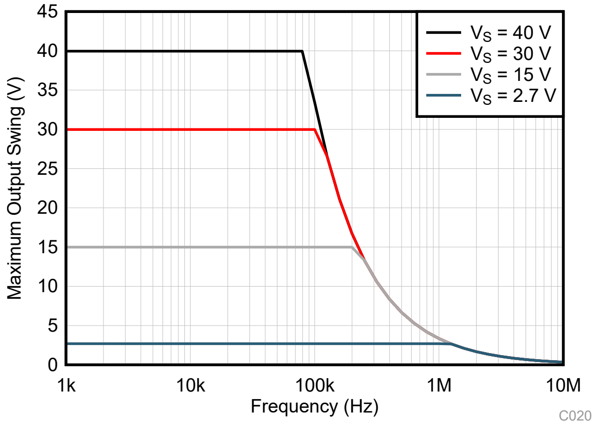


图 39. Maximum Output Voltage vs Frequency

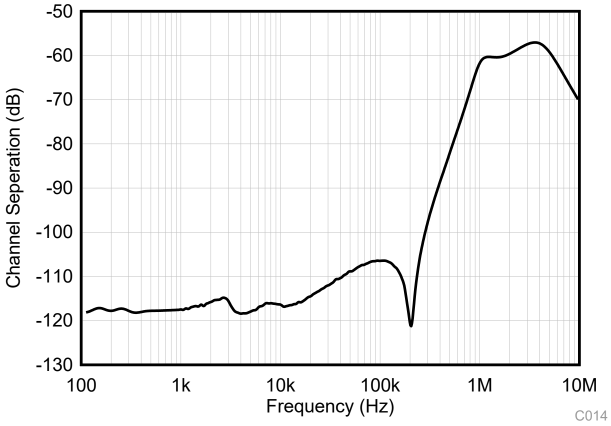


图 40. Channel Separation vs Frequency

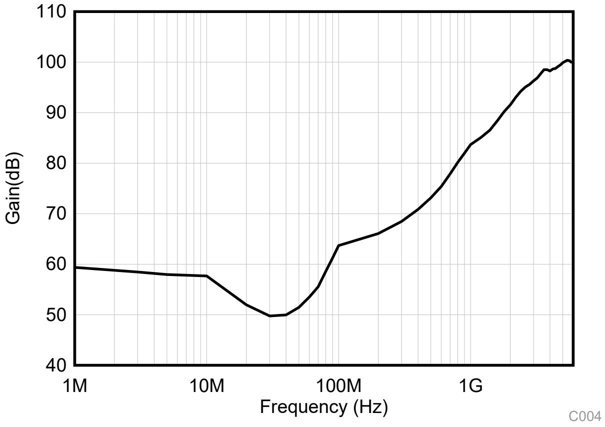


图 41. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

7 Detailed Description

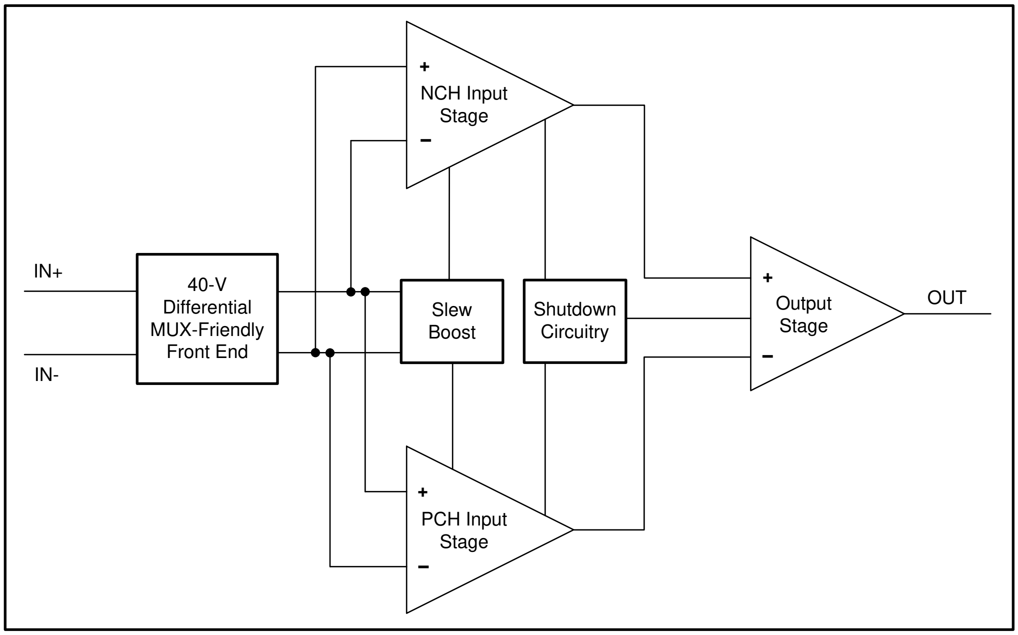
7.1 Overview

The OPAx991 family (OPA991, OPA2991, and OPA4991) is a new generation of 40-V general purpose operational amplifiers.

These devices offer excellent DC precision and AC performance, including rail-to-rail input/output, low offset (±125 µV, typ), low offset drift (±0.3 µV/°C, typ), and 4.5-MHz bandwidth.

Unique features such as differential and common-mode input-voltage range to the supply rail, high output current (±75 mA), high slew rate (21 V/µs), and shutdown functionality make the OPAx991 a robust, high-performance operational amplifier for high-voltage industrial applications.

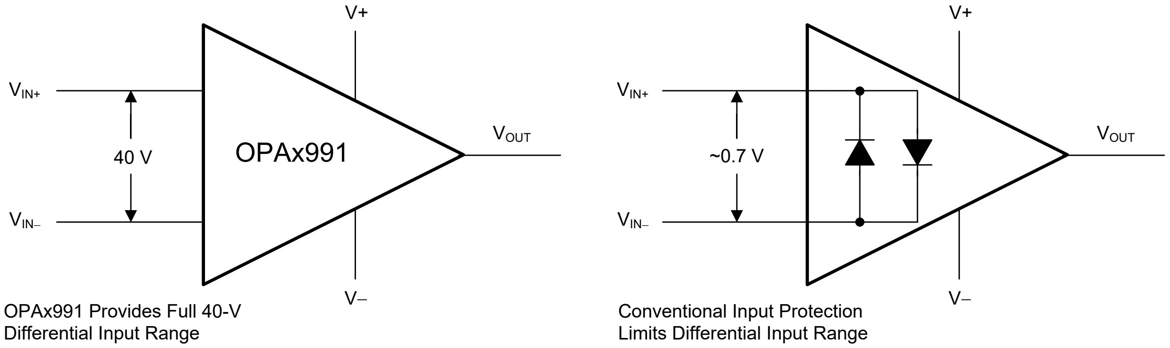
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Protection Circuitry

The OPAx991 uses a unique input architecture to eliminate the requirement for input protection diodes but still provides robust input protection under transient conditions. 图 42 shows conventional input diode protection schemes that are activated by fast transient step responses and introduce signal distortion and settling time delays because of alternate current paths, as shown in 图 43. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current and resulting in extended settling time.



OPAx991 Provides Full 40-V Differential Input Range

Conventional Input Protection Limits Differential Input Range

图 42. OPAx991 Input Protection Does Not Limit Differential Input Capability

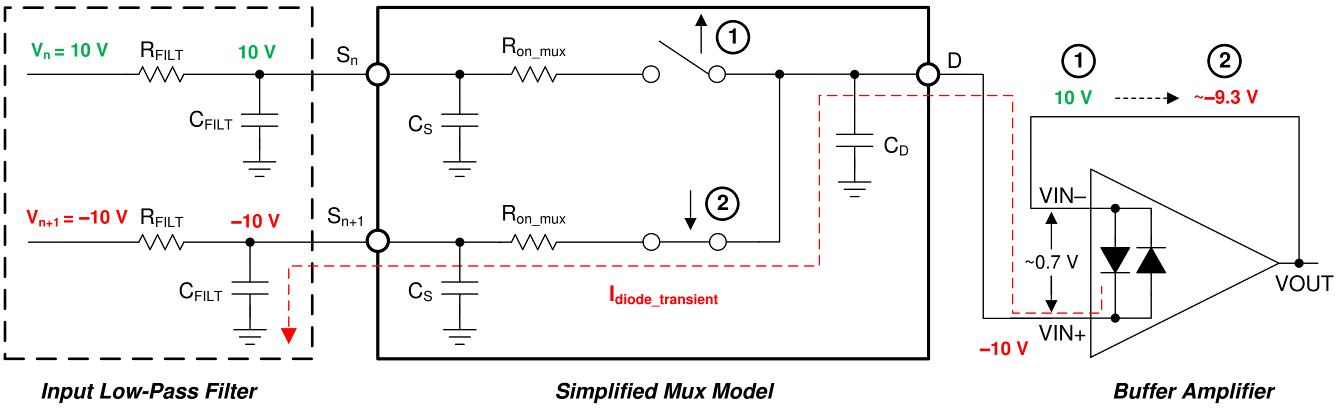


图 43. Back-to-Back Diodes Create Settling Issues

The OPAx991 family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications using a patented input protection architecture that does not introduce additional signal distortion or delayed settling time, making the device an optimal op amp for multichannel, high-switched, input applications. The OPA991 tolerates a maximum differential swing (voltage between inverting and non-inverting pins of the op amp) of up to 40 V, making the device suitable for use as a comparator or in applications with fast-ramping input signals such as data-acquisition systems; see the TI TechNote *MUX-Friendly Precision Operational Amplifiers* for more information.

Feature Description (接下页)

7.3.2 EMI Rejection

The OPAx991 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx991 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 图 44 shows the results of this testing on the OPAx991. 表 2 shows the EMIRR IN+ values for the OPAx991 at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

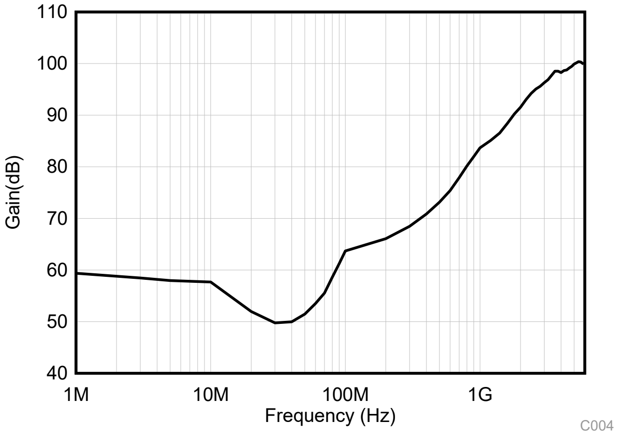


图 44. EMIRR Testing

表 2. OPA991 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	73.2 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	82.5 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	89.7 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	93.9 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	95.7 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	98.0 dB

7.3.3 Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the OPAx991 is 150°C. Exceeding this temperature causes damage to the device. The OPAx991 has a thermal protection feature that reduces damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 170°C. 图 45 shows an application example for the OPA991 that has significant self heating because of its power dissipation (0.81 W). Thermal calculations indicate that for an ambient temperature of 65°C, the device junction temperature must reach 177°C. The actual device, however, turns off the output drive to recover towards a safe junction temperature. 图 45 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3 V. When self heating causes the device junction temperature to increase above the internal limit, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor R_L. If the condition that caused excessive power dissipation is not removed, the amplifier will oscillate between a shutdown and enabled state until the output fault is corrected.

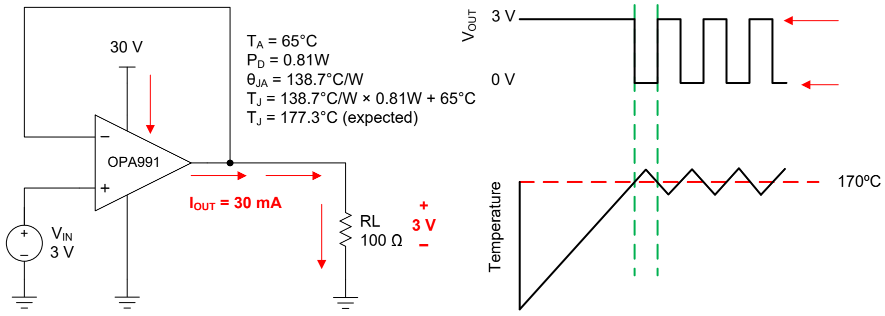


图 45. Thermal Protection

If the device continues to operate at high junction temperatures with high output power over a long period of time, regardless if the device is or is not entering thermal shutdown, the thermal dissipation of the device can slowly degrade performance of the device and eventually cause catastrophic destruction. Designers should be careful to limit output power of the device at high temperatures, or control ambient and junction temperatures under high output power conditions.

7.3.4 Capacitive Load and Stability

The OPAx991 features a resistive output stage capable of driving moderate capacitive loads, and by leveraging an isolation resistor, the device can easily be configured to drive large capacitive loads. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see 图 46 and 图 47. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation.

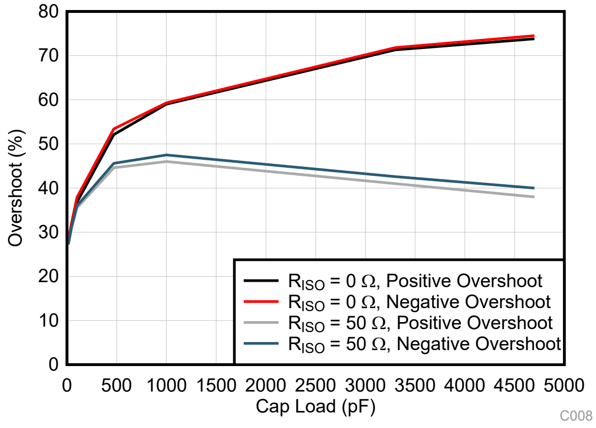


图 46. Small-Signal Overshoot vs Capacitive Load (10-mV Output Step, G = 1)

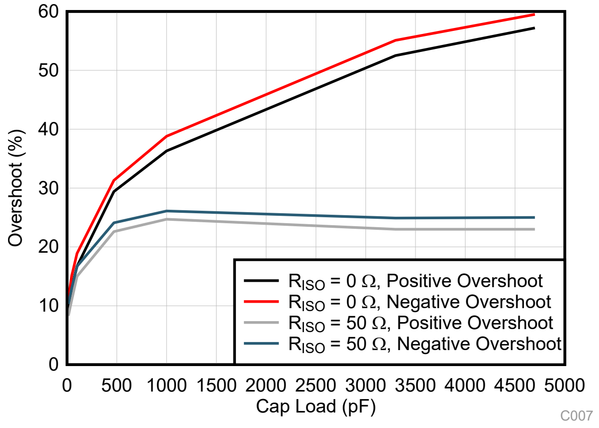


图 47. Small-Signal Overshoot vs Capacitive Load (10-mV Output Step, G = –1)

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small resistor, R_{ISO}, in series with the output, as shown in 图 48. This resistor significantly reduces ringing and maintains DC performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. A high capacitive load drive makes the OPAx991 well suited for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in 图 48 uses an isolation resistor, R_{ISO}, to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin.

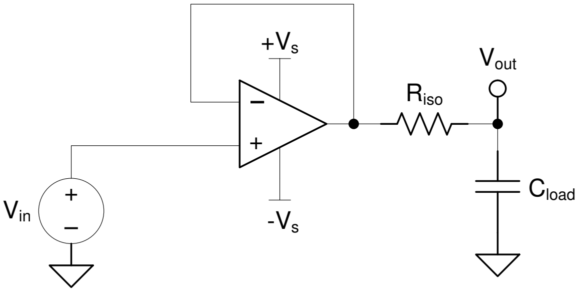


图 48. Extending Capacitive Load Drive With the OPA991

7.3.5 Common-Mode Voltage Range

The OPAx991 is a 40-V, true rail-to-rail input operational amplifier with an input common-mode range that extends 100 mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in 图 49. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1 V to 100 mV above the positive supply. The P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 2 V. There is a small transition region, typically (V+) – 2 V to (V+) – 1 V in which both input pairs are on. This transition region can vary modestly with process variation, and within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance may be degraded compared to operation outside this region.

图 5 shows this transition region for a typical device in terms of input voltage offset in more detail.

For more information on common-mode voltage range and PMOS/NMOS pair interaction, see *Op Amps With Complementary-Pair Input Stages* application note.

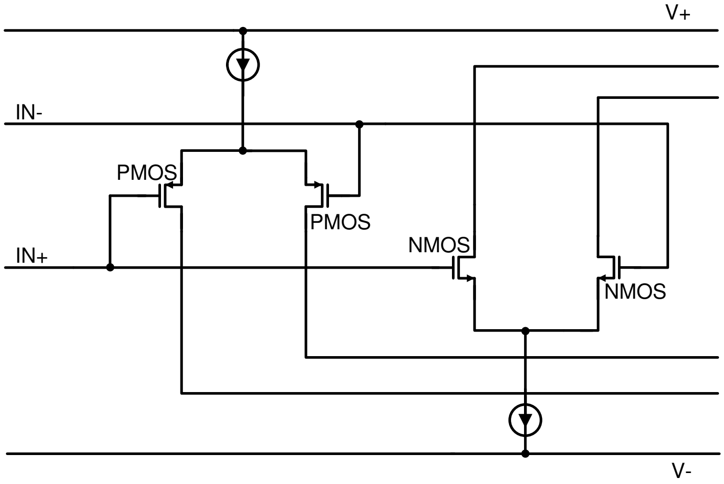


图 49. Rail-to-Rail Input Stage

7.3.6 Phase Reversal Protection

The OPAx991 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in non-inverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx991 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in 图 50. For more information on phase reversal, see *Op Amps With Complementary-Pair Input Stages* application note.

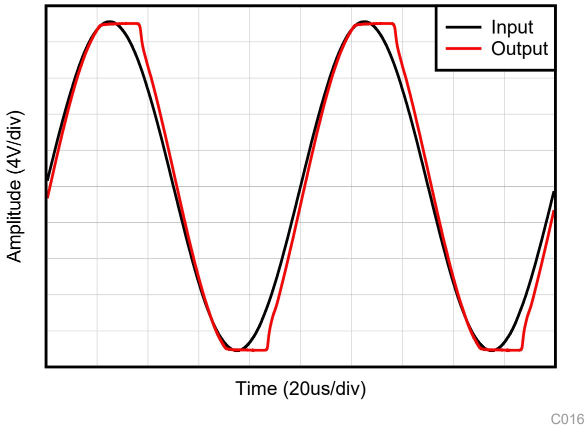


图 50. No Phase Reversal

7.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. 图 51 shows an illustration of the ESD circuits contained in the OPAx991 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

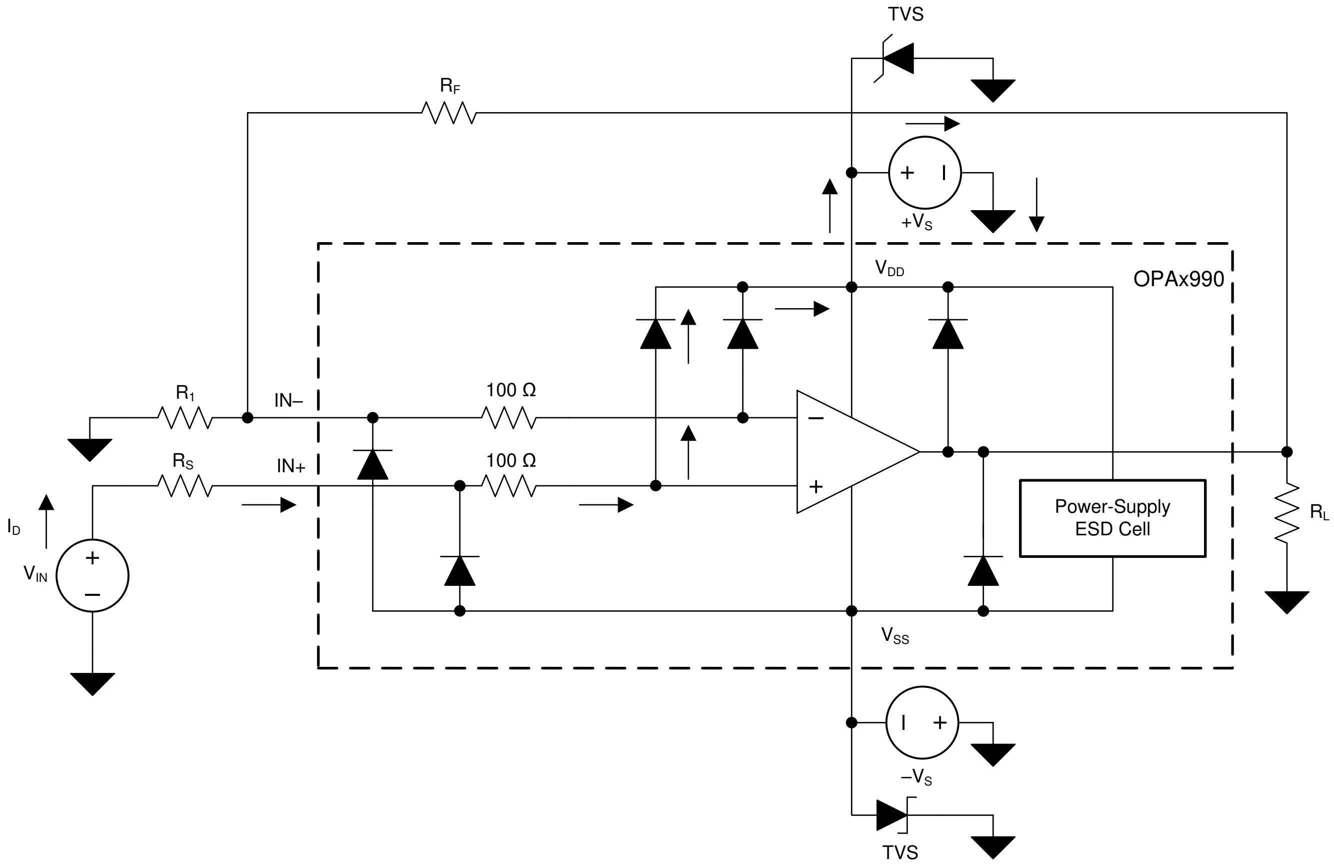


图 51. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example; 1 kV, 100 ns), whereas an EOS event is long duration and lower voltage (for example; 50 V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

7.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx991 is approximately 500 ns.

7.3.9 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier in order to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier will exhibit some amount of deviation from the ideal value, like an amplifier's input offset voltage. These deviations often follow *Gaussian* ("bell curve"), or *normal* distributions, and circuit designers can leverage this information to guardband their system, even when there is not a minimum or maximum specification in the *Electrical Characteristics* table.

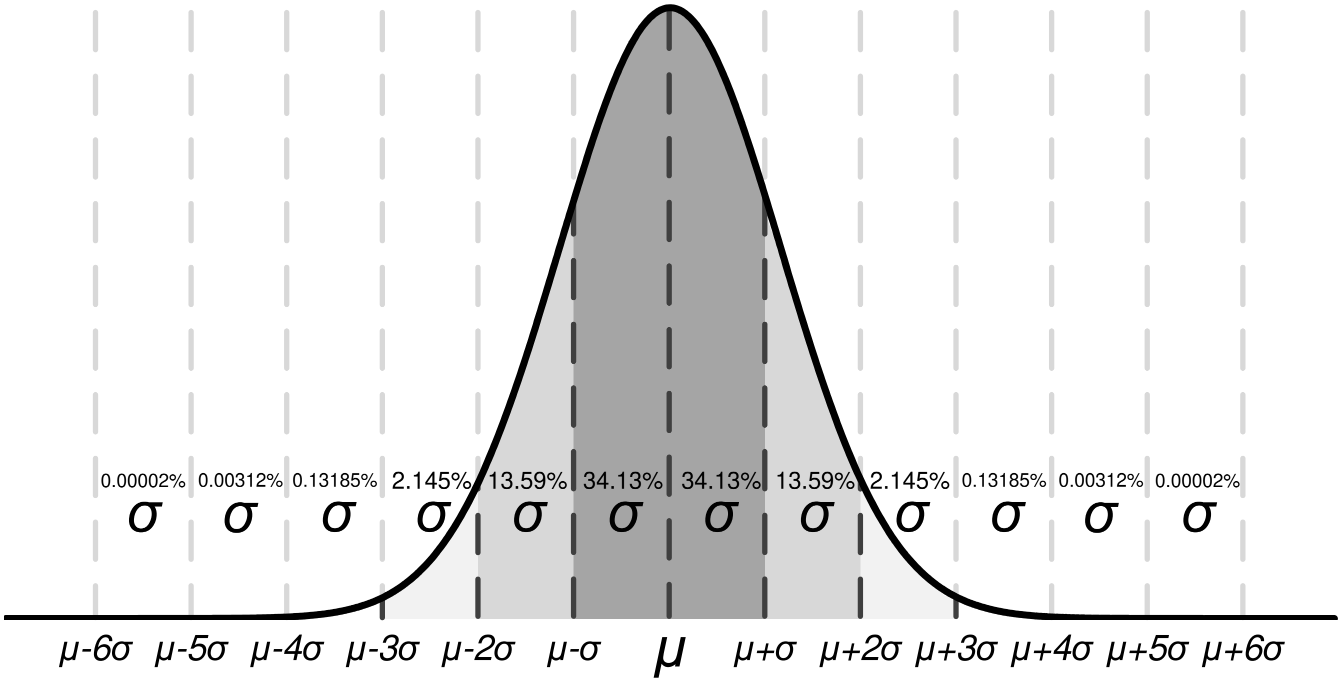


图 52. Ideal Gaussian Distribution

图 52 shows an example distribution, where μ, or *mu*, is the mean of the distribution, and where σ, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from $\mu – \sigma$ to $\mu + \sigma$).

Depending on the specification, values listed in the *typical* column of the *Electrical Characteristics* table are represented in different ways. As a general rule of thumb, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation (μ + σ) in order to most accurately represent the typical value.

You can use this chart to calculate approximate probability of a specification in a unit; for example, for OPAx991, the typical input voltage offset is 125 µV, so 68.2% of all OPAx991 devices are expected to have an offset from –125 µV to 125 µV. At 4 σ (±500 µV), 99.9937% of the distribution has an offset voltage less than ±500 µV, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are assured by TI, and units outside these limits will be removed from production material. For example, the OPAx991 family has a maximum offset voltage of 675 µV at 25°C, and even though this corresponds to about 5 σ (≈1 in 1.7 million units), which is extremely unlikely, TI assures that any unit with larger offset than 675 µV will be removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for your application, and design worst-case conditions using this value. For example, the 6σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and could be an option as a wide guardband to design a system around. In this case, the OPAx991 family does not have a maximum or minimum for offset voltage drift, but based on 图 2 and the typical value of 0.3 µV/°C in the *Electrical Characteristics* table, it can be calculated that the 6-σ value for offset voltage drift is about 1.8 µV/°C. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot assure the performance of a device. This information should be used only to estimate the performance of a device.

7.3.10 Packages With an Exposed Thermal Pad

The OPAx991 family is available in packages such as the WSON-8 (DSG) and WQFN-16 (RTE) which feature an exposed thermal pad. Inside the package, the die is attached to this thermal pad using an electrically conductive compound. For this reason, when using a package with an exposed thermal pad, the thermal pad must either be connected to V– or left floating. Attaching the thermal pad to a potential other than V– is not allowed, and performance of the device is not assured when doing so.

7.3.11 Shutdown

The OPAx991S devices feature one or more shutdown pins (SHDN) that disable the op amp, placing it into a low-power standby mode. In this mode, the op amp typically consumes about 20 µA. The SHDN pins are active high, meaning that shutdown mode is enabled when the input to the SHDN pin is a valid logic high.

The SHDN pins are referenced to the negative supply rail of the op amp. The threshold of the shutdown feature lies around 800 mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to ensure smooth switching characteristics. To ensure optimal shutdown behavior, the SHDN pins should be driven with valid logic signals. A valid logic low is defined as a voltage between V– and V– + 0.4 V. A valid logic high is defined as a voltage between V– + 1.2 V and V– + 20 V. The shutdown pin circuitry includes a pull-down resistor, which will inherently pull the voltage of the pin to the negative supply rail if not driven. Thus, to enable the amplifier, the SHDN pins should either be left floating or driven to a valid logic low. To disable the amplifier, the SHDN pins must be driven to a valid logic high. The maximum voltage allowed at the SHDN pins is V– + 20 V. Exceeding this voltage level will damage the device.

The SHDN pins are high-impedance CMOS inputs. Channels of single and dual op amp packages are independently controlled, and channels of quad op amp packages are controlled in pairs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The typical enable time out of shutdown is 30 µs; disable time is 3 µs. When disabled, the output assumes a high-impedance state. This architecture allows the OPAx991S family to operate as a gated amplifier, multiplexer, or programmable-gain amplifier. Shutdown time (t_{OFF}) depends on loading conditions and increases as load resistance increases. To ensure shutdown (disable) within a specific shutdown time, the specified 10-kΩ load to midsupply (V_S / 2) is required. If using the OPAx991S without a load, the resulting turnoff time significantly increases.

7.4 Device Functional Modes

The OPAx991 has a single functional mode and is operational when the power-supply voltage is greater than 2.7 V (±1.35 V). The maximum power supply voltage for the OPAx991 is 40 V (±20 V).

The OPAx991S devices feature a shutdown pin, which can be used to place the op amp into a low-power mode. See *Shutdown* section for more information.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx991 family offers excellent DC precision and AC performance. These devices operate up to 40-V supply rails and offer true rail-to-rail input/output, low offset voltage and offset voltage drift, as well as 4.5-MHz bandwidth and high output drive. These features make the OPAx991 a robust, high-performance operational amplifier for high-voltage industrial applications.

8.2 Typical Applications

8.2.1 Low-Side Current Measurement

图 53 shows the OPA991 configured in a low-side current sensing application. For a full analysis of the circuit shown in 图 53 including theory, calculations, simulations, and measured data, see TI Precision Design TIPD129, *0-A to 1-A Single-Supply Low-Side Current-Sensing Solution*.

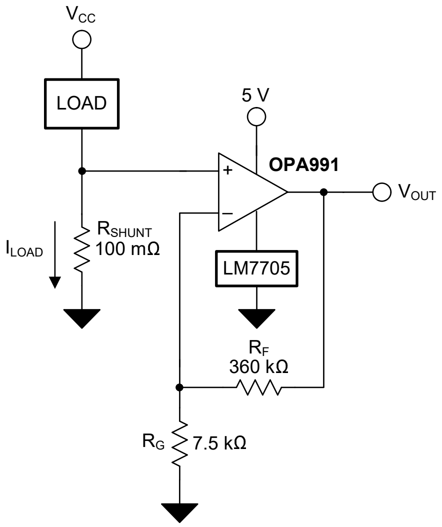


图 53. OPA991 in a Low-Side, Current-Sensing Application

8.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.9 V
- Maximum shunt voltage: 100 mV

Typical Applications (接下页)

8.2.1.2 Detailed Design Procedure

The transfer function of the circuit in 图 53 is given in 公式 1:

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using 公式 2:

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100mV}{1A} = 100m\Omega \quad (2)$$

Using 公式 2, R_{SHUNT} is calculated to be 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the OPA991 to produce an output voltage of 0 V to 4.9 V. The gain needed by the OPA991 to produce the necessary output voltage is calculated using 公式 3:

$$Gain = \frac{\left(V_{OUT\_MAX} - V_{OUT\_MIN}\right)}{\left(V_{IN\_MAX} - V_{IN\_MIN}\right)} \quad (3)$$

Using 公式 3, the required gain is calculated to be 49 V/V, which is set with resistors R_F and R_G. 公式 4 is used to size the resistors, R_F and R_G, to set the gain of the OPA991 to 49 V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Choosing R_F as 360 kΩ, R_G is calculated to be 7.5 kΩ. R_F and R_G were chosen as 360 kΩ and 7.5 kΩ because they are standard value resistors that create a 49:1 ratio. Other resistors that create a 49:1 ratio can also be used. 图 54 shows the measured transfer function of the circuit shown in 图 53.

8.2.1.3 Application Curves

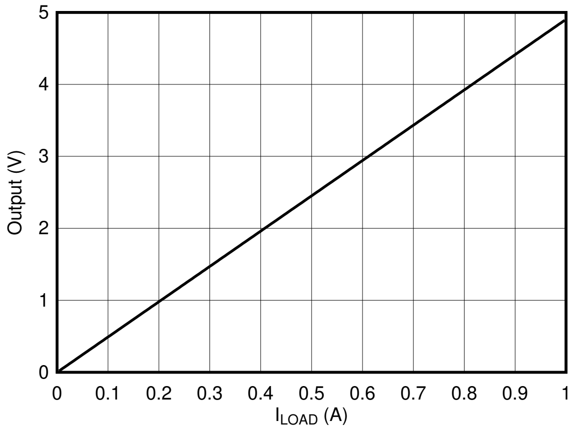


图 54. Low-Side, Current-Sense, Transfer Function

9 Power Supply Recommendations

The OPAx991 is specified for operation from 2.7 V to 40 V (±1.35 V to ±40 V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in 图 56, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

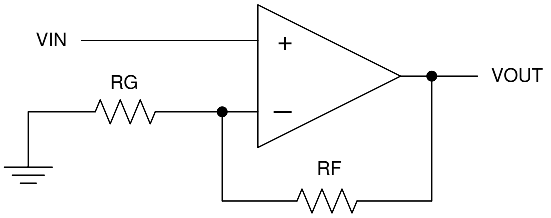


图 55. Schematic Representation

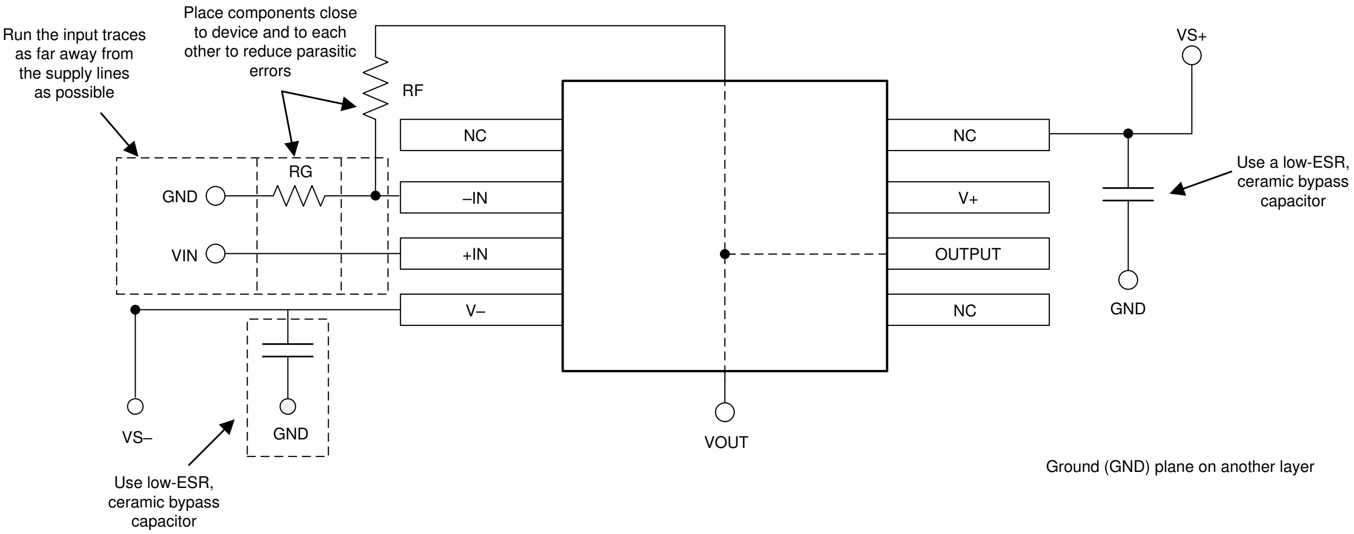


图 56. Operational Amplifier Board Layout for Noninverting Configuration

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 TINA-TI™（免费软件下载）

TINA™是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。TINA-TI 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI 可从 Analog eLab Design Center（模拟电子实验室设计中心）免费下载，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。虚拟仪器提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

注

这些文件需要安装 TINA 软件（由 DesignSoft™提供）或者 TINA-TI 软件。请从 TINA-TI 文件夹 中下载免费的 TINA-TI 软件。

11.1.1.2 TI 高精度设计

OPAx991 采用多种 TI 高精度设计，有关内容可通过 http://www.ti.com.cn/ww/analog/precision-designs/ 在线获取。TI 高精度设计是由 TI 公司高精度模拟 应用 专家创建的模拟解决方案，提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

德州仪器 (TI)，*《模拟工程师电路设计指导手册：放大器》* 解决方案指南

德州仪器 (TI)，*《AN31 放大器电路集合》* 应用手册

德州仪器 (TI)，*《支持多路复用器的精密运算放大器》* 技术手册

德州仪器 (TI)，*《运算放大器的 EMI 抑制比》* 应用报告

德州仪器 (TI)，*《具有互补对输入级的运算放大器》* 应用手册

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 商标

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TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2991IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O91F	Samples
OPA2991IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	26UT	Samples
OPA2991IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OP2991	Samples
OPA2991IDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O91G	Samples
OPA2991IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2991P	Samples
OPA2991SIRUGR	ACTIVE	X2QFN	RUG	10	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	GFF	Samples
OPA4991IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA4991D	Samples
OPA4991IDYYR	ACTIVE	SOT-23-THIN	DYY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA4991I	Samples
OPA4991IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	OP4991PW	Samples
OPA4991IRUCR	ACTIVE	QFN	RUC	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I4F	Samples
OPA991IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O91V	Samples
OPA991IDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1HB	Samples
OPA991SIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O91S	Samples
OPA991TIDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1JE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2991, OPA4991, OPA991 :

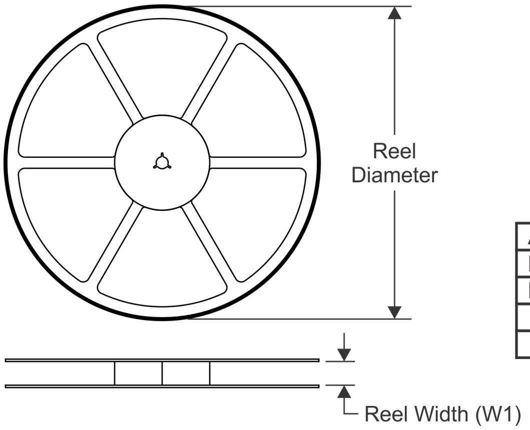
- Automotive : OPA2991-Q1, OPA4991-Q1, OPA991-Q1

NOTE: Qualified Version Definitions:

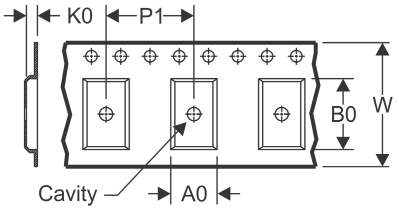
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

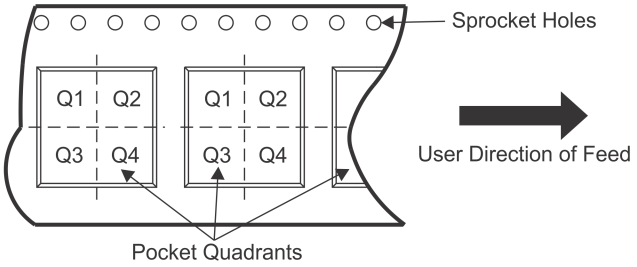


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

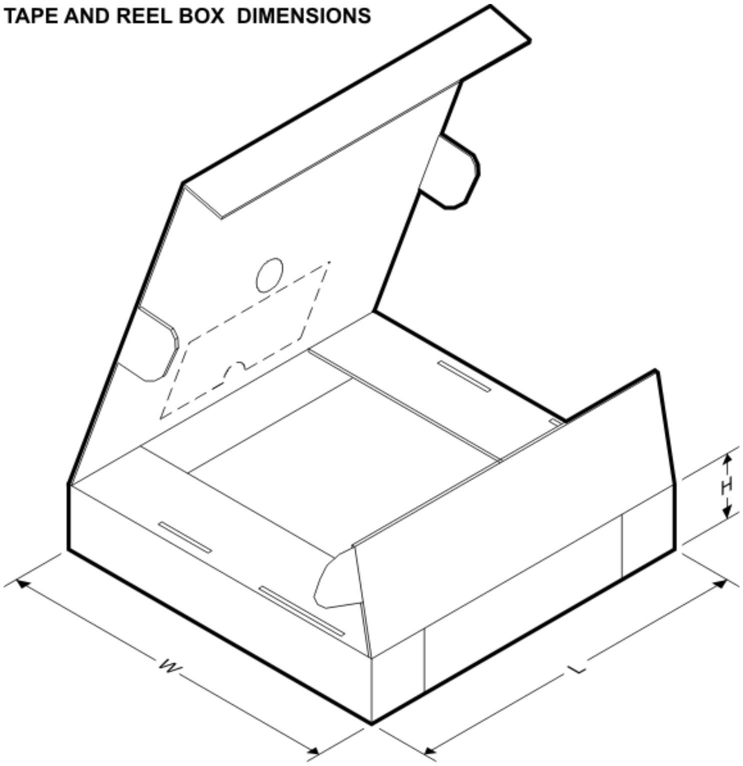
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2991IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA2991IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2991IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2991IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA2991IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
OPA2991SIRUGR	X2QFN	RUG	10	3000	178.0	8.4	1.75	2.25	0.56	4.0	8.0	Q1
OPA4991IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4991IDYYR	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
OPA4991IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4991IRUCR	QFN	RUC	14	3000	180.0	9.5	2.16	2.16	0.5	4.0	8.0	Q2
OPA991IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA991IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA991SIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA991TIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

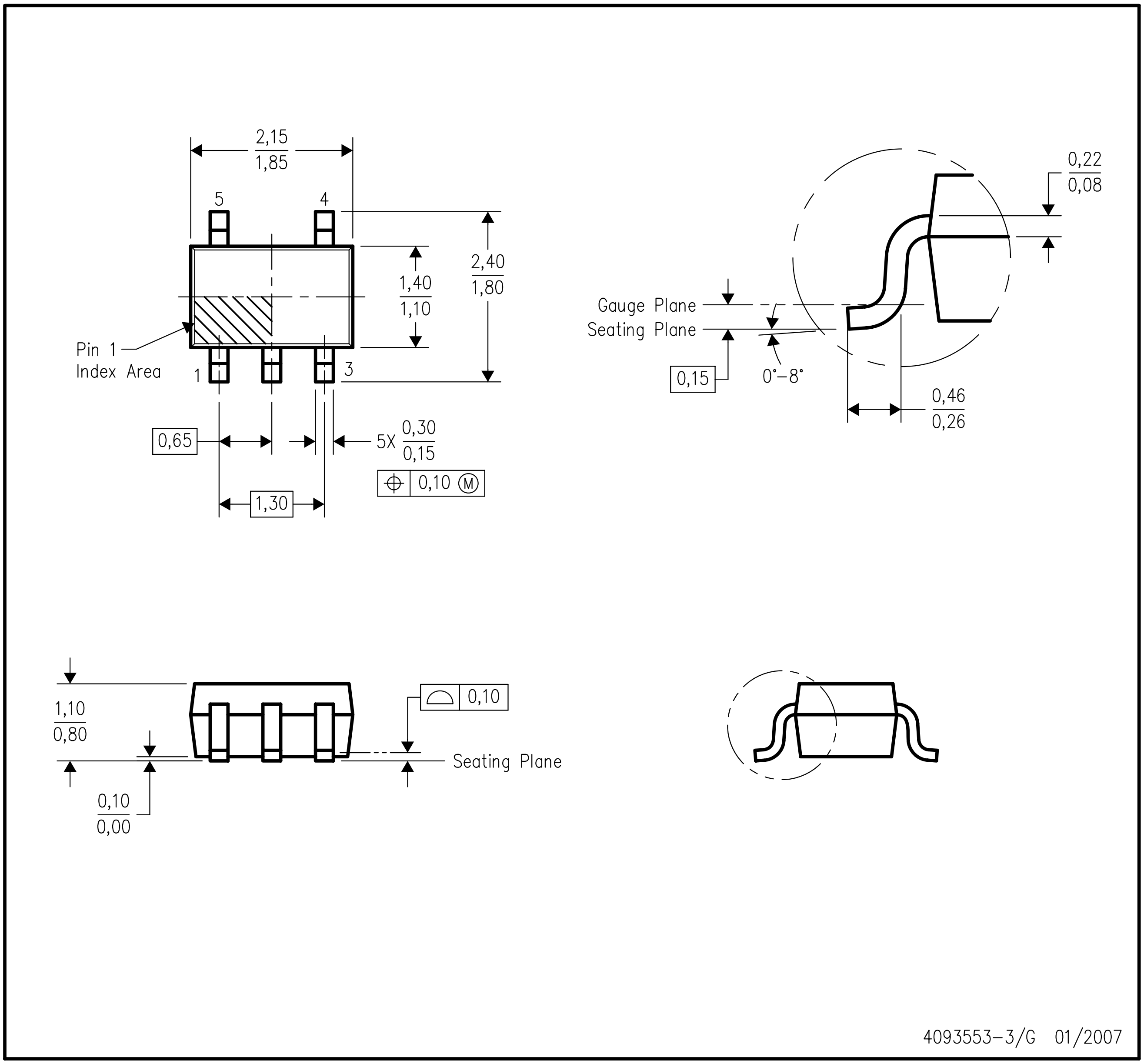
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

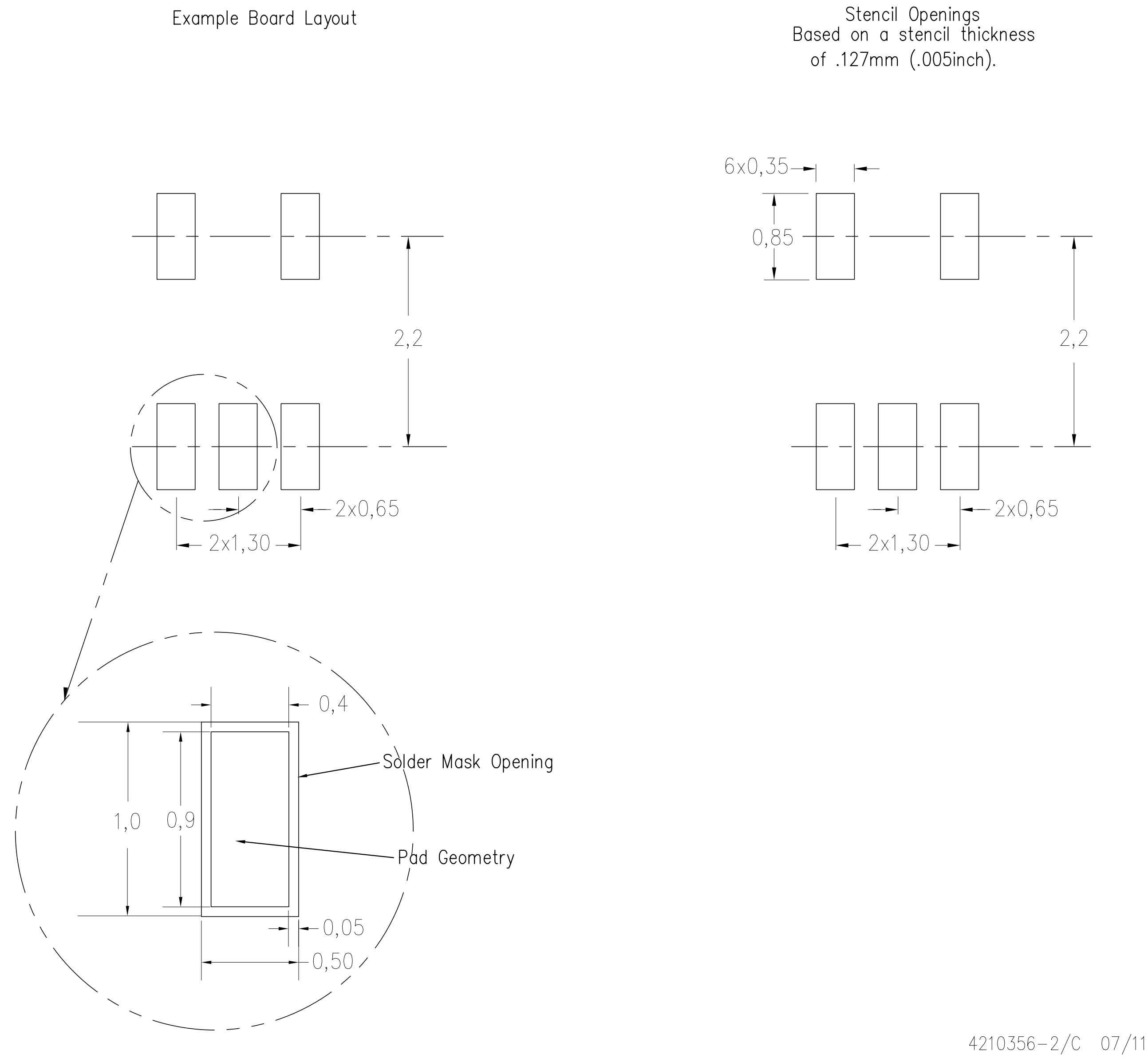
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2991IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
OPA2991IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2991IDR	SOIC	D	8	2500	853.0	449.0	35.0
OPA2991IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
OPA2991IPWR	TSSOP	PW	8	2000	853.0	449.0	35.0
OPA2991SIRUGR	X2QFN	RUG	10	3000	205.0	200.0	33.0
OPA4991IDR	SOIC	D	14	2500	853.0	449.0	35.0
OPA4991IDYYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
OPA4991IPWR	TSSOP	PW	14	2000	366.0	364.0	50.0
OPA4991IRUCR	QFN	RUC	14	3000	205.0	200.0	30.0
OPA991IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA991IDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
OPA991SIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
OPA991TIDCKR	SC70	DCK	5	3000	190.0	190.0	30.0

DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



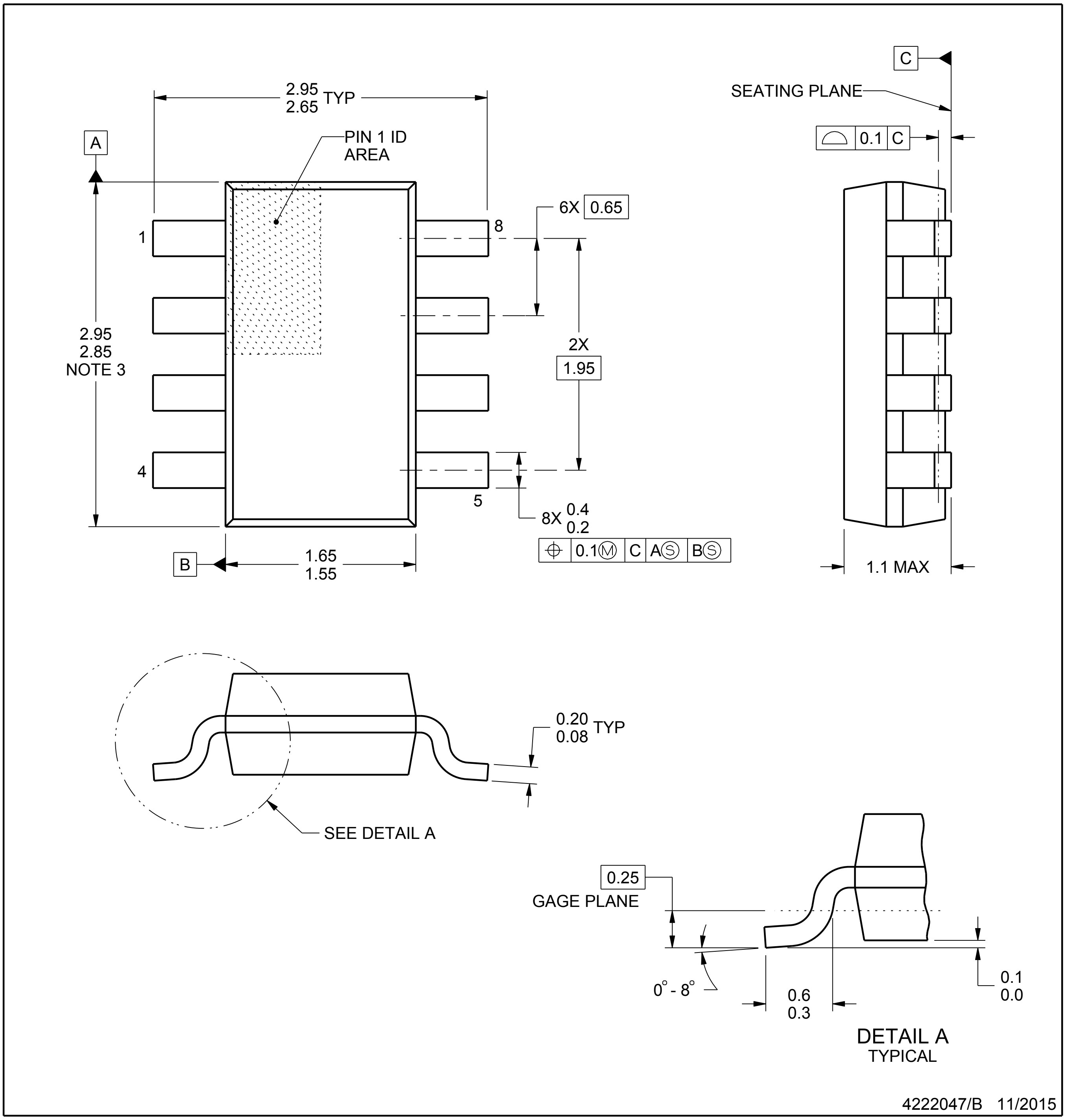
4210356–2/C 07/11

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DDF0008A

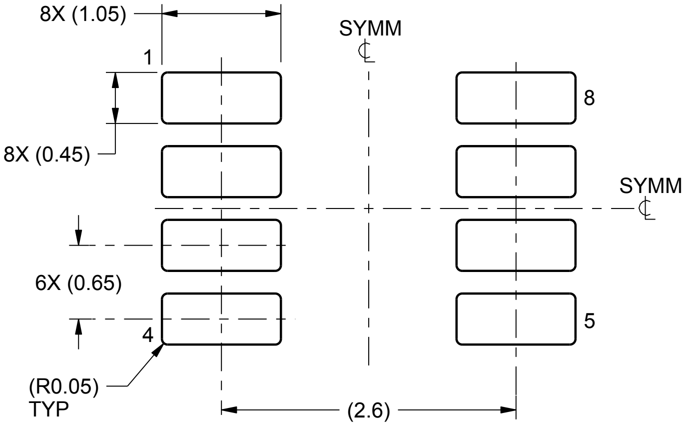
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE

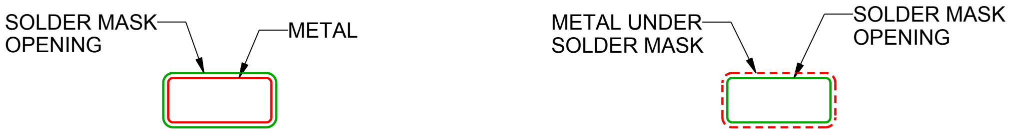


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

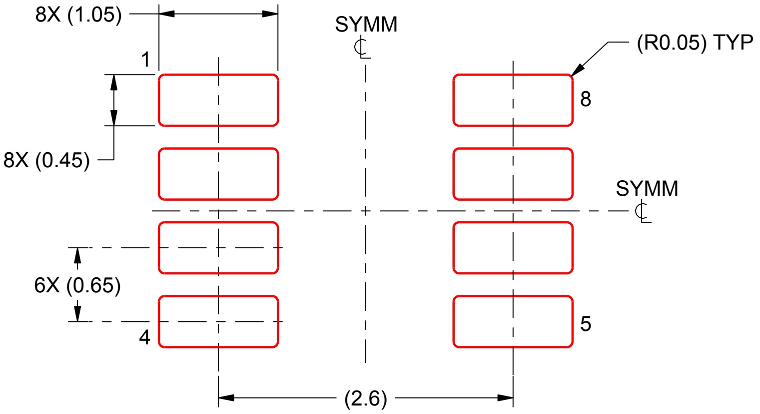
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

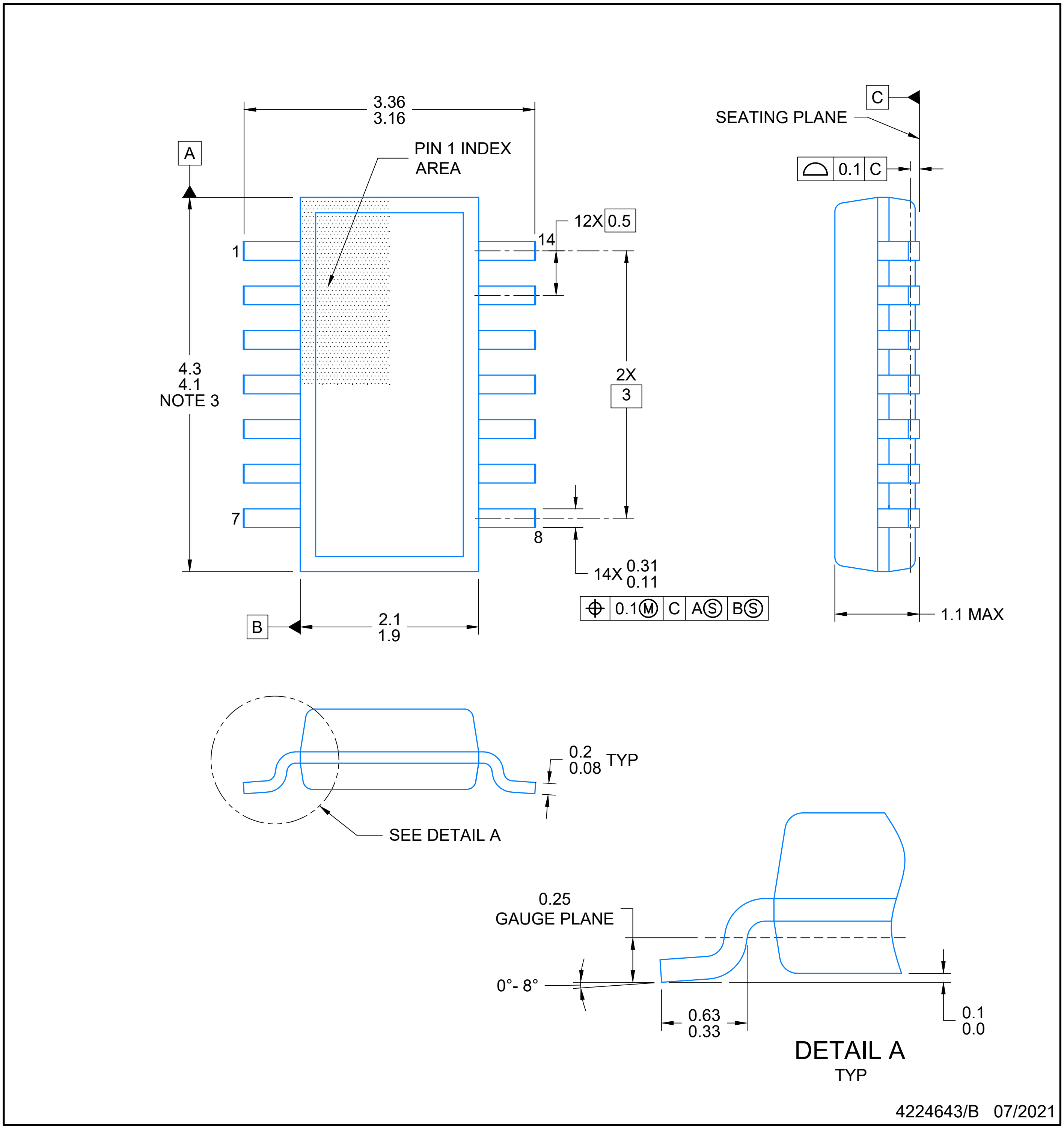


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

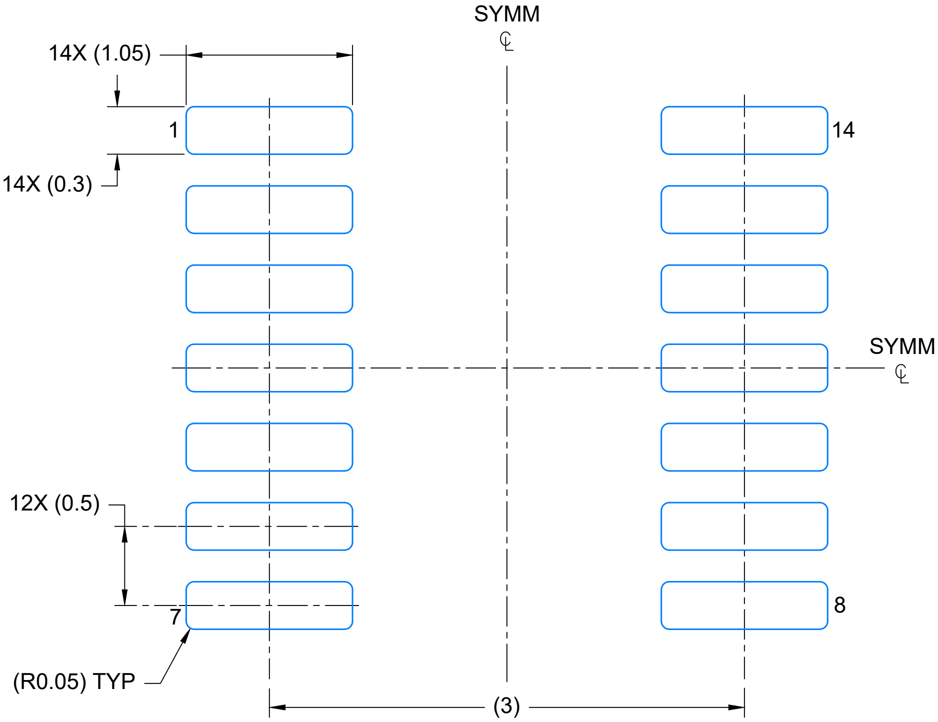
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

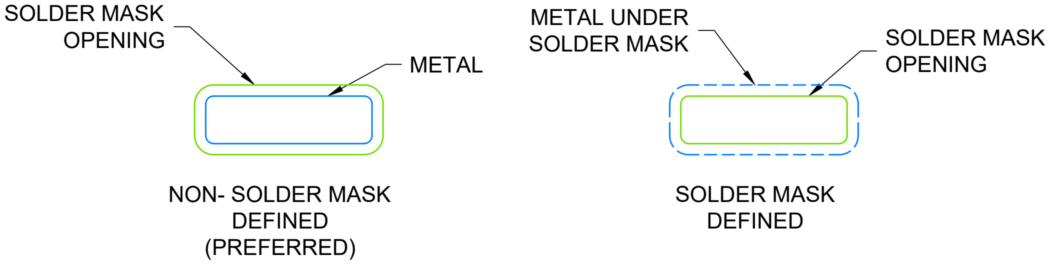


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

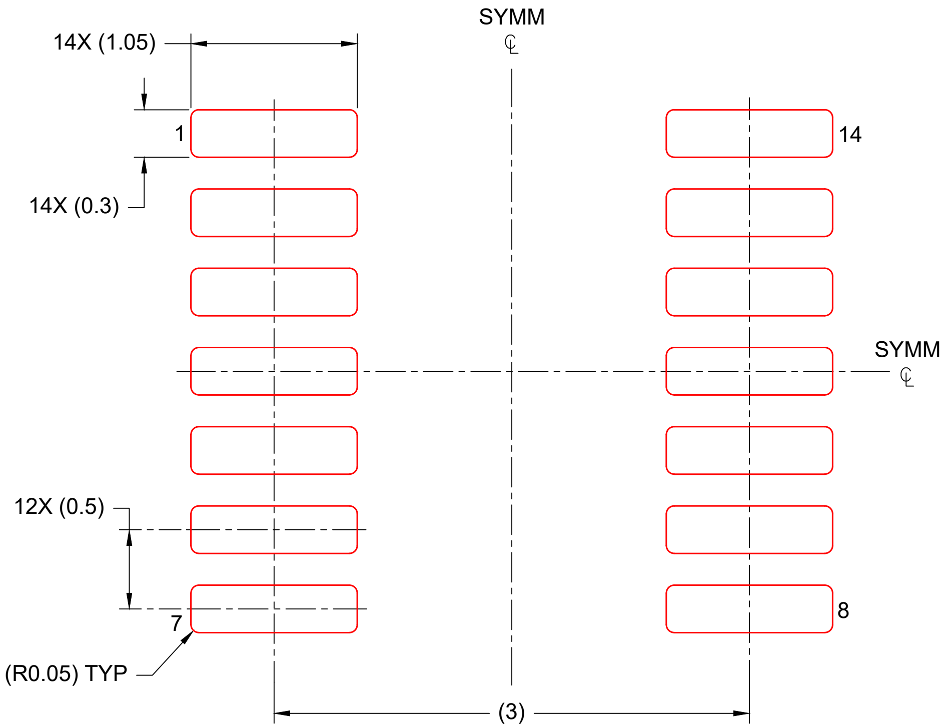


SOLDER MASK DETAILS

4224643/B 07/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

NOTES: (continued)

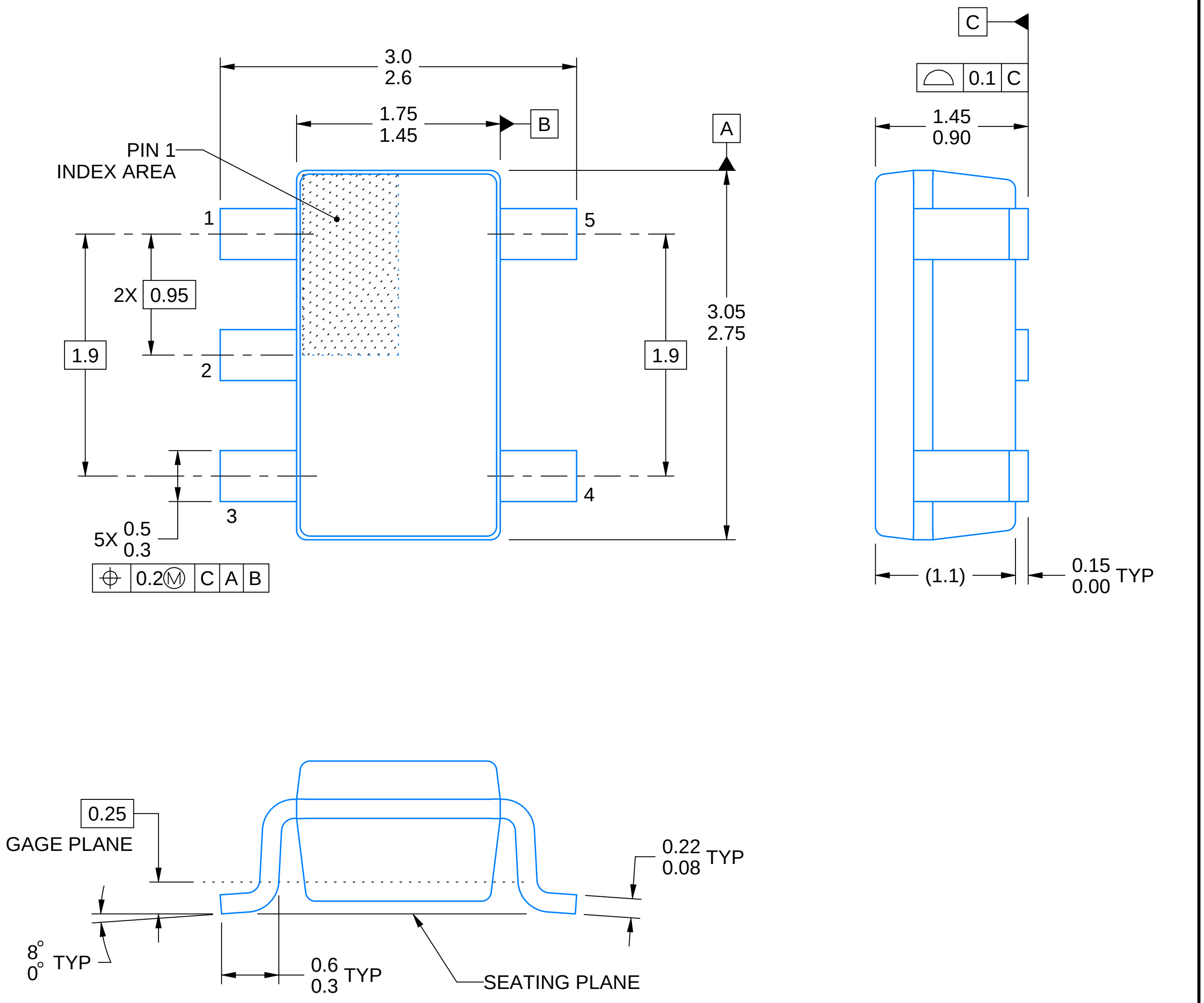
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

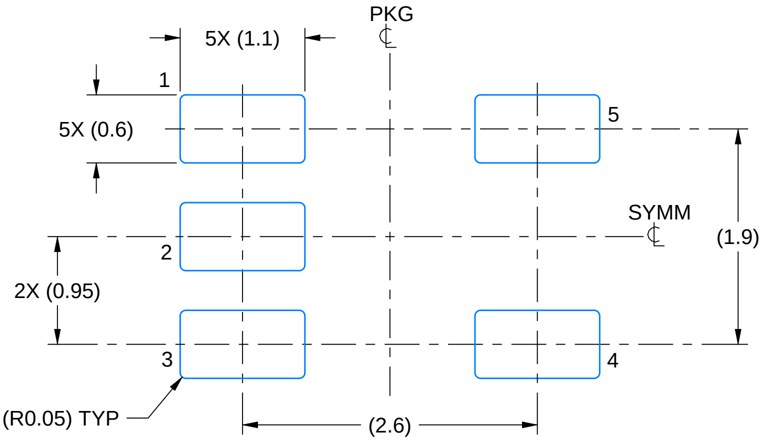
SMALL OUTLINE TRANSISTOR



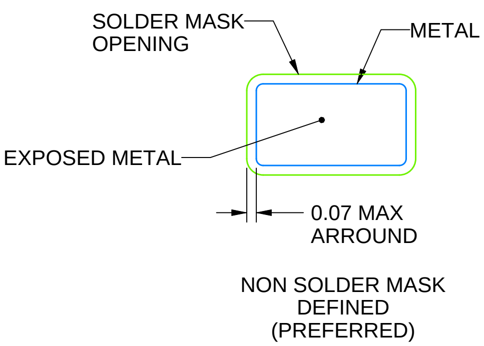
4214839/F 06/2021

NOTES:

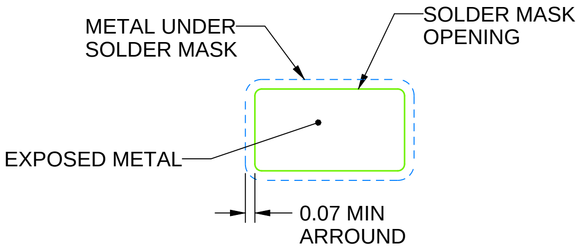
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

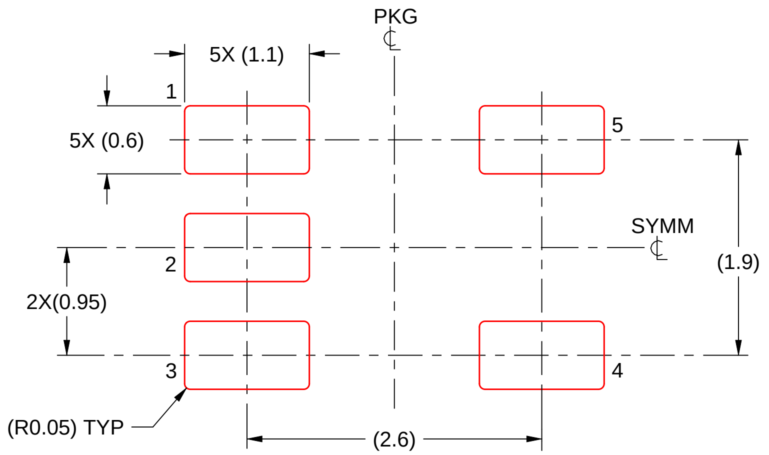


SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

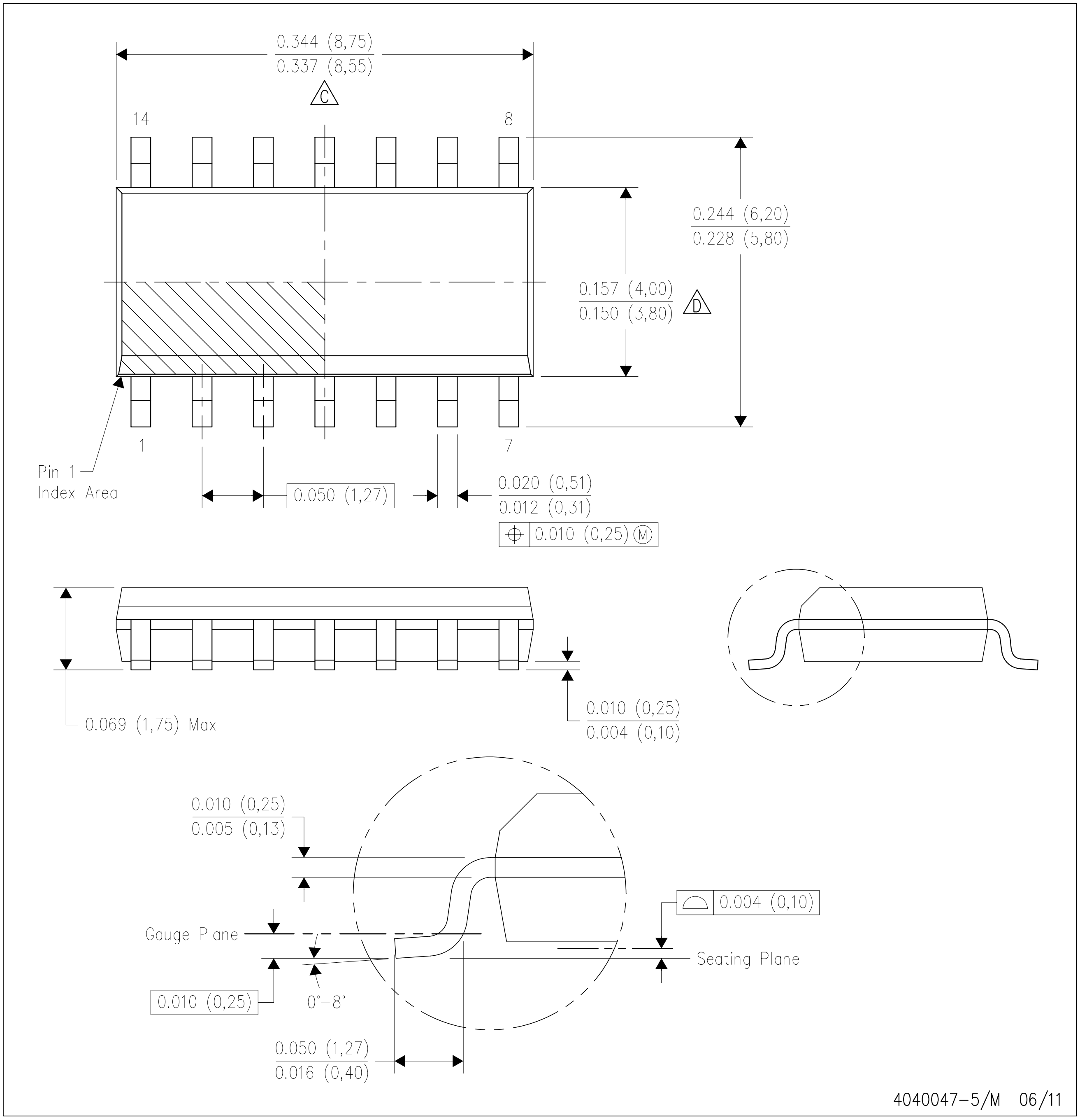


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

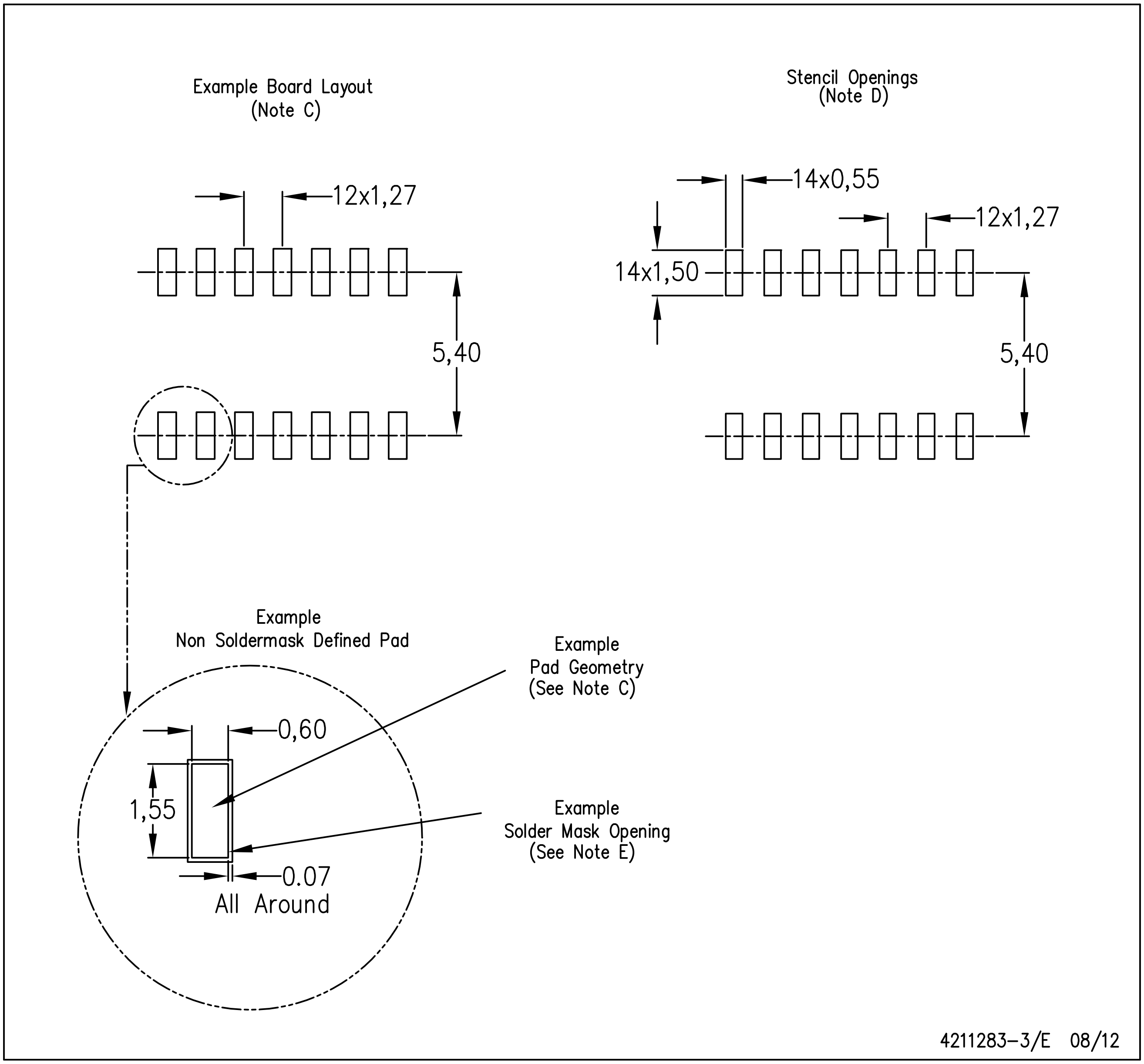
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

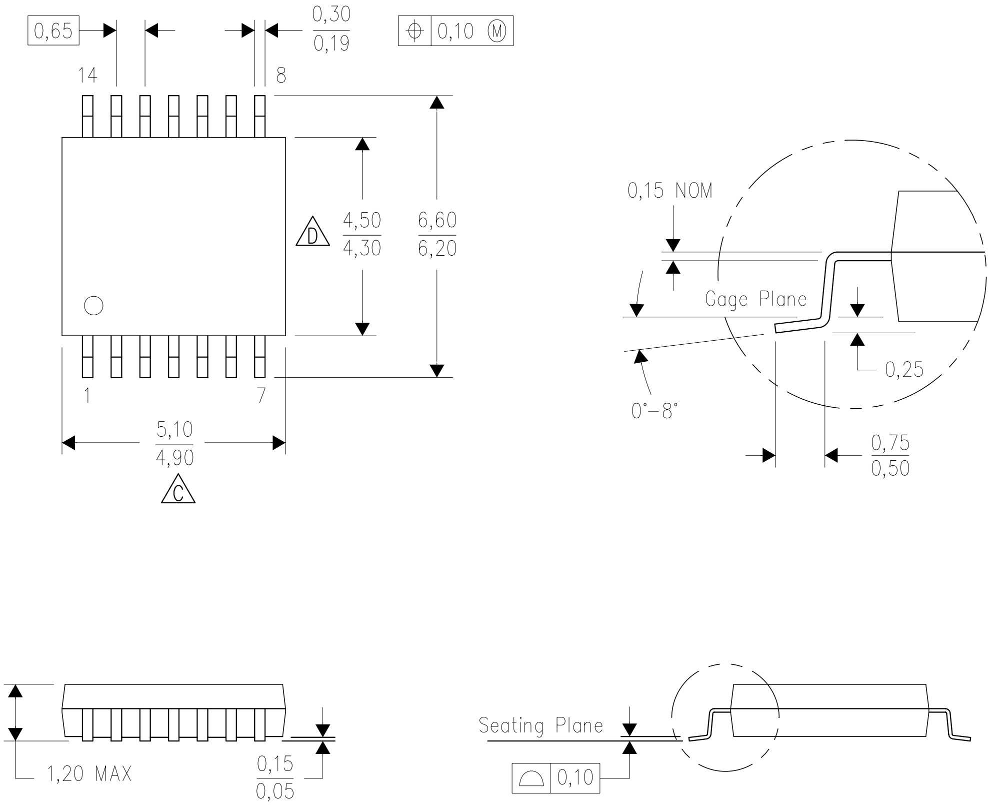
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

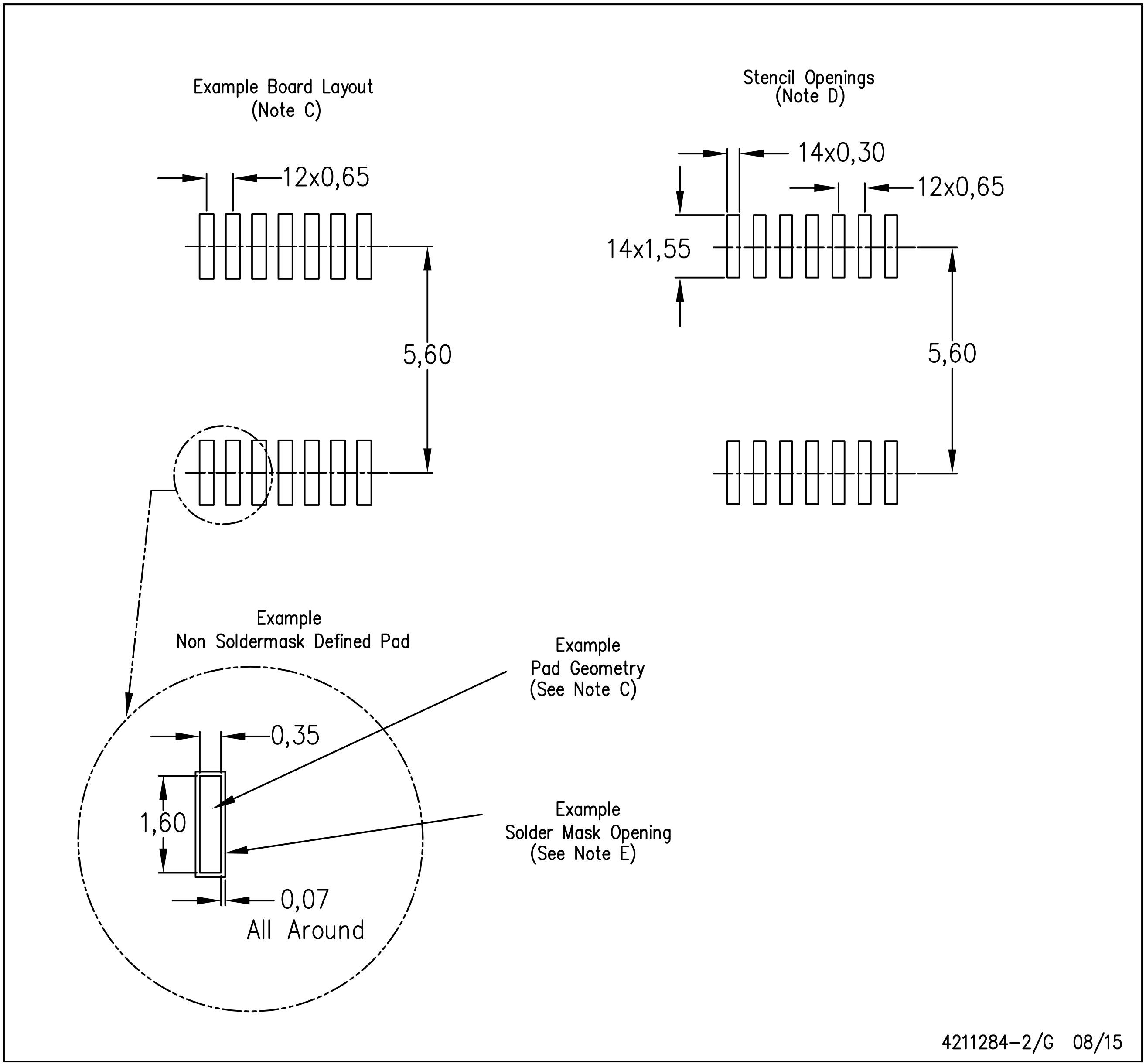
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

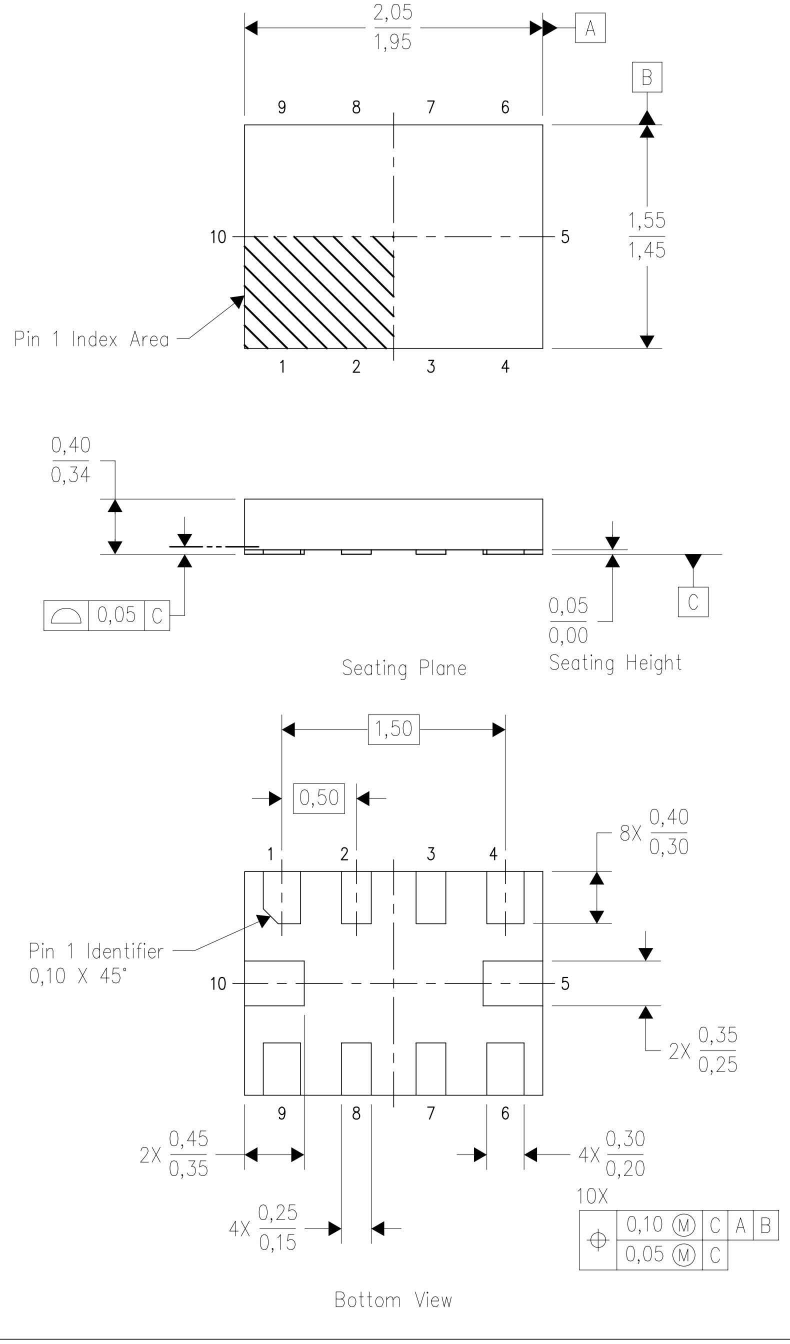
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

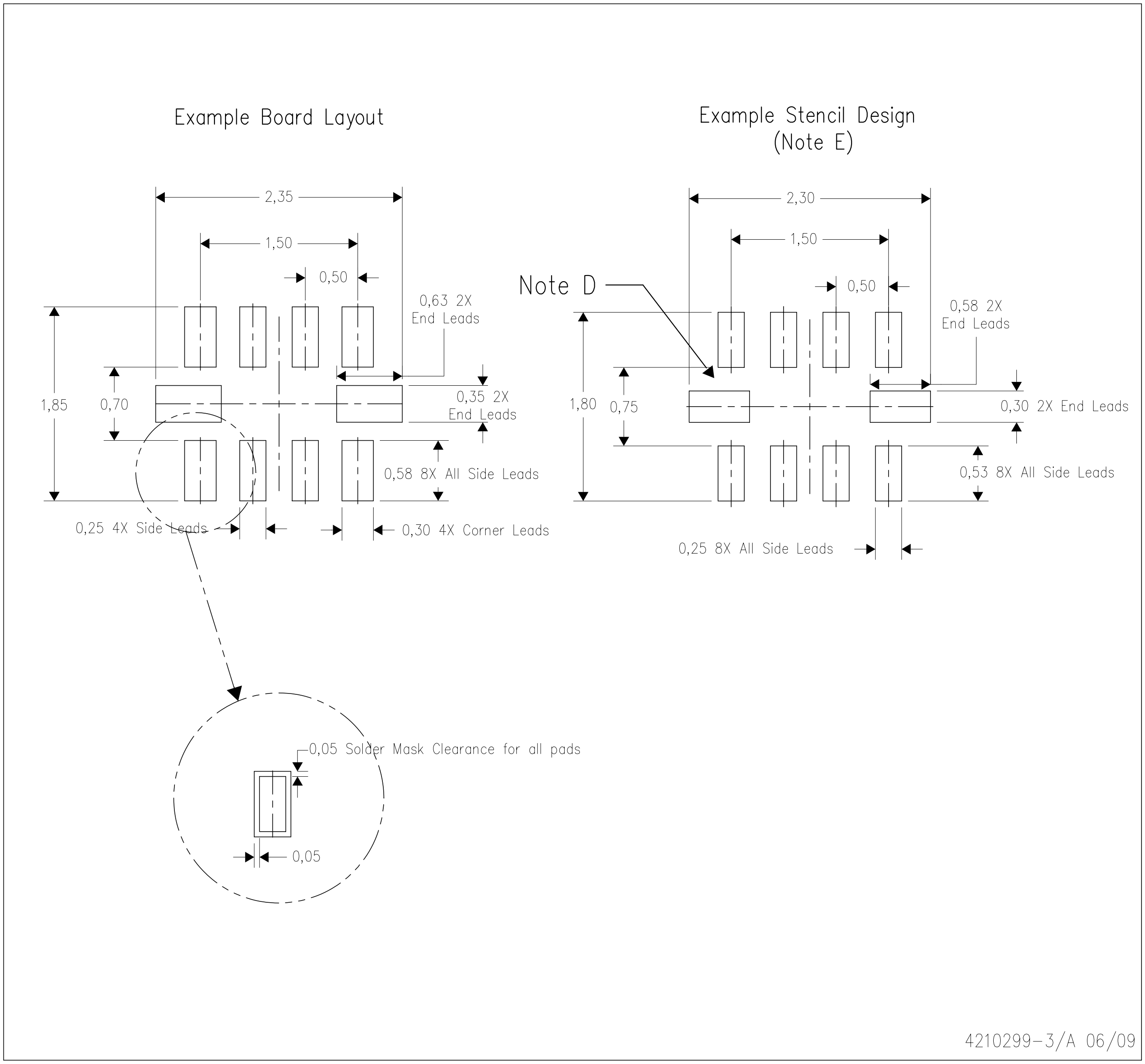
RUG (R–PQFP–N10) PLASTIC QUAD FLATPACK



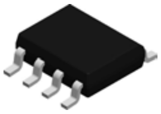
4208528–3/B 04/2008

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. This package complies to JEDEC MO–288 variation X2EFD.

RUG (R–PQFP–N10)



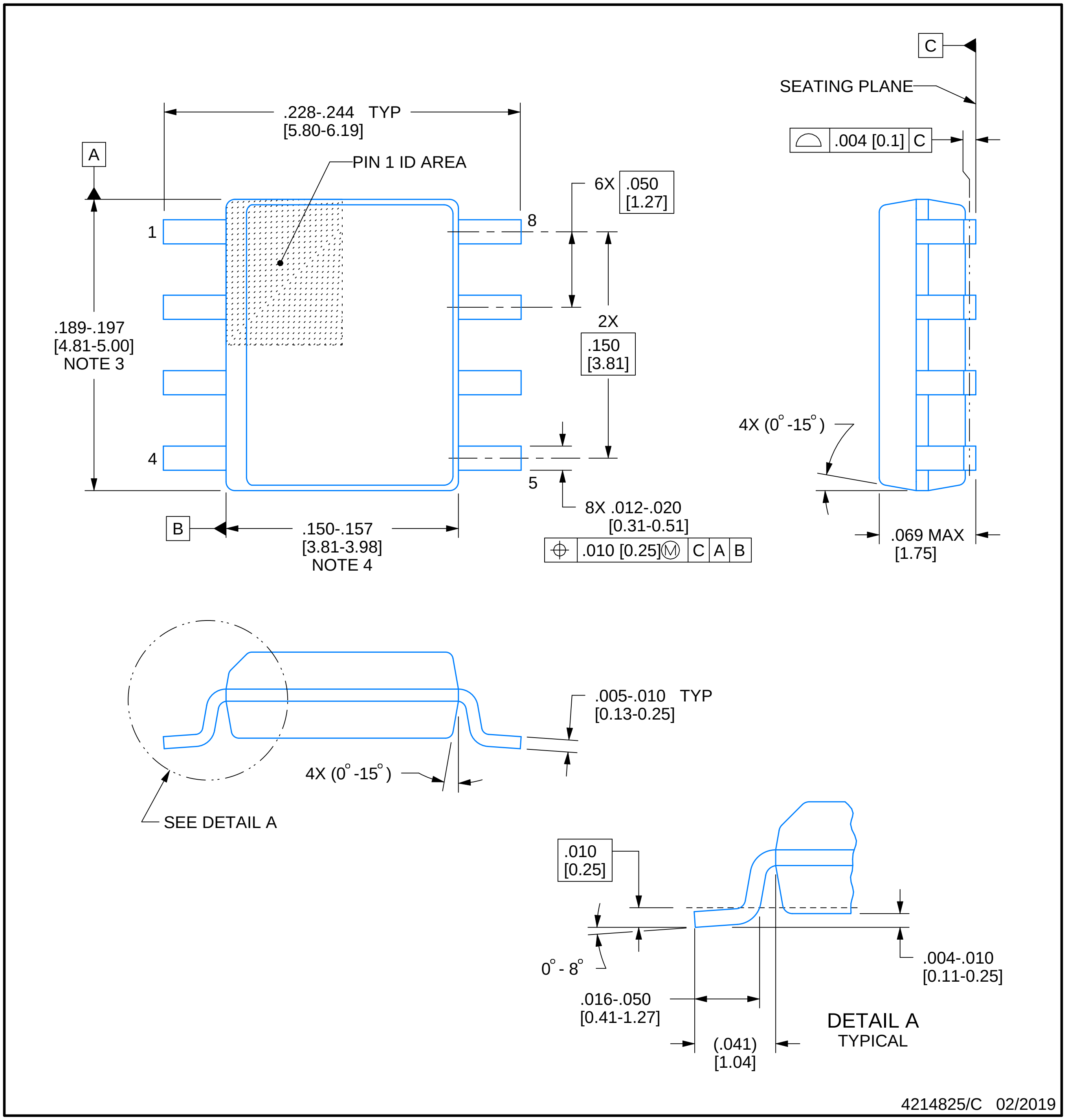
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.



PACKAGE OUTLINE

SOIC - 1.75 mm max height

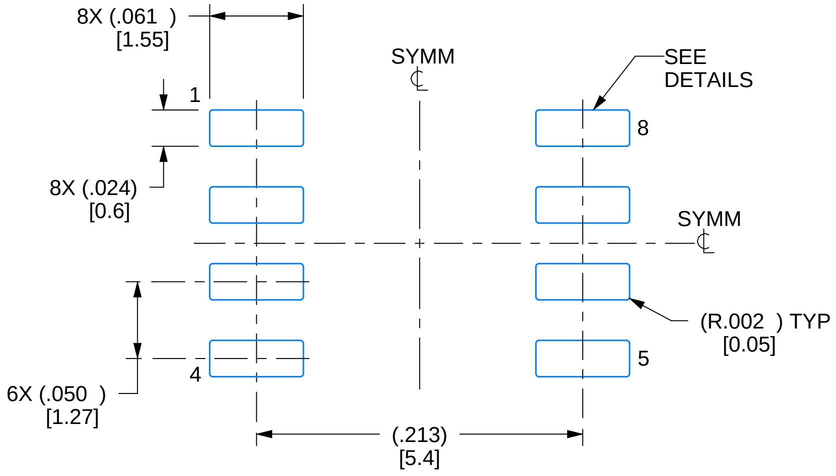
SMALL OUTLINE INTEGRATED CIRCUIT



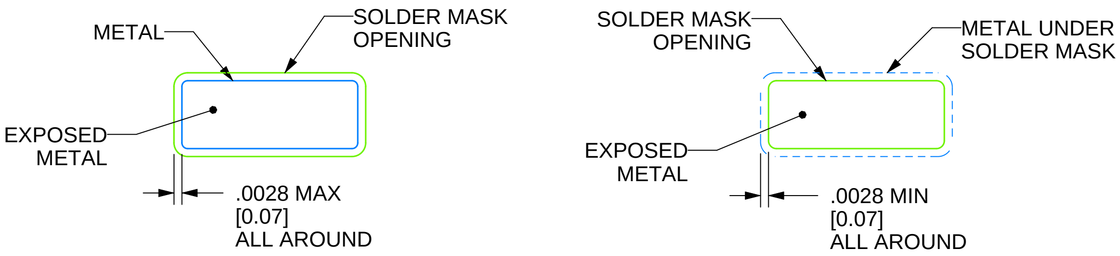
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

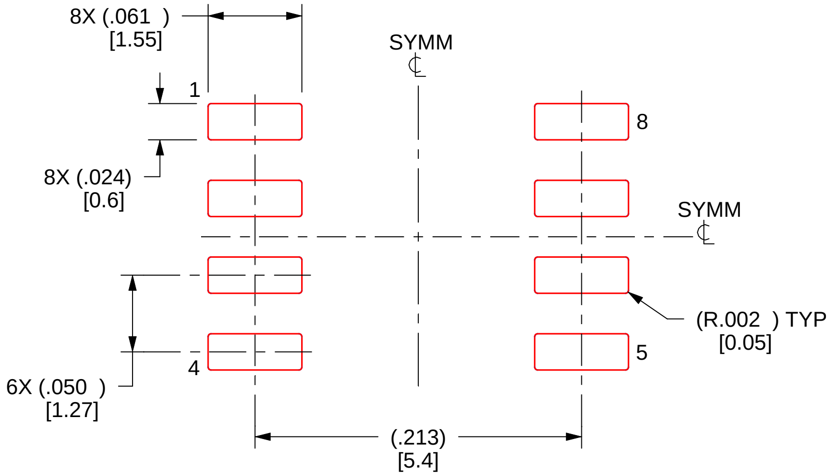
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

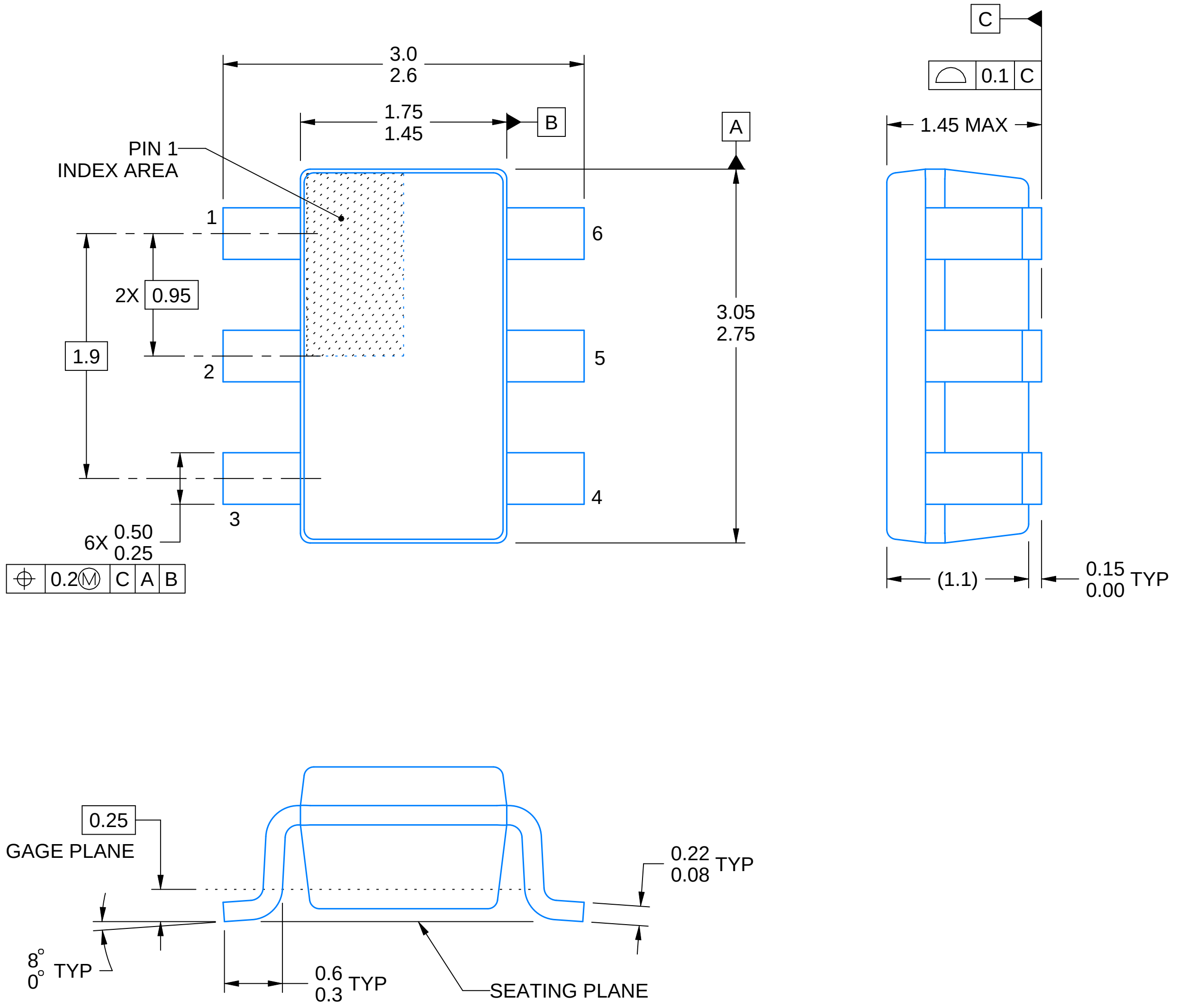


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

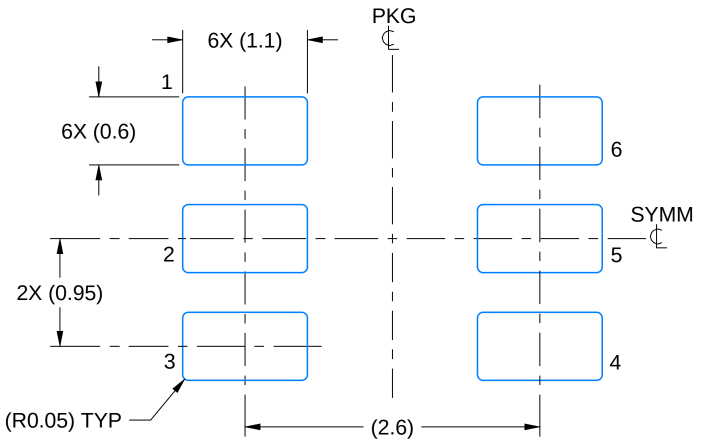
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



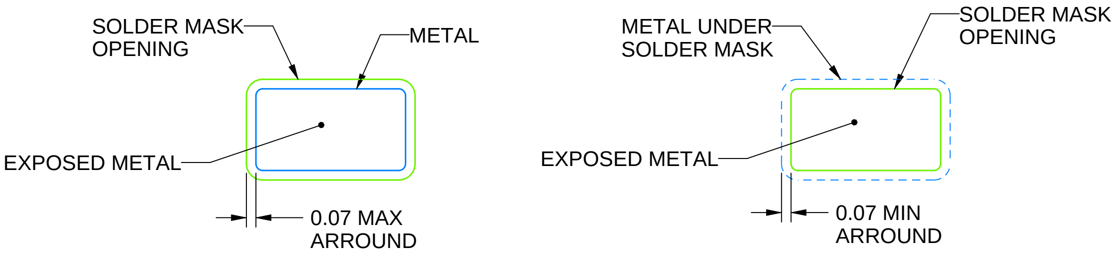
4214840/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



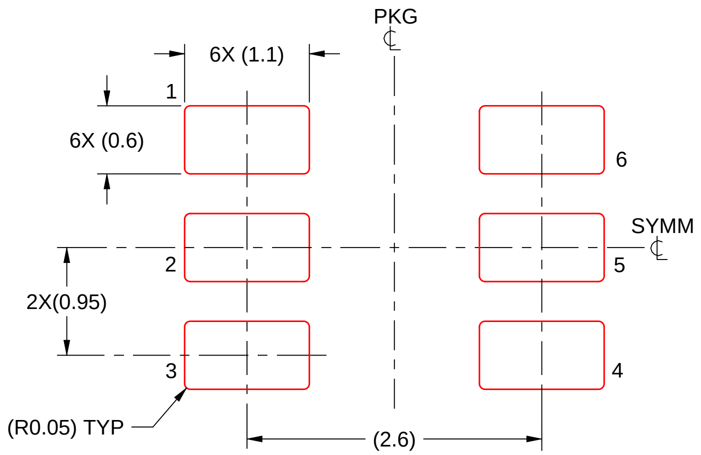
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



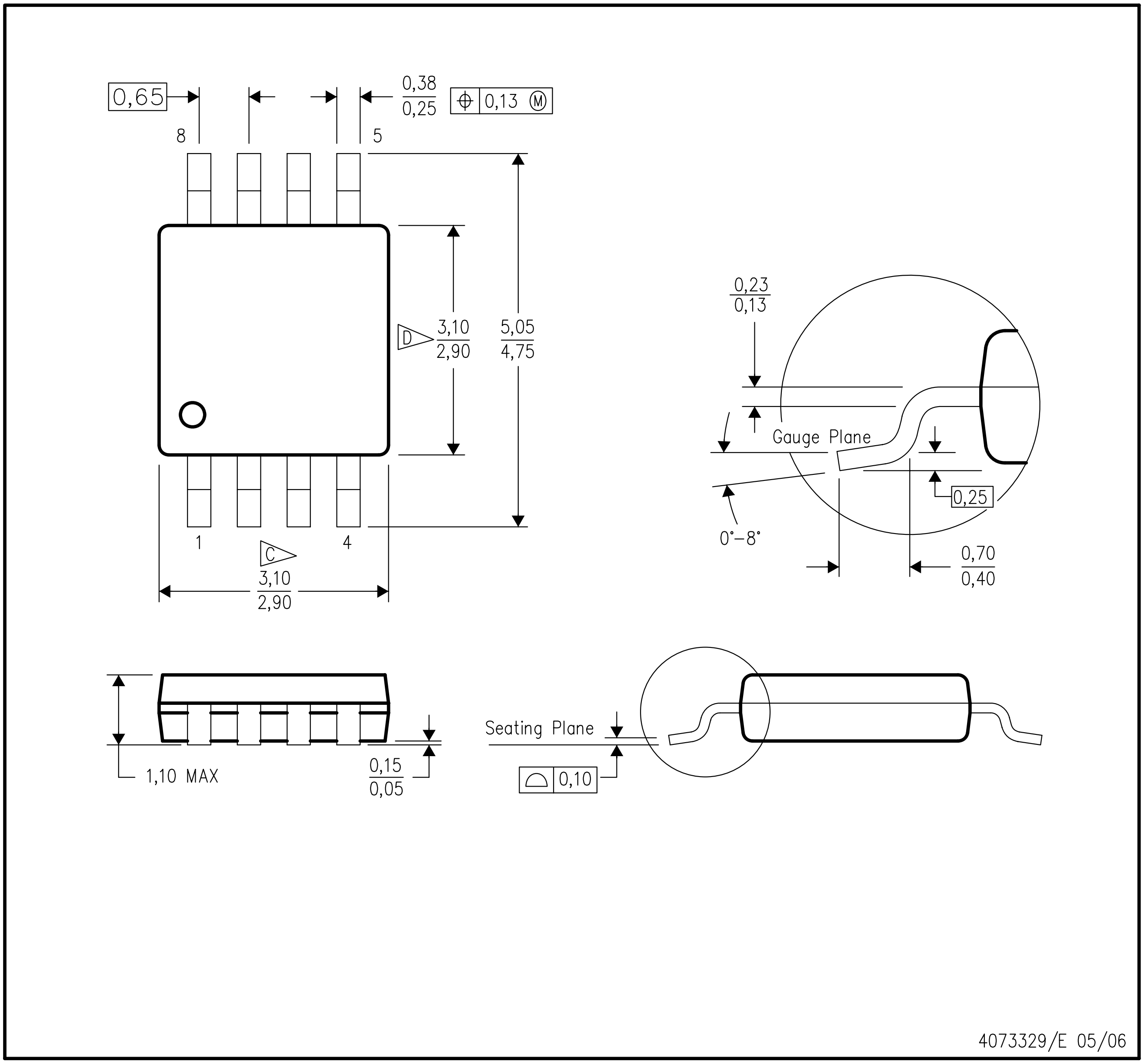
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

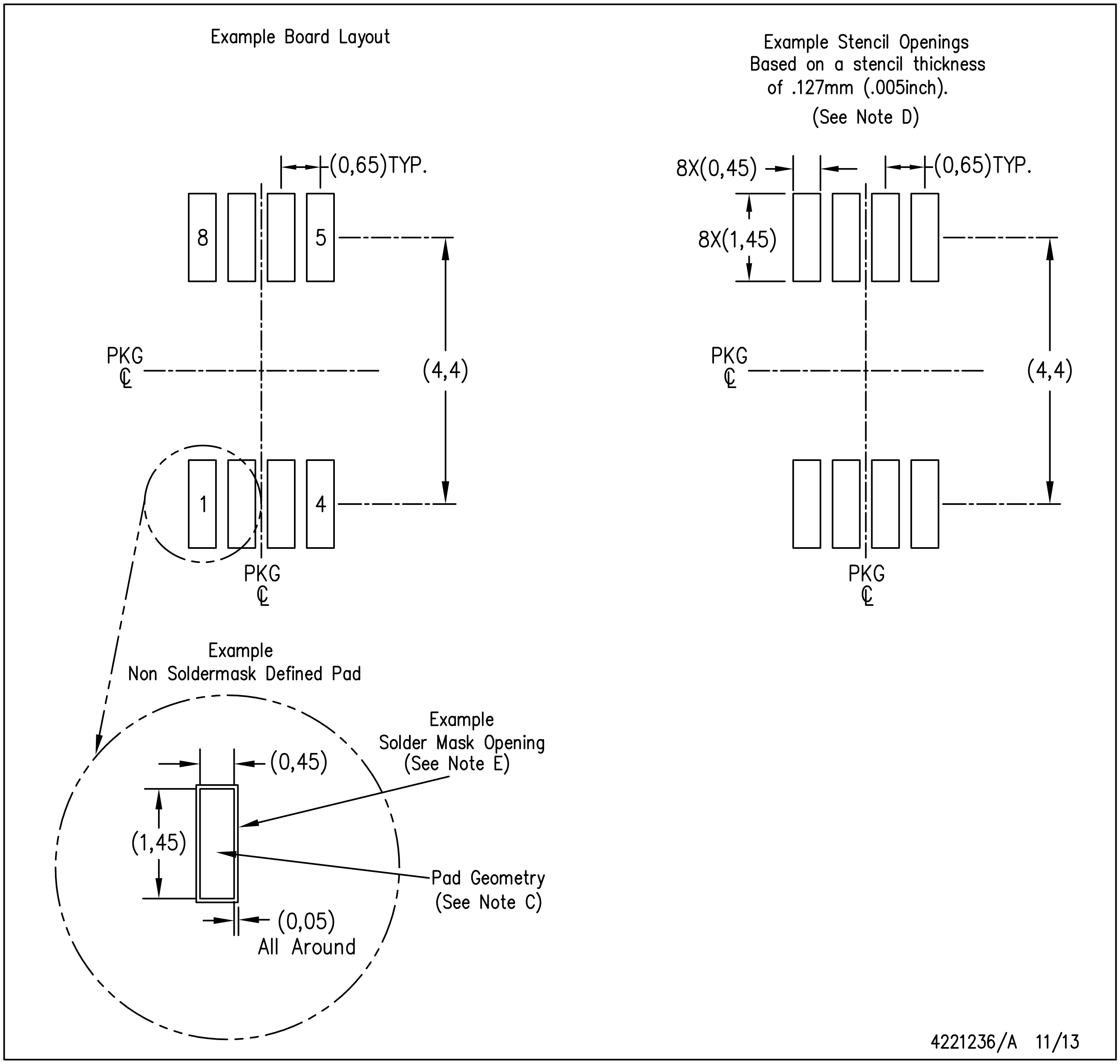
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

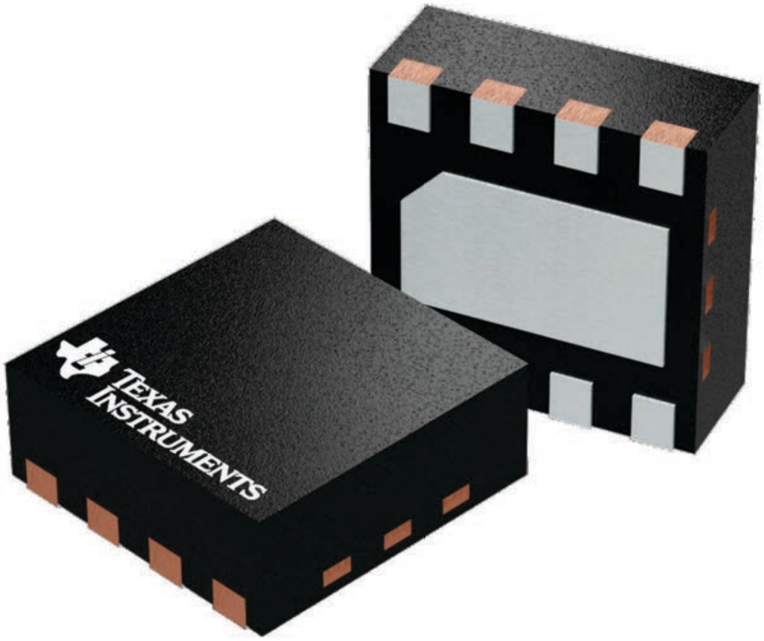
DSG 8

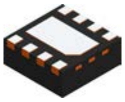
WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

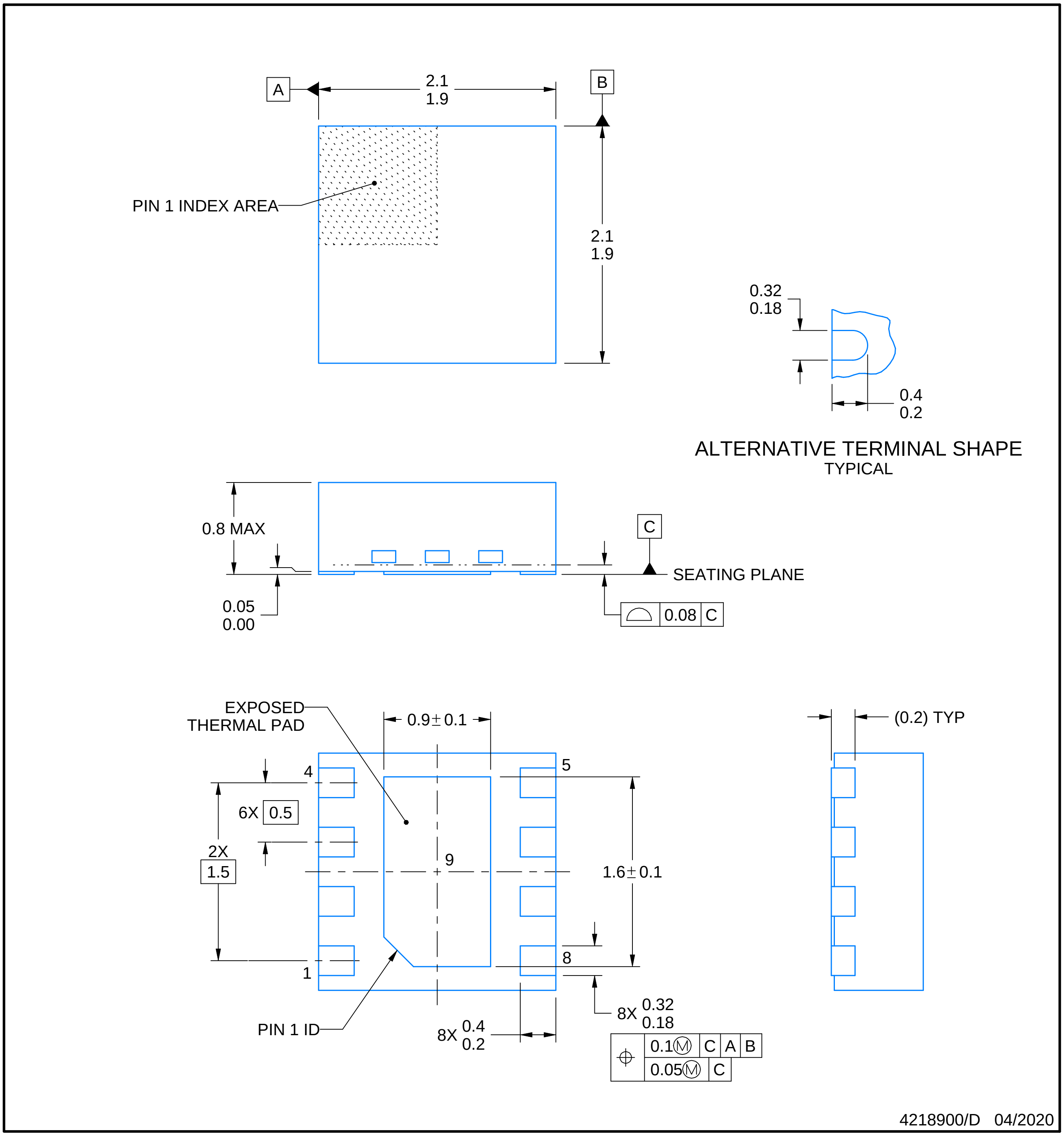




PACKAGE OUTLINE

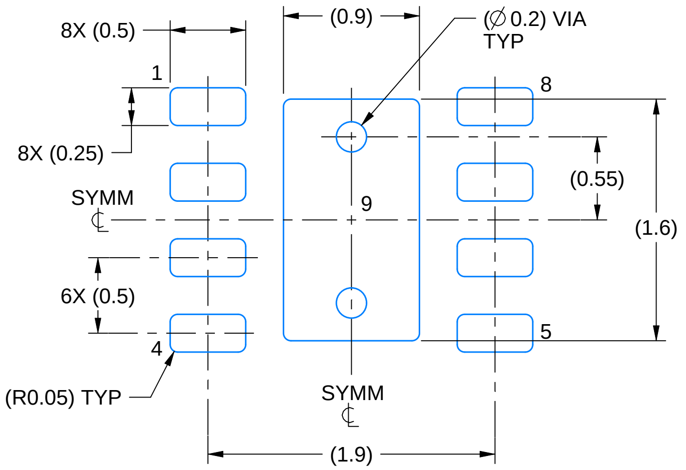
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

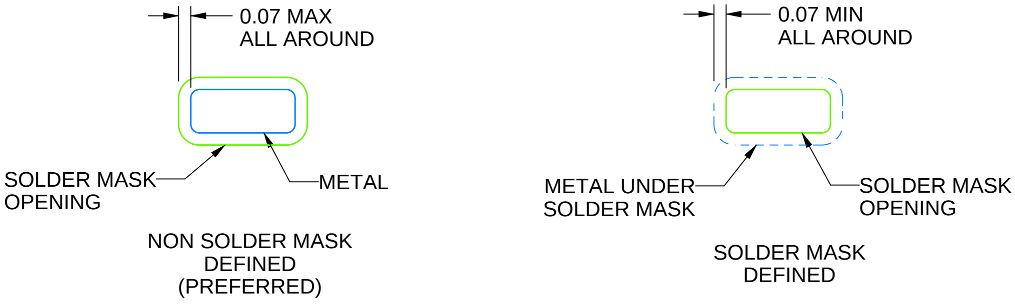


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



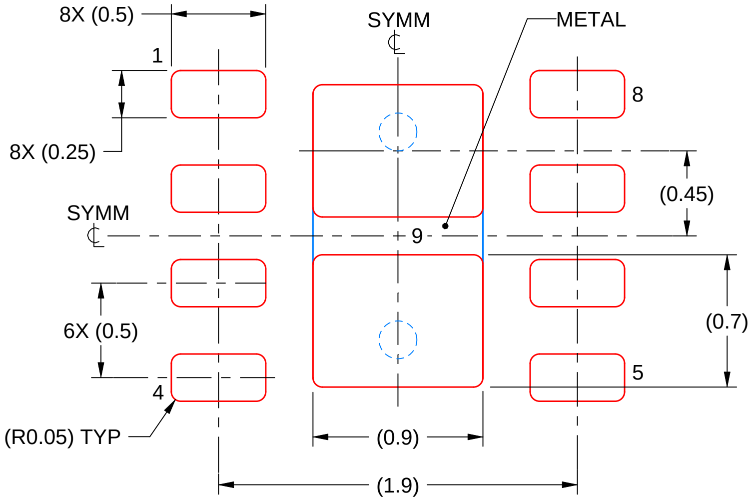
LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



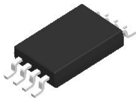
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

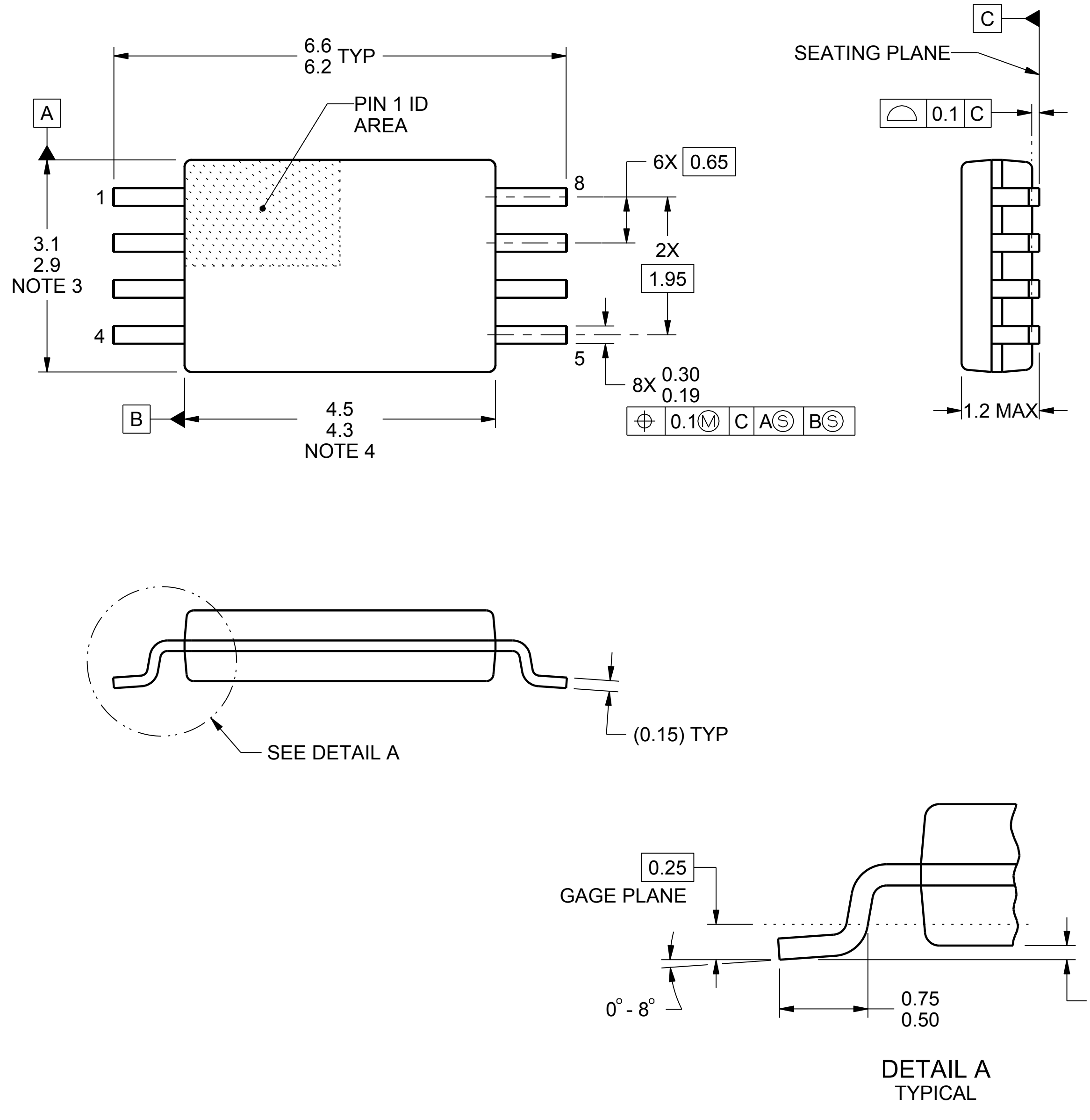
PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

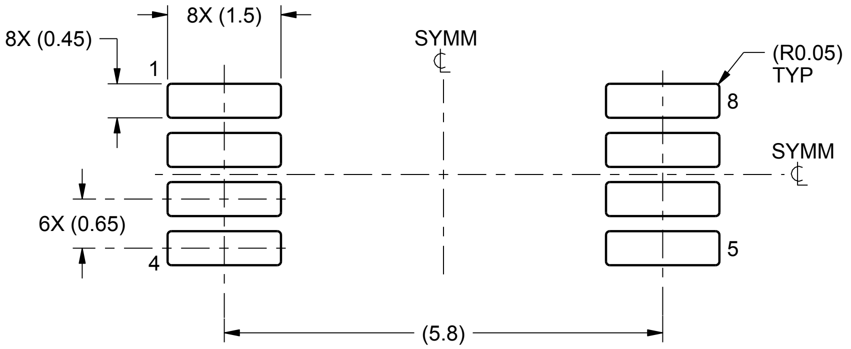
SMALL OUTLINE PACKAGE



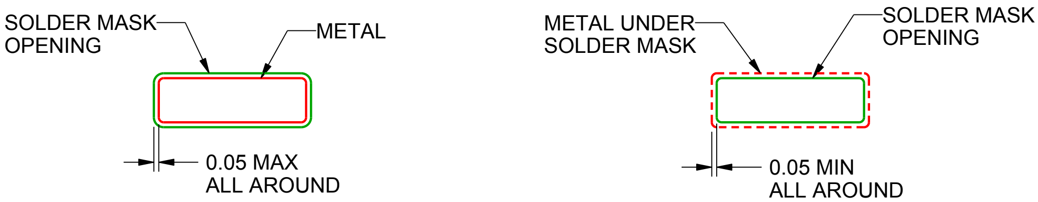
4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK
DEFINED

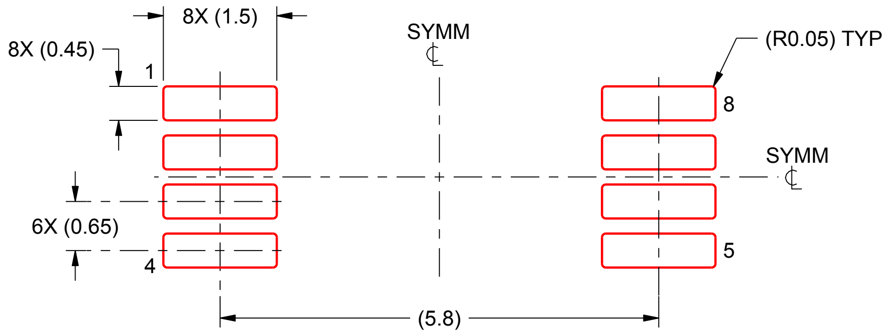
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

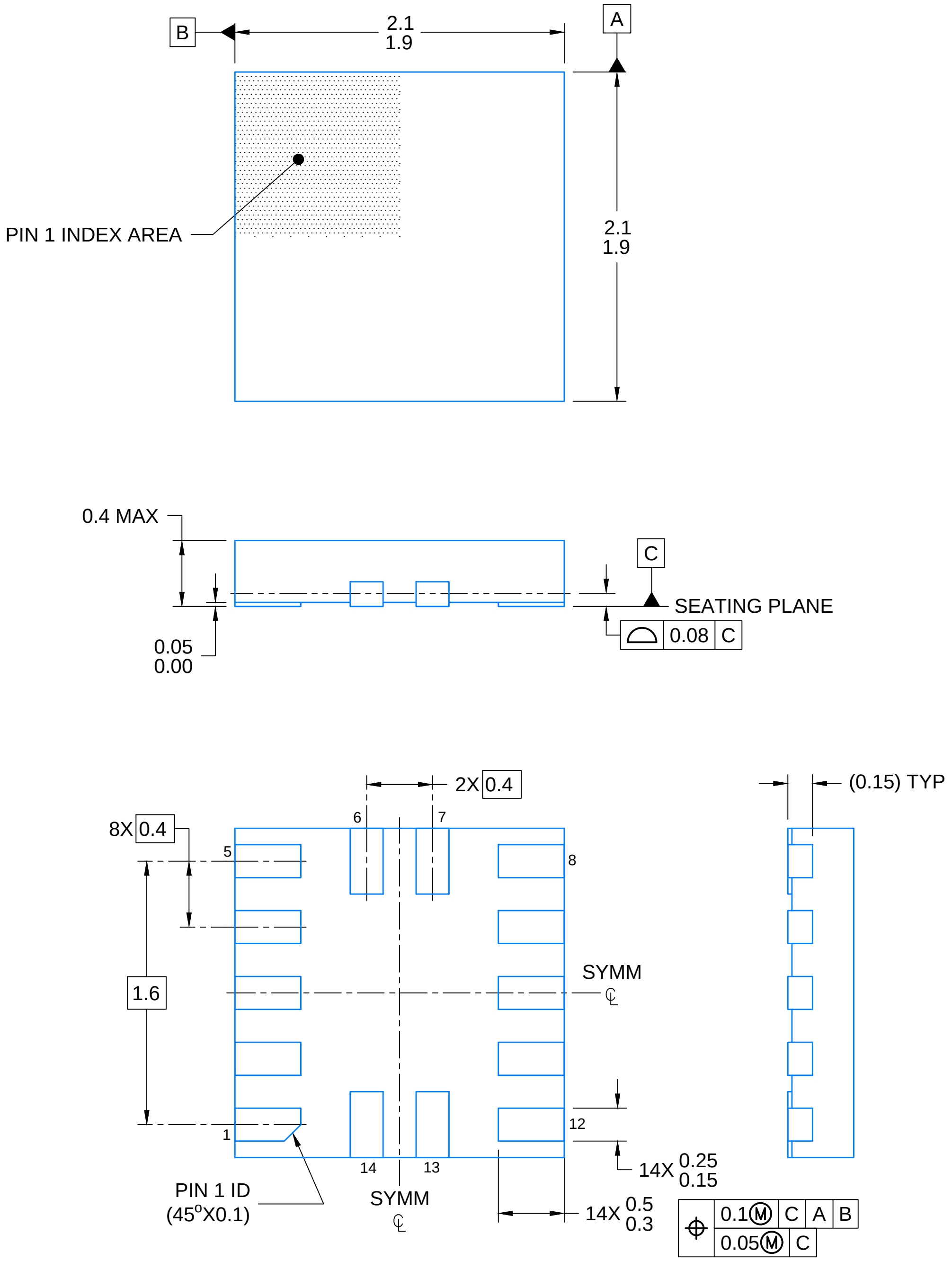
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

NOTES: (continued)

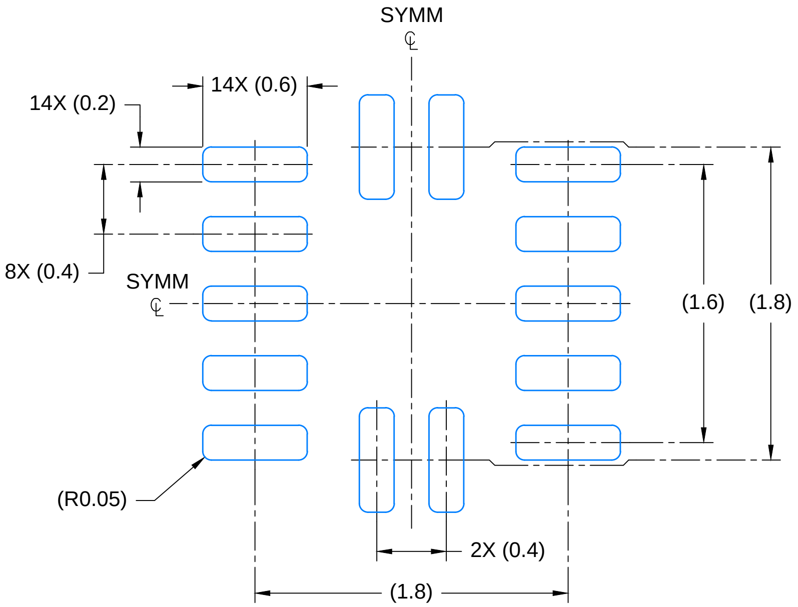
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



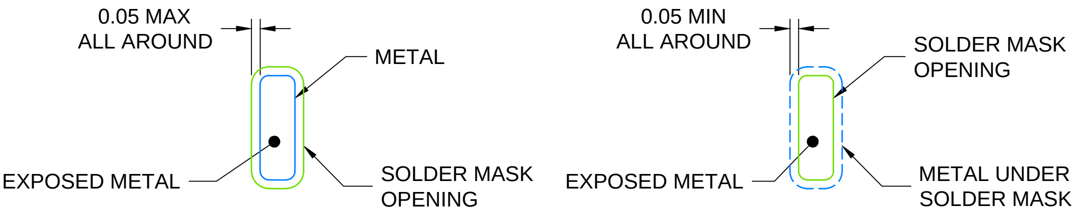
4220584/A 05/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 23X



NON-SOLDER MASK
DEFINED
(PREFERRED)

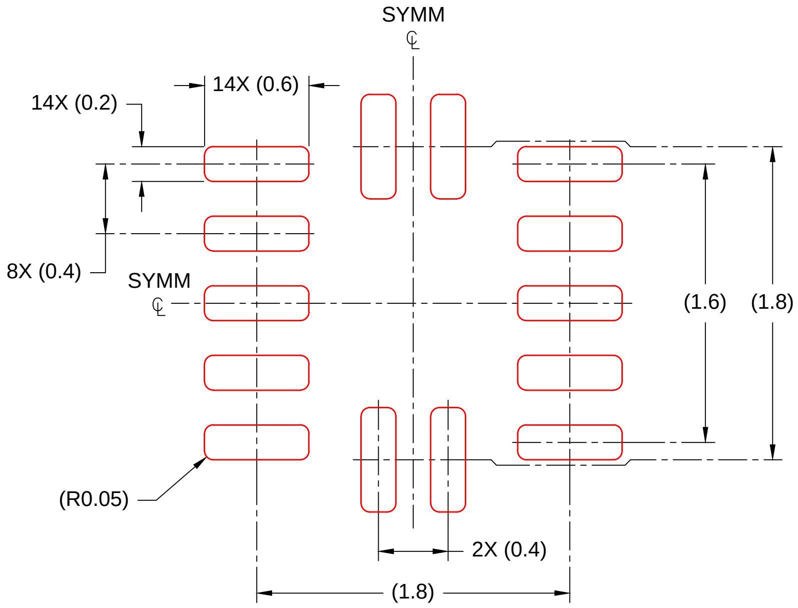
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220584/A 05/2019

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.100mm THICK STENCIL
SCALE: 23X

4220584/A 05/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265