

# 具有清零和预设功能且通过汽车认证的 **SN74HC74-Q1** 双路 D 类正边沿触发器

## 1 特性

- 符合AEC-Q100 车规认证:
  - 器件温度等级 1:  $-40^{\circ}\text{C}$  至  $+125^{\circ}\text{C}$ ,  $T_A$
- 缓冲输入
- 正负输入钳位二极管
- 宽工作电压范围: 2V 至 6V
- 支持多达 10 个 LSTTL 负载的扇出
- 与 LSTTL 逻辑 IC 相比, 可显著降低功耗

## 2 应用

- 将瞬时开关转换为拨动开关
- 二等分或四等分时钟信号

## 3 说明

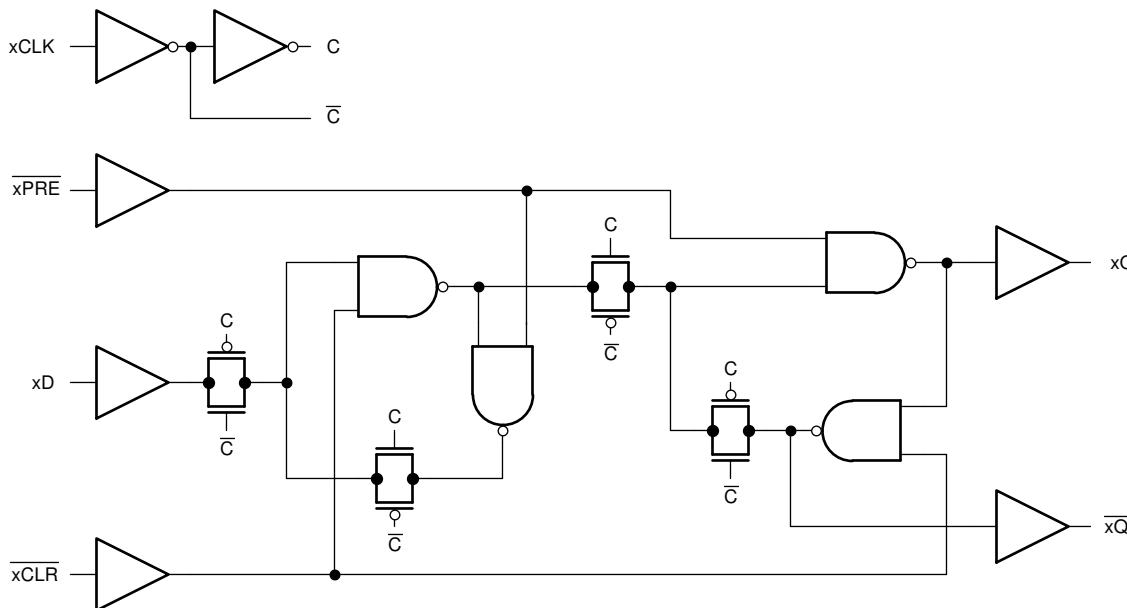
**SN74HC74-Q1** 器件包含两个具有异步预设和清零引脚的独立 D 类正边沿触发器。

### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
SN74HC74QDRQ1	SOIC (14)	8.70mm x 3.90mm
SN74HC74QPWRQ1	TSSOP (14)	5.00mm x 4.40mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

**SN74HC74-Q1** 的功能引脚



本文档旨在为方便起见, 提供有关 TI 产品中文版本的信息, 以确认产品的概要。有关适用的官方英文版本的最新信息, 请访问 [www.ti.com](http://www.ti.com), 其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前, 请务必参考最新版本的英文版本。

English Data Sheet: [SCLS577](#)

## 目录

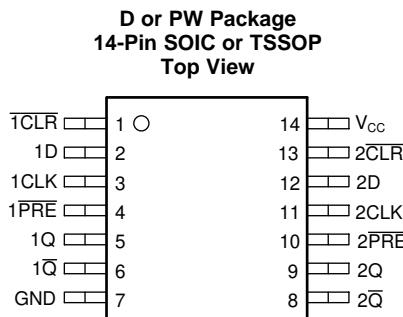
1	特性	1
2	应用	1
3	说明	1
4	修订历史记录	2
5	Pin Configuration and Functions	3
6	Specifications	3
6.1	Absolute Maximum Ratings	3
6.2	ESD Ratings	4
6.3	Recommended Operating Conditions	4
6.4	Thermal Information	4
6.5	Electrical Characteristics	5
6.6	Timing Characteristics	5
6.7	Switching Characteristics	6
6.8	Operating Characteristics	6
6.9	Typical Characteristics	6
7	Parameter Measurement Information	7
8	Detailed Description	8
8.1	Overview	8
8.2	Functional Block Diagram	8
8.3	Feature Description	8
8.4	Device Functional Modes	9
9	Application and Implementation	10
9.1	Application Information	10
9.2	Typical Application	10
10	Power Supply Recommendations	13
11	Layout	13
11.1	Layout Guidelines	13
11.2	Layout Example	13
12	器件和文档支持	14
12.1	文档支持	14
12.2	相关链接	14
12.3	社区资源	14
12.4	商标	14
12.5	静电放电警告	14
12.6	Glossary	14
13	机械、封装和可订购信息	14

## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (April 2008) to Revision B	Page
• 更新至全新数据表标准	1
• Changed $R_{\theta JA}$ for PW package from 113 °C/W to 151.7 °C/W	4
• Changed $R_{\theta JA}$ for D package from 86 °C/W to 133.6 °C/W	4

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1CLR	1	Input	Channel 1, Clear Input, Active Low
1D	2	Input	Channel 1, Data Input
1CLK	3	Input	Channel 1, Positive edge triggered clock input
1PRE	4	Input	Channel 1, Preset Input, Active Low
1Q	5	Output	Channel 1, Output
1Q-bar	6	Output	Channel 1, Inverted Output
GND	7	—	Ground
2Q-bar	8	Output	Channel 2, Inverted Output
2Q	9	Output	Channel 2, Output
2PRE	10	Input	Channel 2, Preset Input, Active Low
2CLK	11	Input	Channel 2, Positive edge triggered clock input
2D	12	Input	Channel 2, Data Input
2CLR	13	Input	Channel 2, Clear Input, Active Low
Vcc	14	—	Positive Supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>cc</sub>	Supply voltage		-0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>cc</sub>		±20	mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>cc</sub>		±20	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>cc</sub>		±25	mA
	Continuous current through V <sub>cc</sub> or GND			±50	mA
T <sub>J</sub>	Junction temperature <sup>(3)</sup>			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) Guaranteed by design.

## 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD Classification Level 2	±2000
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1000

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		V
		V <sub>CC</sub> = 4.5 V	3.15		
		V <sub>CC</sub> = 6 V	4.2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5	V
		V <sub>CC</sub> = 4.5 V		1.35	
		V <sub>CC</sub> = 6 V		1.8	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>		V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>		V
Δt/Δv	Input transition rise and fall rate	V <sub>CC</sub> = 2 V		1000	ns
		V <sub>CC</sub> = 4.5 V		500	
		V <sub>CC</sub> = 6 V		400	
T <sub>A</sub>	Operating free-air temperature		–40	125	°C

## 6.4 Thermal Information

THERMAL METRIC		SN74HC74-Q1		UNIT
		PW (TSSOP)	D (SOIC)	
		14 PINS	14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	151.7	133.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	79.4	89.0	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	94.7	89.5	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	25.2	45.5	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	94.1	89.1	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

## 6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS		$V_{CC}$	Operating free-air temperature ( $T_A$ )			UNIT	
					25°C		-40°C to 125°C		
					MIN	TYP	MAX		
$V_{OH}$	High-level output voltage	$V_I = V_{IH}$ or $V_{IL}$	$I_{OH} = -20 \mu\text{A}$	2 V	1.9	1.998	1.9	V	
				4.5 V	4.4	4.499	4.4		
				6 V	5.9	5.999	5.9		
			$I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.3	3.7		
			$I_{OH} = -5.2 \text{ mA}$	6 V	5.48	5.8	5.2		
$V_{OL}$	Low-level output voltage	$V_I = V_{IH}$ or $V_{IL}$	$I_{OL} = 20 \mu\text{A}$	2 V	0.002	0.1	0.1	V	
				4.5 V	0.001	0.1	0.1		
				6 V	0.001	0.1	0.1		
			$I_{OL} = 4 \text{ mA}$	4.5 V	0.17	0.26	0.4		
			$I_{OL} = 5.2 \text{ mA}$	6 V	0.15	0.26	0.4		
$I_I$	Input leakage current	$V_I = V_{CC}$ or 0		6 V	$\pm 0.1$	$\pm 100$	$\pm 1000$	nA	
$I_{CC}$	Supply current	$V_I = V_{CC}$ or 0	$I_O = 0$	6 V		4	80	$\mu\text{A}$	
$C_i$	Input capacitance			2 V to 6 V	3	10	10	pF	

## 6.6 Timing Characteristics

$C_L = 50 \text{ pF}$ ; over operating free-air temperature range (unless otherwise noted). See [Parameter Measurement Information](#).

PARAMETER			$V_{CC}$	Operating free-air temperature ( $T_A$ )				UNIT	
				25°C		-40°C to 125°C			
				MIN	MAX	MIN	MAX		
$f_{clock}$	Clock frequency			2 V		6	4.2	MHz	
				4.5 V		31	21		
				6 V	0	36	0		
$t_w$	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low		2 V	100	150		ns	
				4.5 V	20	30			
				6 V	17	25			
		CLK high or low		2 V	80	120			
				4.5 V	16	24			
				6 V	14	20			
$t_{su}$	Setup time before CLK↑	Data		2 V	100	150		ns	
				4.5 V	20	30			
				6 V	17	25			
		$\overline{PRE}$ or $\overline{CLR}$ inactive		2 V	25	40			
				4.5 V	5	8			
				6 V	4	7			
$t_h$	Hold time, data after CLK↑			2 V	0	0		ns	
				4.5 V	0	0			
				6 V	0	0			

## 6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM	TO	V <sub>CC</sub>	Operating free-air temperature (T <sub>A</sub> )			UNIT
					25°C		-40°C to 125°C	
					MIN	TYP	MAX	
f <sub>max</sub>	Max switching frequency			2 V	6	10	4.2	MHz
				4.5 V	31	50	21	
				6 V	36	60	25	
t <sub>pd</sub>	Propagation delay	PRE or CLR	Q or $\bar{Q}$	2 V	70	230	345	ns
				4.5 V	20	46	69	
				6 V	15	39	59	
		CLK	Q or $\bar{Q}$		70	175	250	
					20	35	50	
					15	30	42	
t <sub>t</sub>	Transition-time		Q or $\bar{Q}$	2 V	28	75	110	ns
				4.5 V	8	15	22	
				6 V	6	13	19	

## 6.8 Operating Characteristics

over operating free-air temperature range; typical values measured at T<sub>A</sub> = 25°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C <sub>pd</sub>	Power dissipation capacitance per gate	No load	35		pF

## 6.9 Typical Characteristics

T<sub>A</sub> = 25°C

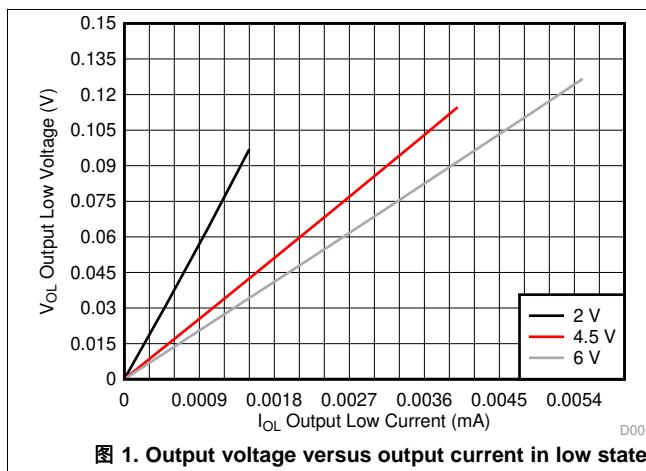


图 1. Output voltage versus output current in low state

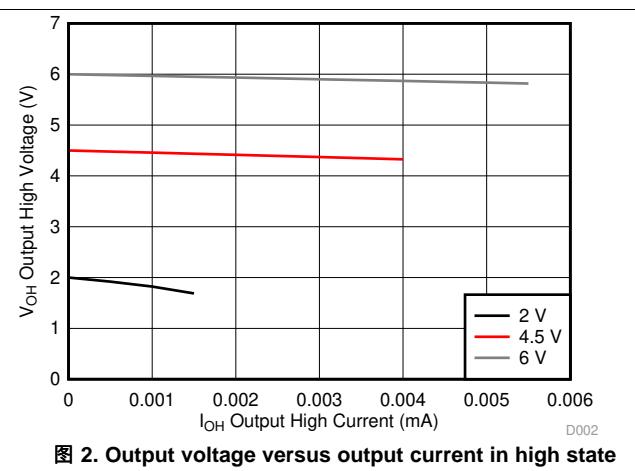
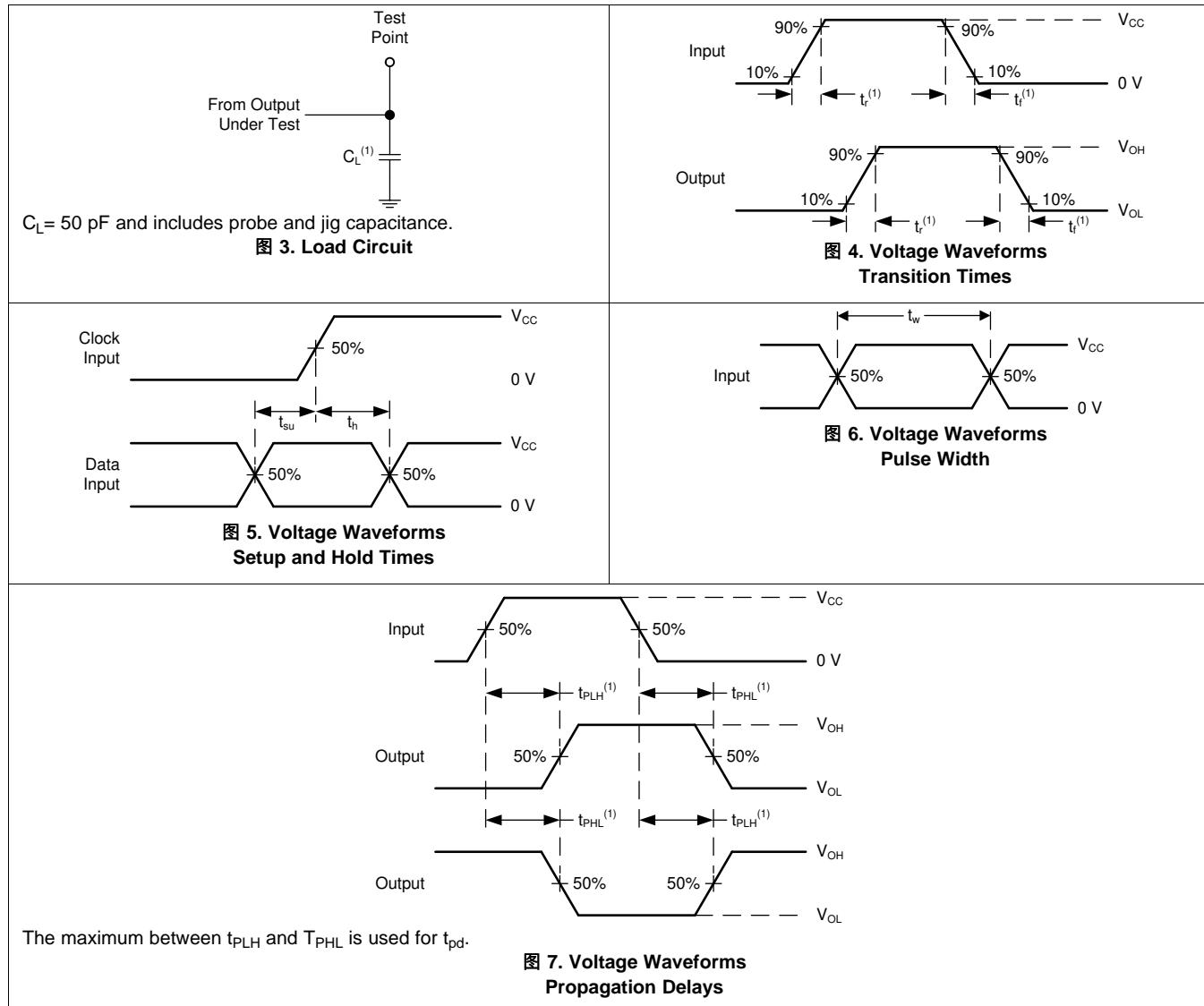


图 2. Output voltage versus output current in high state

## 7 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_t < 6$  ns.
- The outputs are measured one at a time, with one input transition per measurement.

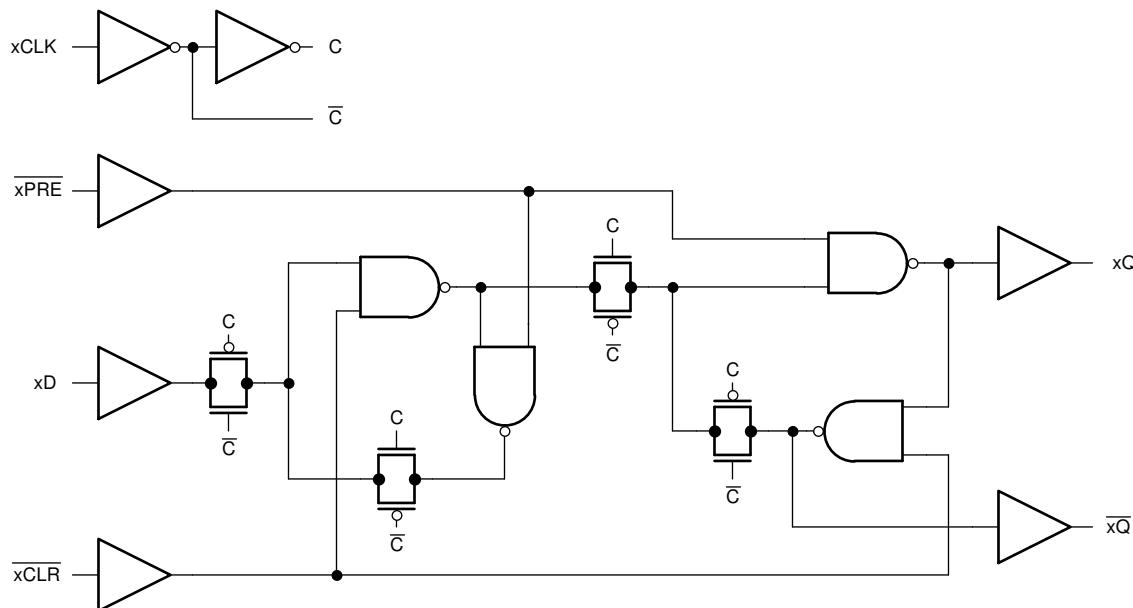


## 8 Detailed Description

## 8.1 Overview

The SN74HC74-Q1 devices contain two independent D-type positive-edge-triggered flip-flops with asynchronous preset and clear pins for each.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

The SN74HC74-Q1 can drive a load with a total capacitance less than or equal to 50 pF connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 70 pF. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the [Absolute Maximum Ratings](#).

### 8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the [Electrical Characteristics](#). The worst case resistance is calculated with the maximum input voltage, given in the [Absolute Maximum Ratings](#), and the maximum input leakage current, given in the [Electrical Characteristics](#), using ohm's law ( $R = V \div I$ ).

Signals applied to the inputs need to have fast edge rates, as defined by  $\Delta t/\Delta v$  in the [Recommended Operating Conditions](#) to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

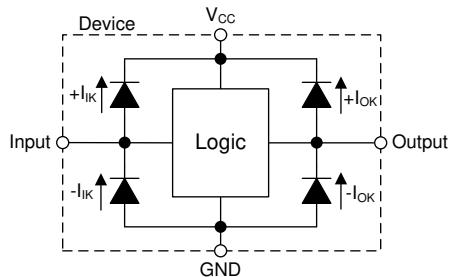
## Feature Description (接下页)

### 8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in [图 8](#).

#### CAUTION

Voltages beyond the values specified in the [Absolute Maximum Ratings](#) table can cause damage to the device. The recommended input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



**图 8. Electrical Placement of Clamping Diodes for Each Input and Output**

### 8.4 Device Functional Modes

**表 1. Function Table**

INPUTS				OUTPUTS		
$\overline{PRE}$	$\overline{CLR}$	$\overline{CL\ K}$	D	Q	$\overline{Q}$	
L	H	X	X	H	L	
H	L	X	X	L	H	
L	L	X	X	$H^{(1)}$	$H^{(1)}$	
H	H	↑	H	H	L	
H	H	↑	L	L	H	
H	H	L	X	$Q_0$	$\overline{Q}_0$	

- (1) This configuration is nonstable; that is, it does not persist when  $\overline{PRE}$  or  $\overline{CLR}$  returns to its inactive (high) level.

## 9 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

Toggle switches are typically large, mechanically complex and relatively expensive. It is desirable to use a momentary switch instead because they are small, mechanically simple and low cost. Some systems require a toggle switch's functionality but are space or cost constrained and must use a momentary switch instead. The SN74HC74-Q1 together with a dual Schmitt-trigger buffer such as SN74LVC2G17 can be used to convert a momentary switch to a toggle switch.

If the data input (D) of the SN74HC74-Q1 is tied to the inverted output ( $\bar{Q}$ ), then each clock pulse will cause the value at the output (Q) to toggle. The momentary switch can be debounced and connected to the buffered clock input (CLK) to toggle the output. These connections are shown in [图 9](#)

### 9.2 Typical Application

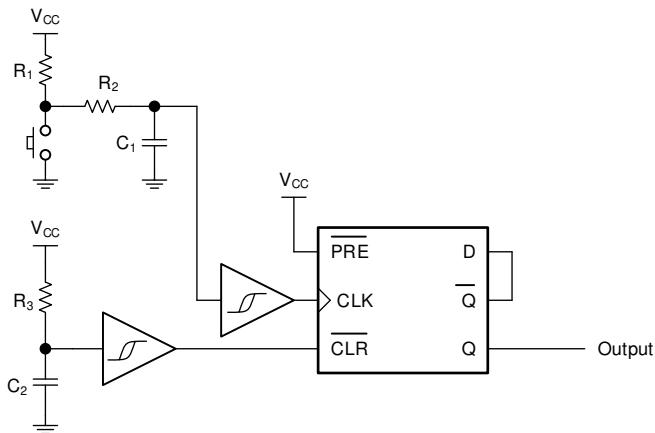


图 9. Typical application schematic

#### 9.2.1 Design Requirements

- Most switches require a debounce time constant of at least 10ms ( $2.2 \times R2 \times C1 > 10ms$ )
- The debounce delay needs to be much smaller than the power on reset circuit's delay to prevent a false trigger during power on ( $R3 \times C3 \gg R2 \times C1$ )
- Conditions for output
  - Q output is LOW at system startup due to the provided reset circuit
  - Each button press will toggle the Q output between LOW and HIGH

##### 9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the [Recommended Operating Conditions](#). The supply voltage sets the device's electrical characteristics as described in the [Electrical Characteristics](#).

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HC74-Q1 plus the maximum supply current,  $I_{CC}$ , listed in the [Electrical Characteristics](#). The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or  $V_{CC}$  listed in the [Absolute Maximum Ratings](#).

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and  \$C\_{pd}\$  Calculation](#).

## Typical Application (接下页)

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

### CAUTION

The maximum junction temperature,  $T_J(\max)$  listed in the [Absolute Maximum Ratings](#), is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the [Absolute Maximum Ratings](#). These limits are provided to prevent damage to the device.

### 9.2.1.2 Input Considerations

Unused inputs must be terminated to either  $V_{CC}$  or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HC74-Q1, as specified in the [Electrical Characteristics](#), and the desired input transition rate. A 10-k $\Omega$  resistor value is often used due to these factors.

The SN74HC74-Q1 has standard CMOS inputs, so input signal edge rates cannot be slow. Slow input edge rates can cause oscillations and damaging shoot-through current. The recommended rates are defined in the [Recommended Operating Conditions](#).

Refer to the [Feature Description](#) for additional information regarding the inputs for this device.

### 9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the [Electrical Characteristics](#). Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the [Electrical Characteristics](#).

Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to the [Feature Description](#) for additional information regarding the outputs for this device.

### 9.2.1.4 Timing Considerations

The SN74HC74-Q1 is a clocked device. As such, it requires special timing considerations to ensure normal operation.

Primary timing factors to consider:

- Maximum clock frequency: the maximum operating clock frequency defined in [Timing Characteristics](#) is the maximum frequency at which the device is guaranteed to function. This value refers specifically to the triggering waveform, measuring from one trigger level to the next.
- Pulse duration: ensure that the triggering event duration is larger than the minimum pulse duration, as defined in the [Timing Characteristics](#).
- Setup time: ensure that the data has changed at least one setup time prior to the triggering event, as defined in the [Timing Characteristics](#).
- Hold time: ensure that the data remains in the desired state at least one hold time after the triggering event, as defined in the [Timing Characteristics](#).

### 9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the [Layout](#).
2. Ensure the capacitive load at the output is  $\leq 70$  pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HC74-Q1 to the receiving device.
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(\max)}) \Omega$ . This will ensure that the maximum

## Typical Application (接下页)

output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.

4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#)

### 9.2.3 Application Curves

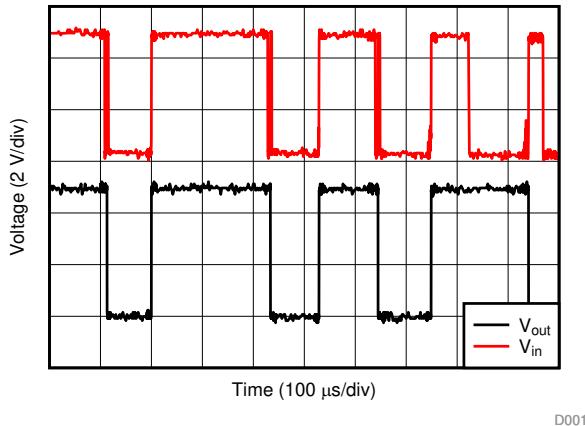


图 10. Circuit response without RC debounce  
 $V_{in}$  := CLK input,  $V_{out}$  := Q output

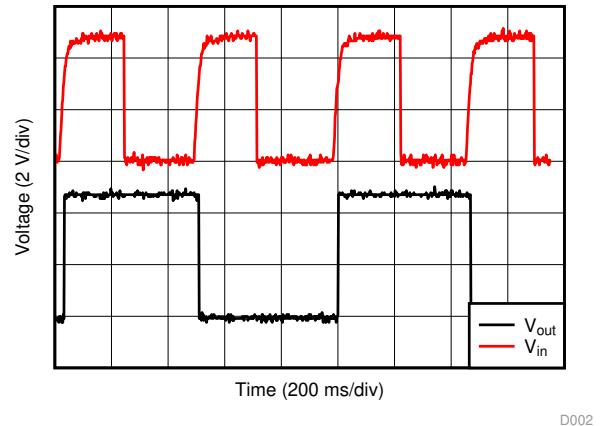


图 11. Circuit response with RC debounce  
 $V_{in}$  := CLK input,  $V_{out}$  := Q output

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a bypass capacitor to prevent power disturbance. A  $0.1\text{-}\mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The  $0.1\text{-}\mu\text{F}$  and  $1\text{-}\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in [图 12](#).

## 11 Layout

### 11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

### 11.2 Layout Example

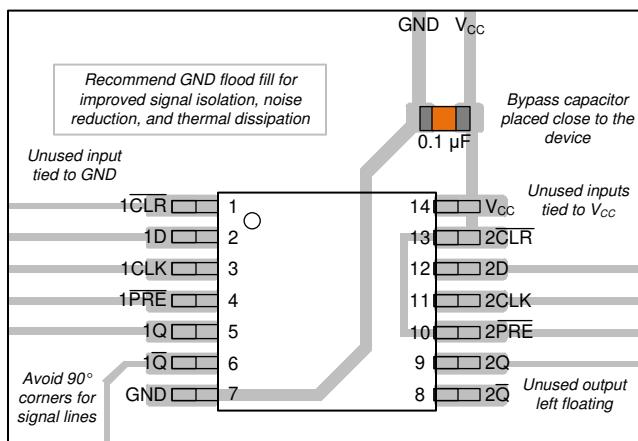


图 12. Example layout for the SN74HC74-Q1

## 12 器件和文档支持

### 12.1 文档支持

#### 12.1.1 相关文档

请参阅如下相关文档：

- [《HCMOS 设计注意事项》](#)
- [《CMOS 功耗与 CPD 计算》](#)
- [《使用逻辑器件进行设计》](#)

### 12.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

### 12.3 社区资源

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 12.4 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 12.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 12.6 Glossary

[SLYZ022 — TI Glossary](#).

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC74QDRG4Q1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC74Q	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HC74QDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC74Q	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HC74QPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC74Q	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HC74QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC74Q	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and



www.ti.com

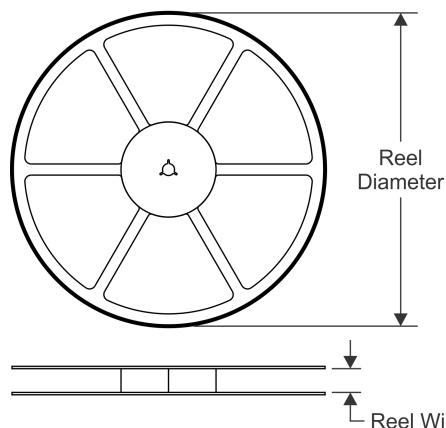
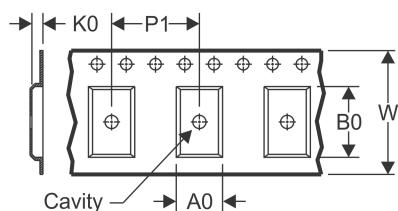
## PACKAGE OPTION ADDENDUM

10-Dec-2020

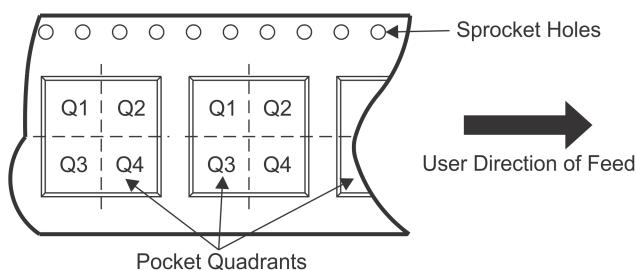
---

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

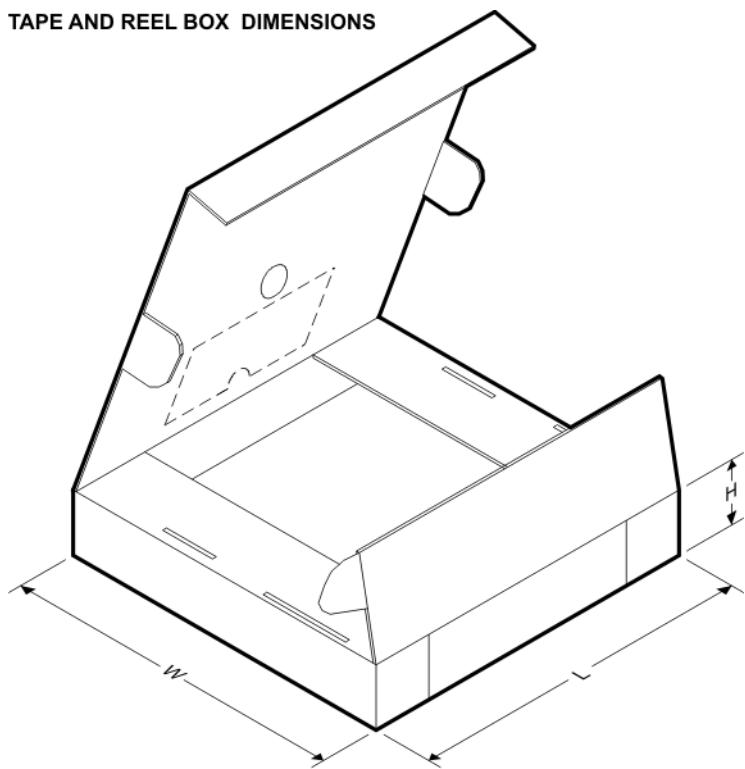
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC74QDRG4Q1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC74QDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC74QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC74QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

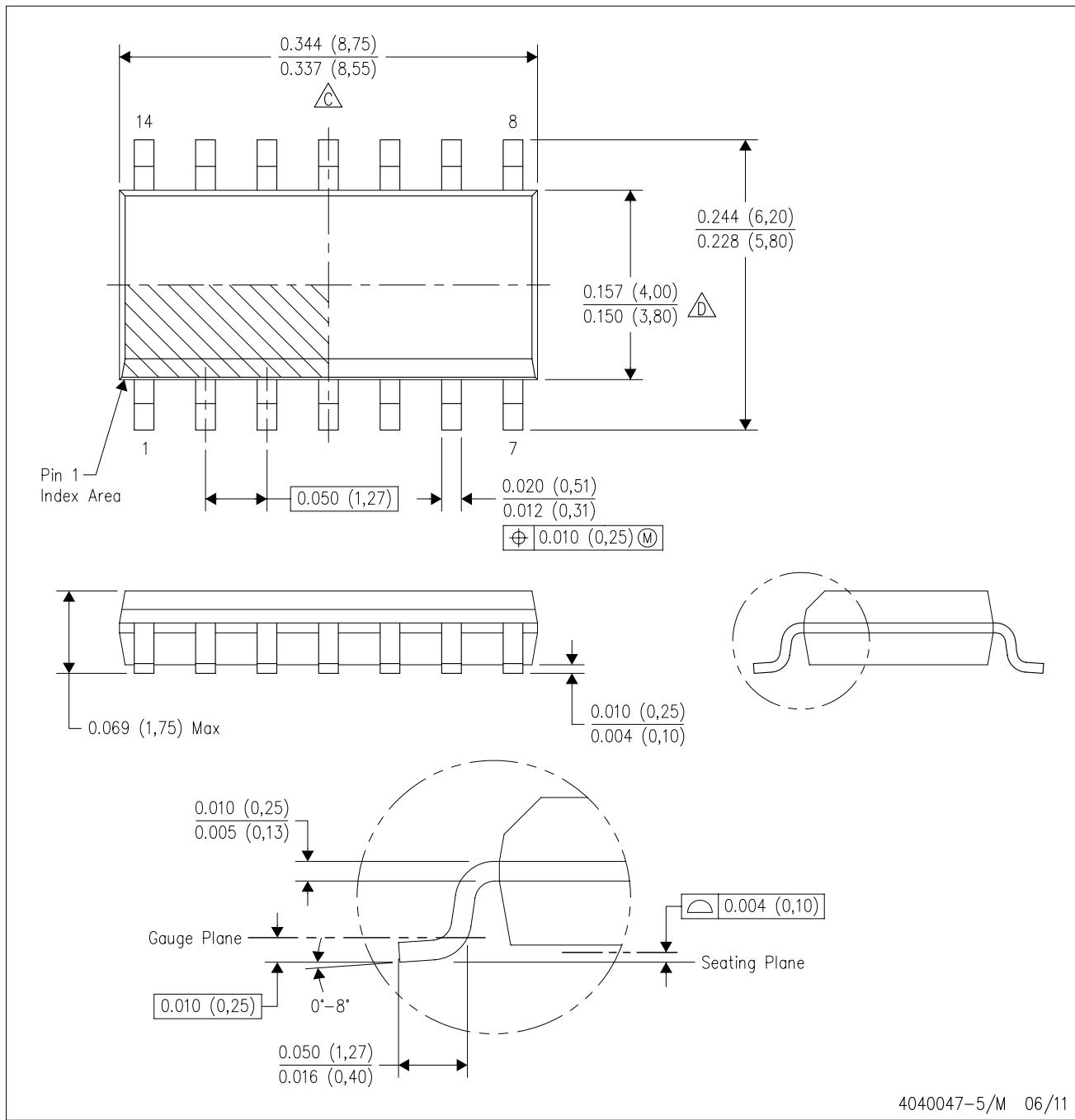
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC74QDRG4Q1	SOIC	D	14	2500	853.0	449.0	35.0
SN74HC74QDRQ1	SOIC	D	14	2500	853.0	449.0	35.0
SN74HC74QPWRG4Q1	TSSOP	PW	14	2000	853.0	449.0	35.0
SN74HC74QPWRQ1	TSSOP	PW	14	2000	853.0	449.0	35.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

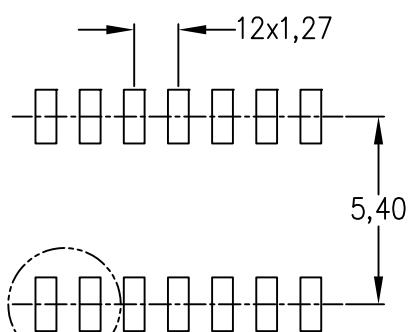
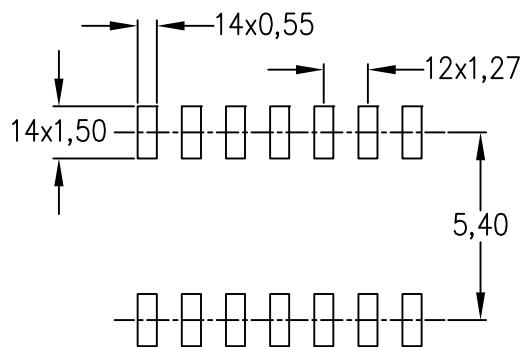
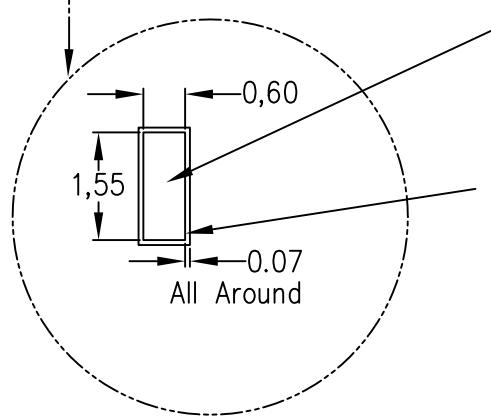
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

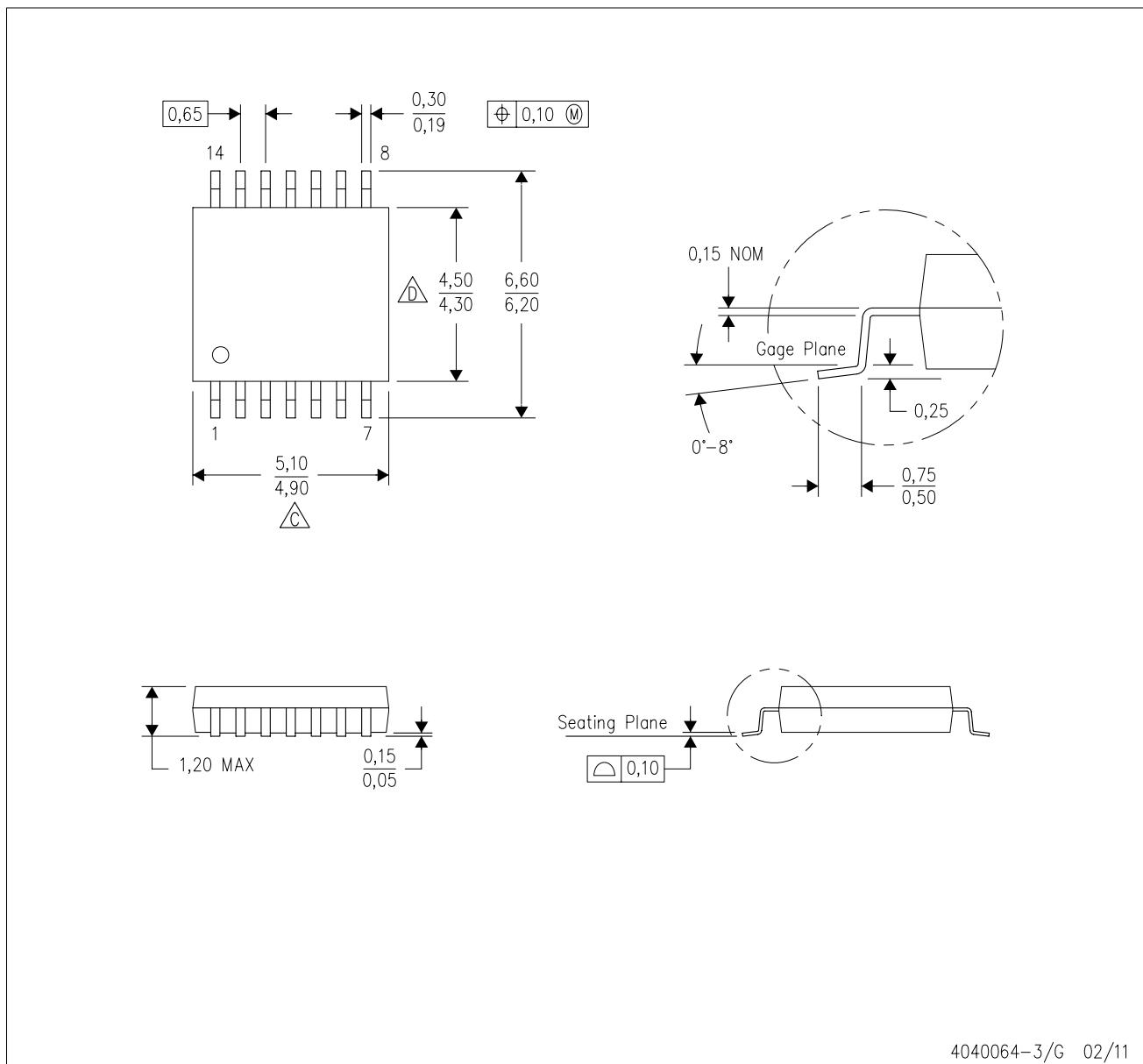
Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

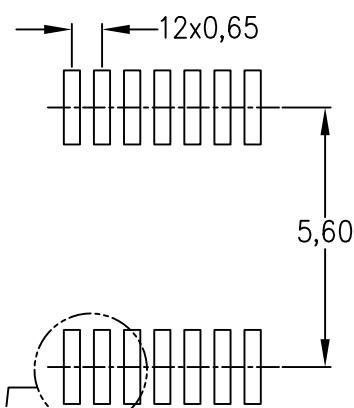
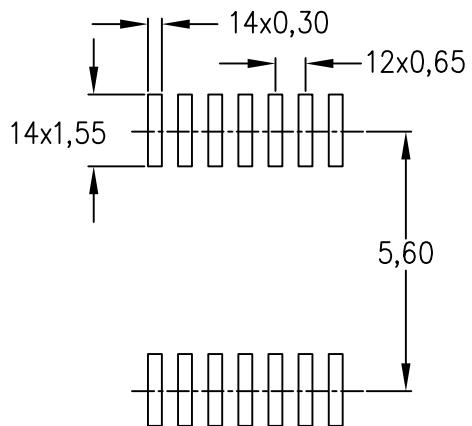
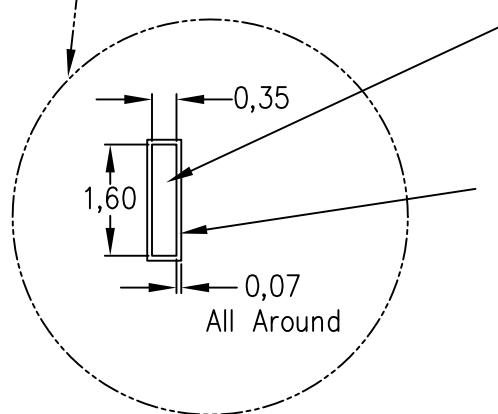
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

4211284-2/G 08/15

## NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## 重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2021, 德州仪器 (TI) 公司