TPS793 Low-Noise, High PSRR, RF, 200-mA Low-Dropout Linear Regulators in NanoStar™ Wafer Chip Scale and SOT-23

1 Features

- 200-mA RF Low-Dropout Regulator With Enable
- Available in Fixed-Voltage Versions from 1.8 V to 4.75 V and Adjustable (1.22 V to 5.5 V)
- High PSRR (70 dB at 10 kHz)
- Low Noise (32 μV_{RMS}, TPS79328)
- Fast Start-Up Time (50 µs)
- Stable With a 2.2-µF Ceramic Capacitor
- Excellent Load and Line Transient Response
- Very Low Dropout Voltage (112 mV at 200 mA, TPS79330)
- 5- and 6-Pin SOT23 (DBV) and NanoStar Wafer Chip Scale (YZQ) Packages

2 Applications

- RF: VCOs, Receivers, ADCs
- Audio
- Cellular and Cordless Telephones
- *Bluetooth*®, Wireless LAN
- Handheld Organizers, PDAs

3 Description

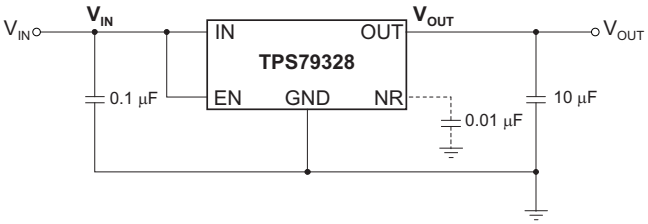
The TPS793 family of low-dropout (LDO) low-power linear voltage regulators features high power-supply rejection ratio (PSRR), ultralow-noise, fast start-up, and excellent line and load transient responses in NanoStar™ wafer chip scale and SOT23 packages. NanoStar packaging gives an ultrasmall footprint as well as an ultralow profile and package weight, making these devices ideal for portable applications such as handsets and PDAs. Each device in the family is stable, with a small, 2.2-µF ceramic capacitor on the output. The TPS793 family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (for example, 112 mV at 200 mA, TPS79330). Each device achieves fast start-up times (approximately 50 µs with a 0.001-µF bypass capacitor) while consuming very low quiescent current (170 µA typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 µA. The TPS79328 exhibits approximately 32 μV_{RMS} of output voltage noise at 2.8-V output with a 0.1-µF bypass capacitor. Applications with analog components that are noise-sensitive, such as portable RF electronics, benefit from the high PSRR and low-noise features as well as the fast response time.

Device Information(1)

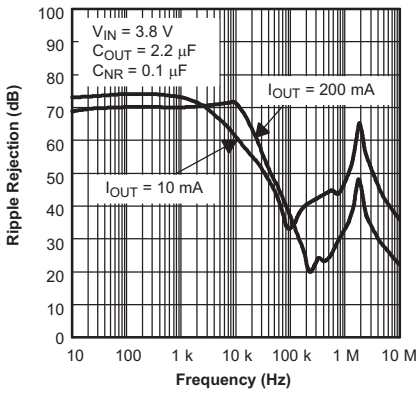
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS793	SOT-23 (6)	2.90 mm × 1.60 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
	DSBGA (5)	1.35 mm × 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



Ripple Rejection vs Frequency



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision K (October 2007) to Revision L — **Page**

- Changed title of data sheet ... 1
- Deleted references to *YEQ* package throughout document (package is obsolete) ... 1
- Changed fourth bullet of *Features* list to *low noise* ... 1
- Changed front-page figure ... 1
- Changed *Absolute Maximum Ratings* condition statement ... 4
- Added *Pin Configurations and Functions* section, ESD Ratings table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 4
- Deleted *Dissipation Ratings* table; added *Thermal Information* table ... 5
- Deleted $T_J = 25°C$ test condition from PSRR specification measurements because of redundancy ... 6
- Added condition statement to *Typical Characteristics* ... 7
- Changed Figure 23; changed capacitor notation to C_{FF} in figure and related table ... 14
- Changed Figure 24; changed capacitor notation to C_{FF} in figure, changed 2.2µF capacitor value to 10µF, and changed device name ... 15

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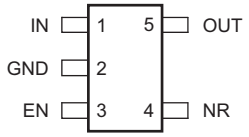
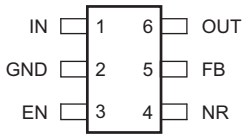
5 Pin Configuration and Functions

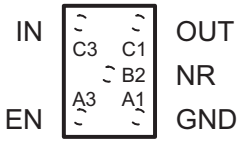
DBV Package
5-Pin SOT-23 Fixed Voltage Version
Top View



DBV Package
6-Pin SOT-23 Adjustable Voltage Version
Top View



YZQ Package
5-Pin DSBGA
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	DBV	YZQ		
EN	3	A3	I	Enable pin. Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
FB	5	—	I	Feedback pin. This terminal is the feedback input pin for the adjustable device. Fixed voltage versions in the DBV package do not have this pin.
GND	2	A1	—	Regulator ground.
IN	1	C3	I	Input to the device.
NR	4	B2	—	Noise Reduction pin. Connecting an external capacitor to this pin filters noise generated by the internal bandgap. This configuration improves power-supply rejection and reduces output noise.
OUT	6	C1	O	Output of the regulator.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted). All voltages are with respect to GND.[1]

			MIN	MAX	UNIT
Voltage	Input, V_{IN}		–0.3	6	V
	Enable, V_{EN}		–0.3	6	V
	Output, V_{OUT}		–0.3	6	V
Current	Peak output, $I_{OUT(max)}$		Internally limited		A
Output short-circuit duration			Indefinite		
Total power dissipation	Continuous, $P_{D(tot)}$		See *Thermal Information*		
Temperature	Junction, T_J	DBV package	–40	150	°C
		YZQ package	–40	125	°C
	Storage, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range	2.7		5.5	V
V_{EN}	Enable supply voltage range	0		V_{IN}	V
V_{OUT}	Output voltage range	V_{FB}		5	V
I_{OUT}	Output current	0		200	mA
T_J	Operating junction temperature	–40		125	°C
C_{IN}	Input capacitor	0.1	1		µF
C_{OUT}	Output capacitor	2.2[1]	10		µF
C_{NR}	Noise reduction capacitor	0	10		nF
C_{FF}	Feed-forward capacitor		15		pF
R_2	Lower feedback resistor		30.1		kΩ

(1) If C_{FF} is not used or $V_{OUT(nom)}$ < 1.8 V, the minimum recommended C_{OUT} = 4.7 µF.

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6.4 Thermal Information

THERMAL METRIC[1]		TPS79301		UNIT
		DBV (SOT-23)	YZQ (DSBGA)	
		6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	225.1	178.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.4	1.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.7	62.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.3	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.8	62.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over recommended operating temperature range T_J = –40°C to 125°C, V_{EN} = V_{IN}, V_{IN} = $V_{OUT(nom)}$ + 1 V[1], I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF (unless otherwise noted). Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range[1]				2.7		5.5	V
I_{OUT}	Continuous output current				0		200	mA
V_{FB}	Internal reference (TPS79301)				1.201	1.225	1.250	V
V_{OUT}	Output voltage range	TPS79301			V_{FB}		5.5 – V_{DO}	V
		TPS79318	0 µA < I_{OUT} < 200 mA, 2.8 V < V_{IN} < 5.5 V		1.764	1.8	1.836	
		TPS79325	0 µA < I_{OUT} < 200 mA, 3.5 V < V_{IN} < 5.5 V		2.45	2.5	2.55	
		TPS79328	0 µA < I_{OUT} < 200 mA, 3.8 V < V_{IN} < 5.5 V		2.744	2.8	2.856	
		TPS793285	0 µA < I_{OUT} < 200 mA, 3.85 V < V_{IN} < 5.5 V		2.793	2.85	2.907	
		TPS79330	0 µA < I_{OUT} < 200 mA, 4 V < V_{IN} < 5.5 V		2.94	3	3.06	
		TPS79333	0 µA < I_{OUT} < 200 mA, 4.3 V < V_{IN} < 5.5 V		3.234	3.3	3.366	
		TPS793475	0 µA < I_{OUT} < 200 mA, 5.25 V < V_{IN} < 5.5 V		4.655	4.75	4.845	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation		V_{OUT} + 1 V < V_{IN} ≤ 5.5 V			0.05	0.12	%/V
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation		0 µA < I_{OUT} < 200 mA, T_J = 25°C			5		mV
V_{DO}	Dropout voltage[2] (V_{IN} = $V_{OUT(nom)}$ – 0.1 V)	TPS79328	I_{OUT} = 200 mA			120	200	mV
		TPS793285	I_{OUT} = 200 mA			120	200	
		TPS79330	I_{OUT} = 200 mA			112	200	
		TPS79333	I_{OUT} = 200 mA			12	180	
		TPS793475	I_{OUT} = 200 mA			77	125	
I_{CL}	Output current limit		V_{OUT} = 0 V		285		600	mA
I_{GND}	Ground pin current		0 µA < I_{OUT} < 200 mA			170	220	µA
$I_{SHUTDOWN}$	Shutdown current[3]		V_{EN} = 0 V, 2.7 V < V_{IN} < 5.5 V			0.07	1	µA
I_{FB}	FB pin current		V_{FB} = 1.8 V				1	µA
PSRR	Power-supply rejection ratio	TPS79328	f = 100 Hz, I_{OUT} = 10 mA			70		dB
			f = 100 Hz, I_{OUT} = 200 mA			68		
			f = 10 kHz, I_{OUT} = 200 mA			70		
			f = 100 kHz, I_{OUT} = 200 mA			43		
V_n	Output noise voltage	TPS79328	BW = 200 Hz to 100 kHz, I_{OUT} = 200 mA	C_{NR} = 0.001 µF		55		μV_{RMS}
				C_{NR} = 0.0047 µF		36		
				C_{NR} = 0.01 µF		33		
				C_{NR} = 0.1 µF		32		
t_{STR}	Startup time	TPS79328	R_L = 14 Ω, C_{OUT} = 1 µF	C_{NR} = 0.001 µF		50		µs
				C_{NR} = 0.0047 µF		70		
				C_{NR} = 0.01 µF		100		
$V_{EN(high)}$	High-level enable input voltage		2.7 V < V_{IN} < 5.5 V		1.7		V_{IN}	V
$V_{EN(low)}$	Low-level enable input voltage		2.7 V < V_{IN} < 5.5 V		0		0.7	V
I_{EN}	EN pin current		V_{EN} = 0 V		–1		1	µA
	UVLO		Threshold, V_{CC} rising		2.25		2.65	V
			Hysteresis			100		mV

(1) Minimum V_{IN} is 2.7 V or V_{OUT} + V_{DO}, whichever is greater.
(2) Dropout is not measured for the TPS79318 and TPS79325 because minimum V_{IN} = 2.7 V.
(3) For adjustable versions, this parameter applies only after V_{IN} is applied; then V_{EN} transitions high to low.

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6.6 Typical Characteristics

Over recommended operating temperature range T_J = –40°C to 125°C, $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF, $V_{OUT(nom)}$ = 2.8 V (unless otherwise noted). Typical values are at T_J = 25°C.

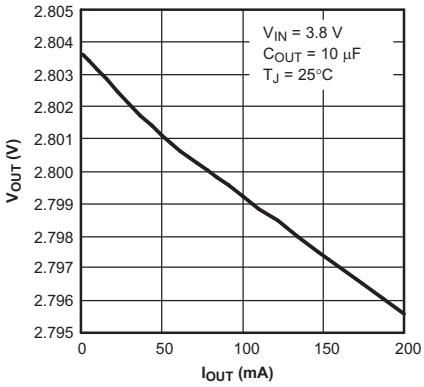

Figure 1. TPS79328 Output Voltage vs Output Current

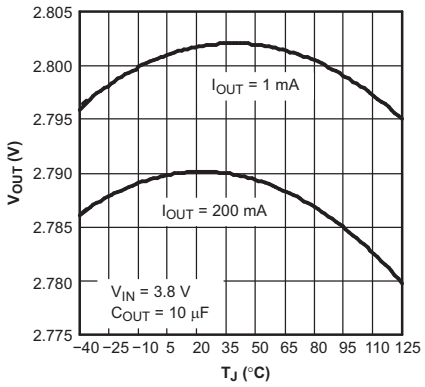

Figure 2. TPS79328 Output Voltage vs Junction Temperature

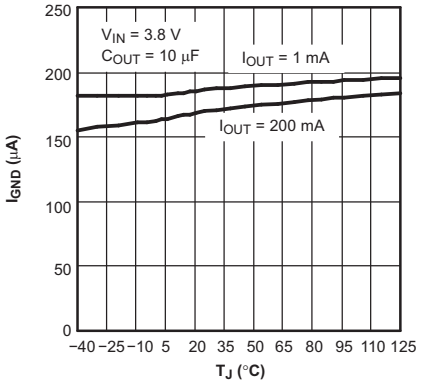

Figure 3. TPS79328 Ground Current vs Junction Temperature

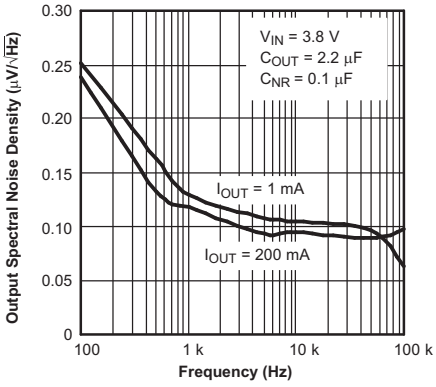

Figure 4. TPS79328 Output Spectral Noise Density vs Frequency

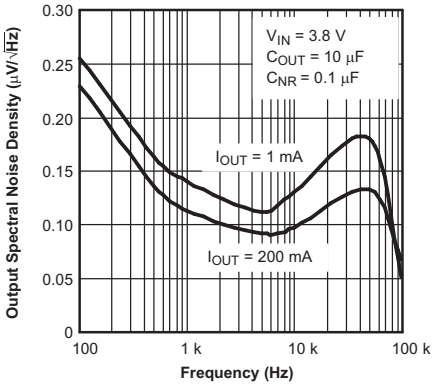

Figure 5. TPS79328 Output Spectral Noise Density vs Frequency

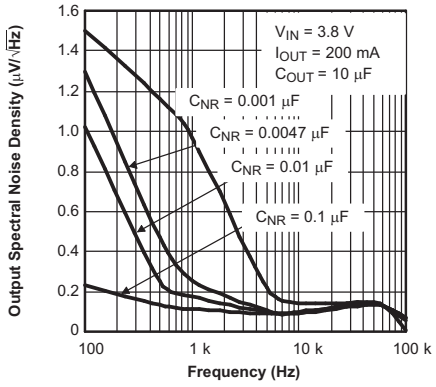

Figure 6. TPS79328 Output Spectral Noise Density vs Frequency

Typical Characteristics (continued)

Over recommended operating temperature range T_J = –40°C to 125°C, V_{EN} = V_{IN}, V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF, $V_{OUT(nom)}$ = 2.8 V (unless otherwise noted). Typical values are at T_J = 25°C.

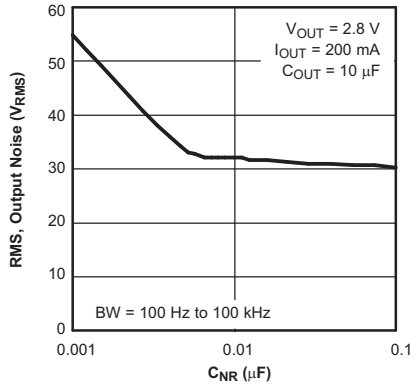

Figure 7. Root Mean Square Output Noise vs C_{NR}

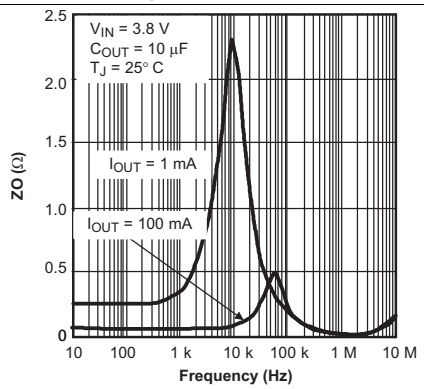

Figure 8. Output Impedance vs Frequency

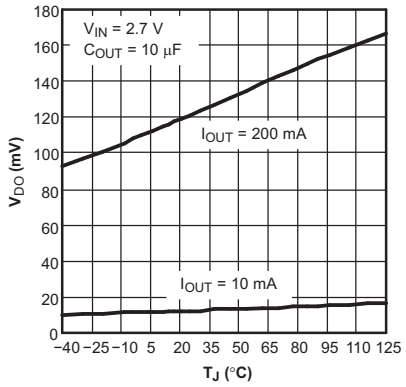

Figure 9. TPS79328 Dropout Voltage vs Junction Temperature

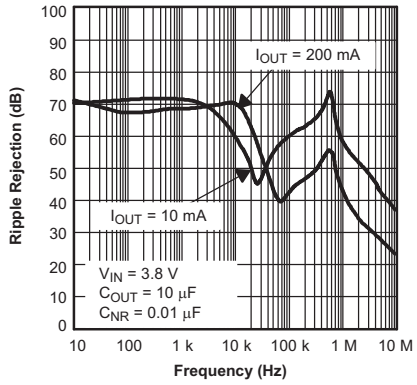

Figure 10. TPS79328 Ripple Rejection vs Frequency

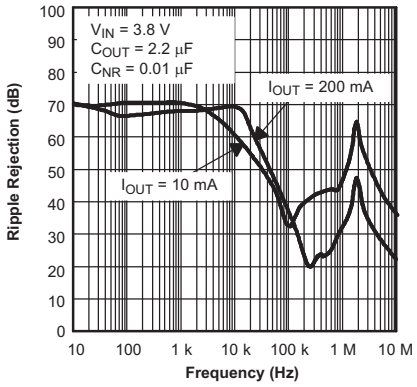

Figure 11. TPS79328 Ripple Rejection vs Frequency

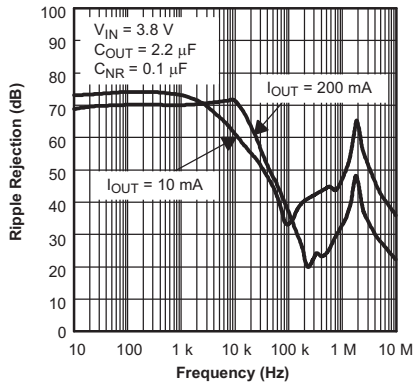

Figure 12. TPS79328 Ripple Rejection vs Frequency

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Typical Characteristics (continued)

Over recommended operating temperature range T_J = –40°C to 125°C, $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF, $V_{OUT(nom)}$ = 2.8 V (unless otherwise noted). Typical values are at T_J = 25°C.

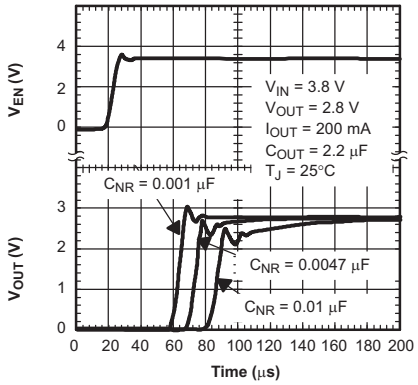

Figure 13. TPS79328 Output Voltage, Enable Voltage vs Time (Start-Up)

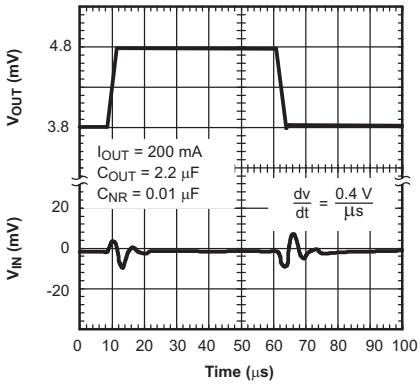

Figure 14. TPS79328 Line Transient Response

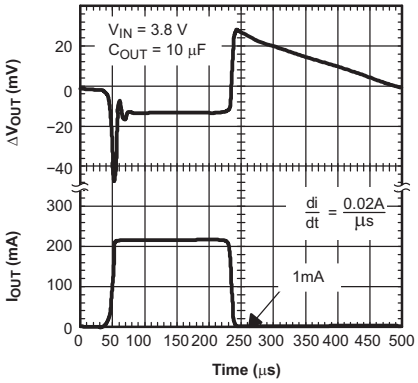

Figure 15. TPS79328 Load Transient Response

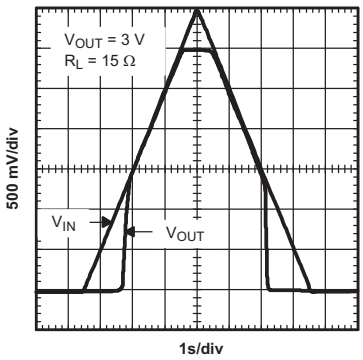

Figure 16. Power-Up and Power-Down

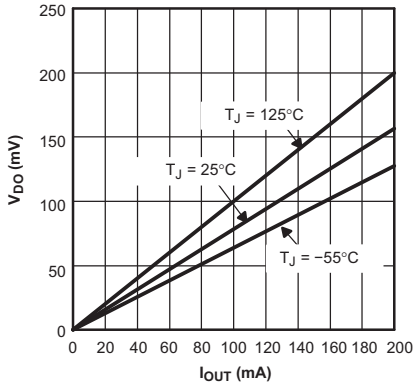

Figure 17. Dropout Voltage vs Output Current

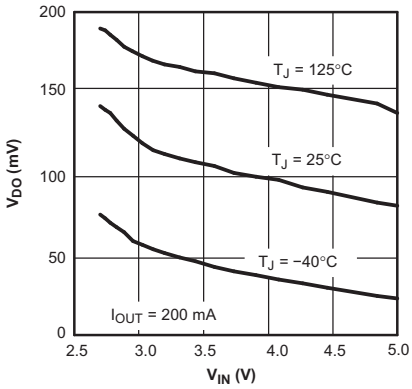

Figure 18. TPS79301 Dropout Voltage vs Input Voltage

Typical Characteristics (continued)

Over recommended operating temperature range T_J = –40°C to 125°C, V_{EN} = V_{IN}, V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF, $V_{OUT(nom)}$ = 2.8 V (unless otherwise noted). Typical values are at T_J = 25°C.

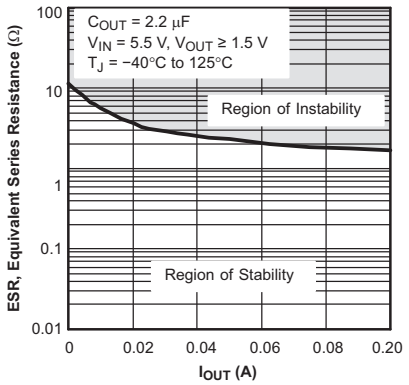

Figure 19. Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

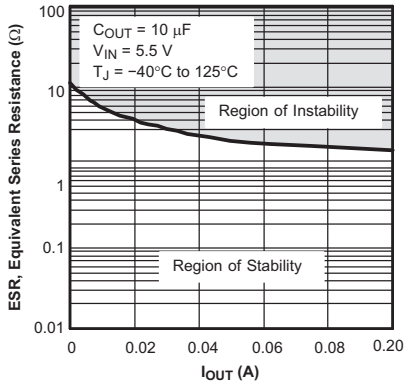

Figure 20. Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

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7 Detailed Description

7.1 Overview

The TPS793 family of LDO regulators has been optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (170 μA typically), and enable-input to reduce supply currents to less than 1 μA when the regulator is turned off.

7.2 Functional Block Diagrams

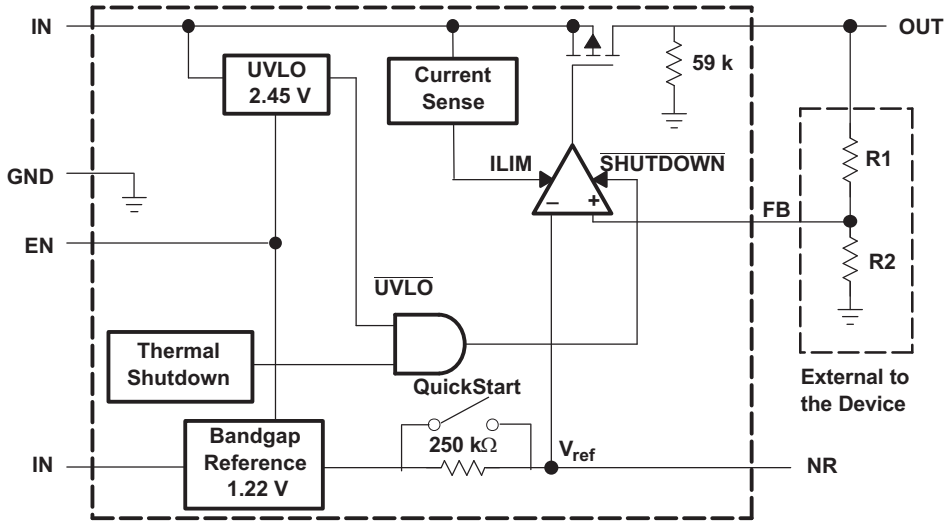

Figure 21. TPS79301 Block Diagram (Adjustable Version)

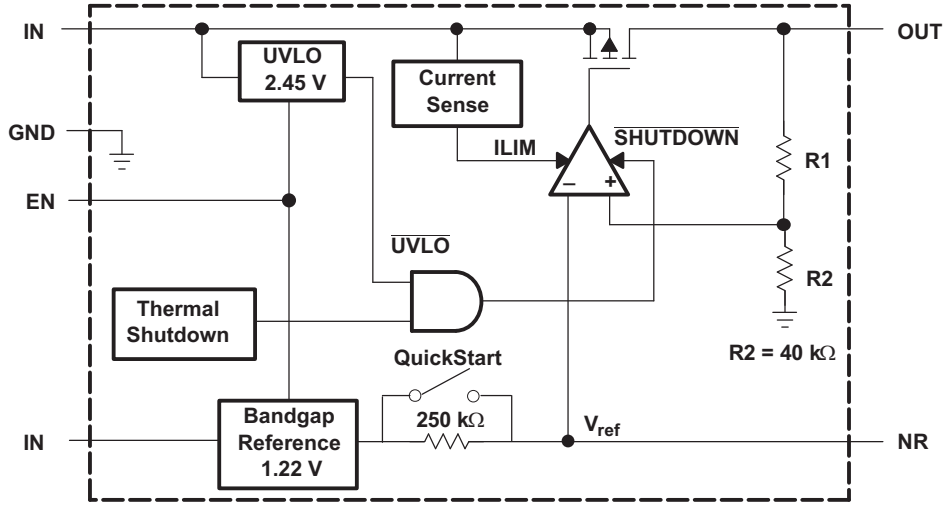

Figure 22. TPS793 Block Diagram (Fixed Version)

7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The TPS793 uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage. This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry, $V_{IN(min)}$.

7.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(high)}$ (1.7 V, minimum). Turn off the device by forcing the EN pin to drop below 0.7 V. If shutdown capability is not required, connect EN to IN.

7.3.3 Foldback Current Limit

The TPS793 features internal current limiting and thermal protection. During normal operation, the TPS793 limits output current to approximately 400 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package or the absolute maximum voltage ratings of the device.

7.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the device from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature must be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TPS793 internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS793 into thermal shutdown degrades device reliability.

7.3.5 Reverse Current Operation

The TPS793 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

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7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(min)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage is greater than $V_{EN(min)}$.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.
- The input voltage is less than $UVLO_{falling}$.

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(high)}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(high)}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	$V_{IN} < UVLO_{falling}$	$V_{EN} < V_{EN(low)}$	—	$T_J > 165°C$ (1)

(1) Approximate value for thermal shutdown.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS793 family of LDO regulators has been optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (170 μA typically), and enable-input to reduce supply currents to less than 1 μA when the regulator is turned off.

8.1.1 Adjustable Operation

The output voltage of the TPS79301 adjustable regulator is programmed using an external resistor divider as shown in Figure 23. The output voltage is calculated using Equation 1:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$$

where:

- V_{REF} = 1.2246 V typ (the internal reference voltage) (1)

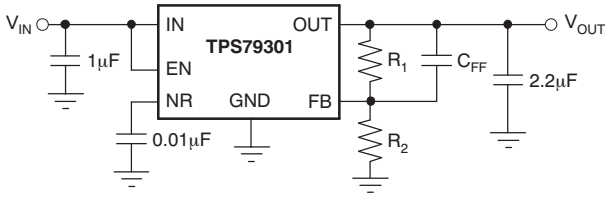
Resistors R_1 and R_2 should be chosen for approximately 50-μA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistors values can cause accuracy issues and other problems. The recommended design procedure is to choose R_2 = 30.1 kΩ to set the divider current at 50 μA, C_{FF} = 15 pF for stability, and then calculate R_1 using Equation 2:

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_2 \quad (2)$$

To improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between OUT and FB. For output voltages less than 1.8 V, the value of this capacitor should be 100 pF. For output voltages greater than 1.8 V, the approximate value of this capacitor can be calculated as shown in Equation 3:

$$C_{FF} = \frac{(3 \times 10^{-7}) \times (R_1 + R_2)}{(R_1 \times R_2)} \quad (3)$$

The suggested value of this capacitor for several resistor ratios is shown in the table in Figure 23. If this capacitor is not used (such as in a unity-gain configuration) or if an output voltage less than 1.8 V is chosen, then the minimum recommended output capacitor is 4.7 μF instead of 2.2 μF.



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R_1	R_2	C_{FF}
1.22V	short	open	0pF
2.5V	31.6kΩ	30.1kΩ	22pF
3.3V	51kΩ	30.1kΩ	15pF
3.6V	59kΩ	30.1kΩ	15pF

Figure 23. TPS79301 Adjustable LDO Regulator Programming

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8.2 Typical Application

A typical application circuit is shown in Figure 24.

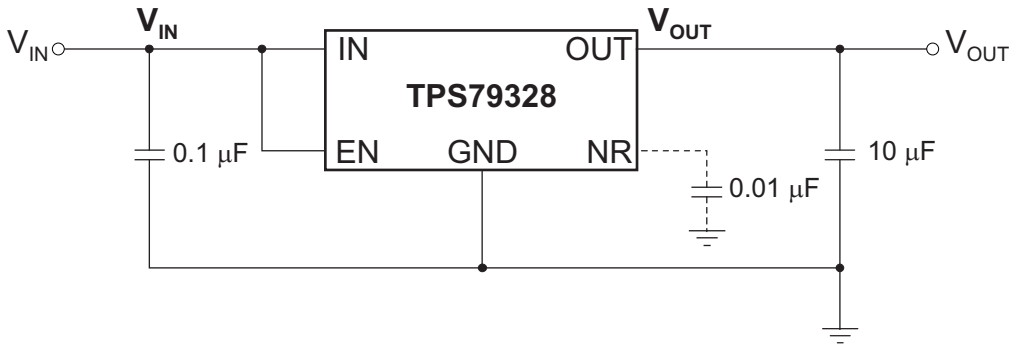

Figure 24. Typical Application Circuit

8.2.1 Design Requirements

Table 2 lists the design requirements.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	4.2 V to 3 V (Lithium Ion battery)
Output voltage	1.8 V, ±1%
DC output current	10 mA
Peak output current	75 mA
Maximum ambient temperature	65°C

8.2.2 Detailed Design Procedure

Pick the desired output voltage option. An input capacitor of 0.1 µF is used as the battery is connected to the input through a via and a short 10-mil (0.01-in) trace. An output capacitor of 10 µF is used to provide optimal response time for the load transient. Verify that the maximum junction temperature is not exceed by referring to Figure 30.

8.2.2.1 Capacitor Recommendations

Low equivalent series resistance (ESR) capacitors should be used for the input, output, noise reduction, and bypass capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved over-temperature performance, while ceramic X5R capacitors are more cost-effective and are available in higher values.

8.2.2.2 Input and Output Capacitor Requirements

A 0.1-µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS793, is required for stability and improves transient response, noise rejection, and ripple rejection. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated or the device is located several inches from the power source.

Like most low-dropout regulators, the TPS793 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 2.2 µF. Any 2.2-µF or larger ceramic capacitor is suitable, provided the capacitance does not vary significantly over temperature. If load current is not expected to exceed 100 mA, a 1.0-µF ceramic capacitor can be used. If a feed-forward capacitor is not used (such as in a unity-gain configuration) or if an output voltage less than 1.8 V is chosen, then the minimum recommended output capacitor is 4.7 µF instead of 2.2 µF. Table 3 lists the recommended output capacitor sizes for several common configurations.

Table 3. Output Capacitor Sizing

Condition	C_{OUT} (µF)
V_{OUT} < 1.8 V or C_{FF} = 0 nF	4.7
V_{OUT} > 1.8 V, I_{OUT} > 100 mA	2.2
V_{OUT} > 1.8 V, I_{OUT} < 100 mA	1

8.2.2.3 Noise Reduction and Feed-Forward Capacitor Requirements

The internal voltage reference is a key source of noise in an LDO regulator. The TPS793 has an NR pin which is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor, thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor should be no more than 0.1 µF to ensure that it is fully charged during the quickstart time provided by the internal switch shown in the *Functional Block Diagrams*.

As an example, the TPS79328 exhibits only 32 μV_{RMS} of output voltage noise using a 0.1-µF ceramic bypass capacitor and a 2.2-µF ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases due to the RC time constant at the NR pin that is created by the internal 250-kΩ resistor and external capacitor. This RC time constant is affected by the quick-start circuit, especially for values near or below 10 nF. See Figure 13 for a comparisons of C_{NR} capacitors and startup times.

A feed-forward capacitor is recommended to improve the stability of the device. If R_2 = 30.1 kΩ, set C_1 to 15 pF for optimal performance. For voltages less than 1.8 V, the value of this capacitor should be 100 pF. For voltages greater than 1.8 V, the approximate value of this capacitor can be calculated as shown in Equation 3.

8.2.3 Application Curves

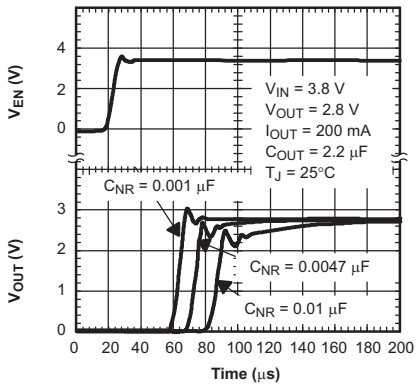

Figure 25. TPS79328 Output Voltage, Enable Voltage vs Time (Start-Up)

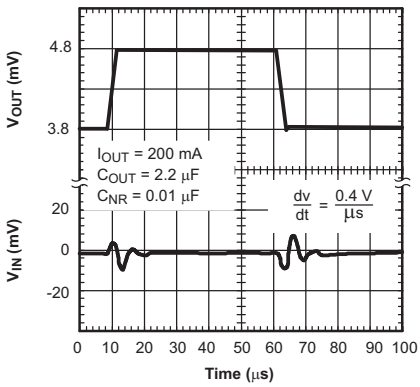

Figure 26. TPS79328 Line Transient Response

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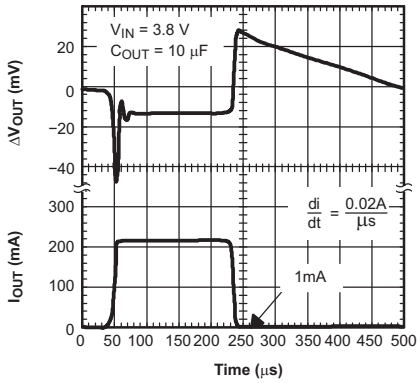

Figure 27. TPS79328 Load Transient Response

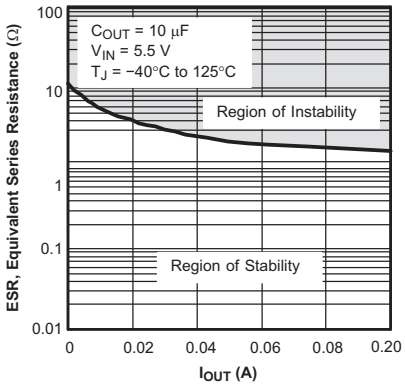

Figure 28. Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

8.3 Do's and Don'ts

Do place at least one, low ESR, 2.2-µF capacitor as close as possible between the OUT pin of the regulator and the GND pin.

Do place at least one, low ESR, 0.1-µF capacitor as close as possible between the IN pin of the regulator and the GND pin.

Do provide adequate thermal paths away from the device.

Do not place the input or output capacitor more than 10 mm away from the regulator.

Do not exceed the absolute maximum ratings.

Do not float the Enable (EN) pin.

Do not resistively or inductively load the NR pin.

Do not let the output voltage get more than 0.3 V above the input voltage.

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range from 2.7 V to 5.5 V. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well-regulated and stable. A 0.1-µF input capacitor is required for stability; if the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

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10 Layout

10.1 Layout Guidelines

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with an X5R or X7R dielectric.

Equivalent series inductance (ESL) and equivalent series resistance (ESR) must be minimized to maximize performance and ensure stability. Every capacitor (C_{IN}, C_{OUT}, $C_{NR/SS}$, C_{FF}) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because these circuits may impact system performance negatively, and even cause instability.

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac measurements like PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

10.2 Layout Example

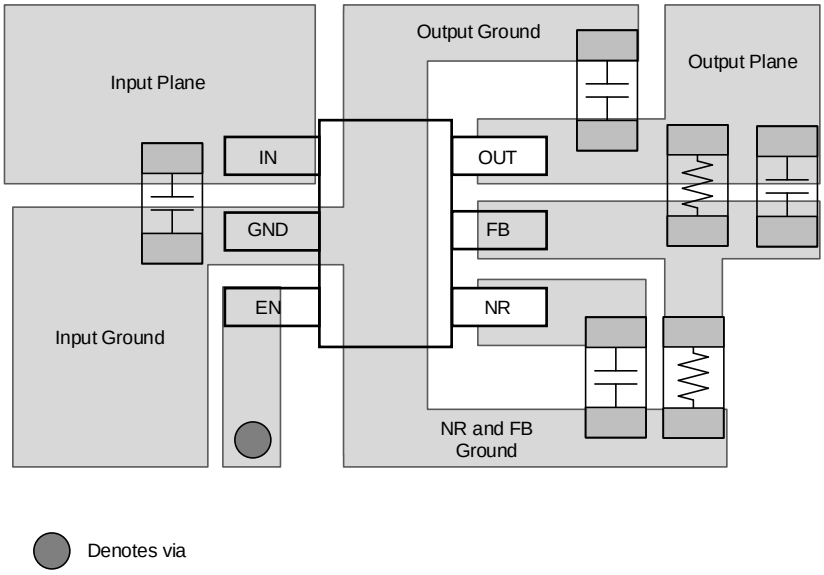

Figure 29. Layout Example (DBV Package)

10.3 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in *Thermal Information*. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) can be approximated by the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 4.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{4}$$

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Power Dissipation (continued)

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

Figure 30 shows the maximum ambient temperature versus the power dissipation of the TPS730. This figure assumes the device is soldered on a JEDEC standard, high-K layout with no airflow over the board. Actual board thermal impedances vary widely. If the application requires high power dissipation, having a thorough understanding of the board temperature and thermal impedances is helpful to ensure the TPS730 does not operate above a junction temperature of 125°C.

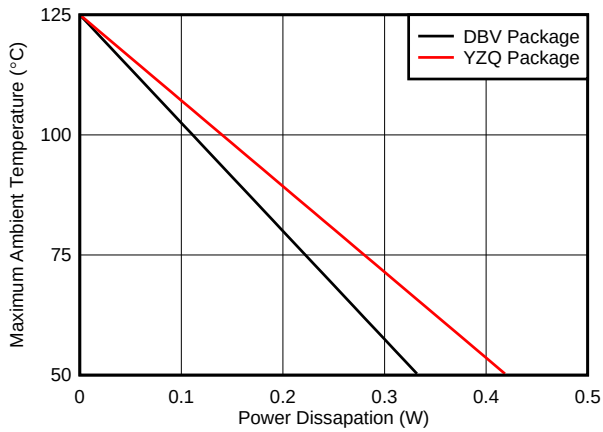

Figure 30. Maximum Ambient Temperature vs Power Dissipation

Estimating the junction temperature can be done by using the thermal metrics Ψ_{JT} and Ψ_{JB}, shown in *Thermal Information*. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with Equation 5.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$

$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D$$

where

- P_D is the power dissipation shown by Equation 4.
- T_T is the temperature at the center-top of the IC package.
- T_B is the PCB temperature measured 1 mm away from the IC package *on the PCB surface*. (5)

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

Seven evaluation modules (EVMs) are available to assist in the initial circuit performance evaluation using the TPS793:

- TPS79301EVM
- TPS79318YEQEVM
- TPS79325YEQEVM
- TPS793285YEQEVM
- TPS79328EVM
- TPS79328YEQEVM
- TPS79330YEQEVM

These EVMs can be requested at the Texas Instruments website through the device product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS793 is available through the product folders under *Tools & Software*.

11.1.2 Device Nomenclature

Table 4. Ordering Information(1)(2)

PRODUCT	V_{OUT}
TPS793**xx***yyy***z**	**XX(X)** is the nominal output voltage (for example, 28 = 2.8 V; 285 = 2.85 V; 01 = adjustable version). **YYY** is the package designator. **Z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 1.2 V to 4.8 V in 50-mV increments are available. Contact the factory for details and availability.

11.2 Documentation Support

11.2.1 Related Documentation

- Application note, *Using New Thermal Metrics*, SBVA025.
- Application note, *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator*, SBVA042.
- *TPS793xxYEQEVM User's Guide*, SBVU001.
- *TPS79301EVM, TPS79328EVM LDO Linear Regulator Evaluation Module User's Guide*, SLVU060A.

11.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.4 Trademarks

NanoStar, E2E are trademarks of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HPA01085DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHJI	Samples
TPS79301DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGVI	Samples
TPS79301DBVRG4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGVI	Samples
TPS79301DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGVI	Samples
TPS79318DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHHI	Samples
TPS79318DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHHI	Samples
TPS79318DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHHI	Samples
TPS79318DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHHI	Samples
TPS79318YZQR	ACTIVE	DSBGA	YZQ	5	3000	TBD	Call TI	Call TI	-40 to 125	E3	Samples
TPS79318YZQT	ACTIVE	DSBGA	YZQ	5	250	TBD	Call TI	Call TI	-40 to 125	E3	Samples
TPS79325DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGWI	Samples
TPS79325DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGWI	Samples
TPS79325YZQR	ACTIVE	DSBGA	YZQ	5	3000	TBD	Call TI	Call TI	-40 to 125	E4	Samples
TPS793285DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHII	Samples
TPS793285DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHII	Samples
TPS79328DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGXI	Samples
TPS79328DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGXI	Samples
TPS79328YZQR	ACTIVE	DSBGA	YZQ	5	3000	TBD	Call TI	Call TI	-40 to 125	E2	Samples
TPS79328YZQT	ACTIVE	DSBGA	YZQ	5	250	TBD	Call TI	Call TI	-40 to 125	E2	Samples
TPS79330DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGYI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79330DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGYI	Samples
TPS79330YZQR	ACTIVE	DSBGA	YZQ	5	3000	TBD	Call TI	Call TI	-40 to 125	E6	Samples
TPS79330YZQT	ACTIVE	DSBGA	YZQ	5	250	TBD	Call TI	Call TI	-40 to 125	E6	Samples
TPS79333DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHUI	Samples
TPS79333DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHUI	Samples
TPS793475DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHJI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS793 :

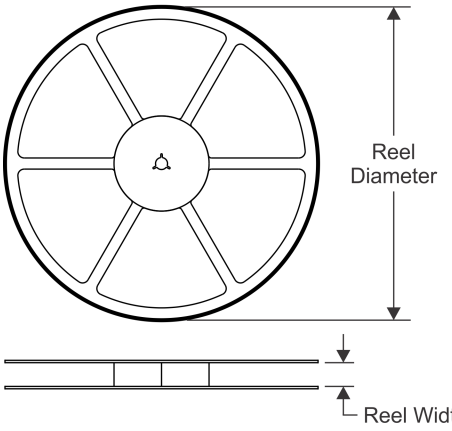
- Automotive : TPS793-Q1

NOTE: Qualified Version Definitions:

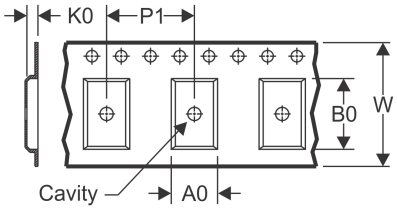
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

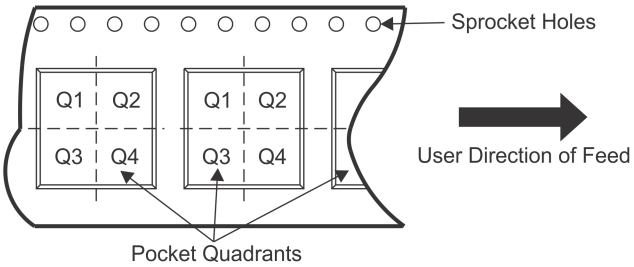


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

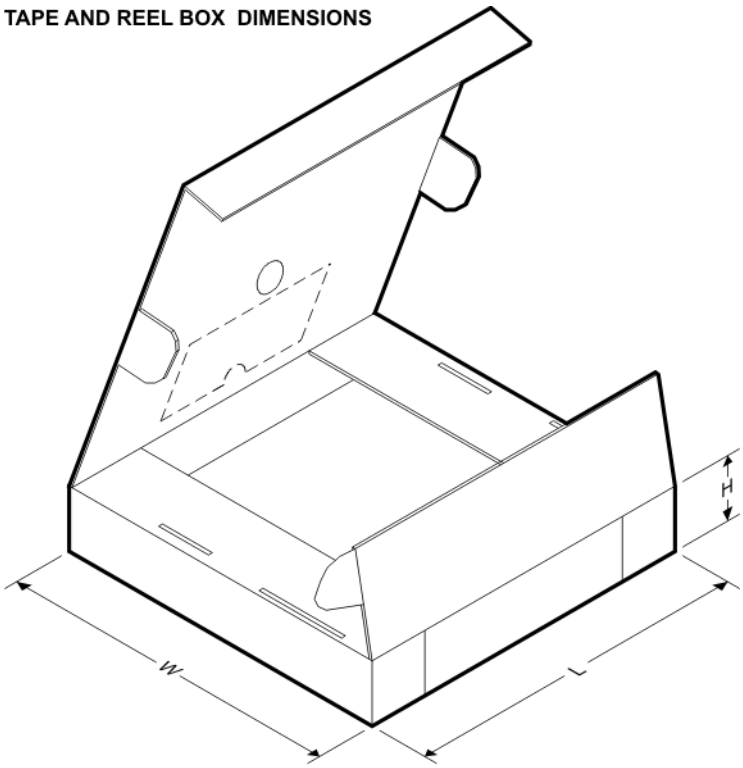
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

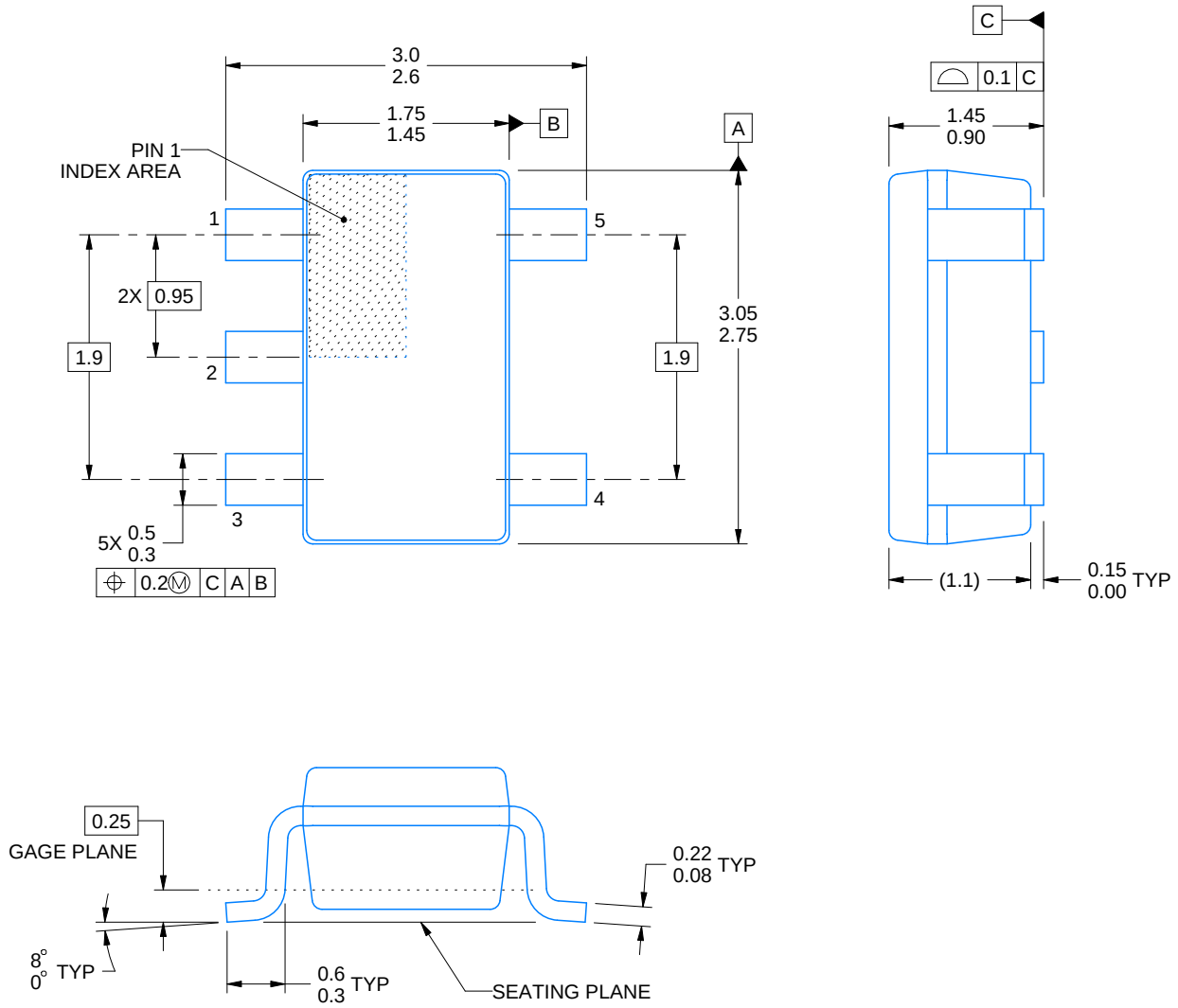
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79301DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79301DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79318DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79318DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79325DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS793285DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS793285DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79328DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79330DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79333DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79333DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS793475DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS793475DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

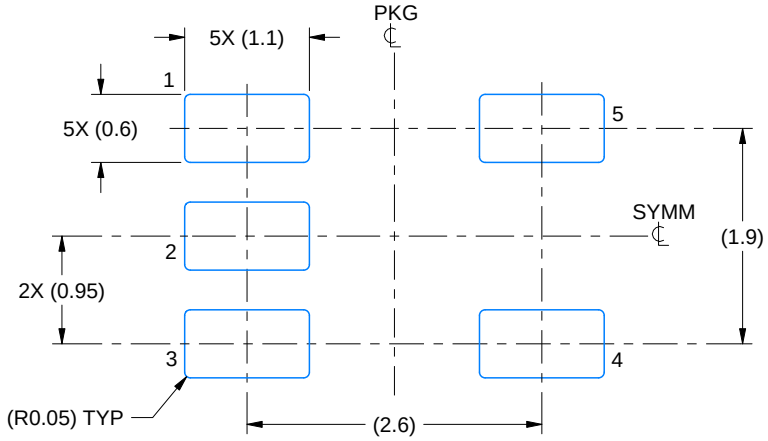
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79301DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS79301DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS79318DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS79318DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS79325DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS793285DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS793285DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS79328DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS79330DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS79333DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS79333DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS793475DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS793475DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0



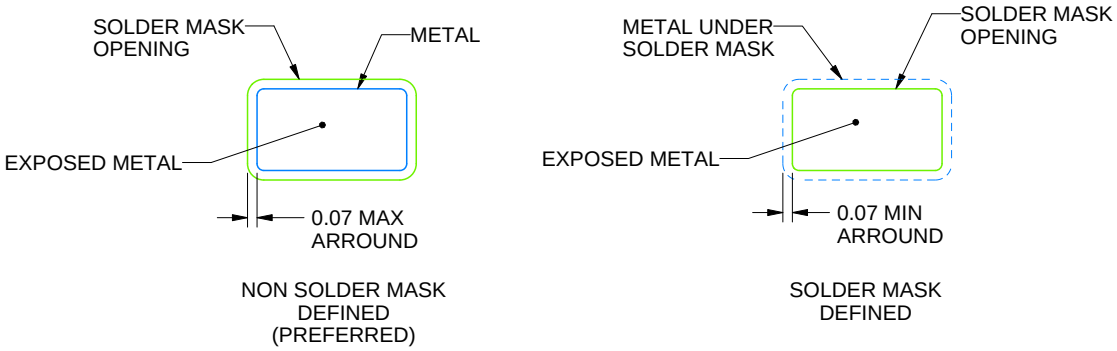
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

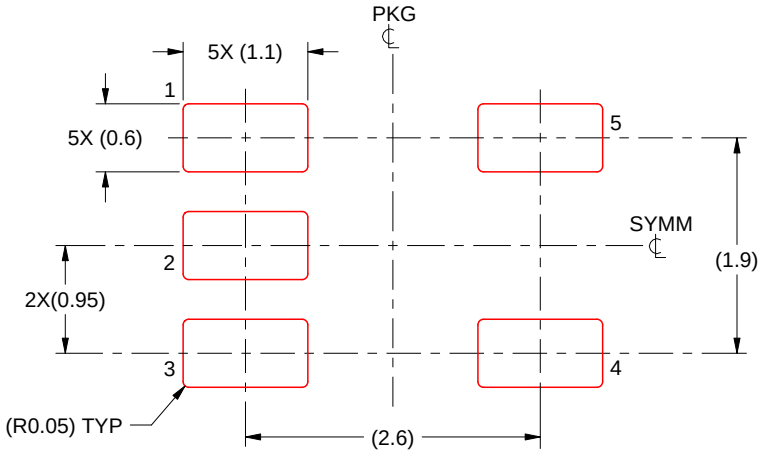


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



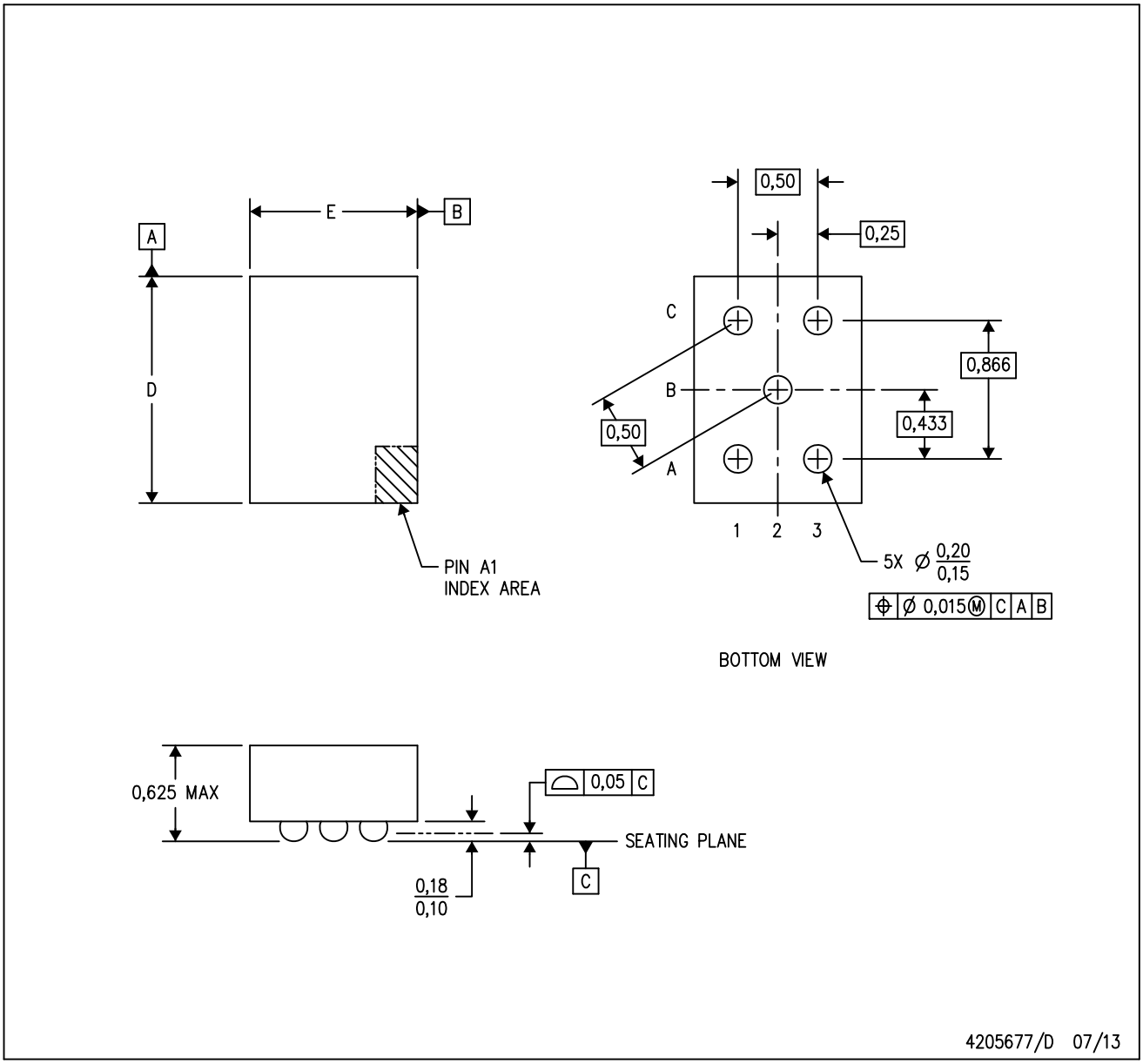
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

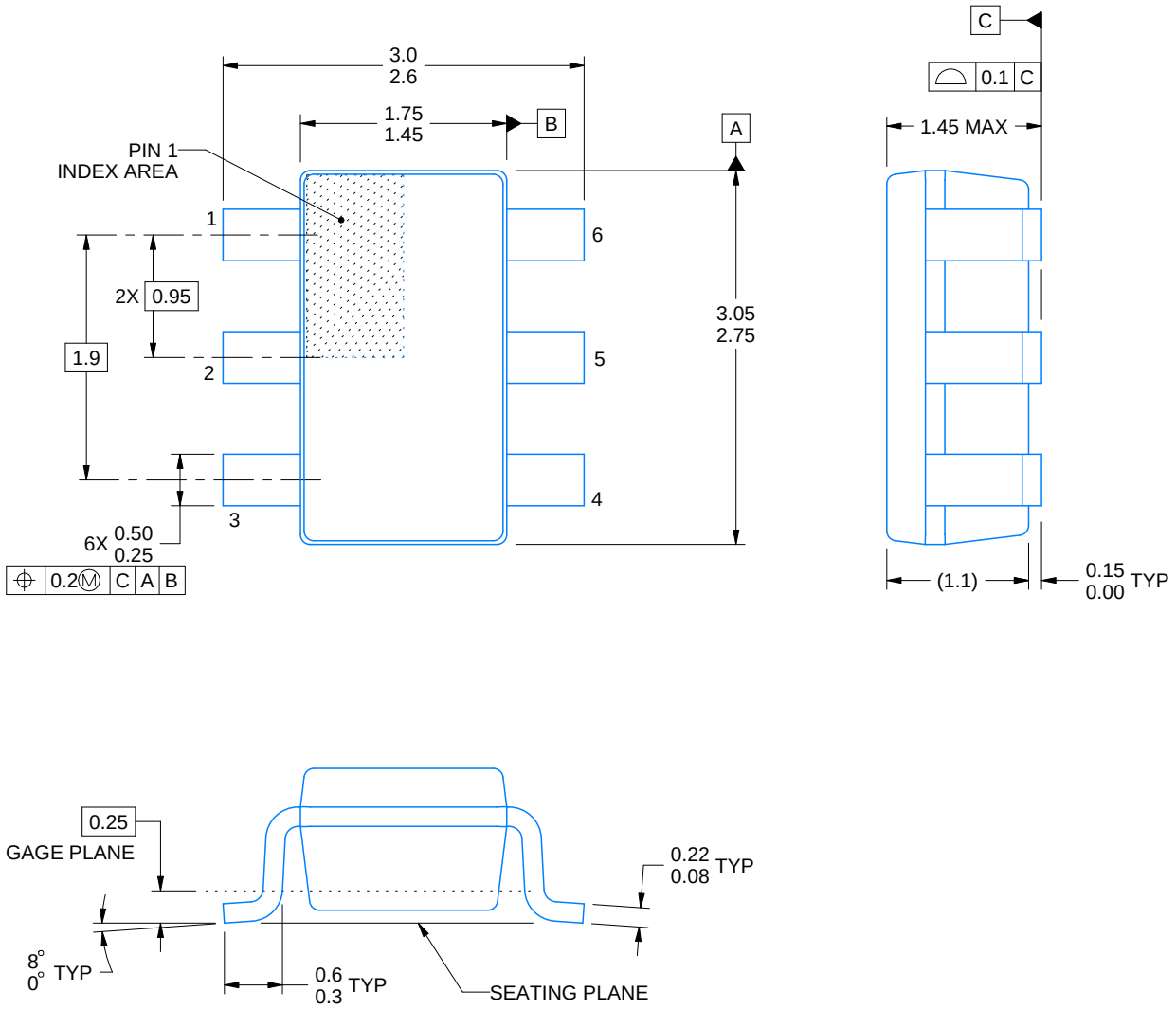
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

YZQ (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



Notes: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree ™ package configuration.

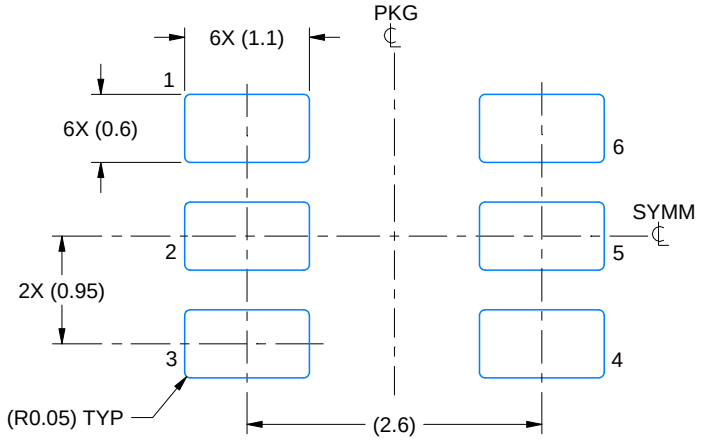
NanoFree is a trademark of Texas Instruments.



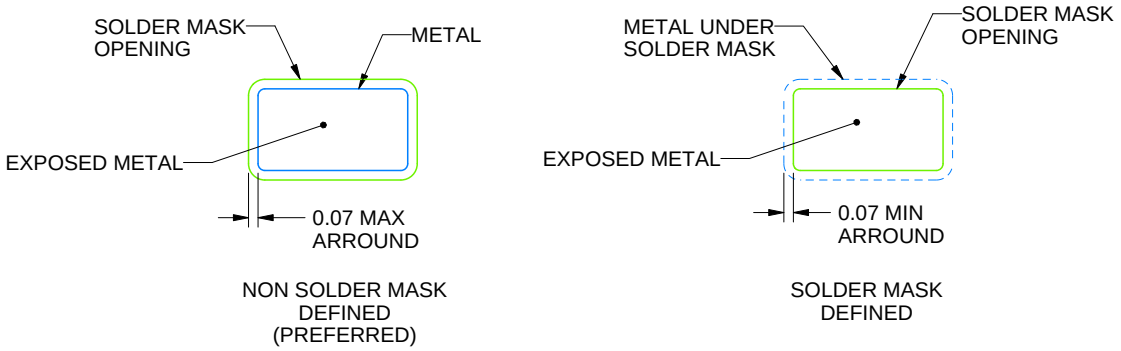
4214840/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

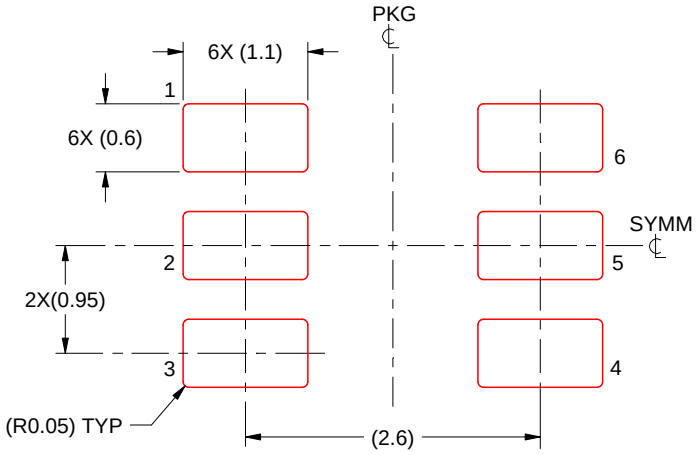


SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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