采用 SC70 封装的 TMP300 1.8V 电阻器可编程温度开关和模拟输出温度传感器

1 特性

- 精度：±1°C（典型值为 +25°C）
- 可编程跳闸点
- 可编程迟滞：5°C/10°C
- 漏极开路输出
- 低功耗：110µA（最大值）
- 宽电压范围：+1.8V 至 +18V
- 温度范围：–40°C 至 +125°C
- 模拟输出：10mV/°C
- SC70-6 以及 SOT23-6 封装

2 应用

- 电源系统
- 直流/直流模块
- 过热监控
- 电子保护系统

3 说明

TMP300 是一款低功率、电阻器可编程、数字输出温度开关。可通过添加外部电阻器设置器件阈值点。提供两种等级的迟滞。TMP300 有一个 V_{TEMP} 模拟输出，此输出能被用做一个测试点或者被用于温度补偿环路。

TMP300 电源电压低至 1.8V 并且电流消耗较低，因此非常适合功耗敏感型系统。

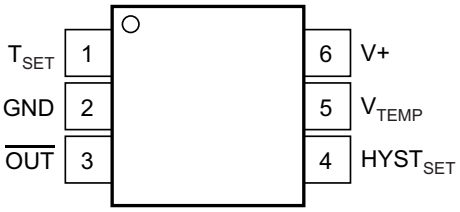
该器件采用具有经证实的热特性的 2 个微封装，可为需要简单可靠热管理的用户提供完整、简单的解决方案。

器件信息(1)

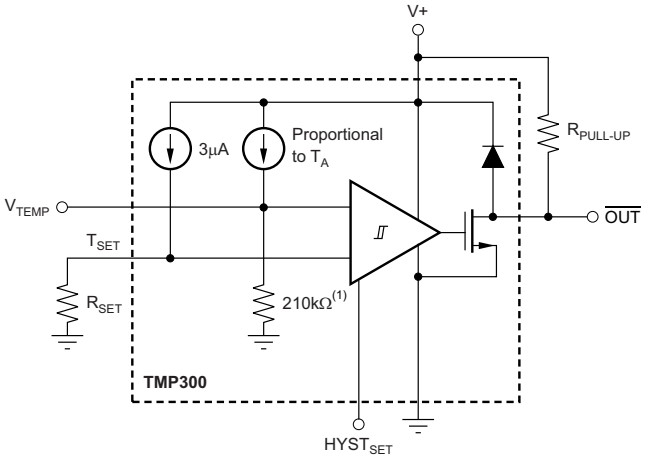
器件型号	封装	封装尺寸（标称值）
TMP300	SOT-23 (6)	2.90mm × 1.60mm
	SC70 (6)	2.00mm × 1.25mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

引脚分配



应用原理图



注意：(1) 薄膜电阻器精度误差大约为 10%，但是该精度误差在出厂时已经过校准。

目录

4 修订历史记录

Changes from Revision D (January 2016) to Revision E **Page**

- Added *Pin Configuration and Functions* section ... 3

Changes from Revision C (January 2011) to Revision D **Page**

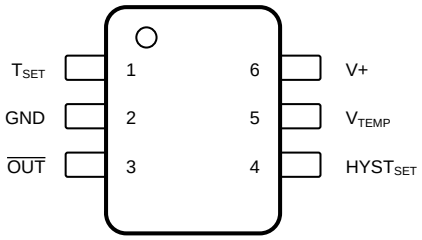
- 添加了*器件信息* 表、*ESD 额定值* 表、*特性* *说明* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1
- 更改了*温度范围* 特性 项目符号 ... 1
- 为引脚增加了封装名称 ... 1
- Deleted *Ordering Information* table ... 4
- Changed Temperature Range, *TA, Functional Range* parameter name in *Electrical Characteristics* table ... 5
- Added footnote 4 to *Electrical Characteristics* table ... 5

Changes from Revision B (November 2008) to Revision C **Page**

- 已删除 将第二句话从*说明*部分删除 ... 1
- Added TMP300B grade device specifications to *Electrical Characteristics* table ... 5

5 Pin Configuration and Functions

DCK and DBV Package
6-Pin SOT-23 and SC70
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
T_{SET}	1	I	Temperature set pin. Connects to a resistor to set the trip point
GND	2	—	Ground
$\overline{OUT}$	3	O	Trip output
$HYST_{SET}$	4	I	Hystersis Set. Connect to Ground for 5°C hysteresis or connect to V+ for 10°C hysteresis
V_{TEMP}	5	I	Analog Temperature output
V+	6	O	Supply voltage: 1.8 V to 18 V

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
V+	Supply voltage		+18	V
	Signal input pins, voltage(2)	–0.5	(V+) + 0.5	V
	Signal input pins, current(2)	–10	10	mA
I_{SC}	Output short-circuit(3)	Continuous		
	Open-drain output		(V+) + 0.5	V
T_A	Functional temperature	–40	+150	°C
T_{stg}	Storage temperature	–55	+150	°C
T_J	Junction temperature		+150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.
(3) Short-circuit to ground.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)	±4000	V
		Charged-device model (CDM)	±1000	

6.3 Electrical Characteristics

At V_S = 3.3V and T_A = –40°C to +125°C, unless otherwise noted.

PARAMETER			TEST CONDITIONS	TMP300			TMP300B			UNIT
				MIN(1)	TYP(1)	MAX(1)	MIN	TYP	MAX	
TEMPERATURE MEASUREMENT										
Measurement range			V_S = 2.35V to 18V	–40		+125	–40		+125	°C
			V_S = 1.8V to 2.35V	–40		100 × (V_S – 0.95)	–40		100 × (V_S – 0.95)	
TRIP POINT										
Total accuracy			T_A = –40°C to +125°C		±2	±4(2)		±2	±6	°C
R_{SET} equation			T_C is in °C		R_{SET} = 10 (50 + T_C)/3			R_{SET} = 10 (50 + T_C)/3		kΩ
HYSTERESIS SET INPUT										
LOW threshold						0.4			0.4	V
HIGH threshold				V_S – 0.4			V_S – 0.4			V
Threshold hysteresis			$HYST_{SET}$ = GND		5			5		°C
			$HYST_{SET}$ = V_S		10			10		
DIGITAL OUTPUT										
Logic family					CMOS			CMOS		
Open-drain leakage current			OUT = V_S			10			10	µA
V_{OL}	Logic levels		V_S = 1.8V to 18V, I_{SINK} = 5mA			0.3			0.3	V
ANALOG OUTPUT										
Accuracy					±2	±3		±2	±5	°C
Temperature sensitivity					10			10		mV/°C
Output voltage			T_A = +25°C	720	750	780	720	750	780	mV
V_{TEMP} pin output resistance					210			210		kΩ
POWER SUPPLY										
I_Q	Quiescent current(3)		V_S = 1.8V to 18V, T_A = –40°C to +125°C			110			110	µA
TEMPERATURE RANGE										
T_A	Specified range		V_S = 2.35V to 18V	–40		+125	–40		+125	°C
			V_S = 1.8V to 2.35V	–40		100 × (V_S – 0.95)	–40		100 × (V_S – 0.95)	
	Functional range(4)		V_S = 2.35V to 18V	–40		+150	–40		+150	
			V_S = 1.8V to 2.35V	–50		100 × (V_S – 0.95)	–50		100 × (V_S – 0.95)	
θ_{JA}	Thermal resistance	SC70			250			250		°C/W
		SOT23-6			180			180		

(1) 100% of production is tested at T_A = +85°C. Specifications over temperature range are ensured by design.
(2) Shaded cells indicate characteristic performance difference.
(3) See Figure 1 for typical quiescent current.
(4) The TMP300 is functional over this range and no indication of performance is implied.

6.4 Typical Characteristics

At V_S = 5V, unless otherwise noted.

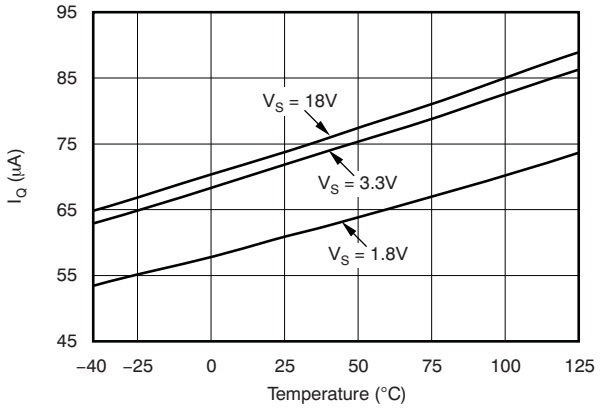


Figure 1. Quiescent Current Over Temperature and Supply

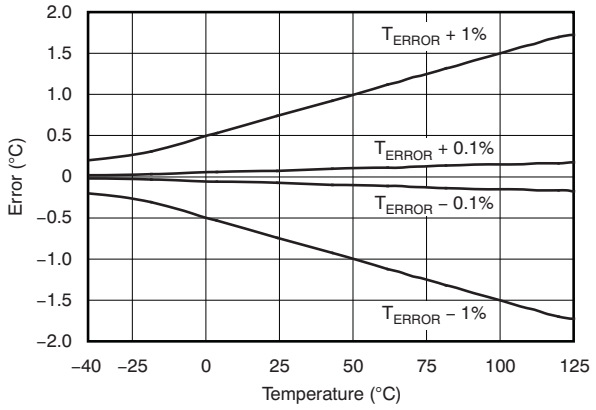


Figure 2. R_{SET} Shift Resulting From R_{SET} Tolerance

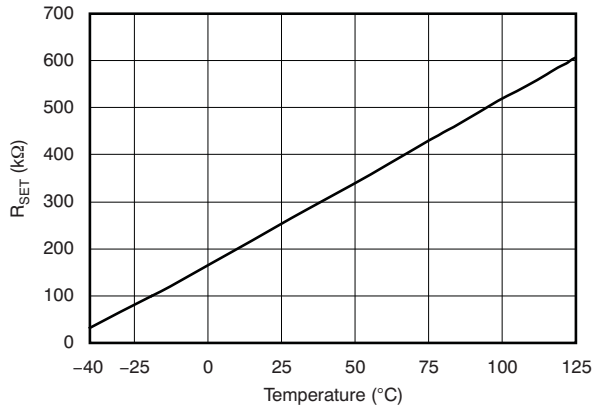


Figure 3. R_{SET} vs Temperature

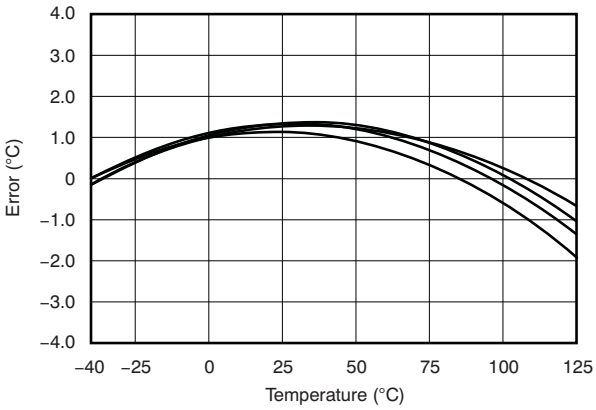


Figure 4. Typical Trip Error

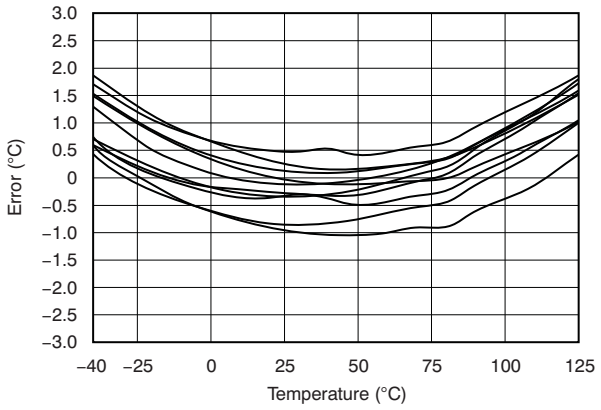


Figure 5. Typical Analog Output Error

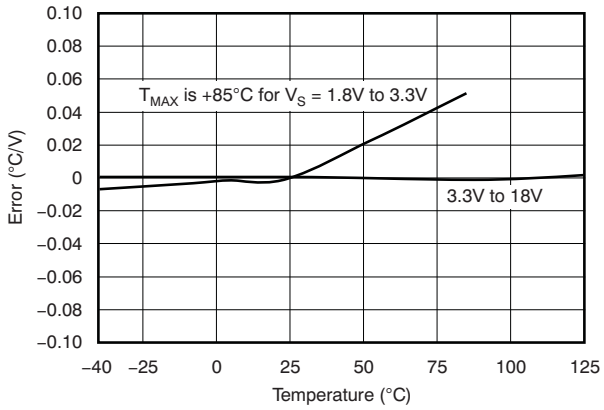


Figure 6. Analog PSR Over Temperature

Typical Characteristics (continued)

At V_S = 5V, unless otherwise noted.

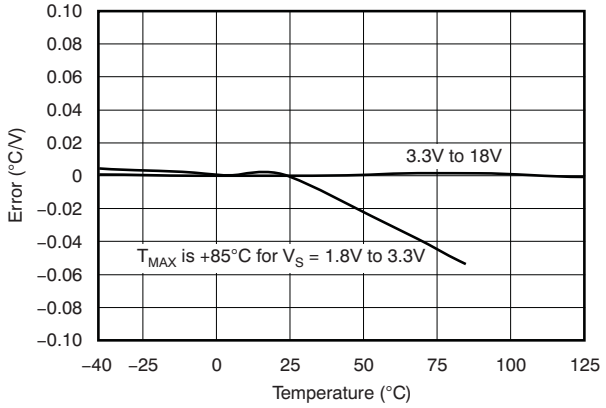


Figure 7. Trip PSR Over Temperature

7 Detailed Description

7.1 Overview

The TMP300 is a thermal sensor designed for over-temperature protection circuits in electronic systems. The TMP300 uses a set resistor to program the trip temperature of the digital output. An additional high-impedance (210kΩ) analog voltage output provides the temperature reading.

7.2 Feature Description

7.2.1 Calculating R_{SET}

The set resistor (R_{SET}) provides a threshold voltage for the comparator input. The TMP300 trips when the V_{TEMP} pin exceeds the T_{SET} voltage. The value of the set resistor is determined by the analog output function and the 3μA internal bias current.

To set the TMP300 to trip at a preset value, calculate the R_{SET} resistor value according to Equation 1 or Equation 2:

$$R_{SET} = \frac{(T_{SET} \times 0.01 + 0.5)}{3e^{-6}} \quad (1)$$

where

- T_{SET} is in °C; or

$$R_{SET} \text{ in } k\Omega = \frac{10(50 + T_{SET})}{3} \quad (2)$$

where

- T_{SET} is in °C.

7.2.2 Using V_{TEMP} to Trip the Digital Output

The analog voltage output can also serve as a voltage input that forces a trip of the digital output to simulate a thermal event. This simulation facilitates easy system design and test of thermal safety circuits, as shown in Figure 8.

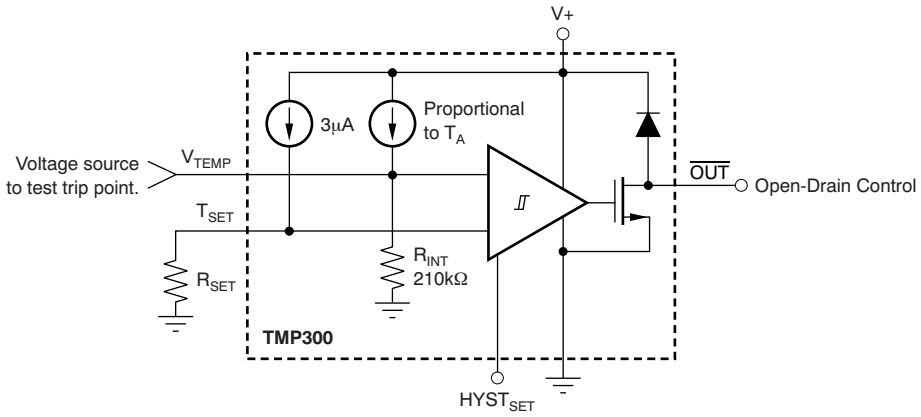


Figure 8. Applying Voltage to Trip Digital Output

Feature Description (continued)

7.2.3 Analog Temperature Output

The analog out or V_{TEMP} pin is high-impedance (210kΩ). Avoid loading this pin to prevent degrading the analog out value or trip point. Buffer the output of this pin when used for direct thermal measurement. Figure 9 shows buffering of the analog output signal.

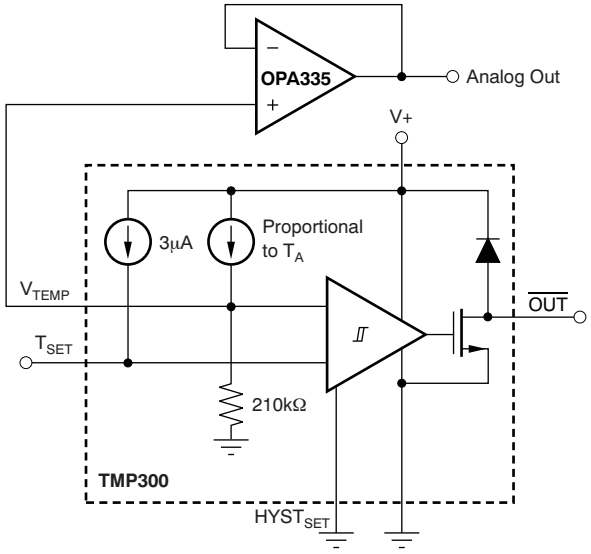


Figure 9. Buffering the Analog Output Signal

7.2.4 Using a DAC to Set the Trip Point

The trip point is easily converted by changing the digital-to-analog converter (DAC) code. This technique can be useful for control loops where a large thermal mass is being brought up to the set temperature and the $\overline{OUT}$ pin is used to control the heating element. The analog output can be monitored in a control algorithm that adjusts the set temperature to prevent overshoot. Trip set voltage error versus temperature is shown in Figure 10, which shows error in °C of the comparator input over temperature. An alternative method of setting the trip point by using a DAC is illustrated in Figure 11.

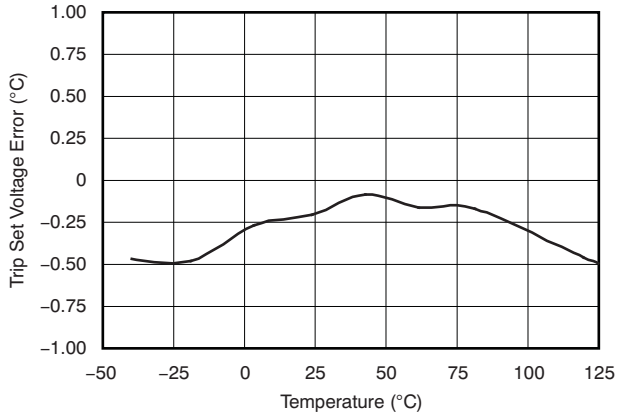


Figure 10. Trip Set Voltage Error vs Temperature

Feature Description (continued)

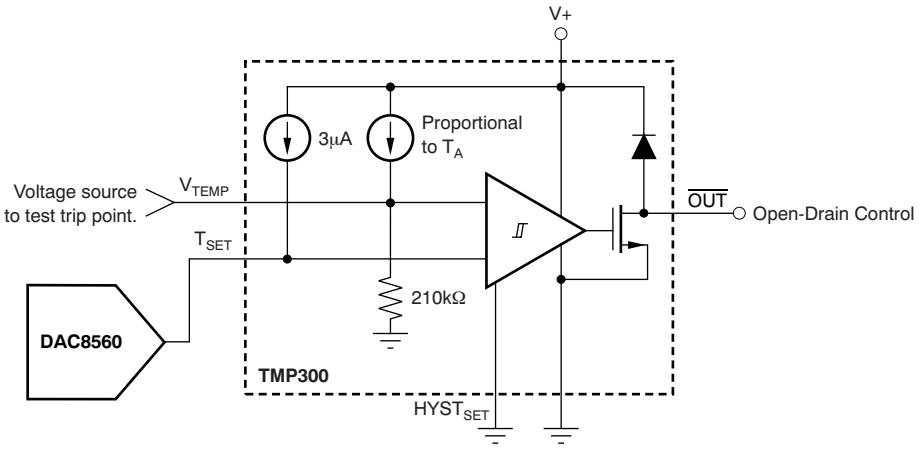


Figure 11. DAC Generates the Voltage-Driving T_{SET} Pin

7.2.5 Hysteresis

The hysteresis pin has two settings. Grounding $HYST_{SET}$ results in 5°C of hysteresis. Connecting $HYST_{SET}$ to V_S results in 10°C of hysteresis. Hysteresis error variation over temperature is shown in Figure 12 and Figure 13.

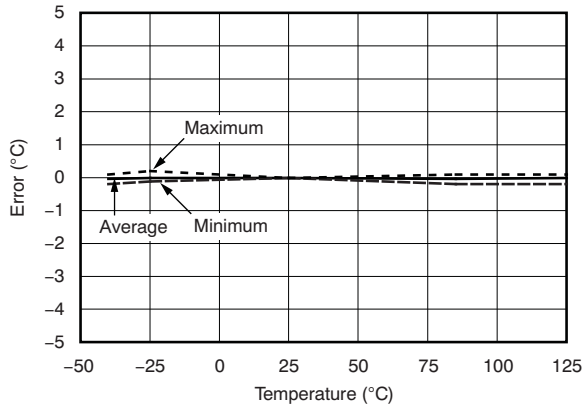


Figure 12. 5°C Hysteresis Error vs Temperature

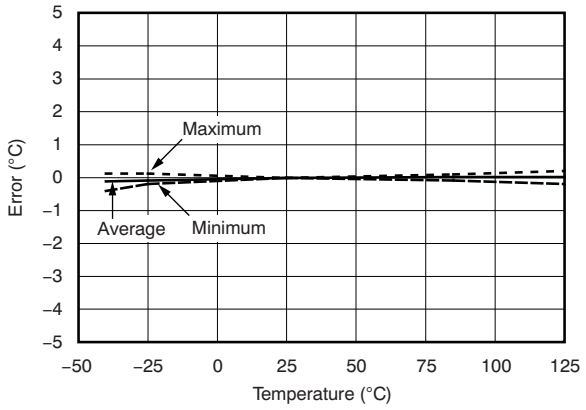


Figure 13. 10°C Hysteresis Error vs Temperature

Feature Description (continued)

Use bypass capacitors on the supplies as well as on the R_{SET} and analog out (V_{TEMP}) pins when in noisy environments, as shown in Figure 14. These capacitors reduce premature triggering of the comparator.

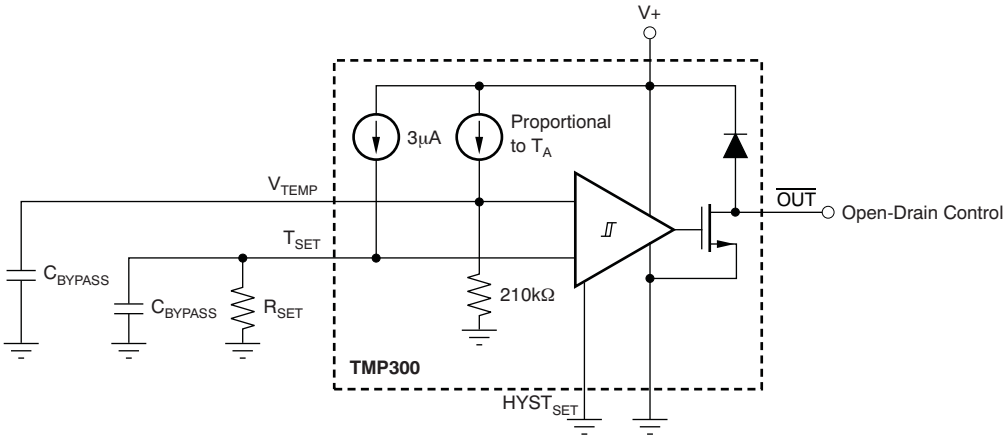


Figure 14. Bypass Capacitors Prevent Early Comparator Toggling Due to Circuit Board Noise

8 器件和文档支持

8.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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8.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

8.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

9 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP300AIDBVR	NRND	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T300	
TMP300AIDBVT	NRND	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T300	
TMP300AIDCKR	NRND	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BPN	
TMP300AIDCKT	NRND	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BPN	
TMP300BIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DUDC	Samples
TMP300BIDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DUDC	Samples
TMP300BIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QWL	Samples
TMP300BIDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QWL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

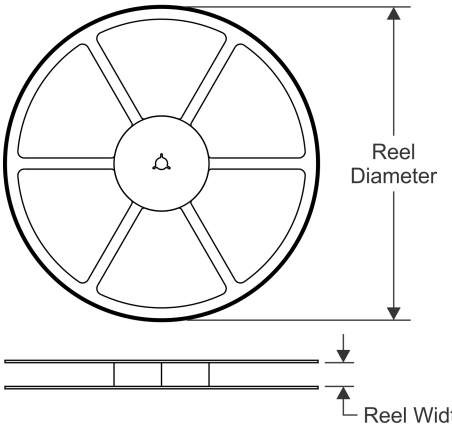
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

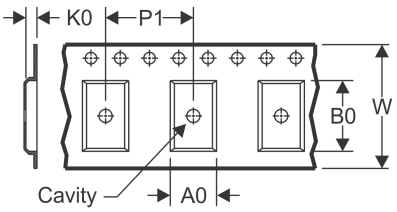
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

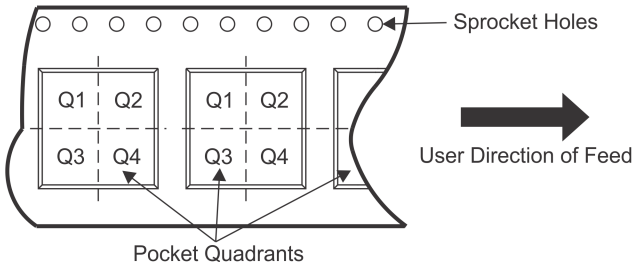


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

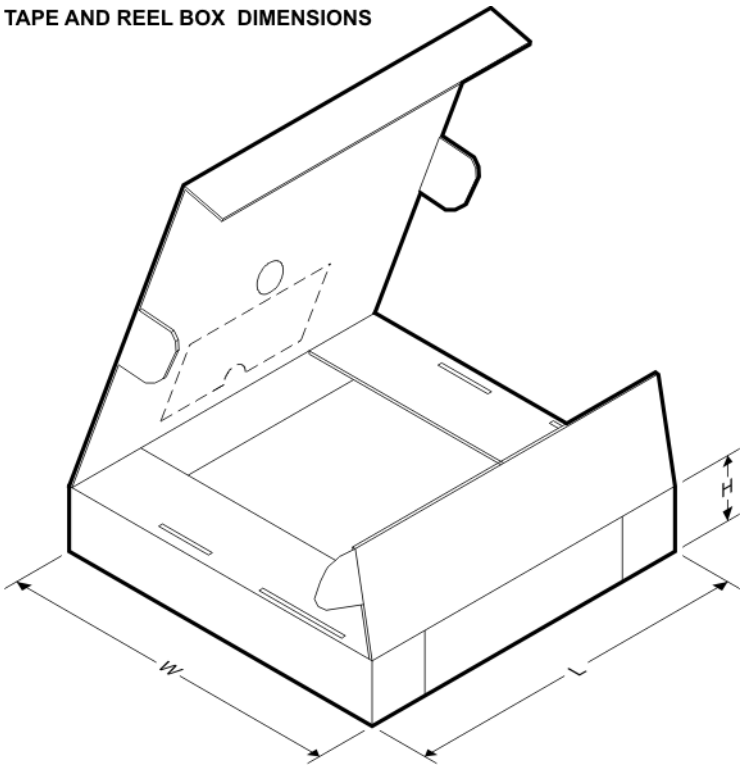
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP300AIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TMP300AIDBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TMP300AIDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TMP300AIDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TMP300BIDBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TMP300BIDBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TMP300BIDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TMP300BIDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3

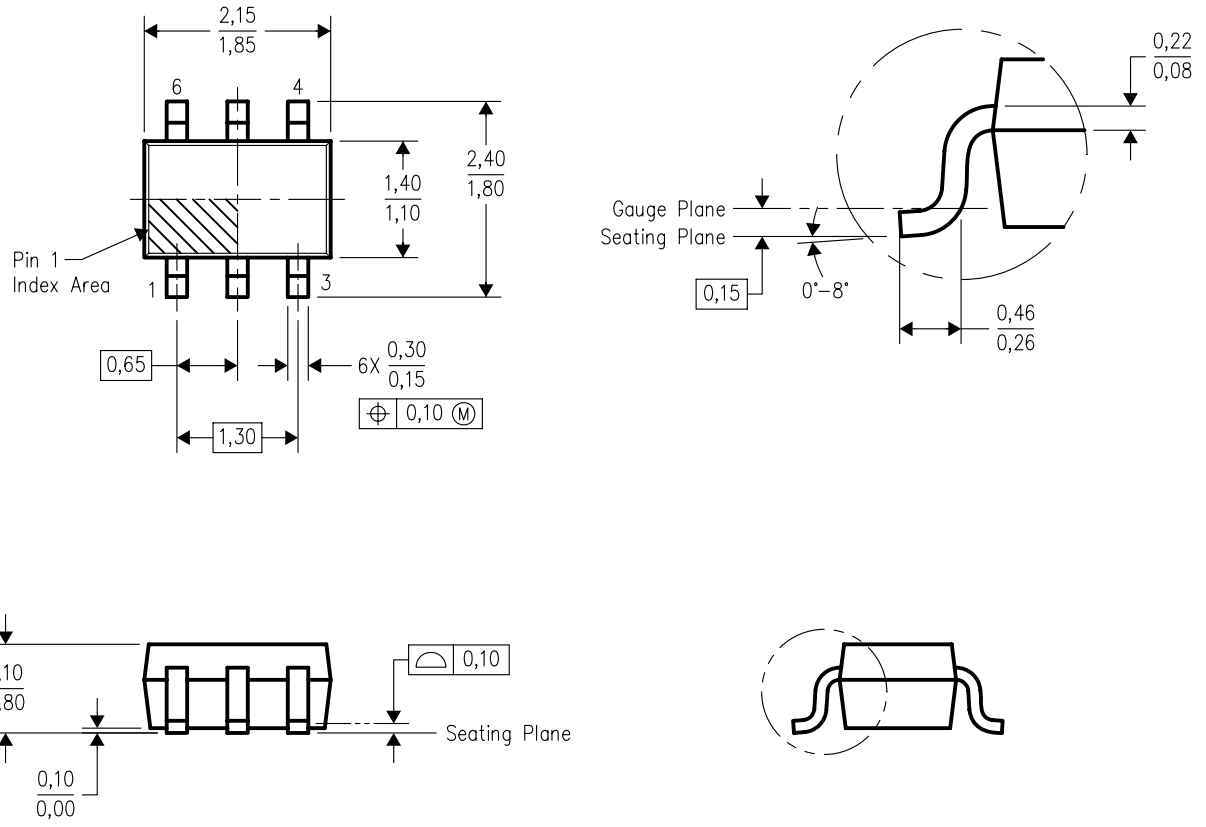
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP300AIDBVR	SOT-23	DBV	6	3000	200.0	183.0	25.0
TMP300AIDBVT	SOT-23	DBV	6	250	200.0	183.0	25.0
TMP300AIDCKR	SC70	DCK	6	3000	200.0	183.0	25.0
TMP300AIDCKT	SC70	DCK	6	250	200.0	183.0	25.0
TMP300BIDBVR	SOT-23	DBV	6	3000	200.0	183.0	25.0
TMP300BIDBVT	SOT-23	DBV	6	250	200.0	183.0	25.0
TMP300BIDCKR	SC70	DCK	6	3000	200.0	183.0	25.0
TMP300BIDCKT	SC70	DCK	6	250	200.0	183.0	25.0

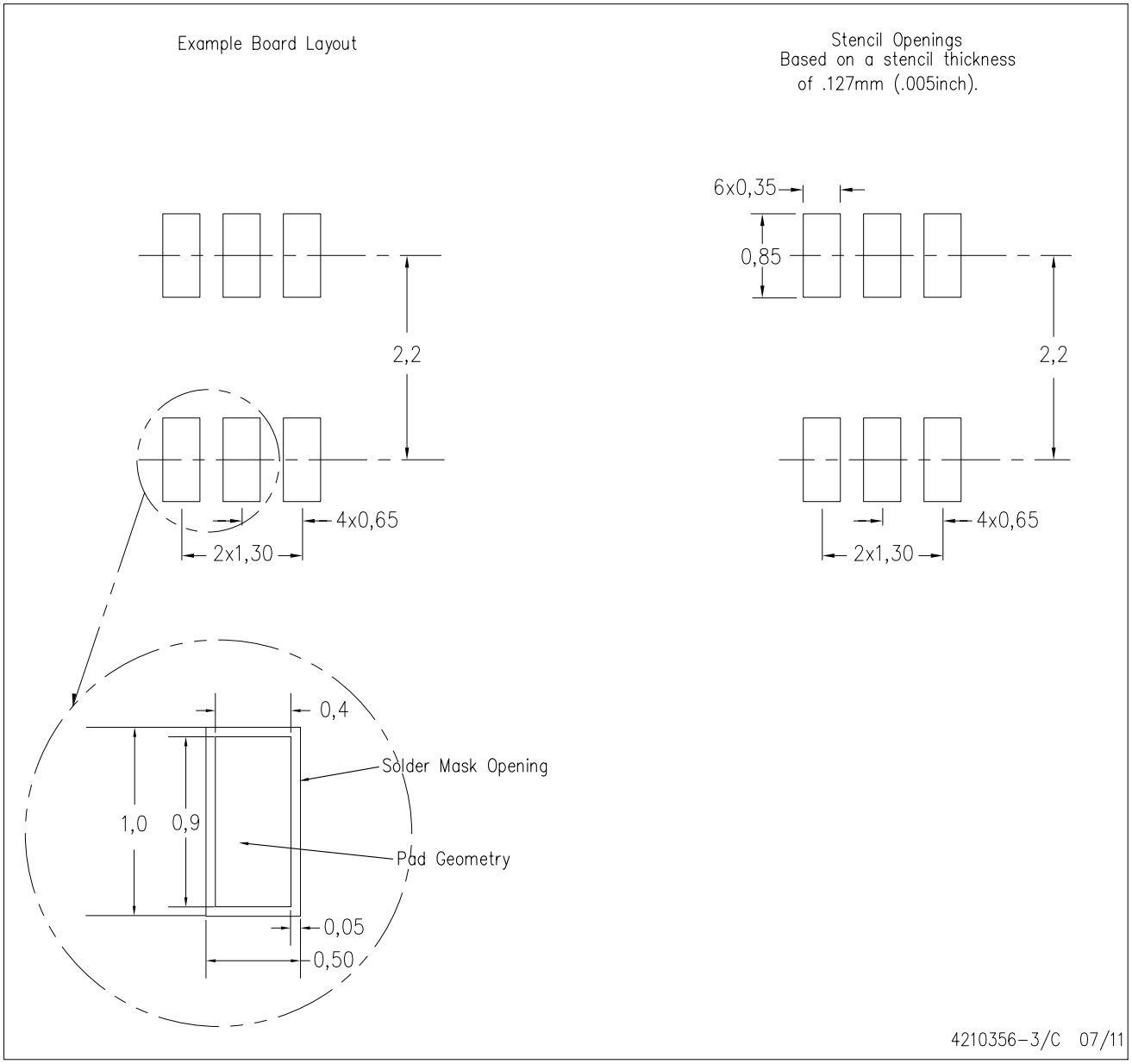
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



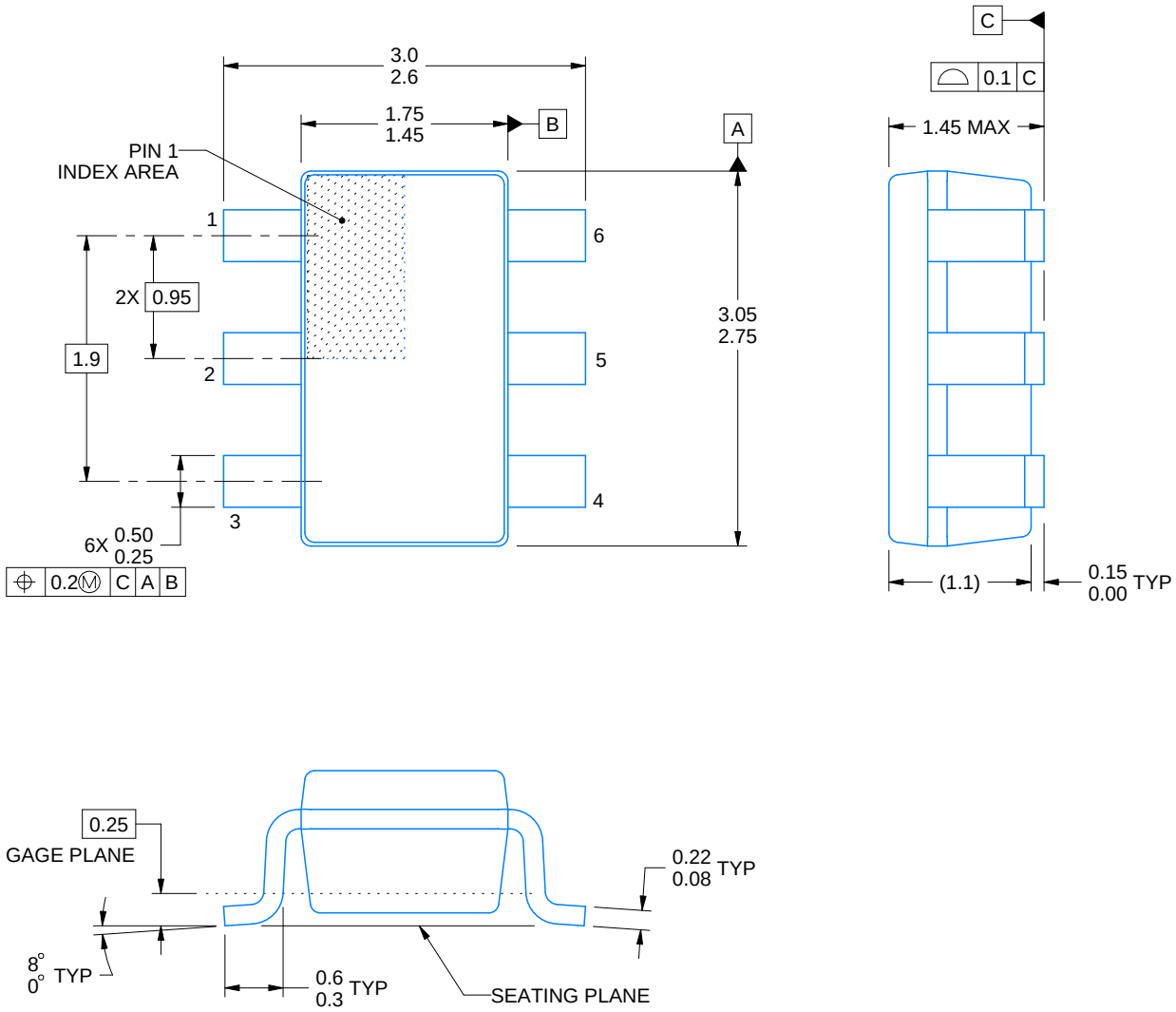
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

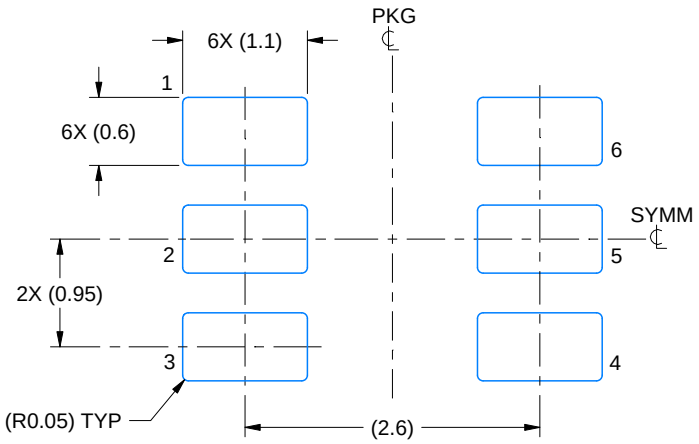
SMALL OUTLINE TRANSISTOR



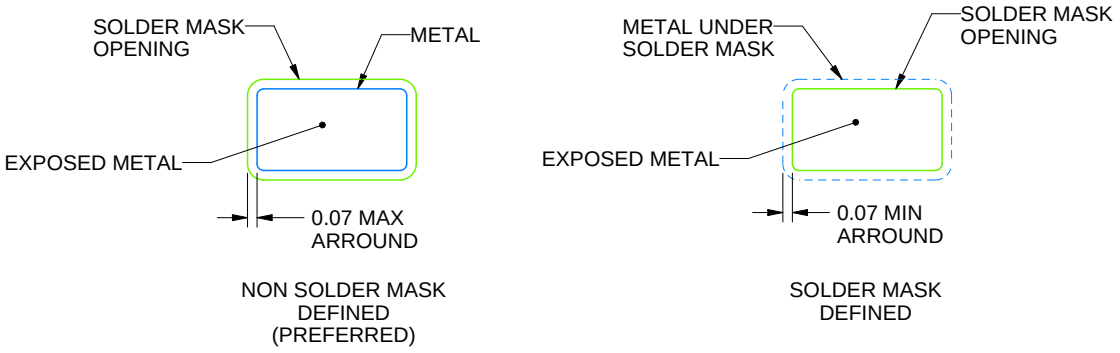
4214840/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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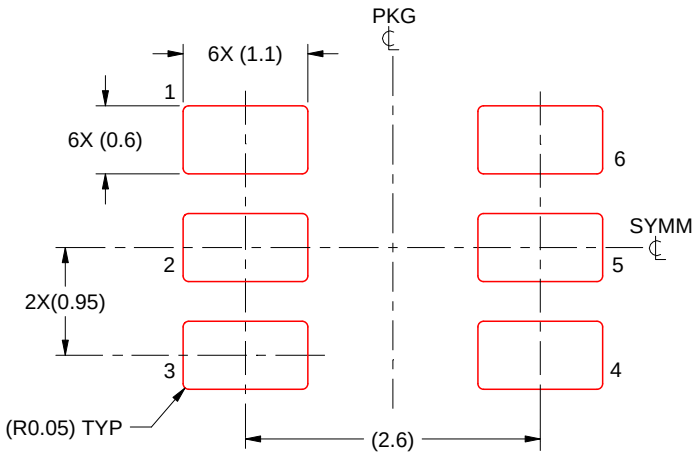
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

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