TPS2661x：具有输入和输出误接线保护功能的 50V 通用 4mA - 20mA、±20mA 电流环路保护器

1 特性

- 工作电压为 ±50V，绝对最大值为 ±55V
- 集成固定双极 32mA 电流限制
- 启动时电流限制翻倍
- 与典型的分立式保护电路相比，节省 50% 的空间
- 低 R-on：典型值为 7.5Ω
- 低 I_Q (< 100nA) – 由外部电源供电时从环路汲取的电流
- 防止输入和输出接线错误
- 信号线浪涌保护 IEC61000-4-5（采用外部 TVS）
- 标准 A EFT (IEC61000-4-4) 抗扰度（采用外部 TVS）
- 支持无电源的环路测试（仅限 TPS26610）
- 符合 HART 标准
- 使能端控制
- 使用 $\overline{SGOOD}$ 进行系统运行状况监测
- 热关断

2 应用

- 工厂自动化和控制 – PLC - 模拟输入和输出模块
- 电机驱动控制
- HART 输入
- HVAC 控制器
- UART IO 保护
- 热控制器

3 说明

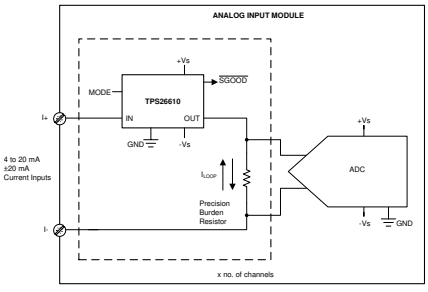
TPS2661x 是一款紧凑、功能丰富且完全集成的电流环路保护器，适用于模拟输入、模拟输出、传感器变送器、HART 输入和 UART IO 保护。该器件提供 ±20mA、0mA 至 20mA、4mA 至 20mA 的通用输入保护。7.5Ω 的低 R_{ON} 值可有效降低电流环路中的压降，从而扩展工作电压范围，即使在使用低压电源的情况下也可支持器件运行。该器件可以承受高达 ±50V 正负电源电压并保护负载免受影响。MODE 引脚提供了灵活性，可以使通过器件的电流限制翻倍，从而能够正确启动两个线控变送器。该器件能够使用低至 ±2.25V 至 ±20V 的外部双极性电源供电，还可以使用低至 3V 至 30V 的单极性电源供电。TPS26610 和 TPS26613 具有环路电源模式，便于在没有 ±Vs 电源的无电状态下进行环路测试。

该器件还通过关闭电流路径来保护系统，防止模拟输出和传感器变送器的输出侧误接线。TPS2661x 内部强大的保护控制模块以及 50V 额定电压有助于防止信号线的浪涌 (IEC61000-4-5) 和 EFT (IEC61000-4-4) 瞬变。该器件采用 2.9mm × 1.6mm 8 引脚 SOT-23 封装，大幅减小了系统占用空间。

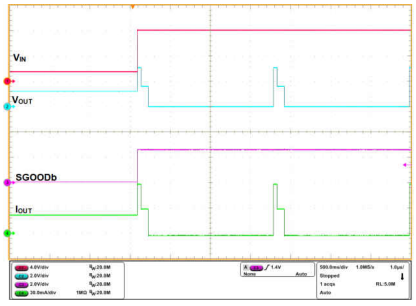
器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS26610	SOT-23 (8)	2.9mm × 1.6mm
TPS26611		
TPS26612		
TPS26613		
TPS26614		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型的电路原理图



现场电源输入端的误接线保护

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

Table of Contents

1 特性.....1
2 应用.....1
3 说明.....1
4 Revision History.....2
5 Device Comparison Table.....3
6 Pin Configuration and Functions.....3
7 Specifications.....4
7.1 Absolute Maximum Ratings.....4
7.2 ESD Ratings.....4
7.3 Recommended Operating Conditions.....4
7.4 Thermal Information.....4
7.5 Electrical Characteristics.....5
7.6 Timing Requirements.....7
7.7 Typical Characteristics.....9
8 Detailed Description.....13
8.1 Overview.....13
8.2 Functional Block Diagram.....13
8.3 Feature Description.....15
8.4 Device Functional Modes.....22
9 Application and Implementation.....26
9.1 Application Information.....26
9.2 Typical Application: Analog Input Protection for Current Inputs with TPS26610.....26
9.3 Typical Application: Analog Input Protection for Multiplexed Current and Voltage Inputs with TPS26611.....29
9.4 System Examples.....31
10 Power Supply Recommendations.....35
11 Layout.....36
11.1 Layout Guidelines.....36
11.2 Layout Example.....36
12 Device and Documentation Support.....37
12.1 接收文档更新通知.....37
12.2 支持资源.....37
12.3 Trademarks.....37
12.4 Electrostatic Discharge Caution.....37
12.5 术语表.....37
13 Mechanical, Packaging, and Orderable Information.....37

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (May 2021) to Revision C (December 2021)	Page
• 向数据表添加了 TPS26613 和 TPS26614	1

Changes from Revision A (March 2021) to Revision B (May 2021)	Page
• 删除了*器件信息*表中 TPS26611 和 TPS26612 的预览说明	1

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5 Device Comparison Table

PART NUMBER	EN PIN	LOOP TESTING WITHOUT ±Vs SUPPLIES (LOOP POWER MODE)	EXTENDED OVERLOAD DURATION FOR FIRST OVERLOAD EVENT	LATCH-OFF or AUTO-RETRY WITH INPUT < – Vs	APPLICATION
TPS26610	No	Yes	No	Latch-off	Current Inputs. See *Typical Application: Analog Input Protection for Current Inputs with TPS26610*.
TPS26611	Yes	No	No	Latch-off	Multiplexed voltage and current inputs. Analog outputs. See *Typical Application: Analog Input Protection for Multiplexed Current and Voltage Inputs with TPS26611*.
TPS26612	Yes	No	Yes. Overload expiry time is increased up to 5 s (t_{AR_dis}).	Latch-off	Power supply protection for transmitters and Analog outputs. See *Power Supply Protection of 2-Wire Transmitter with TPS26612*.
TPS26613	No	Yes	No	Auto-retry	Current inputs
TPS26614	Yes	No	No	Auto-retry	Multiplexed voltage and current inputs. Analog outputs

6 Pin Configuration and Functions

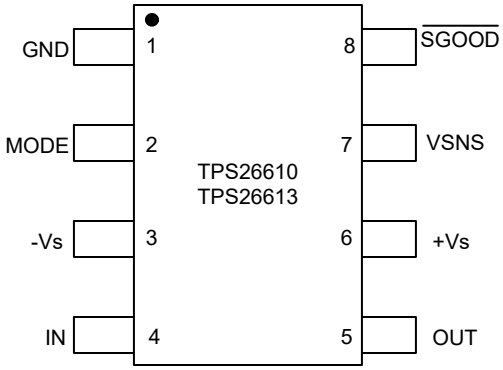


图 6-1. TPS26610 and TPS26613 DDF Package 8-Pin SOT-23 (Top View)

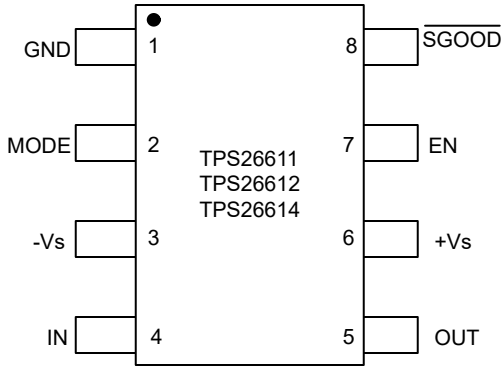


图 6-2. TPS26611, TPS26612, and TPS26614 DDF Package 8-Pin SOT-23 (Top View)

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	1	—	Reference ground for all internal voltages. Connect to GND of the ±Vs supply.
MODE	2	I	MODE selection pin for overload response. Sets current limit to I_{OL}, 2 × I_{OL}, or 2 × I_{OL} with extended I_{OL} expiry time. See the *Device Functional Modes* for details.
– Vs	3	P	Negative supply for dual supply configurations. Connect to GND when used in a single supply configuration.
IN	4	P	Signal/power input
OUT	5	P	Signal/power output
+Vs	6	P	Positive supply for powering the device
EN	7	I	*For the TPS26611, TPS26612, and TPS26614:* Enable control. Pull EN low to turn off the device. EN has internal an pullup and it can be left floating to enable the device.
VSNS		I	*For the TPS26610 and TPS26613:* Supply sensing input for transition to loop power mode. If not used, this pin can be left open or floating.
$\overline{\text{SGOOD}}$	8	O	Signal good indicator pin. Whenever the device is within normal operating condition, $\overline{\text{SGOOD}}$ shows low indicating signal is good to read. This pin can also be used to drive an external LED to give a visual indication about the state of system.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
IN, OUT, IN-OUT		–55	55	V
$\overline{SGOOD}$, EN,MODE, VSNS		–0.3	5.5	V
+Vs		-0.3	32	V
-Vs		–22	0.3	V
I_{MODE}, $I_{\overline{SGOOD}}$, I_{EN}	Source Current	Internally Limited		
$I_{\overline{EN}}$	Sink Current	Internally Limited		
$I_{\overline{SGOOD}}$			200	µA
T_J	Operating Junction temperature	–40	150	°C
	Transient Junction temperature	–65	$T_{(TSD)}$	
T_{stg}	Storage temperature	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IN,OUT	Voltage	–50		50	V
+Vs,	Supply Voltage	0		30	
-Vs		–20		0	V
EN, $\overline{SGOOD}$, VSNS	Voltage	0		5	V
MODE		0		3	V
T_J	Operating Junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS2661 DDF (SOT-23-THN) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	117.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.2	°C/W

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7.4 Thermal Information (continued)

THERMAL METRIC(1)		TPS2661 DDF (SOT-23-THN) 8 PINS	UNIT
Ψ_{JB}	Junction-to-board characterization parameter	40	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

– 40° C ⩽ $T_A = T_J$ ⩽ +125° C, 2.25 V < +Vs < 30 V, -20 V < -Vs < 0 V, MODE = GND, $\overline{SGOOD}$ = Open, EN = 3.3 V (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SIGNAL INPUT (IN)						
$V_{(IN)}$	IN Signal Voltage		– 50		50	V
I_Q	Sum of Leakage Cureent from IN and OUT pins to GND in normal operation	(– Vs) < V_{IN} , V_{OUT} < (+Vs – 0.35 V)	– 0.1		0.1	µA
		(+Vs – 0.35 V) < V_{IN}, V_{OUT} < +Vs			1	uA
I_{QFLT}	Sum of leakage current from IN and OUT pins to -Vs pin during fault as percentage of loop current	V_{IN} > +Vs, Current Limit Operation			20	%
$I_{(OL)}$	Bipolar current limit	$V_{(IN)}$-$V_{(OUT)}$ = ±1 V, -Vs connected to negative supply	±25	±32	±40	mA
	Unipolar Current limit	$V_{(IN)}$ – $V_{(OUT)}$ = +1 V, -Vs connected to GND	25	32	40	mA
	Unipolar current limit with V_{IN} <-V_S	$V_{(IN)}$ = – 24-V $V_{(OUT)}$ = – 19 V, – Vs = – 20 V. TPS26613/14 Only	– 40	– 32	– 25	mA
$I_{(OL_Pulse)}$	Transient Pulse Over Current Limit	$V_{(IN)}$ – $V_{(OUT)}$ = +1.5 V, MODE = Floating	50	60	72	mA
$I_{(FASTRIP)}$	Fast-trip current limit	MODE = GND	±65		±165	mA
		MODE = Floating or 180 kΩ to GND	±140		±275	mA
$I_{Off\text{-}Lkg\text{-}IN}$ + $I_{Off\text{-}Lkg\text{-}OUT}$	Sum of leakage current from IN and OUT pins in Off state (Source)	-12.5 V < V_{IN} <12.5 V; V_{OUT} = 0 V; EN = Low; +V_s = 15V; (-V_s) = -15 V ,TPS26611/12/14 Only	– 9.75		– 5.25	µA
		-12.5 V < V_{OUT} < 12.5 V; V_{IN} = 0 V; EN = Low; +V_s = 15V; (-V_s) = -15 V, TPS26611/12/14 Only	– 9.75		– 5.25	µA
$I_{Off\text{-}Lkg\text{-}IN}$	Leakage current from IN pin in Off state (Source)	-12.5 V< V_{IN} <12.5 V; V_{OUT} = 0 V; EN = Low; +V_s = 15V; (-V_s) = -15 V ,TPS26611/12/14 Only	– 6		– 1	µA
$I_{Off\text{-}Lkg\text{-}OUT}$	Leakage current from OUT pin in Off state (Source)	-12.5 V < V_{OUT} < 12.5 V; V_{IN} = 0 V; EN = Low; +V_s = 15V; (-V_s) = -15 V ,TPS26611/12/14 Only	– 6		– 1	µA
Overvoltage and Undervoltage Cutoff for OUT Pin						
V_{OUT_OVLO}	OUT Overvoltage Protection Threshold, Rising	TPS26610/11/13/14 Only	(+Vs)+0.05		(+Vs)+0.30	V
		TPS26612 Only	(+Vs)+1		(+Vs)+1.50	V
$V_{OUT_OVLO_hyst}$	OUT Overvoltage Hysterises		30		75	mV
V_{O/I_UVLO}	OUT/IN Undervoltage Protection Threshold, Falling	TPS26610/11/12 Only	(– Vs)-0.40		(– Vs)-0.20	V

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7.5 Electrical Characteristics (continued)

–40° C ≤ T_A = T_J ≤ +125° C, 2.25 V < +Vs < 30 V, -20 V < -Vs < 0 V, MODE = GND, $\overline{SGOOD}$ = Open, EN = 3.3 V (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{O/I_UVLO_hyst}	OUT/IN undervoltage Hysterises	TPS26610/11/12 Only	30		75	mV
V_{O_UVLO}	OUT Undervoltage Protection Threshold, Falling	TPS26613/14 Only	(–Vs)-0.40		(–Vs)-0.20	V
$V_{O_UVLO_hyst}$	OUT undervoltage Hysterises	TPS26613/14 Only	30		75	mV
POWER SUPPLY PINS (+Vs/-Vs)						
$V_{(+Vs)}$	+Vs Supply Operating Voltage	TPS26610/11/13/14	2.25		30	V
$V_{(+Vs)}$	+Vs Supply Operating Voltage	TPS26612 only	4		30	V
$V_{(-Vs)}$	-Vs Supply Operating Voltage		–20		0	V
$Vs_{_DIFF}$	Difference between +Vs and -Vs		3		50	V
$I_{(+Vs)}$	Current sourced from +Vs supply to GND in normal operation	$\overline{SGOOD}$ = Floating		1.07	1.65	mA
$I_{(+Vs)}$	Current sourced from +Vs supply to GND in fault operation	$\overline{SGOOD}$ = Floating		1.2	1.75	mA
$I_{(-Vs)}$	Current sinked by -Vs supply from GND				0.2	mA
I_{VS_OFF}	OFF State Supply Current	EN = Low (TPS26611/12/14 only)			0.27	mA
Loop Testing Vs/-Vs UNPOWERED (TPS26610/13 only)						
$V_{(IN-OUT)no_Vs}$	Current Loop Testing : IN to OUT Voltage drop	+/-20mA current through IN pin		±5	±8.5	V
I_{Qno_Vs}	Percentage of forced IN current going to -Vs pin				20	%
I_{OL_noVs}	No supply current limit		±22		±45.5	mA
PASS FET						
R_{ON}	IN to OUT total ON resistance	–40 ℃ < T < 125 ℃, $I_{(IN)}$ < Overload Current	4.8	7.5	12.5	Ω
ENABLE (EN) TPS26611/12/14 Only						
$V_{(ENR)}$	EN Rising Threshold				1.72	V
$V_{(ENF)}$	EN Falling Threshold		1			V
$I_{(EN_LKG)}$	EN Leakage Current (Sink)	$V_{(EN)}$ = 5.5 V			10	µA
$I_{(EN_LKG)}$	EN Leakage Current (Source)	$V_{(EN)}$ = 0 V	-10			µA
$V_{(EN)}$	EN Open Circuit Voltage	$I_{(EN)}$ = –0.1 µA		2.1	2.5	V
VSNS (Supply Sensing) TPS26610/13 only						
$V_{(SNSR)}$	VSNS Rising threshold				1.72	V
$V_{(SNSF)}$	VSNS Falling threshold		1			V
SIGNAL GOOD ($\overline{SGOOD}$)						
$V_{OH_\overline{SGOOD}}$	$\overline{SGOOD}$ Output Level, HIGH	(+Vs) ≤ 2.5 V, 0 mA < $I_{\overline{SGOOD}}$ < 1 mA	(+Vs)*(0.8)		(+Vs)	V

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7.5 Electrical Characteristics (continued)

– 40° C ≤ T_A = T_J ≤ +125° C, 2.25 V < +Vs < 30 V, -20 V < -Vs < 0 V, MODE = GND, $\overline{SGOOD}$ = Open, EN = 3.3 V (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH_\overline{SGOOD}}$	$\overline{SGOOD}$ Output Level, HIGH	(+Vs) > 2.5 V, 0 mA < $I_{\overline{SGOOD}}$< 1 mA	2		3	V
$R_{\overline{SGOOD}}$	$\overline{SGOOD}$ pull down impedance	0 µA < $I_{\overline{SGOOD}}$ < 200 µA			6.3	kΩ
MODE						
$I_{(MODE)}$	MODE Source Current		1.55	2	2.4	µA
R_{MODE}	Mode Selection Resistor			180		kΩ
THERMAL SHUTDOWN						
$T_{(TSD)}$	Thermal Shutdown (TSD) threshold, Rising			160		°C
$T_{(TSDHyst)}$	Thermal Shutdown (TSD) Hysterises			11		°C
HART						
BW	Input small signal bandwidth	– 25 mA < I_{IN} < 25 mA, Δ I_{IN} = 1 mA_{pp} at 1 kΩ		10		kHz

7.6 Timing Requirements

– 40° C ≤ T_A = T_J ≤ +125° C, 2.25 V < +Vs < 30 V, -20 V < -Vs < 0 V, MODE = GND, $\overline{SGOOD}$ = Open, EN = 3.3V (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON_dly}	Turn ON delay with Vs/-Vs supply	Delay from +Vs/-Vs supply applied to FET on, EN = Floating		120		µs
t_{OFF_dly}	Turn OFF delay with +Vs/-Vs supply	Delay from +Vs/-Vs supply removed to FET off, EN = Floating			10	µs
$t_{ON_EN_dly}$	Turn ON delay with EN pin	+Vs/-Vs supply present, Delay from EN HIGH to FET on,		120		µs
$t_{OFF_EN_dly}$	Turn OFF delay with EN pin	+Vs/-Vs supply present, Delay from EN LOW to FET off			10	µs
t_{OL}	Overload Current Limit response time	Load transient from 20 mA to 50 mA. Time from Load Transient to Current coming within 20%.of I_{OL}.		30	55	µs
t_{OL_PULSE}	Pulse Overload Current Limit response time	Load transient from 20 mA to 80 mA. Time from Load Transient to Current coming within 20% of I_{OL_Pulse}		20	50	µs
$t_{FASTRIP}$	Fast-Trip Response Time	MODE = GND, Current exceeding 120mA to FET off			5	µs
		MODE = 180-kΩto GND or Open, Current exceeding 240 mA to FET off			5	µs
$T_{SG_Deglitch}$	$\overline{SGOOD}$ Deglitch Delay	Deglitch delay during $\overline{SGOOD}$ assertion		685		µs
		Deglitch delay during $\overline{SGOOD}$ de-assertion			1.3	ms
$t_{OUT_OV_CUT}$	OUT OVLO Cutoff detection-time	$V_{(OUT)}$ ↑ 100 mV above V_{OUT_OVLO} to FET OFF	1		5	µs
t_{O/I_UV_CUT}	OUT OR IN UVLO Cutoff detectiontime	OUT/IN ↓ 100 mV below V_{O/I_UVLO} to FET OFF, TPS26610/11/12 Only	1		5	µs
$t_{O_UV_CUT}$	OUT UVLO Cutoff detection-time	OUT ↓ 100 mV below V_{O_UVLO} to FET OFF, TPS26613/14 Only	1		5	µs

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7.6 Timing Requirements (continued)

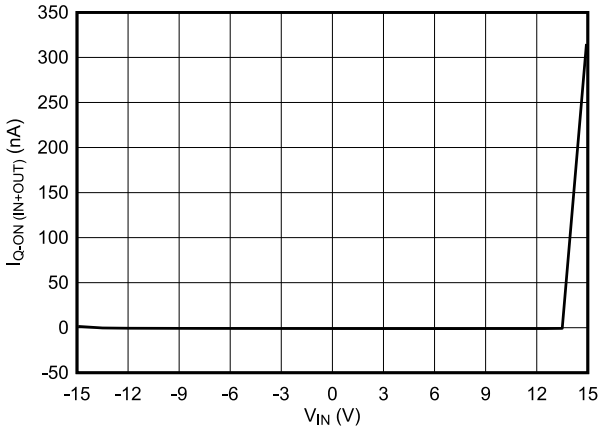
–40° C ≤ T_A = T_J ≤ +125° C, 2.25 V < +Vs < 30 V, -20 V < -Vs < 0 V, MODE = GND, $\overline{SGOOD}$ = Open, EN = 3.3V (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{OUT_CUT_Rec}$	OUT Cutoff recovery time	$V_{(OUT)}$ ↓ 100 mV below $V_{OUT_OVLO_hyst}$ to FET ON		21		µs
t_{O/I_CUT_Rec}	IN OR OUT Cutoff recovery time	OUT/IN ↑ 100 mV above VO/ I_UVLO_hyst to FET ON, TPS26610/11/12 Only		23.5		µs
$t_{O_CUT_Rec}$	OUT Cutoff recovery time	OUT ↑ 100 mV above $V_{O_UVLO_hyst}$ to FET ON, TPS26613/14 Only		23.5		µs
t_{OL_Expiry}	Overload Current Limit expiry time	Load transient from 20 mA to 50 mA		100		ms
$t_{OL_Pulse_Expiry}$	Pulse Overload Current expiry	Load transient from 20 mA to 100 mA		50		ms
t_{OL_Extend}	I_{OL} < I < I_{OL_PULSE} expiry timer			5.00		s
t_{RETRY1}	Auto Retry Timer 1			0.80		s
t_{RETRY2}	Auto Retry Timer 2			1.60		s
t_{AR_dis}	Auto Retry disabled time (TPS26612 only)			5		s

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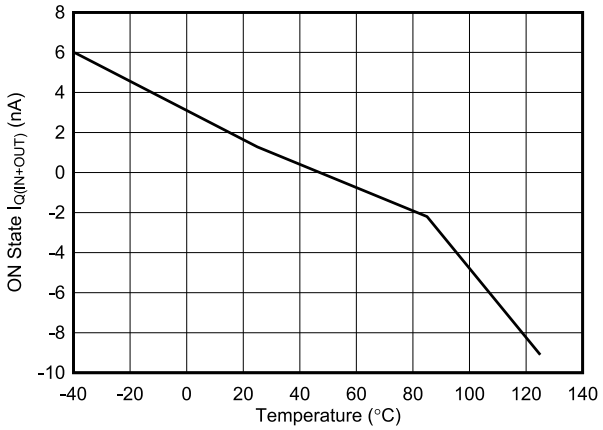
7.7 Typical Characteristics

+Vs = 15 V; –Vs = –15 V, MODE = OPEN, $\overline{SGOOD}$ = OPEN; EN/VSNS = OPEN; T_A = 25° C (unless otherwise noted)



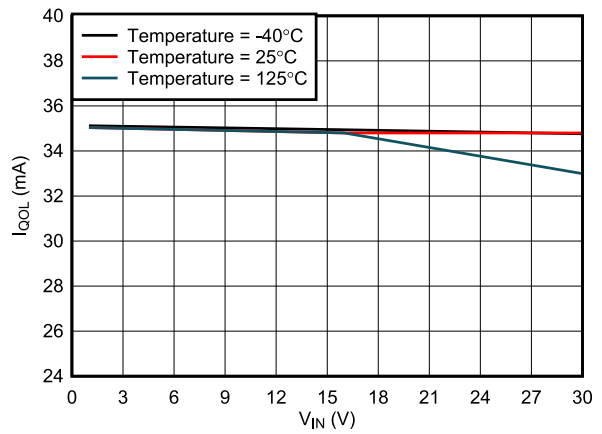
+Vs = 15 V; -Vs = GND; V_{IN} = V_{OUT}

图 7-1. $I_{Q-ON\ (IN+OUT)}$ vs V_{IN} in Normal Operation



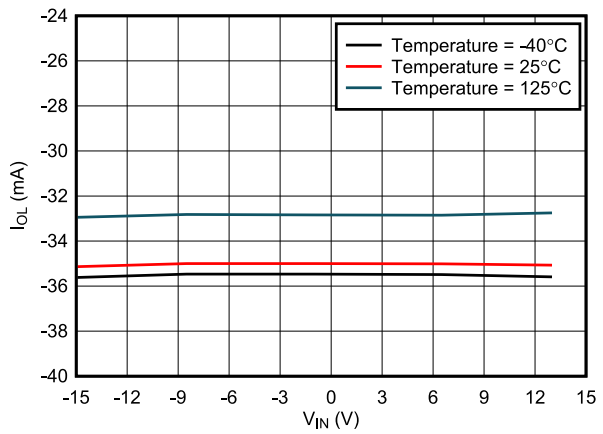
V_{IN} = V_{OUT} = 0 V

图 7-2. $I_{Q\ (IN+OUT)}$ vs Temperature in Normal Operation



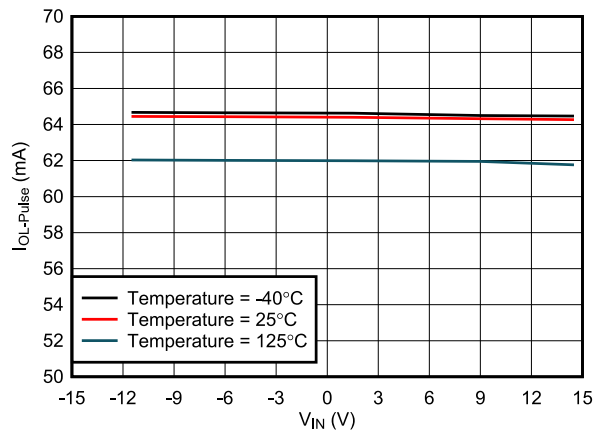
+Vs = 30 V; –Vs = GND; V_{IN} = V_{OUT} + 1 V

图 7-3. I_{OL} vs V_{IN} for I_{OUT} > 0



V_{IN} = V_{OUT} - 1 V

图 7-4. I_{OL} vs V_{IN} for I_{OUT} < 0



V_{IN} = V_{OUT} + 1.5 V; MODE = Open or 180 kΩ

图 7-5. $I_{OL-Pulse}$ vs V_{IN}

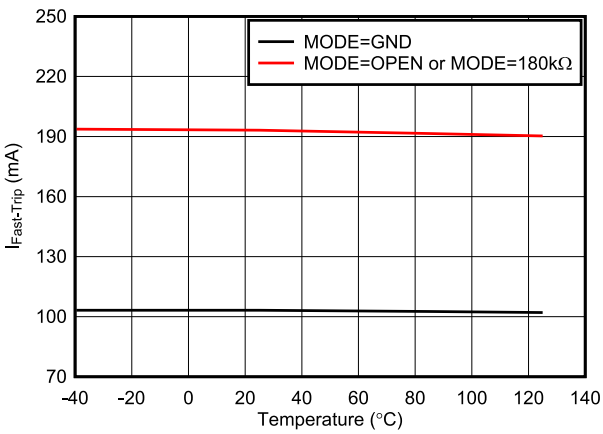


图 7-6. $I_{Fast-trip}$ vs Temperature for I_{OUT} > 0

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7.7 Typical Characteristics (continued)

+Vs = 15 V; – Vs = – 15 V, MODE = OPEN, $\overline{SGOOD}$ = OPEN; EN/VSNS = OPEN; T_A = 25° C (unless otherwise noted)

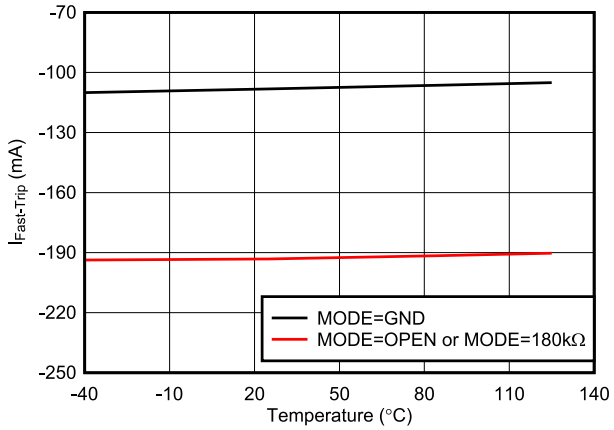
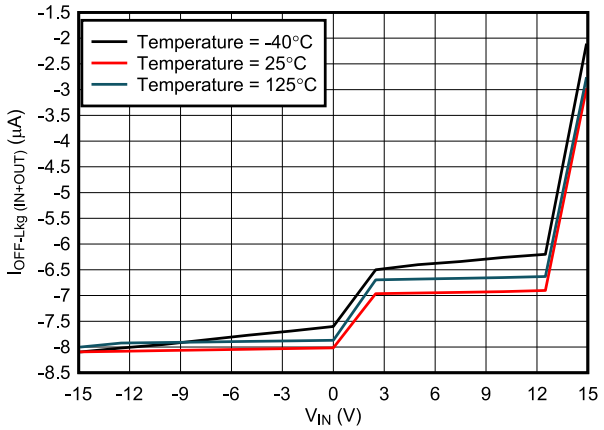
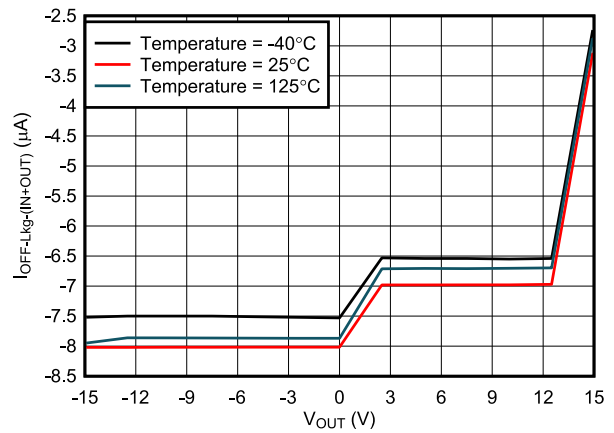


图 7-7. $I_{Fast\text{-}trip}$ vs Temperature for I_{OUT} < 0



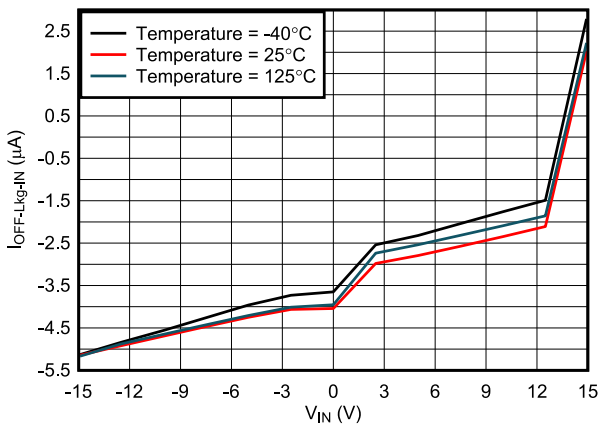
V_{OUT} = 0 V

图 7-8. ($I_{OFF\text{-}Leakage\text{-}IN}$ + $I_{OFF\text{-}Leakage\text{-}OUT}$) vs V_{IN}



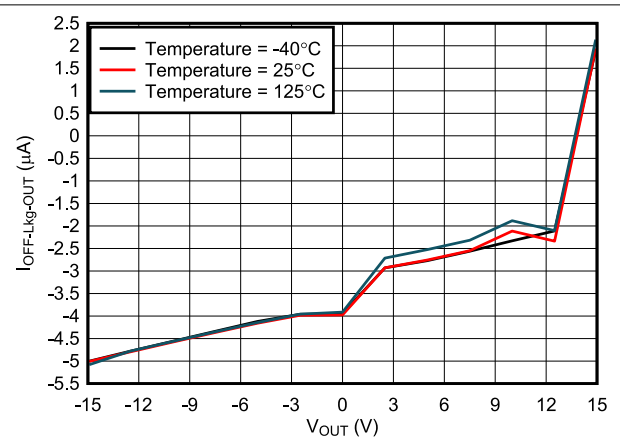
V_{IN} = 0 V

图 7-9. ($I_{OFF\text{-}Leakage\text{-}IN}$ + $I_{OFF\text{-}Leakage\text{-}OUT}$) vs V_{OUT}



V_{OUT} = 0 V

图 7-10. $I_{OFF\text{-}Leakage\text{-}IN}$ vs V_{IN}



V_{IN} = 0 V

图 7-11. $I_{OFF\text{-}Leakage\text{-}OUT}$ vs V_{OUT}

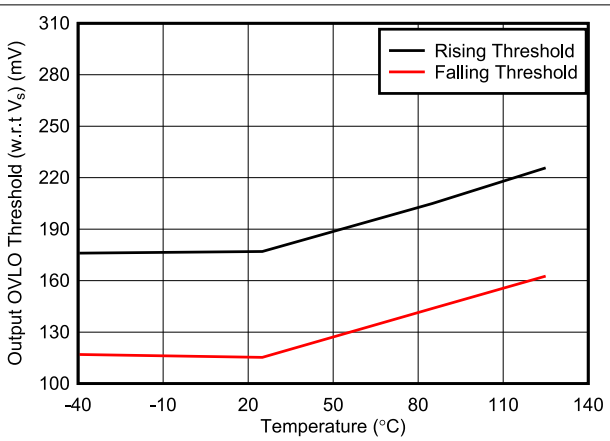


图 7-12. OUT OVLO Thresholds (w.r.t Vs) vs Temperature for TPS26611 and TPS26610

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7.7 Typical Characteristics (continued)

+Vs = 15 V; –Vs = –15 V, MODE = OPEN, $\overline{SGOOD}$ = OPEN; EN/VSNS = OPEN; T_A = 25° C (unless otherwise noted)

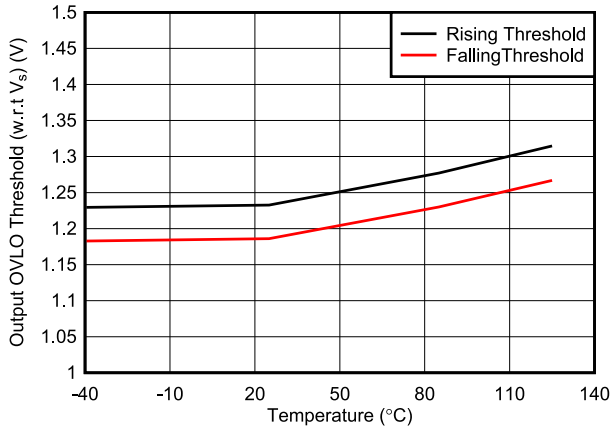


图 7-13. OUT OVLO Thresholds (w.r.t Vs) vs Temperature for TPS26612

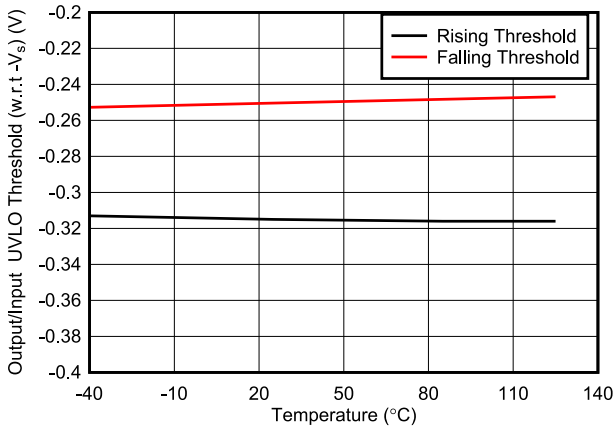


图 7-14. OUT and IN UVLO Thresholds (w.r.t -Vs) vs Temperature

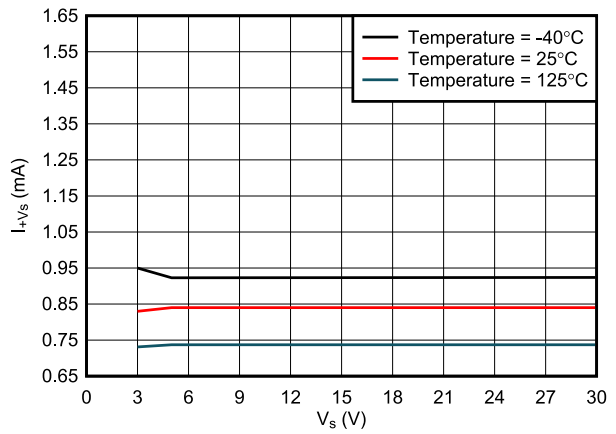


图 7-15. I_{Vs} vs Vs in ON State

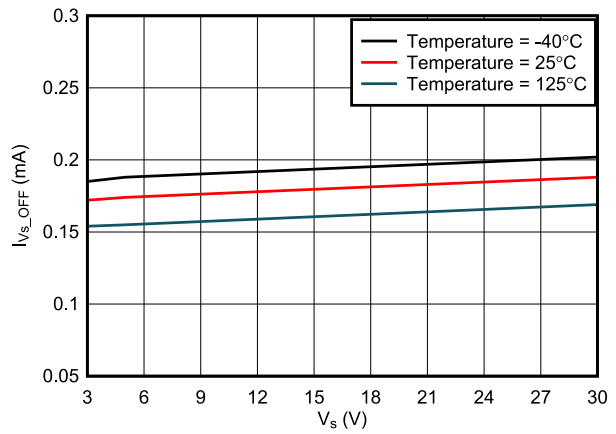


图 7-16. I_{Vs} vs Vs in OFF State (EN = 0) for TPS26611 and TPS26612

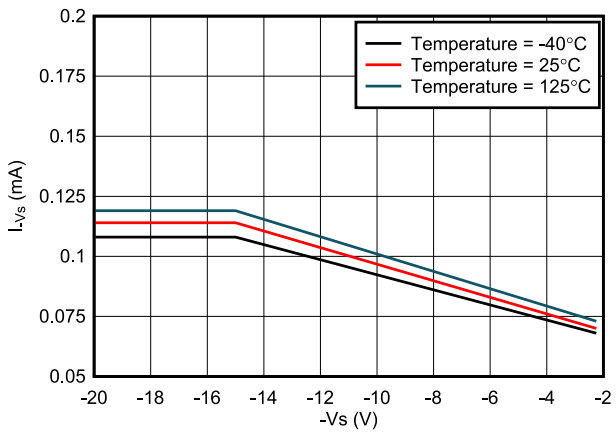


图 7-17. I_{-Vs} vs -Vs in ON State

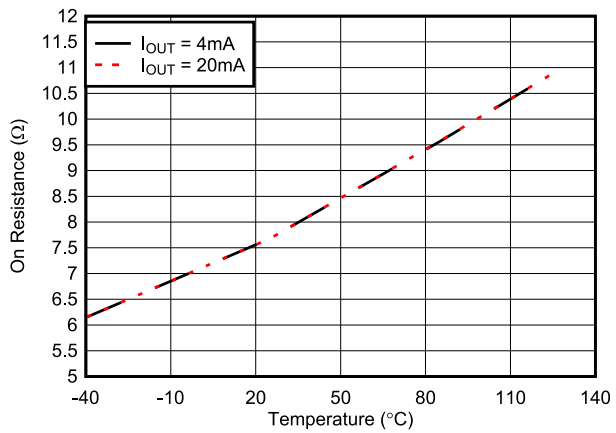
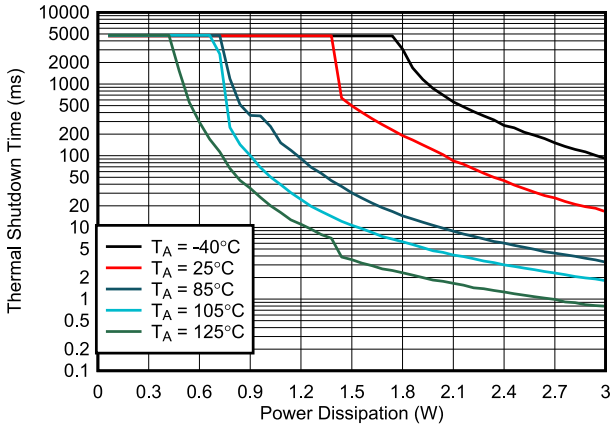


图 7-18. R_{ON} vs Temperature

7.7 Typical Characteristics (continued)

+Vs = 15 V; – Vs = – 15 V, MODE = OPEN, $\overline{SGOOD}$ = OPEN; EN/VSNS = OPEN; T_A = 25° C (unless otherwise noted)



I_{OUT} = 60 mA, MODE = 180 kΩ

图 7-19. Thermal shutdown time vs Power Dissipation

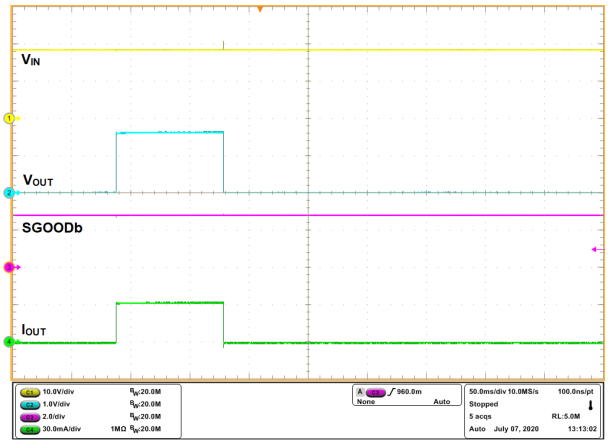


图 7-20. Current Limit with MODE = GND

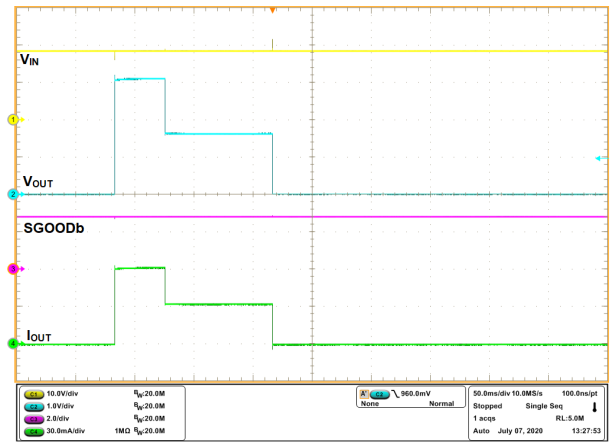


图 7-21. Current Limit with MODE = OPEN

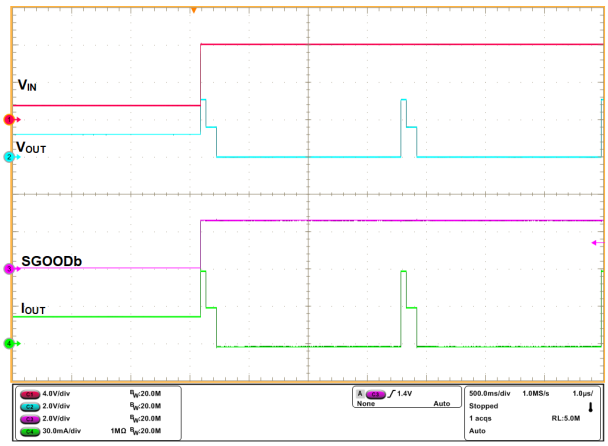


图 7-22. Auto Retry with MODE = 180 kΩ

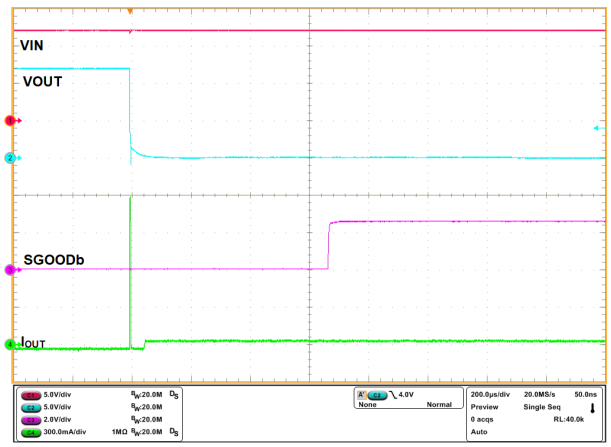


图 7-23. Fast-Trip Protection

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8 Detailed Description

8.1 Overview

The TPS2661x is a family of devices providing complete protection for current inputs, voltage inputs/outputs, and sensor supply in industrial and process automation systems. The device supports both unipolar 4-mA to 20-mA current loops and bipolar ±20-mA current loops. The TPS26610 and TPS26613 are tailored for current inputs. The device can be powered from an external supply and draws < 100-nA maximum current from the current loop enabling design of high accuracy analog input systems. The devices feature an accurate 32-mA current limit, which enables using low power components in the loop like the sense resistors, which reduces the overall system size and cost. The TPS26611 and TPS26614 are specifically tailored for universal current inputs and voltage/current multiplexed inputs while the TPS26612 is tailored for protection of two wire sensor transmitters. The TPS2661x devices feature a configurable MODE pin to allow higher current for powering up of a variety of two wire transmitters. The TPS26611 also has enable control for designing V/I multiplexed analog inputs or universal analog input-output modules. The device also features a signal-good output to indicate if the there is a valid current input. The signal good pin goes high in the event of any fault or during start-up of the system if there is an inrush current. The device also protects the system from output miswiring in analog output modules or sensor transmitters by cutting off the current path if the OUT pin goes outside the +/ – Vs supply rails.

The robust protection of the TPS2661x along with its ±50-V rating helps to simplify the system designs for surge compliance. The TPS2661x devices are immune to noise tests like electrical fast transients that are common in industrial applications. These devices also simplify the system design for protection from surge transients (IEC61000-4-5).

8.2 Functional Block Diagram

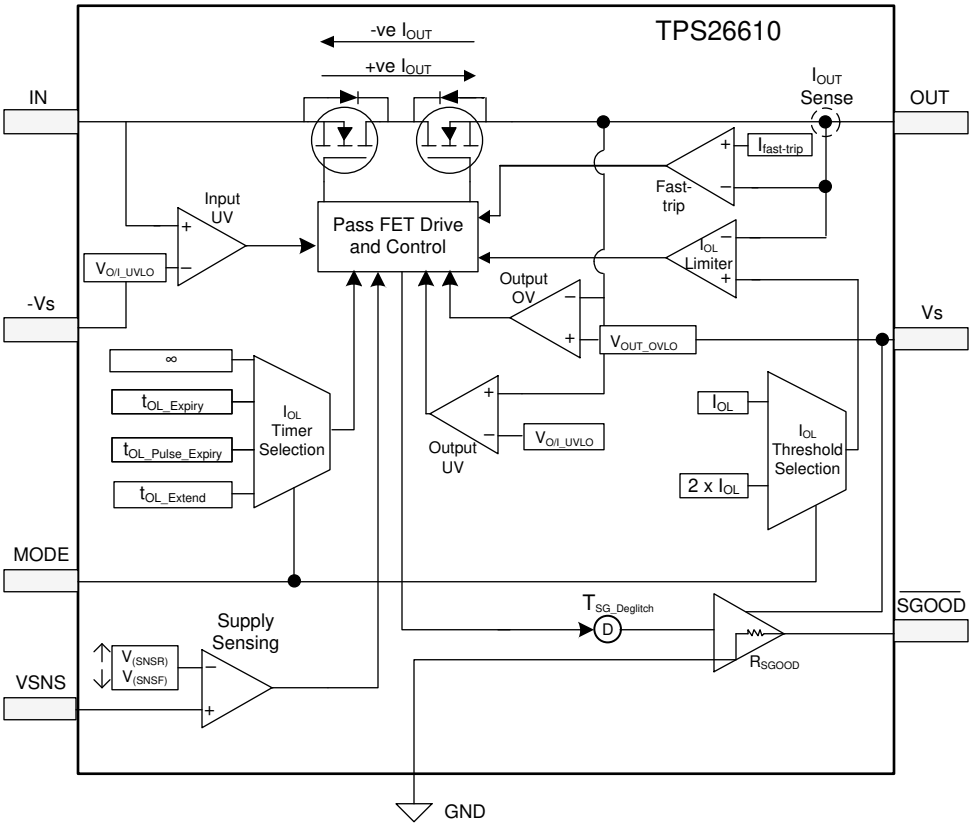


图 8-1. Functional Block Diagram for TPS26610

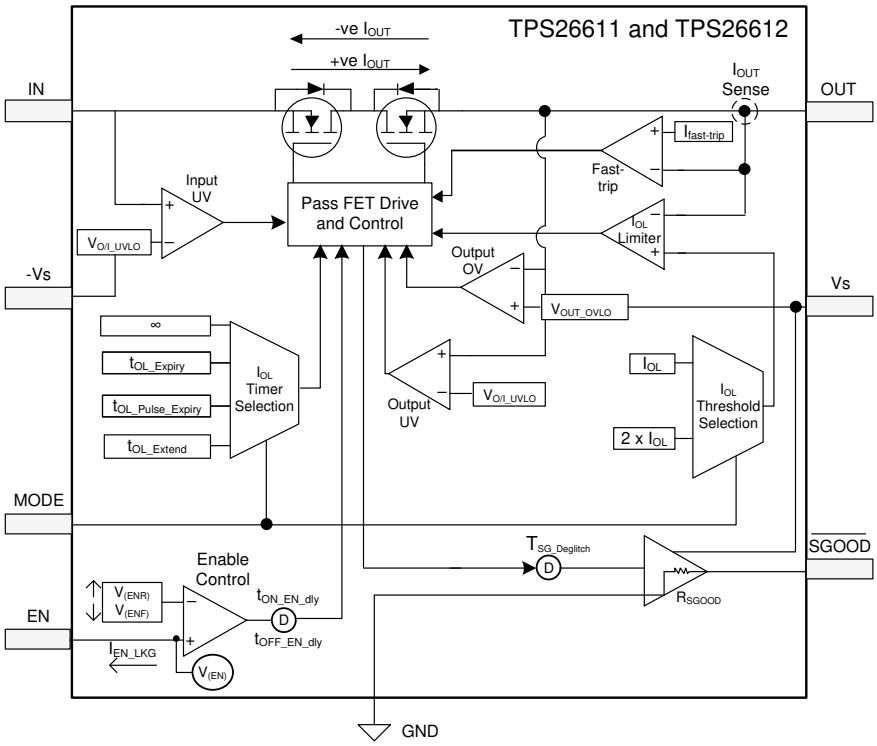


图 8-2. Functional Block Diagram for TPS26611 and TPS26612

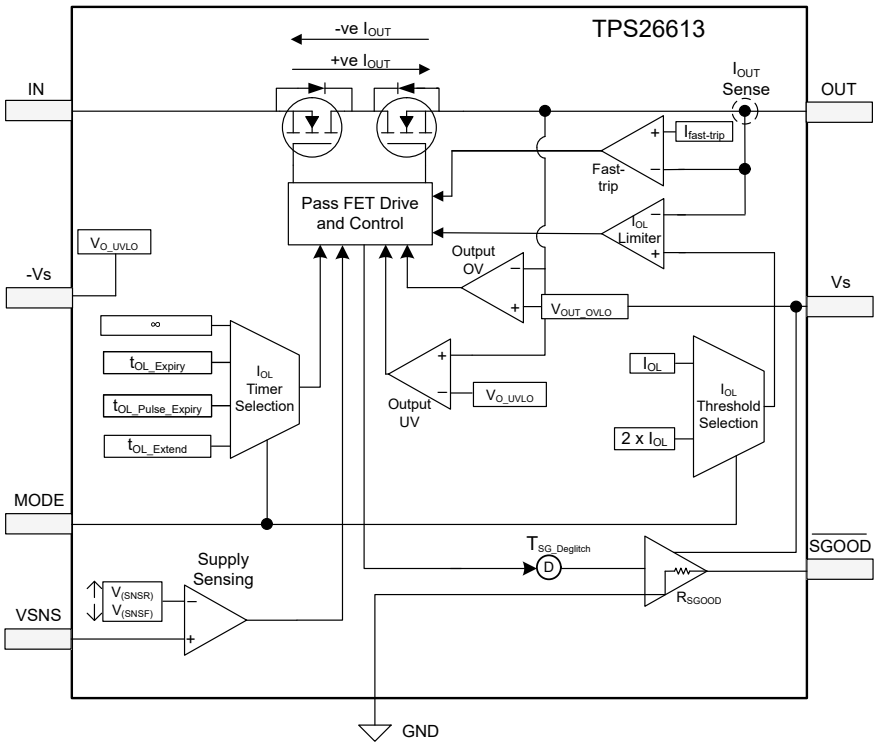


图 8-3. Functional Block Diagram for TPS26613

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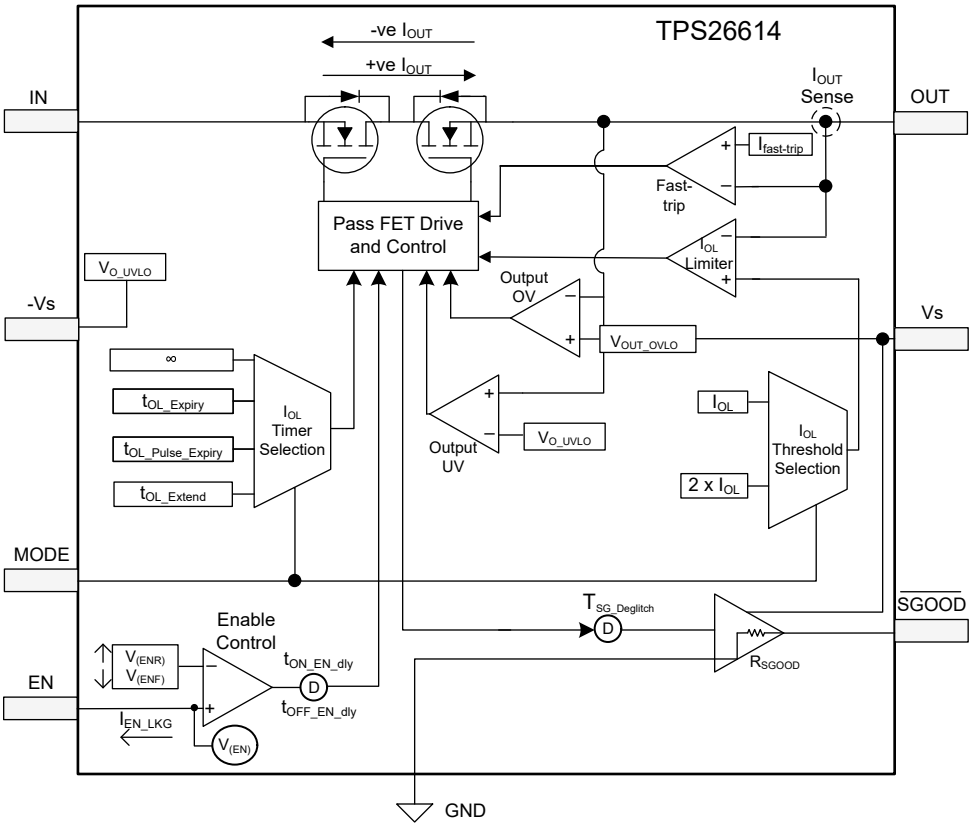


图 8-4. Functional Block Diagram for TPS26614

8.3 Feature Description

8.3.1 Overload Protection and Fast-Trip

The TPS2661x devices feature a fixed I_{OL} value of 32-mA typical, bidirectional current limit. For use in unipolar systems like 4 – 20-mA current loops where negative current is not desired, connect – Vs to GND to cut off when there is a flow of reverse current (OUT to IN). If the current tries to exceed the I_{OL} limit, the device regulates the current, eventually reducing the output voltage. Overload current threshold and time for overload protection can be selected by the MODE pin. See *Device Functional Modes* for details. The power dissipation across the device during current regulation is (V_{IN} – V_{OUT}) × I_{OUT}, which can heat up the device and lead to thermal shutdown. After thermal shutdown, the device goes into auto retry. The mode pin selects the auto retry period. See 表 8-3 and 图 8-24 for selection of the auto retry period.

The TPS2661x devices also feature a fast-trip comparator. During fast transient events like output short circuit, miswiring, hotplug, and so forth, the current through the device increases rapidly. Due to limited bandwidth, the current limit amplifier cannot respond quickly to these events . Hence, the fast-trip comparator architecture is included for fast turn OFF of the internal FET during these events. The device turns off the internal FETs within a time of $t_{(FASTTRIP)}$. See the *Timing Requirements* for $t_{(FASTTRIP)}$. The fast-trip circuit holds the internal FET off for a short duration (50 µs), after which, the device turns back on slowly, allowing the current-limit loop to regulate the output current to current limit as per MODE pin configuration. 图 8-5 and 图 8-7 illustrate the current limit behavior of TPS2661x devices. 图 8-8 illustrates the fast-trip protection of TPS2661x devices and 图 8-9 illustrates the auto-retry behavior in overload fault.

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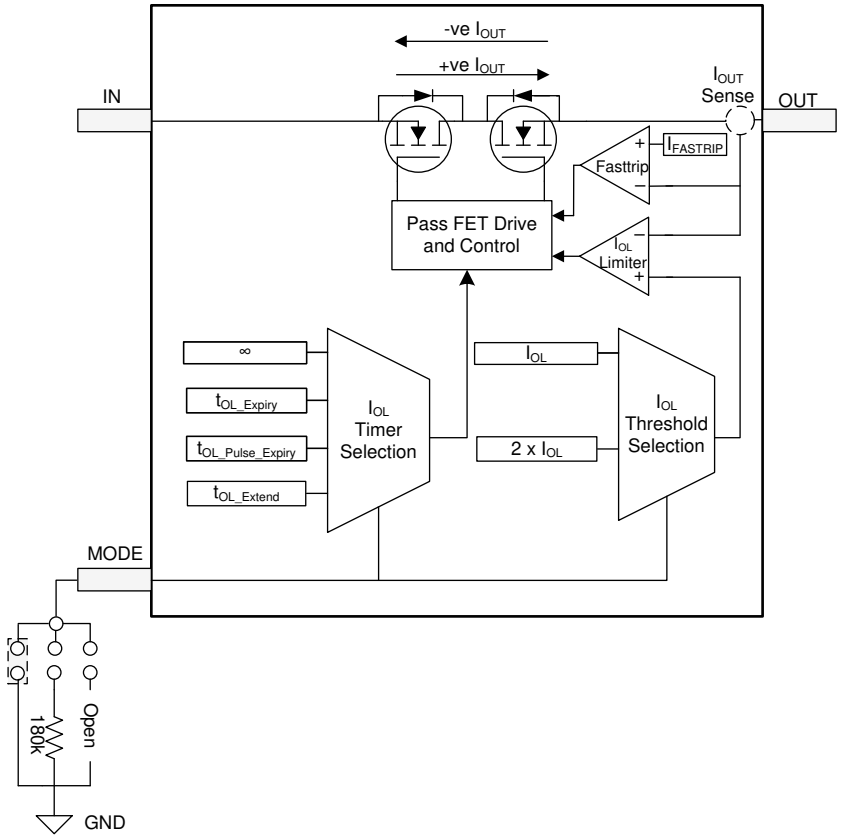


图 8-5. Overload Protection and Fast-Trip

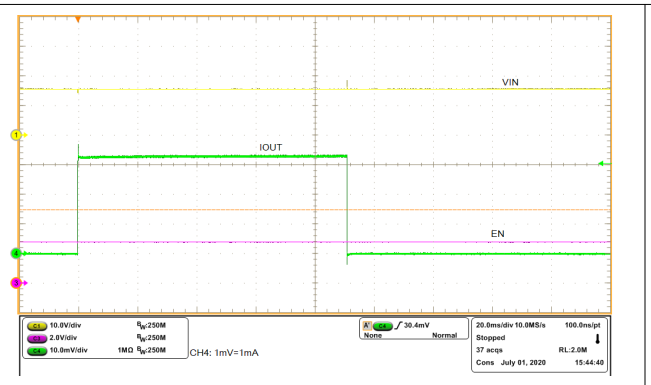


图 8-6. Current Limit Behavior for I_{OUT} < 2 × I_{OL} with MODE = GND

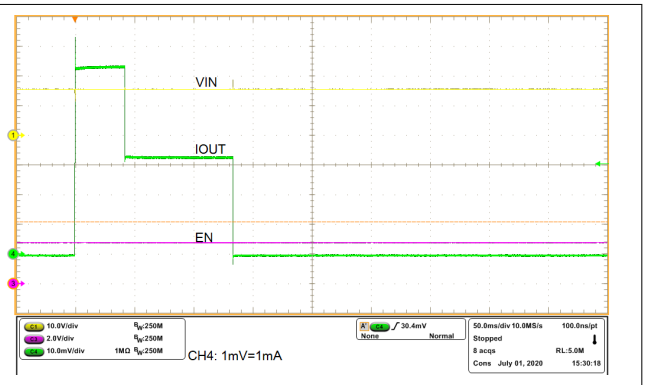


图 8-7. Current Limit Behavior for I_{OUT} > 2 × I_{OL} with MODE = 180 kΩ

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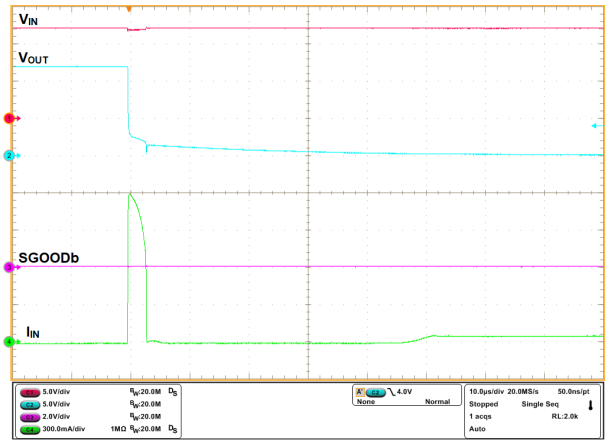


图 8-8. Fast-Trip Behavior

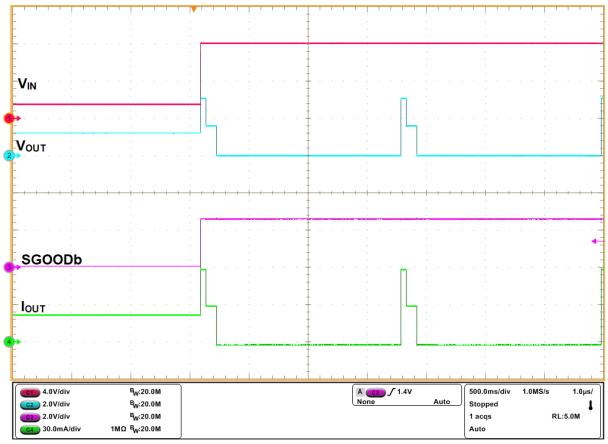


图 8-9. Auto-Retry Behavior

8.3.2 Reverse Current Blocking for Unipolar Current Inputs TPS26610, TPS26611 and TPS26612 (4 – 20 mA, 0 – 20 mA)

For reverse current blocking with TPS26610, TPS26611 and TPS26612 devices, connect burden resistor to GND and use single supply (+Vs, GND) with the device as shown in 图 8-10. In this configuration, the device blocks the reverse current (OUT to IN) when IN pin voltage is negative.

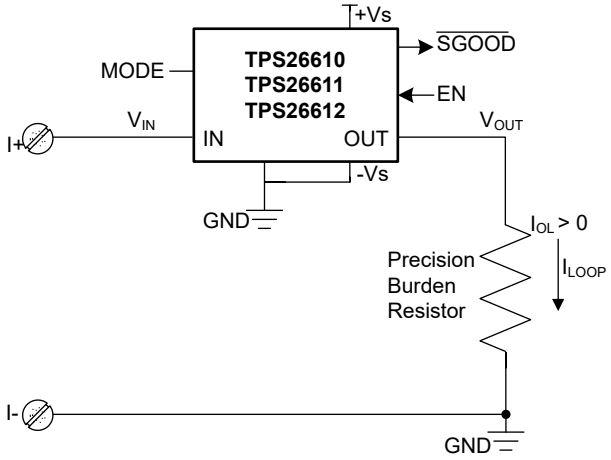


图 8-10. Reverse Current Blocking for Unipolar Current Inputs With TPS26610, TPS26611 and TPS26612

8.3.3 OUTPUT and INPUT Cutoff During Overvoltage, Undervoltage Due to Miswiring

表 8-1 summarizes the output and input cutoff present in TPS2661 devices

表 8-1. Output and Input Miswiring Protection in TPS2661 Devices

Device	Output Overvoltage	Output Undervoltage	Input Undervoltage
TPS26610	Y	Y	Y
TPS26611	Y	Y	Y
TPS26612	Y	Y	Y
TPS26613	Y	Y	N
TPS26614	Y	Y	N

8.3.3.1 Output Overvoltage With TPS2661x Devices

The TPS2661x devices provide protection from overvoltage events on OUT pin by turning off the internal pass FETs and cutting off the signal path whenever V_{OUT} goes above V_{OUT_OVLO} threshold. The signal path through

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TPS2661x is restored again when V_{OUT} goes below [V_{OUT_OVLO} – $V_{OUT_OVLO_Hyst}$] value. The device turns off the internal FETs within a time of $t_{OUT_OV_CUT}$ after output voltage has gone above V_{OUT_OVLO} threshold. See Timing Requirements in Specifications for $t_{OUT_OV_CUT}$.The device recovers from output overvoltage within a time of $t_{OUT_CUT_Rec}$ after output voltage has gone below [V_{OUT_OVLO} – $V_{OUT_OVLO_Hyst}$] value. See the *Timing Requirements* in Specifications for $t_{OUT_OV_CUT}$. 图 8-11 illustrates the output overvoltage protection in TPS2661x devices.

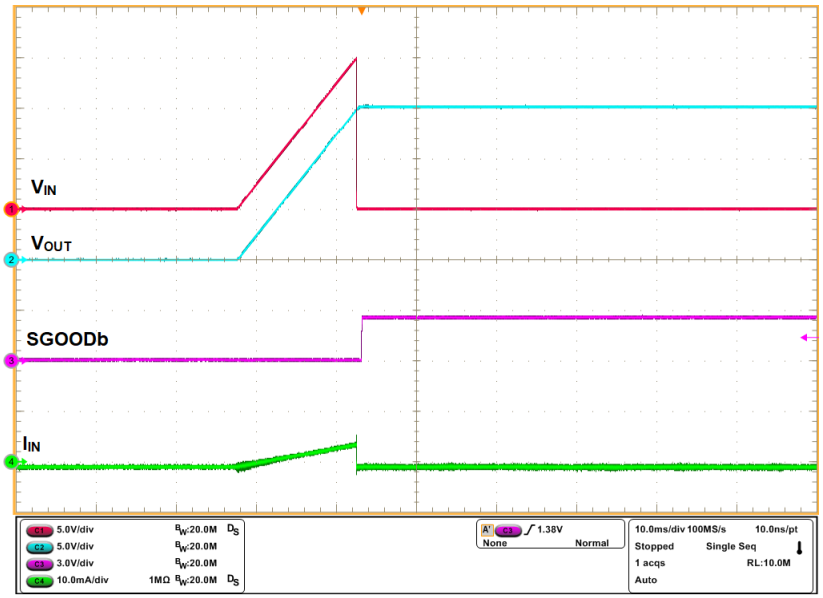


图 8-11. Output Overvoltage Protection

8.3.3.2 Output or Input Undervoltage With TPS26610, TPS26611 and TPS26612

TPS26610, TPS26611 and TPS26612 devices provide protection from undervoltage events on IN and OUT pins by turning off the internal pass FETs and cutting off the signal path whenever V_{OUT} or V_{IN} goes below V_{O/I_UVLO} threshold. The signal path through the device is restored again when V_{OUT} or V_{IN} goes above [V_{O/I_UVLO} – V_{O/I_UVLO_Hyst}] value. The device turns off the internal FETs within a time of t_{O/I_UV_CUT} after output or input voltage has gone below V_{O/I_UVLO} threshold. The device recovers from output or input undervoltage within a time of $t_{OUT_CUT_Rec}$ after output or input voltage has gone above [V_{O/I_UVLO} – V_{O/I_UVLO_Hyst}] voltage. See the *Timing Requirements* in Specifications for t_{O/I_UV_CUT} and $t_{OUT_CUT_Rec}$.

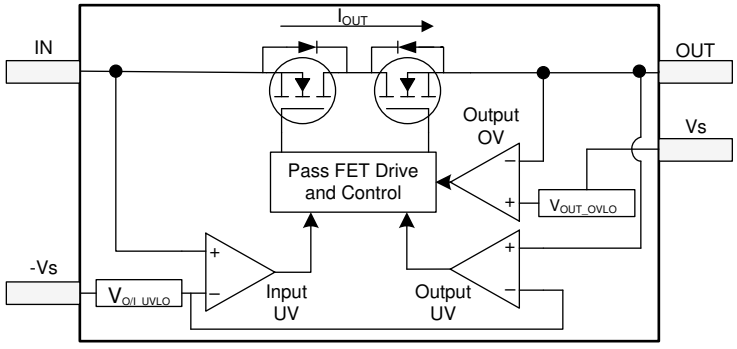


图 8-12. Output and Input Undervoltage Cutoff With TPS26610, TPS26611 and TPS26612

In case of overvoltage, undervoltage and miswiring events on IN and OUT pins, voltages exceeding Absolute Maximum Ratings (see *Specifications*) for IN and OUT Pins can damage the device. 图 8-13 and 图 8-14 illustrate the output and input undervoltage protection in these devices.

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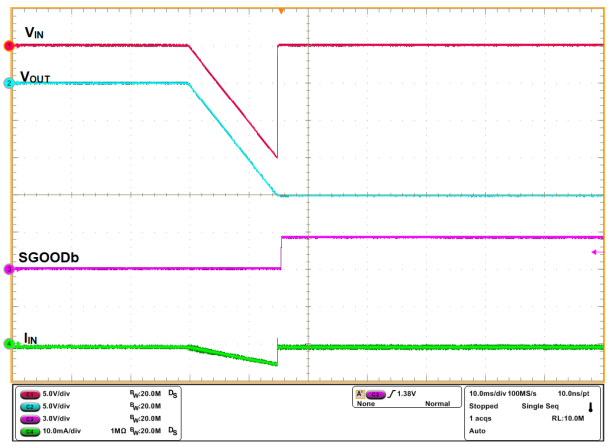


图 8-13. Output Undervoltage Protection

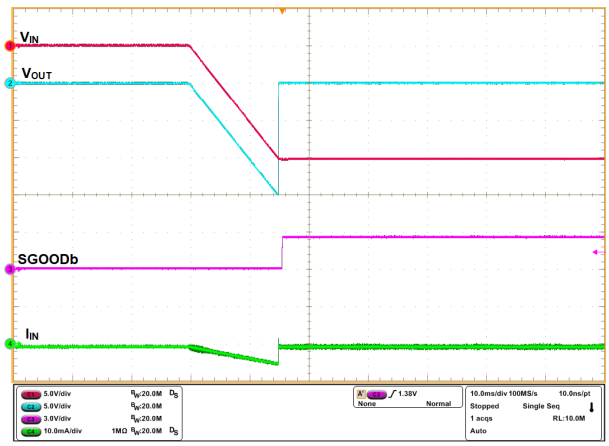


图 8-14. Input Undervoltage Protection

8.3.3.3 Output Undervoltage With TPS26613 and TPS26614

TPS26613 and TPS26614 devices provide protection from undervoltage events OUT pins by turning off the internal pass FETs and cutting off the signal path whenever VOUT goes below V_{O_UVLO} threshold. The signal path through the device is restored again when VOUT goes above [V_{O_UVLO} – $V_{O_UVLO_Hyst}$] value. The device turns off the internal FETs within a time of $t_{O_UV_CUT}$ after output voltage has gone below V_{O_UVLO} threshold. The device recovers from output undervoltage within a time of $t_{OUT_CUT_Rec}$ after output voltage has gone above [V_{O_UVLO} – $V_{O_UVLO_Hyst}$] voltage. See the *Timing Requirements* in Specifications for $t_{O_UV_CUT}$ and $t_{OUT_CUT_Rec}$.

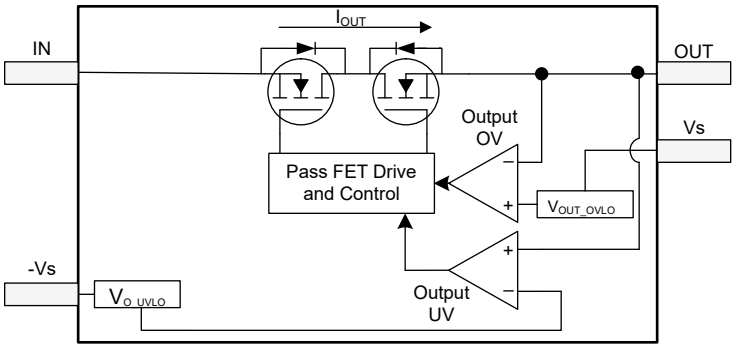


图 8-15. Output Undervoltage Cutoff in TPS26613 and TPS26614

8.3.4 External Power Supply (±Vs)

The TPS2661x devices are powered from an external +Vs/ – Vs supply. This feature ensures that the TPS2661x does not draw any current from the IN/OUT pins which carry current information. TPS26610 allows current conduction from IN to OUT pins when +Vs/-Vs supplies are not present. TPS26611 and TPS26612 devices need +Vs/ – Vs or +Vs/GND for operation.

For systems requiring positive and negative voltage on IN and OUT pins of TPS2661x, use bipolar supplies (+Vs and – Vs) with TPS2661x. Connect positive supply rail to +Vs and negative supply rail to – Vs pins. The device supports dual supplies from as low as ±2.25 V up to ±20 V.

For systems requiring only positive voltage on IN and OUT pins of TPS2661x, use unipolar supply (+Vs and GND) with TPS2661x .Connect positive supply rail to +Vs, and – Vs pin must be connected to GND of device. When powered from single supplies, TPS26610, TPS26611, TPS26613 and TPS26614 devices can be powered from +3 V up to +30 V and TPS26612 can be powered from +4 V up to +30 V.

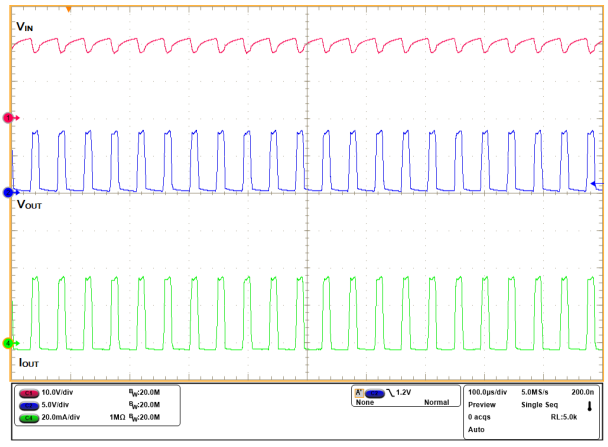
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The device turns on the internal FETs with a delay time of t_{ON_dly} after powering up of +Vs supply and turns off the internal FET with a delay time of t_{OFF_dly} after powering down of +Vs supply. See the *Timing Requirements* in Specifications for t_{ON_dly} and t_{OFF_dly}.

8.3.5 Loop Testing Without ±Vs Supply (Loop Power Mode in TPS26610, TPS26613 Only)

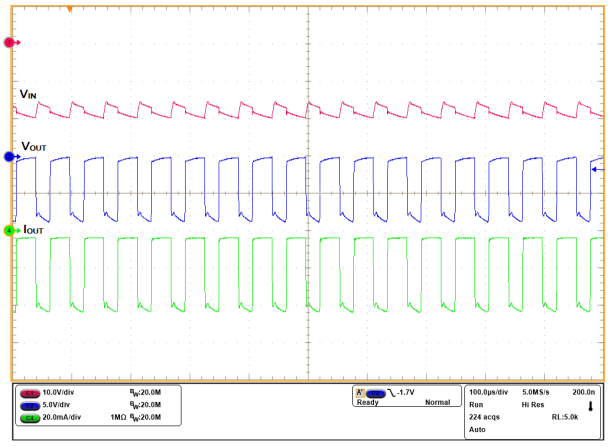
TPS26610 and TPS26613 devices allow a bipolar current limited conduction through the device even when the external +Vs/ – Vs supplies are not there. When the external supply is not there, the device switches to loop power mode and derives its operating power from the 4 – 20-mA or ±20-mA current loop. This feature enables the field installation engineer to check the wiring of the whole current loop system by passing a test current through the current loop without actually powering on the system. This feature also helps in design of safety critical redundant systems with two redundant measurements for the same current loop. In case power is not available in one system, a second system connected in the loop is still be able to read the current information because the loop is not broken. During loop testing without ±Vs supply, the device has a voltage drop of $V_{(IN-OUT)no_Vs}$, the current through device is limited to I_{OL_noVs}. During loop testing, the device draws a current of I_{OL_noVs} from IN pin. See the *Electrical Characteristics* in Specifications for $V_{(IN-OUT)no_Vs}$, I_{qno_Vs} and I_{OL_noVs}.

The device provides thermal protection during loop testing, if the power dissipation in device increases above 500 mW (typical), the devices turns off internal FET for short durations to limit the power dissipation. 图 8-16 and 图 8-17 illustrate the thermal protection during loop testing.



+Vs = 15 V, – Vs = – 15 V, R_{OUT} = 250 Ω, V_{IN} = 21 V

图 8-16. Thermal Protection During Loop Testing for I_{LOOP} > 0



+Vs = 15 V, – Vs = – 15 V, R_{OUT} = 250 Ω, V_{IN} = – 21 V

图 8-17. Thermal Protection During Loop Testing for I_{LOOP} < 0

8.3.5.1 Supply Sensing With VSNS for Loop Power Mode With TPS26610 and TPS26613

For the TPS26610 and TPS26613 devices, the set-point for transition to loop power mode can be set by connecting resistors (R1, R2) from +Vs pin to VSNS pin and GND pin as shown in 图 8-18. The set-point can be calculated as per 表 8-2. TI recommends to use resistors R1 and R2 for supply sensing when voltage across burden resistor (I_{LOOP} × R_{Burden}) is more than 1.8 V. If VSNS is left open or floating, the device transitions to loop power mode when +Vs is less than 1.8 V.

表 8-2. Supply Sensing With VSNS for Loop Power Mode

Device Power Mode	+Vs Voltage
±Vs supplies	+Vs ≥ $V_{(SNSR)}$ × (R1 + R2) / R2 (1)
Loop power	+Vs ≤ $V_{(SNSF)}$ × (R1 + R2) / R2 (1) (2)

(1) Use (R1 + R2) ≤ (+Vs) / (45 μA). For $V_{(SNSR)}$ and $V_{(SNSF)}$ values, see the *Electrical Characteristics*.
(2) Keep $V_{(SNSF)}$ × (R1 + R2) / R2 > (I_{LOOP} × R_{Burden})

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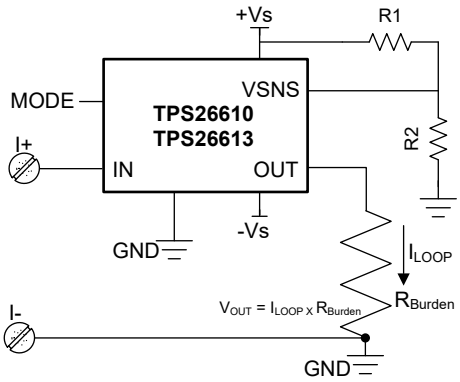
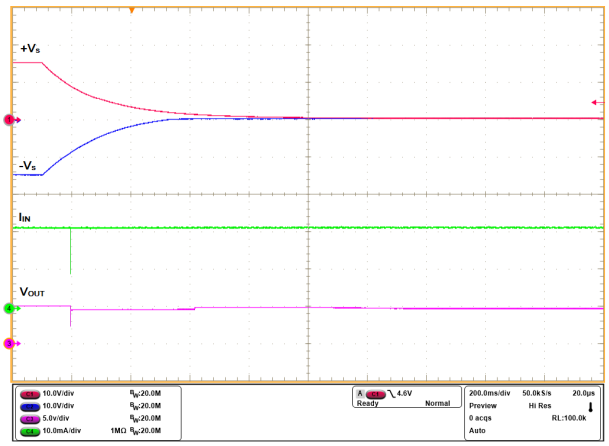
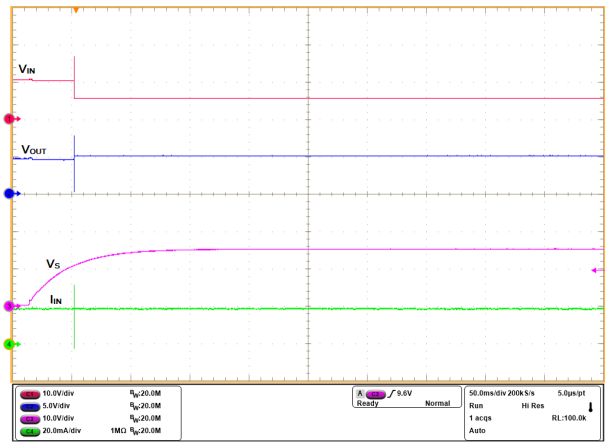


图 8-18. Supply Sensing With VSNS



+Vs = 15 V, – Vs = – 15 V, R_{OUT} = 250 Ω, MODE = GND

图 8-19. Transition to Loop Power With R1 = 47 kΩ and R2 = 6.8 kΩ for Supply Sensing



+Vs = 15 V, – Vs = – 15 V, R_{OUT} = 250 Ω, MODE = GND

图 8-20. Transition to ± Vs Supplies Power with R1 = 47 kΩ and R2 = 6.8 kΩ for supply Sensing

8.3.6 Enable Control With TPS26611, TPS26612, and TPS26614

TPS26611, TPS26612, and TPS26614 devices feature an EN pin for externally controlling the device through a GPIO pin. To enable the device, EN pin can be left floating. The pin is internally pulled up with $V_{(EN)}$.

EN can also be made high with external voltage more than $V_{(ENR)}$ but less that or equal to 5 V. The internal FETs are turned off when EN is pulled below $V_{(ENF)}$. EN pin can source and sink a current of $I_{(EN_LKG)}$. See *Electrical Characteristics* for $V_{(ENF)}$, $V_{(ENR)}$ and $I_{(EN_LKG)}$. The EN feature helps the system designer to design universal voltage and current analog inputs and outputs where a lot of pin multiplexing options are made available to the end user. For turn-on and turn-off delay with EN pin, see $t_{ON_EN_dly}$ and $t_{OFF_EN_dly}$ in *Timing Requirements*. 图 8-22 and 图 8-23 illustrate the turn-on and turn-off control with enable pin.

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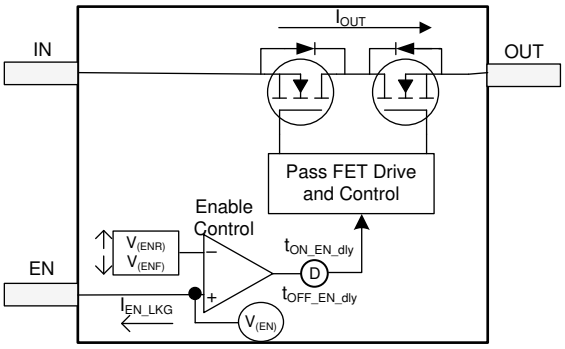


图 8-21. Enable Control

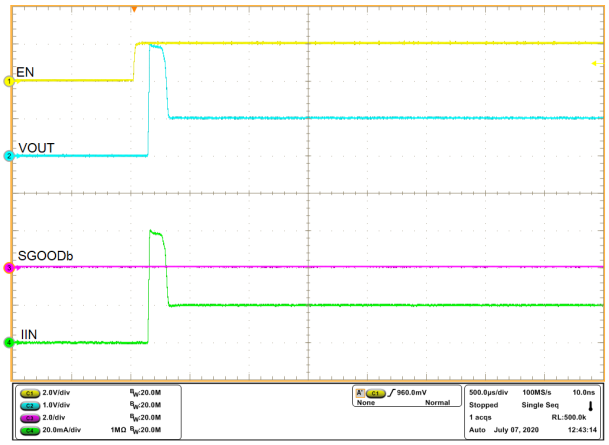


图 8-22. Turn-On With EN Pin

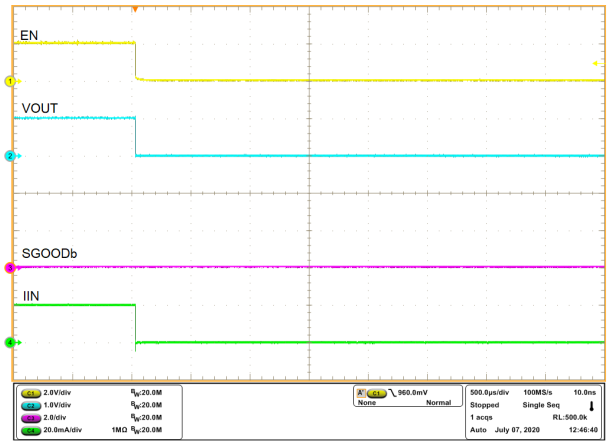


图 8-23. Turn-Off With EN Pin

8.3.7 Signal Good Indicator ($\overline{\text{SGOOD}}$)

The TPS2661x provides an indication of the current signal flowing through pass FETs on the $\overline{\text{SGOOD}}$ pin. Whenever the device is in normal operating condition, the $\overline{\text{SGOOD}}$ gives a signal LOW output. However in below cases when the device is outside normal operating condition, the $\overline{\text{SGOOD}}$ pin goes HIGH:

- Device current is > I_{OL} (32-mA typical)
- OUT goes outside +Vs/ – Vs supply
- IN goes below – Vs supply rail (for TPS26610, TPS26611, and TPS26612 only)
- Device shuts down due to thermal limit or current limit

The $\overline{\text{SGOOD}}$ pin is also capable of driving an external LED to give a visual indication whenever the system is outside normal operating conditions.

The $\overline{\text{SGOOD}}$ pin sourcing current is derived from +Vs supply rail. For de-glitch delays in assertion and de-assertion of $\overline{\text{SGOOD}}$, see $T_{SG_Deglitch}$ in *Timing Requirements* in Specifications.

8.4 Device Functional Modes

The device can provide higher current up to 2 × I_{OL} for short durations. MODE pin of the device configures the behavior of the device for higher current. 表 8-3 and 图 8-24 describe the device behavior in different modes for I_{OL} > 0.

With MODE = GND, the device limits the current to I_{OL} value for I_{OUT} > I_{OL}.

With MODE = OPEN, the device limits the output current as:

- For I_{OL} < I_{OUT} < 2 × I_{OL}, the device allows current up to 2 × I_{OL} for a duration of $t_{OL_Pulse_Expiry}$ and then limits the current to I_{OL} value for a duration t_{OL_Expiry}.

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- For 2 × I_{OL} < I_{OUT} < $I_{(FASTRIP)}$, the device limits the current 2 × I_{OL} value and for a duration of $t_{OL_Pulse_Expiry}$ and then limits the current to I_{OL} value for a duration t_{OL_Expiry}.

After the completion of t_{OL_Expiry} period, the device goes into auto-retry.

With MODE = 180 kΩ, the device limits the output current as:

- For I_{OL}< I_{OUT} < 2 × I_{OL}, the device allows current up to 2 × I_{OL} for a duration of t_{OL_Extend} and then limits the current to I_{OL} value for a duration t_{OL_Expiry}.
- For 2 × I_{OL} < I_{OUT} < $I_{(FASTRIP)}$, the device limits the current 2 × I_{OL} value and for a duration of $t_{OL_Pulse_Expiry}$ and then limits the current to I_{OL} value for a duration t_{OL_Expiry}.

After the completion of t_{OL_Expiry} period, the device goes into auto-retry. If the device heats up during overload and the device temperature exceeds $T_{(TSD)}$ value, the device turns off the internal pass FETs. As the device cools down and its temperature goes below [$T_{(TSD)}$ – $T_{(TSDHyst)}$] value, the device goes into auto-retry.

表 8-3. Device Operation Under Different MODE Configurations for I_{OL} > 0

MODE Pin Configuration	I_{OUT} < I_{OL} (32 mA)	I_{OL} (32 mA) < I_{OUT} < 2 × I_{OL} (60 mA)	2 × I_{OL} (60 mA) < I_{OUT} < $I_{(FASTRIP)}$	Auto-Retry Time
Shorted to GND	Current flows normally	Current limited to I_{OL} for a duration of t_{OL_Expiry} (100 ms). t_{OL_Expiry} (100 ms) timer starts when I_{OUT} exceeds I_{OL}.	Current limited to I_{OL} for a duration of t_{OL_Expiry} (100 ms). t_{OL_Expiry} (100 ms) timer starts when I_{OUT} exceed I_{OL}.	t_{RETRY1} (800 ms)
Open	Current flows normally	Device allows current for $t_{OL_Pulse_Expiry}$ (50 ms) time after which it is limited to I_{OL} for t_{OL_Expiry} (100 ms) time and then auto retry. $t_{OL_Pulse_Expiry}$ (50 ms) timer starts when I_{OUT} exceeds I_{OL}.	Current limited to 2 × I_{OL} for $t_{OL_Pulse_Expiry}$ (50 ms) time after which it is limited to I_{OL} for t_{OL_Expiry} (100 ms) time and then auto retry. $t_{OL_Pulse_Expiry}$ (50 ms) timer starts when I_{OUT} exceeds I_{OL}.	t_{RETRY1} (800 ms)
180 kΩ from MODE to GND	Current flows normally	Device allows current for t_{OL_Extend} (5 s) time after which it is limited to I_{OL} for t_{OL_Expiry} (100 ms) time and then auto retry. t_{OL_Extend} (5 s) timer starts when I_{OUT} exceeds I_{OL}.	Current limited to 2 × I_{OL} for $t_{OL_Pulse_Expiry}$ (50 ms) time after which it is limited to I_{OL} for t_{OL_Expiry} (100 ms) time and then auto retry. $t_{OL_Pulse_Expiry}$ (50ms) timer starts when I_{OUT} exceeds I_{OL}.	t_{RETRY2} (1.6 s)

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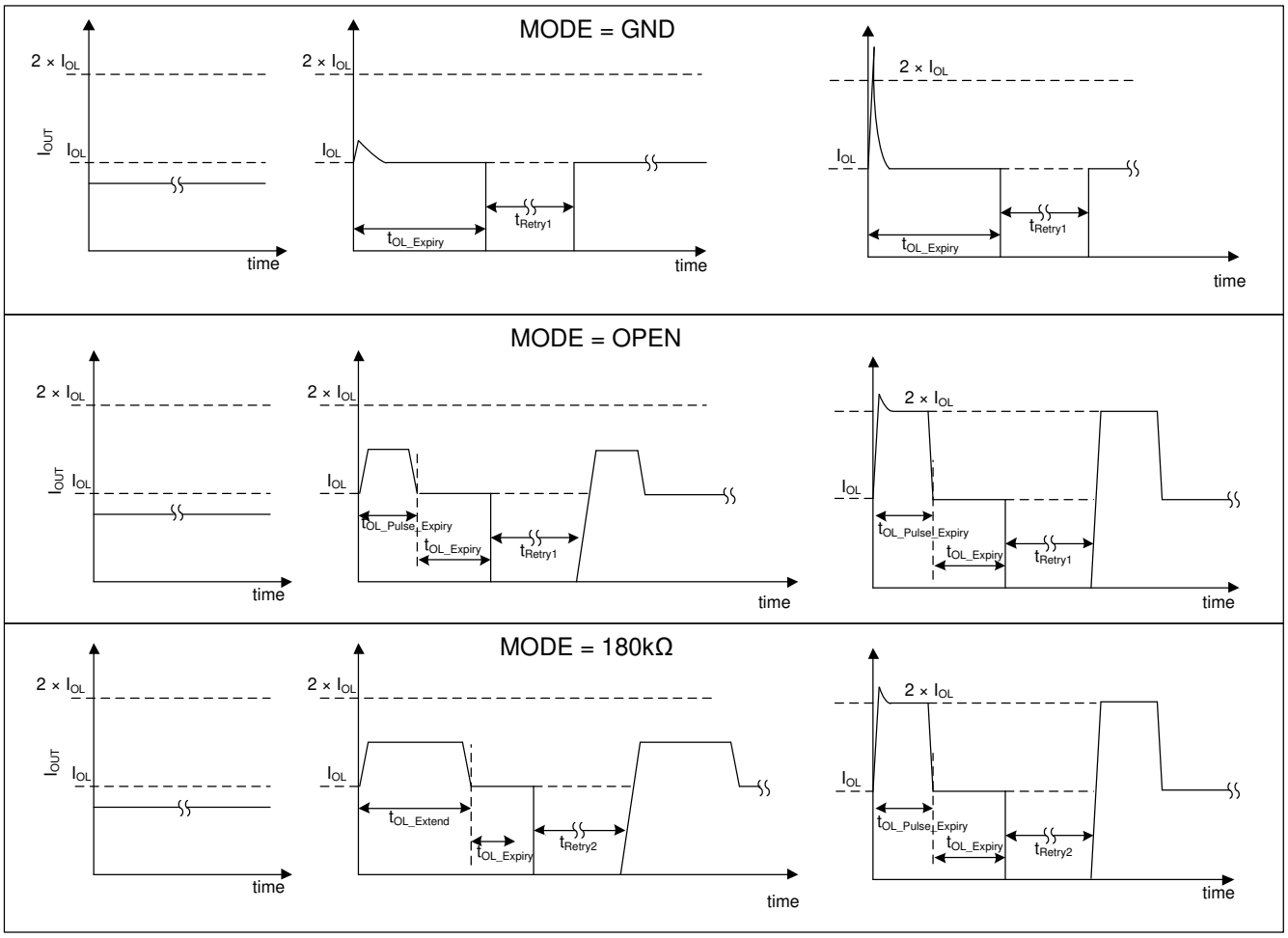


图 8-24. Device Operation Under Different MODE Configurations for I_{OL} > 0

表 8-4 and 图 8-25 describe the device behavior in different modes for I_{OL} < 0.

表 8-4. Device Operation Under Different MODE Configurations for I_{OL} < 0

MODE Pin Configuration	I_{OUT} > – I_{OL} (– 32 mA)	– 2 × I_{OL}(– 60 mA) < I_{OUT} < – I_{OL} (– 32 mA)	– $I_{(FASTRIP)}$ < I_{OUT} < – 2 × I_{OL} (– 60 mA)	Auto-Retry Time
Shorted to GND or Open or 180 kΩ from MODE to GND	Current flows normally	Current limited to I_{OL} for a duration of t_{OL_Expiry} (100 ms). t_{OL_Expiry} (100 ms) timer starts when I_{OUT} exceeds I_{OL}.	Current limited to I_{OL} for a duration of t_{OL_Expiry} (100ms). t_{OL_Expiry} (100ms) timer starts when I_{OUT} exceed I_{OL}.	t_{RETRY1} (800 ms)

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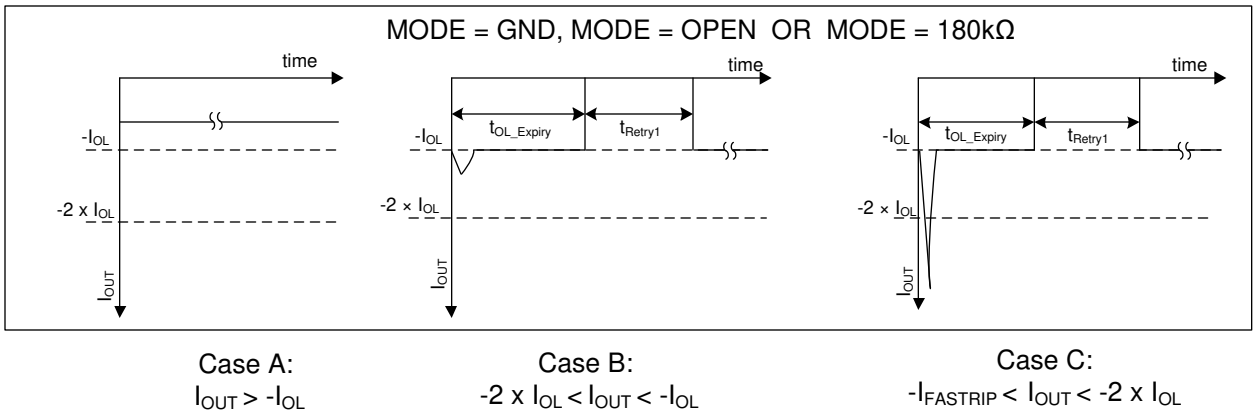


图 8-25. Device Operation Under Different MODE Configurations for I_{OL} < 0

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The TPS2661x is an industrial current loop protector, providing a robust signal line protection in a wide range of industrial and automation systems. It is suitable for protection of all kinds of current loops like the 4 – 20-mA or ±20-mA current loops. TPS26610 is suitable for protection in current inputs whereas TPS26611 is suitable for protection in multiplexed V/I inputs.

TPS26612 is suitable for protection in power supply of two wire current transmitters. With disabled auto-retry time for first overload event, TPS26612 enables startup of power hungry transmitters requiring higher start up current for longer durations.

TPS26611 and TPS26612 devices can be also used to protect voltage outputs or digital communication signals like UART from miswiring of power supplies at these outputs. The device breaks the signal path by turning off the FETs when there is a voltage higher than supply voltage and thus keeping the system protected.

TPS2661x provides complete protection from industrial surge transients (IEC61000-4-5) and provides immunity from industrial fast transients (IEC610000-4-4) for signal lines.

9.2 Typical Application: Analog Input Protection for Current Inputs with TPS26610

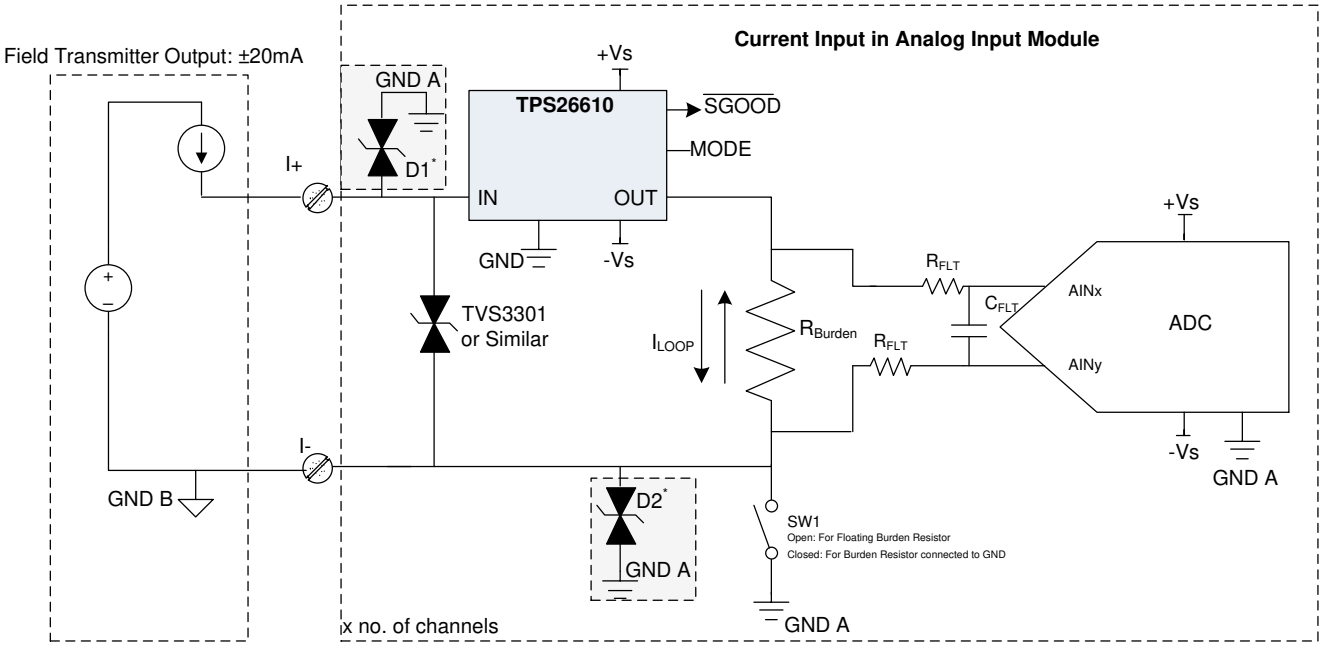


图 9-1. Current Input Protection in AI Module

A. TVS Diodes D1*, D2* are required for protection from surge transients (IEC61000-4-5) when burden resistor is floating (SW1 = Open).

TPS26610 can be used for protection of current inputs in an Analog Input module as shown in 图 9-1. The current signal is measured by ADC across R_{burden}. Bipolar current limit of ±32 mA ensures that the precision burden resistor as well as the ADC front end stays well protected against any unwanted voltages or currents caused due to faulty transmitter or miswiring. High Voltage rating of IN pin of TPS26610 ensures that it also protects the system from surge and EFT events as well. For reverse current blocking (OUT to IN), connect burden resistor to GND (SW1 = Closed) and used single supply (+Vs,GND) with TPS26610.

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9.2.1 Design Requirements

Table 3 shows the design requirements for current input protection with TPS26610.

表 9-1. Design Requirements

DESIGN PARAMETER		EXAMPLE VALUE
$I_{(IN)}$	Input current	±20 mA
$V_{(IN)}$	Input voltage	– V_s to 50 V
$V_{(OUT)}$	Output voltage	±V_s
$I_{(LIM)}$	Current limit	±30 mA
R_{Burden}	Burden resistance	50 to 250 Ω

9.2.2 Detailed Design Procedure for Current Inputs with TPS26610

9.2.2.1 Selecting ±Vs Supplies for TPS26610

Select the ±Vs supplies for TPS2661x devices higher than absolute analog input voltage for ADC inputs.

TPS2661x devices have undervoltage and overvoltage protection on OUT pin and the internal FETs are turned off if OUT pin has voltage higher than +Vs or lower than – Vs.

TPS2661x devices also have undervoltage protection on IN pin and the internal FETs are turned off if IN pin has a voltage lower than – Vs. See *External Power Supply* for using unipolar or bipolar supply with TPS2661x.

9.2.2.2 Selecting R_{Burden}

The value of R_{burden} must be selected to meet the analog the input range of the ADC for the loop current range. In case of miswiring faults to field supplies, the maximum current and power dissipated in R_{burden} is decided by MODE configuration of TPS26610 device.

表 9-2. Selection of R_{burden}

R_{burden} (Ω)	MODE Configuration	Maximum Current in R_{burden}(mA)	Maximum Power Dissipated in R_{burden} (mW)
50	MODE = GND	40	80
100	MODE = GND	40	160
250	MODE = GND	40	400
50	MODE = OPEN or 180 kΩ	70	245(1)
100	MODE = OPEN or 180 kΩ	70	490(1)
250	MODE = OPEN or 180 kΩ	70	1225(1)

(1) Power dissipated only for a pulse duration of 50 ms

9.2.2.3 Selecting MODE Configuration for TPS26610

For minimum power dissipation in burden resistor, use MODE = GND. See *Device Functional Modes* for selecting the mode configuration.

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9.2.3 Application Performance Plots for Current Inputs with TPS26610

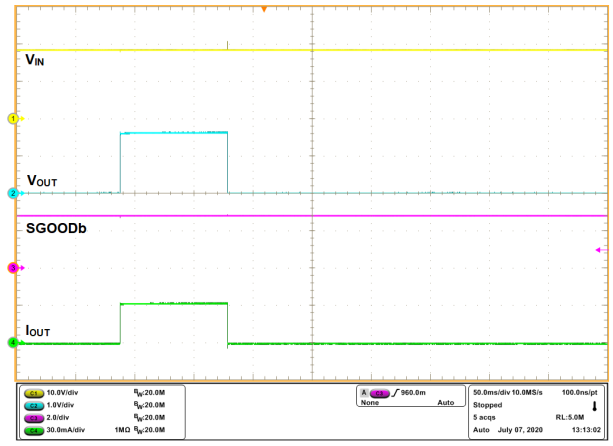


图 9-2. Current Limiting with MODE = GND, R_{burden} = 50 Ω

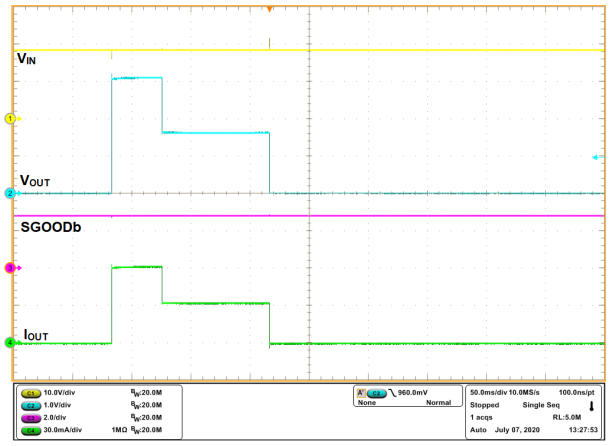


图 9-3. Current Limiting with MODE = OPEN, R_{burden} = 50 Ω

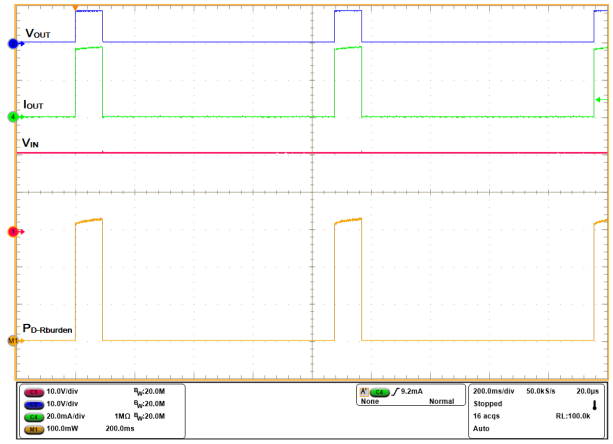


图 9-4. Power Dissipation in R_{burden} = 250 Ω with MODE = GND

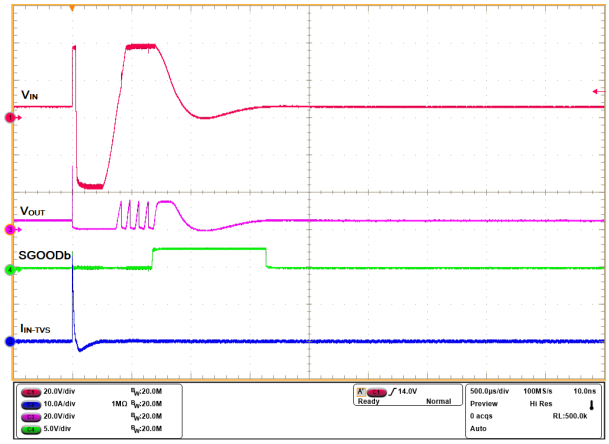


图 9-5. IEC61000-4-5 (+1 kV, 42 Ω) Signal Line Surge immunity with TVS3301 at IN

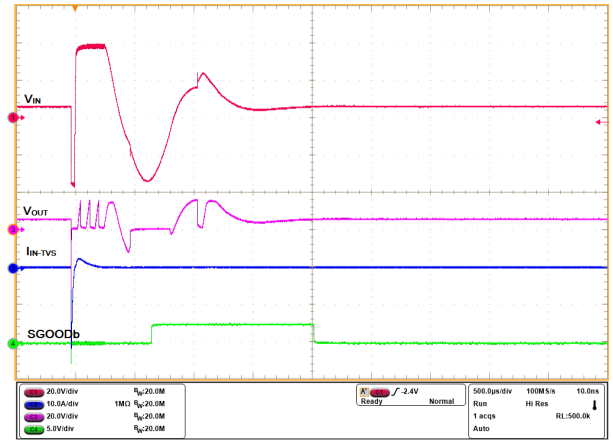


图 9-6. IEC61000-4-5 (– 1 kV, 42 Ω) Signal Line Surge immunity with TVS3301 at IN

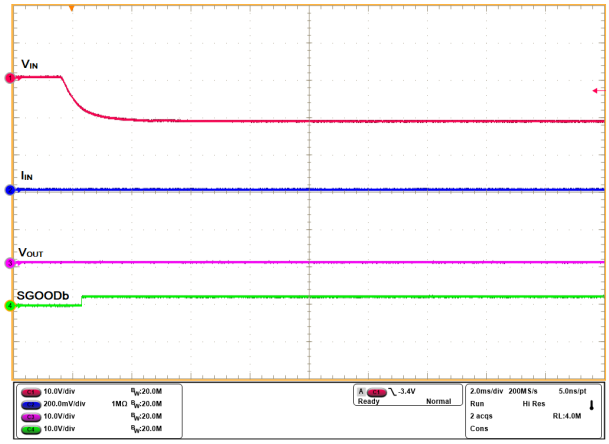


图 9-7. Reverse Current blocking with VIN = – 12 V, – V_S = GND and SW1 = Closed

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9.3 Typical Application: Analog Input Protection for Multiplexed Current and Voltage Inputs with TPS26611

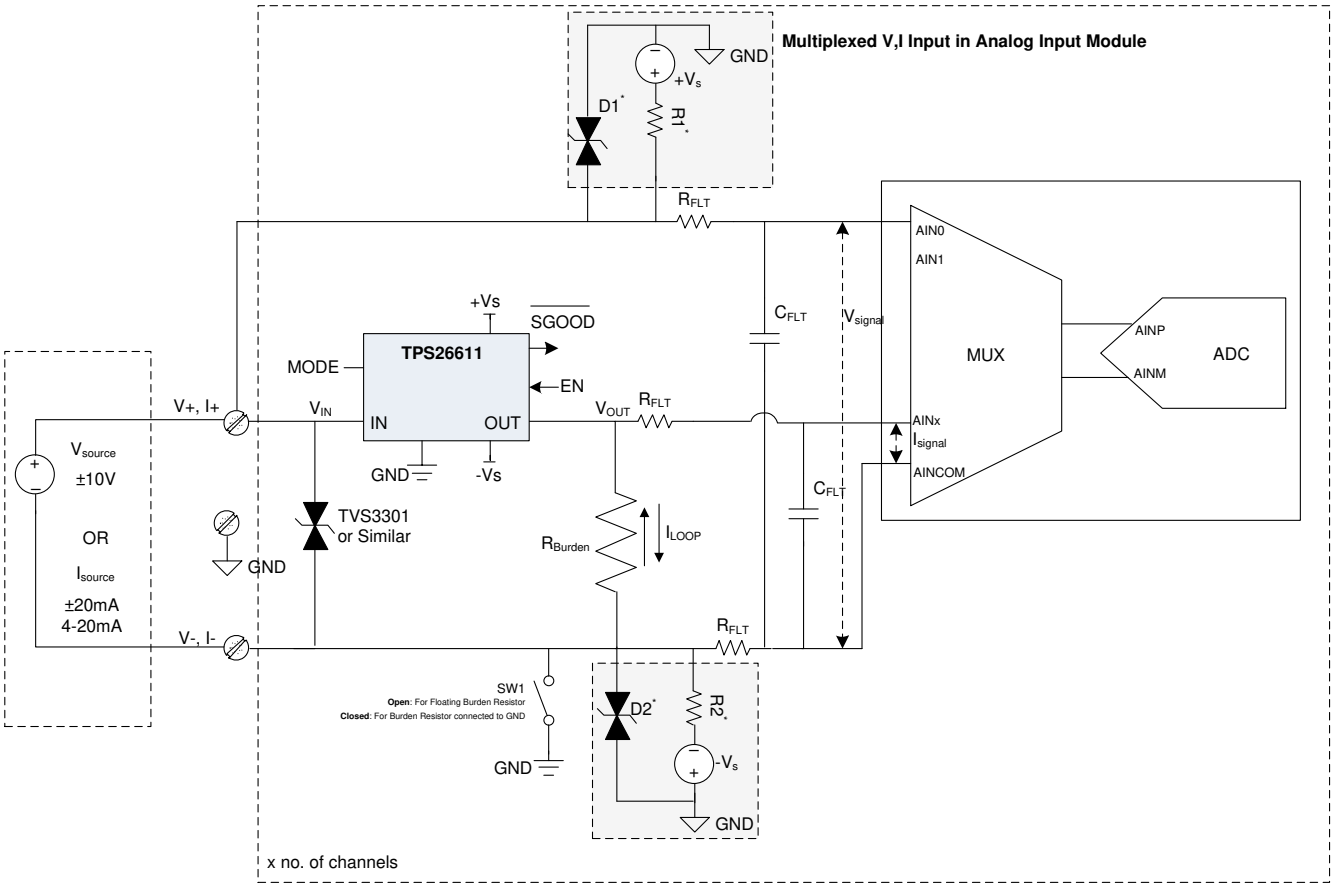


图 9-8. Protection for Multiplexed V/I Inputs in AI Module

A. Bias Resistors R1*, R2* are required for setting the common mode voltage for voltage input (EN = 0) when burden resistor is floating (SW1 = Open).

B. Diodes D1*, D2* are required surge protection when burden resistor is floating (SW1 = Open).

TPS26611 can be used for protection of multiplexed inputs in an Analog Input module as shown in 图 9-8. For this configuration, connect the IN pin of TPS26611 to one channel of the ADC for voltage measurement and connect OUT pin of TPS26611 to the other channel of ADC for current measurement. EN pin of TPS26611 can be used to swtch between current and voltage measurements. With EN = 0, the internal FETs of TPS26611 are turned off and voltage signal can be measured by ADC between AIN0 and AINCOM pins. Whereas with EN = 1, the internal FETs of TPS26611 are turned on and current signal can be measured by ADC between AINx and AINCOM pins.

9.3.1 Design Requirements

表 9-3. Design Parameters

PARAMETER	VALUE
Input Current (I_{IN})	±20 mA
Input Voltage (V_{IN})	± 10 V
Current Limit for (I_{IN})	±32 mA
R_{Burden}	50 to 250 Ω

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9.3.2 Detailed Design Procedure for Analog Input Protection for Multiplexed Current and Voltage Inputs with TPS26611

9.3.2.1 Selecting ±V_S Supplies for TPS26611

See Vs supply selection in *Typical Application: Analog Input Protection for Current Inputs with TPS26610*.

9.3.2.2 Selecting MODE Configuration for TPS26611

For minimum power dissipation in burden resistor, use MODE = GND. See *Device Functional Modes* for selecting the mode configuration.

9.3.2.3 Selecting Bias Resistors R1, R2 for Setting Common Mode Voltage for Voltage Inputs

For setting the common mode voltage with floating burden resistor (SW1 = Open), bias resistor R1 and R2 are required.

Resistors R1, R2 provide low impedance path for off state (EN = 0) leakage currents from IN and OUT pins of TPS26611. R1, R2 are selected to keep bias current less than 4 μA through these resistors for current measurements with R_{burden} (EN = 1).

表 9-4. Selection of Bias Resistors R1, R2

Analog Input Voltage for ADC	±V_S Supplies	Bias Current Through R1, R2	R1	R2
±10 V	±15 V	< 4 μA	1.39 to 1.66 MΩ	6.67 to 6.94 MΩ
±12.5 V	±15 V	< 4 μA	1.35 to 1.71 MΩ	6.62 to 6.98 MΩ
±15 V	±18 V	< 4 μA	1.29 to 1.75 MΩ	6.58 to 7.04 MΩ

9.3.3 Application Performance Plots for V/I Inputs with TPS26611

In addition to current limiting, reduced power dissipation in burden resistor, reverse current blocking and surge protection illustrated in *Application Performance Plots for Current Inputs with TPS26610*, TPS26611 provides enable control for selecting between voltage and current inputs.

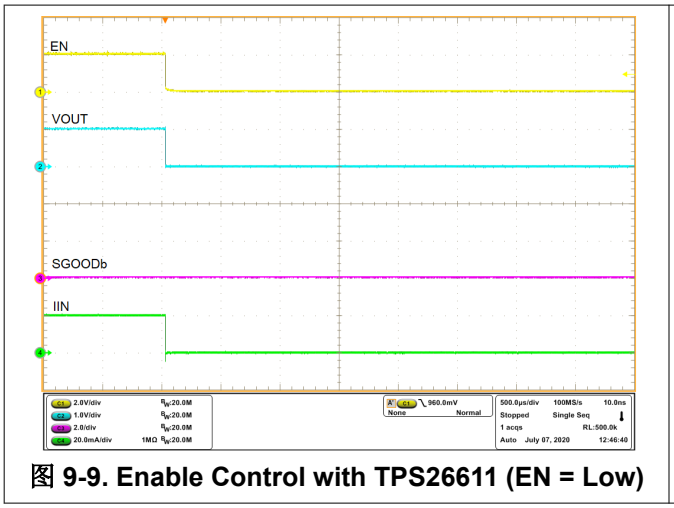


图 9-9. Enable Control with TPS26611 (EN = Low)

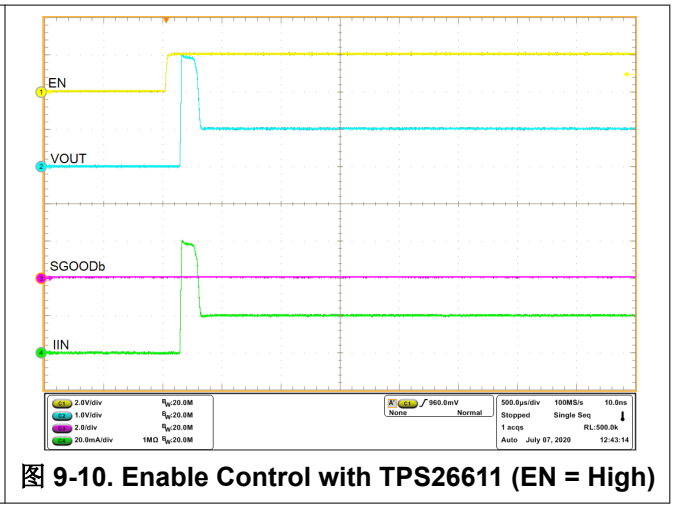


图 9-10. Enable Control with TPS26611 (EN = High)

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9.4 System Examples

9.4.1 Power Supply Protection of 2-Wire Transmitter with TPS26612

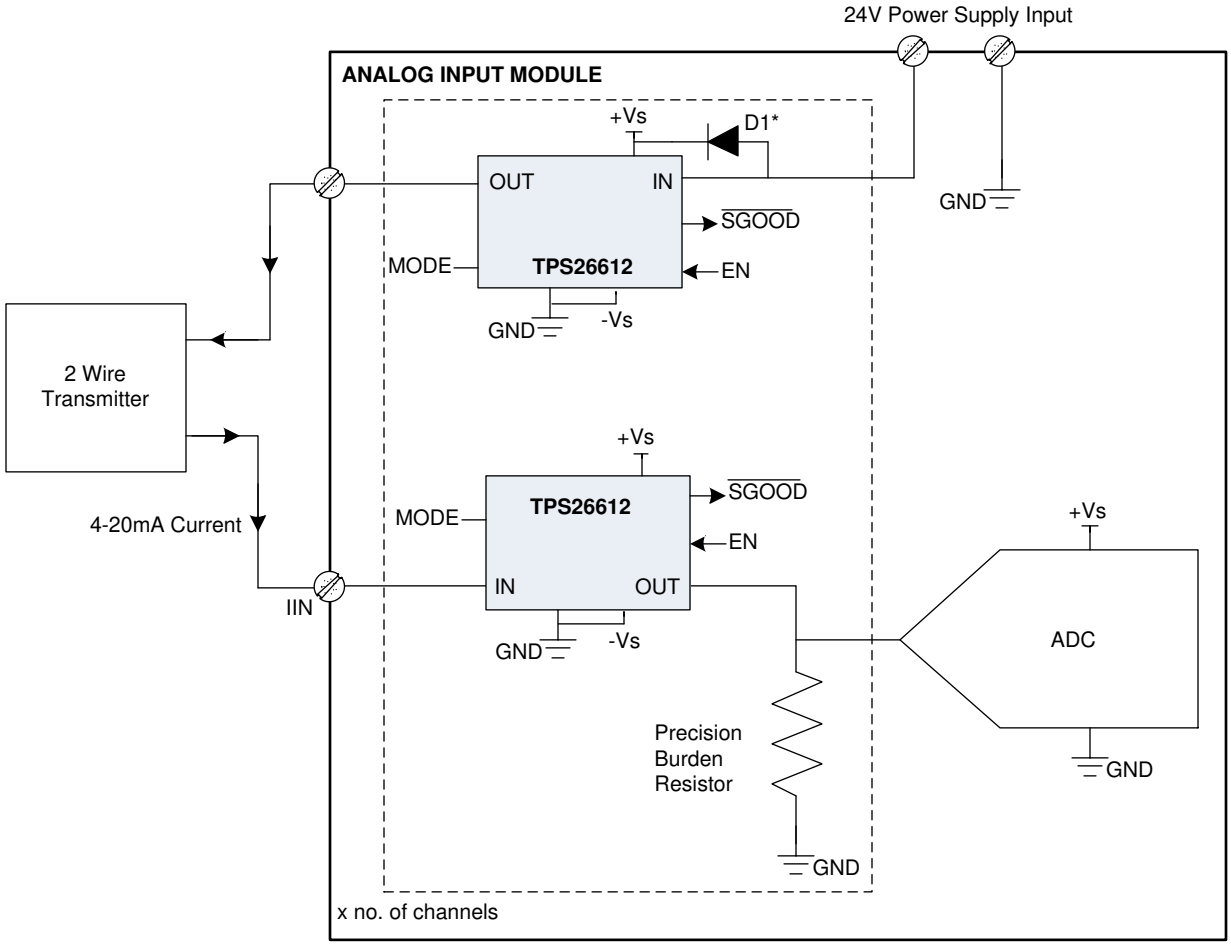
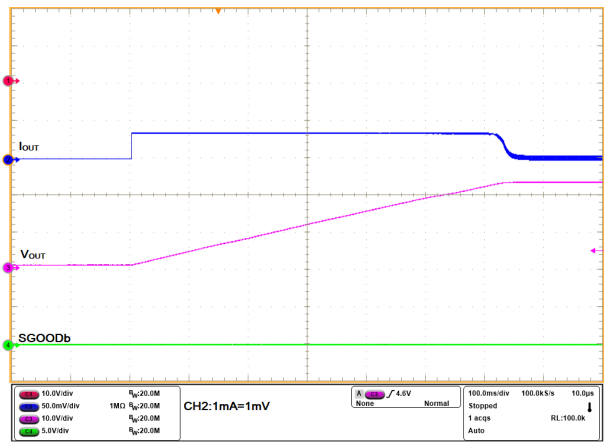


图 9-11. Power Supply Protection for 2-Wire Transmitter with TPS26612

TPS26612 can be used for protection of power supply powering a two wire field transmitter as shown in 图 9-11. Connect an external signal diode (D1) from IN to +Vs pin of TPS26612 in case of external field supply to protect the system from miswiring. In case the supply is internal to the module and miswiring is not a possibility, the signal diode (D1) is not needed. TPS26612 device includes higher threshold for overvoltage protection on OUT to accommodate the voltage drop of diode (D1) between IN and +Vs.

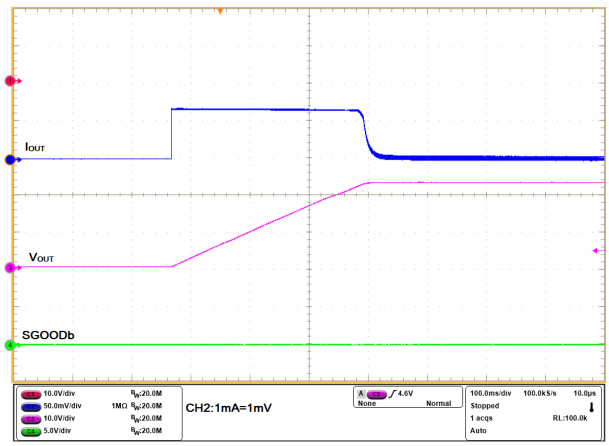
TPS26612 has over-load expiry time (t_{OL_expiry}) disabled for the first overload fault after power-up up to a duration of t_{AR_dis} (5 sec). With overload expiry time disabled, TPS26612 is able to power up 2-wire transmitters requiring higher start-up for longer durations (up to 5 sec.). The current limit threshold (I_{OL} or 2 x I_{OL}) for startup can be selected by MODE pin.

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V_{IN} = 24 V, C_{OUT} = 1 mF

图 9-12. TPS26612: Startup of 2-Wire transmitter with MODE = GND, I_{OUT} = 30 mA

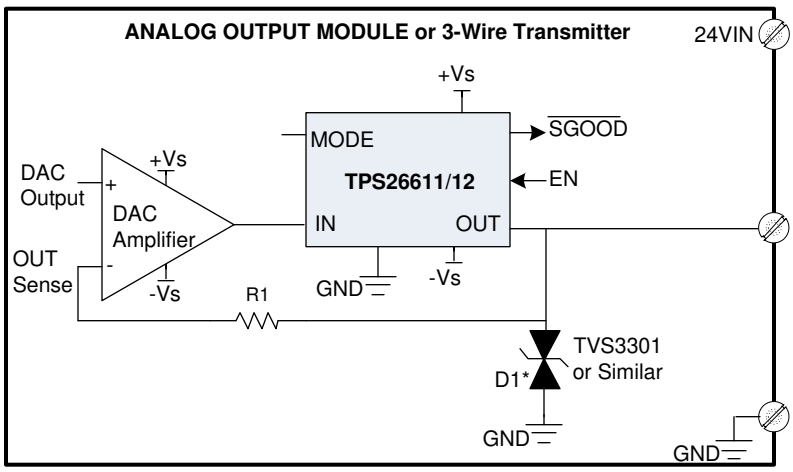


V_{IN} = 24 V, C_{OUT} = 1 mF

图 9-13. TPS26612: Startup of 2-Wire transmitter with MODE = Open, I_{OUT} = 60 mA

During the first overload fault, if the junction temperature reaches T_{SD}, the device turns off the internal FETs and turns on as the junction temperature goes below [T_{TSD} – $T_{TSDHyst}$].

9.4.2 Protection of 3-Wire Transmitters and Analog Output Modules With TPS26611, TPS26612



Diode (D1) is required for Signal line Surge (IEC61000-4-5) protection.

图 9-14. Analog Output Protection with TPS26611 or TPS26612

TPS26611 or TPS26612 can be used for protection of the analog output a 3/4-wire transmitter and analog output module against any high voltage field miswiring as shown in 图 9-14. The OUT pin voltage is monitored with respect to the +Vs/ – Vs supply voltages. If the OUT voltage goes outside the +Vs/ – Vs supply rails, the FETs cutoff current conduction path and protects the whole system.The voltage at OUT pin of TPS2661x can be sensed by DAC amplifier to compensate for R_{ON} of TPS2661x

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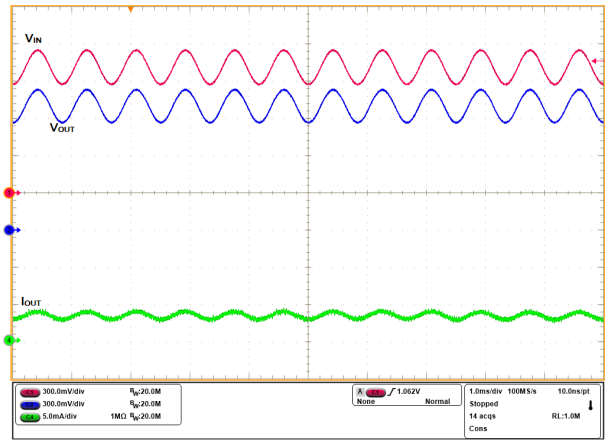


图 9-15. 1.2-kHz HART Signal Through TPS2661x with R_{OUT} = 250 Ω

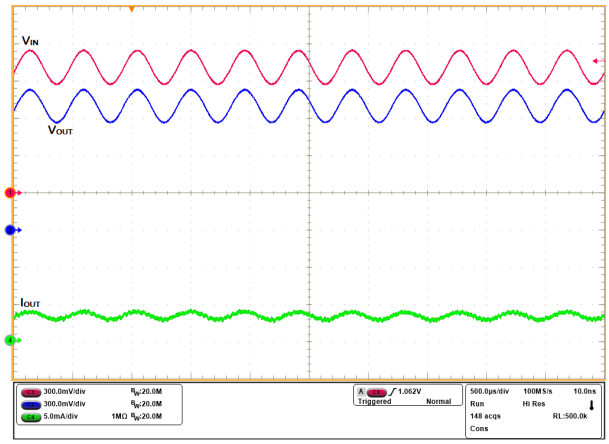


图 9-16. 2.2-kHz HART Signal Through TPS2661x with R_{OUT} = 250 Ω

9.4.3 UART IO Protection With TPS26611, TPS26612

TPS26611 or TPS26612 can be used for protection of UART IO lines as shown in 图 9-17. The OUT pin voltage is monitored with respect to the +Vs/ – Vs supply voltages. If the OUT voltage goes outside the +Vs/ – Vs supply rails, the FETs cutoff the current conduction path and protects the whole system.

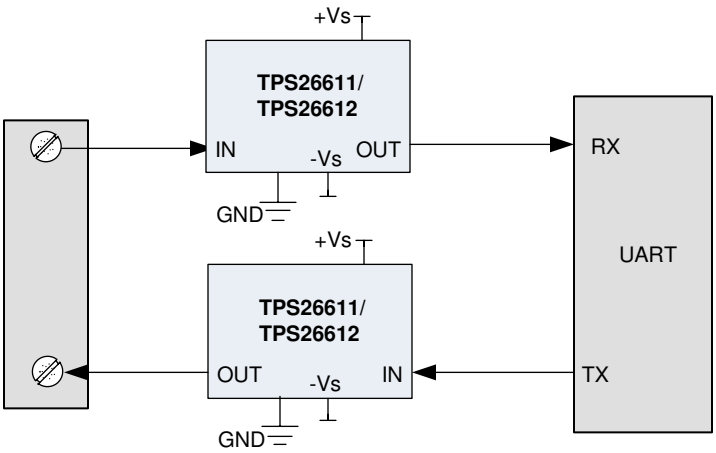


图 9-17. UART IO Protection

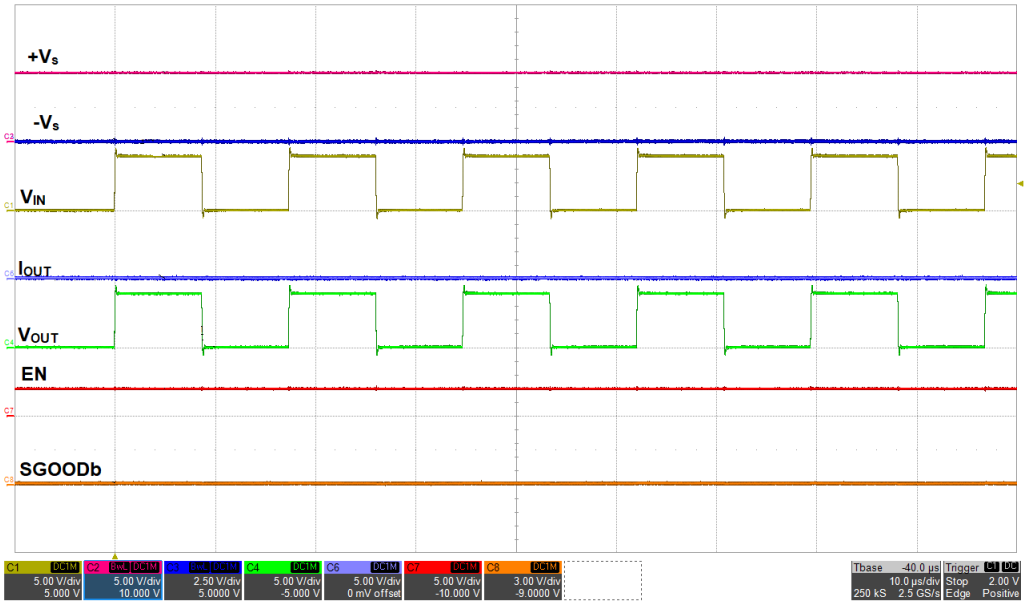


图 9-18. 115.2-Kbps UART Signal Through TPS2661x with V_S of 5 V

图 9-18 shows a UART signal of 115.2 Kbps through TPS2661x with amplitude of 4 V.

9.4.4 Higher Loop Impedance With TPS26613 and TPS26614

TPS26613 and TPS26614 devices can support higher loop impedance by providing auto-retry feature when input voltage is less than –Vs. TPS26613 and TPS26614 devices do not have UVLO protection on input and provide auto-retry for transmitter output supporting higher loop impedance. 图 9-19 provides the behavior of TPS26613 device with input voltage less than –Vs.

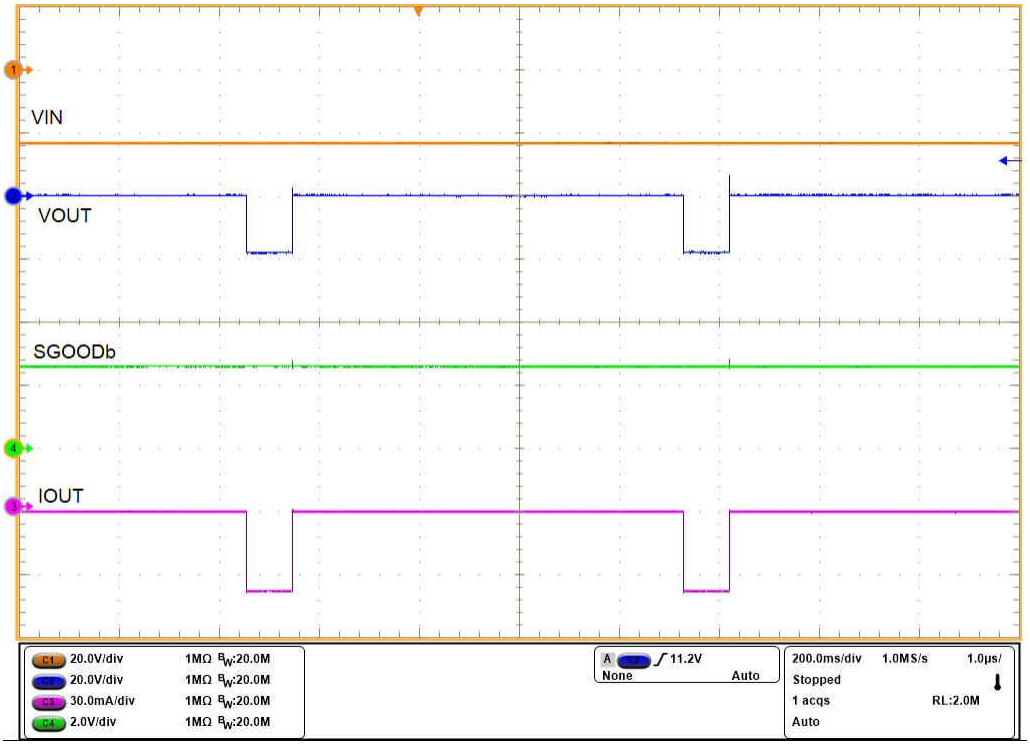


图 9-19. Auto-Retry in TPS26613 and TPS26614 for Vin < –Vs

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10 Power Supply Recommendations

表 10-1. Power Supplies for TPS2661x Devices

Device	Dual Supply (±Vs)	Single Supply (+Vs, GND)
TPS26610, TPS26611, TPS26613, TPS26614	+Vs: 2.25 V to 30 V, –Vs: –20 V to 0 V	+Vs: 3 V to 30 V, –Vs: GND
TPS26612	+Vs: 2.25 V to 30 V, –Vs: –20 V to 0 V	+Vs: 4 V to 30 V, –Vs: GND

For operation with dual supplies, TPS2661x devices need a minimum difference of 3 V between +Vs and –Vs. For reverse current blocking with single supply, see *Reverse Current Blocking for Unipolar Current Inputs (4 –20 mA, 0 –20 mA)*.

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11 Layout

11.1 Layout Guidelines

- Keep the loop current power-path as short as possible.
- Place R_{MODE} resistor close to MODE and GND pins of the device.
- For protection from IEC61000-4-5 surge transients (signal lines) on input, place the TVS close to IN pin of the device.
- Place at least 100-nF ceramic capacitors close to the device if power supplies for $\pm V_s$ are far from the device.
- Connect GND pin of the device to GND of $\pm V_s$ supplies.
- Route both terminals of R_{burden} differentially to ADC inputs (AINP, AINM).
- Keep EN and $\overline{SGOOD}$ signal lines away from loop current to avoid digital noise.

11.2 Layout Example

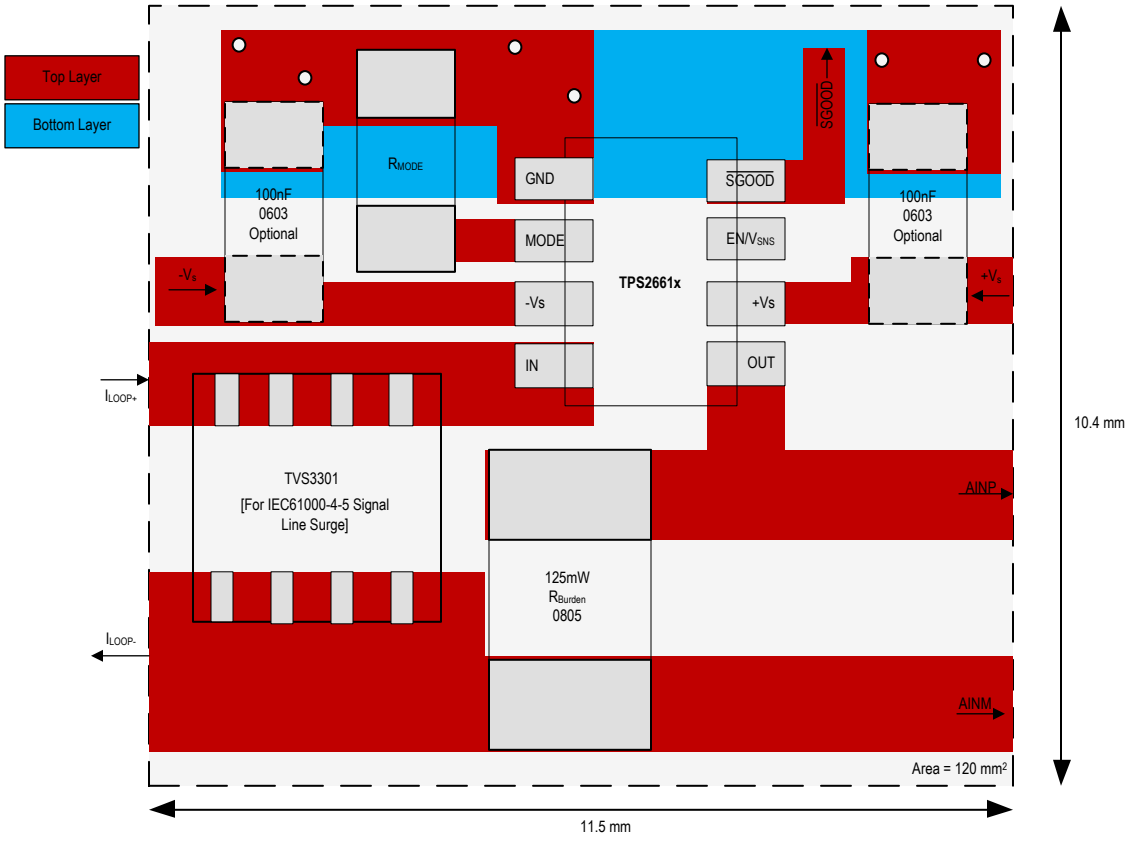


图 11-1. Layout Example

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12 Device and Documentation Support

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.3 Trademarks

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12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS26610DDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2HSF	Samples
TPS26611DDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2HTF	Samples
TPS26612DDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2HUF	Samples
TPS26613DDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2L4F	Samples
TPS26614DDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2L5F	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

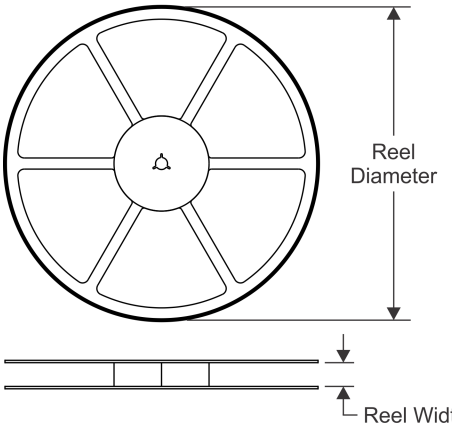
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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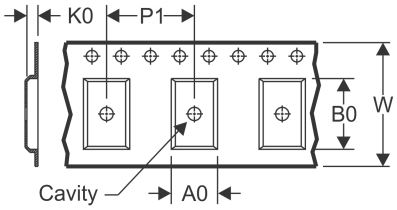
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

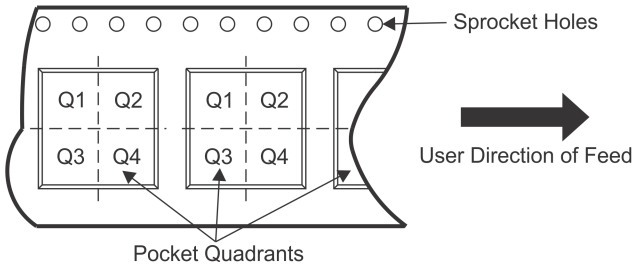


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

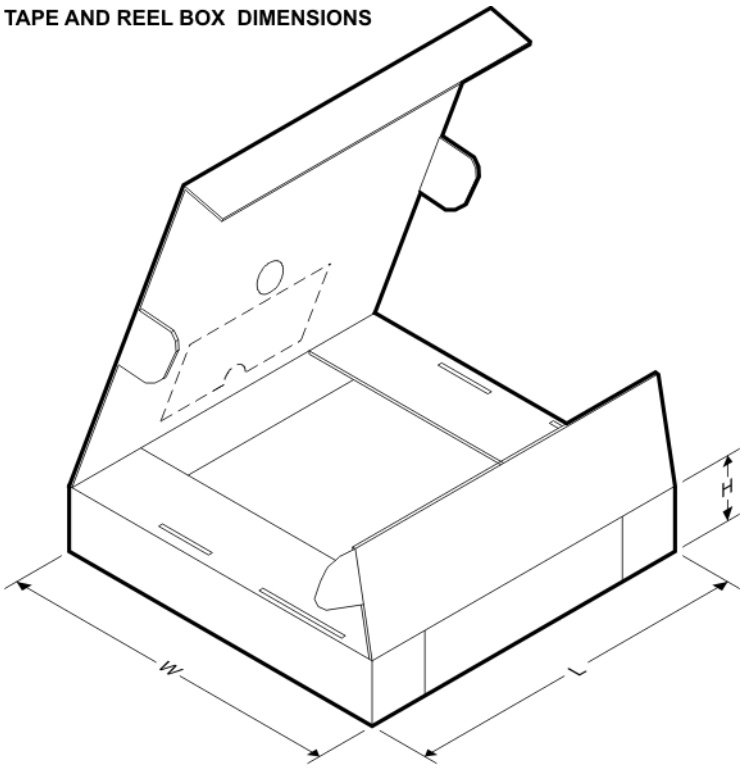
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS26610DDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS26611DDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS26612DDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS26613DDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS26614DDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

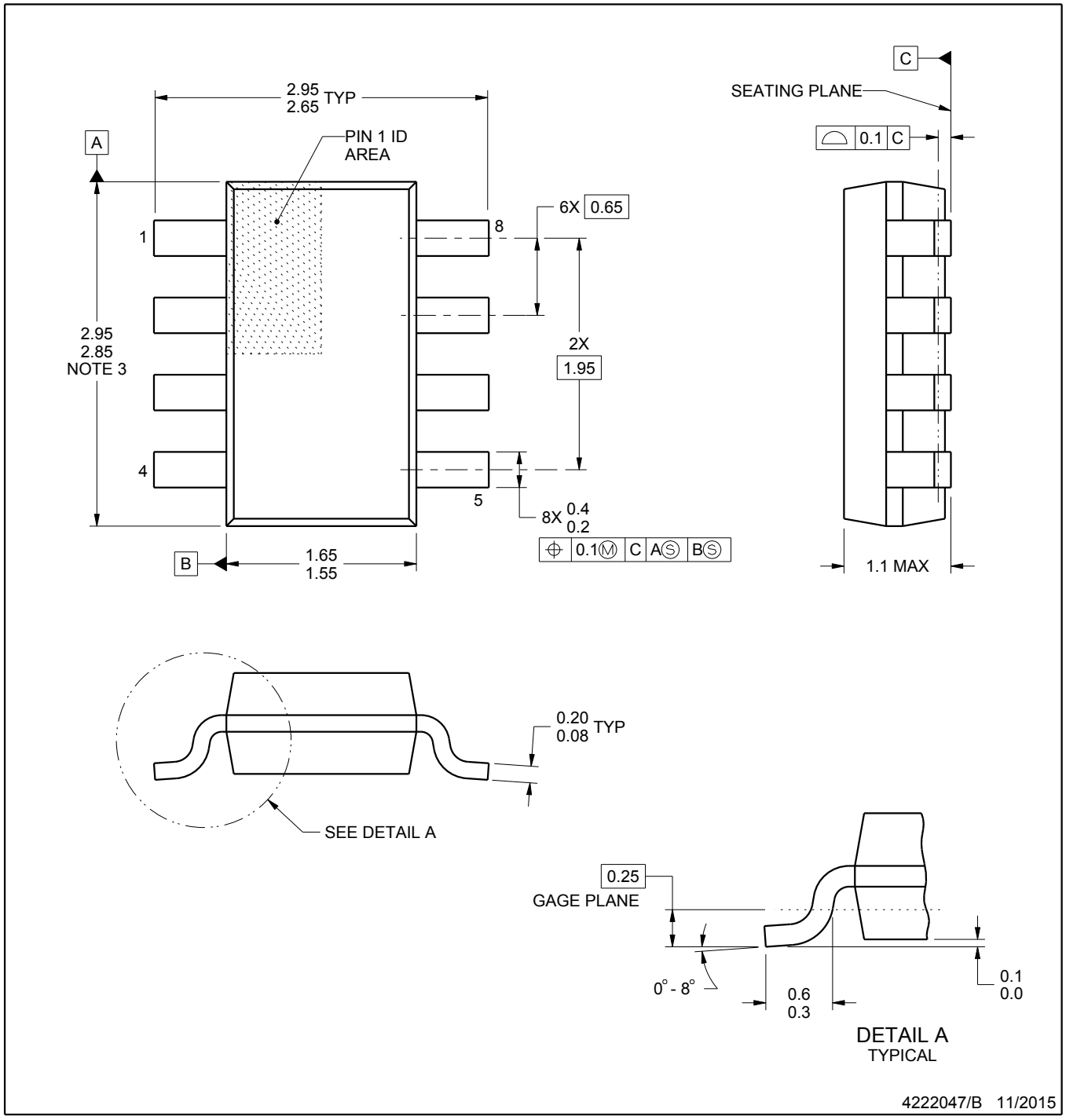
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS26610DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS26611DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS26612DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS26613DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS26614DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DDF0008A

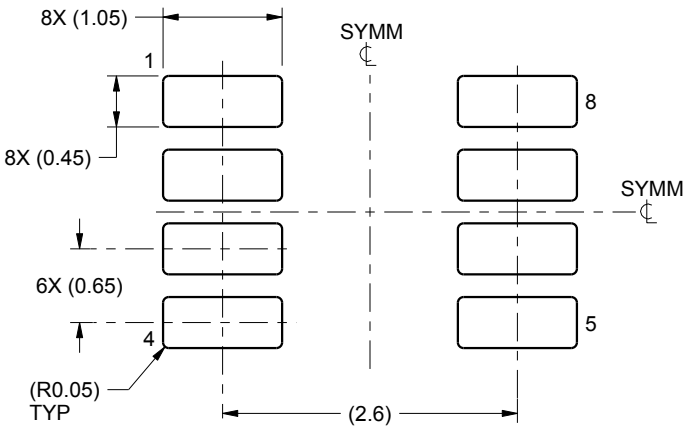
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE

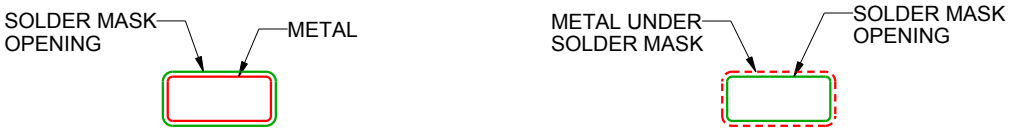


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

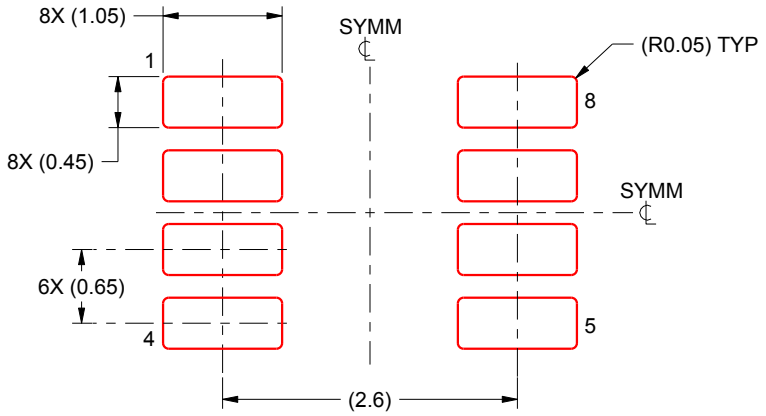
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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