TCAN104xAV-Q1 具有 1.8V I/O 支持和待机模式的汽车类双路 CAN FD 收发器

ADVANCE INFORMATION

1 特性

- AEC-Q100（等级 1）：符合汽车应用要求
- 两个具有独立模式控制功能的高速 CAN 收发器
- 符合 ISO 11898-2:2016 物理层标准要求
- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 支持传统 CAN 和经优化的 CAN FD 性能（数据速率为 2、5 和 8Mbps）
  - 具有较短的对称传播延迟时间，可增加时序裕量
- I/O 电压范围为 1.7V 至 5.5V
  - 支持 1.8V、2.5V、3.3V 和 5V 应用
- 支持 12V 和 24V 电池应用
- 接收器共模输入电压：±12V
- 保护特性：
  - 总线故障保护：±58V
  - 欠压保护
  - TXD 显性超时 (DTO)
    - 数据速率低至 9.2kbps
  - 热关断保护 (TSD)
- 工作模式：
  - 正常模式
  - 支持远程唤醒请求功能的低功耗待机模式
- 优化了未上电时的性能
  - 总线和逻辑引脚为高阻抗（运行总线或应用上无负载）
  - 支持热插拔：在总线和 RXD 输出上可实现上电和断电无干扰运行
- 结温范围：–40°C 至 150°C
- 采用 SOIC (14) 封装和无引线 VSON (14) 封装 (4.5mm x 3.0mm)，具有改进的自动光学检查 (AOI) 功能

2 应用

- 汽车和运输
  - 车身控制模块
  - 汽车网关
  - 高级驾驶辅助系统 (ADAS)
  - 信息娱乐系统

3 说明

TCAN1046V-Q1 和 TCAN1048V-Q1 (TCAN104xAV-Q1) 是双路高速控制器局域网 (CAN) 收发器，符合 ISO 11898-2:2016 高速 CAN 规范的物理层要求。

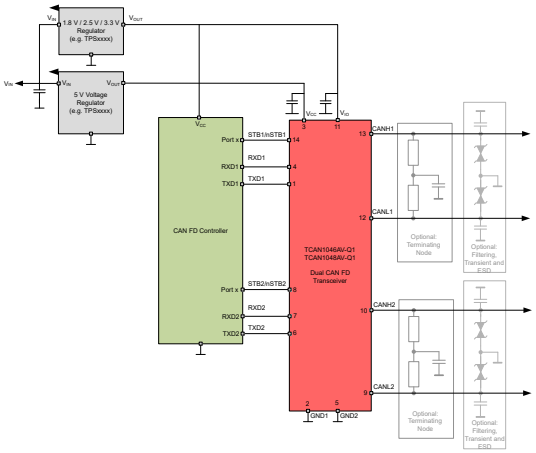
TCAN104xAV-Q1 收发器支持传统 CAN 和 CAN FD 网络（数据速率高达 8 兆位/秒 (Mbps)）。该器件包含通过 V_{IO} 端子实现的内部逻辑电平转换功能，允许将收发器 IO 直接连接到 1.8V、2.5V、3.3V 或 5V 逻辑 IO。

两个 CAN 通道通过待机引脚支持独立的模式控制。因此，可以在不影响其他 CAN 通道状态的情况下将每个收发器置于低功耗状态待机模式。在待机模式下，该器件可通过 ISO 11898-2:2016 定义的唤醒模式 (WUP) 实现远程唤醒。

器件信息

器件型号	封装	封装尺寸（标称值）
TCAN1046AV-Q1	VSON (14)	4.50mm x 3.00mm
	SOIC (14)	8.95mm x 3.91mm
	SOT-23 (14)(1)	4.20mm × 1.90mm
TCAN1048AV-Q1	VSON (14)	4.50mm x 3.00mm
	SOIC (14)	8.95mm x 3.91mm

(1) 产品预发布



简化版电路原理图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

4 说明（续）

这些收发器具有很多保护和诊断功能，包括热关断 (TSD)、TXD 显性超时 (DTO) 电源欠压检测和高达 ±58V 的总线故障保护，并定义了电源欠压或引脚悬空情况下的失效防护行为。

5 Device Comparison

表 5-1. Device Comparison Table

Part Number	Bus Fault Protection on both CAN Channels	Low Voltage I/O Logic Support	Standby (STB) Pin Mode
TCAN1046AV-Q1	±58 V	Yes	Active-high
TCAN1048AV-Q1	±58 V	Yes	Active-low

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6 Pin Configuration and Functions

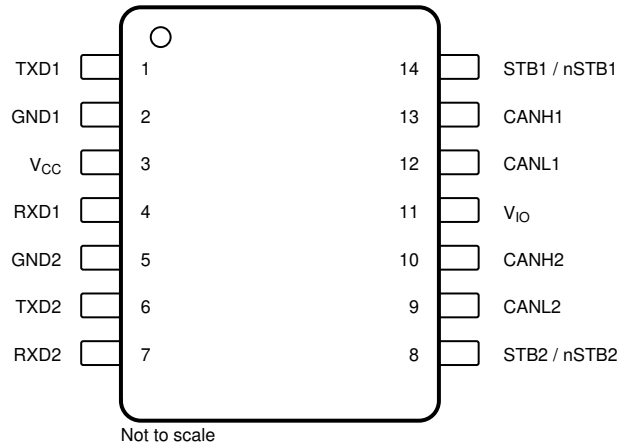


图 6-1. D Package , 14 Pin SOIC, Top View

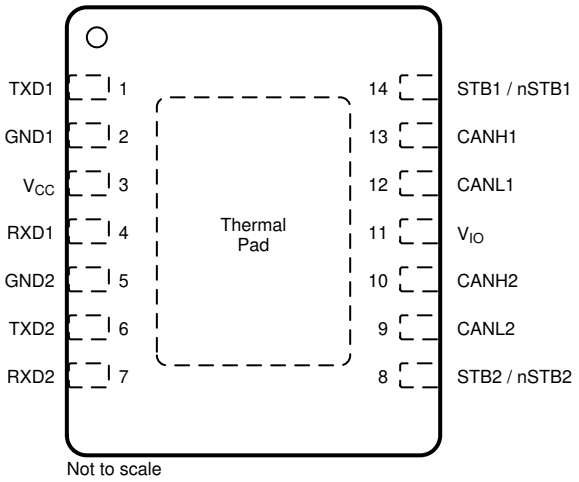


图 6-2. DMT Package, 14 Pin VSON, Top View

表 6-1. Pin Functions

Pins		Type	Description
Name	No.		
TXD1	1	Digital Input	CAN transmit data input 1, integrated pull-up
GND1	2	GND	Ground connection
V_{CC}	3	Supply	5-V supply voltage
RXD1	4	Digital Output	CAN receive data output 1, tri-state when $V_{IO} < UV_{VIO}$
GND2	5	GND	Ground connection
TXD2	6	Digital Input	CAN transmit data input 2, integrated pull-up
RXD2	7	Digital Output	CAN receive data output 2, tri-state when $V_{IO} < UV_{VIO}$
STB2	8	Digital Input	Standby input 2 for mode control, integrated pull up (TCAN1046AV – Q1)
nSTB2			Standby input 2 for mode control, inverse logic with integrated pull down (TCAN1048V – Q1)
CANL2	9	Bus IO	Low-level CAN bus 2 input/output line
CANH2	10	Bus IO	High-level CAN bus 2 input/output line
V_{IO}	11	Supply	IO supply voltage
CANL1	12	Bus IO	Low-level CAN bus 1 input/output line
CANH1	13	Bus IO	High-level CAN bus 1 input/output line
STB1	14	Digital Input	Standby input 1 for mode control, integrated pull up (TCAN1046AV – Q1)
nSTB1			Standby input 1 for mode control, inverse logic with integrated pull down (TCAN1048AV – Q1)
Thermal Pad (VSON only)		—	Electrically connected to GND, connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief

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7 Device and Documentation Support

7.1 Device Support

This device conforms to the following CAN standards. The core of what is needed is covered within this system specification; however, reference should be made to these standards and any discrepancies pointed out and discussed. This document should provide all the basics of what is needed. However, for a full understanding of CAN including the protocol these additional sources are helpful as the scope of CAN protocol in detail is outside the scope of this physical layer (transceiver) specification.

7.1.1 Device Nomenclature

CAN Transceiver Physical Layer Standards:

- ISO 11898-2:2016 High speed medium access unit (original High Speed CAN transceiver standard)
- ISO 11898-5 High speed medium access unit with low power mode (super sets -2 standard electrically in several specs and adds the original wake up capability via the bus in low power mode).
- ISO 11898-6 High speed medium access unit with selective wake.
- ISO 8802-3: CSMA/CD – referenced for collision detection from ISO11898-2
- CAN FD 1.0 Spec and Papers
- Bosch “Configuration of CAN Bit Timing”, Paper from 6th International CAN Conference (ICC), 1999. This is repeated a lot in the DCAN IP CAN Controller spec copied into this system spec.
- GMW3122: GM requirements for HS CAN
- SAE J2284-2: High Speed CAN (HSC) for Vehicle Applications at 250 kbps
- SAE J2284-3: High Speed CAN (HSC) for Vehicle Applications at 500 kbps

EMC requirements:

- HW Requirements for CAN, LIN, FR V1.3: German OEM requirements for HS CAN

Conformance Test requirements:

- HS_TRX_Test_Spec_V_1_0: GIFT / ICT CAN test requirements for High Speed Physical Layer

7.2 Documentation Support

7.2.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

表 7-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TCAN1046AV-Q1	Click here	Click here	Click here	Click here	Click here
TCAN1048AV-Q1	Click here	Click here	Click here	Click here	Click here

7.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

7.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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7.5 Trademarks

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7.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

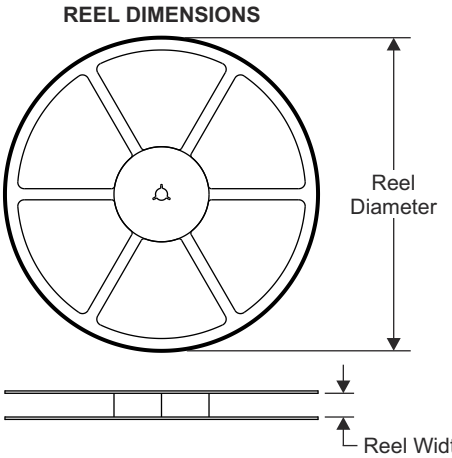
7.7 术语表

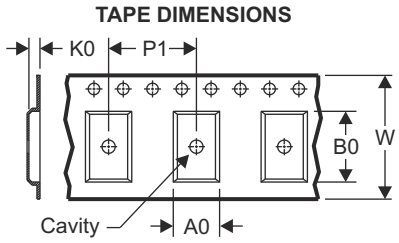
TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

8 Mechanical, Packaging, and Orderable Information

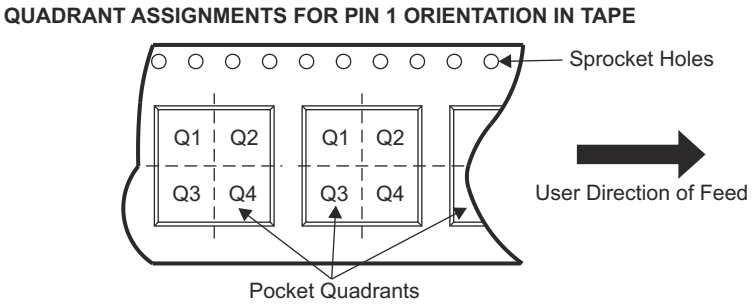
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

8.1 Tape and Reel Information





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



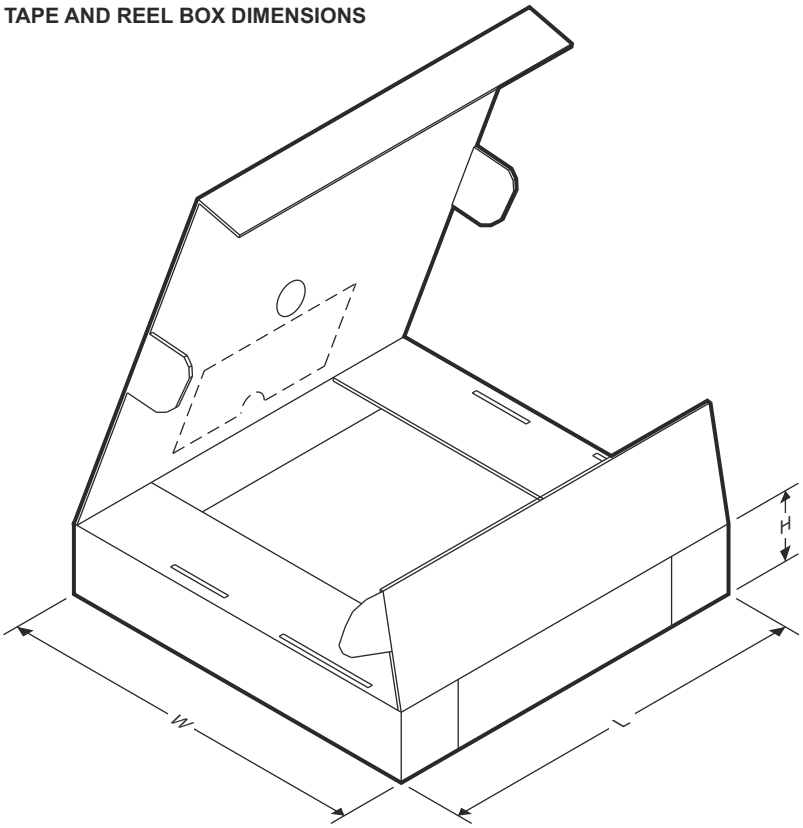
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1046AVDMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.2	4.7	1.15	8.0	12.0	Q1
TCAN1048AVDMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.2	4.7	1.15	8.0	12.0	Q1
TCAN1046AVDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TCAN1048AVDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

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ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1046AVDMTRQ1	VSON	DMT	14	3000	370.0	355.0	55.0
TCAN1048AVDMTRQ1	VSON	DMT	14	3000	370.0	355.0	55.0
TCAN1046AVDRQ1	SOIC	D	14	2500	853.0	449.0	35.0
TCAN1048AVDRQ1	SOIC	D	14	2500	853.0	449.0	35.0

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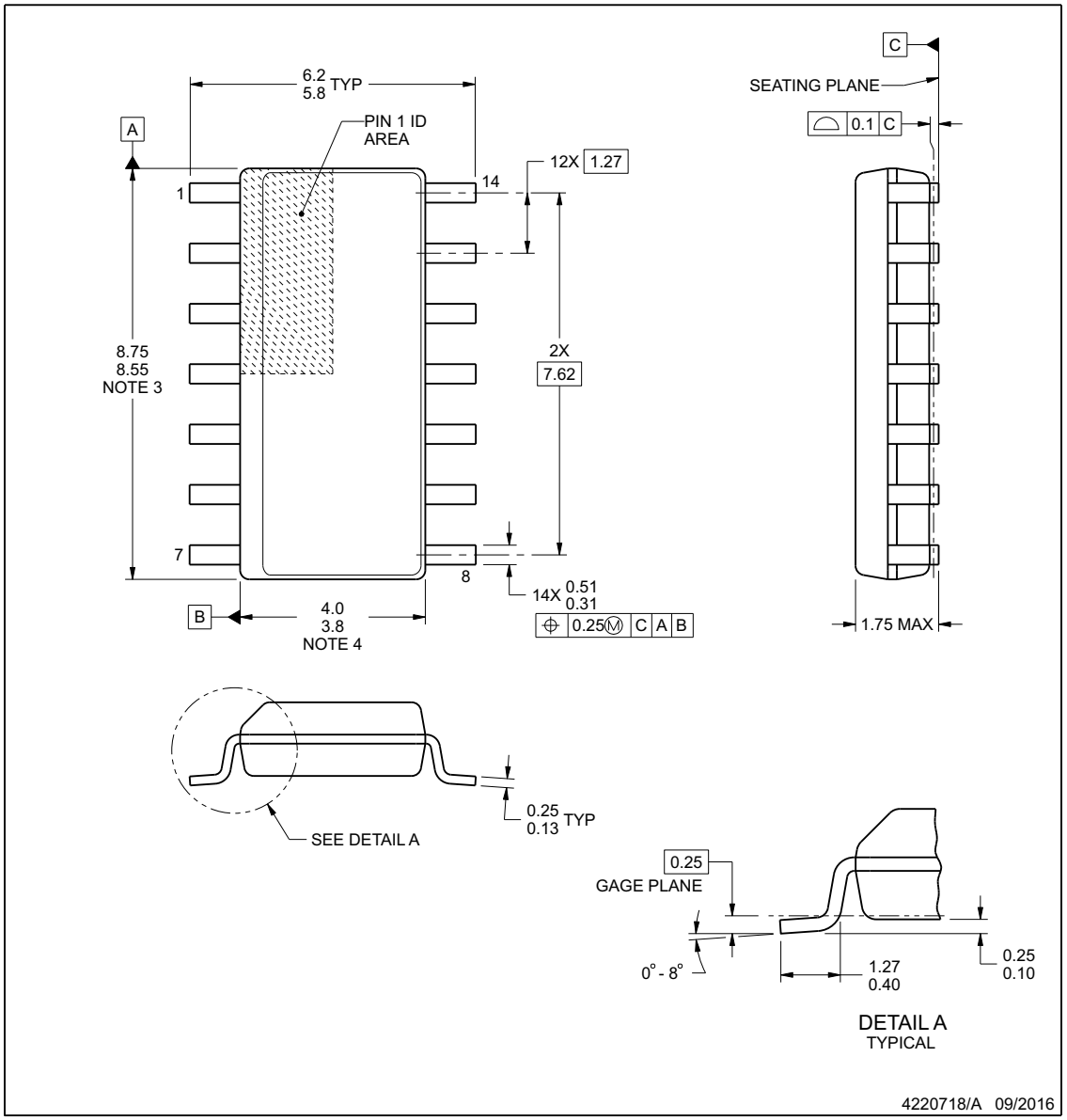


PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

ADVANCE INFORMATION

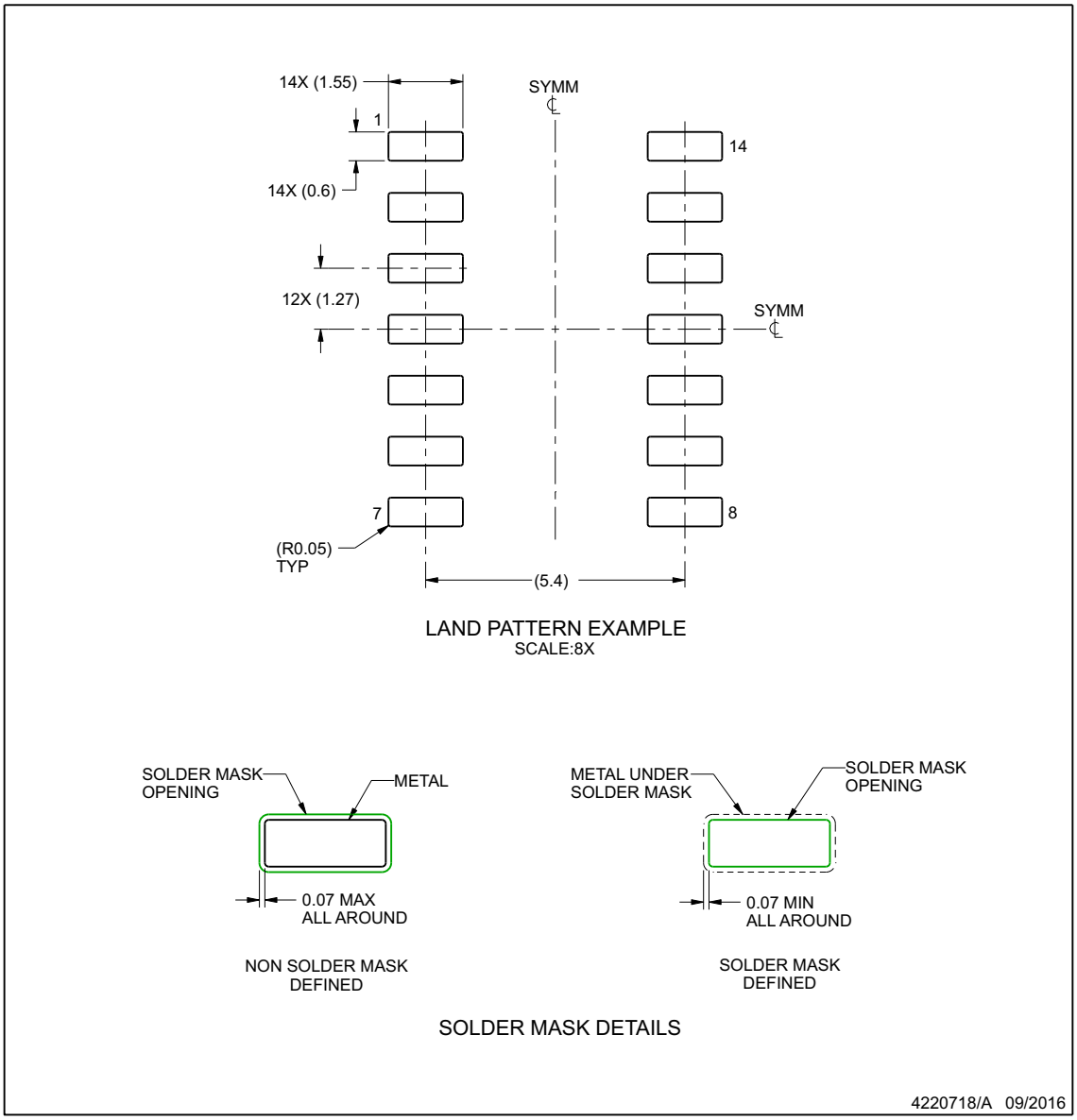
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ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

D0014A — SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

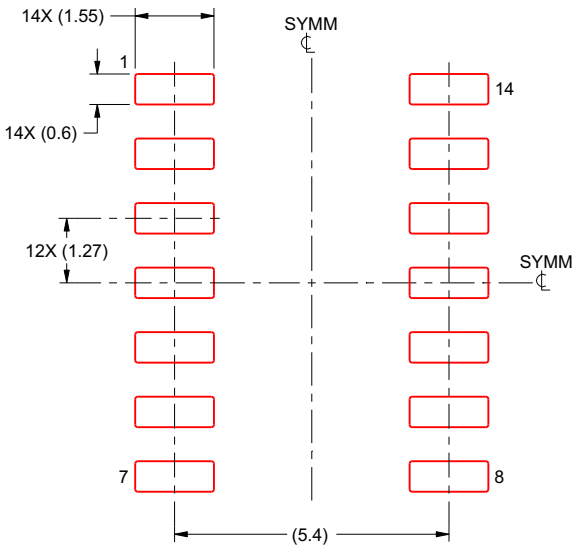
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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EXAMPLE STENCIL DESIGN

D0014A — **SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

ADVANCE INFORMATION

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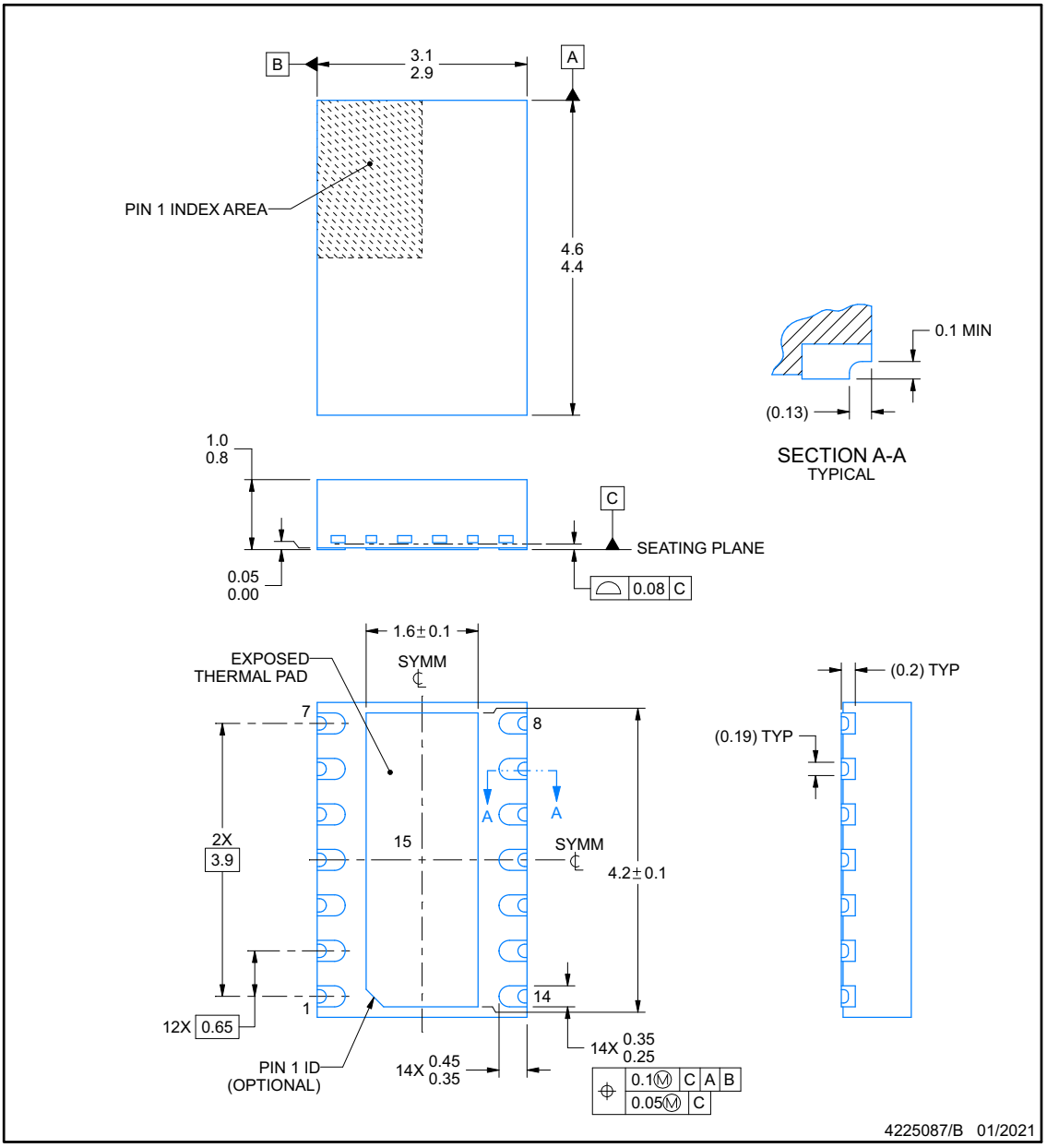
ADVANCE INFORMATION

PACKAGE OUTLINE

DMT0014B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

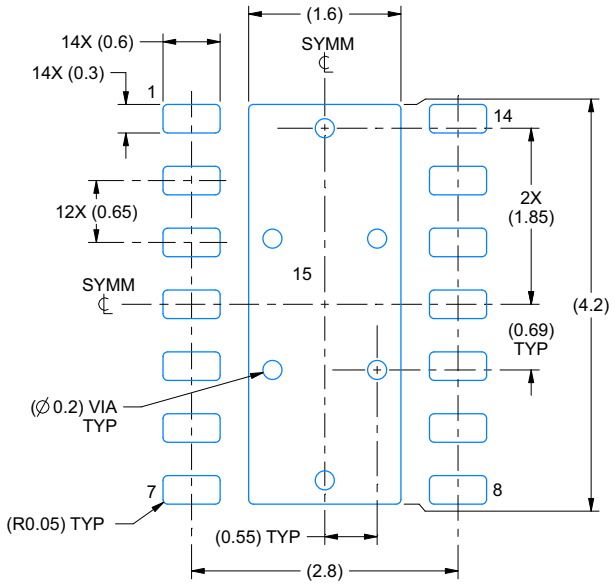
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EXAMPLE BOARD LAYOUT

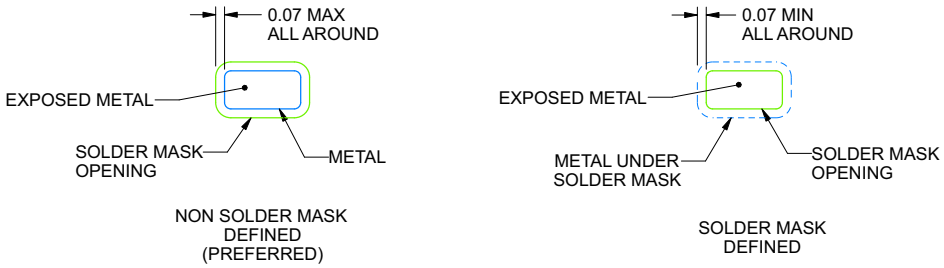
DMT0014B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4225087/B 01/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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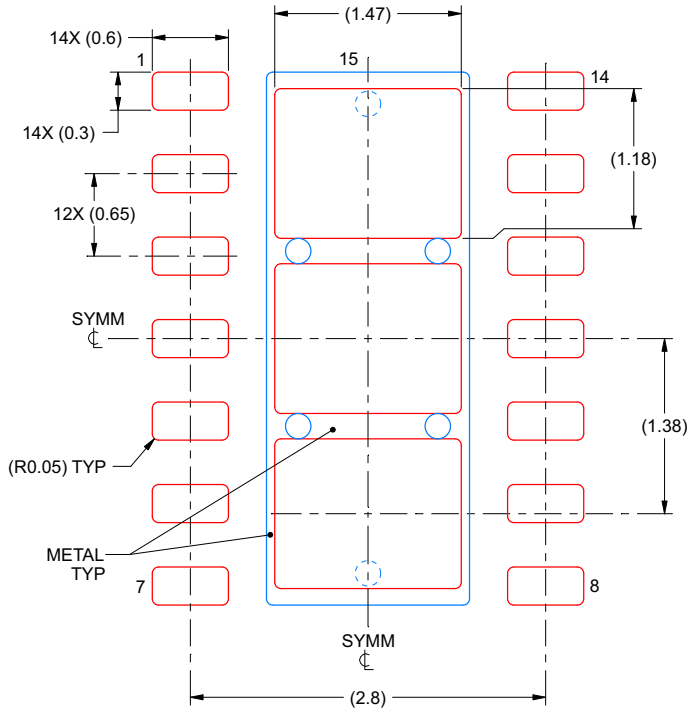
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DMT0014B — **VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4225087/B 01/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTCAN1046AVDRQ1	ACTIVE	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 150		Samples
PTCAN1048AVDRQ1	ACTIVE	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 150		Samples
TCAN1046AVDMTRQ1	ACTIVE	VSON	DMT	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	46AV	Samples
TCAN1046AVDYYRQ1	ACTIVE	SOT-23-THIN	DYY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1046AV	Samples
TCAN1048AVDMTRQ1	ACTIVE	VSON	DMT	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	48AV	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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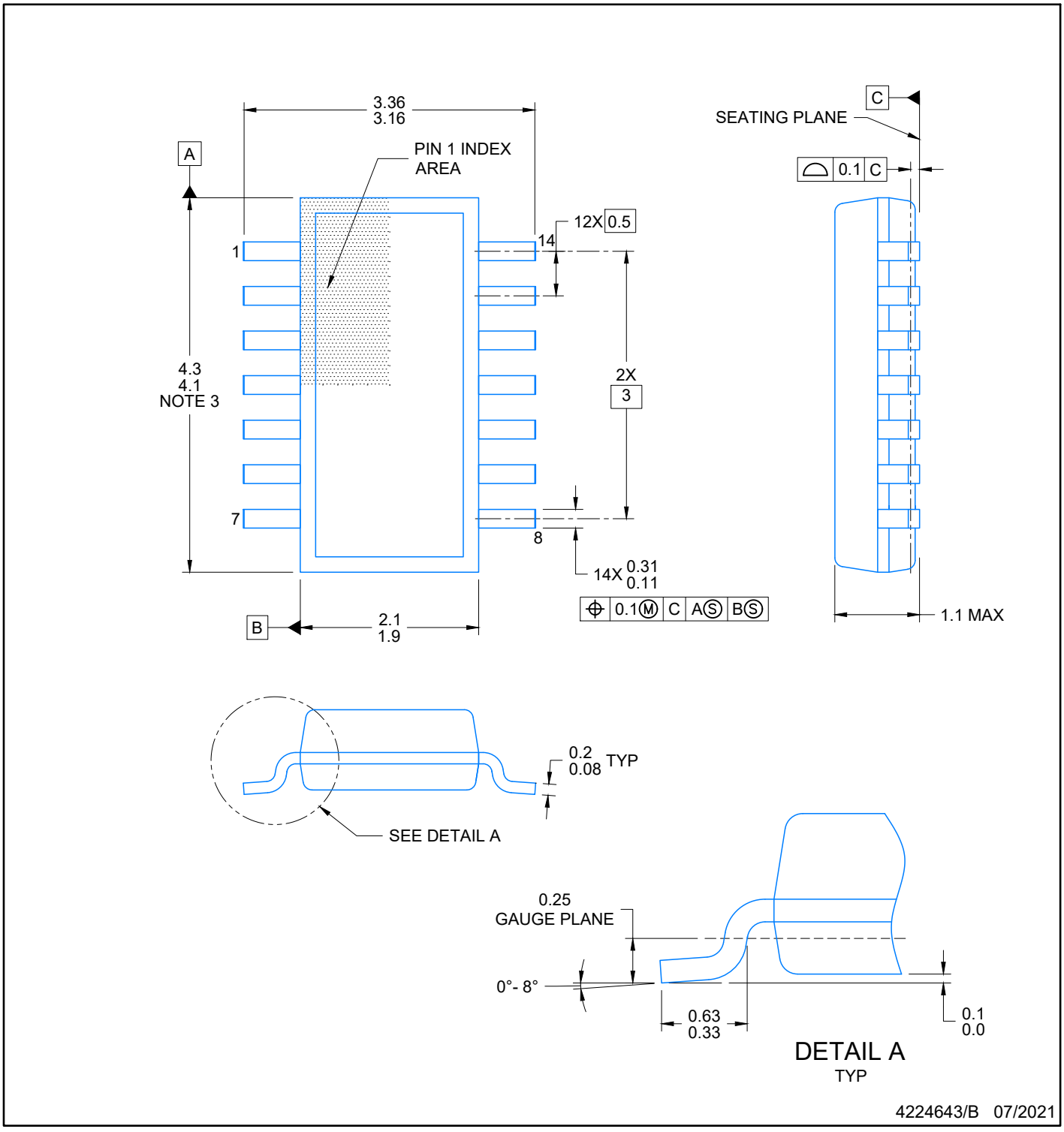
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

DYY0014A

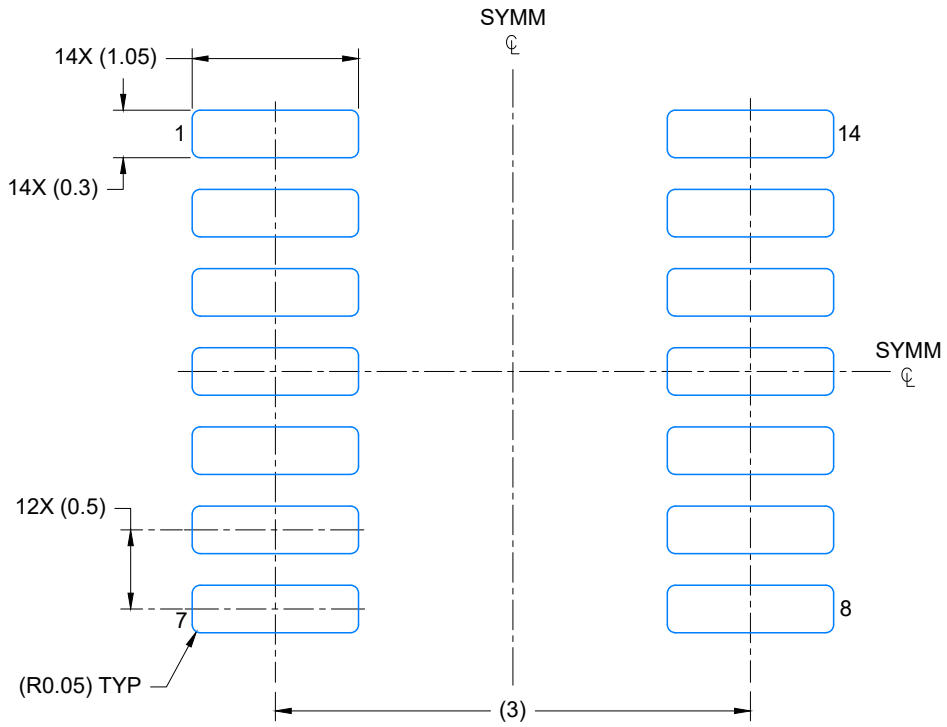
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

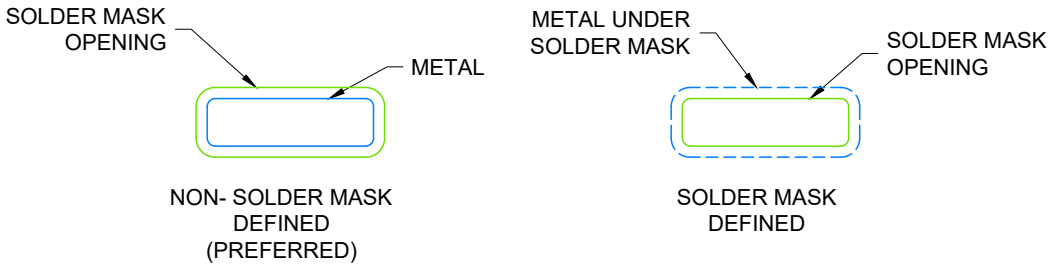


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

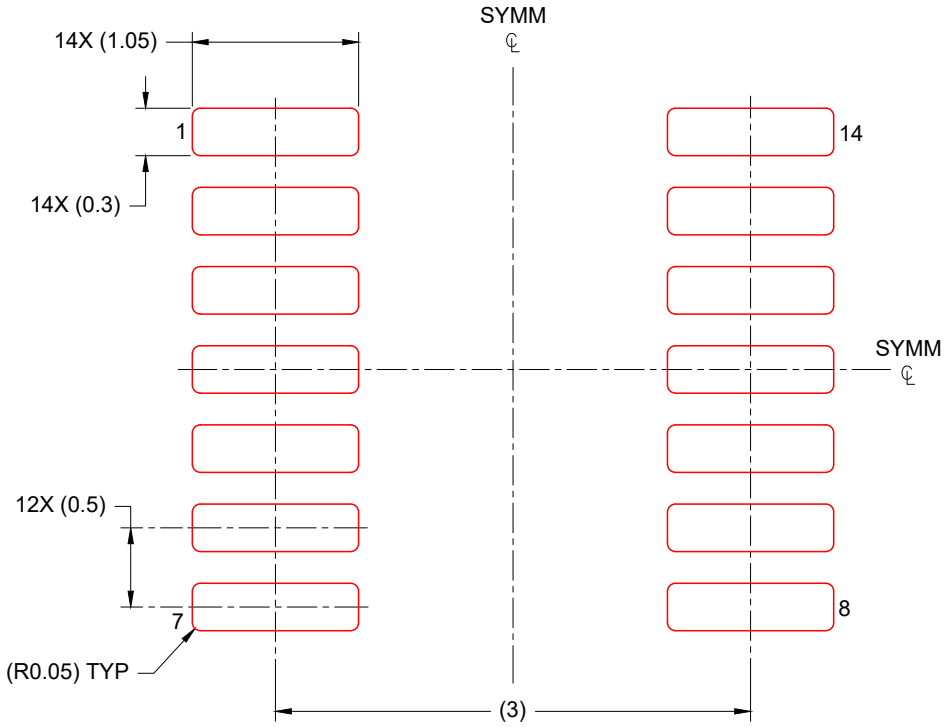


SOLDER MASK DETAILS

4224643/B 07/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/B 07/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

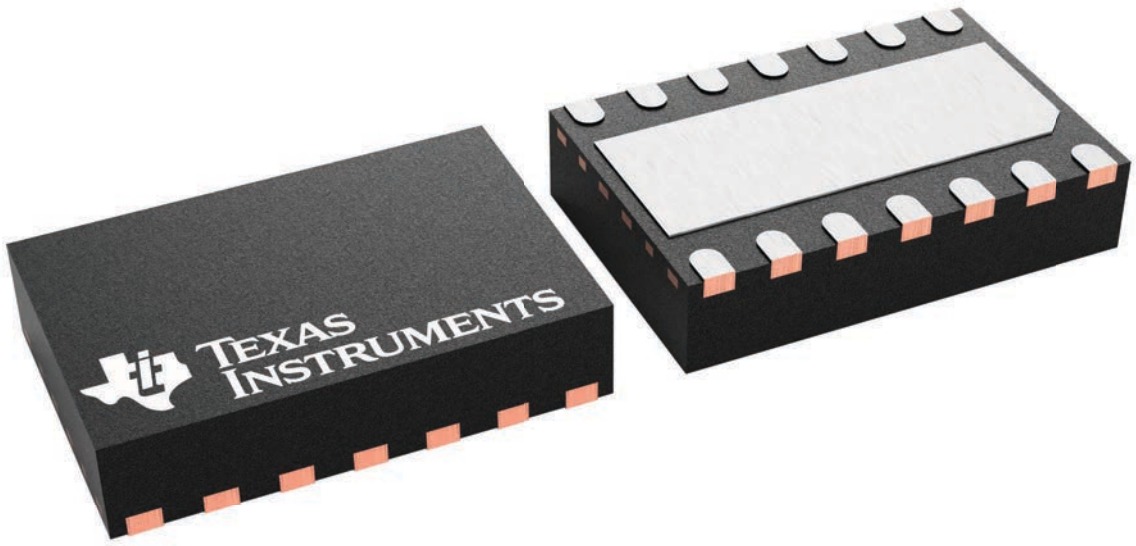
DMT 14

VSON - 0.9 mm max height

3 x 4.5, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



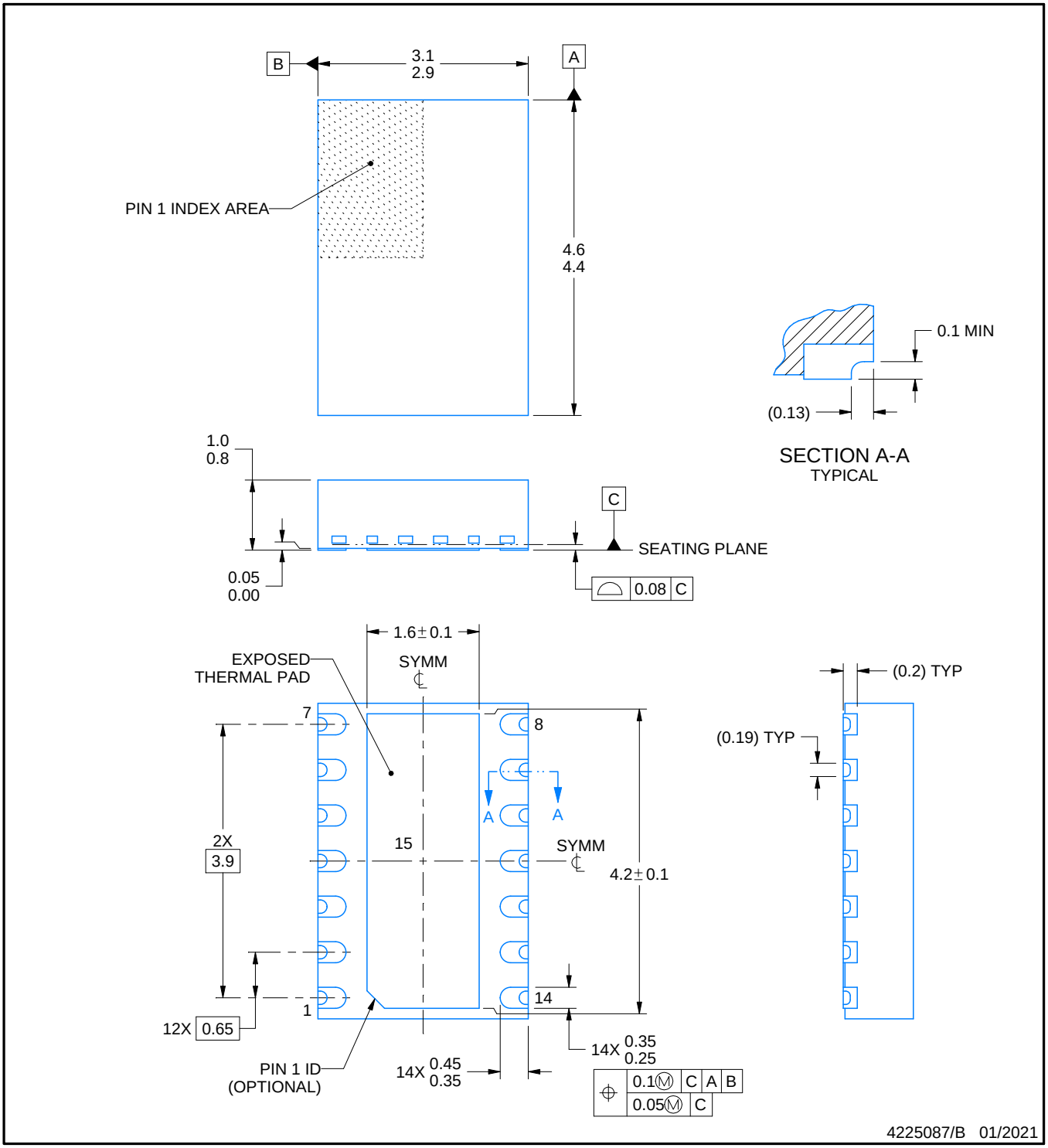
4225088/A

DMT0014B

PACKAGE OUTLINE

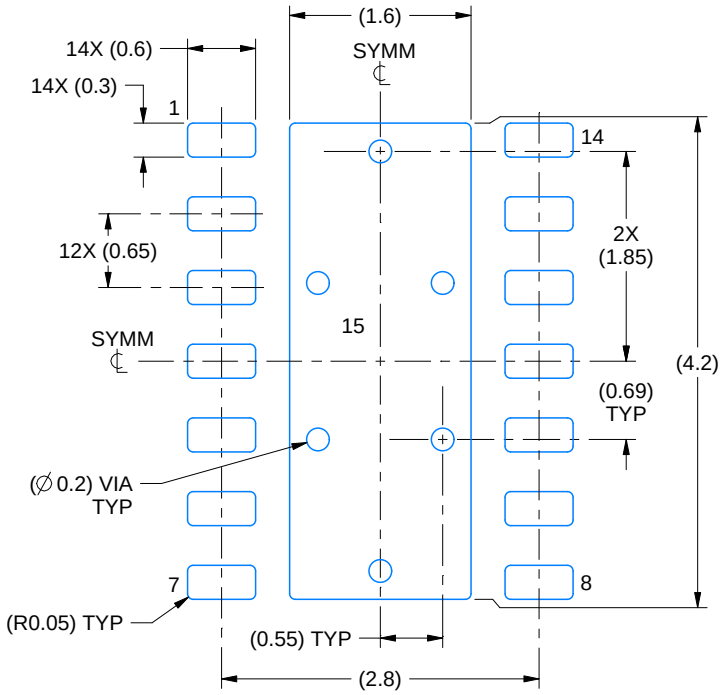
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

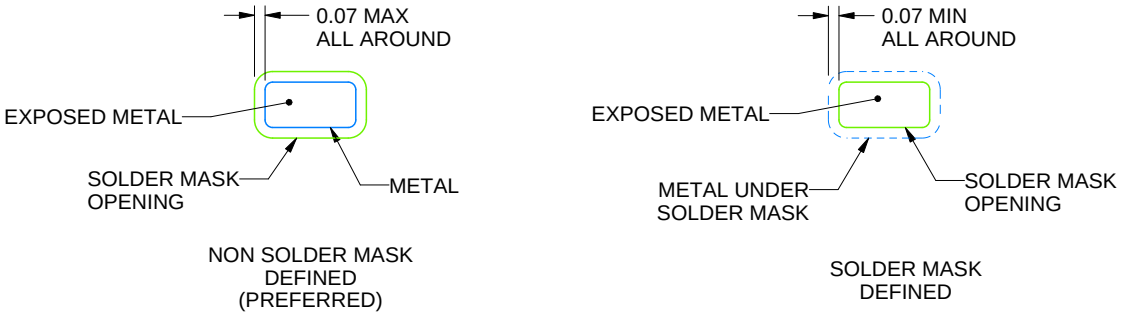


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

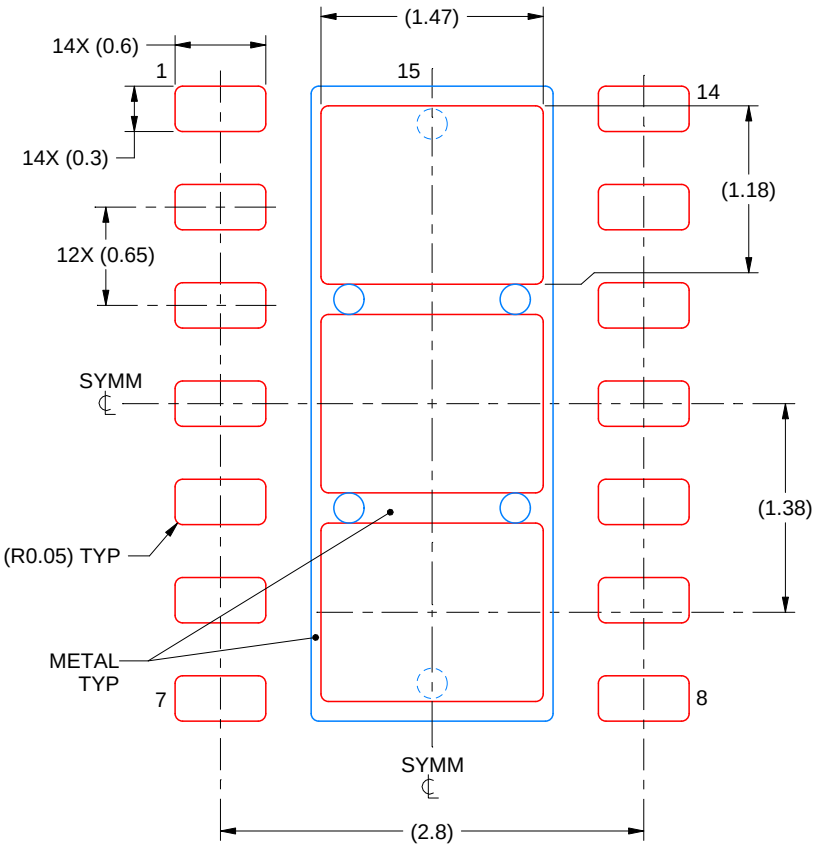


SOLDER MASK DETAILS

4225087/B 01/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

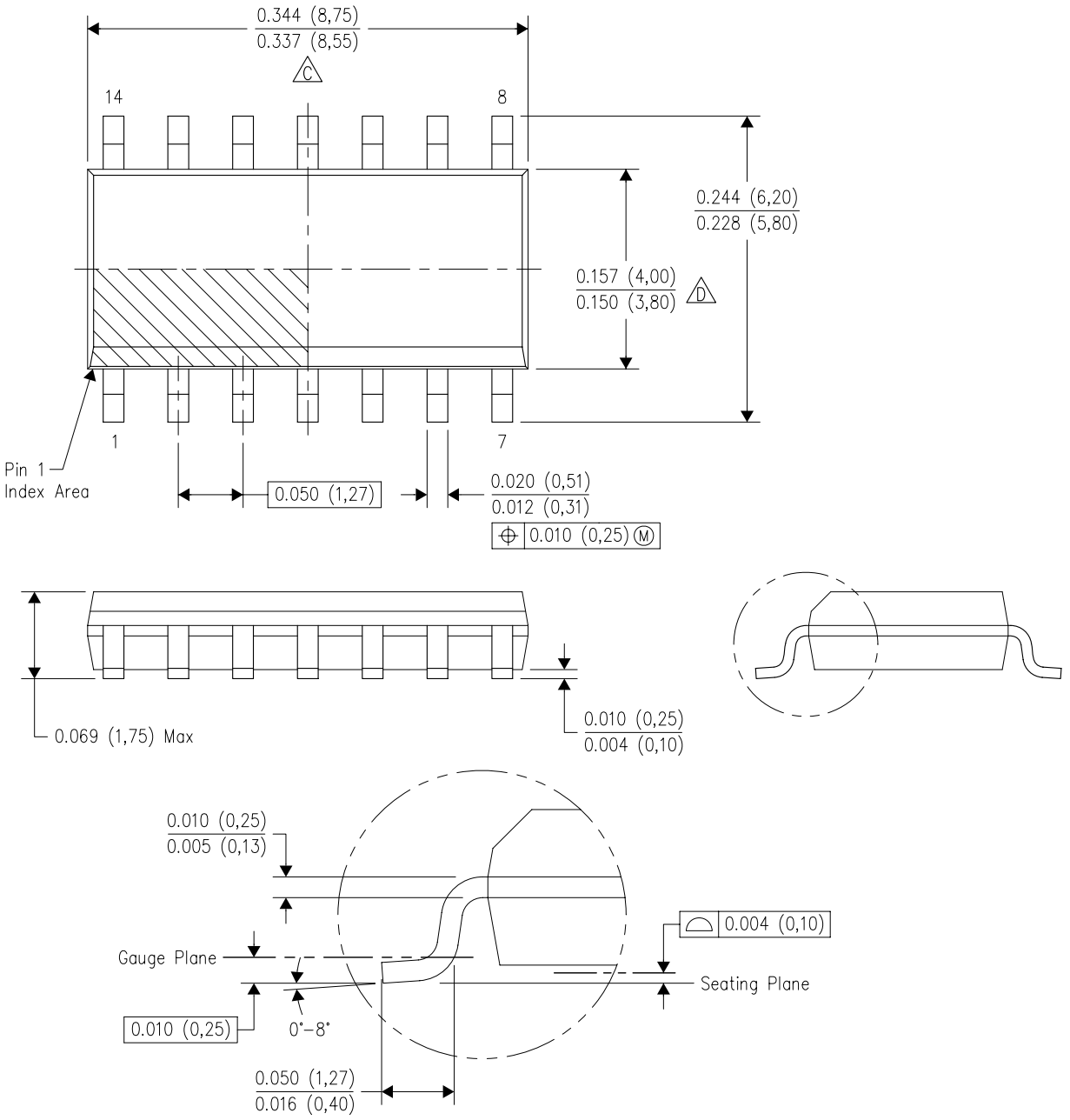
EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4225087/B 01/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

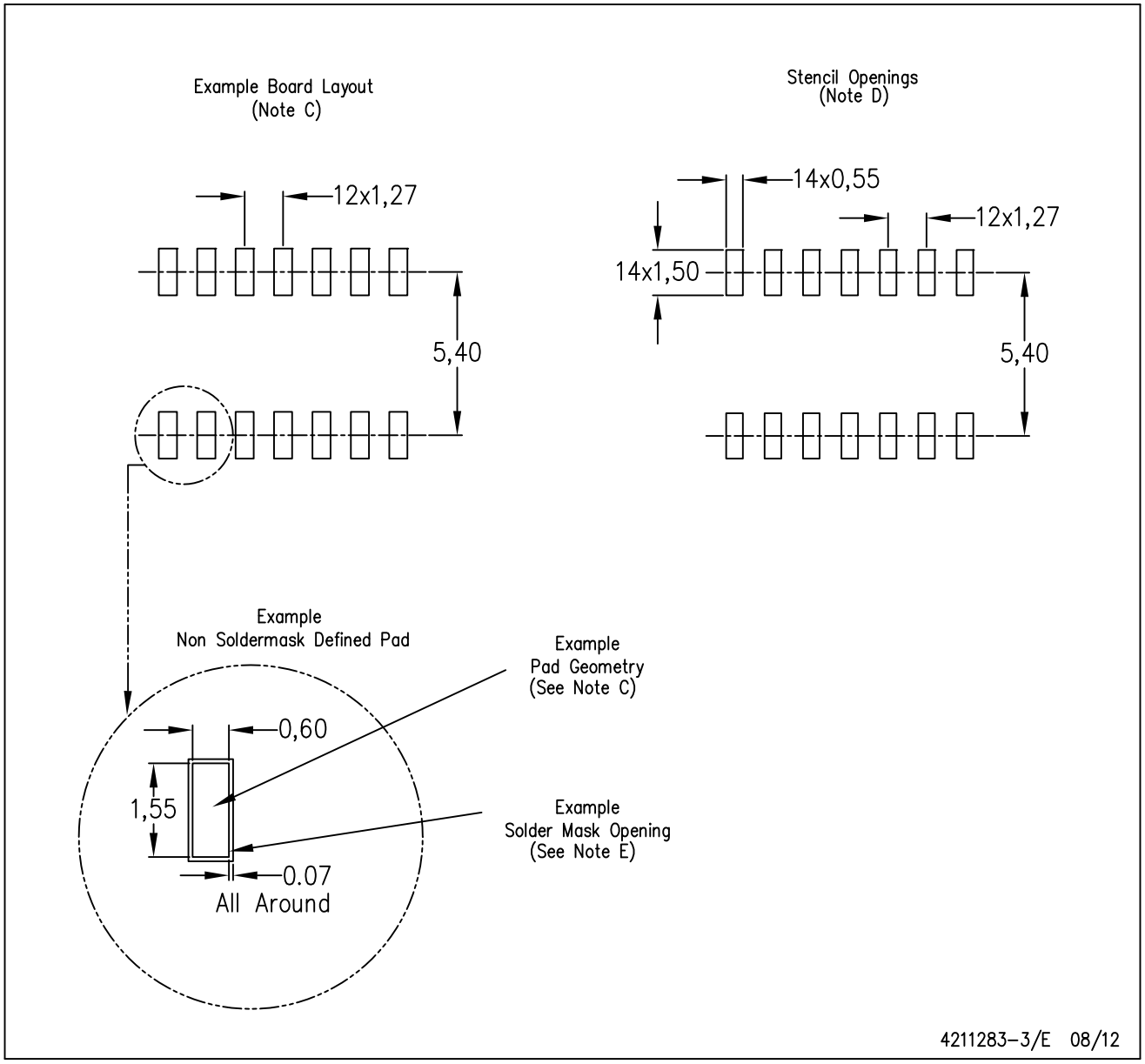
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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