



TPD6F002-Q1 面向 LCD 显示屏和 FPD-Link 的汽车类 ESD 保护和 EMI 滤波器

1 特性

- 符合 AEC-Q101 标准
- 针对数据端口的 6 通道电磁干扰 (EMI) 滤波
 - 100MHz 频率下的串扰衰减为 -47dB
 - 800MHz 频率下的插入损耗为 -30dB
 - 100MHz 频率下的带宽为 -3dB
- Pi 型 (C-R-C) 滤波器配置
($R = 100\Omega$, $C_{TOTAL} = 34pF$)
- 优异的静电放电 (ESD) 保护, 超过了 IEC 61000-4-2 标准 (4 级)
 - $\pm 20kV$ IEC 61000-4-2 接触放电
 - $\pm 30kV$ IEC 61000-4-2 气隙放电
- 低泄漏电流 20nA (最大值)
- 采用节省空间的小外形尺寸无引线 (SON) 封装 (3mm × 1.35mm)

2 应用

- 液晶显示屏 (LCD) 显示接口
- 通用输入/输出 (GPIO)
- 存储器接口
- 采用柔性电缆的数据线
- FPD-Link

3 说明

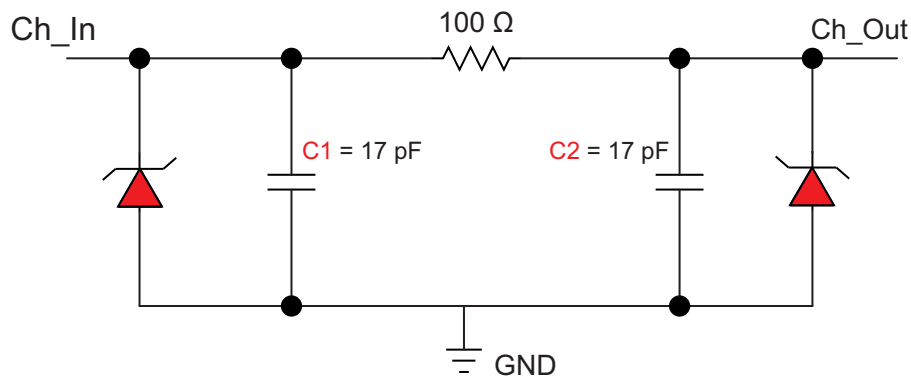
TPD6F002-Q1 是一款高度集成的器件, 该器件提供有 6 通道 EMI 滤波器和基于瞬态电压抑制器 (TVS) 的 ESD 保护二极管阵列。低通滤波器阵列可为数据端口抑制 EMI/射频干扰 (RFI) 辐射, 防止其受到电磁干扰。TVS 二极管阵列的额定 ESD 冲击消散值高于 IEC 61000-4-2 国际标准中规定的最高水平。此器件高度集成, 并且采用易于布线的小型 DSV 封装, 可对 LCD 显示屏、存储器接口、GPIO 线和 FPD-Link 提供强力的电路保护。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
TPD6F002-Q1	SON (12)	3.00mm x 1.35mm

(1) 要了解所有可用封装, 请见数据表末尾的可订购产品附录。

4 简化电路原理图



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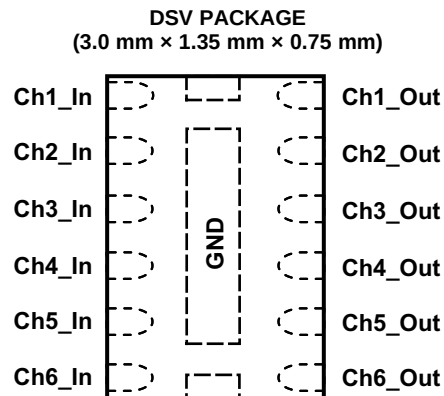
5 修订历史记录

Changes from Original (December 2014) to Revision A

Page

• 最初发布的完整版数据表。	1
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6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ChX_In	1, 2, 3, 4, 5, 6	IO	ESD-protected channel, connected to corresponding ChX_Out
ChX_Out	7, 8, 9, 10, 11, 12	IO	ESD-protected channel, connected to corresponding ChX_In
GND	G	G	Ground

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V _{IO} IO to GND		5.75	V
T _J Junction temperature		125	°C
T _{stg} Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002, all pins ⁽¹⁾	±10
		Charged device model (CDM), per AEC Q101-005, all pins	±1.5
		IEC 61000-4-2 Contact Discharge	±20
		IEC 61000-4-2 Air-Gap Discharge	±30

- (1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V _{IO} Input pin voltage	0		5.5	V
T _A Operating free-air temperature	–40		125	°C

TPD6F002-Q1

ZHCSDL8A–DECEMBER 2014–REVISED FEBRUARY 2015

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7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPD6F002-Q1	UNIT
		DSV	
		12 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	120.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	104.4	
R _{θJB}	Junction-to-board thermal resistance	78.5	
ψ _{JT}	Junction-to-top characterization parameter	13.0	
ψ _{JB}	Junction-to-board characterization parameter	77.7	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	66.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

T_A = –40°C to 125°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{BR}	DC breakdown voltage	I _{IO} = 10 μA	6			V
R	Resistance	V _{IN} = 3.3 V, I _{IN-to-out} = 1mA	85	100	115	Ω
C	Capacitance (C1 or C2)	V _{IO} = 2.5 V		17		pF
I _{IO}	Channel leakage current	V _{IO} = 3.3 V		1	20	nA
f _C	Cut-off frequency	Z _{SOURCE} = 50 Ω, Z _{LOAD} = 50 Ω		100		MHz

(1) Typical values are at T_A = 25°C.

7.6 Typical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

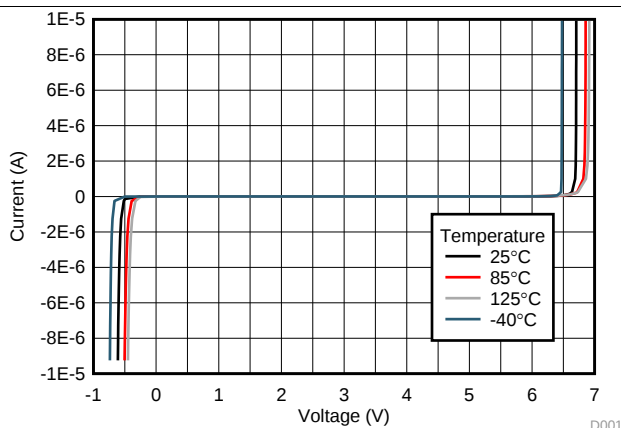


Figure 1. DC Voltage-Current Sweep across Input, Output Pins

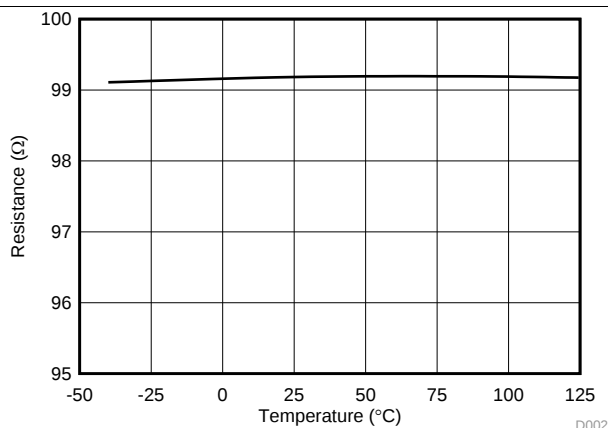


Figure 2. Series Resistance vs Temperature

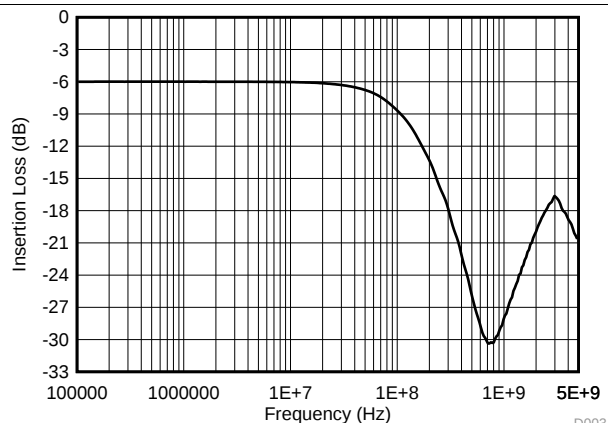


Figure 3. Typical Insertion-loss Characteristics (DC Bias = 0 V, 50 Ω Environment)

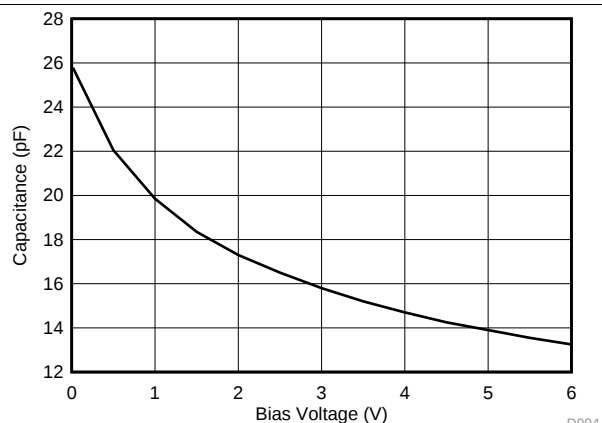


Figure 4. Capacitance (C1 or C2) vs. Bias Voltage

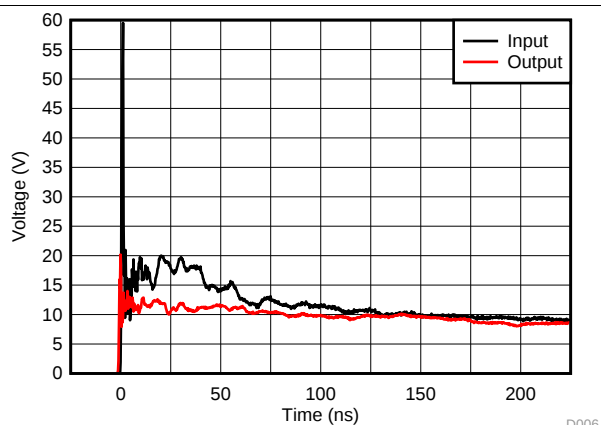


Figure 5. +8-kV IEC Waveform

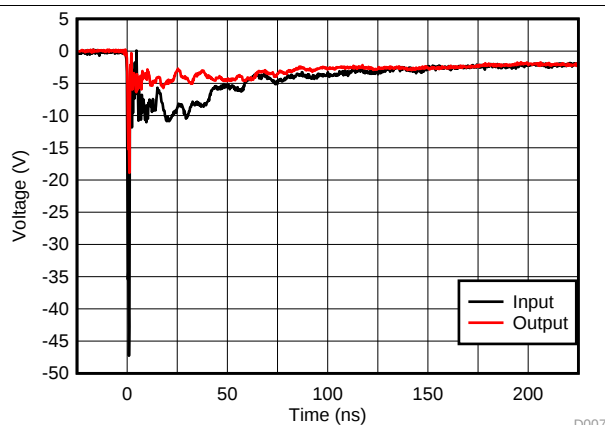


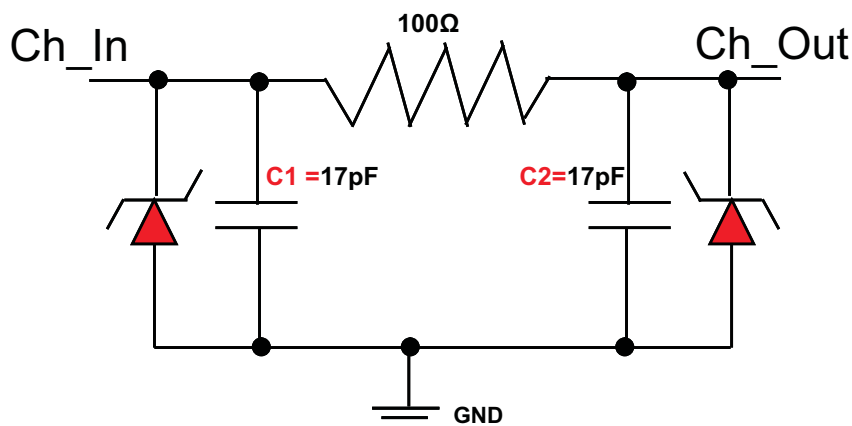
Figure 6. -8-kV IEC Waveform

8 Detailed Description

8.1 Overview

The TPD6F002-Q1 is a highly integrated device that provides a six channel EMI filter and a TVS based ESD protection diode array. The low-pass filter array suppresses EMI/RFI emissions for data ports subject to electromagnetic interference. The TPD6F002-Q1 is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard. The high level of integration, combined with its small easy-to-route DSV package, makes this device ideal for protecting interfaces like LCD displays, memory interfaces, and FPD-Link.

8.2 Functional Block Diagram



8.3 Feature Description

The TPD6F002-Q1 is a highly integrated device that provides a six channel EMI filter and a TVS based ESD protection diode array. The low-pass filter array suppresses EMI/RFI emissions for data ports subject to electromagnetic interference. The TVS diode array is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard. The high level of integration, combined with its small easy-to-route DSV package, allows this device to provide great circuit protection for LCD displays, memory interfaces, GPIO lines, and FPD-Link.

8.3.1 AEC-Q101 Qualified

This device is qualified to AEC-Q101 standards. It passes HBM H3B (± 8 kV) and CDM C5 (± 1 kV) ESD ratings and is qualified to operate from -40°C to 125°C .

8.3.2 Six-Channel EMI Filtering

This device provides six channels for EMI filtering of data lines with the following parameters:

- -47 dB Crosstalk Attenuation at 100 MHz
- -30 dB Insertion Loss at 800 MHz
- -3 dB Bandwidth: 100 MHz

8.3.3 Pi-Style Filter Configuration

This device has a pi-style filtering configuration composed of a series resistor and two capacitors in parallel with the I/O pins. The typical resistor value is $100\ \Omega$ and the typical capacitor values are 17 pF each.

8.3.4 Robust ESD Protection

The ESD protection on all pins exceeds the IEC 61000-4-2 level 4 standard. Contact ESD is rated at ± 20 kV and Air-gap ESD is rated at ± 30 kV.

Feature Description (continued)

8.3.5 Low Leakage Current

The I/O pins feature an ultra-low leakage current of 20-nA (max) with a bias of 3.3 V

8.3.6 Space-Saving SON Package

The layout of this device makes it easy to add protection to existing layouts. The packages offer flow-through routing which requires minimal changes to existing layout for addition of these devices. Additionally, the device offers a small space-saving package that takes a minimal footprint on the board.

8.4 Device Functional Modes

The TPD6F002-Q1 is a passive integrated circuit that passively filters EMI and triggers when voltages are above V_{BR} or below the lower diode voltage (-0.6 V). During ESD events, voltages as high as ± 30 kV (air) can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels, the device reverts to passive.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPD6F002-Q1 is a highly integrated device that provides a six channel EMI filter and a TVS based ESD protection diode array. The low-pass filter array suppresses EMI/RFI emissions for data ports subject to electromagnetic interference. The TVS diode array is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard. The high level of integration, combined with its small easy-to-route DSV package, allows this device to provide great circuit protection for LCD displays, memory interfaces, GPIO lines, and FPD-Link.

9.2 Typical Application

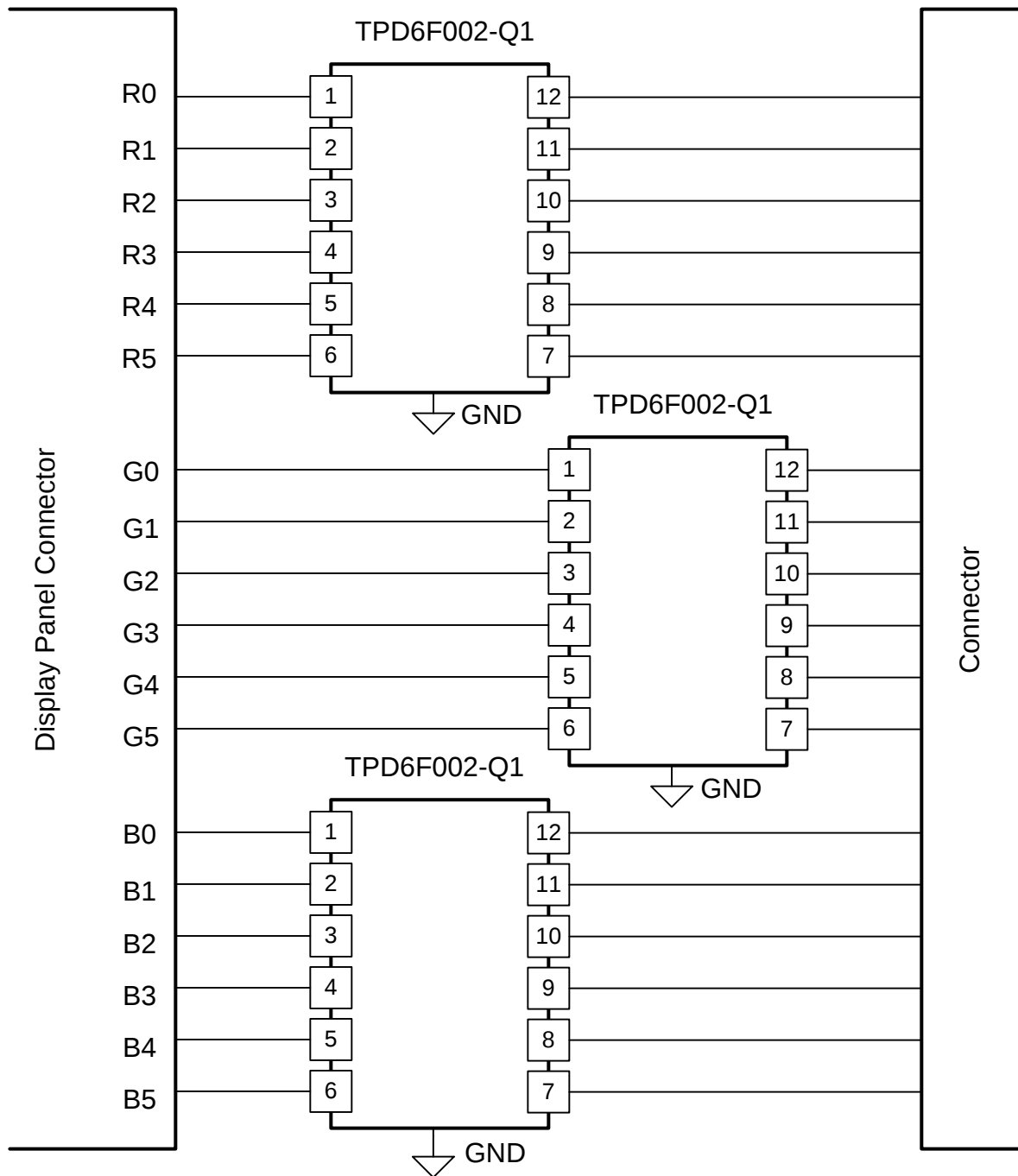


Figure 7. Display Panel Schematic

Typical Application (continued)

9.2.1 Design Requirements

For this design example, three TPD6F002-Q1 devices are being used in an 18-bit display panel application. This will provide a complete ESD and EMI protection solution for the display connector.

Given the display panel application, the following parameters are known.

DESIGN PARAMETER	VALUE
Signal range on all pins except GND	0 V to 5 V
Operating Frequency	50 MHz

9.2.2 Detailed Design Procedure

To begin the design process, some design parameters must be decided; the designer needs to know the following:

- Signal range of all the protected lines
- Operating frequency
- Crosstalk response

9.2.2.1 Signal Range on All Protected Lines

The TPD6F002-Q1 has 6 identical protection channels for signal lines. All I/O pins will support a signal range from 0 to 5.5 V.

9.2.2.2 Operating Frequency

The TPD6F002-Q1 has a 100 MHz –3 dB bandwidth, which supports the operating frequency for this display.

9.2.2.3 Crosstalk Response

The TPD6F002-Q1 has a –47 dB near-side crosstalk attenuation at 100 MHz, sufficient for this display.

9.2.3 Application Curves

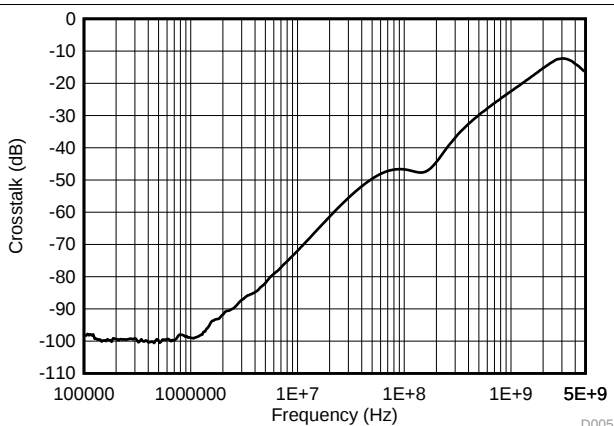


Figure 8. Near-Side Crosstalk

10 Power Supply Recommendations

This device is a passive EMI and ESD device so there is no need to power it. Care should be taken to not violate the recommended V_{IO} specification (5.5 V) to ensure the device functions properly.

11 Layout

11.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
 - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
 - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
 - Electric fields tend to build up on corners, increasing EMI coupling.

11.2 Layout Example

This application is typical of an 18-bit RGB display panel layout.

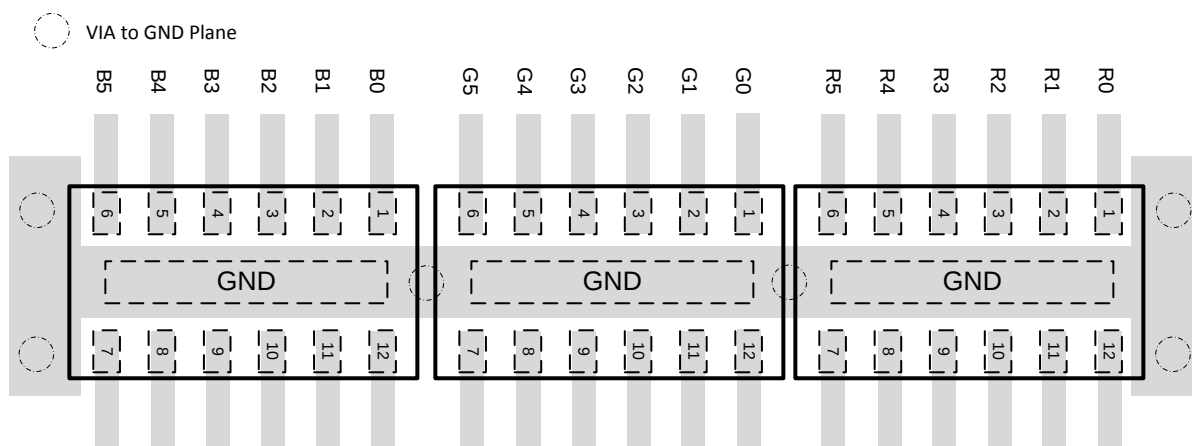


Figure 9. TPD6F002-Q1 Layout

12 器件和文档支持

12.1 商标

All trademarks are the property of their respective owners.

12.2 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.3 术语表

[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD6F002QDSVRQ1	ACTIVE	SON	DSV	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UNS	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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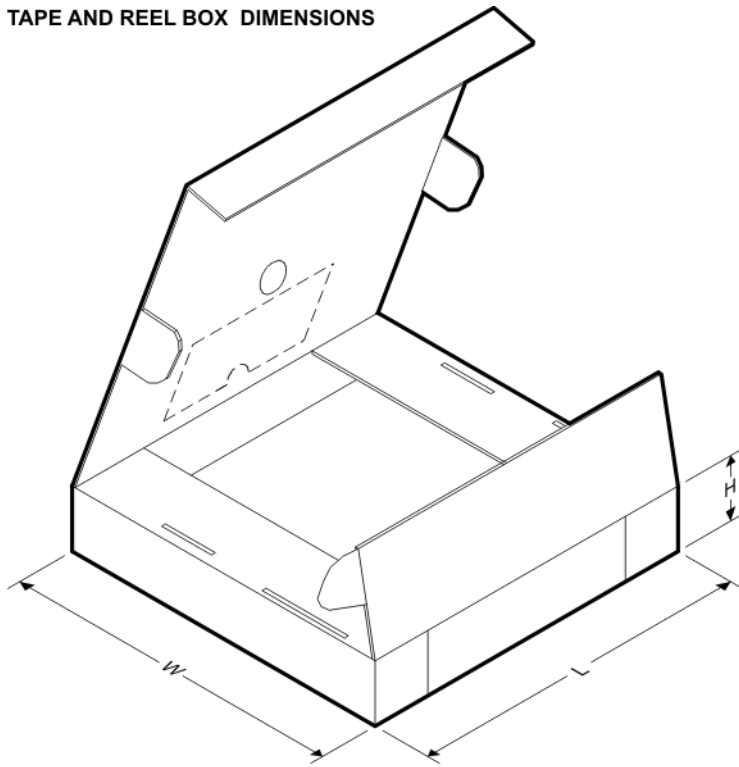
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD6F002QDSVRQ1	SON	DSV	12	3000	180.0	8.4	1.74	3.33	1.05	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

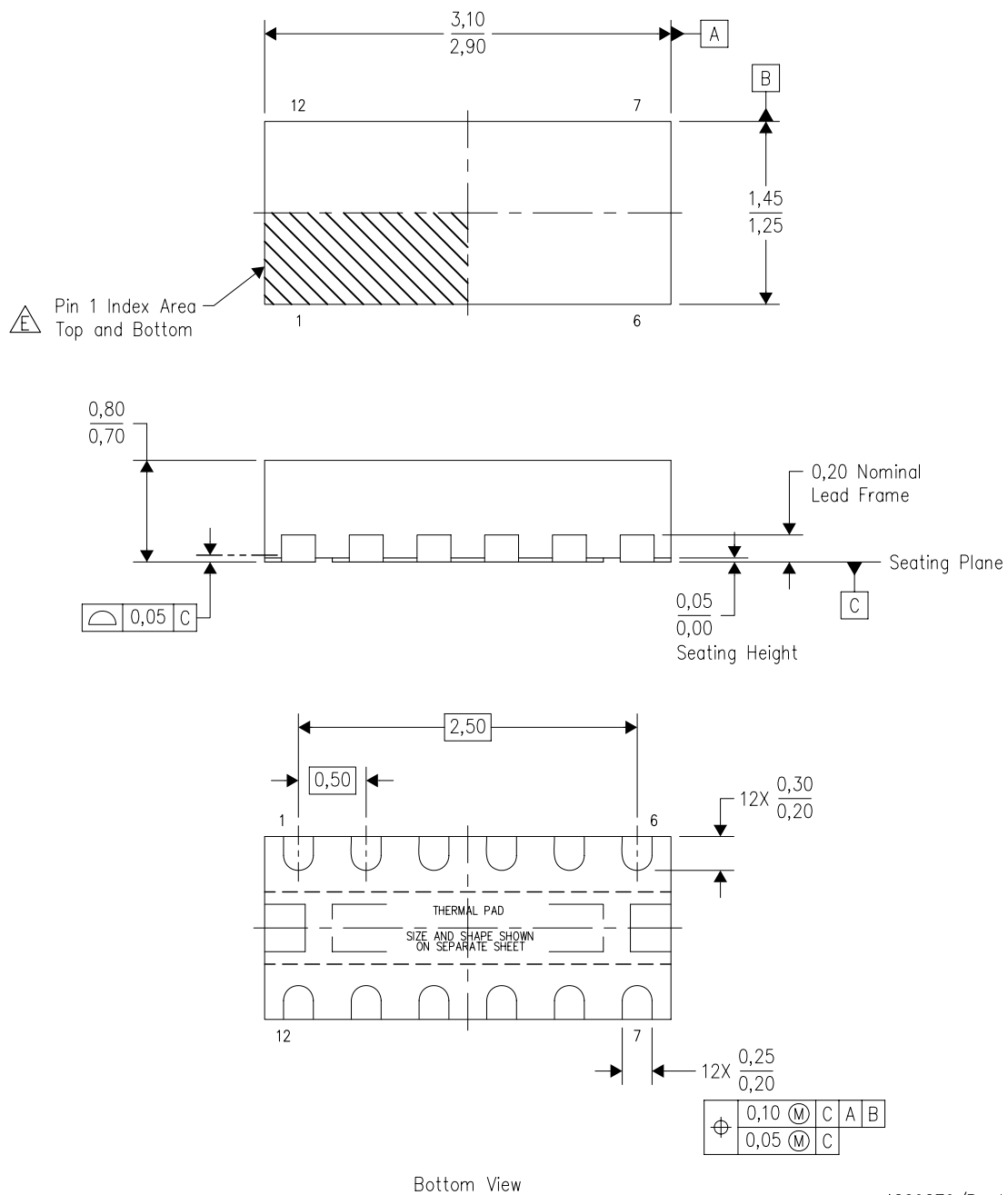


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD6F002QDSVRQ1	SON	DSV	12	3000	213.0	191.0	35.0

DSV (R-PWSON-N12)

PLASTIC SMALL OUTLINE NO-LEAD



4209279/B 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

THERMAL PAD MECHANICAL DATA

DSV (R-PWSON-N12)

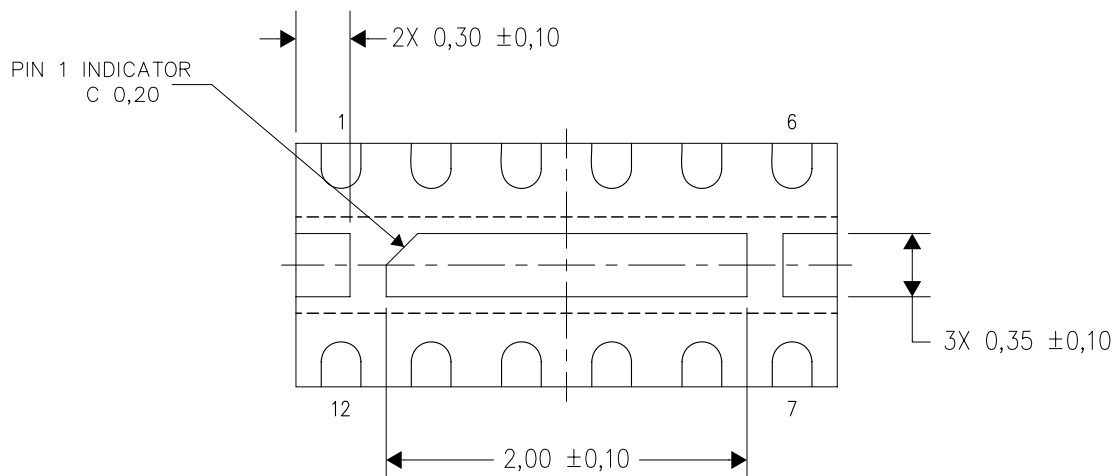
PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

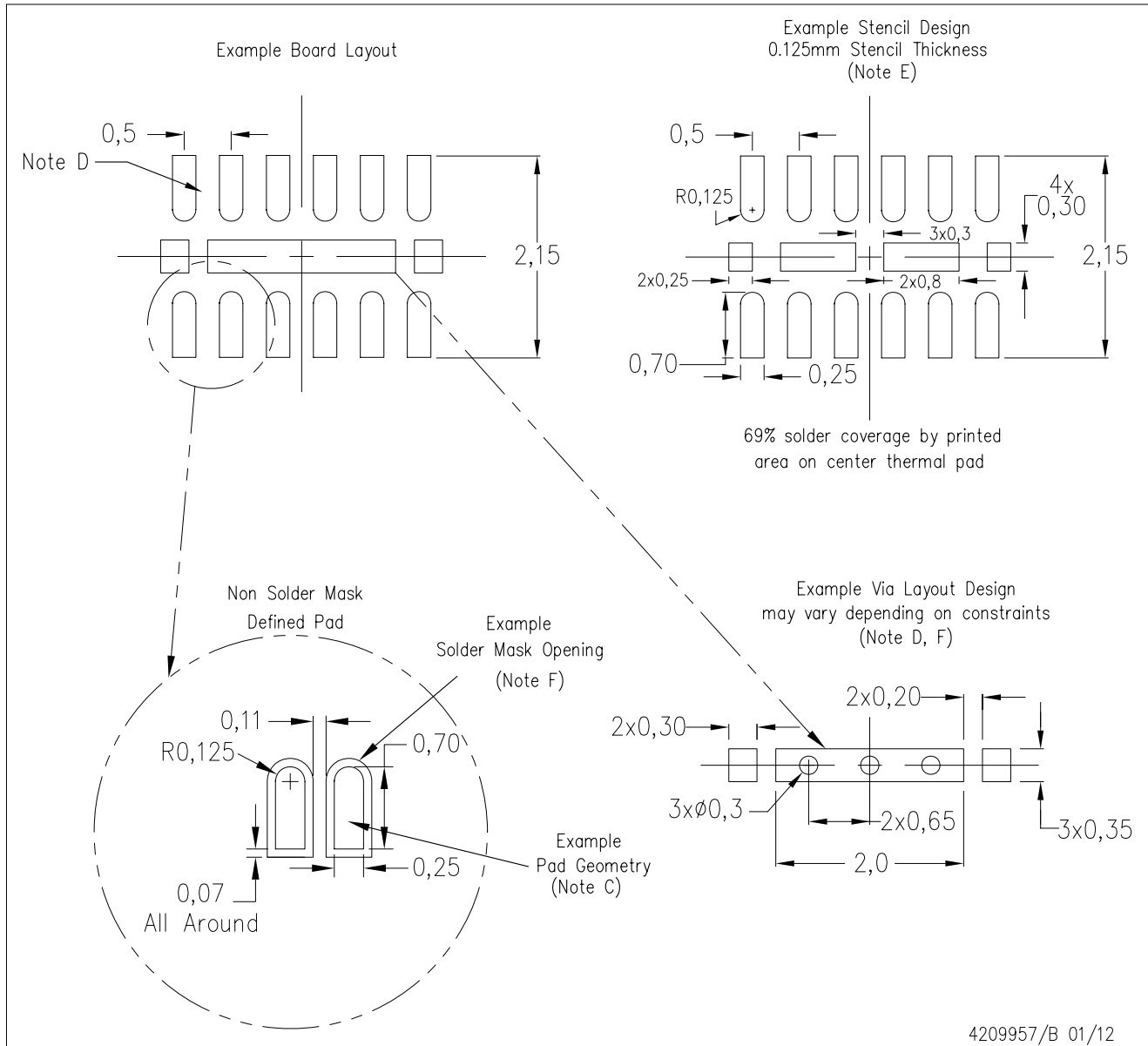
Exposed Thermal Pad Dimensions

4209318/B 12/11

NOTE: All linear dimensions are in millimeters

DSV (R-PWSON-N12)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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