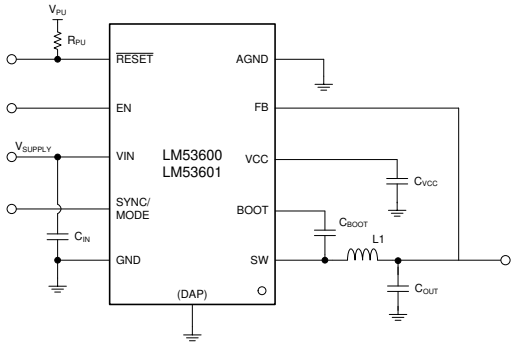
LM53600/01-Q1 0.65A/1A、36V 同步、2.1MHz 汽车级降压直流/直流转换器

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：-40°C 至 125°C 环境工作温度范围
  - 器件 HBM 分类等级 2
  - 器件 CDM 分类等级 C5
- -40°C 至 150°C 的结温范围（可用）
- 宽工作输入电压范围：3.55V 到 36V（瞬态电压高达 42V）
- 提供扩展频谱选项
- 2.1MHz 固定开关频率
- 低静态电流：23 μA
- 关断电流：1.8μA
- 可调、3.3V 或 5V 三种输出
- 最大电流负载：LM53600-Q1 为 650mA，LM53601-Q1 为 1000mA
- 引脚可选强制 PWM 模式
- 具有滤波和延迟释放功能的 $\overline{\text{RESET}}$ 输出
- 外部频率同步
- 内部补偿、软启动、电流限制和欠压锁定 (UVLO)
- 具有可湿性侧面和非可湿性侧面的 10 引脚 3mm x 3mm SON 封装

2 应用

- 汽车摄像头应用
- 汽车驾驶辅助系统
- 汽车车身应用



简化原理图 – 固定输出

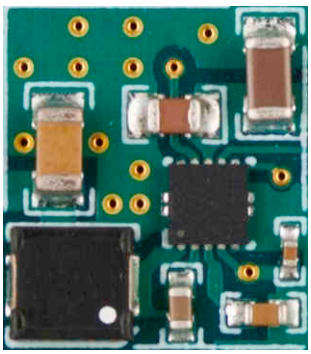
3 说明

LM53600-Q1 和 LM53601-Q1 同步降压稳压器器件针对汽车应用进行了优化，能够提供 5V、3.3V 的输出电压或可调输出电压。LM53600-Q1 支持高达 650mA 的负载电流，而 LM53601-Q1 支持高达 1000mA 的负载电流。LM53600-Q1 和 LM53601-Q1 器件可利用高级高速电路在 2.1MHz 的固定频率下实现从 18V 输入到 3.3V 输出的稳压。这两款器件采用创新型架构，在输入电压仅为 3.8V 时也可提供 3.3V 稳压输出。输入电压最高可达 36V，容许的最高瞬态电压达 42V，这简化了输入浪涌保护设计。开漏复位输出具有滤波和延迟释放功能，可提供正确的系统状态指示。凭借这一特性，器件无需使用附加监控元件，这节省了成本和电路板空间。这两款器件可在 PWM 和 PFM 两种模式之间无缝切换，并且静态电流仅为 23μA，这确保了其在所有负载条件下均可展现高效率和出色的瞬态响应。只需很少的外部元件，因此印刷电路板 (PCB) 布局可以更加紧凑。尽管 LM53600-Q1 和 LM53601-Q1 器件属于 Q1 级，但均可在 –40°C 至 150°C 的结温范围内保证电气特性。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
LM53600-Q1	WSON (10)	3.00mm x 3.00mm
LM53601-Q1		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



汽车类 11.2mm x 12.7mm 布局

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

Changes from Revision C (April 2021) to Revision D (May 2021) — **Page**

- 添加了非可湿性侧面选项 1

Changes from Revision B (February 2016) to Revision C (April 2021) — **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式 1

Changes from Revision A (December 2015) to Revision B (February 2016) — **Page**

- Updated tables in the *Device Comparison Table* 3
- Removed last sentence in SYNC/MODE description in Pin Functions table in *Pin Configuration and Functions* 4
- Updated I_B Parameter in *节 7.5* table 6
- Changed R_{RESET} MAX from "80" to "120" in *节 7.5* table 6
- Changed V_{out} to $V_{out_3_3V}$, V_{out_5V}, and V_{out_ADJ} for 3.3-V, 5-V, and ADJ output voltage options in *节 7.6* table 8
- Corrected references for SNAU190 and SNAU191 in *节 12.1.1* 32

Changes from Revision * (June 2015) to Revision A (December 2015) — **Page**

- 将器件状态从产品预览更改为量产数据 1

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5 Device Comparison

LM53600-Q1 Devices

Part Number[(1)]	Output Voltage	Spread Spectrum	Package Qty [(2)]	Wettable (WF)/Non-Wettable Flanks (non-WF)
LM53600AQDSXRQ1	Adjustable	No	3000	WF
LM53600AQDSXTQ1	Adjustable	No	250	WF
LM536003QDSXRQ1	3.3 V	No	3000	WF
LM536003QDSXTQ1	3.3 V	No	250	WF
LM536005QDSXRQ1	5.0 V	No	3000	WF
LM536005QDSXTQ1	5.0 V	No	250	WF
LM53600MQDSXRQ1	Adjustable	Yes	3000	WF
LM53600MQDSXTQ1	Adjustable	Yes	250	WF
LM53600NQDSXRQ1	3.3 V	Yes	3000	WF
LM53600NQDSXTQ1	3.3 V	Yes	250	WF
LM53600LQDSXRQ1	5.0 V	Yes	3000	WF
LM53600LQDSXTQ1	5.0 V	Yes	250	WF
LM53600MQUDSXRQ1	Adjustable	Yes	3000	Non-WF

(1) LM53600-Q1 devices have maximum recommended operating current of 650 mA.
(2) See Package Option Addendum for tape and reel details as well as links used to order parts.

LM53601-Q1 Devices

Part Number[(1)]	Output Voltage	Spread Spectrum	Package Qty [(2)]	Wettable (WF)/Non-Wettable Flanks (non-WF)
LM53601AQDSXRQ1	Adjustable	No	3000	WF
LM53601AQDSXTQ1	Adjustable	No	250	WF
LM536013QDSXRQ1	3.3 V	No	3000	WF
LM536013QDSXTQ1	3.3 V	No	250	WF
LM536015QDSXRQ1	5.0 V	No	3000	WF
LM536015QDSXTQ1	5.0 V	No	250	WF
LM53601MQDSXRQ1	Adjustable	Yes	3000	WF
LM53601MQDSXTQ1	Adjustable	Yes	250	WF
LM53601NQDSXRQ1	3.3 V	Yes	3000	WF
LM53601NQDSXTQ1	3.3 V	Yes	250	WF
LM53601LQDSXRQ1	5.0 V	Yes	3000	WF
LM53601LQDSXTQ1	5.0 V	Yes	250	WF
LM536015QUDSXRQ1	5.0 V	No	3000	Non-WF
LM536013QUDSXRQ1	3.3 V	No	3000	Non-WF
LM53601MQUDSXRQ1	Adjustable	Yes	3000	Non-WF

(1) LM53601-Q1 devices have maximum recommended operating current of 1000 mA.
(2) See Package Option Addendum for tape and reel details as well as links used to order parts.

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6 Pin Configuration and Functions

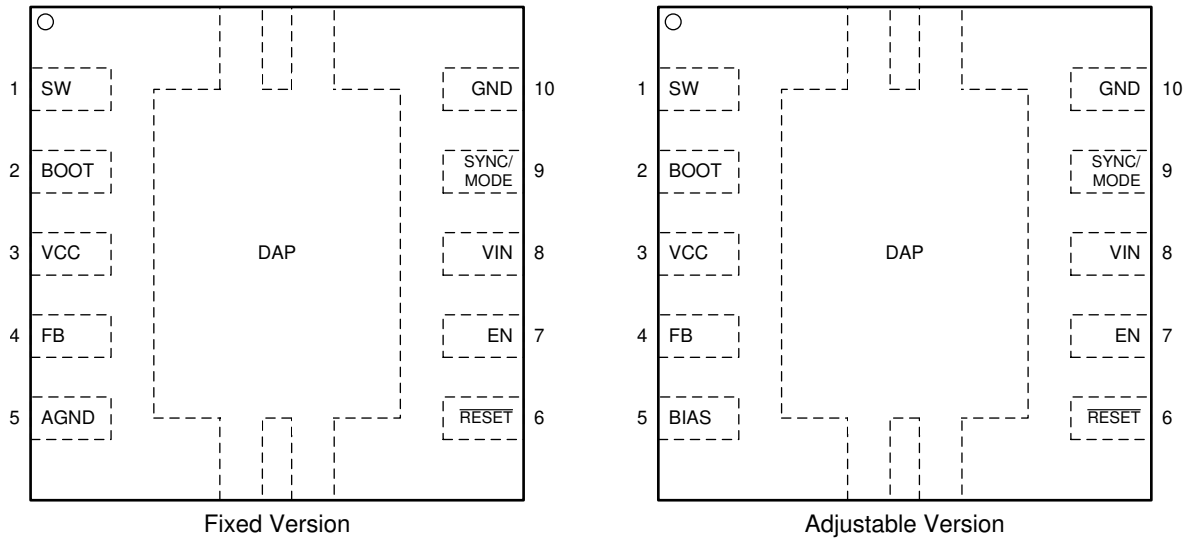

图 6-1. DSX Package 10-Pin WSON Top View

表 6-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	SW	P	Regulator switch node. Connect to output inductor.
2	BOOT	I	High side gate driver upper supply rail. Connect a 100-nF capacitor from SW pin to BOOT. An internal diode charges the capacitor while SW node is low.
3	VCC	P	Internal 3-V regulator output. Used as supply to internal control circuits. Connect a high quality 1.0-μF capacitor from this pin to AGND for fixed versions or to GND for adjustable versions.
4	FB (Fixed Versions)	I/P	Fixed version only, this pin serves as feedback for output voltage as well as power source for VCC’s regulator. Connect to output node. Place 10-nF bypass capacitor immediately adjacent to this pin.
	FB (ADJ Version)	I	ADJ version only, this pin serves as feedback for output voltage only. Connect to output through a voltage divider which determines output voltage set point.
5	AGND (Fixed Version)	G	Fixed versions only, this is the ground to which input signals and FB are compared.
	BIAS (ADJ Version)	P	Power source for VCC’s regulator. Connect to output node. Place 10-nF bypass capacitor immediately adjacent to this pin.
6	$\overline{\text{RESET}}$	O	Open drain reset output. Connect to suitable voltage supply through a current limiting pull up resistor. High = regulator OK, Low = regulator fault. Will go low when EN = low. See Detailed Description.
7	EN	I	Enable input to regulator. High = on, Low = off. Can be connected to Vin. Do not float.
8	VIN	I	Input supply to regulator. Connect input bypass capacitors directly between this pin and GND.
9	SYNC/MODE	I	This is a multifunction mode control input which is tolerant of voltages up to input voltage. With a valid synchronization signal at this pin, the device will switch in forced PWM mode at the external clock frequency and synchronize with it at the rising edge of the clock. See the *Electrical Characteristics* for synchronization signal specifications. With this input tied high, the device will switch at the internal clock frequency in forced PWM mode. With this input tied low, the device will switch at the internal clock frequency in AUTO mode with diode emulation at light load. Spread spectrum is disabled if there is a valid synchronization signal. Do not float.
10	GND	G	Bypass to VIN immediately adjacent to this pin.
DAP (EXPOSED PAD)	Thermal, GND	Thermal	Connect to ground – The sole function of the DAP interface is the thermal improvement of the device, a direct thermal connection to a ground plane is required. The DAP is not meant as an electrical interconnect. Electrical characteristics are not ensured.

(1) G = Ground, I = Input, O = Output, P = Power

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7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)

	MIN	MAX	UNIT
VIN to GND[1]	–0.3	42	V
SW to GND[2]	–0.3	VIN+0.3	
BOOT to SW	–0.3	3.6	
EN to GND [1]	–0.3	42	
BIAS to GND: LM53600-Q1/LM53601-Q1-ADJ	–0.3	16	
FB to GND : LM53600-Q1/LM53601-Q1 - 3.3 V, LM53600-Q1/LM53601-Q1 - 5.0 V	–0.3	16	
FB to GND : LM53600-Q1/LM53601-Q1-ADJ	–0.3	5.5	
$\overline{\text{RESET}}$ to GND	–0.3	8	
$\overline{\text{RESET}}$ sink current[3]		8	mA
SYNC/MODE to GND[1]	–0.3	42	V
VCC	–0.3	3.6	
GND[4] to AGND (Fixed version only)	–1	2	
Storage temperature, T_{stg}	–40	150	°C

(1) A maximum of 42 V can be sustained at this pin for a duration of ≤100 ms at a duty cycle of ≤1%.
(2) A voltage of 2-V below GND and 2-V above VIN can appear on this pin for ≤200 ns with a duty cycle of ≤ 0.01%.
(3) Do not exceed pin’s voltage rating.
(4) This specification applies to voltage durations of 1 µs or less. The maximum D.C. voltage should not exceed ±0.3 V.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	VIN, SW, CBOOT	±2000	V
			EN, BIAS, $\overline{\text{RESET}}$, FB, SYNC, PWM, VCC	±2000	
		Charged device model (CDM), per AEC Q100-011	Other pins	±750	
			Corner pins (1, 5, 6, and 10)	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage range after startup[1]		3.8		36	V
Output voltage range	5 V[2]	0		5.5	V
	3.3 V[2]	0		3.63	
Output adjustment range[3]for LM53600-Q1-ADJ [2], LM53601-Q1-ADJ[2]		3.3		6	V
Load current range	LM53600-Q1	0		650	mA
	LM53601-Q1	0		1000	
Operating junction temperature[4]		–40		150	°C

(1) An extended input voltage range to 3.55 V is possible; see 节 7.6. See input UVLO in 节 7.5 for startup conditions.
(2) Output voltage should not be allowed to fall below 0 V during normal operation.
(3) The LM53600-Q1 and LM53601-Q1 devices can operate outside of the listed range output voltage range. For output voltage outside of the listed range, contact Texas Instruments concerning alternate application circuit BOM and additional operational limitations such as higher I_Q.
(4) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

7.4 Thermal Information

THERMAL METRIC[1]		LM53600-Q1, LM53601-Q1 DSX (WSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction -to-ambient thermal resistance	46.2	°C/W
$R_{\theta JC}$	Junction -to-case (top) thermal resistance	31.5	°C/W
$R_{\theta JB}$	Junction -to-board thermal resistance	20.9	°C/W
Φ_{JT}	Junction- to-top characterization parameter	0.3	°C/W
Φ_{JB}	Junction-to-board characterization parameter	21.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics

Limits apply to the recommended operating junction temperature range of –40°C to 150°C, unless otherwise noted. Minimum and maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_j = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{in} = 13.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Initial output voltage accuracy	V_{in}= 3.8 V to 36 V T_j=25°C, Open Loop	–1%		1%	
		V_{in}= 3.8 V to 36 V, Open Loop	–1.5%		1.5%	
I_Q	Operating quiescent current; measured at V_{IN} pin	V_{in}= 13.5 V, Not switching V_{bias}= 5 V		6.5		µA
		V_{in}= 13.5 V, Not switching V_{bias}= 5 V, T_j= 85°C			16	
I_B	Bias current into BIAS pin for adjustable versions and FB pin for fixed versions	V_{in}= 13.5 V, Not switching V_{bias}= 5 V, Mode = 0 V		46	80	
I_{SD}	Shutdown quiescent current; measured at V_{IN} pin	EN = 0, VIN = 13.5 V T_j = 25°C		1.8		µA
		EN = 0, VIN = 13.5 V T_j = 85°C			3	
V_{in_UVLO}	Minimum input voltage to operate	Rising	3.2	3.6	3.75	V
$V_{in_UVLO_hyst}$	Minimum input voltage hysteresis	Hysteresis	0.2	0.3	0.35	V
V_{reset_OV}	$\overline{RESET}$ upper threshold voltage	Rising, % of Vout	105%	106.5%	110%	
V_{reset_UV}	$\overline{RESET}$ lower threshold voltage	Falling, % Vout	92%	94%	97%	
V_{reset_guard}	Magnitude of $\overline{RESET}$ lower threshold difference from steady state output voltage	Steady state output voltage and $\overline{RESET}$ threshold read at the same T_J, and V_{IN}	3.9%			
V_{reset_hyst}	$\overline{RESET}$ hysteresis as a percent of output voltage set point			1%		
V_{reset_valid}	Minimum input voltage for proper $\overline{RESET}$ function	50 µA pull-up to $\overline{RESET}$ pin, EN = 0 V, T_j = 25°C			1.5	V
V_{OL}	Low level $\overline{RESET}$ function output voltage	50 µA pull-up to $\overline{RESET}$ pin, Vin = 1.5 V, EN = 0 V, T_j = 25°C			0.4	V
		0.5mA pull-up to $\overline{RESET}$ pin, Vin = 13.5 V, EN = 0 V			0.4	
		1mA pull-up to $\overline{RESET}$ pin, Vin = 13.5 V, EN = 3.3 V			0.4	

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Limits apply to the recommended operating junction temperature range of –40°C to 150°C, unless otherwise noted. Minimum and maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_j = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{in} = 13.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{sw}	Switching frequency	V_{IN} = 13.5 V, Center frequency with spread spectrum, PWM operation	1.89	2.1	2.4	MHz
		V_{IN} = 13.5 V, Without spread spectrum, PWM operation	1.89	2.1	2.4	
		V_{IN} = 36 V, 3.3-V fixed output device and adjustable devices regardless of output voltage		1.0		
		V_{IN} = 36 V, 5-V fixed output device		1.5		
F_{SYNC}	Sync frequency range	Output setting + 1 V < V_{IN} < 18 V	1.9	2.1	2.3	MHz
D_{SYNC}	Sync input duty cycle range	High state input < 5.5 V and > 2.3 V	25%		75%	
$V_{SYNC/MODE}$	SYNC/MODE input threshold voltage	SYNC/MODE input high (MODE=FPWM)	1.5			V
		SYNC/MODE input low (MODE = AUTO with diode emulation)			0.4	
		SYNC/MODE input hysteresis	0.185		1	
F_{SSS}	Frequency span of spread spectrum operation(2)			±4%		
F_{PSS}	Spread spectrum pattern frequency(2)				30	Hz
$I_{SYNC/MODE}$	SYNC/MODE leakage current	Vin = 13.5 V, $V_{SYNC/MODE}$ = 3.3 V		1		µA
		V_{IN} = $V_{SYNC/MODE}$ = 13.5 V		5		
t_{MODE}	Mode change transition time (2)	To FPWM Mode 20 mA load, V_{IN} = 13.5 V		100		µs
		To AUTO Mode 20-mA load, V_{IN} = 13.5 V		60		
I_{L_HS}	High side switch current limit (1)	LM53600-Q1 Duty cycle approaches 0%	1.0	1.35	1.65	A
		LM53601-Q1 Duty cycle approaches 0%	1.5	1.83	2.1	
I_{L_LS}	Low side switch current limit	LM53600-Q1	0.65	0.78	0.93	A
		LM53601-Q1	1.0	1.2	1.43	
I_{L_ZC}	Zero-cross current limit MODE/SYNC = Low			–0.01		A
I_{L_NEG}	Negative current limit MODE/SYNC = High	LM53600-Q1		–0.7		A
		LM53601-Q1		–0.7		
R_{dson}	Power switch on-resistance	High side MOSFET Rdson		220		mΩ
		Low side MOSFET Rdson		200		
V_{EN}	Enable input threshold voltage - rising	Enable rising	1.7	-	2.0	V
V_{EN_HYST}	Enable threshold hysteresis		0.40	-	0.55	V
V_{EN_WAKE}	Enable Wake-up threshold		0.4			V
I_{EN}	Enable pin input current	V_{IN} = V_{EN} = 13.5 V		2.7		µA
V_{cc}	Internal Vcc voltage	V_{IN} = 13.5 V, V_{bias}= 0 V		3.05		V
		V_{IN} = 13.5 V, V_{bias}= 3.3 V		3.15		
V_{cc_UVLO}	Internal Vcc input under voltage lock-out	VCC rising		2.7		V
$V_{cc_UVLO_hyst}$	Input under voltage lock-out hysteresis	Hysteresis below V_{cc_uvlo}		190		mV

Limits apply to the recommended operating junction temperature range of –40°C to 150°C, unless otherwise noted. Minimum and maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_j = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{in} = 13.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{FB}	Input current from FB to AGND	LM53600-Q1-ADJ, FB = 1 V		20		nA
V_{ref}	Reference voltage for ADJ option only	T_j = 25°C	0.993	1	1.007	V
			0.985	1	1.015	
R_{RESET}	Rdson of $\overline{RESET}$ output			50	120	Ω
T_{SD}	Thermal shutdown rising threshold(2)		151	167	185	°C
T_{SDF}	Thermal shutdown falling threshold(2)		140	157		
T_{SD_hyst}	Thermal shutdown hysteresis(2)			10		
D_{max}	Maximum switch duty cycle(2)	Fsw = 2.1 MHz		76%		
		While in frequency fold back	96%			

(1) High side current limit is a function of duty factor. Current limit value is highest at small duty factor and less at higher duty factors.
(2) Ensured by design, statistical analysis and production testing of correlated parameters; not tested in production.

7.6 System Characteristics

The following specifications are ensured by design provided that the component values in the typical application circuit are used. These parameters are not ensured by production testing. Limits apply to the recommended operating junction temperature range of –40°C to 150°C, unless otherwise noted. Minimum and Maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at Tj = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: Vin = 13.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{in_min}	Minimum input voltage for full functionality at 500-mA load, after start-up	V_{OUT} = 3.3 V			3.55	V
	Minimum input voltage for full functionality at 100% of max rated load, after start-up	V_{OUT} = 3.3 V			3.8	V
$V_{out_3_3V}$	Output voltage for 3.3-V option	V_{IN} = 4.0 V to 36 V, I_{OUT} = Maximum recommended load current	3.23	3.3	3.37	V
		V_{IN} = 3.8 V to 36 V, I_{OUT}=100 µA to 100 mA, typical value in Auto Mode	3.23	3.33	3.39	
V_{out_5V}	Output voltage for 5-V option	V_{IN} = 5.8 V to 36 V, I_{OUT} = Maximum recommended load current	4.9	5	5.1	V
		V_{IN} = 5.5 V to 36 V, I_{OUT}=100 µA to 100 mA, typical value in Auto Mode	4.9	5.05	5.125	
V_{out_ADJ}	Output voltage ADJ option	V_{IN} = V_{OUT} + 0.6 V to 36 V, I_{OUT} = 100 mA, FPWM mode	–2%		+2%	
		V_{IN} = V_{OUT} + 0.6 V to 36 V, I_{OUT}=100 µA to 100 mA, Auto mode	–2%		+2.5%	
	Load regulation for ADJ option(1)	V_{IN} = V_{OUT} + 1 V to 36 V, I_{OUT} = 0 A to 1 A, T_J = 125°C, FPWM mode		–1%		
I_{Q_VIN} (2)	Input current to V_{IN} node of DC/DC utilizing the LM53600-Q1/LM53601-Q1	V_{IN} = 13.5 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A		23		µA
		V_{IN} = 13.5 V, V_{OUT} = 5 V, I_{OUT} = 0 A		30		
V_{DROP1}	Minimum input to output voltage differential to maintain regulation accuracy, without inductor DCR drop	V_{OUT}=3.3 V, I_{OUT}=1000 mA, +2/–3% output accuracy			0.6	V

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The following specifications are ensured by design provided that the component values in the typical application circuit are used. These parameters are not ensured by production testing. Limits apply to the recommended operating junction temperature range of –40°C to 150°C, unless otherwise noted. Minimum and Maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at Tj = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: Vin = 13.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DROP2}	Minimum input to output voltage differential to maintain $F_{SW} \geqslant 1.85$ MHz, without inductor DCR drop	V_{OUT} = 3.3 V, I_{OUT}=1000 mA, F_{SW} = 1.85 MHz, 2% regulation accuracy			2.0	V
Efficiency	Typical Efficiency without inductor loss	V_{IN} = 13.5 V, V_{OUT} = 5.0 V, I_{OUT} = 1 A		85%		
		V_{IN} = 13.5 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A		80%		
		V_{IN} = 13.5 V, V_{OUT} = 5.0 V, I_{OUT} = 0.65 A		86%		
		V_{IN} = 13.5 V, V_{OUT} = 3.3 V, I_{OUT} = 0.65 A		83%		

(1) 125°C is worst case temperature for load regulation. Layout is critical since adjustable option does not have an AGND terminal.
(2) See 节 8.3.7 in 节 8 for the meaning of this specification and how it can be calculated.

7.7 Timing Requirements

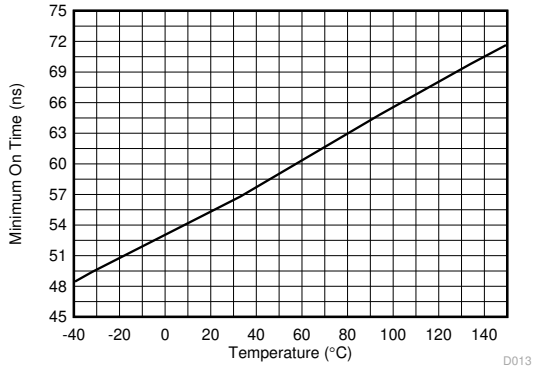
Limits apply to the recommended operating junction temperature range of –40°C to 150°C, unless otherwise noted. Minimum and Maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_j = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{in} = 13.5 V.

			MIN	NOM	MAX	UNIT
t_{on}	Minimum switch on time(1)	V_{IN} = 18 V, I_{OUT} = 500 mA		50	80.5	ns
t_{off}	Minimum switch off time(1)	I_{OUT} = 500 mA		90	125	
t_{reset_act}	Delay time to $\overline{RESET}$ high signal		4	6	8	ms
t_{reset_filter}	Glitch filter time constant for $\overline{RESET}$ function			24		µs
t_{SS}	Soft-start time	Time from first SW node pulse to Vref at 90%, $V_{IN} \geqslant$4.2 V	1.3	3	4.5	ms
t_{EN}	Turn-on delay(2)	Time from EN high until first SW node pulse. V_{IN} = 13.5, Cvcc = 1 µF		0.7		ms
t_W	Short circuit wait time (*Hiccup* time)			4.5		ms

(1) See 节 8
(2) Ensured by design, statistical analysis and production testing of correlated parameters; not tested in production.

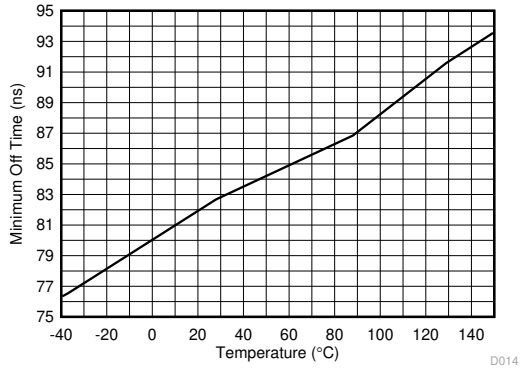
7.8 Typical Characteristics

V_{IN} = 13.5 V, T_A = 25°C (unless otherwise noted). Specified temperatures are ambient.



Device Type = 3.3-V Fixed Output
Input Voltage = 20 V Load = 500 mA

图 7-1. Minimum On-Time vs Temperature



Device Type = 1 A 5-V Fixed Output In Dropout
Output = 4.85 V Load = 500 mA

图 7-2. Minimum Off-Time vs Temperature

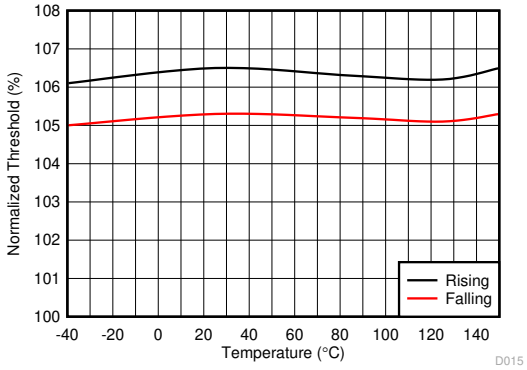
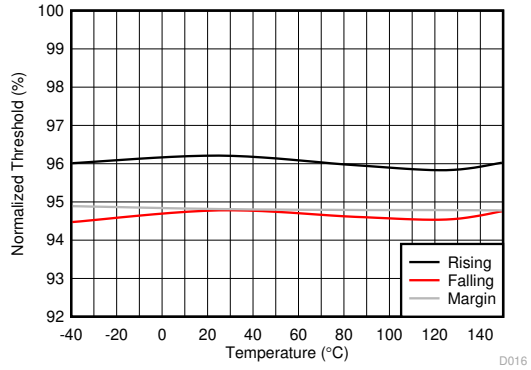


图 7-3. Upper RESET Threshold



Margin is the difference between the falling $\overline{\text{RESET}}$ threshold and actual regulation voltage which includes the effects of temperature.

图 7-4. Lower Reset Threshold

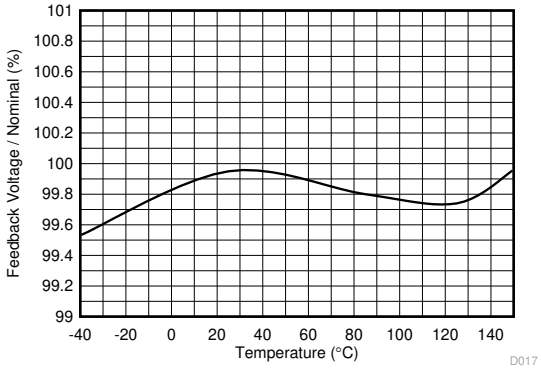


图 7-5. Normalized V_{FB} vs Temperature

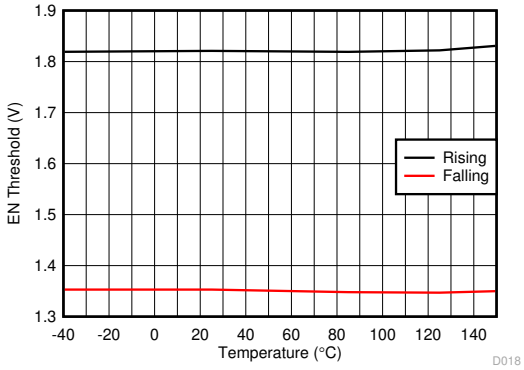


图 7-6. EN Threshold vs Temperature

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8 Detailed Description

8.1 Overview

The LM53600-Q1 and LM53601-Q1 devices are wide-input voltage range, low quiescent current, high-performance regulators with internal compensation designed specifically for the automotive market. These devices are designed to minimize end product cost and size while operating in demanding automotive environments. Normal operating frequency is 2.1 MHz allowing the use of small passive components. State of the art current limit allows the use of inductors that are smaller than those typically used in a 650mA or 1000mA regulator. 2.1MHz is above the AM band, allowing significant saving in input filtering. This part has a low unloaded current consumption eliminating the need for an external back-up LDO. The low shutdown current and high maximum operating voltage of the LM53600-Q1 and LM53601-Q1 devices also allows the elimination of an external load switch. To further reduce system cost, an advanced reset output is provided, which can often eliminate the use of an external reset or supervisory device.

The LM53600-Q1 and LM53601-Q1 devices are AEC Q1 qualified, and also have electrical characteristics ensured up to a maximum junction temperature of 150°C.

8.2 Functional Block Diagram

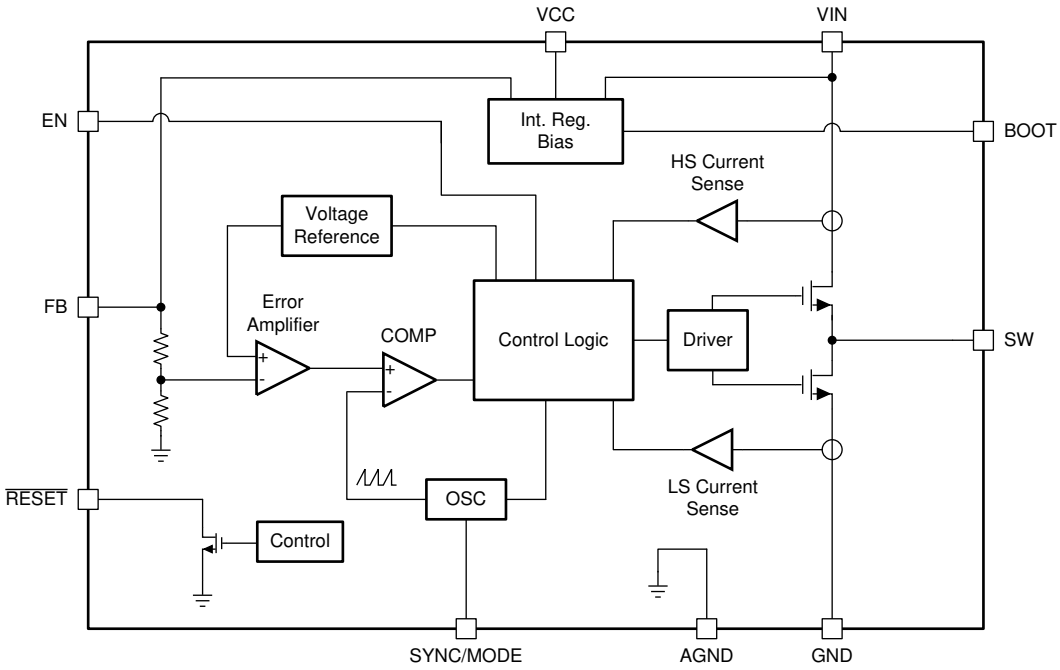

图 8-1. Fixed Versions

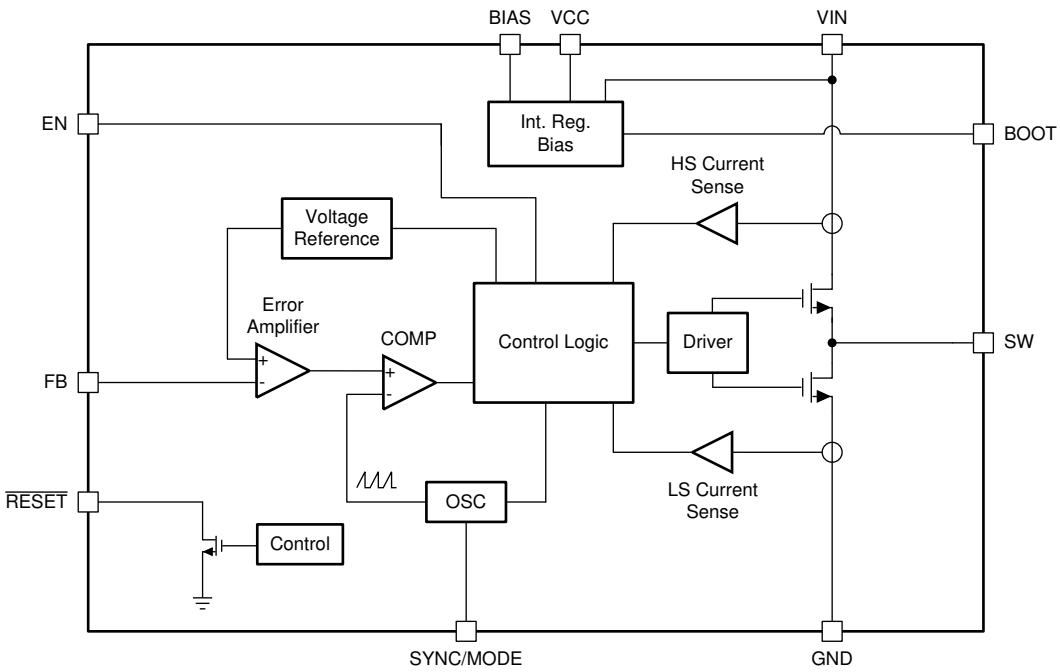

图 8-2. Adjustable Versions

8.3 Feature Description

8.3.1 Control Scheme

The control scheme of the LM53600-Q1 and LM53601-Q1 devices allows this part to operate under a wide range of conditions with a low number of external components. Peak current mode control allows a wide range of input voltages and output capacitance values, while maintaining a constant switching frequency. Stable operation is maintained while output capacitance is changed during operation as well. This allows use in systems that require high performance during load transients and which have load switches which remove loads as system operating state changes. Short minimum on- and off-times ensure constant frequency regulation over a wide range of conversion ratios. These on- and off- times allow for a duty factor window of 13% to 77% at 2.1-MHz switching frequency.

This architecture uses frequency foldback in order to achieve low dropout voltage maintaining output regulation as the input voltage falls close to output voltage. The frequency foldback is smooth and continuous, and activated as off-time approaches its minimum. Under these conditions, the LM53600-Q1 and LM53601-Q1 devices operate much like a constant off-time converter allowing maximum duty cycle to reach 97%, which allows output voltage regulation with 600-mV dropout.

If input voltage exceeds approximately 21 V, frequency is reduced smoothly as a function of input voltage. This frequency reduction allows output voltage regulation and current mode control to operate with duty factor below 13%. Since current mode control continues at high input voltage insensitivity to output capacitance is maintained. This form of fold back will not be active if input voltage is below 18 V, insuring constant frequency operation over normal automotive operating conditions.

High input voltage foldback has two settings; see F_{SW} under 36-V input conditions for detail. Since adjustable output voltage versions fold back under high input voltage conditions as though output voltage were 3.3 V, larger inductance and output capacitance is required if an adjustable device is used with output voltage above 4.2 V. If a 4.7-µH inductor is used in system with greater 4.2-V output using an adjustable device, the converter remains stable but may not achieve full output current when operating at high input voltages, such as 36 V, due to excessive inductor current ripple.

As load current is reduced, the LM53600-Q1 and LM53601-Q1 devices transition to light load mode if SYNC/MODE is low. In this mode, diode emulation is used to reduce RMS inductor current and switching frequency is reduced. Also, fixed voltage versions do not need a voltage divider connected to FB saving additional power. As

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a result, only 23 µA (typical, while converting 13.5 V to 3.3 V) is consumed to regulate output voltage if output is unloaded. Average output voltage increases slightly while lightly loaded.

8.3.2 Soft-Start Function

Soft-start time is fixed internally at about 3.0 ms. Soft-start is achieved by ramping the internal reference. The LM53600-Q1 and LM53601-Q1 devices operate correctly even if there is a voltage present on output before activation of the LM53600-Q1 or LM53601-Q1.

8.3.3 Current Limit

The LM53600-Q1 and LM53601-Q1 devices use two current limits which allow the use of smaller inductors than systems utilizing a single current limit. A coarse high side or peak current limit is provided to protect against faults and saturated inductors. High side current limit limits the duration of high sides FET's on period during a given clock cycle. A precision valley current limit prevents excessive average output current from the Buck converter of the LM53600-Q1 and LM53601-Q1 devices. A new switching cycle is not initiated until inductor current drops below the valley current limit. This scheme allows use of inductors with saturation current rated less than twice the rated operating current of the LM53600-Q1 or LM53601-Q1.

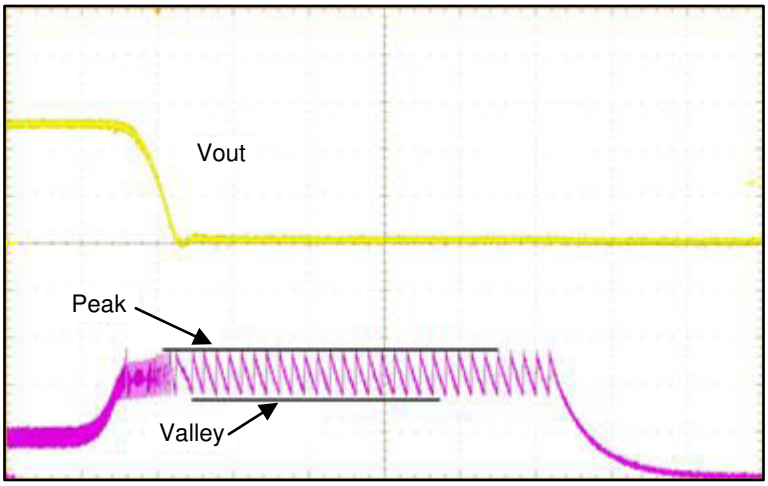

图 8-3. Current Limit Operation

图 8-3 shows the response of the LM53600-Q1 or LM53601-Q1 device to a short circuit: Peak current limit prevents excessive peak current while valley current limit prevents excessive average inductor current. After a small number of cycles, hiccup mode is activated.

8.3.4 Hiccup Mode

In order to prevent excessive heating and power consumption under sustained short circuit conditions, a hiccup mode is included. If an over current condition is maintained, the LM53600-Q1 or LM53601-Q1 device shuts off its output and waits for t_W (approximately 4.5 ms), after which the LM53600-Q1 or LM53601-Q1 restarts operation beginning by activating soft start.

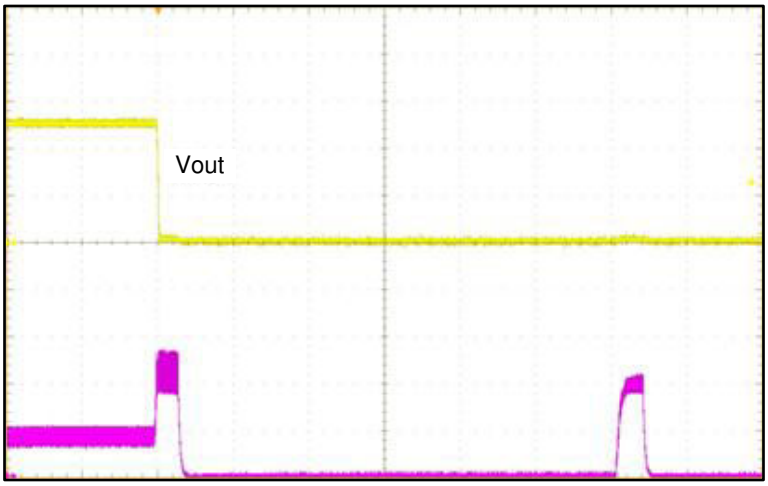

图 8-4. Hiccup Operation

图 8-4 shows hiccup mode operation: The switch node of the LM53600-Q1 LM53601-Q1 is high impedance after a short circuit or over current persists for a short duration. Periodically, the LM53600-Q1 or LM53601-Q1 attempts to restart. If the short has been removed before one of these restart attempts, the LM53600-Q1 or LM53601-Q1 operates normally.

8.3.5 RESET Function

While the reset function of the LM53600-Q1 and LM53601-Q1 devices resembles a standard power good function, its functionality is designed to replace a discrete reset IC, reducing BOM cost. There are three major differences between the reset function and the normal power good function seen in most regulators:

- A delay has been added for release of reset. See waveforms below.
- $\overline{\text{RESET}}$ output signals a fault (pulls its output to ground) while the part is disabled.
- $\overline{\text{RESET}}$ continues to operate with input voltage as low as 1.5 V. Below this input voltage, $\overline{\text{RESET}}$ output may be high impedance.

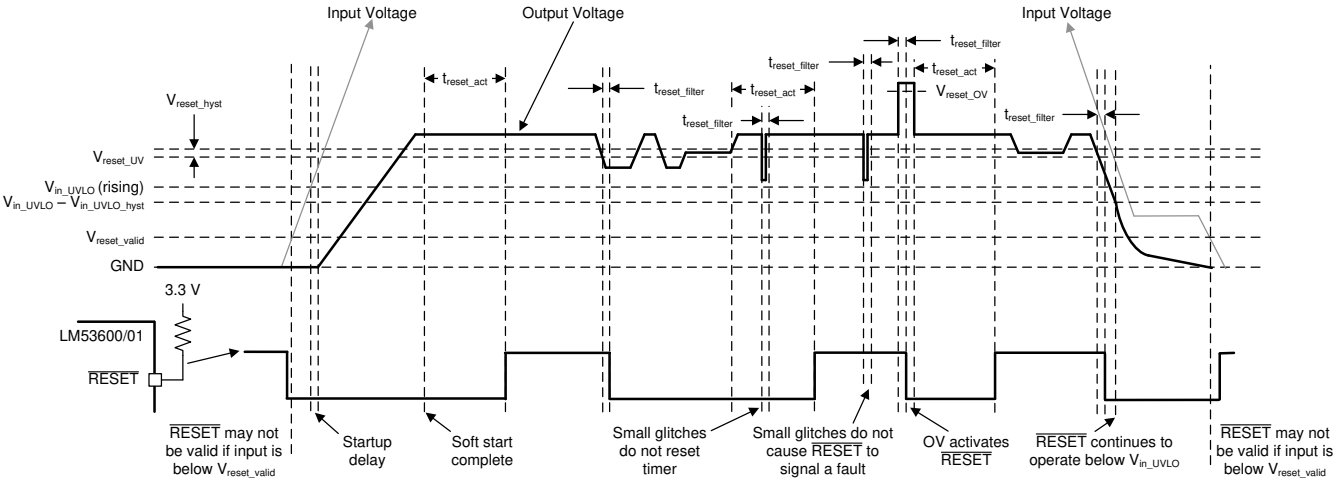

图 8-5. Reset Output Function Operation

The following table summarizes conditions that cause a fault to be flagged by $\overline{\text{RESET}}$. Once a fault is flagged, $\overline{\text{RESET}}$ will not be released (become high impedance) until either there is no fault for t_{reset_act} or VIN drops below V_{reset_valid}.

Table showing conditions that cause $\overline{\text{RESET}}$ to signal a fault (pull low).

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FAULT CONDITION INITIATED	FAULT CONDITION ENDS (AFTER WHICH T_{reset_act} MUST PASS BEFORE $\overline{RESET}$ OUTPUT IS RELEASED)
FB below V_{reset_UV} for longer than t_{reset_filt}	FB above V_{reset_UV} + V_{reset_hyst} for longer than t_{reset_filt}
FB above V_{reset_OV} for longer than t_{reset_filt}	FB below V_{reset_OV} - V_{reset_hyst} for longer than t_{reset_filt}
Junction temperature exceeds T_{SD}	Junction temperature falls below T_{SD} – T_{SD_hyst}
EN low	t_{EN} passes after EN becomes high(1)
VIN falls below V_{in_UVLO} - $V_{in_UVLO_hyst}$ or VCC pin falls below V_{cc_UVLO} - $V_{cc_UVLO_hyst}$	Voltage on V_{IN} exceeds V_{in_UVLO} and VCC exceed V_{cc_UVLO}

(1) As an additional safety feature, $\overline{RESET}$ remains low until approximately 1ms after soft start ends even if all other conditions in this table are met and t_{reset_act} has passed. Lockout during soft start does not require t_{reset_act} to pass before $\overline{RESET}$ is released.

The threshold voltage for the $\overline{RESET}$ function is specified taking advantage of the availability of the LM53600-Q1 internal feedback threshold to the $\overline{RESET}$ circuit. This allows a maximum threshold of 97% of selected output voltage to be specified at the same time as 95.7% of actual operating point. The net result is a more accurate reset function while expanding the system allowance for transient response without the need for extremely accurate internal circuitry. See output voltage error stack up comparison, below.

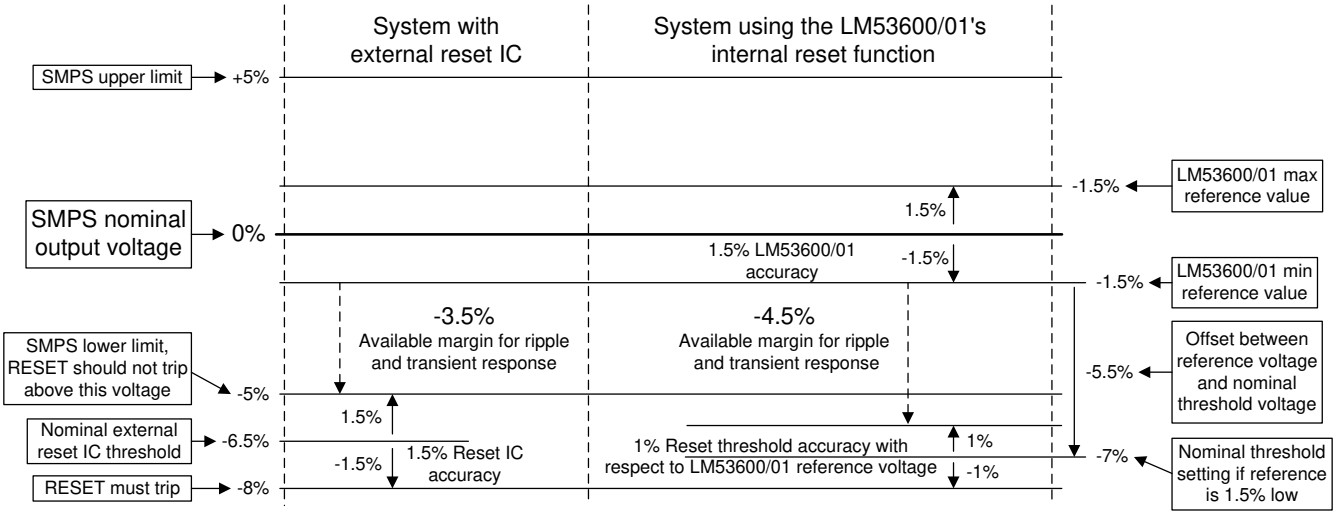

图 8-6. Reset Threshold Voltage Stack Up

8.3.6 Forced PWM Operation

When constant frequency operation is more important than light load efficiency, the SYNC/MODE input of the LM53600-Q1 and LM53601-Q1 devices should be pulled high, or a valid synchronization input be provided. Once activated, this feature ensures that the switching frequency will stay above the AM frequency band, while operating between the minimum and maximum duty cycle limits. Essentially, the diode emulation feature is turned off in this mode. This means that the device will remain in CCM under light loads. Under conditions where the device must reduce the on-time or off-time below the ensured minimum to maintain regulation, the frequency will reduce to maintain the effective duty cycle required for regulation. This occurs for very high and very low input/output voltage ratios.

This feature may be activated and deactivated while the part is regulating without removing the load. This feature activates and deactivates gradually, over approximately 40 µs, preventing perturbation of output voltage. When in FPWM mode, a limited reverse current is allowed through the inductor allowing power to pass from the regulators output to its input.

Note that while FPWM is activated, larger currents pass through the inductor, if lightly loaded, than in *auto* mode. This may result in more EMI, though at a predictable frequency. Once loads are heavy enough to necessitate CCM operation, FPWM mode has no measurable effect on regulator operation.

8.3.7 Auto Mode Operation and I_{Q_VIN}

If SYNC/MODE is held low for a period greater than a few microseconds, the LM53600-Q1 and LM53601-Q1 devices will enable automatic power saving light load operation and diode emulation. In this mode, if peak current needed to regulate output voltage drops below a selected value, the clock of the LM53600-Q1 or LM53601-Q1 device slows to maintain regulation. The gain of this clock slowing circuit is low to maintain stability. Output voltage with no load is approximately 1% higher than with a load high enough to allow full frequency operation.

I_{Q_VIN} is the current consumed by a converter utilizing a LM53600-Q1 or LM53601-Q1 device while regulating without a load. While operating without a load, the LM53600-Q1 or LM53601-Q1 is only powering itself. The LM53600-Q1 and LM53601-Q1 device draws power from two sources, its VIN pin, I_Q, and either its FB pin for fixed versions or BIAS pin for adjustable versions, I_B. Since BIAS or FB is connected to the circuit's output, the power consumed is converted from input power with an effective efficiency, η_{eff}, of ~80%. Here, effective efficiency is the added input power needed when lightly loading the converter of the LM53600-Q1 and LM53601-Q1 devices is divided by the corresponding additional load. This allows unloaded current to be calculated as follows:

$$I_{Q_VIN} = I_Q + I_{EN} + \left(I_B + I_{div}\right)\frac{\text{Output Voltage}}{\eta_{eff} \times \text{Input Voltage}} \tag{1}$$

where

- I_{Q_VIN} is the current consumed by the Buck converter utilizing the LM53600-Q1 or LM53601-Q1 while unloaded.
- I_Q is the current drawn by the LM53600-Q1 or LM53601-Q1 from its VIN terminal. See I_Q in section 7.6.
- I_{EN} is current drawn by the LM53600-Q1 or LM53601-Q1 from its EN terminal. Include this current if EN is connected to VIN. See I_{EN} in section 7.6. Note that this current drops to a very low value if connected to a voltage less than 5 V.
- I_B is bias/feedback current drawn by the LM53600-Q1 or LM53601-Q1 while the Buck converter utilizing it is unloaded. See I_B in section 7.6.
- I_{div} is the current drawn by the feedback voltage divider used to set output voltage for adjustable devices. This current is zero for fixed output voltage devices.
- η_{eff} is the light load efficiency of the Buck converter with I_{Q_VIN} removed from the Buck converter's input current. 0.8 is a conservative value that can be used under normal operating conditions

Note that the EN pin consumes a few microamperes when tied to high; see I_{EN}. Add I_{EN} to I_Q as shown in the above equation if EN is tied to V_{IN}. If EN is tied to a voltage less than 5 V, virtually no current is consumed allowing EN to be used as a UVL once a voltage divider is added.

8.3.8 SYNC Operation

Often it is desirable to synchronize the operation of multiple regulators in a single system. This technique results in better defined EMI and can reduce the need for capacitance on some power rails. The LM53600-Q1 and LM53601-Q1 devices provide a SYNC/MODE input, which allows synchronization with an external clock. The LM53600-Q1/LM53601-Q1 implements an in-phase locking scheme – the rising edge of the clock signal provided to the input of the LM53600-Q1 or LM53601-Q1 device corresponds to turning on the high side device within the LM53600-Q1 or LM53601-Q1. This function is implemented using phase locking over a limited frequency range eliminating large glitches upon initial application of an external clock. The clock fed into the LM53600-Q1 or LM53601-Q1 device replaces the internal free running clock but does not affect frequency fold-back operation. Output voltage will continue to be well regulated with duty factors outside of the normal 15% through 77% range though at reduced frequency.

The device remains in FPWM mode and operates in CCM for light loads when synchronization input is provided.

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8.3.9 Spread Spectrum

The spread spectrum is a factory option. In order to find which parts have spread spectrum enabled, see 节 5.

The purpose of the spread spectrum is to eliminate peak emissions at specific frequencies by spreading emissions across a wider range of frequencies than a part with fixed frequency operation. In most systems containing the LM53600-Q1 and LM53601-Q1 devices, low frequency conducted emissions from the first few harmonics of the switching frequency can be easily filtered. A more difficult design criterion is reduction of emissions at higher harmonics which fall in the FM band. These harmonics often couple to the environment through electric fields around the switch node. The LM53600-Q1 and LM53601-Q1 devices use a ±4% spread of frequencies which spread energy smoothly across the FM band but is small enough to limit sub-harmonic emissions below its switching frequency. Peak emissions at the part’s switching frequency are only reduced by slightly less than 1 dB, while peaks in the FM band are typically reduced by more than 6dB.

The LM53600-Q1 and LM53601-Q1 devices use a cycle to cycle frequency hopping method based on a linear feedback shift register (LFSR). Intelligent pseudo random generator limits cycle to cycle frequency changes to limit output ripple. Pseudo random pattern repeats by approximately 7 Hz which is below the audio band.

The spread spectrum is only available while the clock of the LM53600-Q1 and LM53601-Q1 devices is free running at its natural frequency. Any of the following conditions overrides spread spectrum, turning it off:

1. An external clock is applied to the SYNC/MODE terminal.
2. The clock is slowed due to operation low input voltage – this is operation in dropout.
3. The clock is slowed due to high input voltage – input voltage above approximately 21 V disables spread spectrum.
4. The clock is slowed under light load in Auto mode – this is normally not seen above 200 mA of load. In FPWM mode, spread spectrum is active even if there is no load.

8.4 Device Functional Modes

8.4.1 Shutdown

The LM53600-Q1 and LM53601-Q1 devices shut down most internal circuitry and both high side and low side power switches connected to its switch node under any of the following conditions:

1. EN is below V_{EN}
2. VIN is below V_{in_UVLO}
3. Junction temperature exceeds T_{SD}

Note that the above conditions have hysteresis. Also, $\overline{\text{RESET}}$ remains active to a very low input voltage, V_{reset_valid}.

8.4.2 FPWM Operation

If SYNC/MODE is above $V_{SYNC/MODE}$ high or a valid synchronizing is applied to SYNC/MODE, constant frequency operation is maintained across load. This requires negative current be allowed in the inductor if load is light. If a large negative load is present, operation is halted by a reverse current limit, $I_{L\text{-}NEG}$.

8.4.3 Auto Mode Operation

If SYNC/MODE is below $V_{SYNC/MODE}$ low, reverse current in the inductor is not allowed – this feature is called diode emulation. While load is heavy, operation is the same as in FPWM operation. If load is light, switching frequency is reduced saving energy and allowing regulation to be maintained. Note that while under loads which require moderate reduction of frequency, pulses often are seen if small groups, often called burst mode operation, which can increase output ripple. Under this condition, output ripple can be reduced by increasing output capacitance.

9 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LM53600-Q1 and LM53601-Q1 are step-down DC–DC converters, typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of either 1 A or 650 mA. The following design procedure can be used to select components for the LM53600-Q1 or LM53601-Q1. Alternately, the WEBENCH® Design Tool may be used to generate a complete design. This tool utilizes an iterative design procedure and has access to a comprehensive database of components. This allows the tool to create an optimized design and allows the user to experiment with various design options.

图 9-1 shows the minimum required application circuit for the fixed output voltage versions, while 图 9-2 shows the connections for complete processor control of the LM53601-Q1. Please refer to these figures while following the design procedures. 表 9-2 provides an example of typical design requirements.

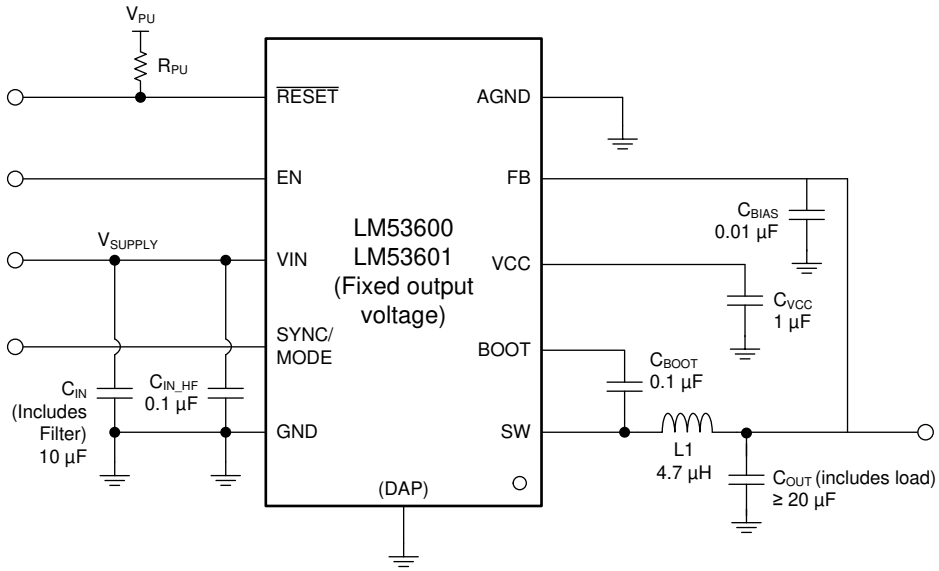

图 9-1. Off Battery, Automotive, Fixed Output Voltage, Buck, 2.1 MHz, Spread Spectrum

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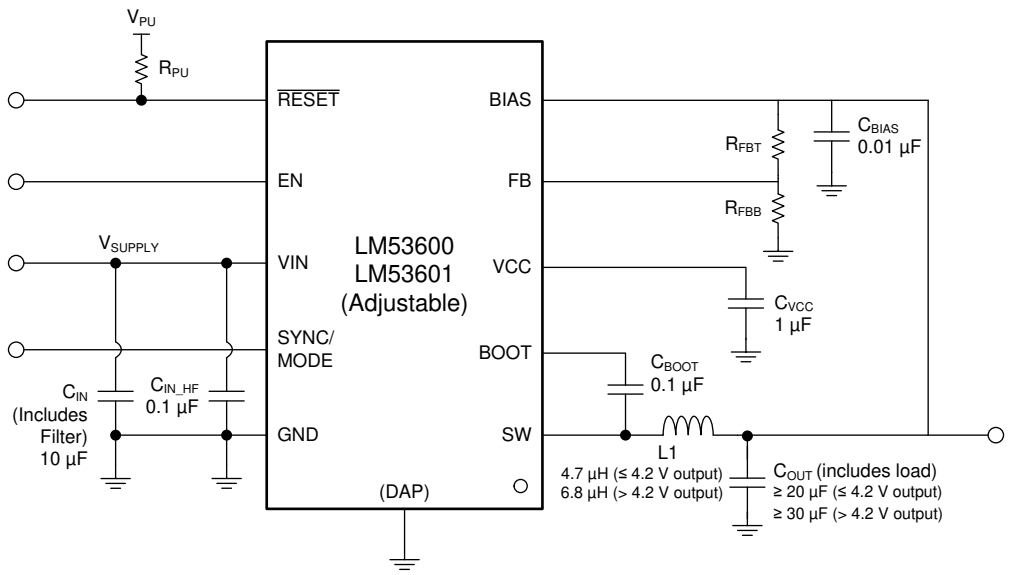

图 9-2. Off Battery, Automotive, Adjustable Output Voltage, Buck, 2.1 MHz, Spread Spectrum

9.2 Typical Applications

9.2.1 Off-Battery 5-V, 1-A Output Automotive Converter with Spread Spectrum

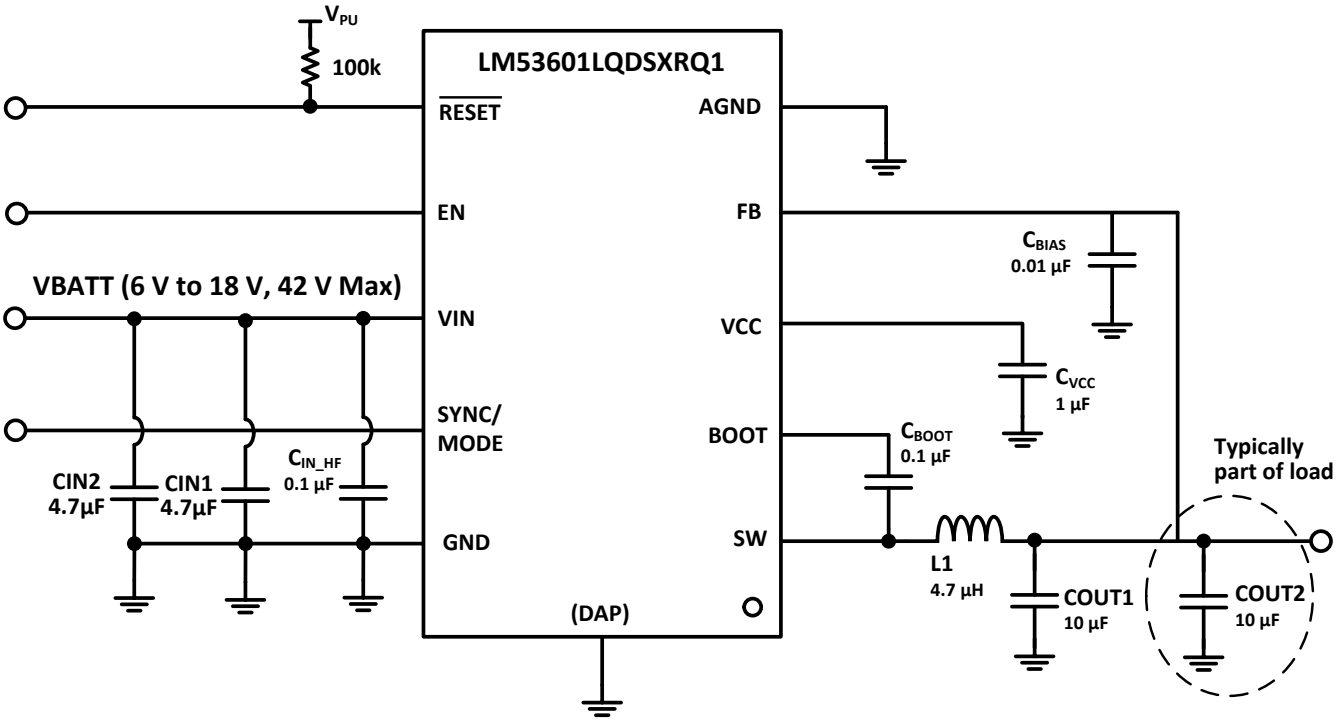

图 9-3. Typical LM53601LQDSXRQ1 Application Schematic

9.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 9-1 as the input parameters.

表 9-1. Design Parameters

DESIGN PARAMETER	VALUE	COMMENT
Input voltage range	6 V to 18 V with excursions to 42 V	This converter will run continuously up to 36 V
Output voltage	5 V	Fixed option used
Output current range	No Load to 1 A	
Light load mode	Switchable	
Spread spectrum	Enabled	Factory option

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Inductor Selection

The LM53600-Q1 and LM53601-Q1 devices run in current mode and has internal compensation. This compensation is stable with inductance between 4 µH and 10 µH. For most applications, 4.7 µH should be used with fixed 5-V and 3.3-V versions of the LM53600-Q1 and LM53601-Q1 devices. The output inductor is limited by current ripple while operating at high input voltage to a minimum rating of 4.7 µH for 3.3 V and 5-V fixed output devices. Since adjustable devices operate at the same frequency under high input voltage conditions as devices set to deliver 3.3 V, inductor current ripple at high input voltages can become excessive while using a 4.7µH while using an adjustable device that is delivering output voltage above 4.2 V. 6.8 µH is recommended if an adjustable device is used to produce output voltage above 4.2 V. Not exceeding 6.8 µH is recommended since use of large inductance causes poor transient load response. For the LM53601-Q1 (1-A output), a saturation rating of about 2 A is recommended since this is the maximum current limit rating. Likewise, a saturation current rating of about 1.5 A is recommended for the LM53600-Q1. See I_{L_HS} in the data sheet.

表 9-2. Output Inductor

PART TYPE	RECOMMENDED INDUCTANCE RATING(1)	RECOMMENDED MINIMUM SATURATION CURRENT(2)	COMMENT
LM53601-Q1 3.3 V and 5 V	4.7 µH	about 2 A	6.8 µH works in systems with less demanding transient load requirements
LM53601-Q1 ADJ set to ≤ 4.2-V output	4.7 µH	about 2 A	
LM53601-Q1 ADJ set to > 4.2-V output	6.8 µH	about 2 A	
LM53600-Q1 3.3 V and 5 V	4.7 µH	about 1.5 A	Up to 10 µH works in systems with less demanding transient load requirements
LM53600-Q1 ADJ set to ≤ 4.2-V output	4.7 µH	about 1.5 A	
LM53600-Q1 ADJ set to > 4.2-V output	6.8 µH	about 1.5 A	

(1) The values shown in this table are standard inductance ratings. The LM53600-Q1/LM53601-Q1 tolerates reduced inductance due to DC current and temperature.
(2) The LM53600-Q1/LM53601-Q1 tolerates partial saturation of inductors (reduction of ~40% reduction of inductance of the current value listed due to saturation. Partial saturation may reduce maximum current available at maximum voltage).

9.2.1.2.2 Output Capacitor Selection

The current mode control scheme of the LM53600-Q1 and LM53601-Q1 devices allows operation over a wide range of output capacitance. A minimum of 10 µF is needed to ensure stability. Capacitance above 20 µF is recommended to ensure load transient response typically desired in systems. 40 µF is recommended for applications with demanding load transient requirements and for which Auto mode ripple is important. 40 µF also aids devices with output voltage below 4-V transition into high voltage mode. Capacitance above 400 µF can cause excessive current to be drawn during start up so is not recommended. These capacitance values include load capacitance – only 10 µF is needed near to the LM53600-Q1 and LM53601-Q1 devices. Output capacitors

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should have low ESR to reduce output ripple. These capacitors should have at least X7R rating and should be of automotive grade if used in automotive applications.

表 9-3. Output Capacitor

LM53600-Q1 AND LM53601-Q1 TYPE AND SYSTEM NEED	RECOMMENDED MINIMUM TOTAL OUTPUT CAPACITANCE	COMMENTS
LM53600-Q1 5 V	20 µF	Approximately 200-mV/A step load response with 1-µs rise/fall time.
LM53601-Q1 5 V with typical system requirements	20 µF	Approximately 200-mV/A step load response with 1-µs rise/fall time.
LM53601-Q1 5V in high performance systems	40 µF	Approximately 150-mV/A step load, approximately 20-mV maximum Auto mode ripple
LM53600-Q1/LM53601-Q1 3.3 V and adjustable parts with less than 4.2-V output setting with typical system requirements	20 µF	Approximately 200-mV/A step load response with 1µs rise/fall time, up to 60 mV of ripple during transition into high voltage mode and in Auto mode.
LM53600-Q1/LM53601-Q1 3.3 V and adjustable parts with less than 4.2 V in high performance systems	40 µF	Approximately 150-mV/A step load, approximately 30-mV maximum Auto mode ripple, and 15-mV maximum HV mode transition ripple.
LM53600-Q1 ADJ set to greater than 4.2-V output	40 µF	Larger capacitance is necessitated by higher inductance needed.

9.2.1.2.3 Input Capacitor Selection

Input capacitors serve two important functions: The first is to reduce input voltage ripple into the LM53601-Q1 and the input filter of the system. The second is to reduce high frequency noise. These two functions are implemented most effectively with separate capacitors, see 表 9-4.

表 9-4. Input Capacitor

CAPACITOR	RECOMMENDED VALUE	COMMENT
C_{IN_HF}	0.1 µF	This capacitor is used to suppress high frequency noise originating during switching events. It is important to place capacitor as close to the LM53600-Q1 and LM53601-Q1 devices as design rules allow. Position is more important than exact capacity. Once high frequency propagates into a system, it can be hard to suppress or filter. Since this capacitor will be exposed to battery voltage in systems that operate directly off of battery, 50 V or greater rating is recommended.
C_{IN}	10 µF	This capacitance is used to suppress input ripple and transients due to output load transients. If CIN is too small, input voltage may dip during load transients resetting the system if the system is operated under low voltage conditions. 10 µF is intended to include all capacitance in the LM53600-Q1/LM53601-Q1’s input node. 4.7 µF adjacent to the LM53600-Q1 and LM53601-Q1 devices is recommended. Since this capacitor will be exposed to battery voltage in systems that operate directly off of battery, 50 V or greater rating is recommended.

表 9-5 shows recommended capacitor values other than input and output capacitors.

表 9-5. Other Capacitors

CAPACITOR	MINIMUM VALUE	COMMENT
C_{BOOT}	0.1 µF	While a voltage rating of only 5 V is necessary, using a higher voltage rating is recommended.
C_{VCC}	1 µF	While a voltage rating of only 5 V is necessary, 16-V capacitors have a low voltage coefficient.
C_{BIAS}	0.01 µF	This capacitor should be rated to survive output voltage.

Note that performance of converters utilizing an adjustable version of the LM53600-Q1 and LM53601-Q1 devices may be enhanced by adding C_{FF}, a capacitor in parallel with R_{FBT}. 100 pF is recommended.

9.2.1.2.4 FB Voltage Divider for Adjustable Versions

The adjustable version of the LM53600RB-Q1 and LM53601RB-Q1 devices regulates output voltage to a level that results in the FB node being V_{ref} which is approximately 1.0 V; see 节 7.5 Output voltage given a specific feedback divider can be calculated using the following equation:

$$\text{Output Voltage} = V_{ref} \times \frac{R_{FBB} + R_{FBT}}{R_{FBB}} \tag{2}$$

See typical applications schematic for adjustable versions of the LM53600-Q1 and LM53601-Q1 devices. Since the value of R_{FBT} is typically set by board leakage considerations, the above equation can be solved for R_{FBB}, the remaining unknown:

$$R_{FBB} = \frac{V_{ref} \times R_{FBT}}{\text{Output Voltage} - V_{ref}} \tag{3}$$

Note that typically, 100 kΩ is used for R_{FBT}.

9.2.1.2.5 R_{PU} - RESET Pull Up Resistor

While RESET is rated to sink up to 8 mA, under low, 1.5-V input voltage conditions, a low output level is only ensured with loads of 50 µA. If accurate RESET output is needed with 1.5-V input voltage, 100 kΩ should be used to pull up to 5 V, or a 66-kΩ resistor should be used when pulling up to a 3.3-V supply. If input voltage is above 3.8 V, values as low as 10 kΩ or 6.6 kΩ can be used to pull up to 5 V or 3.3 V, respectively. Other considerations, such as power consumption may increase any of the values listed above.

9.2.1.3 Application Curves

The following characteristics apply only to the circuit shown in 图 9-3. *These parameters are not tested and represent typical performance only.* Unless otherwise stated, the following conditions apply: V_{IN} = 13.5 V, T_A = 25°C.

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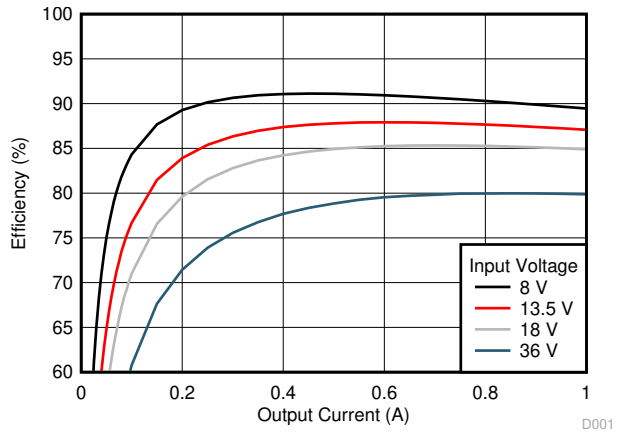
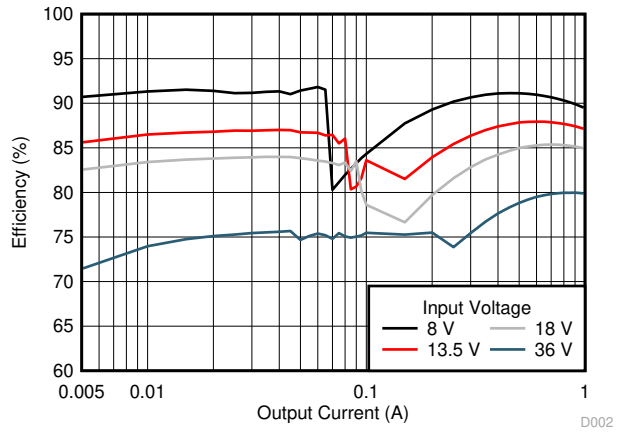


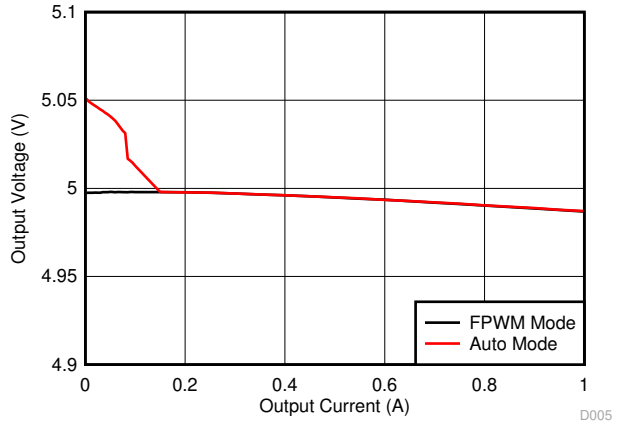
Device type = 1 A Mode = High 5-V Fixed Output

图 9-4. Efficiency



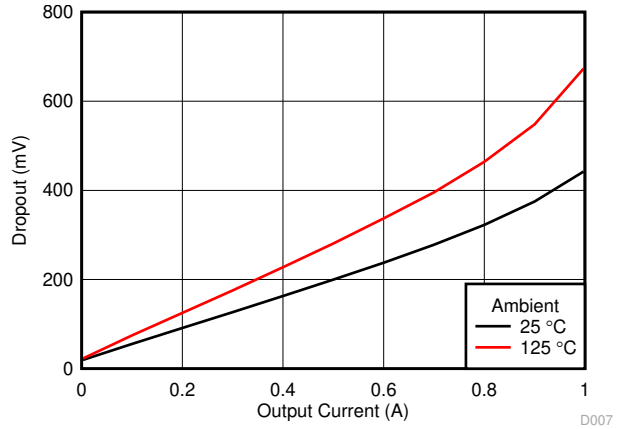
Device Type = 1 A Mode = Auto 5-V Fixed Output

图 9-5. Efficiency



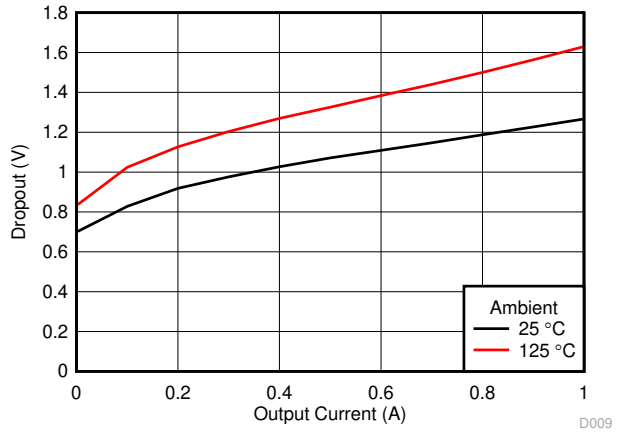
Device Type = 1 A 5-V Fixed Output

图 9-6. Load Regulation



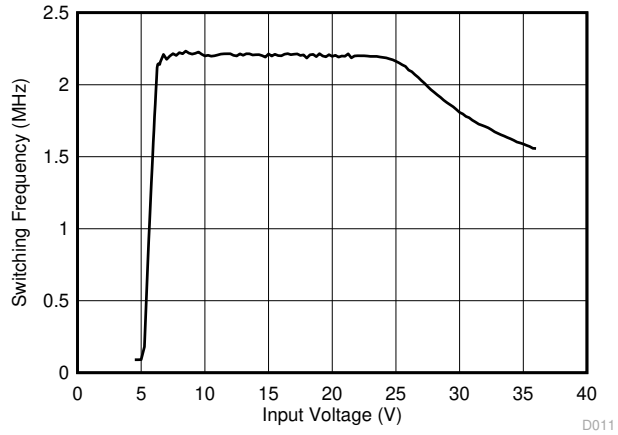
Device Type = 1 A 5-V Fixed Output Output = 4.85 V
92-mΩ Inductor

图 9-7. Dropout Voltage



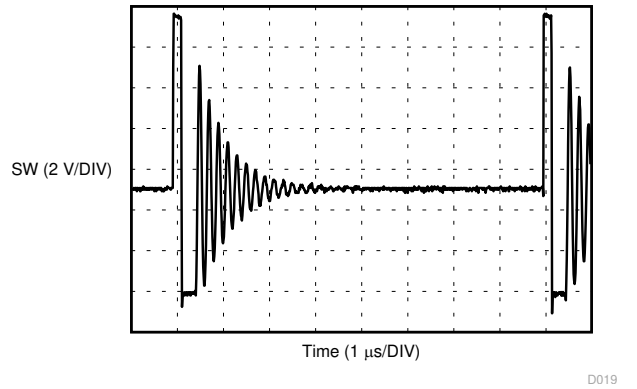
Device Type = 1 A 5-V Fixed Output 92-mΩ inductor
Frequency drops to 1.85MHz

图 9-8. Entry into Dropout



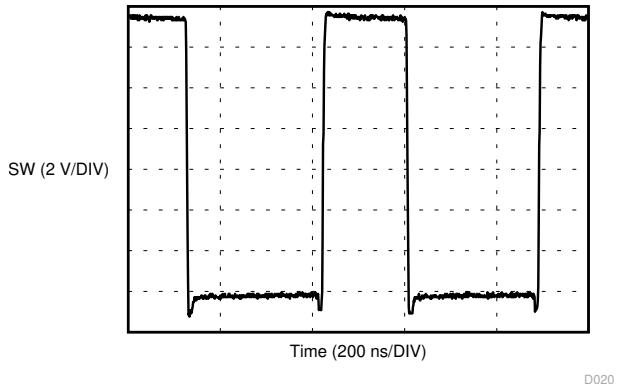
Device Type = 1 A 5-V Fixed Output Spread Spectrum
Load = 500 mA

图 9-9. Frequency vs. Input Voltage



Device Type = 1 A　Load = 10 mA　Mode = Auto
5-V Fixed Output

图 9-10. SW Node Operation



Device Type = 1 A　Mode = Auto　Load = 500 mA
5-V Fixed Output

图 9-11. SW Node Operation

9.2.2 Off-Battery 3.3 V, 1 A Output Automotive Converter with Spread Spectrum

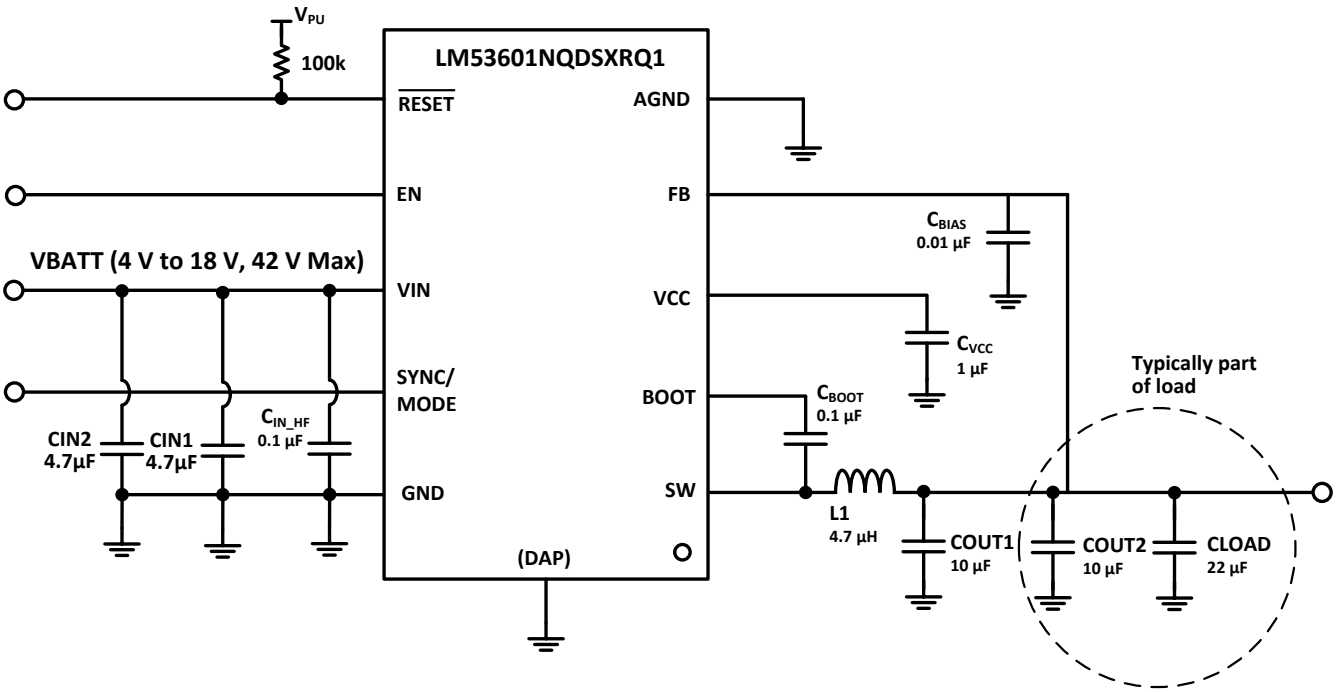


图 9-12. Typical LM53601NQDSXRQ1 Application Schematic

9.2.2.1 Design Requirements

For this design example, use the parameters in 表 9-6 as the input parameters.

表 9-6. Design Parameters

DESIGN PARAMETER	VALUE	COMMENT
Input voltage range	4 V to 18 V with excursions to 42 V	This converter will run continuously up to 36 V
Output voltage	3.3 V	Fixed option used
Output current range	No load to 1 A	
Light load mode	Switchable	
Spread spectrum	Enabled	Factory option

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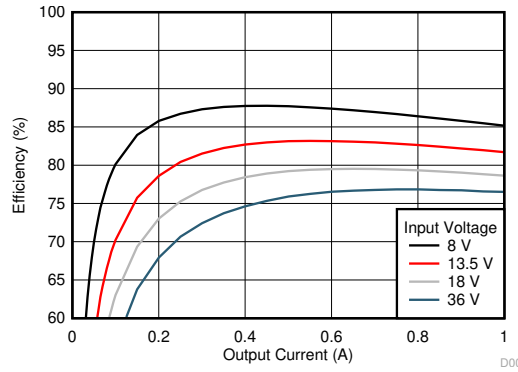
9.2.2.2 Design Procedure

The same detailed design procedure as shown starting in section 7.1.2.1 is used to create the schematic for this example. The most important difference is that the LM53601NQDSXRQ1 is used in place of the LM53601LQDSXRQ1. In addition, more output capacitance is recommended for this option. Most output capacitance will be part of the load and be used as input bypassing for the load.

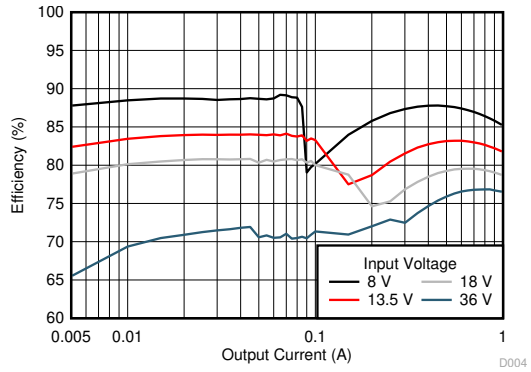
9.2.2.3 Application Curves

The following characteristics apply only to the circuit shown in 图 9-12. These parameters are not tested and represent typical performance only. Unless otherwise stated, the following conditions apply: V_{IN} = 13.5 V, T_A = 25°C.



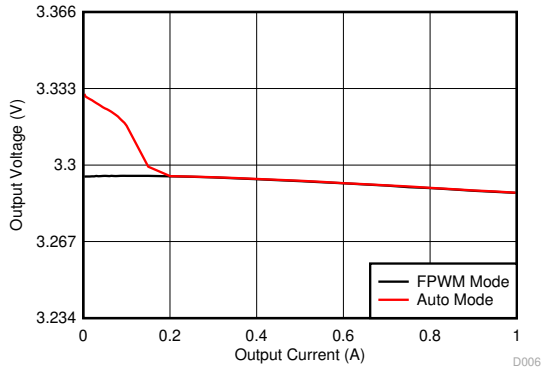
Device Type = 1 A Mode = FPWM 3.3-V Fixed Output

图 9-13. Efficiency



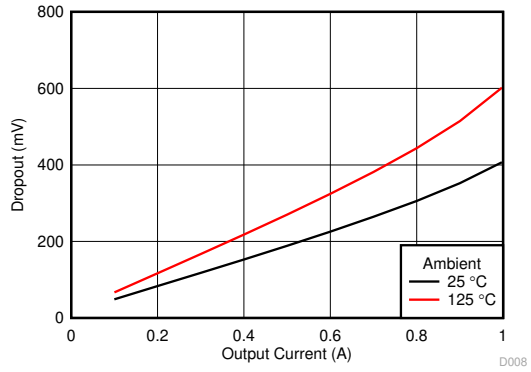
Device Type = 1 A Mode = Auto 3.3-V Fixed Output

图 9-14. Efficiency



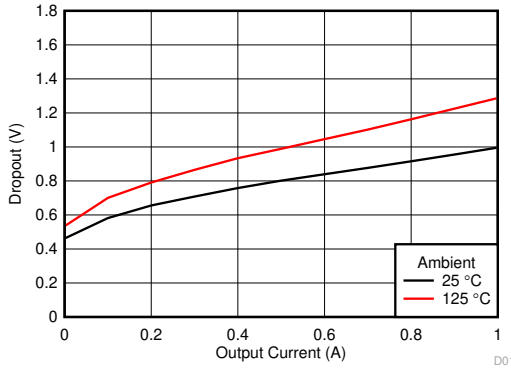
Device Type = 1 A 3.3-V Fixed Output

图 9-15. Load Regulation



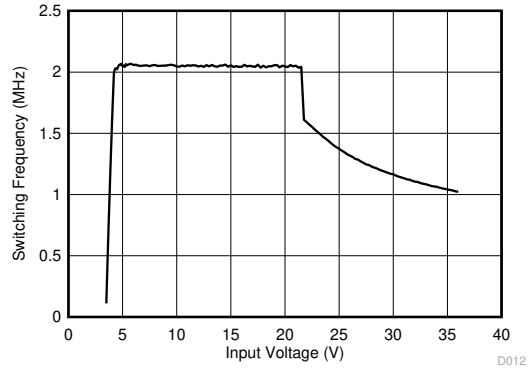
Device Type = 1 A Output = 3.2 V 92-mΩ Inductor
3.3-V Fixed Output

图 9-16. Dropout Voltage



Device Type = 1 A 3.3-V Fixed Output
92-mΩ Inductor Frequency Drops to 1.85 MHz

图 9-17. Entry into Dropout



Device Type = 1 A Spread Spectrum
3.3-V Fixed Output Load = 500 mA

图 9-18. Frequency vs. Input Voltage

9.3 Do's and Don't's

- Don't: Exceed the 节 7.1.
- Don't: Exceed the 节 7.2.

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- Don't: Exceed the 节 7.3.
- Don't: Allow the EN, FPWM or SYNC input to float.
- Don't: Allow the output voltage to exceed the input voltage, nor go below ground.
- Don't: Use the thermal data given in the Thermal Information table to design your application.
- Do: Follow all of the guidelines and/or suggestions found in this data sheet, before committing your design to production. TI Application Engineers are ready to help critique your design and PCB layout to help make your project a success.
- Do: Refer to the helpful documents found in 表 11-1 and 表 11-2.

10 Power Supply Recommendations

The LM53600-Q1 and LM53601-Q1 devices are designed for automotive direct off battery applications needing minimal protection. Protection recommended includes reverse battery protection and EMI/ESD filtering. The LM53600-Q1 and LM53601-Q1 devices are able to continue regulating during load dump with peak voltage less than 42 V, double battery (jump start) conditions down to input voltage as low as V_{DROP} above the selected output voltage. In addition, the LM53600-Q1 and LM53601-Q1 devices continue to operate though may be out of regulation with input voltage as low as 3.8 V. This allows the LM53600-Q1 and LM53601-Q1 devices to operate through cranking in all but the most demanding systems.

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low ESR ceramic input capacitors, can form an under-damped resonant circuit. This circuit may cause over-voltage transients at the VIN pin, each time the input supply is cycled on and off. The parasitic resistance will cause the voltage at the VIN pin to dip when the load on the regulator is switched on, or exhibits a transient. If the regulator is operating close to the minimum input voltage, this dip may cause the device to shutdown and/or reset. The best way to solve these kinds of issues is to reduce the distance from the input supply to the regulator and/or use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors will help to damp the input resonant circuit and reduce any voltage overshoots. A value in the range of 20 µF to 100 µF is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This can lead to instability, as well as some of the effects mentioned above, unless it is designed carefully. The *Simple Success with Conducted EMI for DC – DC Converters* User's Guide (SNVA489) provides helpful suggestions when designing an input filter for any switching regulator

In some cases, a Transient Voltage Suppressor (TVS) is used on the input of regulators. One class of this device has a *snap-back* V-I characteristic (thyristor type). The use of a device with this type of characteristic is not recommend. When the TVS *fires*, the clamping voltage drops to a very low value. If this holding voltage is less than the output voltage of the regulator, the output capacitors will be discharged through the regulator back to the input. This uncontrolled current flow could damage the regulator.

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11 Layout

11.1 Layout Guidelines

The following list is in order of importance starting with the most important item:-

- Place high frequency input bypass capacitor, Cinhf, as close to the LM53600-Q1 and LM53601-Q1 devices as possible.
- Connect AGND and GND to the DAP immediately adjacent to the LM53600-Q1 and LM53601-Q1 devices.
- Do not interrupt the ground plain under the loop containing the VIN and GND pins and Cinhf of the LM53600-Q1 and LM53601-Q1 devices.
- The boot capacitor, CBOOT, should be close to the LM53601-Q1 and the loop from the SW pin, through the boot capacitor and into the BOOT pin should be kept as small as possible.
- Keep the SW node as small as possible. It should be wide enough to carry the converter’s full current without significant drop.
- 4.7 µF of bypassing should be close to the input of the LM53600-Q1 and LM53601-Q1 devices.
- Place CVCC, the VCC pin’s bypass, and CBIAS, the bypass for FB for fixed voltage devices and BIAS for adjustable devices as close to the LM53600-Q1 and LM53601-Q1 devices as possible.
- The first output the trace from the output inductor to the output node should run by an output capacitor before joining the rest of the output node.
- Keep 10 µF close to the output (output inductor and GND) of the LM53600-Q1 and LM53601-Q1 devices.
- Clear the layer beneath the SW node.

表 11-1. PCB Layout Resources

TITLE	LINK
AN-1149 *Layout Guidelines for Switching Power Supplies*	SNVA021
AN-1229 *Simple Switcher PCB Layout Guidelines*	SNVA054
Constructing Your Power Supply- Layout Considerations	SLUP230
SNVA721 *Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x*	SNVA721

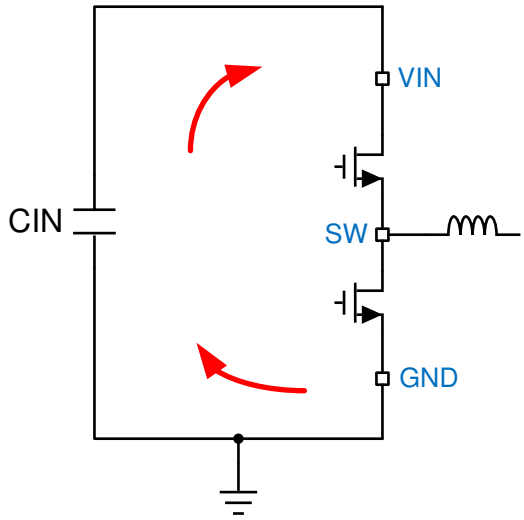

图 11-1. Current Loops with Fast Transients

11.1.1 Ground and Thermal Plane Considerations

As mentioned above, it is recommended to use one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces. It also provides a quiet reference potential for the control circuitry. The AGND and PGND pins should be connected to the ground plane using vias right next to the bypass capacitors. PGND pins are connected to the source of the internal low side MOSFET switch. They should be

connected directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and may bounce due to load variations. The PGND trace, as well as PVIN and SW traces, should be constrained to one side of the ground plane. The other side of the ground plane contains much less noise and should be used for sensitive routes.

It is recommended to provide adequate device heat sinking by utilizing the exposed pad (EP) of the IC as the primary thermal path. Use a minimum 4 by 4 array of 10 mil thermal vias to connect the EP to the system ground plane for heat sinking. The vias should be evenly distributed under the exposed pad. Use as much copper as possible for system ground plane on the top and bottom layers for the best heat dissipation. It is recommended to use a four-layer board with the copper thickness, starting from the top, as: 2 oz / 1 oz / 1 oz / 2 oz. A four-layer board with enough copper thickness and proper layout provides low current conduction impedance, proper shielding and lower thermal resistance.

表 11-2. Resources for Thermal PCB Design

TITLE	LINK
AN-2020 *Thermal Design By Insight, Not Hindsight*	SNVA419
AN-1520 *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages*	SNVA183
SPRA953B *Semiconductor and IC Package Thermal Metrics*	SPRA953
SNVA719 *Thermal Design made Simple with LM43603 and LM43602*	SNVA719
SLMA002 *PowerPAD™ Thermally Enhanced Package*	SLMA002
SLMA004 *PowerPAD Made Easy*	SLMA004
SBVA025 *Using New Thermal Metrics*	SBVA025

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11.2 Layout Example

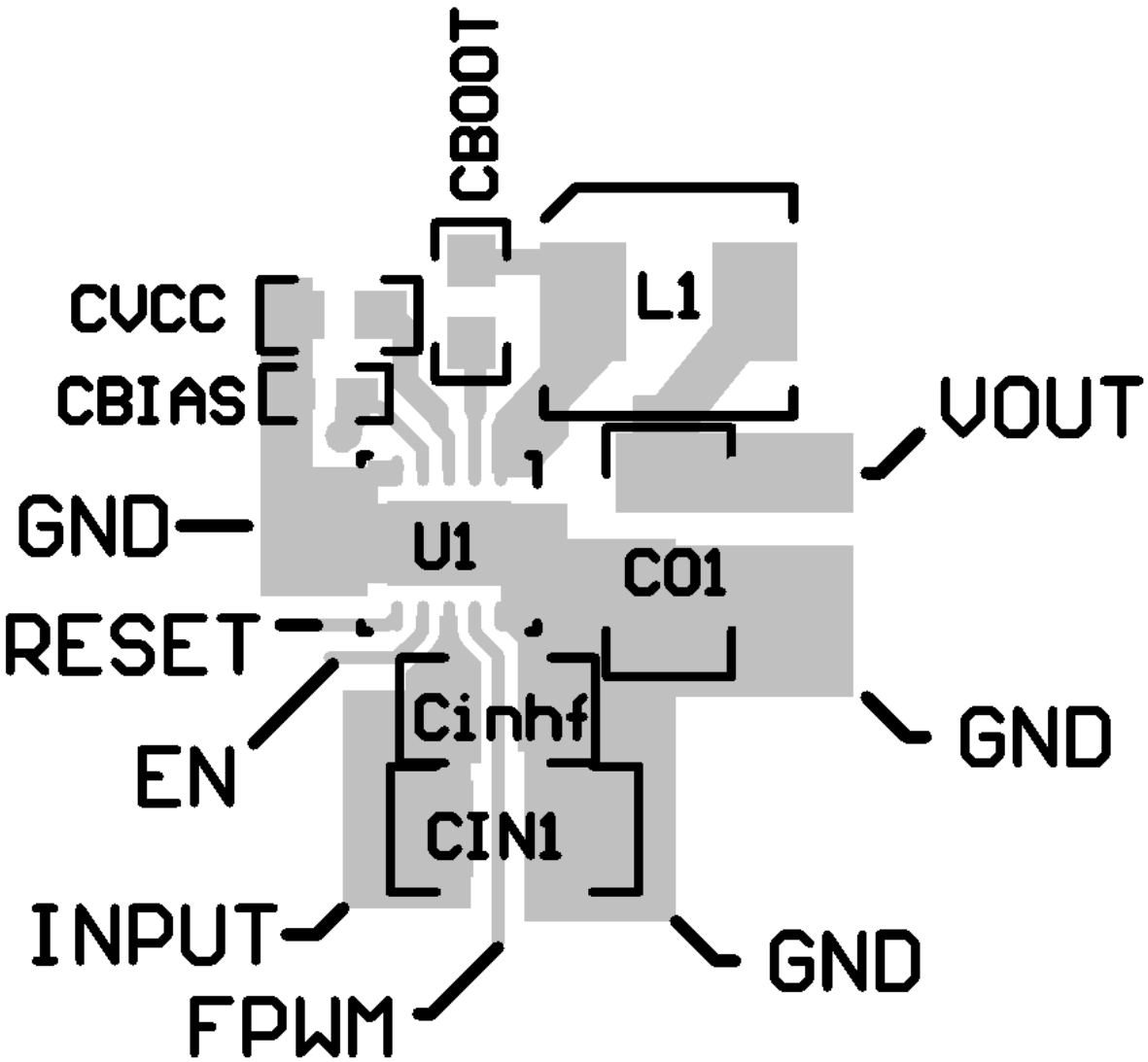

图 11-2. Fixed Output Version

图 11-2 shows an example layout for a fixed output version of the LM53600-Q1 and LM53601-Q1 similar to the one used in the Rev A EVM. Note that the via next to CBIAS connects on the back side of the board to VOUT near CO1. This layout shows 10 µF of output capacitance and 4.7 µF of input capacitance. An additional >10 µF of output capacitance and about 4.7 µF of input capacitance is assumed to be elsewhere in the system. A solid, unbroken ground plane is under this entire circuit except immediately below the SW node.

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation request the following:

AN-1149 *Layout Guidelines for Switching Power Supplies* (SNVA021)

Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x (SNVA721)

Constructing Your Power Supply – Layout Considerations (SLUP230)

AN-1229 *Simple Switcher PCB Layout Guidelines* (SNVA054)

Using New Thermal Metrics (SBVA025)

PowerPAD Made Easy (SLMA004)

PowerPAD™ Thermally Enhanced Package (SLMA002)

Thermal Design made Simple with LM43603 and LM43602 (SNVA719)

Semiconductor and IC Package Thermal Metrics (SPRA953)

AN-2020 *Thermal Design By Insight, Not Hindsight* (SNVA419)

AN-1520 *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages* (SNVA183)

Simple Success with Conducted EMI for DC-DC Converters User's Guide (SNVA489)

EVM User's Guide for Adjustable Versions of the LM53600-Q1 and LM53601-Q1 (SNAU190)

EVM User's Guide for Fixed Versions of the LM53600-Q1 and LM53601-Q1 (SNAU191)

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

PowerPAD™ are trademarks of TI.
TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM536003QDSXRQ1	ACTIVE	WSON	DSX	10	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	53603	Samples
LM536003QDSXTQ1	ACTIVE	WSON	DSX	10	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	53603	Samples
LM536005QDSXRQ1	ACTIVE	WSON	DSX	10	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	53605	Samples
LM536005QDSXTQ1	ACTIVE	WSON	DSX	10	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	53605	Samples
LM53600AQDSXRQ1	ACTIVE	WSON	DSX	10	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	5360A	Samples
LM53600AQDSXTQ1	ACTIVE	WSON	DSX	10	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	5360A	Samples
LM53600LQDSXRQ1	ACTIVE	WSON	DSX	10	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	5360L	Samples
LM53600LQDSXTQ1	ACTIVE	WSON	DSX	10	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	5360L	Samples
LM53600MQDSXRQ1	ACTIVE	WSON	DSX	10	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	5360M	Samples
LM53600MQDSXTQ1	ACTIVE	WSON	DSX	10	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	5360M	Samples
LM53600MQUDSXRQ1	ACTIVE	WSON	DSX	10	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	360MU	Samples
LM53600NQDSXRQ1	ACTIVE	WSON	DSX	10	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	5360N	Samples
LM53600NQDSXTQ1	ACTIVE	WSON	DSX	10	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	5360N	Samples
LM536013QDSXRQ1	ACTIVE	WSON	DSX	10	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	53613	Samples
LM536013QDSXTQ1	ACTIVE	WSON	DSX	10	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	53613	Samples
LM536013QUDSXRQ1	ACTIVE	WSON	DSX	10	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	3613U	Samples
LM536015QDSXRQ1	ACTIVE	WSON	DSX	10	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	53615	Samples
LM536015QDSXTQ1	ACTIVE	WSON	DSX	10	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	53615	Samples
LM536015QUDSXRQ1	ACTIVE	WSON	DSX	10	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	3615U	Samples
LM53601AQDSXRQ1	ACTIVE	WSON	DSX	10	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	5361A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM53601AQDSXTQ1	ACTIVE	WSON	DSX	10	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	5361A	Samples
LM53601LQDSXRQ1	ACTIVE	WSON	DSX	10	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	5361L	Samples
LM53601LQDSXTQ1	ACTIVE	WSON	DSX	10	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	5361L	Samples
LM53601MQDSXRQ1	ACTIVE	WSON	DSX	10	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	5361M	Samples
LM53601MQDSXTQ1	ACTIVE	WSON	DSX	10	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	5361M	Samples
LM53601MQUDSXRQ1	ACTIVE	WSON	DSX	10	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	361MU	Samples
LM53601NQDSXRQ1	ACTIVE	WSON	DSX	10	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	5361N	Samples
LM53601NQDSXTQ1	ACTIVE	WSON	DSX	10	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	5361N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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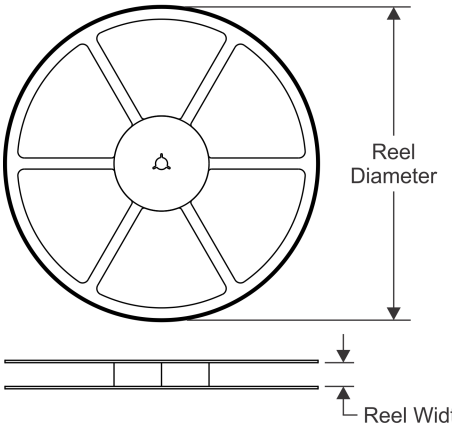
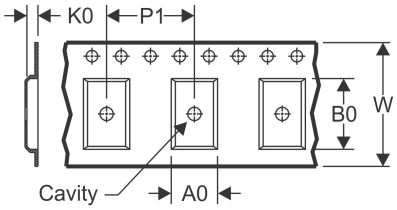
TAPE AND REEL INFORMATION

REEL DIMENSIONS

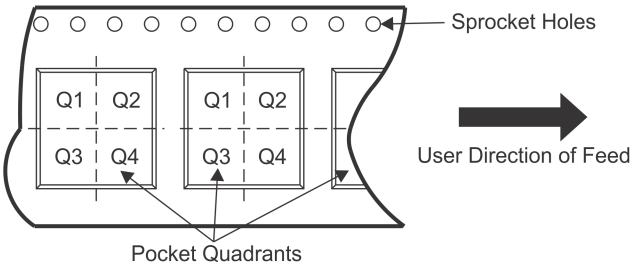


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

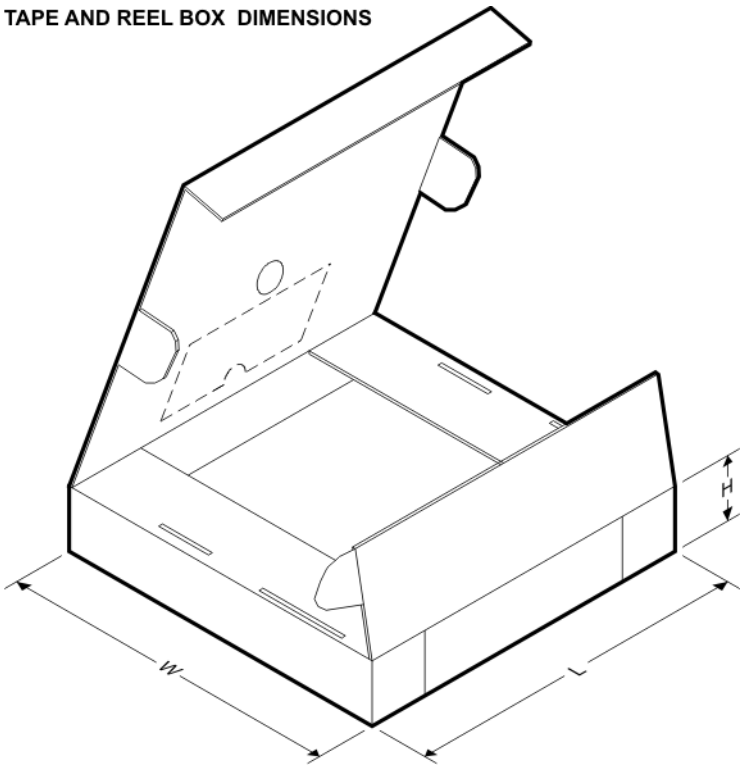


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM536003QDSXTQ1	WSON	DSX	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM536003QDSXTQ1	WSON	DSX	10	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM536005QDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM536005QDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM536005QDSXTQ1	WSON	DSX	10	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM536005QDSXTQ1	WSON	DSX	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM53600AQDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM53600AQDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM53600AQDSXTQ1	WSON	DSX	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM53600AQDSXTQ1	WSON	DSX	10	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM53600LQDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM53600LQDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM53600LQDSXTQ1	WSON	DSX	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM53600LQDSXTQ1	WSON	DSX	10	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM53600MQDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM53600MQDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM53600MQDSXTQ1	WSON	DSX	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM53600MQDSXTQ1	WSON	DSX	10	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM53600MQUDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM53600NQDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM53600NQDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM53600NQDSXTQ1	WSON	DSX	10	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM53600NQDSXTQ1	WSON	DSX	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM536013QDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM536013QDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM536013QDSXTQ1	WSON	DSX	10	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM536013QDSXTQ1	WSON	DSX	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM536013QUDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM536015QDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM536015QDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM536015QDSXTQ1	WSON	DSX	10	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM536015QDSXTQ1	WSON	DSX	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM536015QUDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM53601AQDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM53601AQDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM53601AQDSXTQ1	WSON	DSX	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM53601AQDSXTQ1	WSON	DSX	10	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM53601LQDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM53601LQDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM53601LQDSXTQ1	WSON	DSX	10	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM53601LQDSXTQ1	WSON	DSX	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM53601MQDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM53601MQDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM53601MQDSXTQ1	WSON	DSX	10	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM53601MQDSXTQ1	WSON	DSX	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM53601MQUDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM53601NQDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LM53601NQDSXRQ1	WSON	DSX	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM53601NQDSXTQ1	WSON	DSX	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM53601NQDSXTQ1	WSON	DSX	10	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM536003QDSXTQ1	WSON	DSX	10	250	210.0	185.0	35.0
LM536003QDSXTQ1	WSON	DSX	10	250	213.0	191.0	35.0
LM536005QDSXRQ1	WSON	DSX	10	3000	367.0	367.0	38.0
LM536005QDSXRQ1	WSON	DSX	10	3000	367.0	367.0	35.0
LM536005QDSXTQ1	WSON	DSX	10	250	213.0	191.0	35.0
LM536005QDSXTQ1	WSON	DSX	10	250	210.0	185.0	35.0
LM53600AQDSXRQ1	WSON	DSX	10	3000	367.0	367.0	38.0
LM53600AQDSXRQ1	WSON	DSX	10	3000	367.0	367.0	35.0
LM53600AQDSXTQ1	WSON	DSX	10	250	210.0	185.0	35.0
LM53600AQDSXTQ1	WSON	DSX	10	250	213.0	191.0	35.0
LM53600LQDSXRQ1	WSON	DSX	10	3000	367.0	367.0	35.0
LM53600LQDSXRQ1	WSON	DSX	10	3000	367.0	367.0	38.0
LM53600LQDSXTQ1	WSON	DSX	10	250	210.0	185.0	35.0
LM53600LQDSXTQ1	WSON	DSX	10	250	213.0	191.0	35.0
LM53600MQDSXRQ1	WSON	DSX	10	3000	367.0	367.0	35.0
LM53600MQDSXRQ1	WSON	DSX	10	3000	367.0	367.0	38.0
LM53600MQDSXTQ1	WSON	DSX	10	250	210.0	185.0	35.0
LM53600MQDSXTQ1	WSON	DSX	10	250	213.0	191.0	35.0
LM53600MQUDSXRQ1	WSON	DSX	10	3000	367.0	367.0	38.0
LM53600NQDSXRQ1	WSON	DSX	10	3000	367.0	367.0	38.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM53600NQDSXRQ1	WSON	DSX	10	3000	367.0	367.0	35.0
LM53600NQDSXTQ1	WSON	DSX	10	250	213.0	191.0	35.0
LM53600NQDSXTQ1	WSON	DSX	10	250	210.0	185.0	35.0
LM536013QDSXRQ1	WSON	DSX	10	3000	367.0	367.0	35.0
LM536013QDSXRQ1	WSON	DSX	10	3000	367.0	367.0	38.0
LM536013QDSXTQ1	WSON	DSX	10	250	213.0	191.0	35.0
LM536013QDSXTQ1	WSON	DSX	10	250	210.0	185.0	35.0
LM536013QUDSXRQ1	WSON	DSX	10	3000	367.0	367.0	38.0
LM536015QDSXRQ1	WSON	DSX	10	3000	367.0	367.0	35.0
LM536015QDSXRQ1	WSON	DSX	10	3000	367.0	367.0	38.0
LM536015QDSXTQ1	WSON	DSX	10	250	213.0	191.0	35.0
LM536015QDSXTQ1	WSON	DSX	10	250	210.0	185.0	35.0
LM536015QUDSXRQ1	WSON	DSX	10	3000	367.0	367.0	38.0
LM53601AQDSXRQ1	WSON	DSX	10	3000	367.0	367.0	35.0
LM53601AQDSXRQ1	WSON	DSX	10	3000	367.0	367.0	38.0
LM53601AQDSXTQ1	WSON	DSX	10	250	210.0	185.0	35.0
LM53601AQDSXTQ1	WSON	DSX	10	250	213.0	191.0	35.0
LM53601LQDSXRQ1	WSON	DSX	10	3000	367.0	367.0	35.0
LM53601LQDSXRQ1	WSON	DSX	10	3000	367.0	367.0	38.0
LM53601LQDSXTQ1	WSON	DSX	10	250	213.0	191.0	35.0
LM53601LQDSXTQ1	WSON	DSX	10	250	210.0	185.0	35.0
LM53601MQDSXRQ1	WSON	DSX	10	3000	367.0	367.0	38.0
LM53601MQDSXRQ1	WSON	DSX	10	3000	367.0	367.0	35.0
LM53601MQDSXTQ1	WSON	DSX	10	250	213.0	191.0	35.0
LM53601MQDSXTQ1	WSON	DSX	10	250	210.0	185.0	35.0
LM53601MQUDSXRQ1	WSON	DSX	10	3000	367.0	367.0	38.0
LM53601NQDSXRQ1	WSON	DSX	10	3000	367.0	367.0	38.0
LM53601NQDSXRQ1	WSON	DSX	10	3000	367.0	367.0	35.0
LM53601NQDSXTQ1	WSON	DSX	10	250	210.0	185.0	35.0
LM53601NQDSXTQ1	WSON	DSX	10	250	213.0	191.0	35.0

GENERIC PACKAGE VIEW

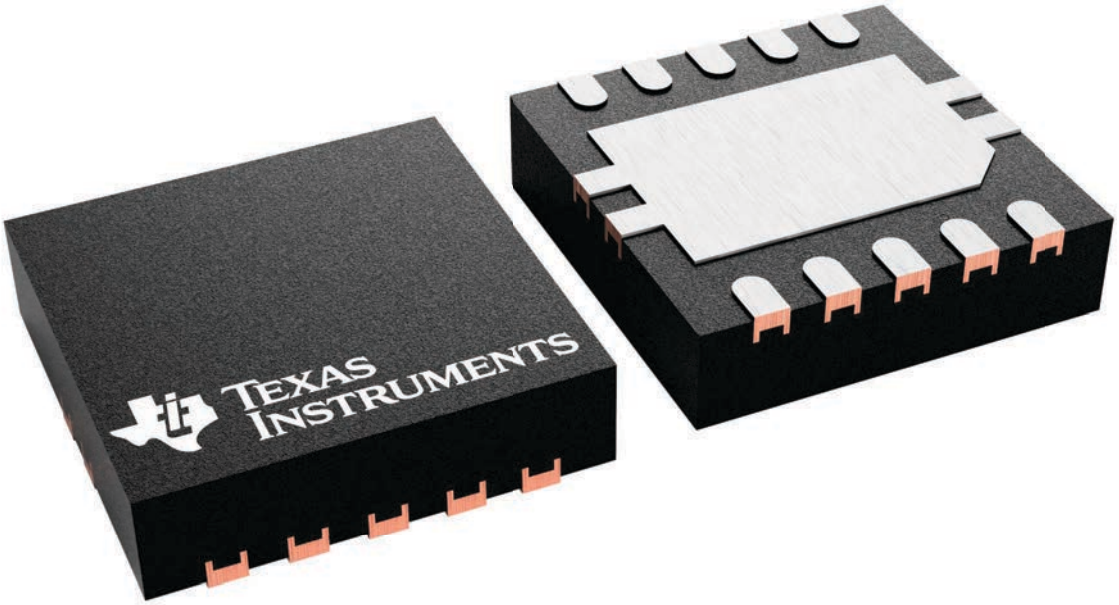
DSX 10

WSON - 0.8 mm max height

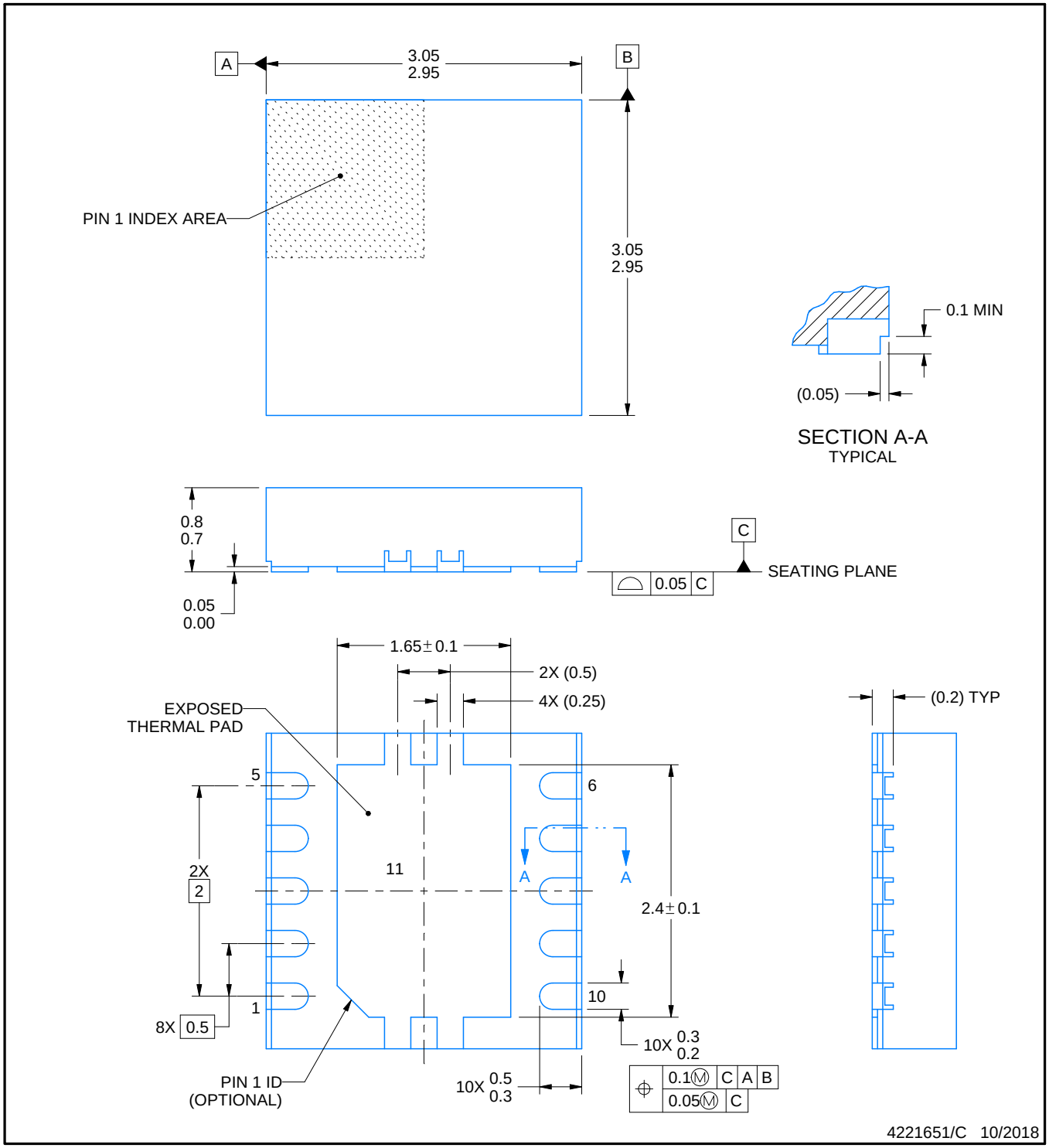
3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

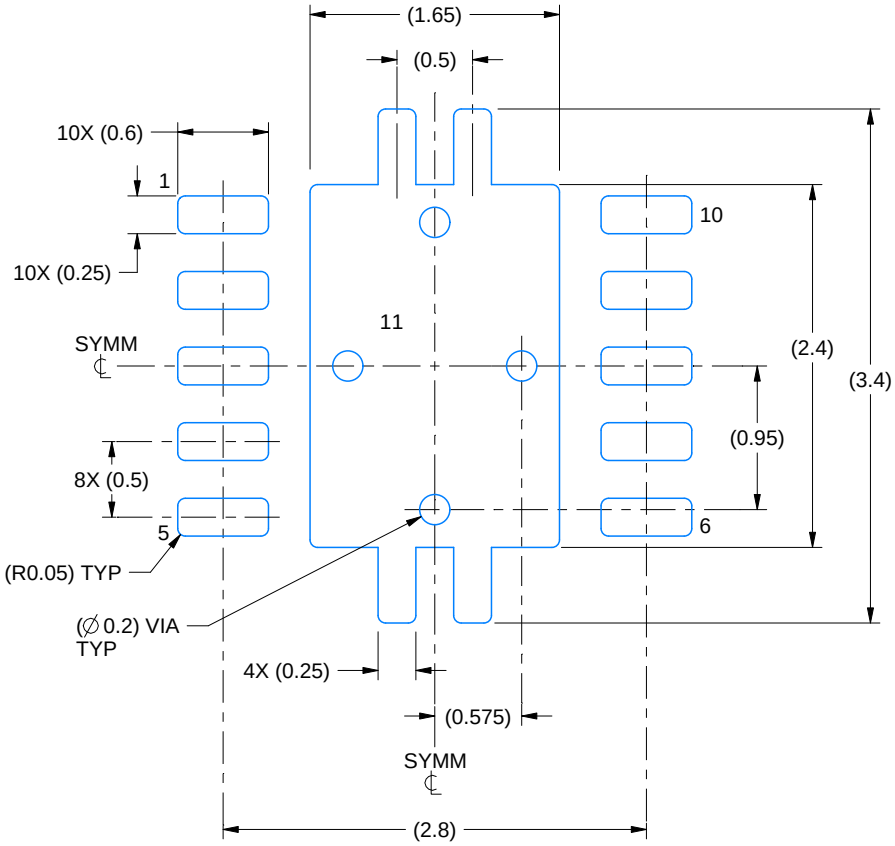


4226665/A

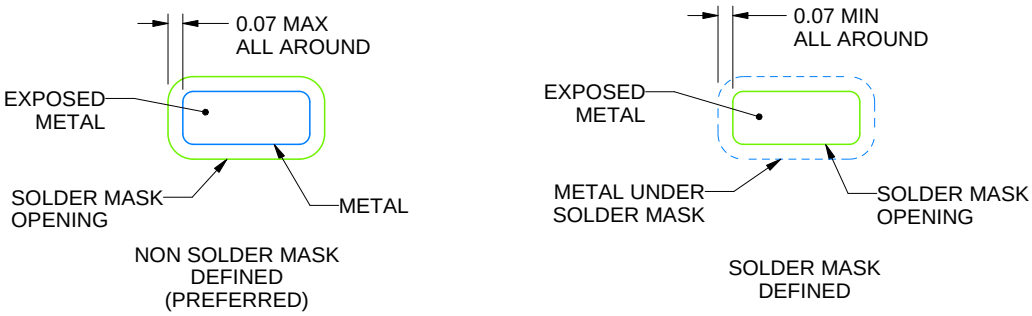


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

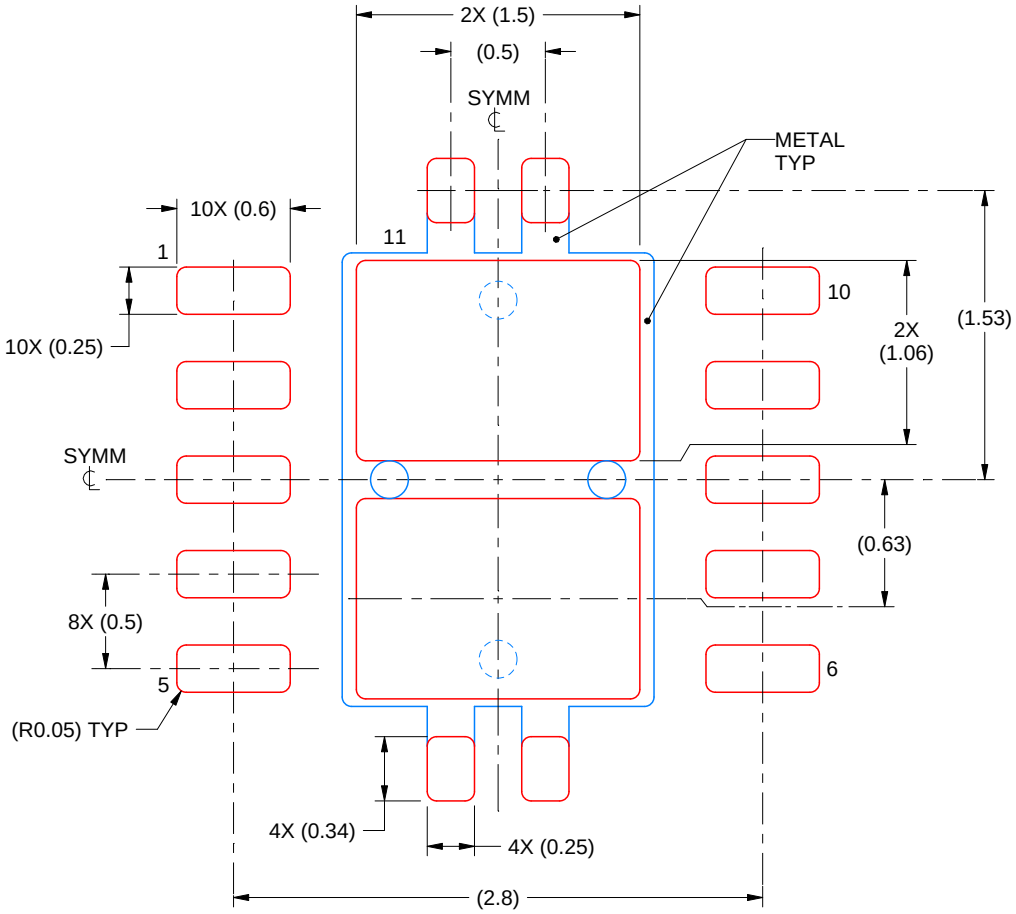


SOLDER MASK DETAILS

4221651/C 10/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



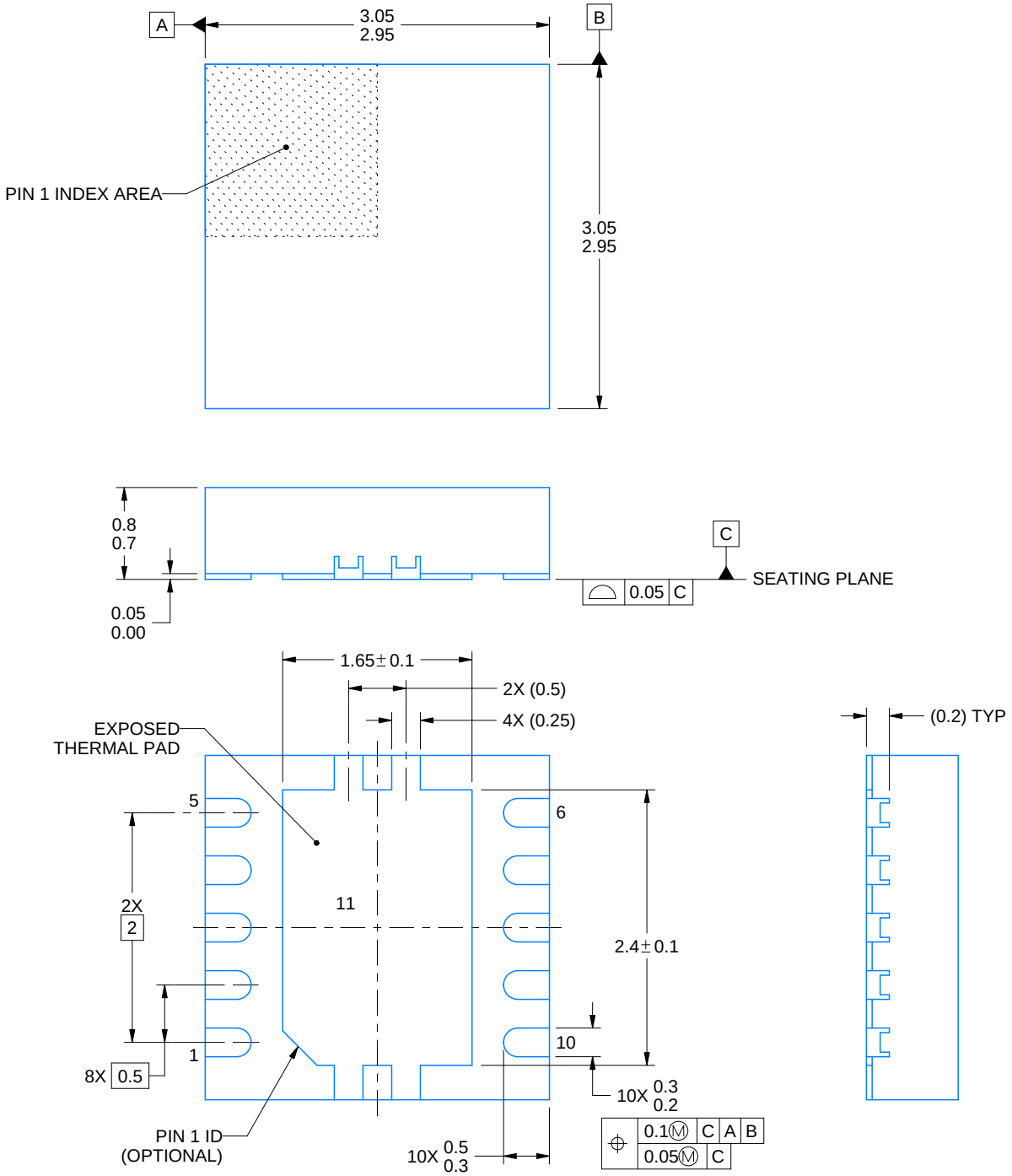
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4221651/C 10/2018

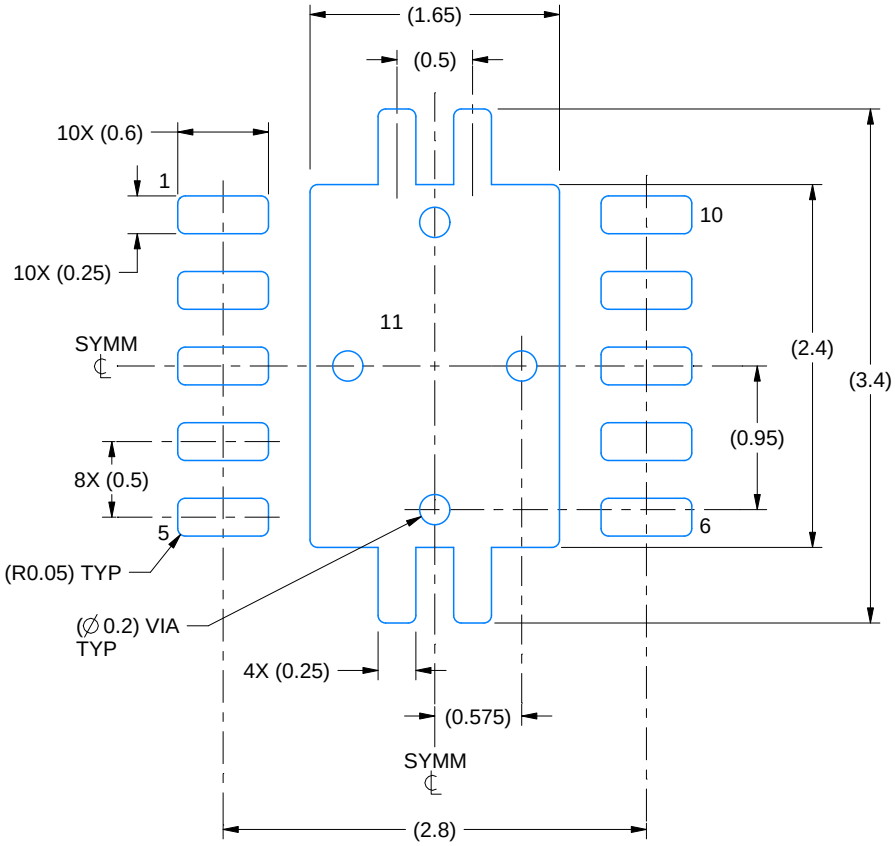
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

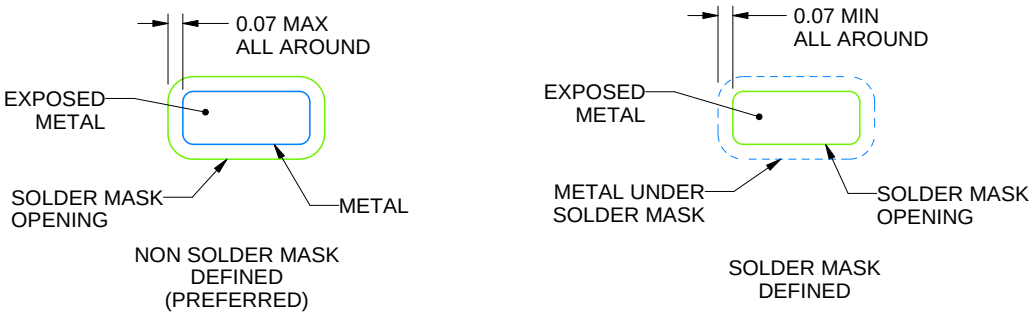


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

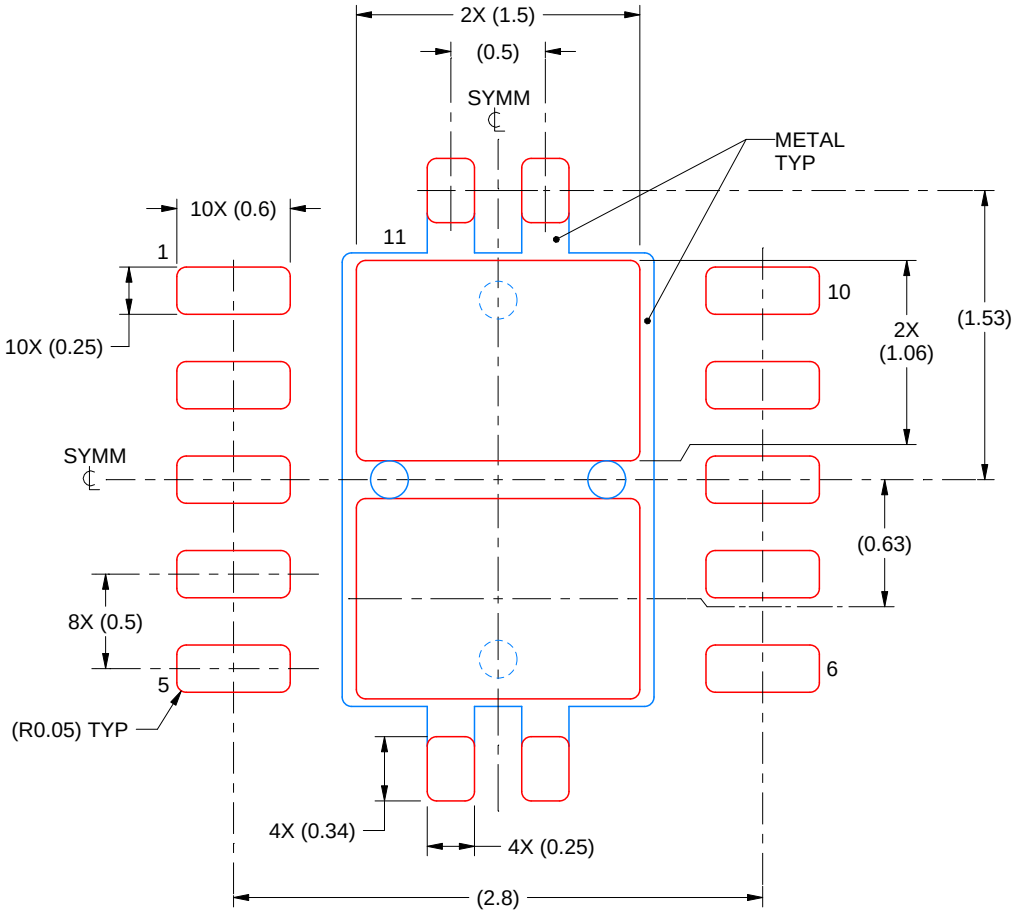


SOLDER MASK DETAILS

4226664/A 03/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



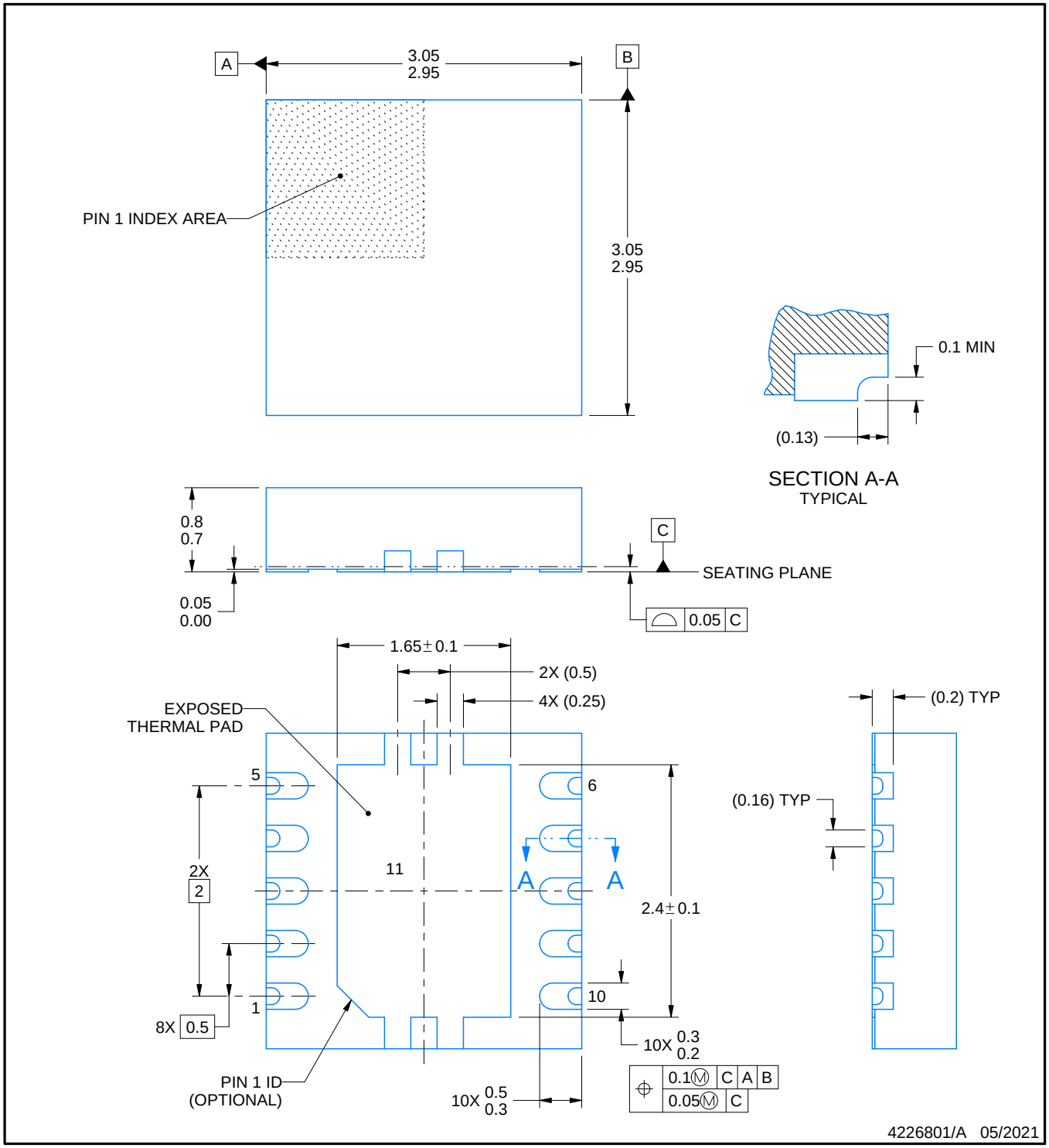
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4226664/A 03/2021

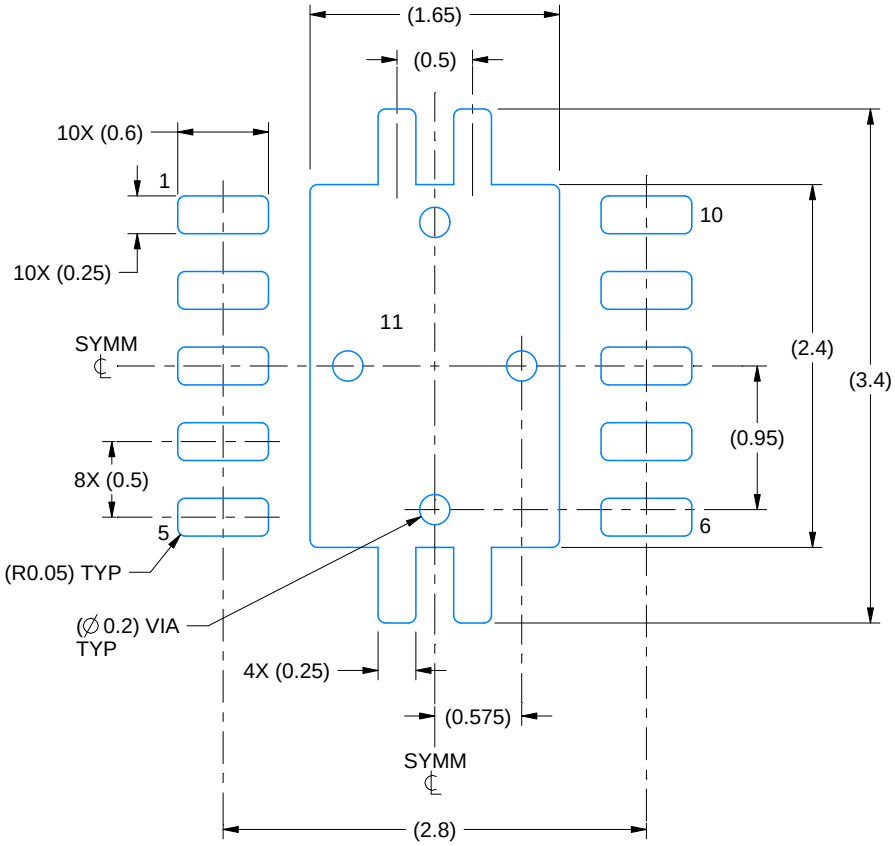
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

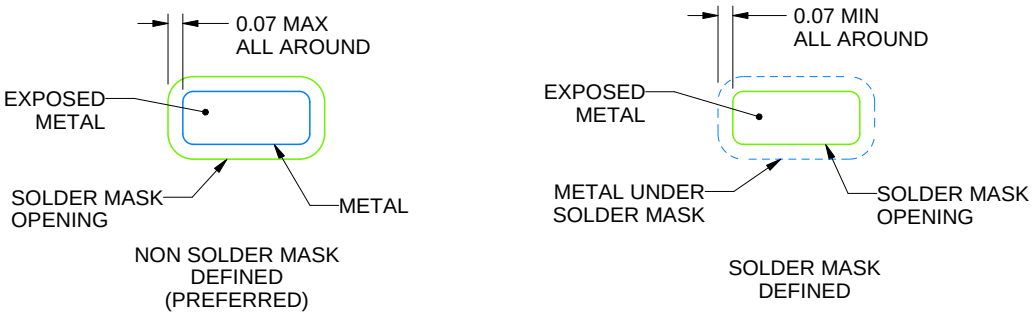


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

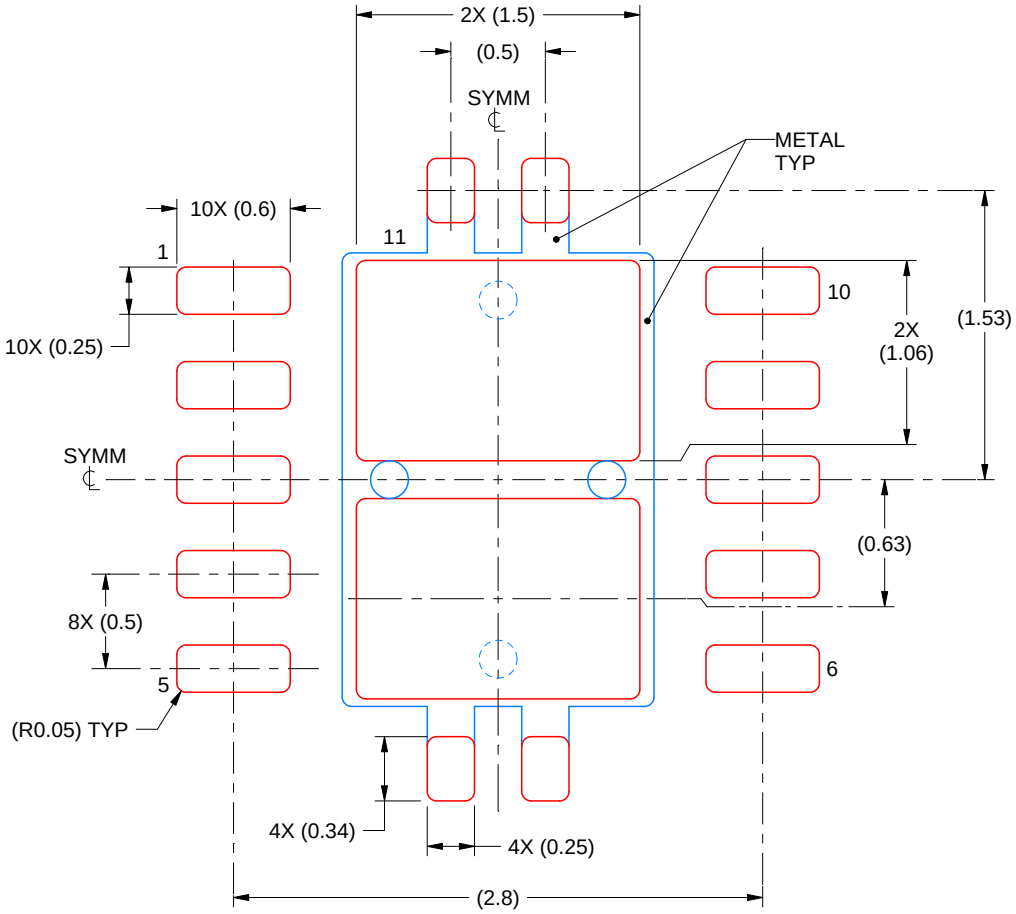


SOLDER MASK DETAILS

4226801/A 05/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4226801/A 05/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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