

INA141

Precision, Low Power, G = 10, 100 INSTRUMENTATION AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: $50\mu\text{V}$ max
- LOW DRIFT: $0.5\mu\text{V}/^\circ\text{C}$ max
- ACCURATE GAIN: $\pm 0.05\%$ at $G = 10$
- LOW INPUT BIAS CURRENT: 5nA max
- HIGH CMR: 117dB min
- INPUTS PROTECTED TO $\pm 40\text{V}$
- WIDE SUPPLY RANGE: ± 2.25 to $\pm 18\text{V}$
- LOW QUIESCENT CURRENT: $750\mu\text{A}$
- 8-PIN PLASTIC DIP, SO-8

APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

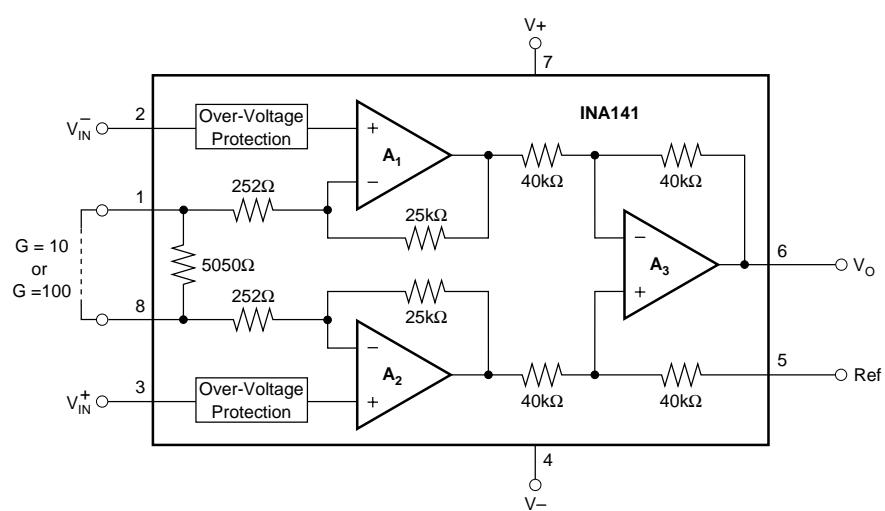
DESCRIPTION

The INA141 is a low power, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (200kHz at $G = 100$).

Simple pin connections set an accurate gain of 10 or 100V/V without external resistors. Internal input protection can withstand up to $\pm 40V$ without damage.

The INA141 is laser trimmed for very low offset voltage (50 μ V), drift (0.5 μ V/ $^{\circ}$ C) and high common-mode rejection (117dB at G = 100). It operates with power supplies as low as \pm 2.25V, and quiescent current is only 750 μ A—ideal for battery operated systems.

The INA141 is available in 8-pin plastic DIP, and SO-8 surface-mount packages, specified for the -40°C to $+85^{\circ}\text{C}$ temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: <http://www.burr-brown.com> • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, and $R_L = 10\text{k}\Omega$, unless otherwise noted.

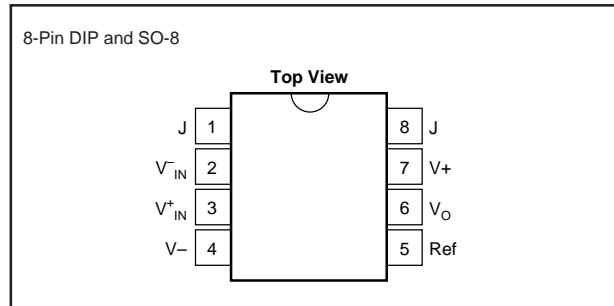
PARAMETER	CONDITIONS	INA141P, U			INA141PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Offset Voltage, RTI	$G = 100$		± 20	± 50		*	± 125	μV
vs Temperature	$G = 10$		± 50	± 100		*	± 250	μV
	$G = 100$		± 0.2	± 0.5		*	± 1.5	$\mu\text{V}/^\circ\text{C}$
vs Power Supply	$G = 10^{(2)}$		± 0.5	± 2		*	± 2.5	$\mu\text{V}/^\circ\text{C}$
	$V_S = \pm 2.25 \text{ to } \pm 18\text{V}$, $G = 100$		± 0.4	± 1		*	± 3	$\mu\text{V}/\text{V}$
Long-Term Stability	$G = 10$		± 2	± 10		*	± 20	$\mu\text{V}/\text{V}$
	$G = 100$		0.2			*		$\mu\text{V}/\text{mo}$
	$G = 10$		0.5			*		$\mu\text{V}/\text{mo}$
Impedance, Differential			$10^{10} \parallel 2$			*		$\Omega \parallel \text{pF}$
Common-Mode			$10^{10} \parallel 9$			*		$\Omega \parallel \text{pF}$
Common-Mode Voltage Range ⁽¹⁾	$V_O = 0\text{V}$	$(V+) - 2$ $(V-) + 2$	$(V+) - 1.4$ $(V-) + 1.7$		*	*		V
Safe Input Voltage				± 40			*	V
Common-Mode Rejection	$V_{CM} = \pm 13\text{V}$, $\Delta R_S = 1\text{k}\Omega$	117 100	125 106		110 93	120 100		dB
$G = 100$								dB
BIAS CURRENT								
vs Temperature			± 2	± 5		*	± 10	nA
Offset Current			± 30			*	± 10	$\text{pA}/^\circ\text{C}$
vs Temperature			± 1	± 5		*		nA
			± 30			*		$\text{pA}/^\circ\text{C}$
NOISE VOLTAGE, RTI								
$f = 10\text{Hz}$	$G = 100$, $R_S = 0\Omega$		10			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 100\text{Hz}$			8			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 1\text{kHz}$			8			*		$\text{nV}/\sqrt{\text{Hz}}$
$f_B = 0.1\text{Hz to } 10\text{Hz}$	$G = 10$, $R_S = 0\Omega$		0.2			*		$\mu\text{V}/\text{p-p}$
$f = 10\text{Hz}$			22			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 100\text{Hz}$			13			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 1\text{kHz}$			12			*		$\text{nV}/\sqrt{\text{Hz}}$
$f_B = 0.1\text{Hz to } 10\text{Hz}$			0.6			*		$\mu\text{V}/\text{p-p}$
Noise Current								
$f = 10\text{Hz}$			0.9			*		$\text{pA}/\sqrt{\text{Hz}}$
$f = 1\text{kHz}$			0.3			*		$\text{pA}/\sqrt{\text{Hz}}$
$f_B = 0.1\text{Hz to } 10\text{Hz}$			30			*		pAp-p
GAIN								
Gain Error	$V_O = \pm 13.6\text{V}$, $G = 100$		± 0.03	± 0.075		*	± 0.15	$\%$
Gain vs Temperature ⁽²⁾	$G = 10$		± 0.01	± 0.05		*	± 0.15	$\%$
Nonlinearity	$G = 10, 100$		± 2	± 10		*	*	$\text{ppm}/^\circ\text{C}$
	$G = 100$		± 0.0005	± 0.002		*	± 0.004	$\%$ of FSR
	$G = 10$		± 0.0003	± 0.001		*	± 0.002	$\%$ of FSR
OUTPUT								
Voltage: Positive	$R_L = 10\text{k}\Omega$	$(V+) - 1.4$	$(V+) - 0.9$			*		V
Negative	$R_L = 10\text{k}\Omega$	$(V-) + 1.4$	$(V-) + 0.9$			*		V
Load Capacitance Stability			1000			*		pF
Short-Circuit Current			+6/-15			*		mA
FREQUENCY RESPONSE								
Bandwidth, -3dB	$G = 100$		200			*		kHz
	$G = 10$		1			*		MHz
Slew Rate	$V_O = \pm 10\text{V}$, $G = 10$		4			*		$\text{V}/\mu\text{s}$
Settling Time, 0.01%	$V_O = \pm 5\text{V}$, $G = 100$		9			*		μs
Overload Recovery	$G = 10$	50% Overdrive	7			*		μs
			4			*		μs
POWER SUPPLY								
Voltage Range	$V_{IN} = 0\text{V}$	± 2.25	± 15	± 18	*	*	*	V
Current, Total			± 750	± 800		*	*	μA
TEMPERATURE RANGE								
Specification								
Operating								
θ_{JA}	8-Pin DIP	-40		85	*	*	*	$^\circ\text{C}$
	SO-8 SOIC	-40		125	*		*	$^\circ\text{C}$
			80			*		$^\circ\text{C}/\text{W}$
			150			*		$^\circ\text{C}/\text{W}$

* Specification same as INA141P, U.

NOTE: (1) Input common-mode range varies with output voltage—see typical curves. (2) Guaranteed by wafer test.

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PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$\pm 18V$
Analog Input Voltage Range	$\pm 40V$
Output Short-Circuit (to ground)	Continuous
Operating Temperature	$-40^{\circ}C$ to $+125^{\circ}C$
Storage Temperature	$-40^{\circ}C$ to $+125^{\circ}C$
Junction Temperature	$+150^{\circ}C$
Lead Temperature (soldering, 10s)	$+300^{\circ}C$

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

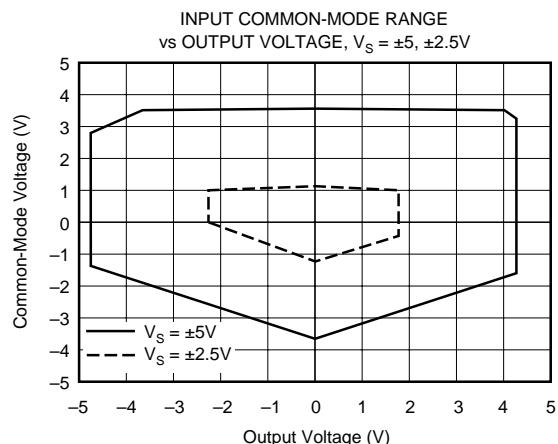
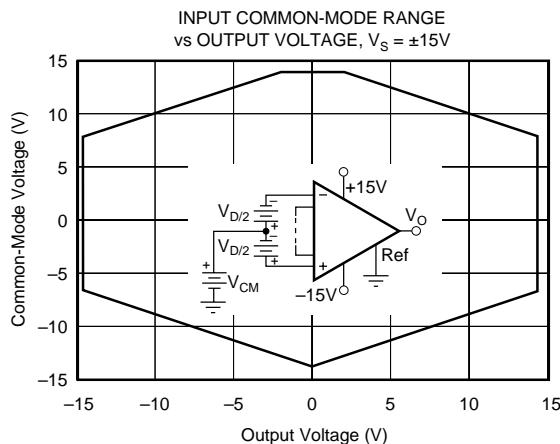
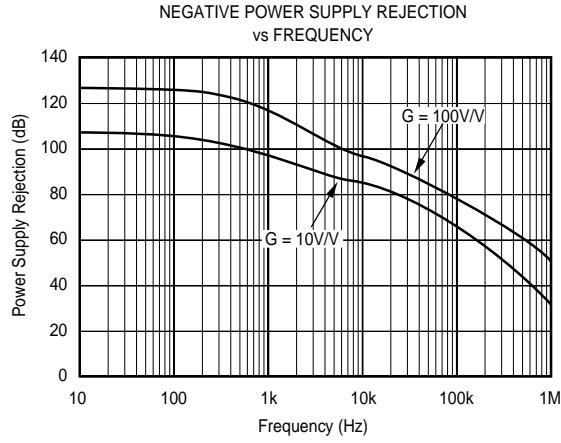
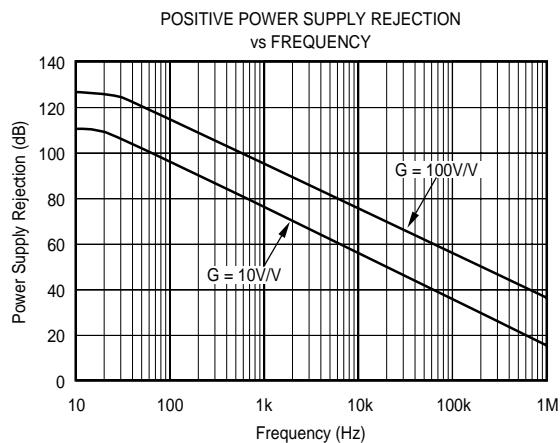
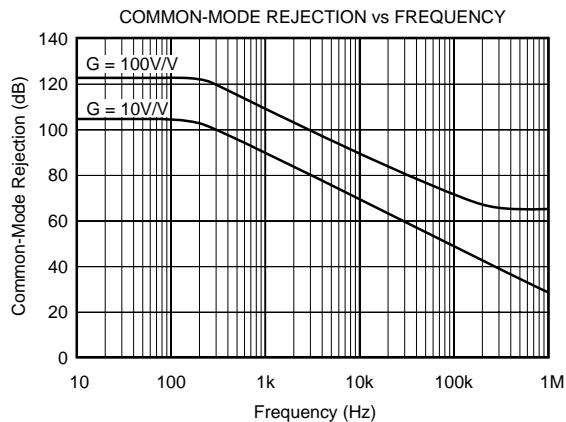
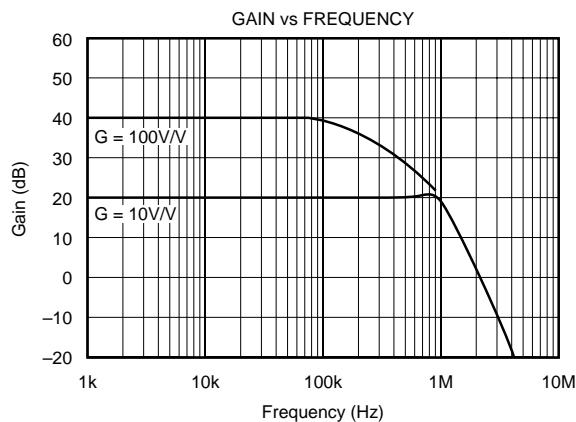
ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	TEMPERATURE RANGE
INA141PA	8-Pin Plastic DIP	006	$-40^{\circ}C$ to $+85^{\circ}C$
INA141P	8-Pin Plastic DIP	006	$-40^{\circ}C$ to $+85^{\circ}C$
INA141UA	SO-8 Surface-Mount	182	$-40^{\circ}C$ to $+85^{\circ}C$
INA141U	SO-8 Surface-Mount	182	$-40^{\circ}C$ to $+85^{\circ}C$

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

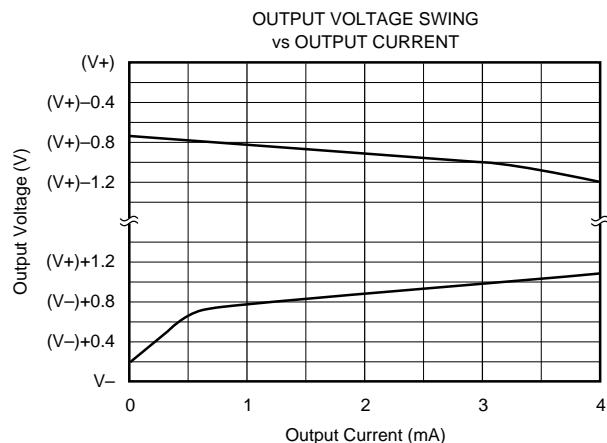
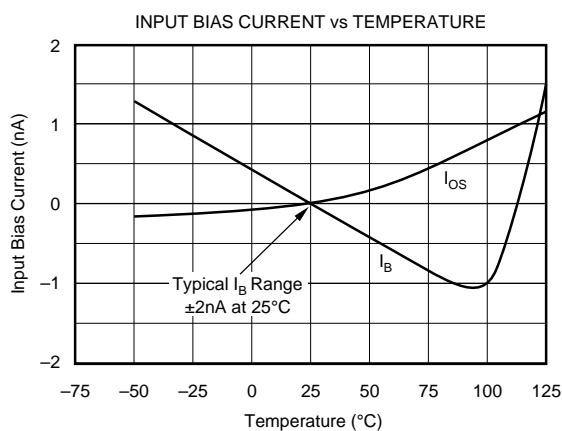
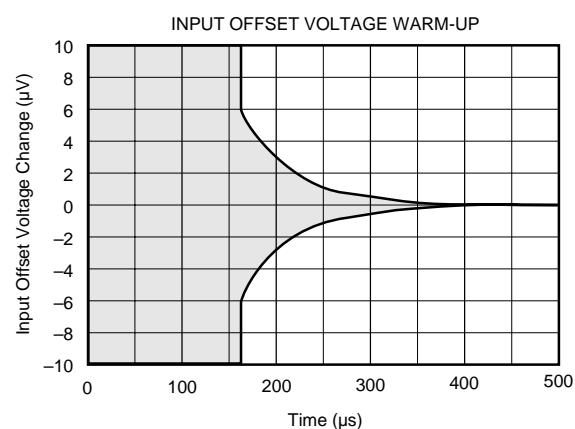
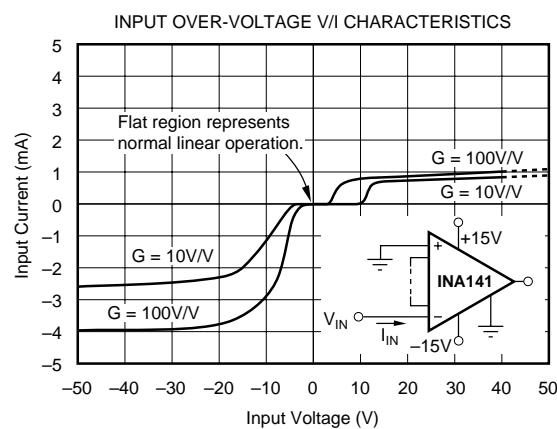
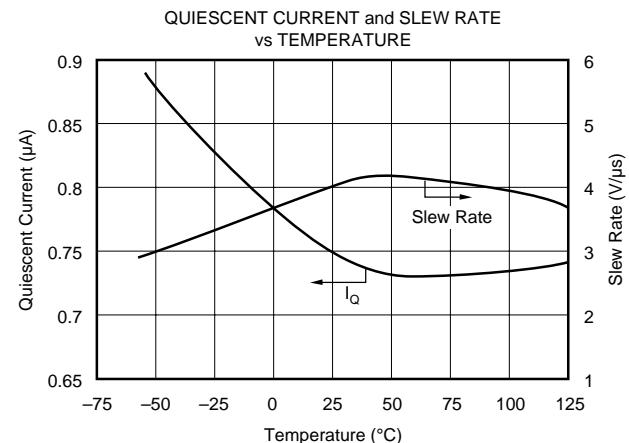
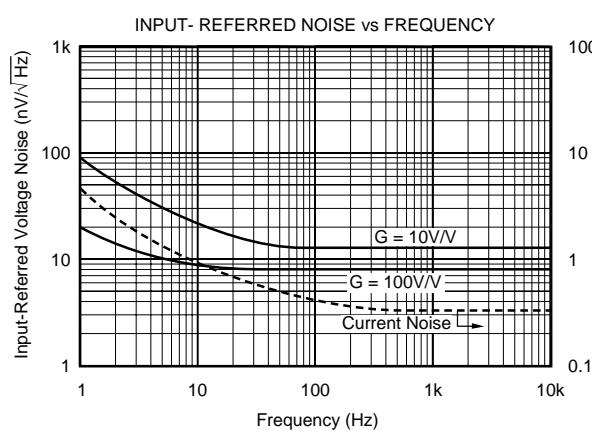
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$ and $V_S = \pm 15\text{V}$, unless otherwise noted.



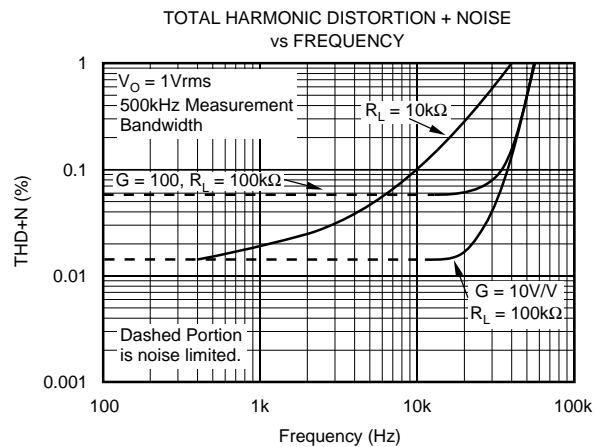
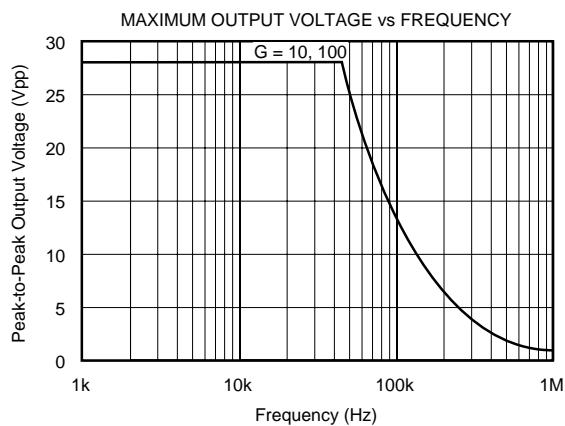
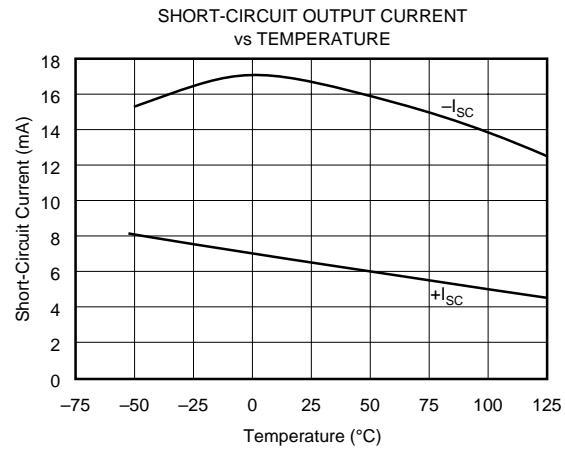
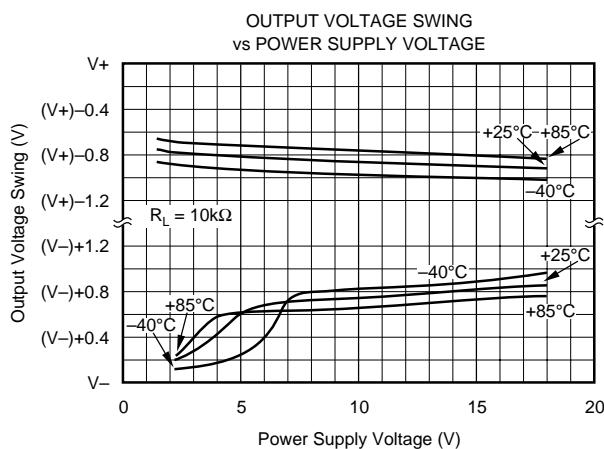
TYPICAL PERFORMANCE CURVES (CONT)

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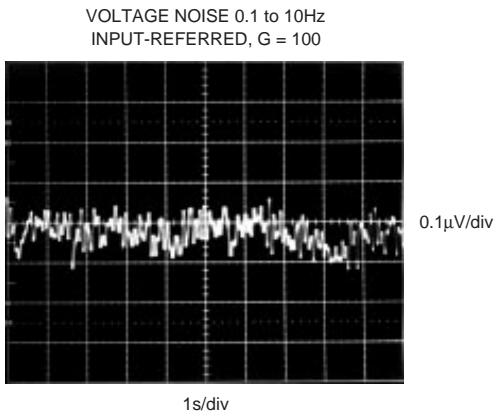
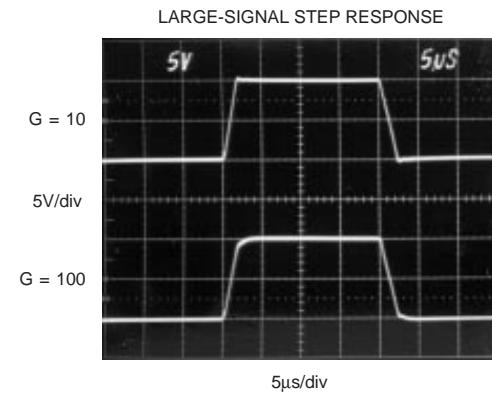
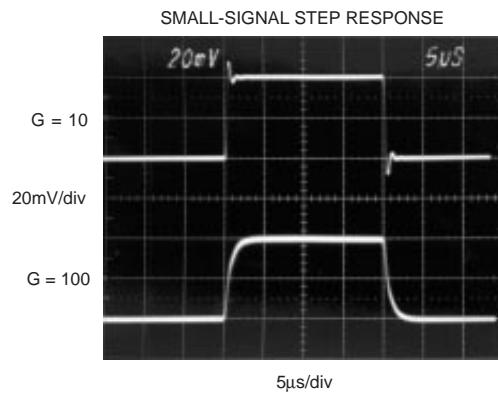
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$ and $V_S = \pm 15\text{V}$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$ and $V_S = \pm 15\text{V}$, unless otherwise noted.



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA141. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 8Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR ($G = 1$).

SETTING THE GAIN

Gain is selected with a jumper connection as shown in Figure 1. $G = 10\text{V/V}$ with no jumper installed. With a jumper installed, $G = 100\text{V/V}$. To preserve good gain accuracy, this jumper must have low series resistance. A resistance of 0.5Ω in series with the jumper will decrease the gain by 0.1%.

Internal resistor ratios are laser trimmed to assure excellent gain accuracy. Actual resistor values can vary by approximately $\pm 25\%$ from the nominal values shown.

Gains between 10 and 100 can be achieved by connecting an external resistor to the jumper pins. This is not recommended, however, because the $\pm 25\%$ variation of internal resistor values makes the required external resistor value uncertain. A companion model, INA128, features accurately trimmed internal resistors so that gains from 1 to 10,000 can be set with an external resistor.

DYNAMIC PERFORMANCE

The typical performance curve “Gain vs Frequency” shows that, despite its low quiescent current, the INA141 achieves wide bandwidth, even at $G = 100$. This is due to the current-feedback topology of the INA141. Settling time also remains excellent at $G = 100$.

NOISE PERFORMANCE

The INA141 provides very low noise in most applications. Low frequency noise is approximately $0.2\mu\text{Vp-p}$ measured from 0.1 to 10Hz ($G = 100$). This provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.

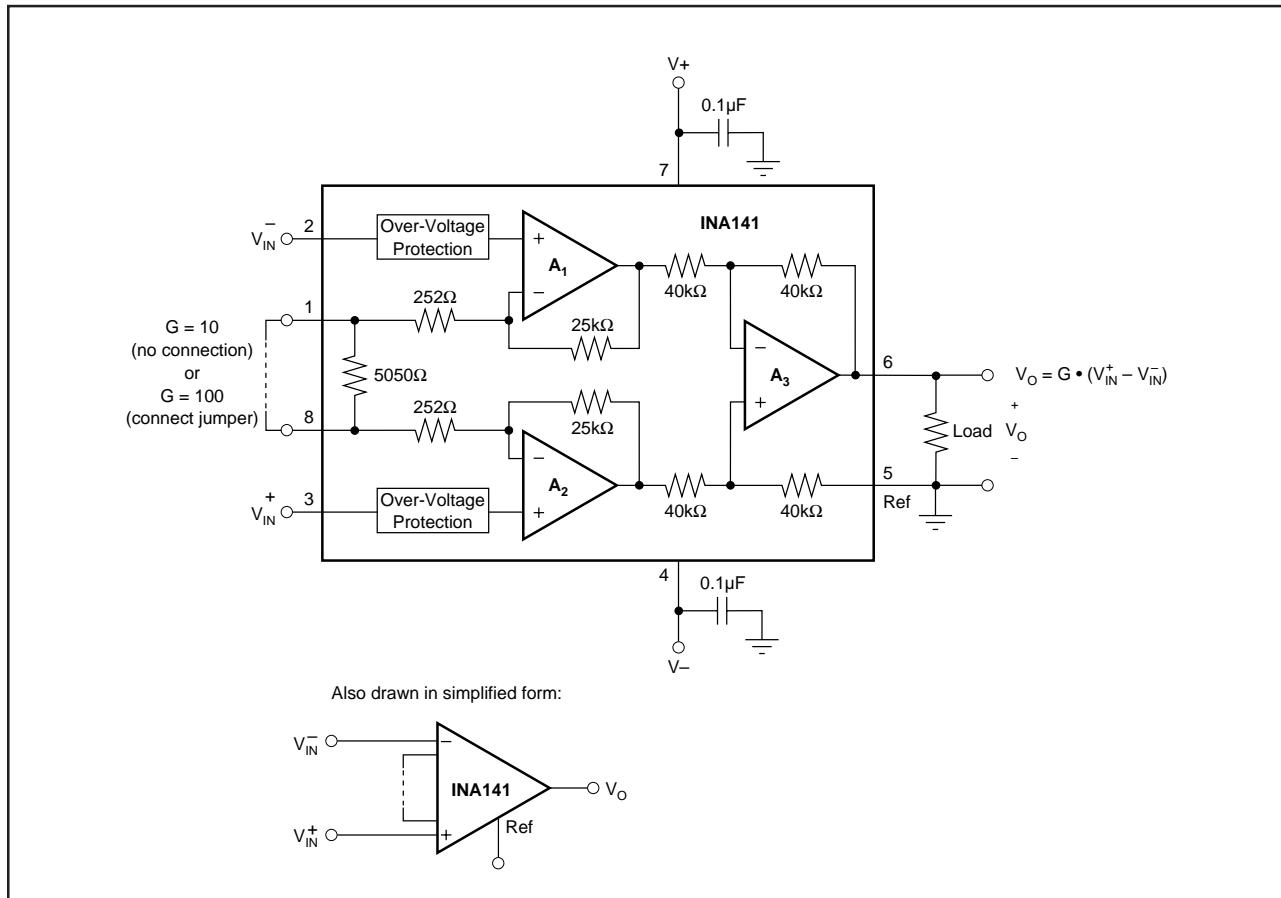


FIGURE 1. Basic Connections.

OFFSET TRIMMING

The INA141 is laser trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed with the output. The op amp buffer provides low impedance at the Ref terminal to preserve good common-mode rejection.

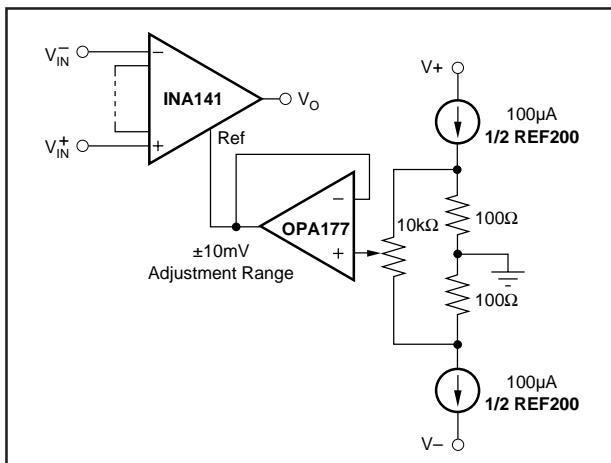


FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA141 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately $\pm 2\text{nA}$. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 3 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range of the INA141 and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

INPUT COMMON-MODE RANGE

The linear input voltage range of the input circuitry of the INA141 is from approximately 1.4V below the positive supply voltage to 1.7V above the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range will be limited by the output voltage swing of amplifiers A_1 and A_2 . So the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see performance curves “Input Common-Mode Range vs Output Voltage”.

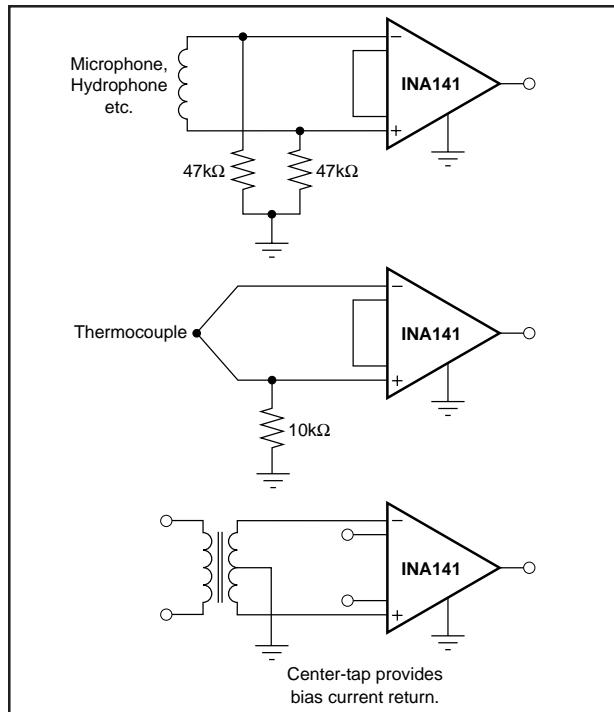


FIGURE 3. Providing an Input Common-Mode Current Path.

Input overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA141 will be near 0V even though both inputs are overloaded.

LOW VOLTAGE OPERATION

The INA141 can be operated on power supplies as low as $\pm 2.25V$. Performance remains excellent with power supplies ranging from $\pm 2.25V$ to $\pm 18V$. Most parameters vary only slightly through this supply voltage range—see Typical Performance Curves. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. Typical performance curves, “Input Common-Mode Range vs Output Voltage” show the range of linear operation for $\pm 15V$, ± 5 , and $\pm 2.5V$ supplies.

INPUT PROTECTION

The inputs of the INA141 are individually protected for voltages up to $\pm 40V$. For example, a condition of $-40V$ on one input and $+40V$ on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 1.5 to 5mA. The typical performance curve "Input Bias Current vs Common-Mode Input Voltage" shows this input current limit behavior. The inputs are protected even if the power supplies are disconnected or turned off.

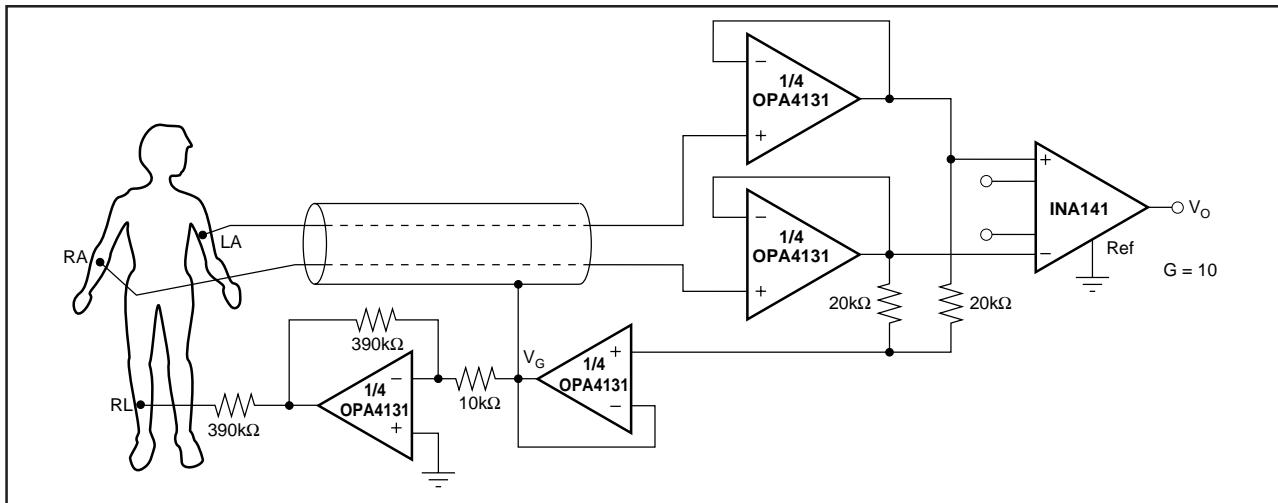


FIGURE 4. ECG Amplifier With Right-Leg Drive.

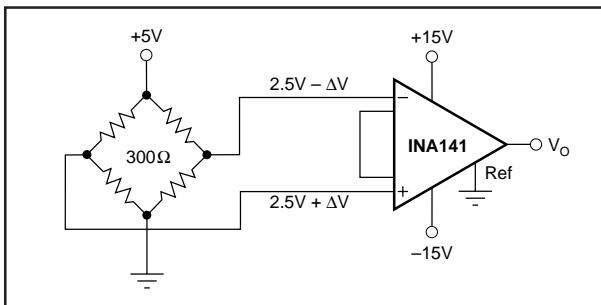


FIGURE 5. Bridge Amplifier.

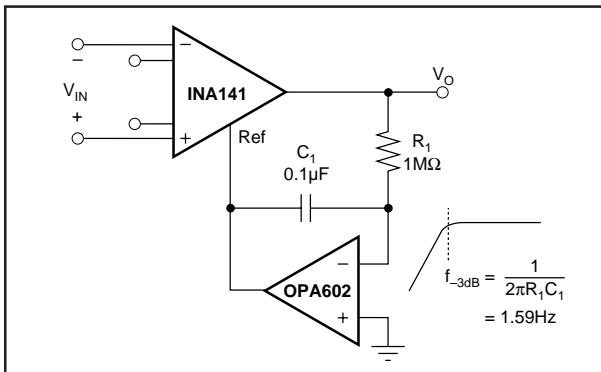


FIGURE 6. AC-Coupled Instrumentation Amplifier.

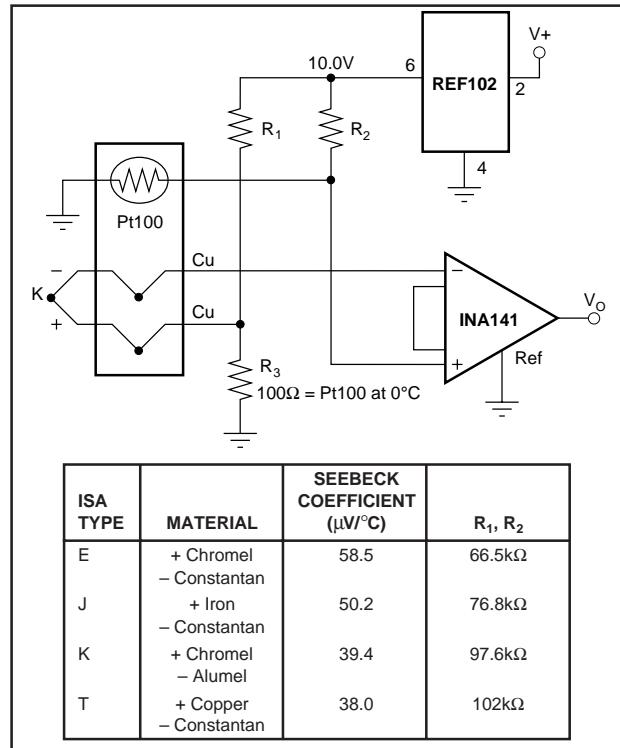


FIGURE 7. Thermocouple Amplifier With RTD Cold-Junction Compensation.

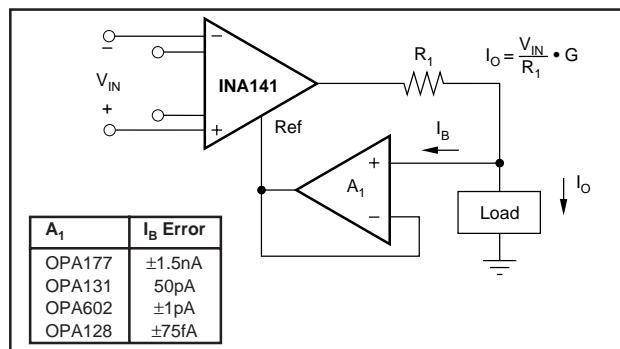


FIGURE 8. Differential Voltage to Current Converter.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA141U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 141U	Samples
INA141U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 141U	Samples
INA141U/2K5E4	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 141U	Samples
INA141UA	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	INA 141U A	Samples
INA141UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	INA 141U A	Samples
INA141UA/2K5E4	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	INA 141U A	Samples
INA141UAE4	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	INA 141U A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

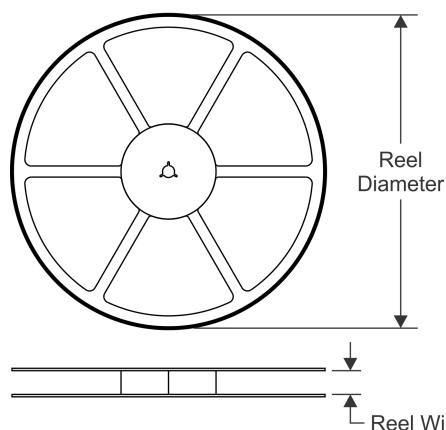
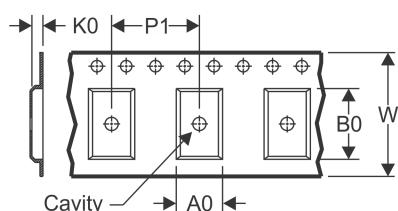
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

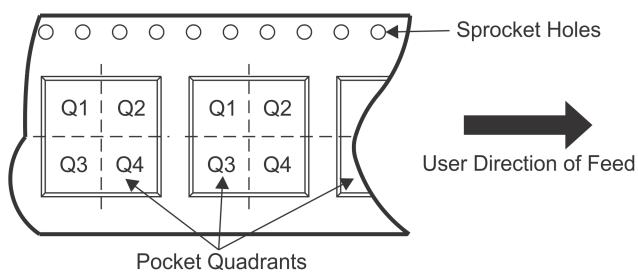
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


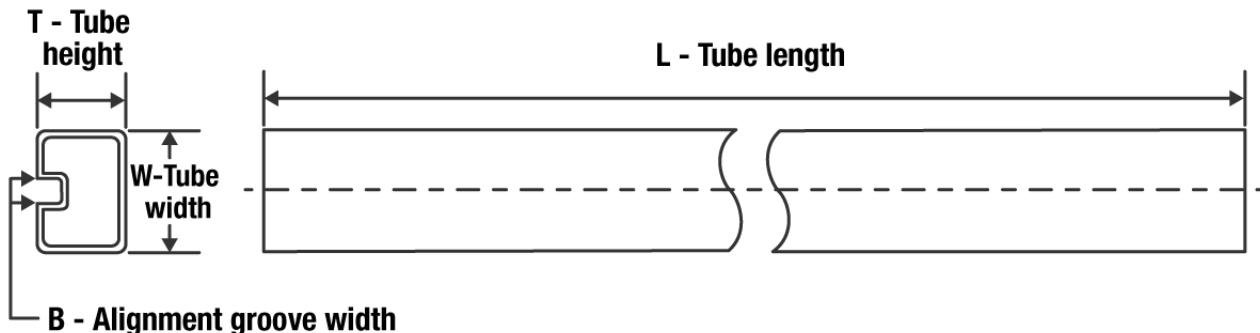
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA141U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA141UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA141U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
INA141UA/2K5	SOIC	D	8	2500	853.0	449.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA141U	D	SOIC	8	75	506.6	8	3940	4.32
INA141UA	D	SOIC	8	75	506.6	8	3940	4.32
INA141UAE4	D	SOIC	8	75	506.6	8	3940	4.32

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