Programmable Gamma-Voltage Generator and V_{COM} Calibrator with Integrated Two-Bank Memory

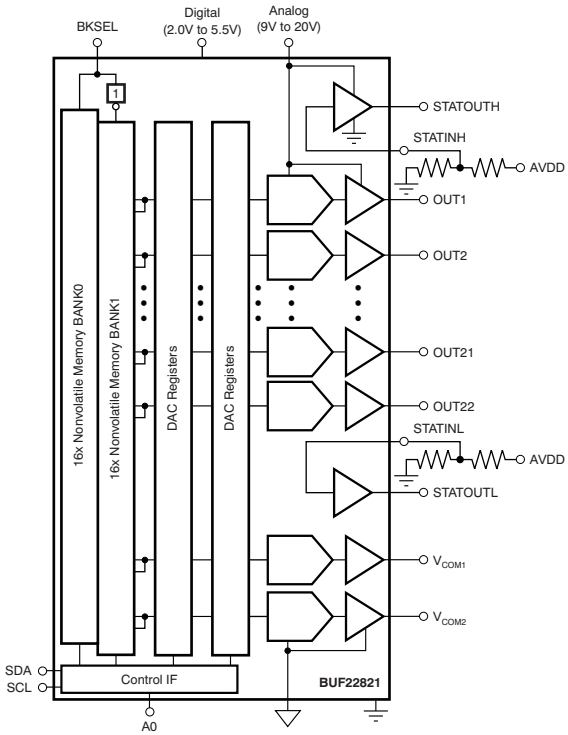
Check for Samples: BUF22821

FEATURES

- **24-CHANNEL GAMMA**
  - **22-CHANNEL PROGRAMMABLE**
  - **2-CHANNEL STATIC GAMMA**
- **2-CHANNEL PROGRAMMABLE V_{COM}**
- **10-BIT RESOLUTION**
- **16x REWRITABLE NONVOLATILE MEMORY**
- **TWO INDEPENDENT MEMORY BANKS**
- **RAIL-TO-RAIL OUTPUT**
- **LOW SUPPLY CURRENT: 0.5mA/channel**
- **SUPPLY VOLTAGE: 9V to 20V**
- **DIGITAL SUPPLY: 2V to 5.5V**
- **I^2C™ INTERFACE**

APPLICATIONS

- **TFT-LCD REFERENCE DRIVERS**



DESCRIPTION

The BUF22821 offers 22 programmable gamma channels, two programmable V_{COM} channels, and two static gamma channels. It is ideal for the new 10-bit source drivers that require 22 gamma channels.

The final gamma and V_{COM} values can be stored in the on-chip, nonvolatile memory. To allow for programming errors or liquid crystal display (LCD) panel rework, the BUF22821 supports up to 16 write operations to the on-chip memory. The BUF22821 has two separate banks of memory, allowing simultaneous storage of two different gamma curves to facilitate switching between gamma curves.

All gamma and V_{COM} channels offer a rail-to-rail output that typically swings to within 100mV of either supply rail with a 10mA load. All channels are programmed using an I^2C interface that supports standard operations up to 400kHz and high-speed data transfers up to 3.4MHz.

The BUF22821 is manufactured using Texas Instruments' proprietary, state-of-the-art, high-voltage CMOS process. This process offers very dense logic and high supply voltage operation of up to 20V. The BUF22821 is offered in a HTSSOP-38 PowerPAD™ package. It is specified from –40°C to +85°C.

RELATED PRODUCTS

FEATURES	PRODUCT
12-Channel Gamma Correction Buffer	BUF12800
20-Channel Programmable Buffer, 10-Bit, V_{COM}	BUF20800
16-/20-Channel Programmable Buffer with Memory	BUF20820
Programmable V_{COM} Driver	BUF01900
18V Supply, Traditional Gamma Buffers	BUF11704
22V Supply, Traditional Gamma Buffers	BUF11705

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	PACKAGE MARKING
BUF22821	HTSSOP-38	DCP	BUF22821

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		BUF22821	UNIT
Supply Voltage, V_S		+22	V
Supply Voltage, V_{SD}		+6	V
Digital Input Terminals, SCL, SDA, AO, BKSEL: Voltage		–0.5 to +6	V
Digital Input Terminals, SCL, SDA, AO, BKSEL: Current		±10	mA
Analog Input Terminals, STATINL, STATINH: Voltage		–0.5 to V_S + 0.5	V
Analog Input Terminals, STATINL, STATINH: Current		±10	mA
Output Short-Circuit(2)		Continuous	
Operating Temperature		–40 to +95	°C
Storage Temperature		–65 to +150	°C
Junction Temperature		+125	°C
ESD Ratings	Human Body Model	4000	V
	Charged-Device Model	1000	V
	Machine Model	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Short-circuit to ground, one channel at a time.

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ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, **T_A = –40°C to +85°C.**
At T_A = +25°C, V_S = +18V, V_{SD} = +2V, R_L = 1.5kΩ connected to ground, and C_L = 200pF, unless otherwise noted.

PARAMETER		CONDITIONS	BUF22821 MIN	BUF22821 TYP	BUF22821 MAX	UNIT
ANALOG GAMMA BUFFER CHANNELS						
Reset Value		Code 512		9		V
OUT 1–22 Output Swing: High		**Code = 1023, Sourcing 10mA**	**17.7**	**17.85**		**V**
OUT 1–22 Output Swing: Low		**Code = 0, Sinking 10mA**		**0.07**	**0.2**	**V**
STATINH Output Swing: High		**V_{IN} = 18V, Sourcing 10mA**	**17.7**	**17.85**		**V**
STATINL Output Swing: Low		**V_{IN} = 0V, Sinking 10mA**		**0.17**	**0.25**	**V**
V_{COM}1, 2 Output Swing: High		**Code = 1023, Sourcing 100mA**	**13**	**16.2**		**V**
V_{COM}1, 2 Output Swing: Low		**Code = 0, Sinking 100mA**		**0.6**	**2**	**V**
Continuous Output Current		Note (1)		30		mA
Output Accuracy				±20	±50	mV
vs Temperature		**Code 512**		**±25**		**µV/°C**
Integral Nonlinearity	INL			0.3		Bits
Differential Nonlinearity	DNL			0.3		Bits
Load Regulation, 10mA	REG	Code 512 or V_{CC}/2, I_{OUT} = +5mA to –5mA Step		0.5	1.5	mV/mA
OTP MEMORY						
Number of OTP Write Cycles					16	Cycles
Memory Retention				100		Years
ANALOG POWER SUPPLY						
Operating Range			9		20	V
Total Analog Supply Current	I_S	Outputs at Reset Values, No Load		12	17	mA
Over Temperature					**18**	**mA**
DIGITAL						
Logic 1 Input Voltage	V_{IH}		0.7 × V_{SD}			V
Logic 0 Input Voltage	V_{IL}				0.3 × V_{SD}	V
Logic 0 Output Voltage	V_{OL}	I_{SINK} = 3mA		0.15	0.4	V
Input Leakage				±0.01	±10	µA
Clock Frequency	**f_{CLK}**	**Standard/Fast Mode**			**400**	**kHz**
		High-Speed Mode			**3.4**	**MHz**
DIGITAL POWER SUPPLY						
Operating Range	V_{SD}		2.0		5.5	V
Digital Supply Current	I_{SD}	Outputs at Reset Values, No Load, Two-Wire Bus Inactive		115	150	µA
Over Temperature				**115**		**µA**
TEMPERATURE RANGE						
Specified Range			–40		+85	°C
Operating Range		Junction Temperature < +125°C	–40		+95	°C
Storage Range			–65		+150	°C
Thermal Resistance(1)	θ_{JA}					
HTSSOP-38		Note (1)		40		°C/W

(1) Thermal pad attached to printed circuit board (PCB), 0lfm airflow, JEDEC High-K test board.

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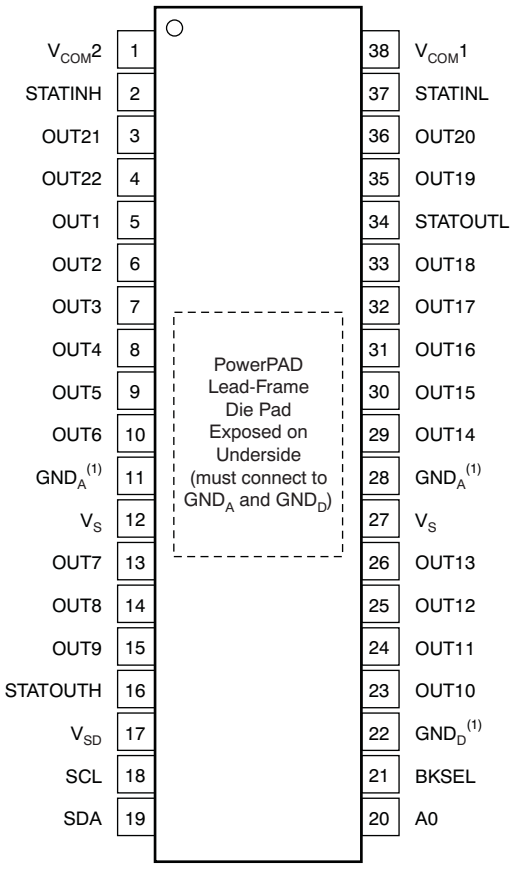
PIN CONFIGURATION

BUF22821
HTSSOP-38
Top View



NOTE: (1) GND_A and GND_D must be connected together.

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PIN DESCRIPTIONS

PIN #	NAME	DESCRIPTION
1	$V_{COM}2$	V_{COM} channel 2
2	STATINH	Static gamma input high; voltage can be set by external voltage divider.
3	OUT21	DAC output 21
4	OUT22	DAC output 22
5	OUT1	DAC output 1
6	OUT2	DAC output 2
7	OUT3	DAC output 3
8	OUT4	DAC output 4
9	OUT5	DAC output 5
10	OUT6	DAC output 6
11, 28	GND_A	Analog ground; must be connected to digital ground (GND_D).
12, 27	V_S	V_S connected to analog supply
13	OUT7	DAC output 7
14	OUT8	DAC output 8
15	OUT9	DAC output 9
16	STATOUTH	Static gamma output high; connect to gamma input on source driver that is closest to V_S.
17	V_{SD}	Digital supply; connect to logic supply
18	SCL	Serial clock input; open-drain, connect to pull-up resistor.
19	SDA	Serial data I/O; open-drain, connect to pull-up resistor.
20	A0	A0 address pin for I^2C address; either connect to logic 1 or logic 0.
21	BKSEL	Selects memory bank 0 or 1; either connect to logic 1 to select bank 1 or logic 0 to select bank 0.
22	GND_D	Digital ground; must be connected to analog ground at the BUF22821.
23	OUT10	DAC output 10
24	OUT11	DAC output 11
25	OUT12	DAC output 12
26	OUT13	DAC output 13
29	OUT14	DAC output 14
30	OUT15	DAC output 15
31	OUT16	DAC output 16
32	OUT17	DAC output 17
33	OUT18	DAC output 18
34	STATOUTL	Static gamma output low; connect to gamma input on source driver that is closest to GND
35	OUT19	DAC output 19
36	OUT20	DAC output 20
37	STATINL	Static gamma input low; voltage can be set by external voltage divider
38	$V_{COM}1$	V_{COM} channel 1

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TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +18V, V_{SD} = +2V, R_L = 1.5kΩ connected to ground, and C_L = 200pF, unless otherwise noted.

OUTPUT VOLTAGE vs OUTPUT CURRENT ($V_{COM}1$ and $V_{COM}2$)

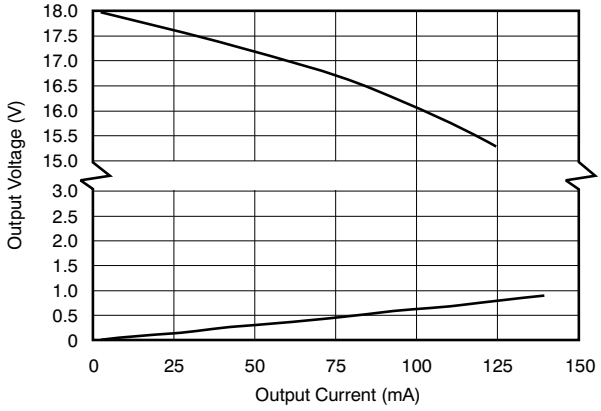

Figure 1.

OUTPUT VOLTAGE vs OUTPUT CURRENT (Channels 1–22)

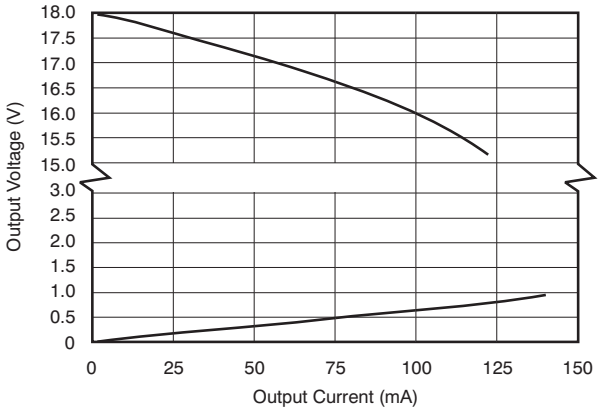

Figure 2.

OUTPUT VOLTAGE vs OUTPUT CURRENT (STATOUTL)

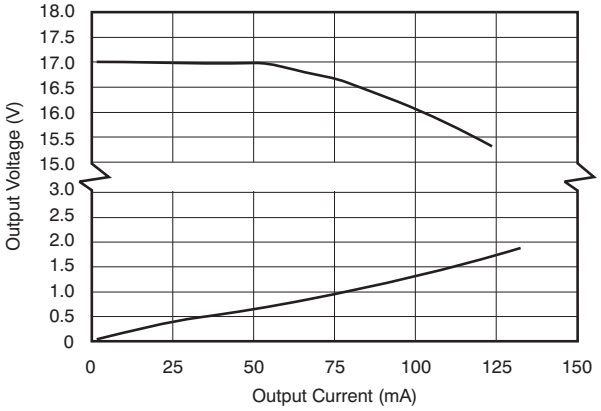

Figure 3.

OUTPUT VOLTAGE vs OUTPUT CURRENT (STATOUTH)

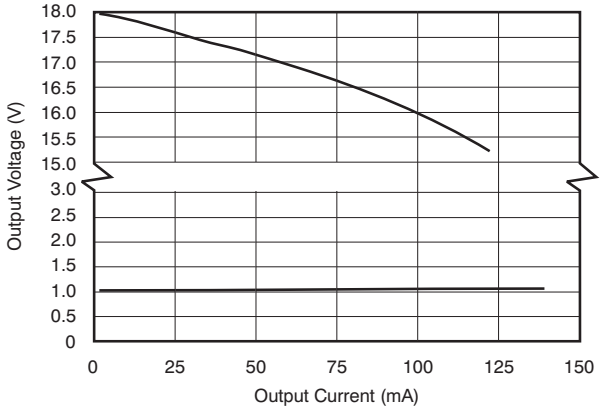

Figure 4.

DIGITAL SUPPLY CURRENT vs TEMPERATURE

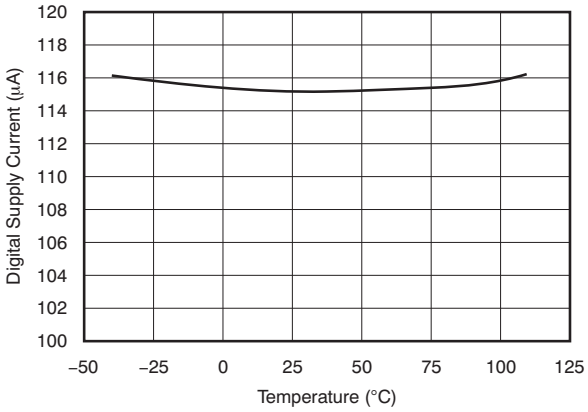

Figure 5.

ANALOG SUPPLY CURRENT vs TEMPERATURE

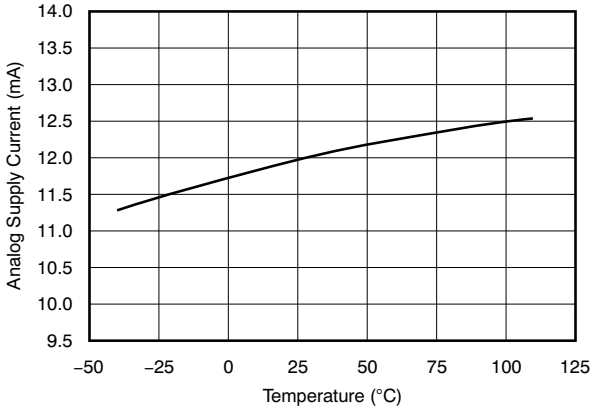

Figure 6.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +18V, V_{SD} = +2V, R_L = 1.5kΩ connected to ground, and C_L = 200pF, unless otherwise noted.

OUTPUT VOLTAGE vs TEMPERATURE

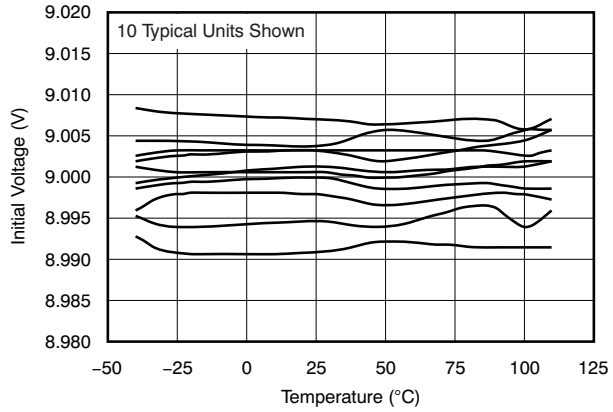

Figure 7.

DIFFERENTIAL LINEARITY ERROR

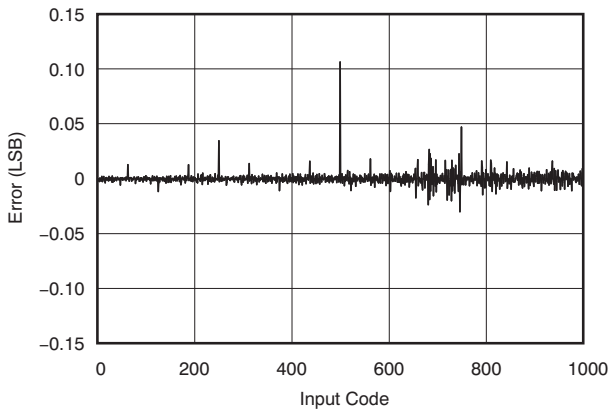

Figure 8.

INTEGRAL LINEARITY ERROR

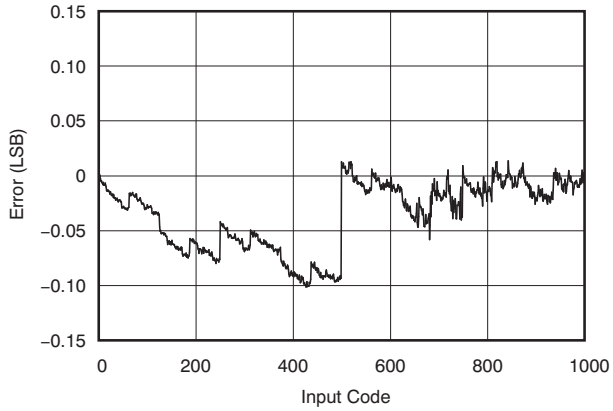

Figure 9.

BKSEL SWITCHING TIME DELAY

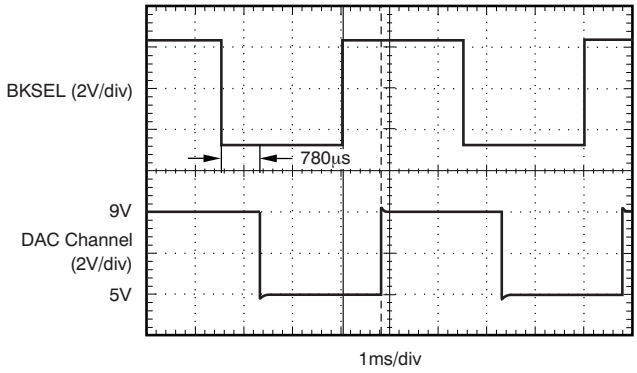

Figure 10.

LARGE-SIGNAL STEP RESPONSE

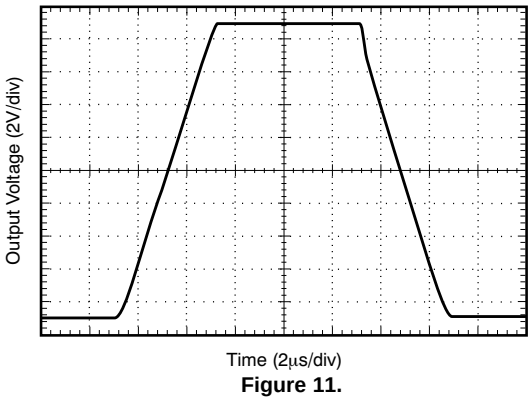

Figure 11.

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APPLICATION INFORMATION

GENERAL

The BUF22821 programmable voltage reference allows fast and easy adjustment of 22 programmable gamma reference outputs and two V_{COM} outputs, each with 10-bit resolution. The BUF22821 is programmed through a high-speed, I^2C interface. The final gamma and V_{COM} values can be stored in the on-chip, nonvolatile memory. To allow for programming errors or liquid crystal display (LCD) panel rework, the BUF22821 supports up to 16 write operations to the on-chip memory. The BUF22821 has two separate banks of memory, allowing simultaneous storage of two different gamma curves to facilitate dynamic switching between gamma curves.

The BUF22821 can be powered using an analog supply voltage from 9V to 20V, and a digital supply from 2V to 5.5V. The digital supply must be applied prior to the analog supply to avoid excessive current and power consumption, or possibly even damage to the device if left connected only to the analog supply for extended periods of time. A typical configuration of the BUF22821 is illustrated in Figure 12.

TWO-WIRE BUS OVERVIEW

The BUF22821 communicates through an industry-standard, two-wire interface to receive data in slave mode. This standard uses a two-wire, open-drain interface that supports multiple devices on a single bus. Bus lines are driven to a logic low level only. The device that initiates the communication is called a *master*, and the devices controlled by the master are *slaves*. The master generates the serial clock on the clock signal line (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, the master initiates a START condition by pulling the data signal line (SDA) from a HIGH to a LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte on the rising edge of SCL, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and eight bits of data are sent, followed by an Acknowledge bit. During data transfer, SDA must remain stable while SCL is HIGH. Any change in SDA while SCL is HIGH is interpreted as a START or STOP condition.

Once all data have been transferred, the master generates a STOP condition, indicated by pulling SDA from LOW to HIGH while SCL is HIGH. The BUF22821 can act only as a slave device; therefore, it never drives SCL. SCL is an input only for the BUF22821.

ADDRESSING THE BUF22821

The address of the BUF22821 is 111010x, where *x* is the state of the A0 pin. When the A0 pin is LOW, the device acknowledges on address 74h (1110100). If the A0 pin is HIGH, the device acknowledges on address 75h (1110101). The A0 pin settings and BUF22821 address options are shown in Table 1.

Other valid addresses are possible through a simple mask change. Contact your TI representative for information.

Table 1. Quick-Reference Table of BUF22821 Addresses

DEVICE/COMPONENT BUF22821 Address:	ADDRESS
A0 pin is LOW (device acknowledges on address 74h)	1110100
A0 pin is HIGH (device acknowledges on address 75h)	1110101

Table 2. Quick-Reference Table of Command Codes

COMMAND	CODE
General Call Reset	Address byte of 00h followed by a data byte of 06h.
High-Speed Mode	00001xxx, with SCL ≤ 400kHz; where *xxx* are bits unique to the Hs-capable master. This byte is called the Hs master code.

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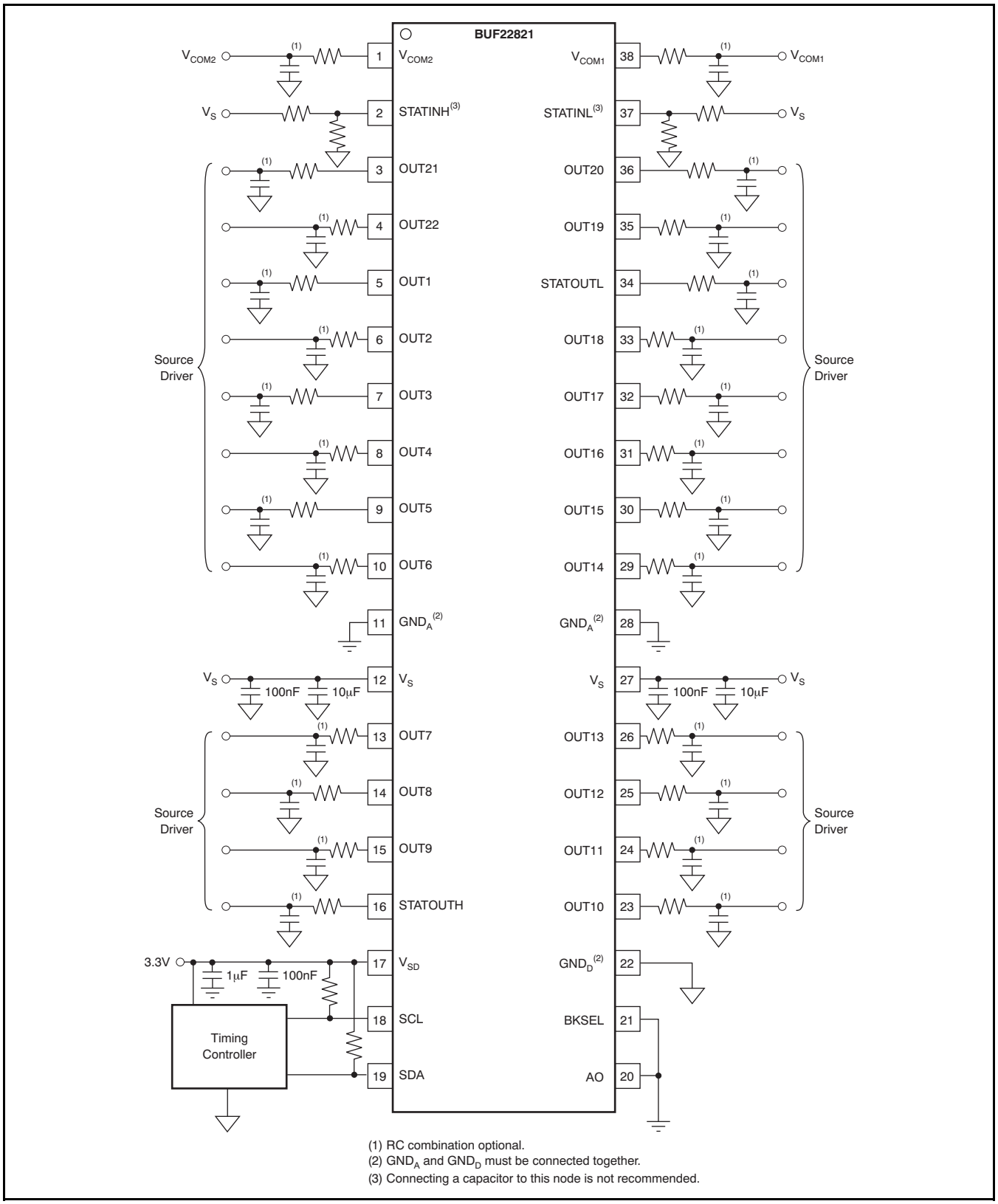

Figure 12. Typical Application Configuration

DATA RATES

The two-wire bus operates in one of three speed modes:

- Standard: allows a clock frequency of up to 100kHz;
- Fast: allows a clock frequency of up to 400kHz; and
- High-speed mode (also called Hs mode): allows a clock frequency of up to 3.4MHz.

The BUF22821 is fully compatible with all three modes. No special action is required to use the device in Standard or Fast modes, but High-speed mode must be activated. To activate High-speed mode, send a special address byte of 00001*xxx*, with SCL = 400kHz, following the START condition; where *xxx* are bits unique to the Hs-capable master, which can be any value. This byte is called the Hs master code. (Note that this is different from normal address bytes—the low bit does not indicate read/write status.) The BUF22821 responds to the High-speed command regardless of the value of these last three bits. The BUF22821 does not acknowledge this byte; the communication protocol prohibits acknowledgement of the Hs master code. On receiving a master code, the BUF22821 switches on its Hs mode filters, and communicates at up to 3.4MHz. Additional high-speed transfers may be initiated without resending the Hs mode byte by generating a repeat START without a STOP. The BUF22821 switches out of Hs mode with the next STOP condition.

GENERAL-CALL RESET AND POWER-UP

The BUF22821 responds to a General-Call Reset, which is an address byte of 00h (0000 0000) followed by a data byte of 06h (0000 0110). The BUF22821 acknowledges both bytes. Upon receiving a General-Call Reset, the BUF22821 performs a full internal reset, as though it had been powered off and then on. It always acknowledges the General-Call address byte of 00h (0000 0000), but does not acknowledge any General-Call data bytes other than 06h (0000 0110).

When the BUF22821 powers up, it automatically performs a reset. As part of the reset, the BUF22821 is configured for all outputs to change to the last programmed nonvolatile memory values, or *1000000000* if the nonvolatile memory values have not been programmed.

OUTPUT VOLTAGE

Buffer output values are determined by the analog supply voltage (V_S) and the decimal value of the binary input code used to program that buffer. The value is calculated using Equation 1:

$$V_{OUT} = V_S \times \left(\frac{CODE_{10}}{1024} \right) \quad (1)$$

The BUF22821 outputs are capable of a full-scale voltage output change in typically 5µs—no intermediate steps are required.

UPDATING THE DAC OUTPUTS

Because the BUF22821 features a double-buffered register structure, updating the digital-to-analog converter (DAC) and/or the V_{COM} **register** is not the same as updating the DAC and/or V_{COM} **output voltage**. There are two methods for updating the DAC/V_{COM} output voltages.

Method 1: Method 1 is used when it is desirable to have the DAC/V_{COM} output voltage change immediately after writing to a DAC register. For each write transaction, the master sets data bit 15 to a '1'. The DAC/V_{COM} output voltage update occurs after receiving the 16th data bit for the currently-written register.

Method 2: Method 2 is used when it is desirable to have all DAC/V_{COM} output voltages change at the same time. First, the master writes to the desired DAC/V_{COM} channels with data bit 15 a '0'. Then, when writing the last desired DAC/V_{COM} channel, the master sets data bit 15 to a '1'. All DAC/V_{COM} channels are updated at the same time after receiving the 16th data bit.

NONVOLATILE MEMORY

BKSEL Pin

The BUF22821 has 16x rewrite capability of the nonvolatile memory. Additionally, the BUF22821 has the ability to store two distinct gamma curves in two different nonvolatile memory banks, each of which has 16x rewrite capability. One of the two available banks is selected using the external input pin, BKSEL. When this pin is low, BANK0 is selected; when this pin is high, BANK1 is selected.

When the BKSEL pin changes state, the BUF22821 acquires the last programmed DAC/V_{COM} values from the nonvolatile memory associated with this newly chosen bank. At power-up, the state of the BKSEL pin determines which memory bank is selected.

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The I^2C master also has the ability to update (acquire) the DAC registers with the last programmed nonvolatile memory values using software control. The bank to be acquired depends on the state of BKSEL.

General Acquire Command

A general acquire command is used to update all registers and DAC/V_{COM} outputs to the last programmed values stored in nonvolatile memory. A single-channel acquire command updates only the register and DAC/V_{COM} output of the DAC/V_{COM} corresponding to the DAC/V_{COM} address used in the single-channel acquire command.

The sequence to initiate a general channel acquire is as follows:

1. Be sure BKSEL is in its desired state and has been stable for at least 1ms.
2. Send a START condition on the bus.
3. Send the appropriate device address (based on A0) and the read/write bit = LOW. The BUF22821 acknowledges this byte.
4. Send a DAC/V_{COM} pointer address byte. Set bit D7 = 1 and D6 = 0. Bits D5–D0 are any valid DAC/V_{COM} address. Only addresses 000000 to 010111 are valid and are acknowledged. See Table 5 for valid DAC/V_{COM} addresses.
5. Send a STOP condition on the bus.

Approximately 750µs (±80µs) after issuing this command, all DAC/V_{COM} registers and DAC/V_{COM} output voltages change to the respective, appropriate nonvolatile memory values.

Single-Channel Acquire Command

The sequence to initiate a single-channel acquire is as follows:

1. Be sure BKSEL is in its desired state and has been stable for at least 1ms.
2. Send a START condition on the bus.
3. Send the device address (based on A0) and read/write bit = LOW. The BUF22821 acknowledges this byte.
4. Send a DAC/V_{COM} pointer address byte using the DAC/V_{COM} address corresponding to the output and register to update with the OTP memory value. Set bit D7 = 0 and D6 = 1. Bits D5–D0 are the DAC/V_{COM} address. Only addresses 000000 to 010111 are valid and are acknowledged. See Table 5 for valid DAC/V_{COM} addresses.
5. Send a STOP condition on the bus.

Approximately 36µs (±4µs) after issuing this command, the specified DAC/V_{COM} register and DAC/V_{COM} output voltage change to the appropriate OTP memory value.

MaxBank

The BUF22821 can provide the user with the number of times the nonvolatile memory of a particular DAC/V_{COM} channel nonvolatile memory has been written to for the current memory bank. This information is provided by reading the register at pointer address *111111*.

There are two ways to update the MaxBank register:

1. After initiating a single-acquire comand, the BUF22821 updates the MaxBank register with a code corresponding to how many times that particular channel memory has been written to.
2. Following a general-acquire command, the BUF22821 updates the MaxBank register with a code corresponding to the maximum number of times the most used channel (OUT1–22 and V_{COM}s) has been written to.

MaxBank is a read-only register and is only updated by performing a general- or single-channel acquire.

Table 3 shows the relationship between the number of times the nonvolatile memory has been programmed and the corresponding state of the MaxBank Register.

Table 3. MaxBank Details

TIMES WRITTEN TO	RETURNS CODE
0	0000
1	0000
2	0001
3	0010
4	0011
5	0100
6	0101
7	0110
8	0111
9	1000
10	1001
11	1010
12	1011
13	1100
14	1101
15	1110
16	1111

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Parity Error Correction

The BUF22821 provides single-bit parity error correction for data stored in the nonvolatile memory to provide increased reliability of the nonvolatile memory. Should a single bit of nonvolatile memory for a channel fail, the BUF22821 corrects for it and updates the appropriate DAC with the intended value when its memory is acquired.

Should more than one bit of nonvolatile memory for a channel fail, the BUF22821 does not correct for it, and updates the appropriate DAC/V_{COM} with the default value of *1000000000*.

DIE_ID AND DIE_REV REGISTERS

The user can verify the presence of the BUF22821 in the system by reading from address *111101*. The BUF22821 returns *0101100100100101* when read at this address.

The user can also determine the die revision of the BUF22821 by reading from register *111100*. The BUF22821 returns *0000000000000000* when a RevA die is present. RevB would be designated by *0000000000000001* and so on.

READ/WRITE OPERATIONS

Read and write operations can be done for a single DAC/V_{COM} or for multiple DACs/V_{COM}s. Writing to a DAC/V_{COM} register differs from writing to the nonvolatile memory. Bits D15–D14 of the most significant byte of data determines if data are written to the DAC/V_{COM} register or the nonvolatile memory.

Read/Write: DAC/V_{COM} Register (volatile memory)

The BUF22821 is able to read from a single DAC/V_{COM}, or multiple DACs/V_{COM}s, or write to the register of a single DAC/V_{COM}, or multiple DACs/V_{COM}s in a single communication transaction. DAC pointer addresses begin with *000000* (which corresponds to OUT1) through *010111* (which corresponds to OUT22).

Write commands are performed by setting the read/write bit LOW. Setting the read/write bit HIGH performs a read transaction.

Writing: DAC/V_{COM} Register (volatile memory)

To write to a single DAC/V_{COM} register:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF22821 acknowledges this byte.
3. Send a DAC/V_{COM} pointer address byte. Set bit D7 = 0 and D6 = 0. Bits D5–D0 are the DAC/V_{COM} address. Only addresses *000000* to *010111* are valid and are acknowledged; see Table 5 for valid addresses.
4. Send two bytes of data for the specified register. Begin by sending the most significant byte first (bits D15–D8, of which only bits D9 and D8 are used, and bits D15–D14 must not be 01), followed by the least significant byte (bits D7–D0). The register is updated after receiving the second byte.
5. Send a STOP or START condition on the bus.

The BUF22821 acknowledges each data byte. If the master terminates communication early by sending a STOP or START condition on the bus, the specified register is not updated. Updating the DAC/V_{COM} register is not the same as updating the DAC/V_{COM} output voltage; see the *Output Latch* section.

The process of updating multiple DAC/V_{COM} registers begins the same as when updating a single register. However, instead of sending a STOP condition after writing the addressed register, the master continues to send data for the next register. The BUF22821 automatically and sequentially steps through subsequent registers as additional data are sent. The process continues until all desired registers have been updated or a STOP or START condition is sent.

To write to multiple DAC/V_{COM} registers:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF22821 acknowledges this byte.
3. Send either the OUT1 pointer address byte to start at the first DAC, or send the pointer address byte for whichever DAC/V_{COM} is the first in the sequence of DACs/V_{COM}s to be updated. The BUF22821 begins with this DAC/V_{COM} and steps through subsequent DACs/V_{COM}s in sequential order.
4. Send the bytes of data; begin by sending the most significant byte (bits D15–D8, of which only bits D9 and D8 have meaning, and bits D15–D14 must not be 01), followed by the least significant byte (bits D7–D0). The first two bytes are for the DAC/V_{COM} addressed in the previous step. The DAC/V_{COM} register is automatically updated after receiving the second byte. The next two bytes are for the following DAC/V_{COM}. That DAC/V_{COM} register is updated after receiving the fourth byte. This process continues until the registers of all following DACs/V_{COM}s have been updated.
5. Send a STOP or START condition on the bus.

The BUF22821 acknowledges each byte. To terminate communication, send a STOP or START condition on the bus. Only DAC registers that have received both bytes of data are updated.

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Reading: DAC/V_{COM}/OTHER Register (volatile memory)

Reading a register returns the data stored in that DAC/V_{COM}/OTHER register.

To read a single DAC/V_{COM}/OTHER register:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF22821 acknowledges this byte.
3. Send the DAC/V_{COM}/OTHER pointer address byte. Set bit D7 = 0 and D6 = 0; bits D5–D0 are the DAC/V_{COM}/OTHER address. Only addresses 000000–010111, 111100, 111101, and 111111 are valid and are acknowledged.
4. Send a START or STOP/START condition.
5. Send the correct device address and read/write bit = HIGH. The BUF22821 acknowledges this byte.
6. Receive two bytes of data. They are for the specified register. The most significant byte (bits D15–D8) is received first; next is the least significant byte (bits D7–D0). In the case of DAC/V_{COM} channels, bits D15–D10 have no meaning.
7. Acknowledge after receiving the first byte.
8. Send a STOP or START condition on the bus or do not acknowledge the second byte to end the read transaction.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not acknowledging.

To read multiple registers:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF22821 acknowledges this byte.
3. Send either the OUT1 pointer address byte to start at the first DAC, or send the pointer address byte for whichever register is the first in the sequence of DACs/V_{COM}s to be read. The BUF22821 begins with this DAC/V_{COM} and steps through subsequent DACs/V_{COM}s in sequential order.
4. Send a START or STOP/START condition on the bus.
5. Send the correct device address and read/write bit = HIGH. The BUF22821 acknowledges this byte.
6. Receive two bytes of data. They are for the specified DAC/V_{COM}. The first received byte is the most significant byte (bits D15–D8, only bits D9 and D8 have meaning), next is the least significant byte (bits D7–D0).
7. Acknowledge after receiving each byte of data.
8. When all desired DACs have been read, send a STOP or START condition on the bus.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not sending the acknowledge bit. The reading of registers DieID, DieRev, and MaxBank is not supported in this mode of operation (they must be read using the single register read method).

Write: Nonvolatile Memory for the DAC Register

The BUF22821 is able to write to the nonvolatile memory of a single DAC/V_{COM} in a single communication transaction. In contrast to the BUF20820, writing to multiple nonvolatile memory words in a single transaction is not supported. Valid DAC/V_{COM} pointer addresses begin with *000000* (which corresponds to OUT1) through *010111* (which corresponds to OUT22).

When programming the nonvolatile memory, the analog supply voltage must be between 9V and 20V. Write commands are performed by setting the read/write bit LOW.

To write to a single nonvolatile register:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF22821 acknowledges this byte. Only addresses 000000 to 010111 are valid and are acknowledged. See Table 5 for DAC/V_{COM} addresses.
3. Send a DAC/V_{COM} pointer address byte. Set bit D7 = 0 and D6 = 0. Bits D5–D0 are the DAC/V_{COM} address.
4. Send two bytes of data for the nonvolatile register of the specified DAC/V_{COM}. Begin by sending the most significant byte first (bits D15–D8, of which only bits D9 and D8 are data bits, and bits D15–D14 must be 01), followed by the least significant byte (bits D7–D0). The register is updated after receiving the second byte.
5. Send a STOP condition on the bus.

The BUF22821 acknowledges each data byte. If the master terminates communication early by sending a STOP or START condition on the bus, the specified nonvolatile register is not updated. Writing a nonvolatile register also updates the DAC/V_{COM} register and output voltage.

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The DAC/V_{COM} register and DAC/V_{COM} output voltage are updated immediately, while the programming of the nonvolatile memory takes up to 250µs. Once a nonvolatile register write command has been issued, no communication with the BUF22821 should take place for at least 250µs. Writing or reading over the serial interface while the nonvolatile memory is being written jeopardizes the integrity of the data being stored.

Read: Nonvolatile Memory for the DAC Register

To read the data present in nonvolatile register for a particular DAC/V_{COM} channel, the master must first issue a general-acquire command, or a single-acquire command with the appropriate DAC/V_{COM} channel chosen. This action updates both the DAC/V_{COM} register(s) and DAC/V_{COM} output voltage(s). The master may then read from the appropriate DAC/V_{COM} register as described earlier.

Table 4. Other Register Pointer Addresses

REGISTER	POINTER ADDRESS
Die_Rev	111100
Die_ID	111101
MaxBank	111111

Table 5. DAC Register Pointer Addresses

REGISTER	POINTER ADDRESS
OUT1	000000
OUT2	000001
OUT3	000010
OUT4	000011
OUT5	000100
OUT6	000101
OUT7	000110
OUT8	000111
OUT9	001000
OUT10	001001
OUT11	001010
OUT12	001011
OUT13	001100
OUT14	001101
OUT15	001110
OUT16	001111
OUT17	010000
OUT18	010001
$V_{COM}1$	010010
$V_{COM}2$	010011
OUT19	010100
OUT20	010101
OUT21	010110
OUT22	010111

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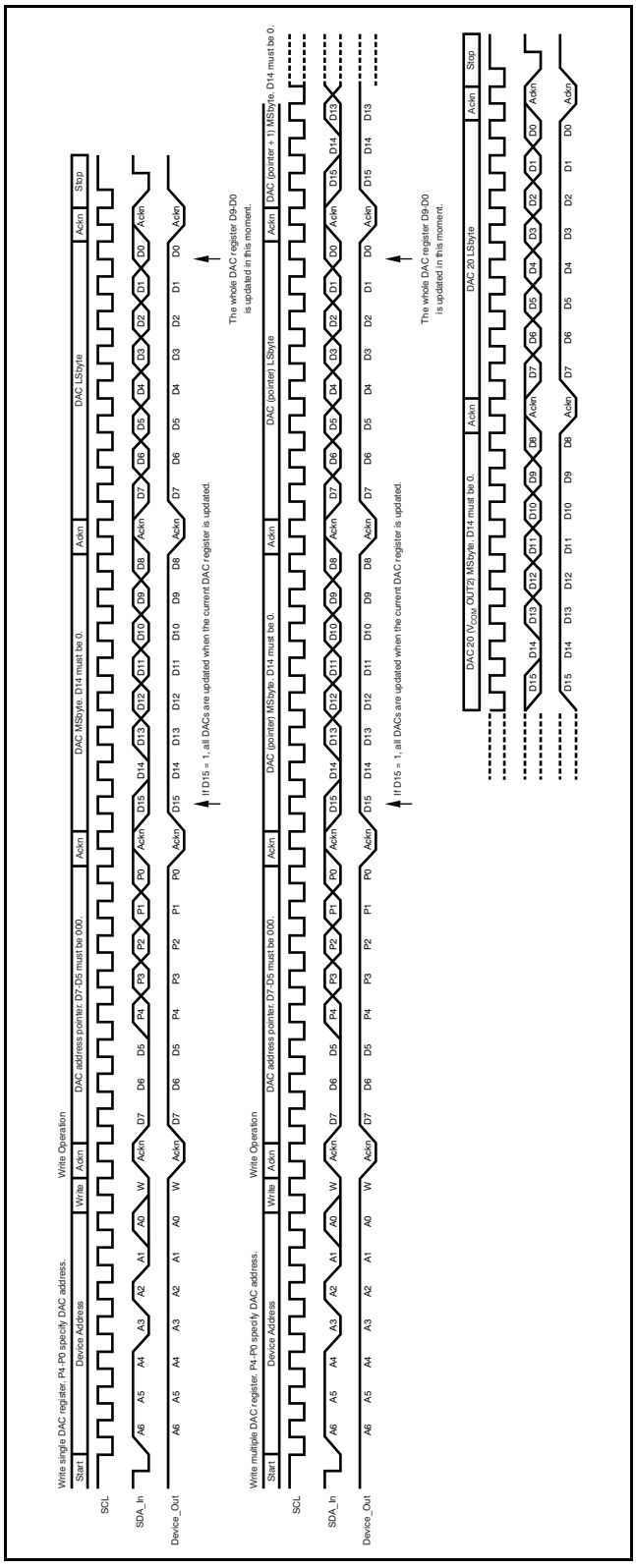

Figure 13. Write DAC Register Timing

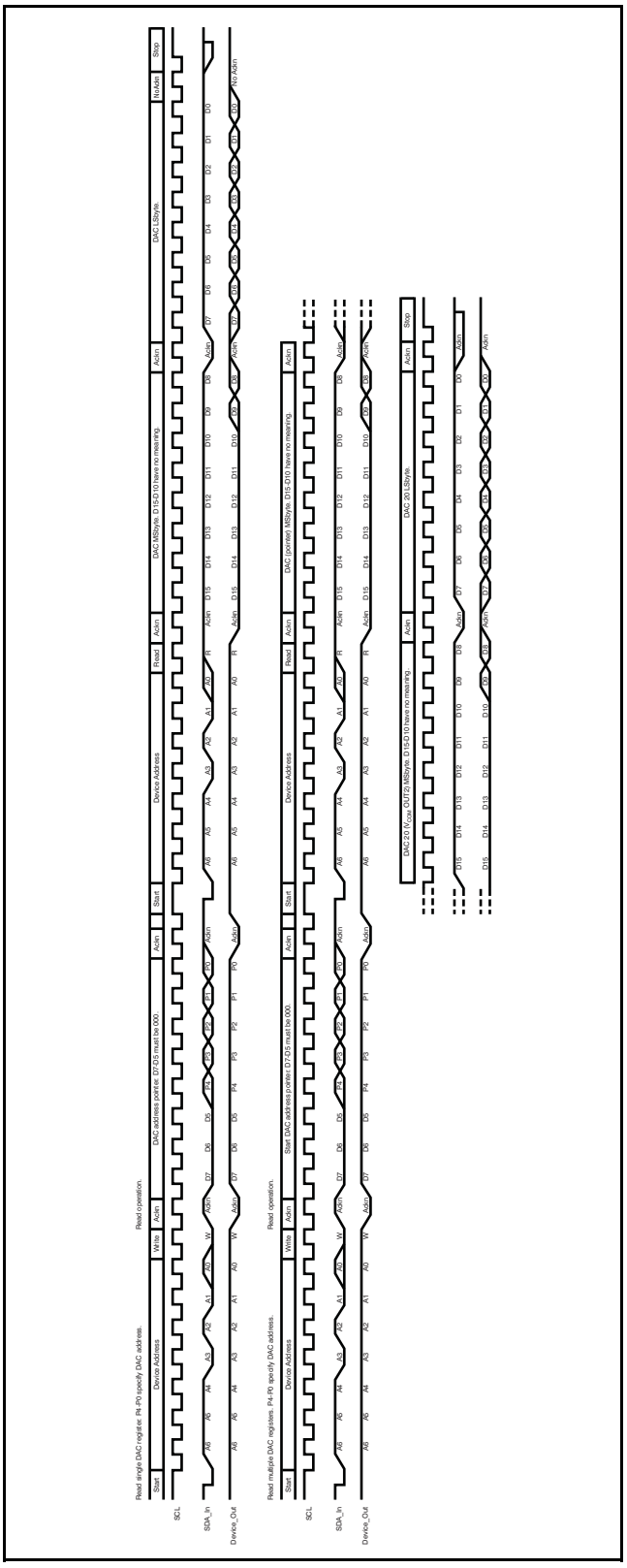

Figure 14. Read Register Timing

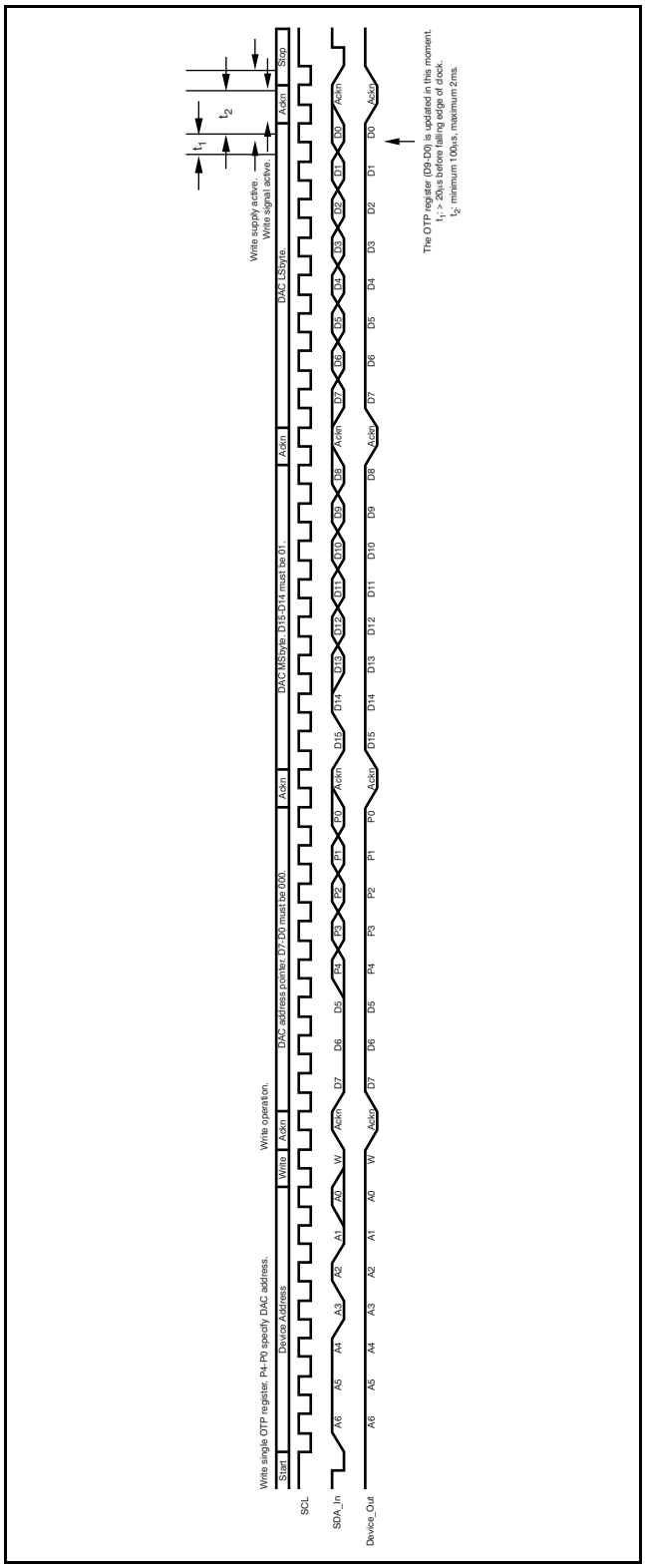

Figure 15. Write Nonvolatile Register Timing

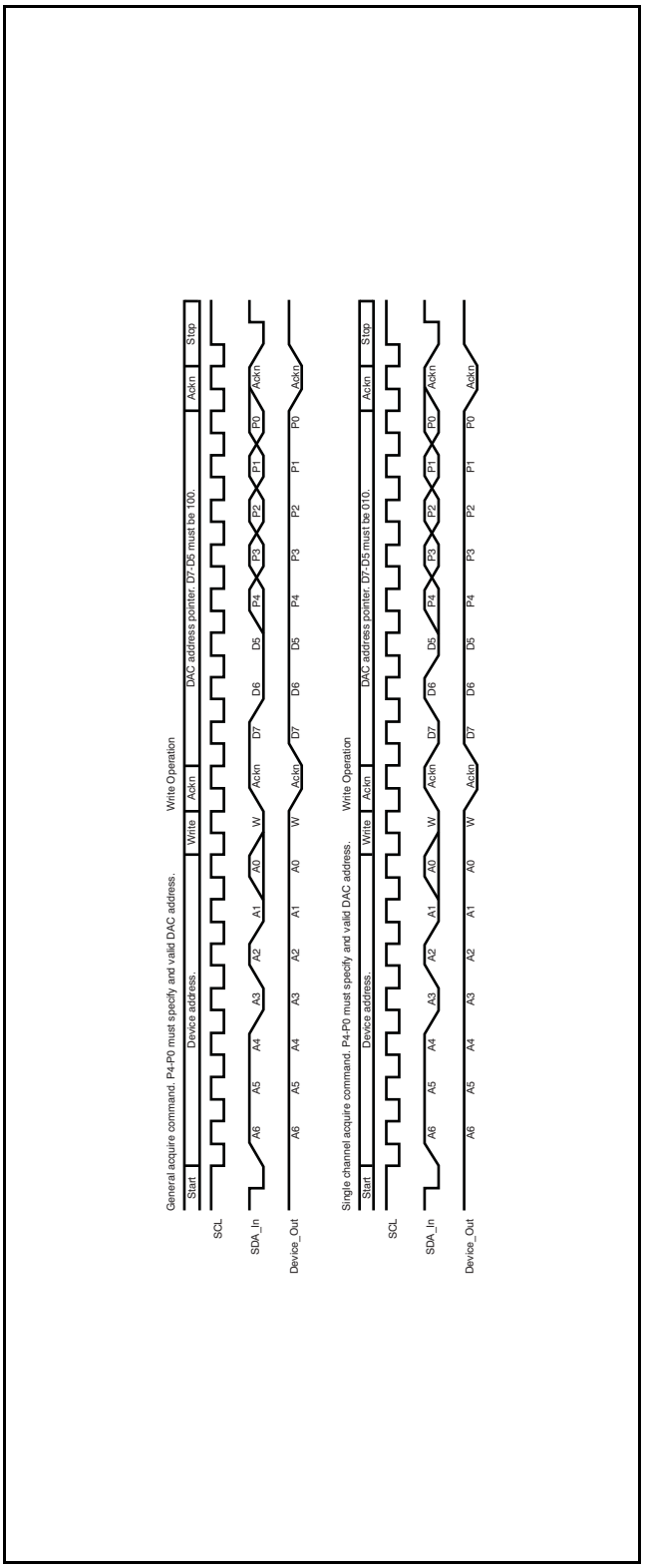

Figure 16. Acquire Operation Timing

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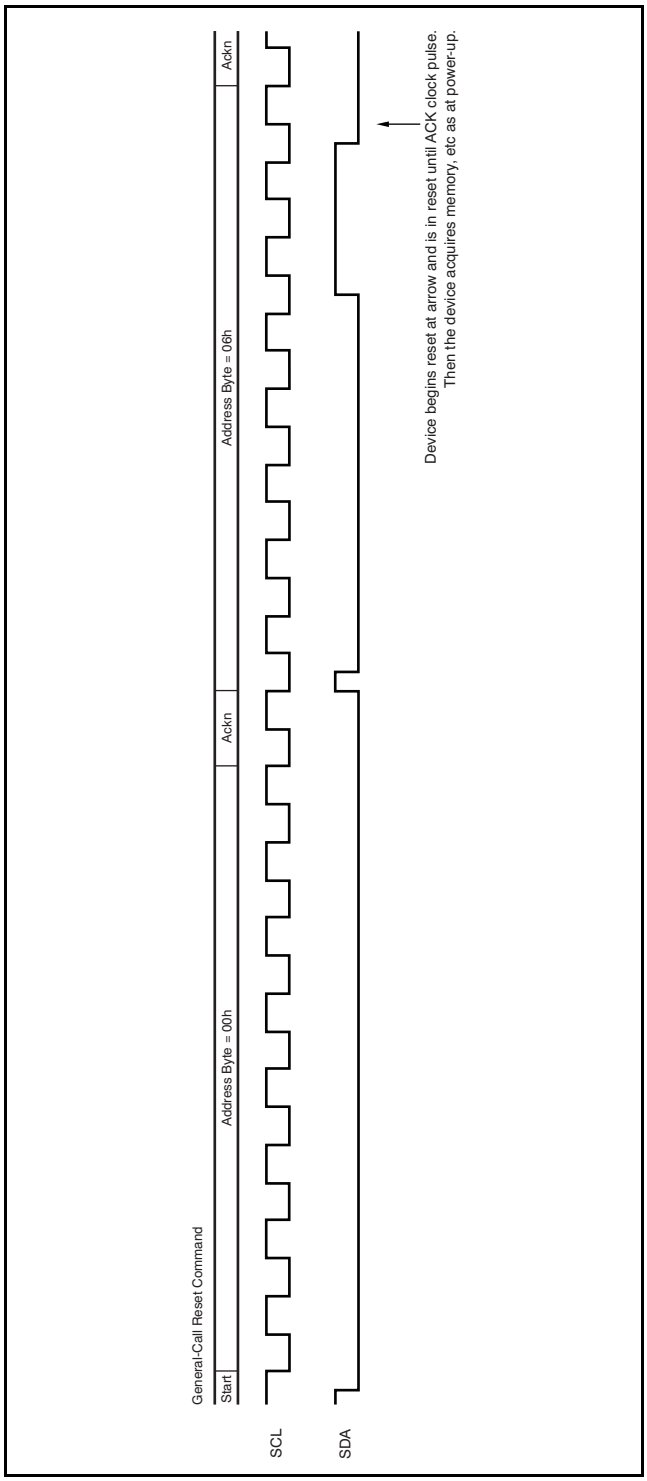

Figure 17. General-Call Reset Timing

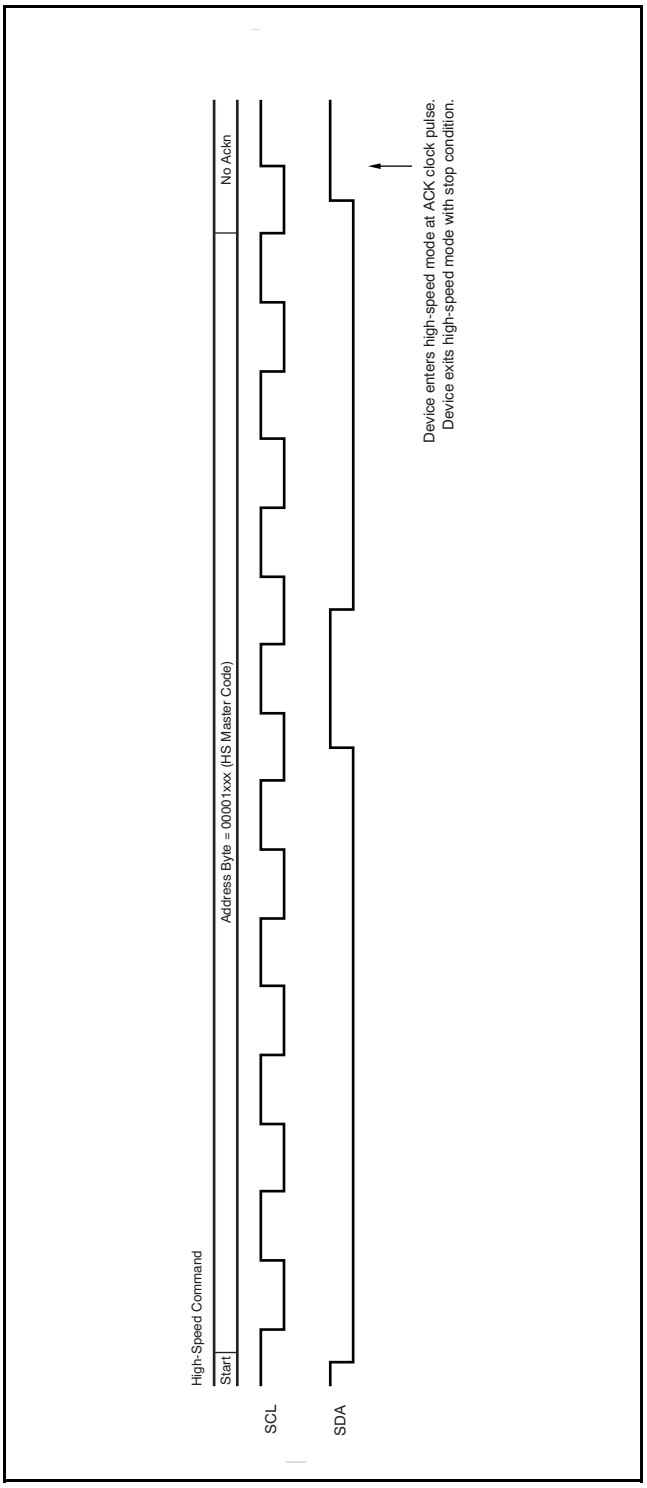

Figure 18. High-Speed Mode Timing

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STATIC GAMMA CHANNELS

The BUF22821 offers two static gamma buffers. These two analog signal paths can be used to provide additional gamma channels. The STATOUTH pin is a buffered version of the STATINH pin. The STATOUTL pin is a buffered version of the STATINL pin. For typical output swing, see the Typical Characteristics.

END-USER SELECTED GAMMA CONTROL

Because the BUF22821 has two banks of nonvolatile memory, it is well-suited for providing two levels of gamma control by using the BKSEL pin, as shown in Figure 19. When the state of the BKSEL pin changes, the BUF22821 updates all 24 programmable buffer outputs simultaneously after 750µs (±80µs).

To update all 24 programmable output voltages simultaneously via hardware:

Toggle the BKSEL pin to switch between Gamma Curve 0 (stored in Bank0) and Gamma Curve 1 (stored in Bank1).

All DAC/V_{COM} registers and output voltages are updated simultaneously after approximately 750µs.

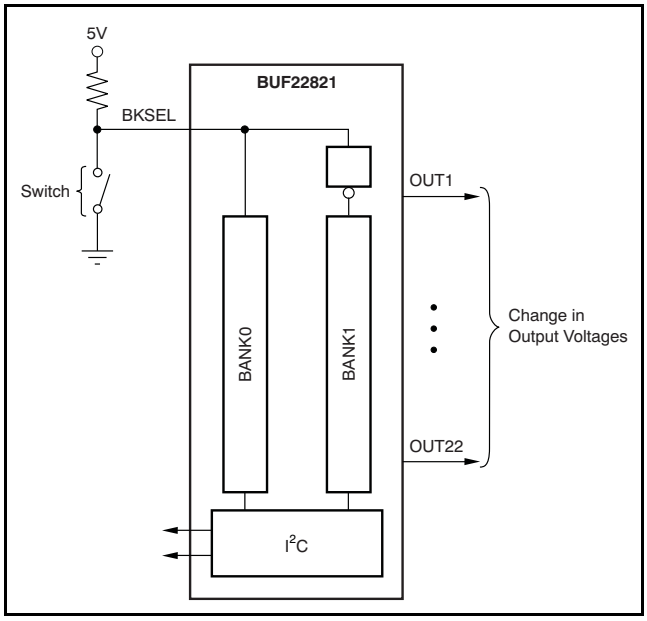

Figure 19. Gamma Control

DYNAMIC GAMMA CONTROL

Dynamic gamma control is a technique used to improve the picture quality in LCD television applications. This technique typically requires switching gamma curves between frames. Using the BKSEL pin to switch between two gamma curves will not likely lead to good results because of the 750µs it takes to transfer the data from the nonvolatile memory to the DAC register. However, dynamic gamma control can still be accomplished by storing two gamma curves in an external EEPROM and writing directly to the DAC register (volatile).

The double register input structure saves programming time by allowing updated DAC values to be pre-stored into the first register bank. Storage of this data can occur while a picture is still being displayed. Because the data are only stored into the first register bank, the DAC/V_{COM} output values remain unchanged—the display is unaffected. At the beginning or the end of a picture frame, the DAC/V_{COM} outputs (and therefore, the gamma voltages) can be quickly updated by writing a '1' in bit 15 of any DAC/V_{COM} register. For details on the operation of the double register input structure, see the *Updating the DAC Outputs* section.

To update all 24 programmable output voltages simultaneously via software:

STEP 1: Write to registers 1–24 with bit 15 always '0'.

STEP 2: Write any DAC/V_{COM} register a second time with identical data. Make sure that bit 15 is set to '1'. All DAC/V_{COM} channels are updated simultaneously after receiving the last bit of data.

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GENERAL POWERPAD DESIGN CONSIDERATIONS

The BUF22821 is available in a thermally-enhanced PowerPAD package. This package is constructed using a downset leadframe upon which the die is mounted, see Figure 20(a) and Figure 20(b). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package; see Figure 20(c). This thermal pad has direct thermal contact with the die; thus, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. Soldering the PowerPAD to the printed circuit board (PCB) is always required, even with applications that have low power dissipation. This provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

The PowerPAD must be connected to the most negative supply voltage on the device, GND_A and GND_D.

1. Prepare the PCB with a top-side etch pattern. There should be etching for the leads as well as etch for the thermal pad.
2. Place recommended holes in the area of the thermal pad. Ideal thermal land size and thermal via patterns for the HTSSOP-38 DCP package can be seen in the technical brief, *PowerPAD Thermally-Enhanced Package* (SLMA002), available for download at www.ti.com. These holes should be 13 mils in diameter. Keep them small, so that solder wicking through the holes is not a problem during reflow. An example thermal land pattern mechanical drawing is attached to the end of this data sheet.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the BUF22821 IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered; thus, wicking is not a problem.
4. Connect all holes to the internal plane that is at the same voltage potential as the GND pins.
5. When connecting these holes to the internal plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the BUF22821 PowerPAD package should make their connection to the internal plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its twelve holes exposed. The bottom-side solder mask should cover the holes of the thermal pad area. This masking prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the BUF22821 IC is simply placed in position and run through the solder reflow operation as any standard surfacemount component. This preparation results in a properly installed part.

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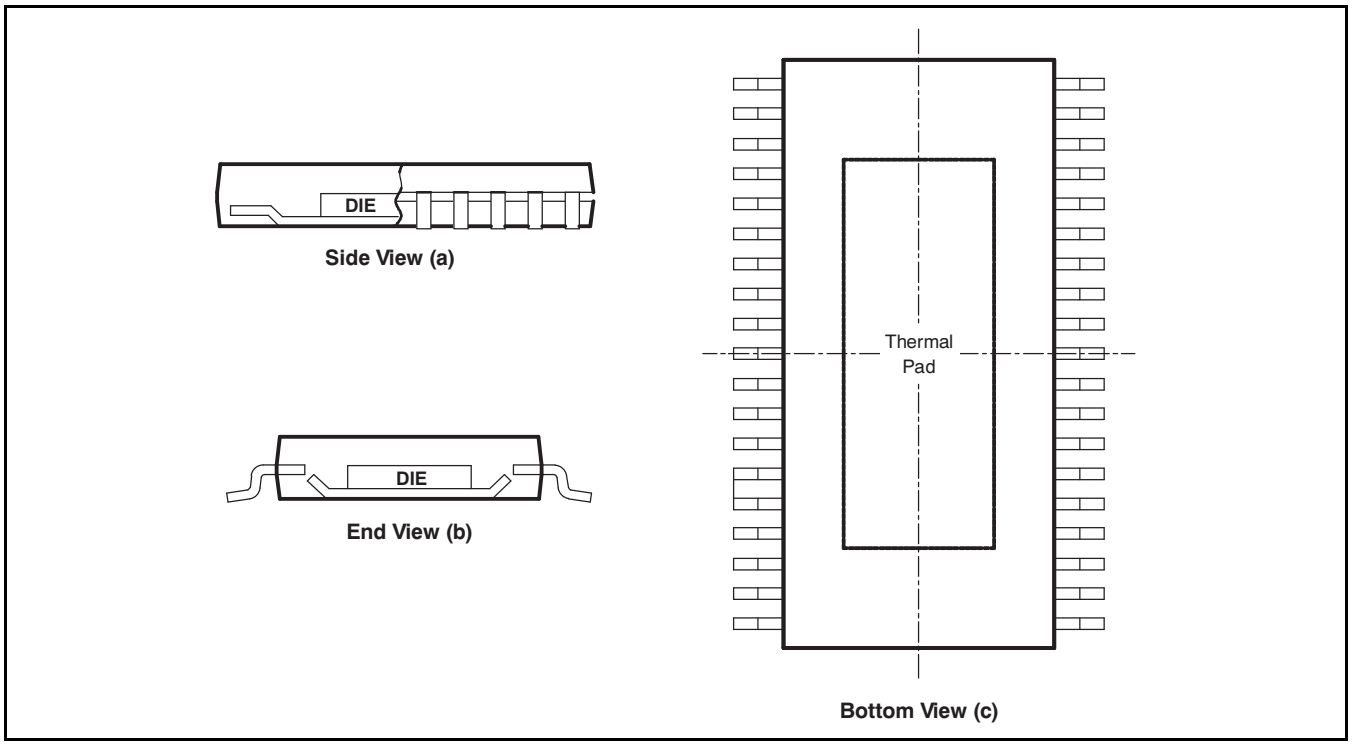

Figure 20. Views of Thermally-Enhanced DCP Package

For a given θ_{JA} (listed in the Electrical Characteristics table), the maximum power dissipation is shown in Figure 21, and is calculated by Equation 2:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right) \quad (2)$$

Where:

P_D = maximum power dissipation (W)

T_{MAX} = absolute maximum junction temperature (+125°C)

T_A = free-ambient air temperature (°C)

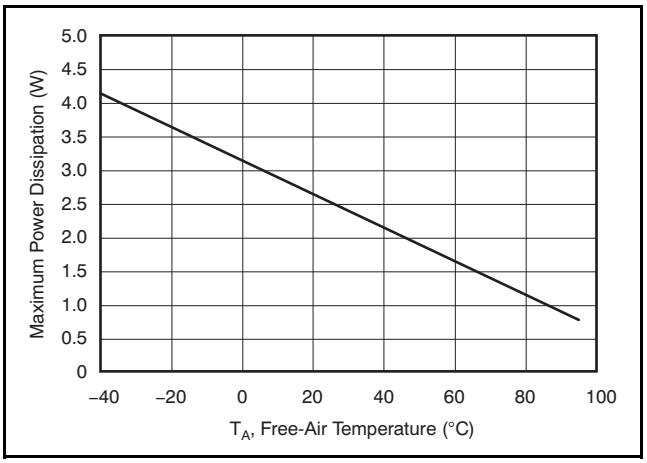

Figure 21. Maximum Power Dissipation vs Free-Air Temperature (with PowerPAD soldered down)

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May, 2009) to Revision D **Page**

- Corrected error in x-axis value for Figure 11 7

Changes from Revision B (February, 2008) to Revision C **Page**

- Updated Figure 5 to reflect specified temperature range 6
- Updated Figure 6 to reflect specified temperature range 6
- Updated Figure 7 to reflect specified temperature range 7
- Changed title of Figure 8 7
- Changed title of Figure 9 7

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BUF22821AIDCPR	ACTIVE	HTSSOP	DCP	38	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 95	BUF22821	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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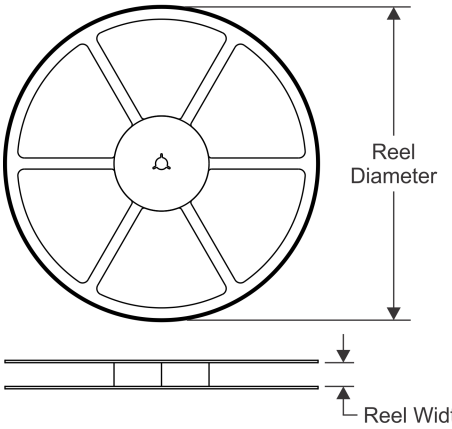
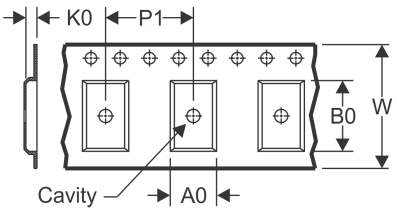
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

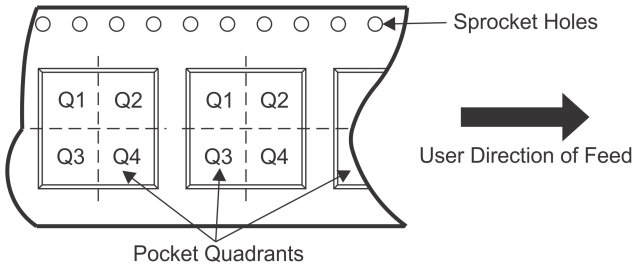


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

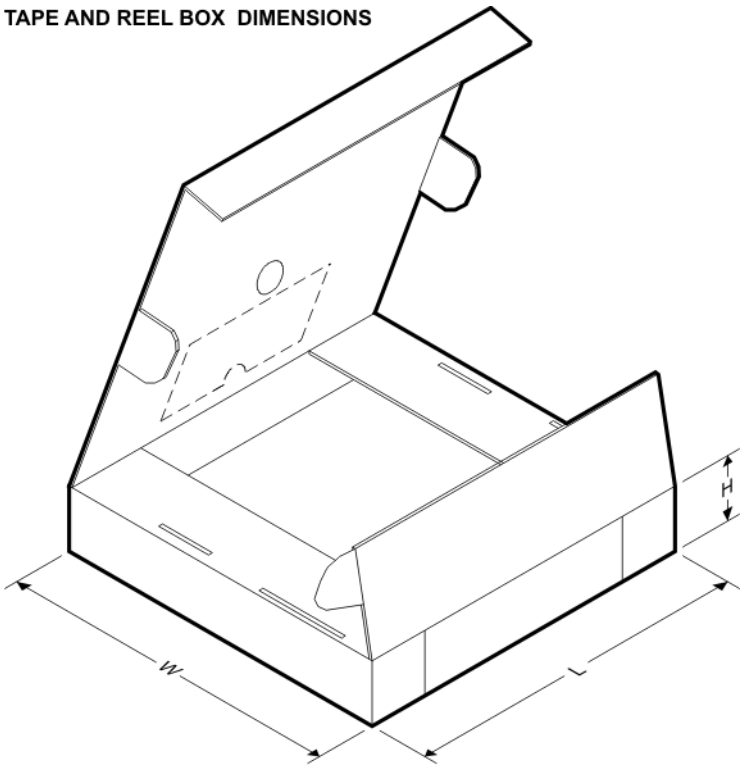
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BUF22821AIDCPR	HTSSOP	DCP	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BUF22821AIDCPR	HTSSOP	DCP	38	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

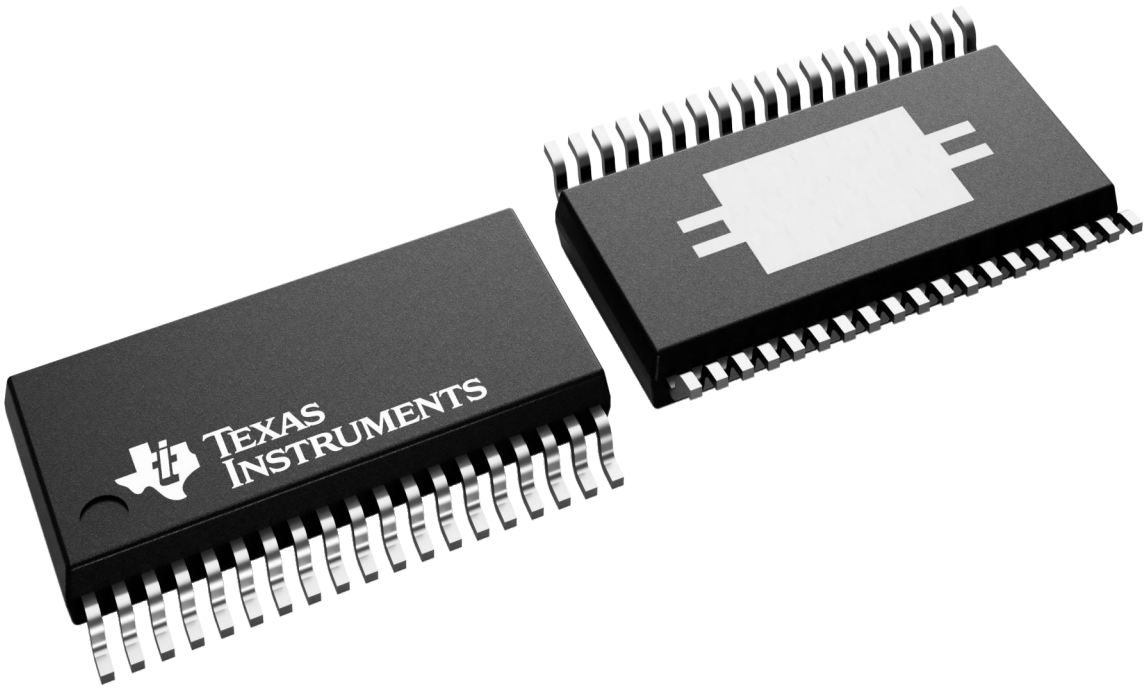
DCP 38

PowerPAD TSSOP - 1.2 mm max height

4.4 x 9.7, 0.5 mm pitch

SMALL OUTLINE PACKAGE

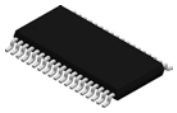
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224560/B

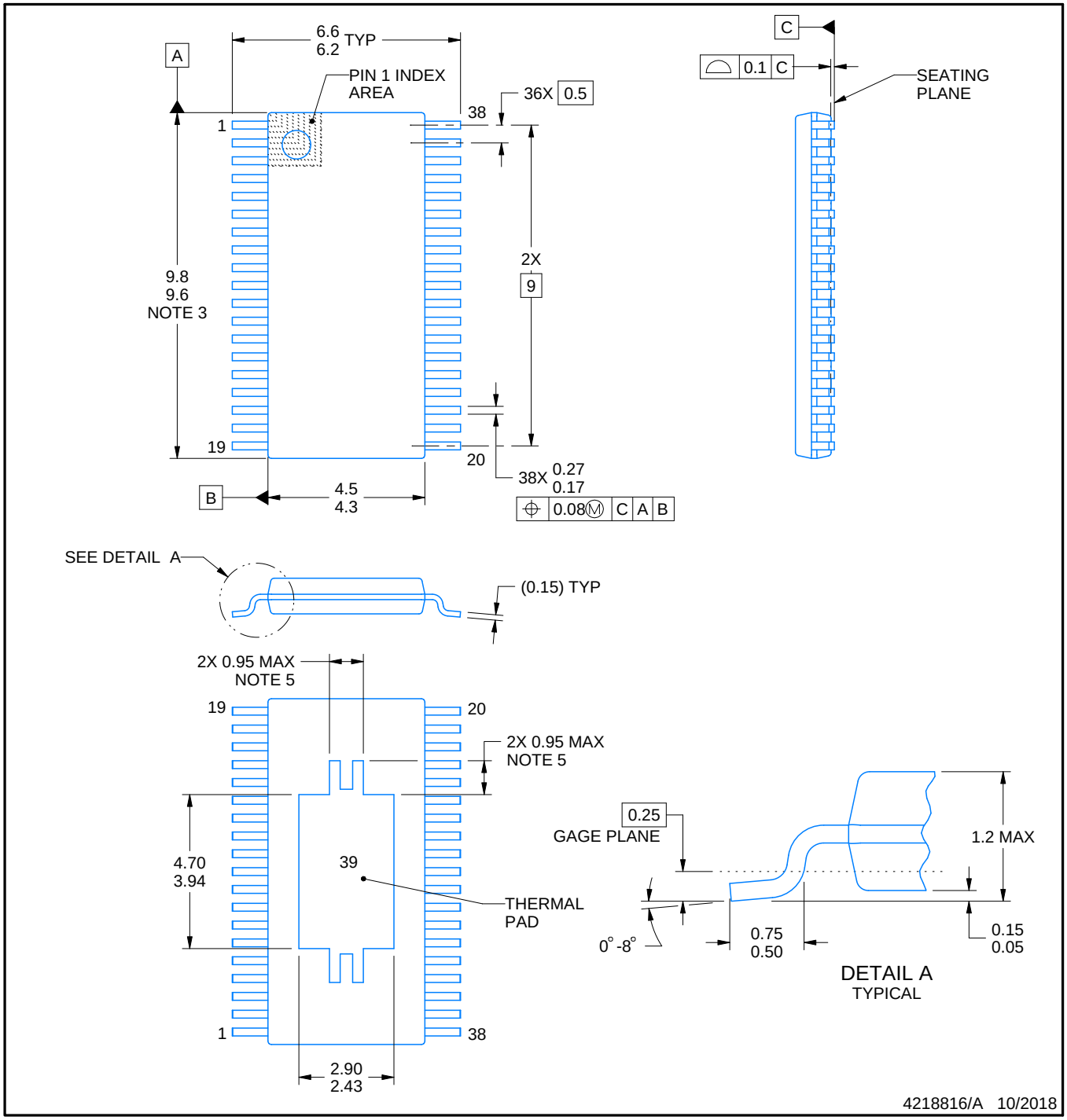
PACKAGE OUTLINE

DCP0038A



PowerPAD™ TSSOP - 1.2 mm max height

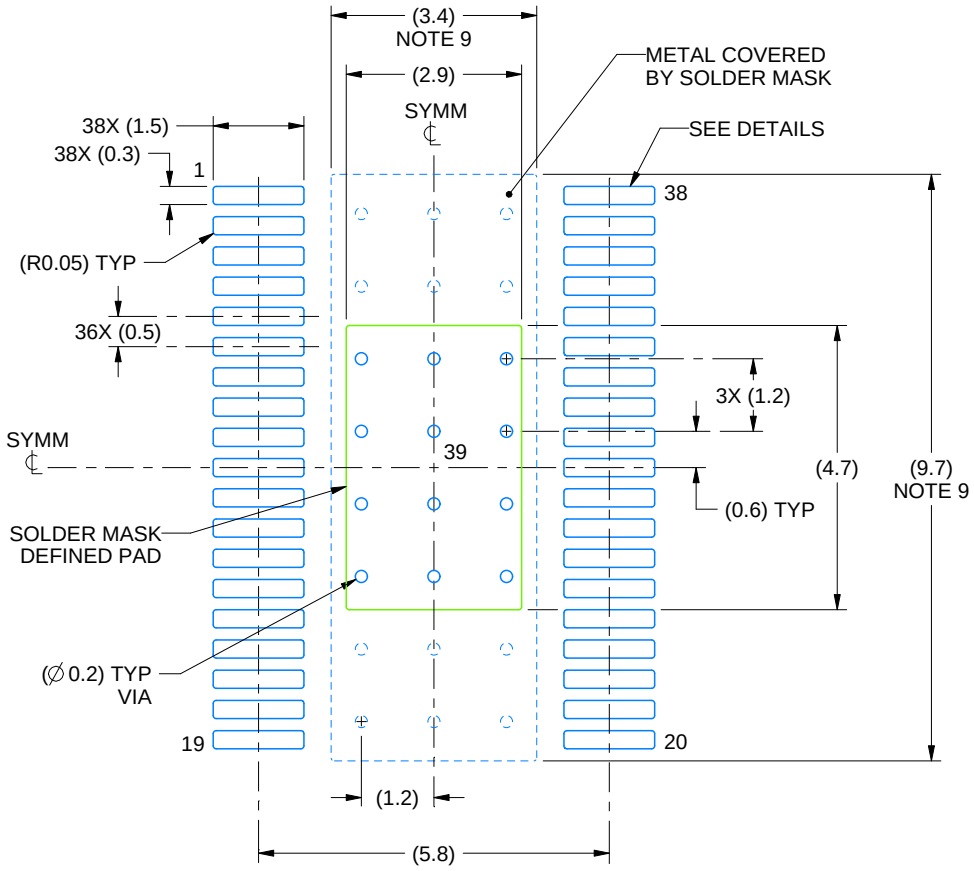
SMALL OUTLINE PACKAGE



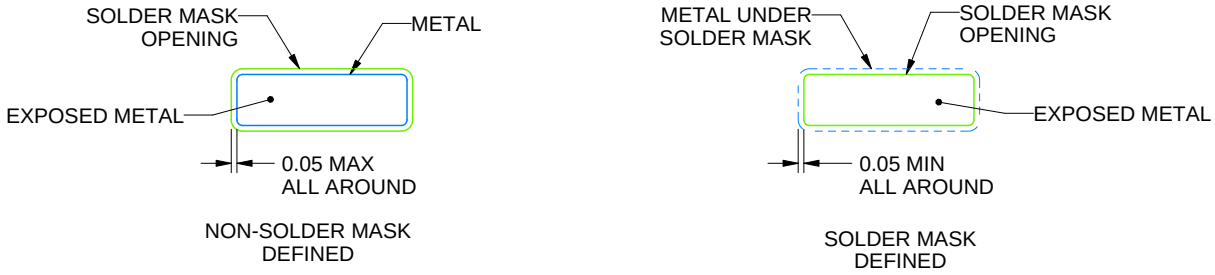
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

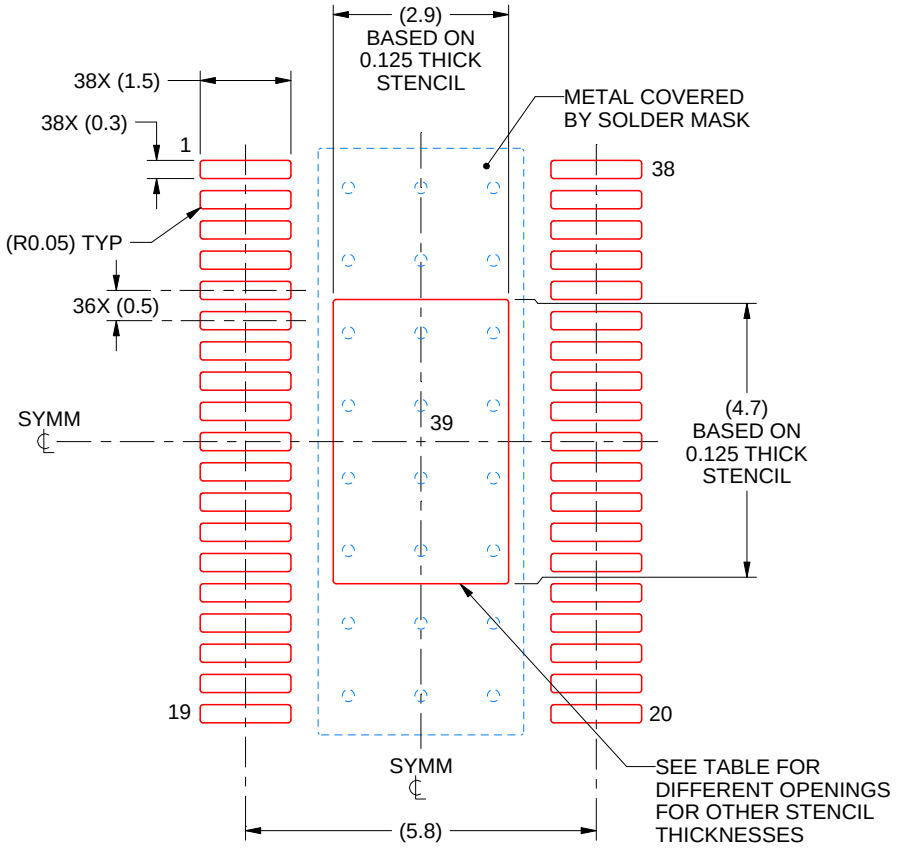


SOLDER MASK DETAILS

4218816/A 10/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.24 X 5.25
0.125	2.90 X 4.70 (SHOWN)
0.15	2.65 X 4.29
0.175	2.45 X 3.97

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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