TPS7A89
小型双路 2A 低噪声 (3.8μV_{RMS}) LDO 稳压器

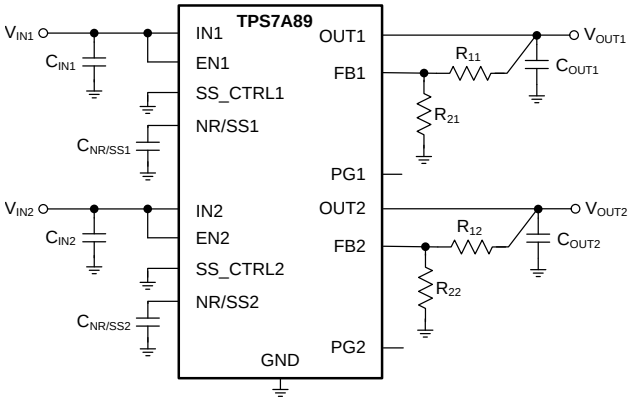
1 特性

- 两个独立的 LDO 通道
- 4mm × 4mm 20 引脚超薄型四方扁平无引线 (WQFN) 封装
- 低输出噪声：3.8μV_{RMS}（10Hz 至 100kHz）
- 低压降：2A 时为 180mV（典型值）
- 宽输入电压范围：1.4V 至 6.5V
- 宽输出电压范围：0.8V 至 5.2V
- 高电源抑制比 (PSRR)：
  - 直流时为 75dB
  - 100kHz 时为 40dB
  - 1MHz 时为 40dB
- 整个线路、负载和温度范围内的精度达 1.0%
- 出色的负载瞬态响应
- 可调节的启动浪涌控制
- 可选软启动充电电流
- 独立开漏电源正常 (PGx) 输出
- 与 10μF 或更大的陶瓷输出电容一起工作时保持稳定

2 应用

- 高速模拟电路：
  - 压控振荡器 (VCO)、模数转换器 (ADC)、数模转换器 (DAC) 以及低压差分信令 (LVDS)
- 成像：互补金属氧化物半导体 (CMOS) 传感器，视频专用集成电路 (ASIC)
- 测试和测量
- 仪器仪表、医疗和音频
- 数字负载辅助电源轨：
  - 串行解串器 (SerDes)、现场可编程门阵列 (FPGA)、数字信号处理器 (DSP)

典型应用电路



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3 说明

TPS7A89 是一款双路、低噪声 (3.8 μV_{RMS})、低压降 (LDO) 稳压器，每通道具有 2A 的拉电流能力，其最高压降仅为 400mV。

TPS7A89 提供两个独立的 LDO，极具灵活性，解决方案尺寸要比两个单通道 LDO 小 60% 左右。每个输出可通过外部电阻在 0.8V 至 5.2 V 范围内进行调节。TPS7A89 的宽输入电压范围支持其在 1.4V 至 6.5V 范围内的电压下工作。

TPS7A89 的输出电压精度（整个线路、负载和温度范围内）达 1%，并且可通过软启动功能减少浪涌电流，因此非常适合为敏感类模拟低压器件 [例如，压控振荡器 (VCO)、模数转换器 (ADC)、数模转换器 (DAC)、高端处理器和现场可编程门阵列 (FPGA)] 供电。

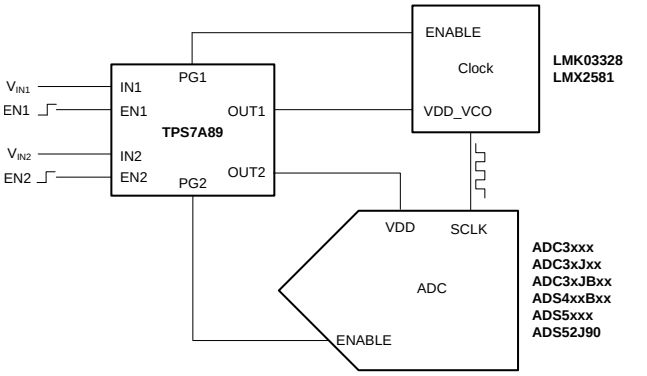
TPS7A89 旨在为噪声敏感类组件供电，广泛适用于高速通信、视频、医疗或测试和测量等 应用。此器件具有 3.8 μV_{RMS} 的超低输出噪声和宽带电源抑制比 (PSRR)（1MHz 时为 40dB），最大限度减少了相位噪声和时钟抖动。这些 功能 最大限度提升了计时器件、ADC 和 DAC 的性能。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS7A89	WQFN (20)	4.00mm x 4.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

为信号链供电



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4 修订历史记录

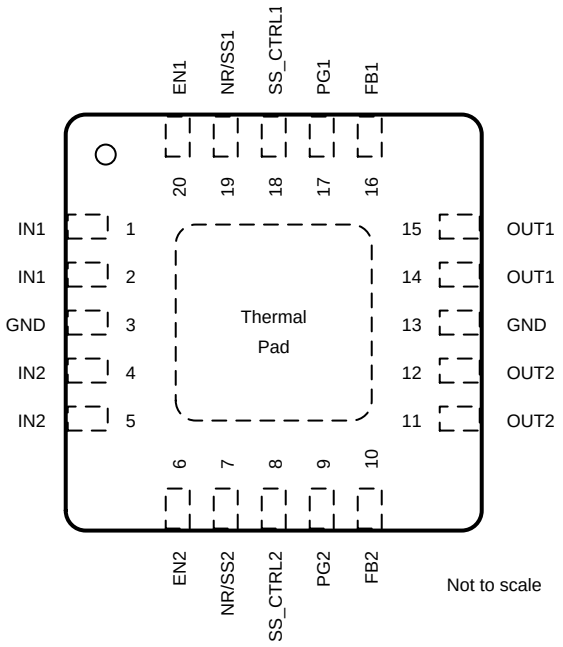
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• 已发布为“量产数据”	1

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5 Pin Configuration and Functions

RTJ Package
4-mm × 4-mm, 20-Pin WQFN
Top View



Pin Functions

PIN			DESCRIPTION
NAME	NO.	I/O	
EN1	20	I	Enable pin for each channel. These pins turn the regulator on and off. If V_{ENx} (1) ≥ $V_{IH(ENx)}$, then the regulator is enabled. If V_{ENx} ≤ $V_{IL(ENx)}$, then the regulator is disabled. The ENx pin must be connected to INx if the enable function is not used.
EN2	6		
FB1	16	I	Feedback pin connected to the error amplifier. Although not required, a 10-nF feed-forward capacitor from FBx to OUTx (as close to the device as possible) is recommended to maximize ac performance. The use of a feed-forward capacitor can disrupt PGx (power good) functionality. See the *Feed-Forward Capacitor (C_{FFx})* and *Setting the Output Voltage (Adjustable Operation)* sections for more details.
FB2	10		
GND	3, 13	—	Ground pin. These pins must be connected to ground, the thermal pad, and each other with a low-impedance connection.
IN1	1, 2	I	Input supply pin for LDO 1. A 10 µF or greater input capacitor is required. Place the input capacitor as close to the input as possible.
IN2	4, 5	I	Input supply pin for LDO 2. A 10 µF or greater input capacitor is required. Place the input capacitor as close to the input as possible.
NR/SS1	19	—	Noise-reduction and soft-start pin for each channel. Connecting an external capacitor between this pin and ground reduces reference voltage noise and also enables the soft-start function. Although not required, a 10 nF or larger capacitor is recommended to be connected from NR/SSx to GND (as close to the pin as possible) to maximize ac performance. See the *Noise-Reduction and Soft-Start Capacitor ($C_{NR/SSx}$)* section for more details.
NR/SS2	7		
OUT1	14, 15	O	Regulated output for LDO 1. A 22-µF or larger ceramic capacitor (10 µF or greater of effective capacitance) from OUTx to ground is required for stability and must be placed as close to the output as possible. Minimize the impedance from the OUT1 pin to the load. See the *Input and Output Capacitor (C_{INx} and C_{OUTx})* section for more details.
OUT2	11, 12	O	Regulated output for LDO 2. A 22-µF or larger ceramic capacitor (10 µF or greater of effective capacitance) from OUTx to ground is required for stability and must be placed as close to the output as possible. Minimize the impedance from the OUT2 pin to the load. See the *Input and Output Capacitor (C_{INx} and C_{OUTx})* section for more details.
PG1	17	O	Open-drain power-good indicator pins for the LDO 1 and LDO 2 output voltages. A 10-kΩ to 100-kΩ external pullup resistor is required. These pins can be left floating or connected to GND if not used. The use of a feed-forward capacitor can disrupt power-good functionality. See the *Feed-Forward Capacitor (C_{FFx})* section for more details.
PG2	9		
SS_CTRL1	18	I	Soft-start control pin for each channel. Connect these pins either to GND or INx to allow normal or fast charging of the NR/SSx capacitor. If a $C_{NR/SSx}$ capacitor is not used, SS_CTRLx must be connected to GND to avoid output overshoot.
SS_CTRL2	8		
Thermal pad		—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

(1) Lowercase x indicates that the specification under consideration applies to both channel 1 and channel 2, one channel at a time.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range and all voltages with respect to GND (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	INx, PGx, ENx(2)	–0.3	7.0	V
	INx, PGx, ENx (5% duty cycle, pulse duration = 200 µs)	–0.3	7.5	
	OUTx	–0.3	V_{INx} + 0.3(3)	
	SS_CTRLx	–0.3	V_{INx} + 0.3(3)	
	NR/SSx, FBx(2)	–0.3	3.6	
Current	OUTx(2)	Internally limited		A
	PGx (sink current into device)(2)		5	mA
Temperature	Operating junction, T_J	–55	150	°C
	Storage, T_{stg}	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Lowercase x indicates that the specification under consideration applies to both channel 1 and channel 2, one channel at a time.
(3) The absolute maximum rating is V_{INx} + 0.3 V or 7.0 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{INx}	Input supply voltage range	1.4	6.5	V
V_{OUTx}	Output voltage range	0.8 – 1%	5.2 + 1%	V
I_{OUTx}	Output current	0	2	A
C_{INx}	Input capacitor, each input	10		µF
C_{OUTx}	Output capacitor	22		µF
$C_{NR/SSx}$	Noise-reduction capacitor		1	µF
R_{PGx}	Power-good pullup resistance	10	100	kΩ
T_J	Junction temperature range	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A89 RTJ (WQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

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6.5 Electrical Characteristics

over operating temperature range (T_J = –40°C to +125°C), V_{INx} = 1.4 V or $V_{OUTx(TARGET)}$ + 0.2 V (whichever is greater), $V_{OUTx(TARGET)}$ = 0.8 V, I_{OUTx} = 50 mA, V_{ENx} = 1.4 V, C_{OUTx} = 10 µF, $C_{NR/SSx}$ = 0 nF, C_{FFx} = 0 nF, SS_CTRLx = GND, PGx pin pulled up to V_{INx} with 100 kΩ, and for each channel (unless otherwise noted); typical values are at T_J = 25°C

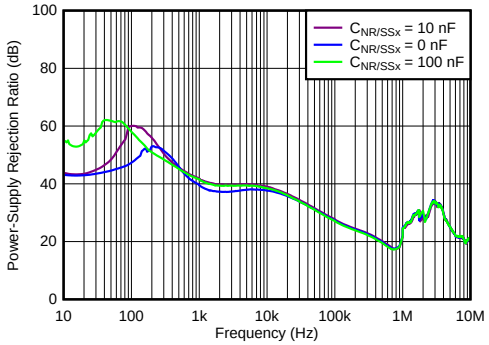
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{INx} (1)	Input supply voltage range		1.4		6.5	V
V_{REF}	Reference voltage			0.8		V
V_{UVLOx}	Input supply UVLOx	V_{INx} rising		1.31	1.39	V
$V_{UVLOx(HYS)}$	V_{UVLOx} hysteresis	V_{INx} falling hysteresis		290		mV
V_{OUTx}	Output voltage range		0.8 – 1%		5.2 + 1%	V
	V_{OUTx} accuracy (2)	0.8 V ≤ V_{OUTx} ≤ 5.2 V, 5 mA ≤ I_{OUTx} ≤ 2 A	–1.0%		1.0%	
$\Delta V_{OUTx(\Delta VINx)}$	Line regulation	I_{OUTx} = 5 mA, 1.4 V ≤ V_{INx} ≤ 6.5 V		0.003		%/V
$\Delta V_{OUTx(\Delta IOUTx)}$	Load regulation	5 mA ≤ I_{OUTx} ≤ 2 A		0.03		%/A
V_{OSx}	Error amplifier offset voltage	T_J = 25°C	–2		2	mV
$V_{OS1} – V_{OS2}$	Delta between each channel offset voltage	T_J = 25°C	–2		2	mV
V_{DO}	Dropout voltage	1.8 V ≤ V_{INx} ≤ 4.8 V, I_{OUTx} = 2 A, V_{FBx} = 0.8 V – 3%		180	300	mV
		1.4 V ≤ V_{INx} < 1.8 V and 4.8 V < V_{INx} ≤ 5.6 V, I_{OUTx} = 2 A, V_{FBx} = 0.8 V – 3%		250	400	
I_{LIM}	Output current limit	V_{OUTx} forced at 0.9 × $V_{OUTx(TARGET)}$	2.3	2.6	2.9	A
I_{GND}	GND pin current	Both channels enabled, per channel, V_{INx} = 6.5 V, I_{OUTx} = 5 mA		2.1	3.5	mA
		Both channels enabled, per channel, V_{INx} = 1.4 V, I_{OUTx} = 2 A			4	
I_{SDN}	Shutdown GND pin current	Both channels shutdown, per channel, PGx = (open), V_{INx} = 6.5 V, V_{ENx} = 0.4 V		0.1	15	µA
I_{ENx}	ENx pin current	V_{INx} = 6.5 V, 0 V ≤ V_{ENx} ≤ 6.5 V	–0.2		0.2	µA
$V_{IL(ENx)}$	ENx pin low-level input voltage (device disabled)		0		0.4	V
$V_{IH(ENx)}$	ENx pin high-level input voltage (device enabled)		1.1		6.5	V
I_{SS_CTRLx}	SS_CTRLx pin current	V_{INx} = 6.5 V, 0 V ≤ V_{SS_CTRLx} ≤ 6.5 V	–0.2		0.2	µA
$V_{IT(PGx)}$	PGx pin threshold	For PGx transitioning low with falling V_{OUTx}, expressed as a percentage of $V_{OUTx(TARGET)}$	82%	88.9%	93%	
$V_{hys(PGx)}$	PGx pin hysteresis	For PGx transitioning high with rising V_{OUTx}, expressed as a percentage of $V_{OUTx(TARGET)}$		1%		
$V_{OL(PGx)}$	PGx pin low-level output voltage	V_{OUTx} < $V_{IT(PGx)}$, I_{PGx} = –1 mA (current into device)			0.4	V
$I_{lkg(PGx)}$	PGx pin leakage current	V_{OUTx} > $V_{IT(PGx)}$, V_{PGx} = 6.5 V			1	µA
$I_{NR/SSx}$	NR/SSx pin charging current	$V_{NR/SSx}$ = GND, 1.4 V ≤ V_{INx} ≤ 6.5 V, V_{SS_CTRLx} = GND	4.0	6.2	9.0	µA
		$V_{NR/SSx}$ = GND, 1.4 V ≤ V_{INx} ≤ 6.5 V, V_{SS_CTRLx} = V_{INx}	65	100	150	
I_{FBx}	FBx pin leakage current	V_{INx} = 6.5 V, V_{FBx} = 0.8 V	–100		100	nA
PSRR	Power-supply rejection ratio	f = 500 kHz, V_{INx} = 3.8 V, V_{OUTx} = 3.3 V, I_{OUTx} = 250 mA, $C_{NR/SSx}$ = 10 nF, C_{FFx} = 10 nF		40		dB
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, V_{INx} = 1.8 V, V_{OUTx} = 0.8 V, I_{OUTx} = 1 A, $C_{NR/SSx}$ = 1 µF, C_{FFx} = 100 nF		3.8		μV_{RMS}
	Noise spectral density	f = 10 kHz, V_{INx} = 1.8 V, V_{OUTx} = 0.8 V, I_{OUTx} = 1 A, $C_{NR/SSx}$ = 10 nF, C_{FFx} = 10 nF		11		$nV/\sqrt{Hz}$
R_{diss}	Output active discharge resistance	V_{ENx} = GND		250		Ω
T_{sdx}	Thermal shutdown temperature	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		

(1) Lowercase x indicates that the specification under consideration applies to both channel 1 and channel 2.
(2) When the device is connected to external feedback resistors at the FBx pins, external resistor tolerances are not included.

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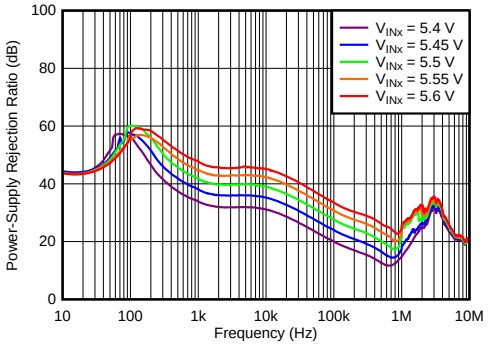
6.6 Typical Characteristics

at T_J = 25°C, 1.4 V ≤ V_{INx} < 6.5 V, V_{INx} ≥ $V_{OUTx(TARGET)}$ + 0.3 V, V_{OUTx} = 0.8 V, SS_CTRLx = GND, I_{OUTx} = 5 mA, V_{ENx} = 1.1 V, C_{OUTx} = 22 µF, $C_{NR/SSx}$ = 0 nF, C_{FFx} = 0 nF, PGx pin pulled up to V_{OUTx} with 100 kΩ, and SS_CTRLx = GND (unless otherwise noted)



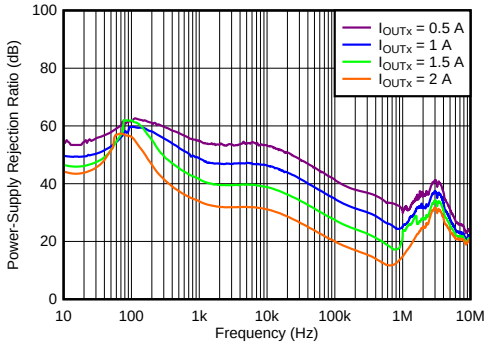
V_{OUTx} = 5 V, V_{INx} = 5.5 V, V_{ENx} = V_{INx}, I_{OUTx} = 2 A, C_{OUTx} = 22 µF, C_{FFx} = 10 nF

图 1. Power-Supply Rejection Ratio vs Frequency and $C_{NR/SSx}$



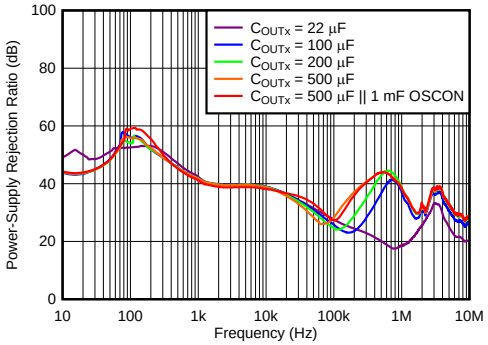
V_{OUTx} = 5 V, I_{OUTx} = 2 A, C_{OUTx} = 22 µF, $C_{NR/SSx}$ = C_{FFx} = 10 nF

图 2. Power-Supply Rejection Ratio vs Frequency and Input Voltage



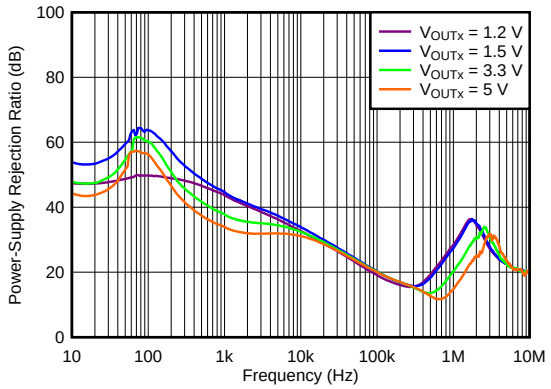
V_{OUTx} = 5 V, V_{INx} = 5.4 V, V_{ENx} = V_{INx}, C_{OUTx} = 22 µF, $C_{NR/SSx}$ = C_{FFx} = 10 nF

图 3. Power-Supply Rejection Ratio vs Frequency and Output Current



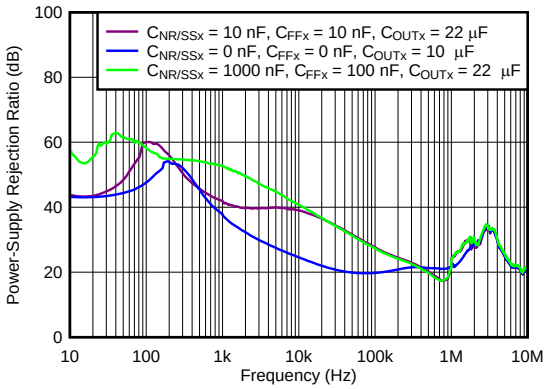
V_{OUTx} = 5.0 V, V_{INx} = 5.5 V, V_{ENx} = V_{INx}, I_{OUTx} = 2 A, C_{OUTx} = ceramic, $C_{NR/SSx}$ = C_{FFx} = 10 nF

图 4. Power-Supply Rejection Ratio vs Frequency and Output Capacitance



V_{INx} = V_{OUTx} + 0.4 V, I_{OUTx} = 2.0 A, C_{OUTx} = 22 µF, $C_{NR/SSx}$ = C_{FFx} = 10 nF

图 5. Power-Supply Rejection Ratio vs Frequency and Output Voltage

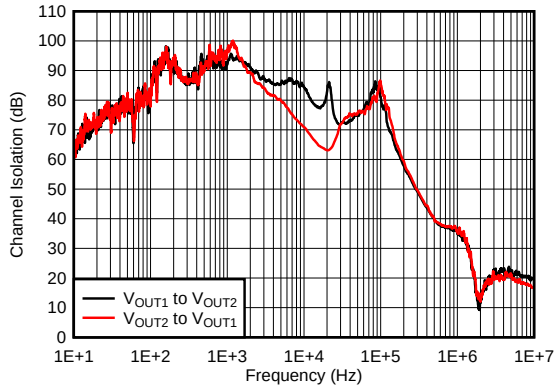


I_{OUTx} = 2 A, V_{INx} = 5.5 V

图 6. Power-Supply Rejection Ratio at V_{OUTx} = 5.0 V

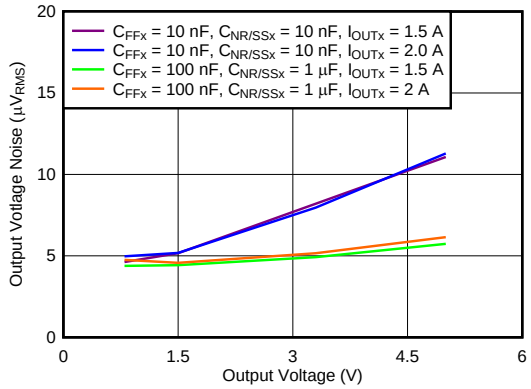
Typical Characteristics (接下页)

at T_J = 25°C, 1.4 V ≤ V_{INx} < 6.5 V, V_{INx} ≥ $V_{OUTx(TARGET)}$ + 0.3 V, V_{OUTx} = 0.8 V, SS_CTRLx = GND, I_{OUTx} = 5 mA, V_{ENx} = 1.1 V, C_{OUTx} = 22 µF, $C_{NR/SSx}$ = 0 nF, C_{FFx} = 0 nF, PGx pin pulled up to V_{OUTx} with 100 kΩ, and SS_CTRLx = GND (unless otherwise noted)



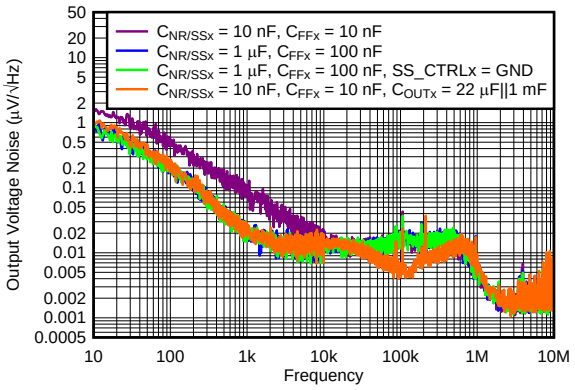
V_{OUTx} = 1.8 V, I_{OUTx} = 100 mA, C_{OUTx} = 22 µF, $C_{NR/SSx}$ = C_{FFx} = 10 nF

图 7. Channel-to-Channel Output Voltage Isolation vs Frequency



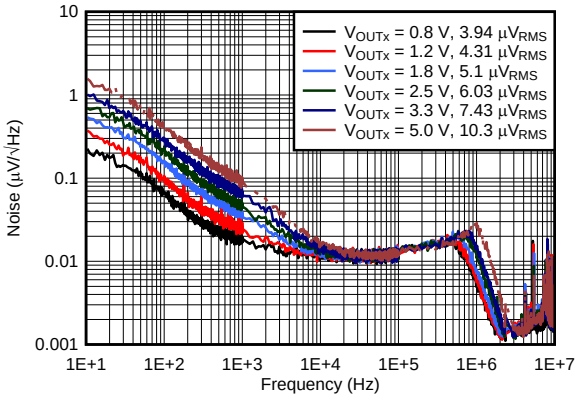
V_{INx} = V_{OUTx} + $V_{DOx(max)}$ + 0.1 V or 1.4 V (whichever is greater), I_{OUTx} = 2 A

图 8. Output Noise vs Output Voltage



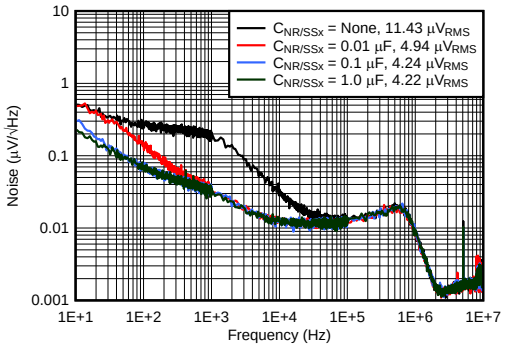
I_{OUTx} = 2 A, V_{INx} = 5.5 V

图 9. Output Noise at V_{OUTx} = 5 V



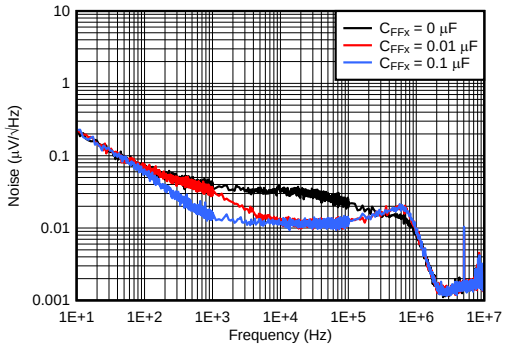
V_{INx} = V_{OUTx} + 1.0 V, I_{OUTx} = 1 A, V_{RMS} BW = 22 Hz to 100 kHz, C_{OUTx} = 10 µF, $C_{NR/SSx}$ = C_{FFx} = 10 nF

图 10. Noise vs Frequency and Output Voltage



V_{INx} = 1.7 V, V_{OUTx} = 1.2 V, I_{OUTx} = 1 A, V_{RMS} BW = 22 Hz to 100 kHz, C_{OUTx} = 10 µF, C_{FFx} = 10 nF

图 11. Noise vs Frequency and $C_{NR/SSx}$



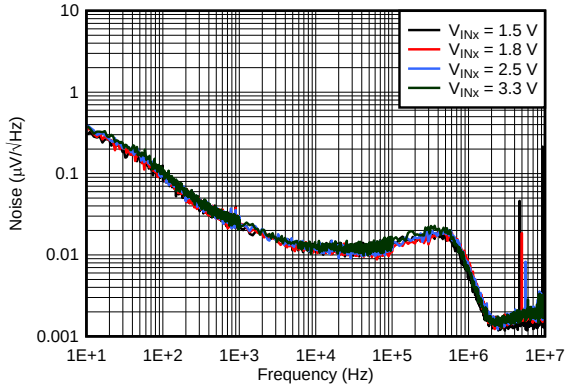
V_{INx} = 3.8 V, V_{OUTx} = 3.3 V, I_{OUTx} = 1 A, V_{RMS} BW = 22 Hz to 100 kHz, C_{OUTx} = 10 µF, $C_{NR/SSx}$ = 10 nF

图 12. Noise vs Frequency and C_{FFx}

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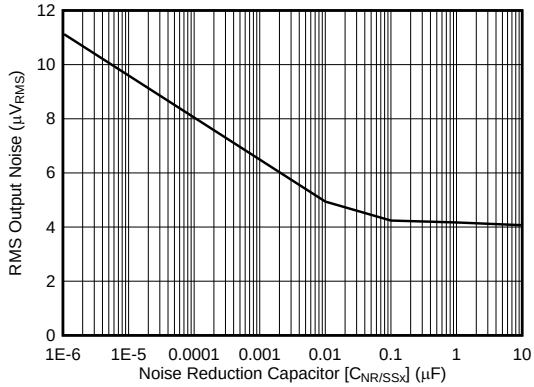
Typical Characteristics (接下页)

at T_J = 25°C, 1.4 V ≤ V_{INx} < 6.5 V, V_{INx} ≥ $V_{OUTx(TARGET)}$ + 0.3 V, V_{OUTx} = 0.8 V, SS_CTRLx = GND, I_{OUTx} = 5 mA, V_{ENx} = 1.1 V, C_{OUTx} = 22 µF, $C_{NR/SSx}$ = 0 nF, C_{FFx} = 0 nF, PGx pin pulled up to V_{OUTx} with 100 kΩ, and SS_CTRLx = GND (unless otherwise noted)



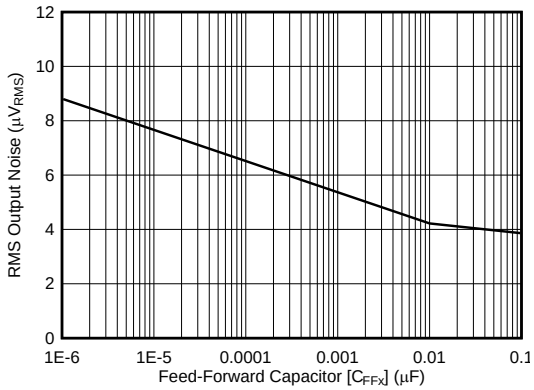
V_{OUTx} = 1.2 V, I_{OUTx} = 1 A, C_{OUTx} = 22 µF, $C_{NR/SSx}$ = 10 nF

图 13. Noise vs Frequency and V_{INx}



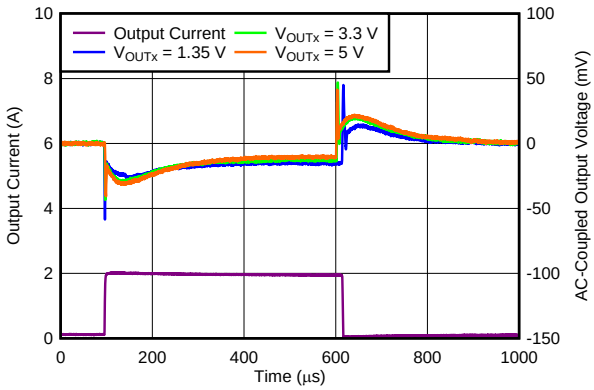
V_{OUTx} = 1.8 V, I_{OUTx} = 1 A, C_{OUTx} = 22 µF, C_{FFx} = 0.01 µF, BW = 10 Hz to 100 kHz

图 14. RMS Output Noise vs $C_{NR/SSx}$



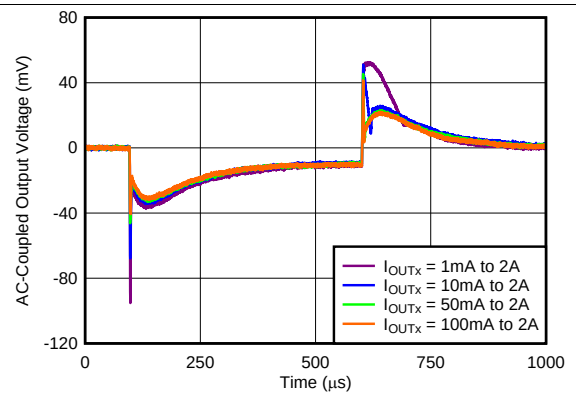
V_{OUTx} = 1.8 V, I_{OUTx} = 1 A, C_{OUTx} = 22 µF, $C_{NR/SSx}$ = 1 µF, BW = 10 Hz to 100 kHz

图 15. RMS Output Noise vs C_{FFx}



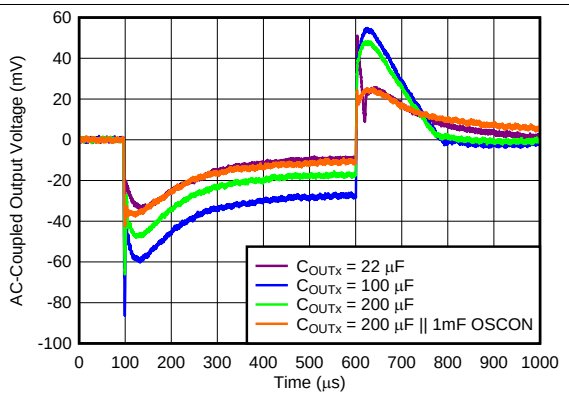
V_{INx} = V_{OUTx} + 0.5 V, I_{OUTx} = 100 mA to 2 A, C_{OUTx} = 22 µF, C_{FFx} = $C_{NR/SSx}$ = 10 nF, slew rate = 1 A/µs

图 16. Load Transient Response vs V_{OUTx}



V_{INx} = 5.5 V, V_{OUTx} = 5 V, C_{OUTx} = 22 µF, C_{FFx} = $C_{NR/SSx}$ = 10 nF, slew rate = 1 A/µs

图 17. Load Transient Response vs DC Load

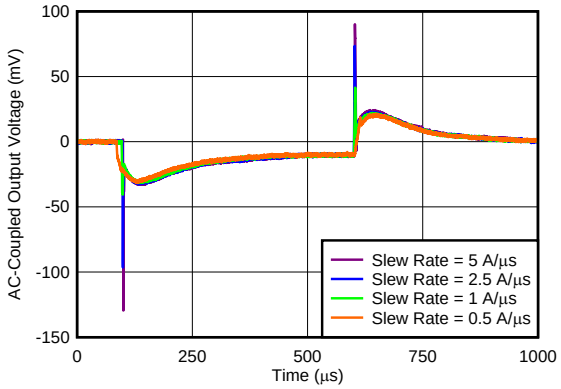


V_{INx} = 5.5 V, V_{OUTx} = 5 V, I_{OUTx} = 100 mA to 2 A, C_{FFx} = $C_{NR/SSx}$ = 10 nF, slew rate = 1 A/µs

图 18. Load Transient Response vs Output Capacitor

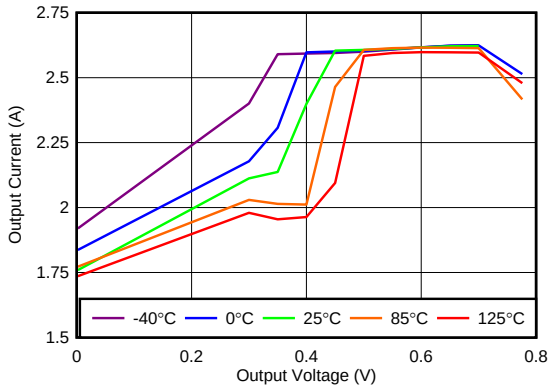
Typical Characteristics (接下页)

at T_J = 25°C, 1.4 V ≤ V_{INx} < 6.5 V, V_{INx} ≥ $V_{OUTx(TARGET)}$ + 0.3 V, V_{OUTx} = 0.8 V, SS_CTRLx = GND, I_{OUTx} = 5 mA, V_{ENx} = 1.1 V, C_{OUTx} = 22 µF, $C_{NR/SSx}$ = 0 nF, C_{FFx} = 0 nF, PGx pin pulled up to V_{OUTx} with 100 kΩ, and SS_CTRLx = GND (unless otherwise noted)



V_{INx} = 5.5 V, V_{OUTx} = 5 V, I_{OUTx} = 100 mA to 2 A, C_{OUTx} = 22 µF, C_{FFx} = $C_{NR/SSx}$ = 10 nF

图 19. Load Transient Response vs Slew Rate



V_{INx} = 1.4 V, V_{OUTx} = 0.8 V

图 20. Current Limit Foldback

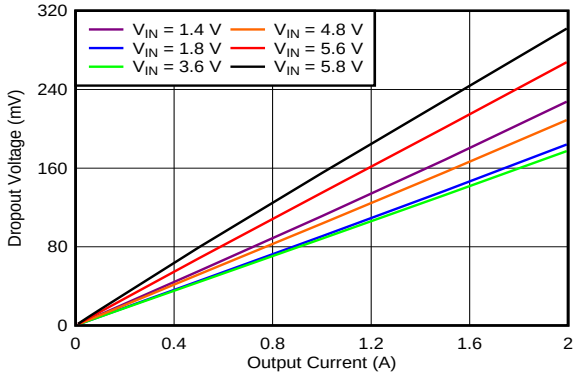


图 21. Dropout Voltage vs Output Current

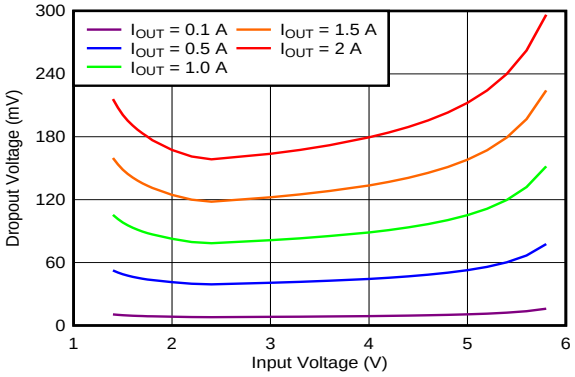


图 22. Dropout Voltage vs Input Voltage

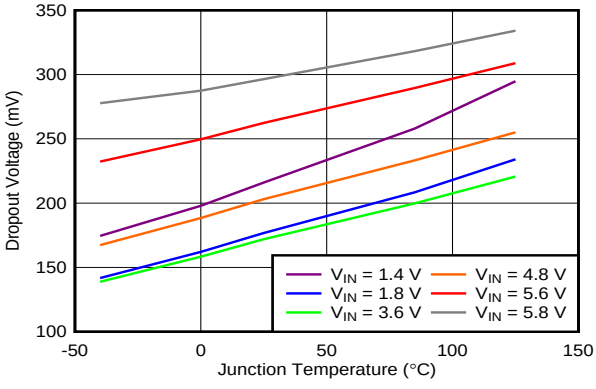


图 23. Dropout Voltage vs Junction Temperature

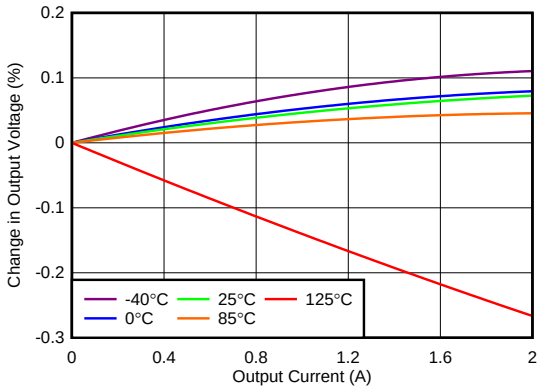
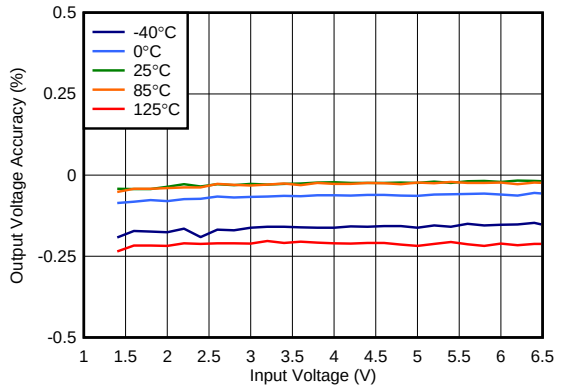


图 24. Load Regulation (V_{OUTx} = 1.2 V)

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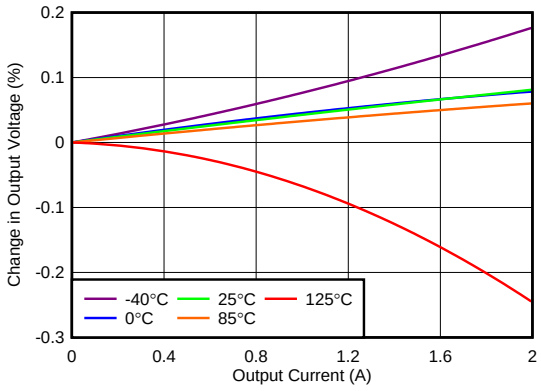
Typical Characteristics (接下页)

at T_J = 25°C, 1.4 V ≤ V_{INx} < 6.5 V, V_{INx} ≥ $V_{OUTx(TARGET)}$ + 0.3 V, V_{OUTx} = 0.8 V, SS_CTRLx = GND, I_{OUTx} = 5 mA, V_{ENx} = 1.1 V, C_{OUTx} = 22 µF, $C_{NR/SSx}$ = 0 nF, C_{FFx} = 0 nF, PGx pin pulled up to V_{OUTx} with 100 kΩ, and SS_CTRLx = GND (unless otherwise noted)



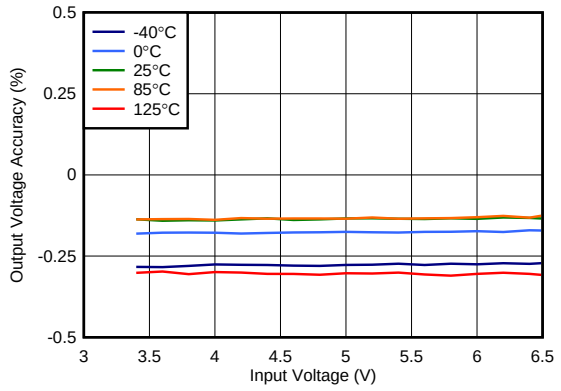
I_{OUTx} = 50 mA

图 25. Line Regulation (V_{OUTx} = 0.8 V)



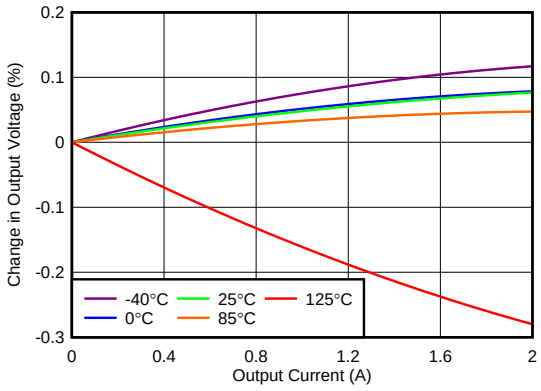
V_{INx} = 3.8 V

图 26. Load Regulation (V_{OUTx} = 3.3 V)



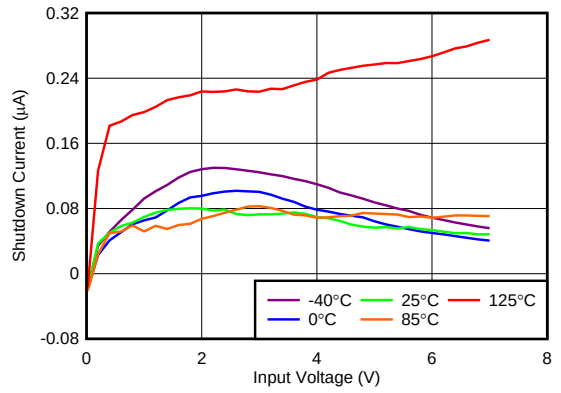
I_{OUTx} = 5 mA

图 27. Line Regulation (V_{OUTx} = 3.3 V)



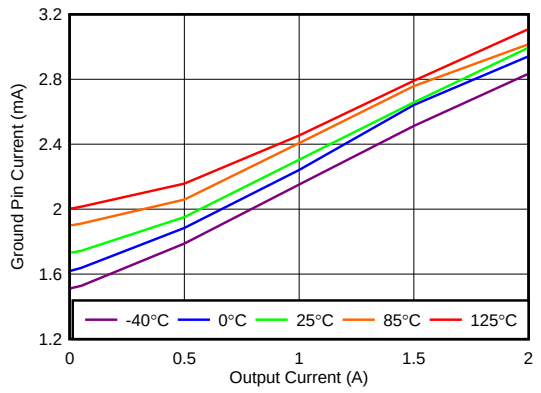
V_{INx} = 5.5 V

图 28. Load Regulation (V_{OUTx} = 5.0 V)



Single Channel

图 29. Shutdown Current vs Input Voltage



V_{INx} = 1.4 V, Single Channel

图 30. Ground Current vs Output Current

Typical Characteristics (接下页)

at T_J = 25°C, 1.4 V ≤ V_{INx} < 6.5 V, V_{INx} ≥ $V_{OUTx(TARGET)}$ + 0.3 V, V_{OUTx} = 0.8 V, SS_CTRLx = GND, I_{OUTx} = 5 mA, V_{ENx} = 1.1 V, C_{OUTx} = 22 µF, $C_{NR/SSx}$ = 0 nF, C_{FFx} = 0 nF, PGx pin pulled up to V_{OUTx} with 100 kΩ, and SS_CTRLx = GND (unless otherwise noted)

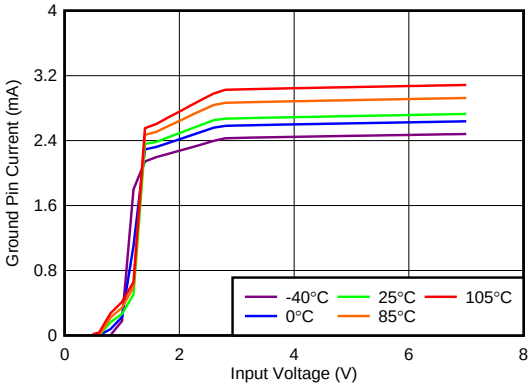


图 31. Ground Current vs Input Voltage

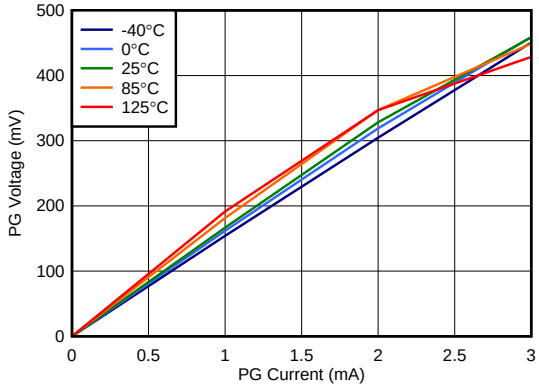


图 32. PGx Low Level vs PGx Current (V_{INx} = 1.4 V)

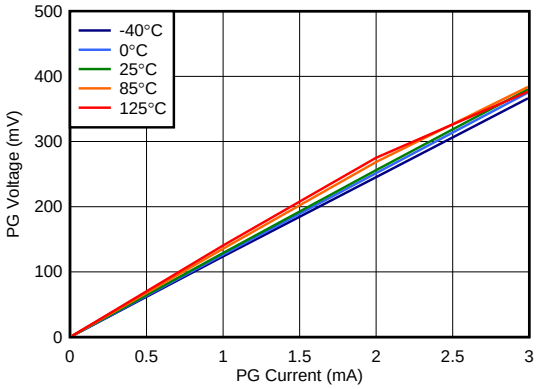


图 33. PGx Low Level vs PGx Current (V_{INx} = 6.5 V)

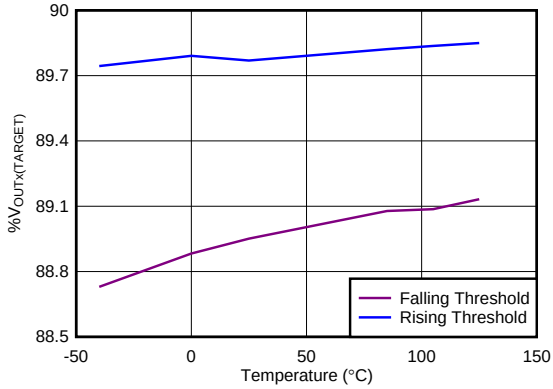


图 34. PGx Threshold vs Temperature

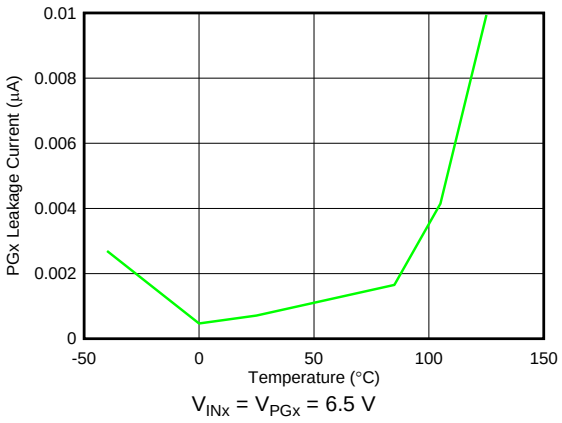


图 35. PGx Leakage Current vs Temperature

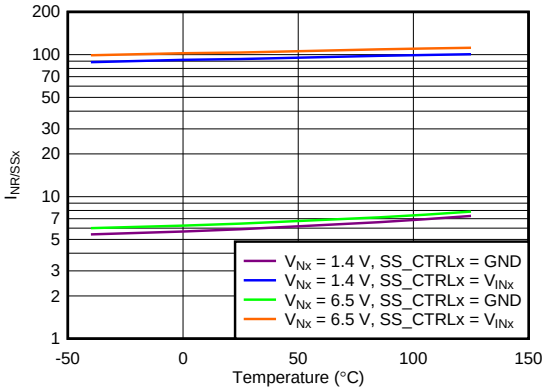


图 36. Soft-Start Current vs Temperature (SS_CTRLx = GND)

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Typical Characteristics (接下页)

at T_J = 25°C, 1.4 V ≤ V_{INx} < 6.5 V, V_{INx} ≥ $V_{OUTx(TARGET)}$ + 0.3 V, V_{OUTx} = 0.8 V, SS_CTRLx = GND, I_{OUTx} = 5 mA, V_{ENx} = 1.1 V, C_{OUTx} = 22 µF, $C_{NR/SSx}$ = 0 nF, C_{FFx} = 0 nF, PGx pin pulled up to V_{OUTx} with 100 kΩ, and SS_CTRLx = GND (unless otherwise noted)

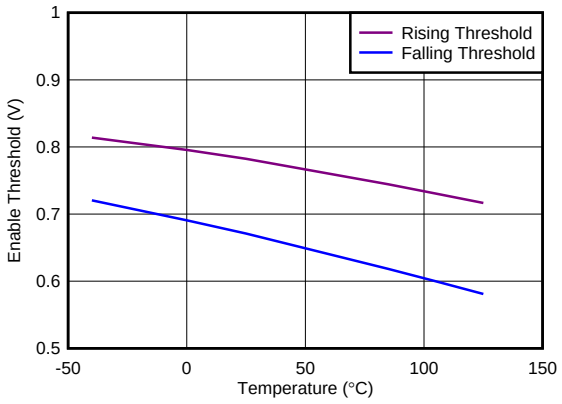


图 37. Enable Threshold vs Temperature

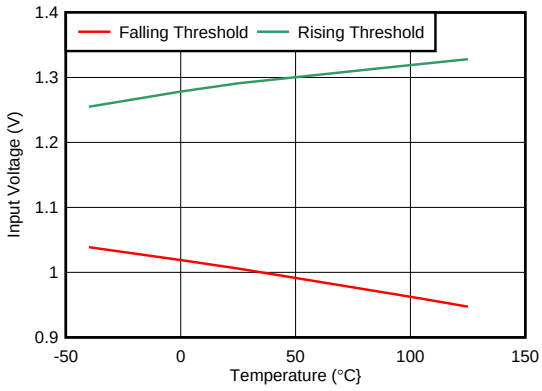
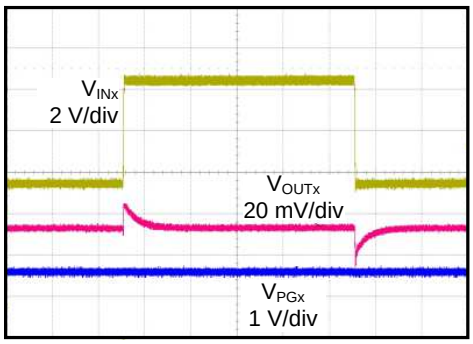
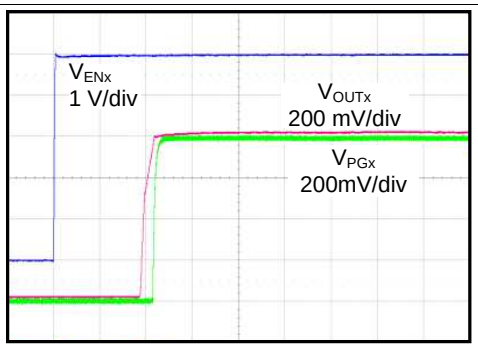


图 38. Input UVLOx Threshold vs Temperature



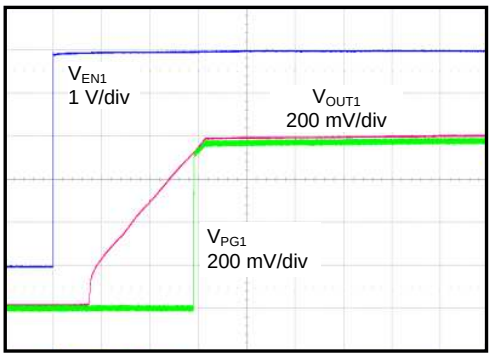
Time (200 µs/div)
V_{INx} = 1.4 V to 6.5 V to 1.4 V at 2 V/µs, V_{OUTx} = 0.8 V,
I_{OUTx} = 1 A, $C_{NR/SSx}$ = C_{FFx} = 10 nF

图 39. Line Transient



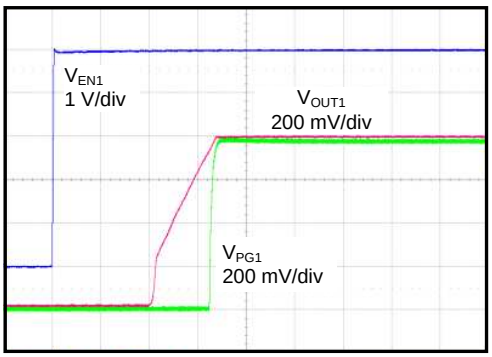
Time (50 µs/div)
V_{INx} = 1.4 V

图 40. Start-Up (SS_CTRLx = GND, $C_{NR/SSx}$ = 0 nF)



Time (500 µs/div)
V_{INx} = 1.4 V

图 41. Start-Up (SS_CTRLx = GND, $C_{NR/SSx}$ = 10 nF)

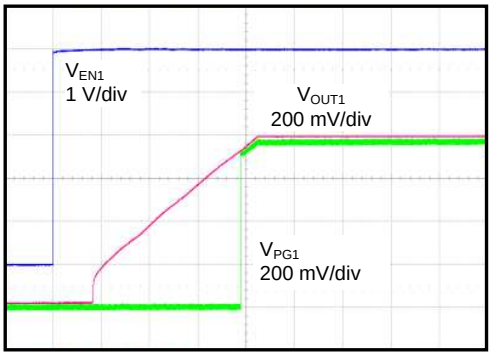


Time (50 µs/div)
V_{INx} = 1.4 V

图 42. Start-Up (SS_CTRLx = V_{INx}, $C_{NR/SSx}$ = 10 nF)

Typical Characteristics (接下页)

at T_J = 25°C, 1.4 V ≤ V_{INx} < 6.5 V, V_{INx} ≥ $V_{OUTx(TARGET)}$ + 0.3 V, V_{OUTx} = 0.8 V, SS_CTRLx = GND, I_{OUTx} = 5 mA, V_{ENx} = 1.1 V, C_{OUTx} = 22 µF, $C_{NR/SSx}$ = 0 nF, C_{FFx} = 0 nF, PGx pin pulled up to V_{OUTx} with 100 kΩ, and SS_CTRLx = GND (unless otherwise noted)



Time (2 ms/div)
V_{INx} = 1.4 V

图 43. Start-Up (SS_CTRLx = V_{INx}, $C_{NR/SSx}$ = 1 µF)

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7 Detailed Description

7.1 Overview

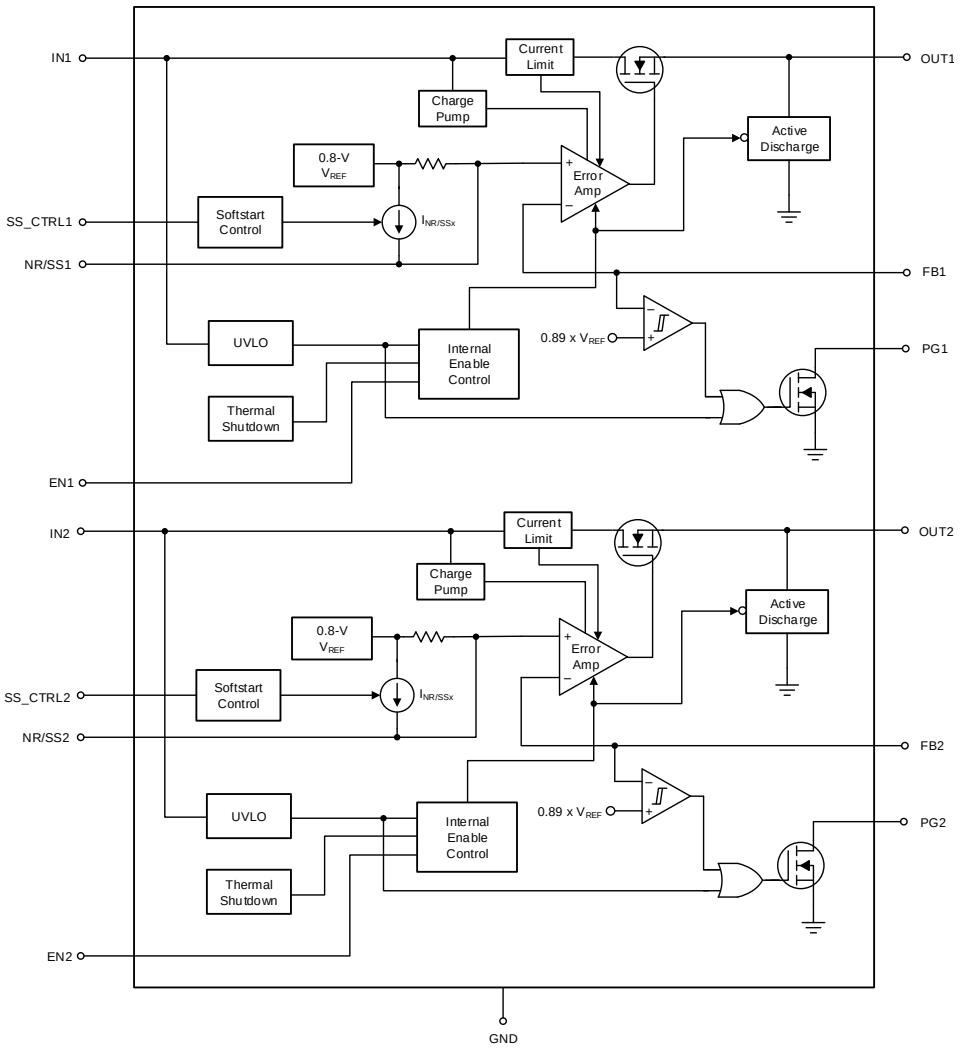
The TPS7A89 is a monolithic, dual-channel, low-dropout (LDO) regulator. Each channel is low-noise, high-PSRR, and capable of sourcing a 2-A load with 400 mV of maximum dropout. These features make the device a robust solution to solve many challenging problems in generating a clean, accurate power supply.

The various features for each of the TPS7A89 fully independent LDOs simplify using the device in a variety of applications. As detailed in the *Functional Block Diagram* section, these features are organized into three categories, as shown in 表 1.

表 1. Features

VOLTAGE REGULATION	SYSTEM START-UP	INTERNAL PROTECTION
High accuracy	Programmable soft-start	Foldback current limit
Low-noise, high-PSRR output	Sequencing controls	Thermal shutdown
Fast transient response	Power-good output	

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Voltage Regulation Features

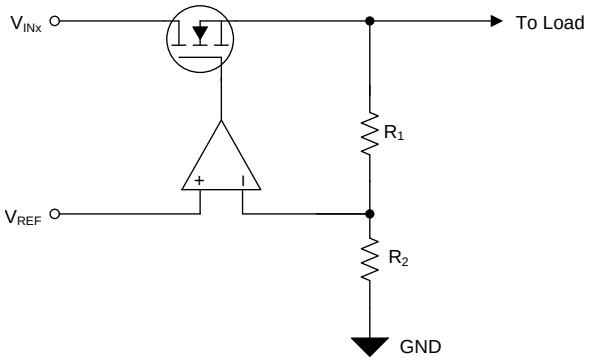
7.3.1.1 DC Regulation

An LDO functions as a class-B amplifier in which the input signal is the internal reference voltage (V_{REF}), as shown in 图 44. V_{REF} is designed to have a very low-bandwidth at the input to the error amplifier through the use of a low-pass filter ($V_{NR/SSx}$).

As such, the reference can be considered as a pure dc input signal. The low output impedance of an LDO comes from the combination of the output capacitor and pass element. The pass element also presents a high input impedance to the source voltage when operating as a current source. A positive LDO can only source current because of the class-B architecture.

This device achieves a maximum of 1% output voltage accuracy primarily because of the high-precision band-gap voltage (V_{BG}) that creates V_{REF}. The low dropout voltage (V_{DO}) reduces the thermal power dissipation required by the device to regulate the output voltage at a given current level, thereby improving system efficiency. Combined, these features help make this device a good approximation of an ideal voltage source.

This device replaces two stand-alone power-supplies, and also provides load-to-load isolation. The LDOs can also be put in series (cascaded) to achieve even higher PSRR by connecting the output of one channel to the input of the other channel.



NOTE: $V_{OUTx} = V_{REF} \times (1 + R_{1x} / R_{2x})$.

图 44. Simplified Regulation Circuit

7.3.1.2 AC and Transient Response

Each LDO responds quickly to a transient (large-signal response) on the input supply (line transient) or the output current (load transient) resulting from the LDO high-input impedance and low output-impedance across frequency. This same capability also means that each LDO has a high power-supply rejection-ratio (PSRR) and, when coupled with a low internal noise-floor (V_n), the LDO approximates an ideal power supply in ac (small-signal) and large-signal conditions.

The performance and internal layout of the device minimizes the coupling of noise from one channel to the other channel (crosstalk). Good printed circuit board (PCB) layout minimizes the crosstalk.

The choice of external component values optimizes the small- and large-signal response. The NR/SSx capacitor ($C_{NR/SSx}$) and feed-forward capacitor (C_{FFx}) easily reduce the device noise floor and improve PSRR; see the *Optimizing Noise and PSRR* section for more information on optimizing the noise and PSRR performance.

7.3.2 System Start-Up Features

In many different applications, the power-supply output must turn-on within a specific window of time to either ensure proper operation of the load or to minimize the loading on the input supply or other sequencing requirements. Each LDO start-up is well-controlled and user-adjustable, solving the demanding requirements faced by many power-supply design engineers in a simple fashion.

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Feature Description (接下页)

7.3.2.1 Programmable Soft-Start (NR/SSx)

Soft-start directly controls the output start-up time and indirectly controls the output current during start-up (in-rush current).

The external capacitor at the NR/SSx pin ($C_{NR/SSx}$) sets the output start-up time by setting the rise time of the internal reference ($V_{NR/SSx}$), as shown in 图 45. SS_CTRLx provides additional control over the rise time of the internal reference by enabling control over the charging current ($I_{NR/SSx}$) for $C_{NR/SSx}$. The voltage at the SS_CTRLx pin (V_{SS_CTRLx}) must be connected to ground (GND) or V_{INx}.

Note that if $C_{NR/SSx}$ = 0 nF and the SS_CTRLx pin is connected to V_{INx}, then the output voltage overshoots during start-up.

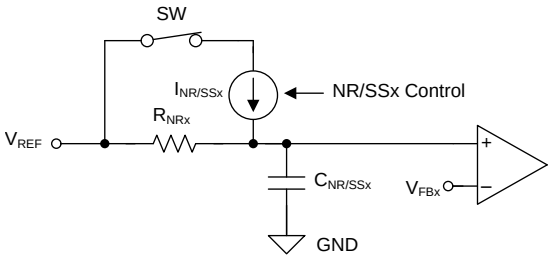


图 45. Simplified Soft-Start Circuit

7.3.2.2 Sequencing

Controlling when a single power supply turns on can be difficult in a power distribution network (PDN) because of the high power levels inherent in a PDN, and the variations between all of the supplies. Control of each channel turn-on and turn-off time is set by the specific channel enable circuit (ENx) and undervoltage lockout circuit (UVLOx), as shown in 图 46 and 表 2.

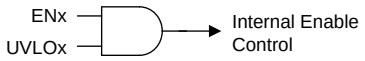


图 46. Simplified Turn-On Control

表 2. Sequencing Functionality Table

INPUT VOLTAGE	ENABLE STATUS	LDO STATUS	ACTIVE DISCHARGE	POWER-GOOD
$V_{INx} \geq V_{UVLOx}$	ENx = 1	On	Off	PGx = 1 when $V_{OUTx} \geq V_{IT(PGx)}$
	ENx = 0	Off	On	PGx = 0
$V_{INx} < V_{UVLOx} - V_{HYS}$	ENx = don't care	Off	On(1)	PGx = 0

(1) The active discharge remains on as long as V_{INx} provides enough headroom for the discharge circuit to function.

7.3.2.2.1 Enable (ENx)

The enable signal (V_{ENx}) is an active-high digital control that enables the LDO when the enable voltage is past the rising threshold ($V_{ENx} \geq V_{IH(ENx)}$) and disables the LDO when the enable voltage is below the falling threshold ($V_{ENx} \leq V_{IL(ENx)}$). The exact enable threshold is between $V_{IH(ENx)}$ and $V_{IL(ENx)}$ because ENx is a digital control. In applications that do not use the enable control, connect ENx to V_{INx}.

7.3.2.2.2 Undervoltage Lockout (UVLOx) Control

The UVLOx circuit responds quickly to glitches on V_{INx} and attempts to disable the output of the device if either of these rails collapse.

As a result of the fast response time of the input supply UVLOx circuit, fast and short line transients well below the input supply UVLOx falling threshold (brownouts) can cause momentary glitches during the edges of the transient. These glitches are typical in most LDOs. The local input capacitance prevents severe brown-outs in most applications; see the *Undervoltage Lockout (UVLOx) Control* section for more details.

7.3.2.2.3 Active Discharge

When either ENx or UVLOx is low, the device connects a resistor of several hundred ohms from V_{OUTx} to GND, discharging the output capacitance.

Do not rely on the active discharge circuit for discharging large output capacitors when the input voltage drops below the targeted output voltage. Current flows from the output to the input (reverse current) when $V_{OUTx} > V_{INx}$, which can cause damage to the device (when $V_{OUTx} > V_{INx} + 0.3$ V); see the *Reverse Current Protection* section for more details.

7.3.2.3 Power-Good Output (PGx)

The PGx signal provides an easy solution to meet demanding sequencing requirements because PGx signals when the output nears its nominal value. PGx can be used to signal other devices in a system when the output voltage is near, at, or above the set output voltage ($V_{OUTx(Target)}$). A simplified schematic is shown in 图 47.

The PGx signal is an open-drain digital output that requires a pullup resistor to a voltage source and is active high. The power-good circuit sets the PGx pin into a high-impedance state to indicate that the power is good.

Using a large feed-forward capacitor (C_{FFx}) delays the output voltage and, because the power-good circuit monitors the FBx pin, the PGx signal can indicate a false positive. A simple solution to this scenario is to use an external voltage detector device, such as the TPS3780; see the *Feed-Forward Capacitor (C_{FFx})* section for more information.

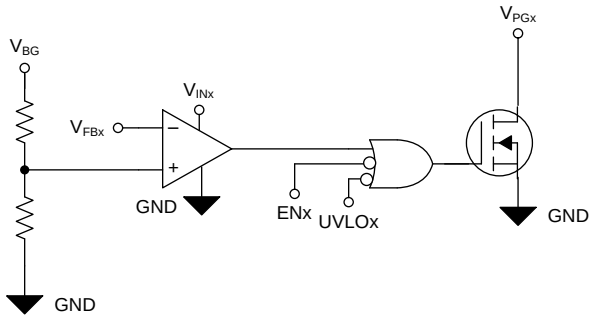


图 47. Simplified PGx Circuit

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7.3.3 Internal Protection Features

In many applications, fault events can occur that damage devices in the system. Short-circuits and excessive heat are the most common fault events for power supplies. The TPS7A89 implements circuitry for each LDO to protect the device and its load during these events. Continuously operating in these fault conditions or above a junction temperature of 125°C is not recommended because the long-term reliability of the device is reduced.

7.3.3.1 Foldback Current Limit (I_{CLx})

The internal current limit circuit protects the LDO against short-circuit and excessive load current conditions. The output current decreases (folds back) when the output voltage falls to better protect the device, as described in 图 20. Each channel features its own independent current limit circuit.

7.3.3.2 Thermal Protection (T_{sdx})

The thermal shutdown circuit protects the LDO against excessive heat in the system, either resulting from current limit or high ambient temperature. Each channel features its own independent thermal shutdown circuit.

The output of the LDO turns off when the LDO temperature (junction temperature, T_J) exceeds the rising thermal shutdown temperature (T_{sdx}). The output turns on again after T_J decreases below the falling thermal shutdown temperature (T_{sdx}).

A high power dissipation across the device, combined with a high ambient temperature (T_A), can cause T_J to be greater than or equal to T_{sdx}, triggering the thermal shutdown and causing the output to fall to 0 V. The LDO can cycle on and off when thermal shutdown is reached under these conditions.

7.4 Device Functional Modes

表 3 provides a quick comparison between the regulation and disabled operation.

表 3. Device Functional Modes Comparison

OPERATING MODE	PARAMETER			
	V_{INx}	ENx	I_{OUTx}	T_J
Regulation(1)	$V_{INx} > V_{OUTx(nom)} + V_{DO}$	$V_{ENx} > V_{IH(ENx)}$	$I_{OUTx} < I_{CLx}$	$T_J < T_{sd}$
Disabled(2)	$V_{INx} < V_{UVLOx}$	$V_{ENx} < V_{IL(ENx)}$	—	$T_J > T_{sd}$

(1) All table conditions must be met.
(2) The device is disabled when any condition is met.

7.4.1 Regulation

The device regulates the output to the targeted output voltage when all the conditions in 表 3 are met.

7.4.2 Disabled

When disabled, the pass device is turned off, the internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal resistor from the output to ground.

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8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

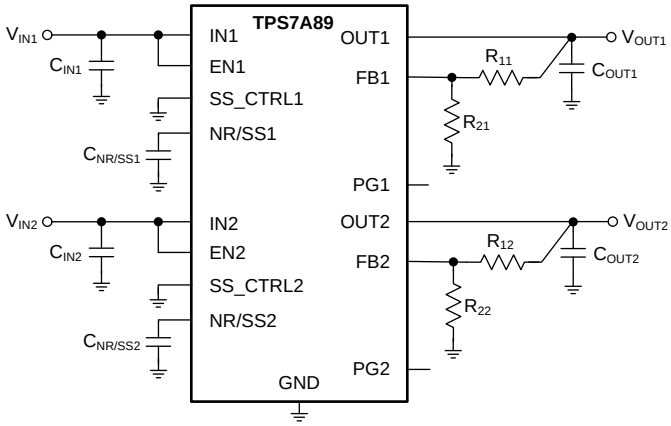
8.1 Application Information

Successfully implementing an LDO in an application depends on the application requirements. This section discusses key device features and how to best implement them to achieve a reliable design.

8.1.1 External Component Selection

8.1.1.1 Setting the Output Voltage (Adjustable Operation)

Each LDO resistor feedback network sets the output voltage, as shown in 图 48, with an output voltage range of 0.8 V to 5.2 V.



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图 48. Adjustable Operation

公式 1 relates the values R_{1x} and R_{2x} to $V_{OUTx(Target)}$ and V_{FBx}. 公式 1 is a rearranged version of 公式 2, simplifying the feedback resistor calculation. The current through the feedback network must be equal to or greater than 5 μA for optimum noise performance and accuracy, as shown in 公式 3.

$$V_{OUTx} = V_{FBx} \times (1 + R_{1x} / R_{2x}) \quad (1)$$

$$R_{1x} = (V_{OUTx} / V_{FBx} - 1) \times R_{2x} \quad (2)$$

$$R_{2x} < V_{REF} / 5\ \mu A \quad (3)$$

The input bias current into the error amplifier (feedback pin current, I_{FBx}) and tighter tolerance resistors must be taken into account for optimizing the output voltage accuracy.

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Application Information (接下页)

表 4 shows the resistor combinations for several common output voltages using commercially-available, 1% tolerance resistors.

表 4. Recommended Feedback-Resistor Values

TARGETED OUTPUT VOLTAGE (V)	FEEDBACK RESISTOR VALUES(1)		CALCULATED OUTPUT VOLTAGE (V)
	R_{1x} (kΩ)	R_{2x} (kΩ)	
0.80	Short	Open	0.800
0.90	1.37	11.0	0.900
0.95	1.91	10.2	0.950
1.00	2.55	10.2	1.000
1.05	3.32	10.7	1.048
1.10	3.57	9.53	1.100
1.15	4.64	10.7	1.147
1.20	5.49	11.0	1.199
1.35	6.98	10.2	1.347
1.50	9.31	10.7	1.496
1.80	13.70	11.0	1.796
1.90	14.70	10.7	1.899
2.50	22.60	10.7	2.490
2.85	27.40	10.7	2.849
3.00	29.40	10.7	2.998
3.30	33.20	10.7	3.282
3.60	35.70	10.2	3.600
4.50	44.20	9.53	4.510
5.00	56.20	10.7	5.002
5.20	53.60	9.76	5.193

(1) R_{1x} is connected from OUTx to FBx; R_{2x} is connected from FBx to GND; see 图 48.

8.1.1.2 Capacitor Recommendations

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output pins. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, ceramic capacitance varies with operating voltage and temperature. As a rule of thumb, derate ceramic capacitors by at least 50%. The input and output capacitors recommended herein account for an effective capacitance derating of approximately 50%, but at higher V_{INx} and V_{OUTx} conditions (that is, V_{INx} = 5.5 V to V_{OUTx} = 5.0 V) the derating can be greater than 50% and must be taken into consideration.

8.1.1.3 Input and Output Capacitor (C_{INx} and C_{OUTx})

The device is designed and characterized for operation with ceramic capacitors of 22 µF or greater (10 µF or greater of effective capacitance) at each input and output. Locate the input and output capacitors as near as practical to the respective input and output pins to minimize the trace inductance from the capacitor to the device.

8.1.1.4 Feed-Forward Capacitor (C_{FFx})

Although a feed-forward capacitor (C_{FFx}) from the FBx pin to the OUTx pin is not required to achieve stability, a 10-nF external C_{FFx} optimizes the transient, noise, and PSRR performance. A higher capacitance C_{FFx} can be used; however, the start-up time is longer and the power-good signal can incorrectly indicate that the output voltage is settled. The maximum recommended value is 100 nF.

To ensure proper PGx functionality, the time constant defined by $C_{NR/SSx}$ must be greater than or equal to the time constant from C_{FFx}. For a detailed description, see the *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator* application report (SBVA042).

8.1.1.5 Noise-Reduction and Soft-Start Capacitor ($C_{NR/SSx}$)

Although a noise-reduction and soft-start capacitor ($C_{NR/SSx}$) from the NR/SSx pin to GND is not required, $C_{NR/SSx}$ is highly recommended to control the start-up time and reduce the noise-floor of the device. The typical value used is 10 nF, and the maximum recommended value is 10 µF.

8.1.2 Start-Up

8.1.2.1 Circuit Soft-Start Control (NR/SSx)

Each output of the device features a user-adjustable, monotonic, voltage-controlled soft-start that is set with an external capacitor ($C_{NR/SSx}$). This soft-start eliminates power-up initialization problems when powering field-programmable gate arrays (FPGAs), digital signal processors (DSPs), or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, thus minimizing start-up transients to the input power bus.

The output voltage (V_{OUTx}) rises proportionally to $V_{NR/SSx}$ during start-up as the LDO regulates so that the feedback voltage equals the NR/SSx voltage ($V_{FBx} = V_{NR/SSx}$). As such, the time required for $V_{NR/SSx}$ to reach its nominal value determines the rise time of V_{OUTx} (start-up time).

The soft-start ramp time depends on the soft-start charging current ($I_{NR/SSx}$), the soft-start capacitance ($C_{NR/SSx}$), and the internal reference (V_{REF}). The approximate soft-start ramp time (t_{SSx}) can be calculated with 公式 4:

$$t_{SSx} = (V_{REF} \times C_{NR/SSx}) / I_{NR/SSx} \quad (4)$$

The SS_CTRLx pin for each output sets the value of the internal current source, maintaining a fast start-up time even with a large $C_{NR/SSx}$ capacitor. When the SS_CTRLx pin is connected to GND, the typical value for the $I_{NR/SSx}$ current is 6.2 µA. Connecting the SS_CTRLx pin to INx increases the typical soft-start charging current to 100 µA. The larger charging current for $I_{NR/SSx}$ is useful when smaller start-up ramp times are needed or when using larger noise-reduction capacitors.

Not using a noise-reduction capacitor on the NR/SSx pin and tying the SS_CTRLx pin to V_{INx} results in output voltage overshoot of approximately 10%. Connecting the SS_CTRLx pin to GND or using a capacitor on the NR/SSx pin minimizes the overshoot.

Values for the soft-start charging currents are provided in the *Electrical Characteristics* table.

8.1.2.1.1 In-Rush Current

In-rush current is defined as the current into the LDO at the INx pin during start-up. In-rush current then consists primarily of the sum of load current and the current used to charge the output capacitor. This current is difficult to measure because the input capacitor must be removed, which is not recommended. However, this soft-start current can be estimated by 公式 5:

$$I_{OUTx}(t) = \left[\frac{C_{OUTx} \times dV_{OUTx}(t)}{dt}\right] + \left[\frac{V_{OUTx}(t)}{R_{LOAD}}\right] \quad (5)$$

where:

- $V_{OUTx}(t)$ is the instantaneous output voltage of the turn-on ramp
- $dV_{OUTx}(t) / dt$ is the slope of the V_{OUTx} ramp
- R_{LOAD} is the resistive load impedance

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8.1.2.2 Undervoltage Lockout (UVLOx) Control

The UVLOx circuit ensures that the device stays disabled before its input or bias supplies reach the minimum operational voltage range, and ensures that the device properly shuts down when the input supply collapses.

图 49 and 表 5 explain the UVLOx circuit response to various input voltage events, assuming $V_{ENx} \geq V_{IH(ENx)}$.

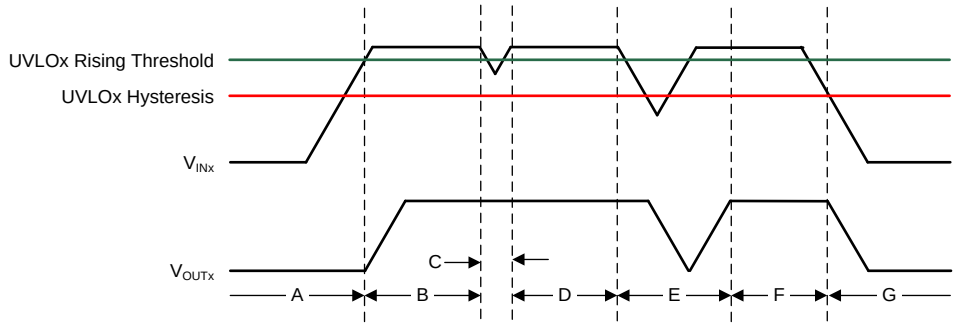


图 49. Typical UVLOx Operation

表 5. Typical UVLOx Operation Description

REGION	EVENT	V_{OUTx} STATUS	COMMENT
A	Turn-on, $V_{INx} \geq V_{UVLOx}$	0	Start-up
B	Regulation	1	Regulates to target V_{OUTx}
C	Brownout, $V_{INx} \geq V_{UVLOx} - V_{HYS}$	1	The output can fall out of regulation but the device is still enabled.
D	Regulation	1	Regulates to target V_{OUTx}
E	Brownout, $V_{INx} < V_{UVLOx} - V_{HYS}$	0	The device is disabled and the output falls because of the load and active discharge circuit. The device is reenabled when the UVLOx rising threshold is reached by the input voltage and a normal start-up then follows.
F	Regulation	1	Regulates to target V_{OUTx}
G	Turn-off, $V_{INx} < V_{UVLOx} - V_{HYS}$	0	The output falls because of the load and active discharge circuit.

Similar to many other LDOs with this feature, the UVLOx circuit takes a few microseconds to fully assert. During this time, a downward line transient below approximately 0.8 V causes the UVLOx to assert for a short time; however, the UVLOx circuit does not have enough stored energy to fully discharge the internal circuits inside of the device. When the UVLOx circuit is not given enough time to fully discharge the internal nodes, the outputs are not fully disabled.

The effect of the downward line transient can be mitigated by using a larger input capacitor to increase the fall time of the input supply when operating near the minimum V_{INx}.

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8.1.2.3 Power-Good (PGx) Function

The power-good circuit monitors the voltage at the feedback pin to indicate the status of the output voltage. The power-good circuit asserts whenever FBx, V_{INx}, or ENx are below their thresholds. The PGx operation versus the output voltage is shown in 图 50, which is described by 表 6.

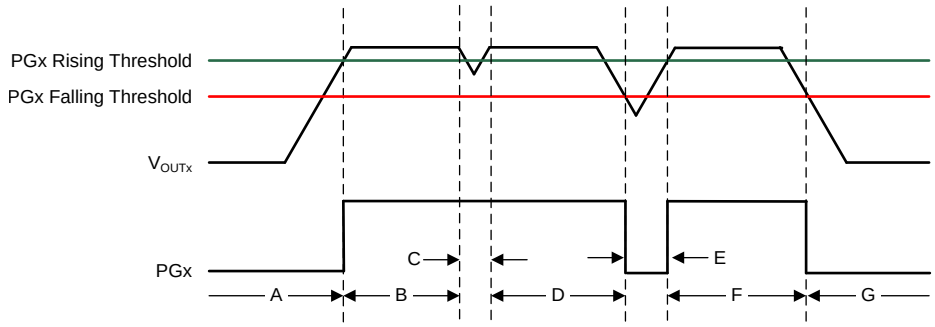


图 50. Typical PGx Operation

表 6. Typical PGx Operation Description

REGION	EVENT	PGx STATUS	FBx VOLTAGE
A	Turn-on	0	$V_{FBx} < V_{IT(PGx)} + V_{HYS(PGx)}$
B	Regulation	Hi-Z	$V_{FBx} \geq V_{IT(PGx)}$
C	Output voltage dip	Hi-Z	
D	Regulation	Hi-Z	
E	Output voltage dip	0	$V_{FBx} < V_{IT(PGx)}$
F	Regulation	Hi-Z	$V_{FBx} \geq V_{IT(PGx)}$
G	Turn-off	0	$V_{FBx} < V_{IT(PGx)}$

The PGx pin is open-drain and connecting a pullup resistor to an external supply enables others devices to receive power-good as a logic signal that can be used for sequencing. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device or devices.

To ensure proper operation of the power-good circuit, the pullup resistor value must be between 10 kΩ and 100 kΩ. The lower limit of 10 kΩ results from the maximum pulldown strength of the power-good transistor, and the upper limit of 100 kΩ results from the maximum leakage current at the power-good node. If the pullup resistor is outside of this range, then the power-good signal may not read a valid digital logic level.

Using a large C_{FFx} with a small $C_{NR/SSx}$ causes the power-good signal to incorrectly indicate that the output voltage has settled during turn-on. The C_{FFx} time constant must be greater than the soft-start time constant to ensure proper operation of the PGx during start-up. For a detailed description, see the *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator* application report (SBVA042).

The state of PGx is only valid when the device operates above the minimum supply voltage. During short brownout events and at light loads, power-good does not assert because the output voltage (therefore V_{FBx}) is sustained by the output capacitance.

8.1.3 AC and Transient Performance

LDO ac performance for a dual-channel device includes power-supply rejection ratio, channel-to-channel output isolation, output current transient response, and output noise. These metrics are primarily a function of open-loop gain, bandwidth, and phase margin that control the closed-loop input and output impedance of the LDO. The output noise is primarily a result of the reference and error amplifier noise.

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8.1.3.1 Power-Supply Rejection Ratio (PSRR)

PSRR is a measure of how well the LDO control-loop rejects signals from V_{INx} to V_{OUTx} across the frequency spectrum (usually 10 Hz to 10 MHz). 公式 6 gives the PSRR calculation as a function of frequency for the input signal [$V_{INx}(f)$] and output signal [$V_{OUTx}(f)$].

$$\text{PSRR (dB)} = 20\,\text{Log}_{10}\left(\frac{V_{INx}(f)}{V_{OUTx}(f)}\right) \tag{6}$$

Even though PSRR is a loss in signal amplitude, PSRR is shown as positive values in decibels (dB) for convenience.

A simplified diagram of PSRR versus frequency is shown in 图 51.

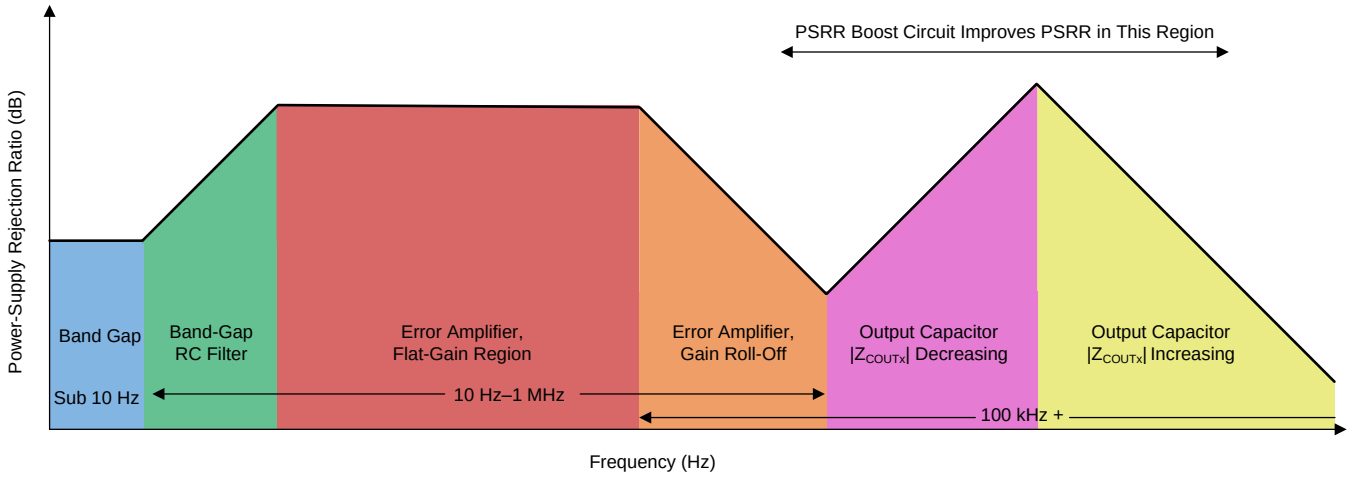


图 51. Power-Supply Rejection Ratio Diagram

An LDO is often employed not only as a dc-dc regulator, but also to provide exceptionally clean power-supply voltages that exhibit ultra-low noise and ripple to sensitive system components. This usage is especially true for the TPS7A89.

The TPS7A89 features an innovative circuit to boost the PSRR between 200 kHz and 1 MHz; see 图 3. To achieve the maximum benefit of this PSRR boost circuit, using a capacitor with a minimum impedance in the 100-kHz to 1-MHz band is recommended.

8.1.3.2 Channel-to-Channel Output Isolation and Crosstalk

Output isolation is a measure of how well the device prevents voltage disturbances on one output from affecting the other output. This attenuation appears in load transient tests on the other output; however, to numerically quantify the rejection, the output channel isolation is expressed in decibels (dB).

Output isolation performance is a strong function of the PCB layout. See the *Layout* section on how to best optimize the isolation performance.

8.1.3.3 Output Voltage Noise

The TPS7A89 is designed for system applications where minimizing noise on the power-supply rail is critical to system performance. For example, the TPS7A89 can be used in a phase-locked loop (PLL)-based clocking circuit can be used for minimum phase noise, or in test and measurement systems where even small power-supply noise fluctuations reduce system dynamic range.

LDO noise is defined as the internally-generated intrinsic noise created by the semiconductor circuits alone. This noise is the sum of various types of noise (such as shot noise associated with current-through-pin junctions, thermal noise caused by thermal agitation of charge carriers, flicker noise, or 1/f noise and dominates at lower frequencies as a function of 1/f). 图 52 shows a simplified output voltage noise density plot versus frequency.

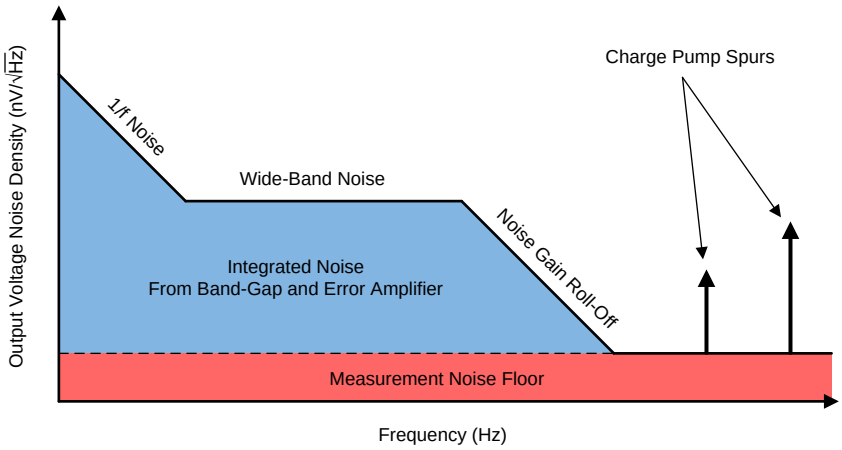


图 52. Output Voltage Noise Diagram

For further details, see the *How to Measure LDO Noise* white paper (SLYY076).

8.1.3.4 Optimizing Noise and PSRR

The ultra-low noise floor and PSRR of the device can be improved in several ways, as described in 表 7.

表 7. Effect of Various Parameters on AC Performance(1)(2)

PARAMETER	NOISE			PSRR		
	LOW-FREQUENCY	MID-FREQUENCY	HIGH-FREQUENCY	LOW-FREQUENCY	MID-FREQUENCY	HIGH-FREQUENCY
$C_{NR/SSx}$	+++	No effect	No effect	+++	+	No effect
C_{FFx}	++	+++	+	++	+++	+
C_{OUTx}	No effect	+	+++	No effect	+	+++
$V_{INx} – V_{OUTx}$	+	+	+	+++	+++	++
PCB layout	++	++	+	+	+++	+++

(1) The number of +'s indicates the improvement in noise or PSRR performance by increasing the parameter value.
(2) Shaded cells indicate the easiest improvement to noise or PSRR performance.

The noise-reduction capacitor, in conjunction with the noise-reduction resistor, forms a low-pass filter (LPF) that filters out the noise from the reference before being gained up with the error amplifier, thereby minimizing the output voltage noise floor. The LPF is a single-pole filter and the cutoff frequency can be calculated with 公式 7. The typical value of R_{NR} is 250 kΩ. The effect of the $C_{NR/SSx}$ capacitor increases when $V_{OUTx(Target)}$ increases because the noise from the reference is gained up when the output voltage increases. For low-noise applications, a 10-nF to 10-µF $C_{NR/SSx}$ is recommended.

$$f_{cutoff} = 1 / (2 \times \pi \times R_{NR} \times C_{NR/SSx}) \quad (7)$$

The feed-forward capacitor reduces output voltage noise by filtering out the mid-band frequency noise. The feed-forward capacitor can be optimized by placing a pole-zero pair near the edge of the loop bandwidth and pushing out the loop bandwidth, thus improving mid-band PSRR.

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A larger C_{OUTx} or multiple output capacitors reduces high-frequency output voltage noise and PSRR by reducing the high-frequency output impedance of the power supply.

Additionally, a higher input voltage improves the noise and PSRR because greater headroom is provided for the internal circuits. However, a high power dissipation across the die increases the output noise because of the increase in junction temperature.

Good PCB layout improves the PSRR and noise performance by providing heatsinking at low frequencies and isolating V_{OUTx} at high frequencies.

表 8 lists the output voltage noise for the 10-Hz to 100-kHz band at a 5-V output for a variety of conditions with an input voltage of 5.5 V, an R_{1x} of 12.1 kΩ, and a load current of 2 A. The 5-V output is chosen because this output is the worst-case condition for output voltage noise.

表 8. Output Noise Voltage at a 5-V Output with a 5.4-V Input

$C_{NR/SSx}$ (nF)	C_{FFx} (nF)	C_{OUTx} (µF)	SS_CTRLx	OUTPUT VOLTAGE NOISE (μV_{RMS})
10	10	22	V_{INx}	11.3
1000	100	22	V_{INx}	6.1
1000	100	22	GND	6.1
1000	100	22 || 1000	V_{INx}	6

8.1.3.4.1 Charge Pump Noise

The device internal charge pump generates a minimal amount of noise.

The high-frequency components of the output voltage noise density curve are filtered out in most applications by using 10-nF to 100-nF bypass capacitors close to the load. Using a ferrite bead between the LDO output and the load input capacitors forms a pi-filter, further reducing the high-frequency noise contribution.

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8.1.3.5 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response: the transition from a light to a heavy load and the transition from a heavy to a light load. The regions shown in 图 53 are broken down in this section and are described in 表 9. Regions A, E, and H are where the output voltage is in steady-state.

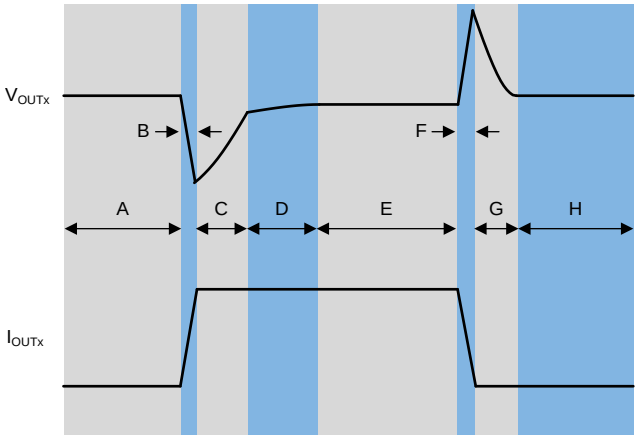


图 53. Load Transient Waveform

表 9. Load Transient Waveform Description

REGION	DESCRIPTION	COMMENT
A	Regulation	Regulation
B	Output current ramping	Initial voltage dip is a result of the depletion of the output capacitor charge.
C	LDO responding to transient	Recovery from the dip results from the LDO increasing its sourcing current, and leads to output voltage regulation.
D	Reaching thermal equilibrium	At high load currents the LDO takes some time to heat up. During this time the output voltage changes slightly.
E	Regulation	Regulation
F	Output current ramping	Initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase.
G	LDO responding to transient	Recovery from the rise results from the LDO decreasing its sourcing current in combination with the load discharging the output capacitor.
H	Regulation	Regulation

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The transient response peaks ($V_{OUTx(max)}$ and $V_{OUTx(min)}$) are improved by using more output capacitance; however, doing so slows down the recovery time (W_{rise} and W_{fall}). 图 54 shows these parameters during a load transient, with a given pulse duration (PW) and current levels ($I_{OUTx(LO)}$ and $I_{OUTx(HI)}$).

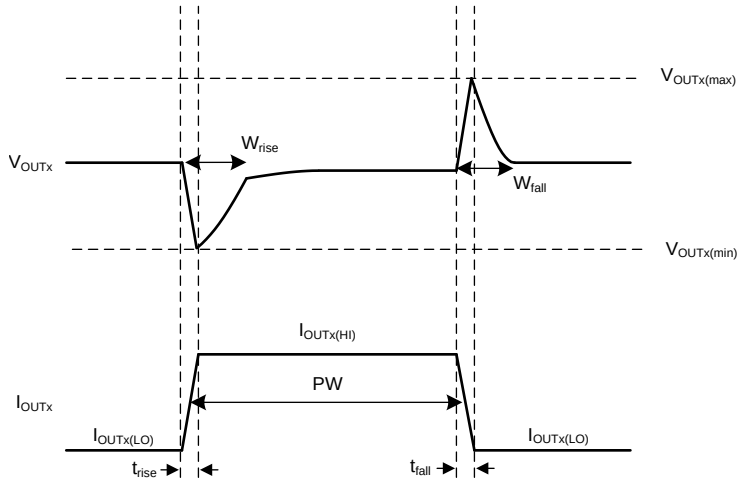


图 54. Simplified Load Transient Waveform

8.1.4 DC Performance

8.1.4.1 Output Voltage Accuracy (V_{OUTx})

The device features an output voltage accuracy of 1% maximum that includes the errors introduced by the internal reference, load regulation, line regulation, and operating temperature as specified by the *Electrical Characteristics* table. Output voltage accuracy specifies minimum and maximum output voltage error, relative to the expected nominal output voltage stated as a percent.

8.1.4.2 Dropout Voltage (V_{DO})

Generally speaking, the dropout voltage often refers to the minimum voltage difference between the input and output voltage ($V_{DO} = V_{INx} – V_{OUTx}$) that is required for regulation. When V_{INx} drops below the required V_{DO} for the given load current, the device functions as a resistive switch and does not regulate output voltage. Dropout voltage is proportional to the output current because the device is operating as a resistive switch, as shown in 图 55.

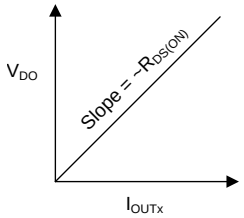


图 55. Dropout Voltage versus Output Current

Dropout voltage is affected by the drive strength for the gate of the pass element, which is nonlinear with respect to V_{INx} on this device because of the internal charge pump. Dropout voltage increases exponentially when the input voltage nears its maximum operating voltage because the charge pump multiplies the input voltage by a factor of 4 and then is internally clamped to 8.0 V.

8.1.4.2.1 Behavior When Transitioning From Dropout Into Regulation

Some applications can have transients that place the LDO into dropout, such as slower ramps on V_{INX} for start-up or load transients. As with many other LDOs, the output can overshoot on recovery from these conditions.

A ramping input supply can cause an LDO to overshoot on start-up when the slew rate and voltage levels are in the right range, as shown in 图 56. This condition is easily avoided through either the use of an enable signal, or by increasing the soft-start time with $C_{SS/NRx}$.

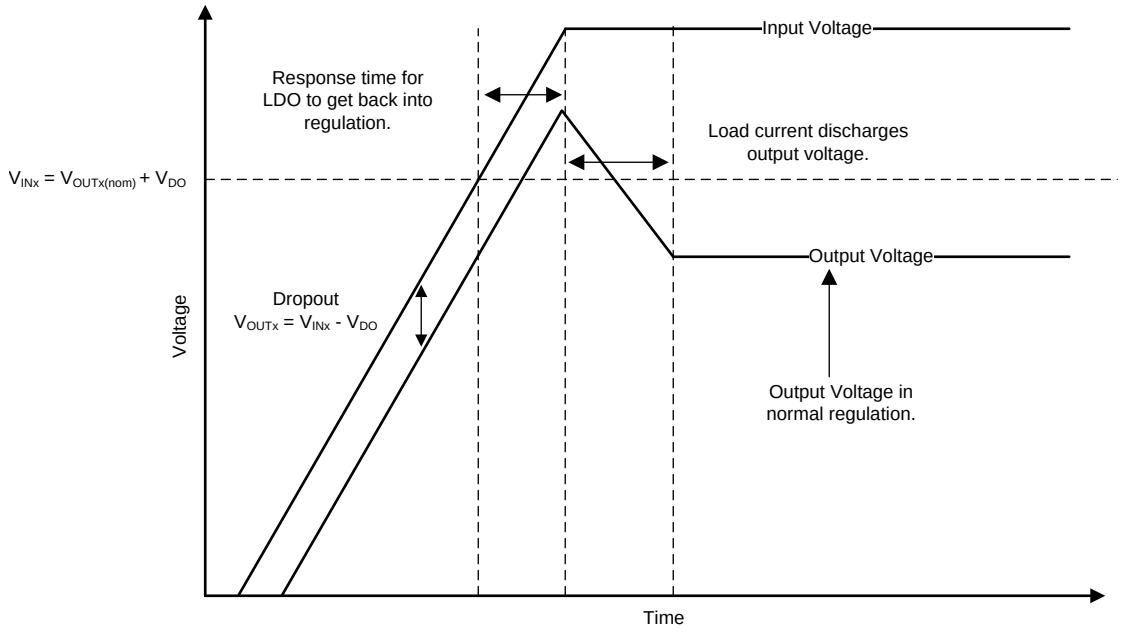


图 56. Start-Up Into Dropout

8.1.5 Reverse Current Protection

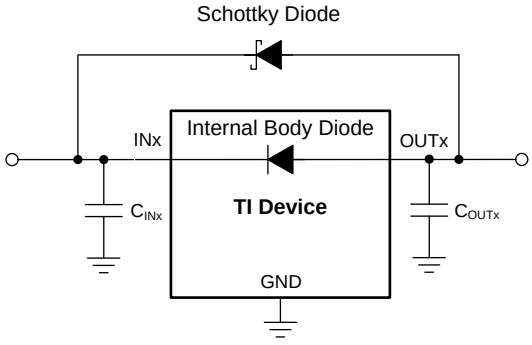
As with most LDOs, this device can be damaged by excessive reverse current.

Reverse current is current that flows through the body diode on the pass element instead of the normal conducting channel. This current flow, at high enough magnitudes, degrades long-term reliability of the device resulting from risks of electromigration and excess heat being dissipated across the device. If the current flow gets high enough, a latch-up condition can be entered.

Conditions where excessive reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUTx} > V_{INx} + 0.3$ V:

- If the device has a large C_{OUTx} and the input supply collapses quickly with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If excessive reverse current flow is expected in the application, then external protection must be used to protect the device. 图 57 shows one approach of protecting the device.



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图 57. Example Circuit for Reverse Current Protection Using a Schottky Diode

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8.1.6 Power Dissipation (P_D)

Circuit reliability demands that proper consideration is given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. P_D can be approximated using 公式 8:

$$P_D = (V_{OUTx} – V_{INx}) \times I_{OUTx} \quad (8)$$

An important note is that power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance (θ_{JA}) of the combined PCB, device package, and the temperature of the ambient air (T_A), according to 公式 9. The equation is rearranged for output current in 公式 10.

$$T_J = T_A + \theta_{JA} \times P_D \quad (9)$$

$$I_{OUTx} = (T_J – T_A) / [\theta_{JA} \times (V_{INx} – V_{OUTx})] \quad (10)$$

Unfortunately, this thermal resistance (θ_{JA}) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The θ_{JA} recorded in the table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. Note that for a well-designed thermal layout, θ_{JA} is actually the sum of the VQFN package junction-to-case (bottom) thermal resistance (θ_{JCbot}) plus the thermal resistance contribution by the PCB copper.

8.1.6.1 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are given in the table and are used in accordance with 公式 11.

Ψ_{JT}: $T_J = T_T + \Psi_{JT} \times P_D$

Ψ_{JB}: $T_J = T_B + \Psi_{JB} \times P_D$

where:

- P_D is the power dissipated as explained in 公式 8
- T_T is the temperature at the center-top of the device package, and
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

(11)

8.1.6.2 Recommended Area for Continuous Operation (RACO)

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator can be separated into the following parts, and is shown in 图 58:

- Limited by dropout: Dropout voltage limits the minimum differential voltage between the input and the output ($V_{INx} – V_{OUTx}$) at a given output current level; see the *Dropout Voltage (V_{DO})* section for more details.
- Limited by rated output current: The rated output current limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- Limited by thermals: The shape of the slope is given by 公式 10. The slope is nonlinear because the junction temperature of the LDO is controlled by the power dissipation across the LDO; therefore, when $V_{INx} – V_{OUTx}$ increases, the output current must decrease in order to ensure that the rated junction temperature of the device is not exceeded. Exceeding this rating can cause the device to fall out of specifications and reduces long-term reliability.
- Limited by V_{INx} range: The rated input voltage range governs both the minimum and maximum of $V_{INx} – V_{OUTx}$.

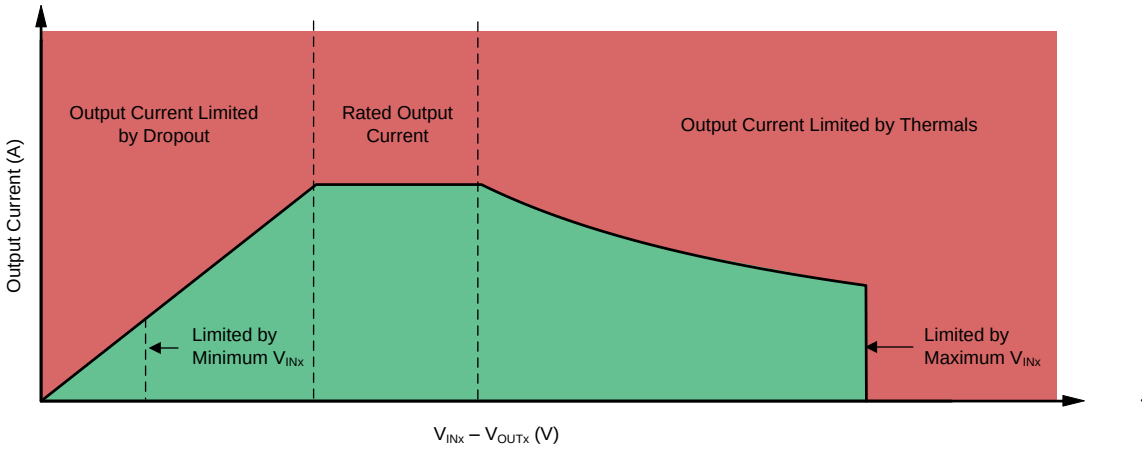


图 58. Continuous Operation Slope Region Description

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图 59 to 图 64 show the recommended area of operation curves for this device on a JEDEC-standard, high-K board with a θ_{JA} = 35.4°C/W, as given in the table.

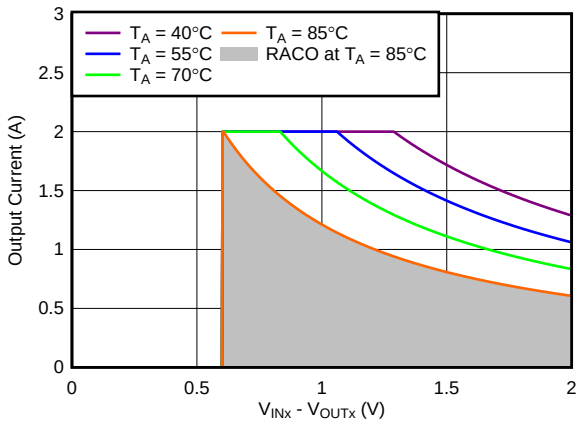


图 59. Recommended Area for Continuous Operation for V_{OUTx} = 0.8 V

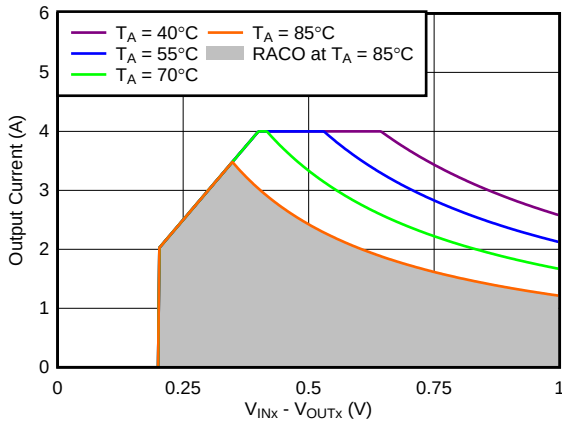


图 60. Recommended Area for Continuous Operation for V_{OUTx} = 1.2 V

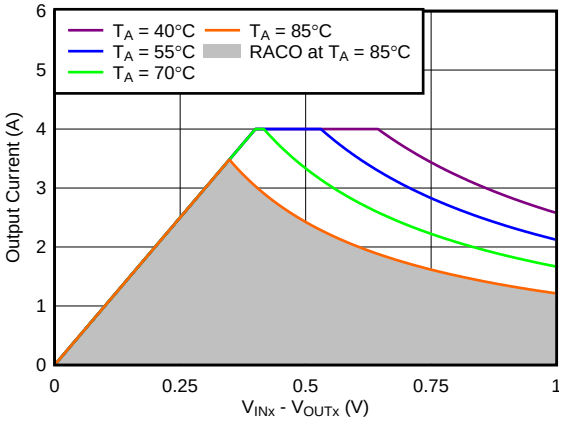


图 61. Recommended Area for Continuous Operation for V_{OUTx} = 1.8 V

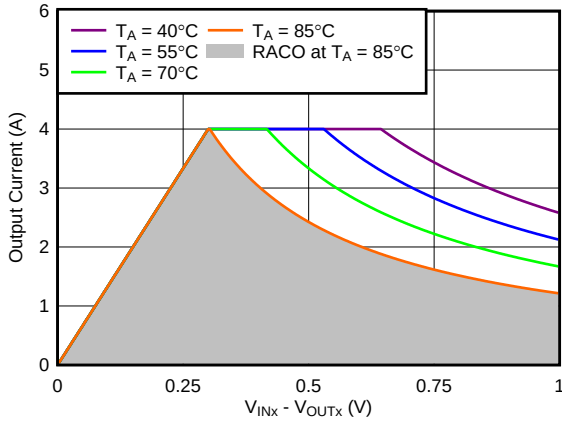


图 62. Recommended Area for Continuous Operation for V_{OUTx} = 2.5 V

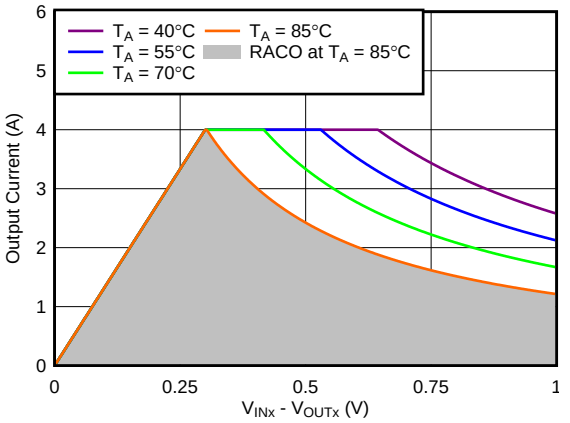


图 63. Recommended Area for Continuous Operation for V_{OUTx} = 3.3 V

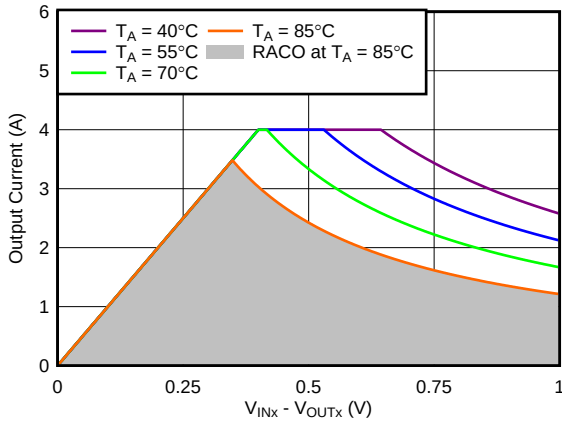
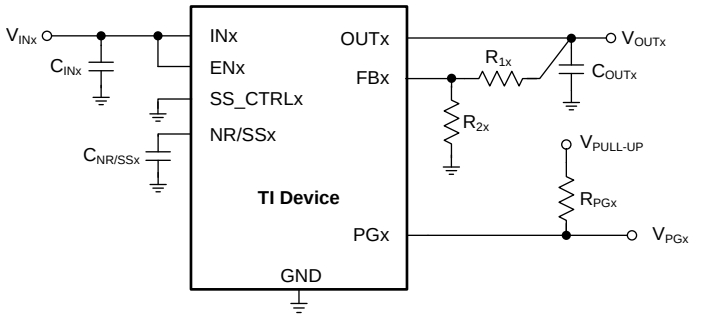


图 64. Recommended Area for Continuous Operation for V_{OUTx} = 5.0 V

8.2 Typical Application

This section discusses the implementation of the TPS7A89 to regulate from a common input voltage to two output voltages of the same value. This application is common for when two noise-sensitive loads must have the same supply voltage but have high channel-to-channel isolation. The schematic for this application circuit is provided in 图 65.



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图 65. Application Example (Single Channel)

8.2.1 Design Requirements

For the design example shown in 图 65, use the parameters listed in 表 10 as the input parameters.

表 10. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltages (V_{IN1} and V_{IN2})	3.7 V, ±1%, provided by the dc-dc converter switching at 750 kHz
Maximum ambient operating temperature	85°C
Output voltages (V_{OUT1} and V_{OUT2})	3.3 V, ±1%, output voltages are isolated
Output currents (I_{OUT2} and I_{OUT2})	2 A (maximum), 100 mA (minimum)
Channel-to-channel isolation	Isolation greater than 50 dB at 100 kHz
RMS noise	< 5 μV_{RMS}, bandwidth = 10 Hz to 100 kHz
PSRR at 750 kHz	> 40 dB
Startup time	< 5 ms

8.2.2 Detailed Design Procedure

The output voltages can be set to 1.2 V by selecting the correct values for R_{1x} and R_{2x}; see 公式 1.

Input and output capacitors are selected in accordance with the *External Component Selection* section. Ceramic capacitances of 10 µF for both inputs and outputs are selected.

To minimize noise, a feed-forward capacitance (C_{FFx}) of 10 nF is selected.

Channel-to-channel isolation depends greatly on the layout of the design. To minimize crosstalk between the outputs, keep the output capacitor grounds on separate sides of the design. See the *Layout* section for an example of how to layout the TPS7A89 to achieve best PSRR, channel-to-channel isolation, and noise.

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8.2.3 Application Curves

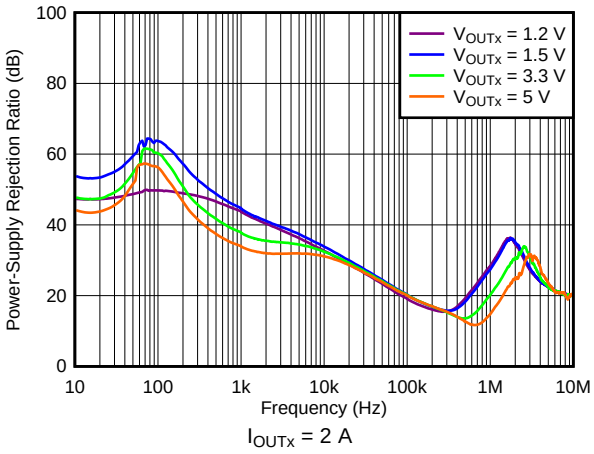


图 66. Power-Supply Rejection Ratio vs Frequency

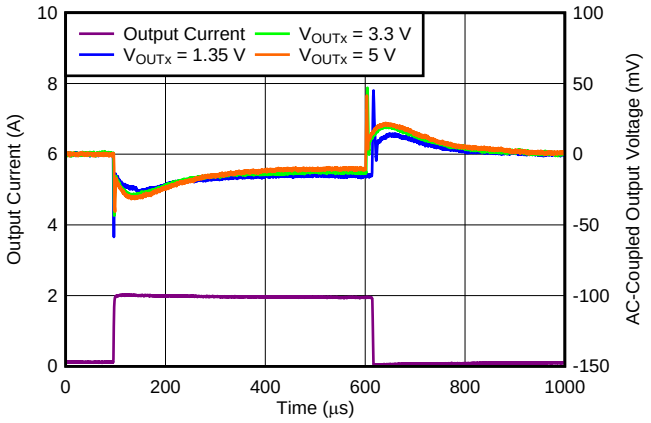


图 67. Load Transient Response vs Time and V_{OUTx}

9 Power Supply Recommendations

Both inputs of the TPS7A89 are designed to operate from an input voltage range between 1.4 V and 6.5 V. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy or has a high output impedance, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

General guidelines for linear regulator designs are to place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance.

10.1.1 Board Layout

To maximize the performance of the device, following the layout example illustrated in 图 68 is recommended. This layout isolates the analog ground (AGND) from the noisy power ground. Components that must be connected to the quiet analog ground are the noise-reduction capacitors ($C_{NR/SSx}$) and the lower feedback resistors (R_{2x}). These components must have a separate connection back to the thermal pad of the device. To minimize crosstalk between the two outputs, the output capacitor grounds are positioned on opposite sides of the layout and only connect back to the device at opposite sides of the thermal pad. Connecting the GND pins directly to the thermal pad and not to any external plane is recommended.

To maximize the output voltage accuracy, the connection from each output voltage back to the top output divider resistors (R_{1x}) must be made as close as possible to the load. This method of connecting the feedback trace eliminates the voltage drop from the device output to the load.

To improve thermal performance, a 3 × 3 thermal via array must connect the thermal pad to internal ground planes. A larger area for the internal ground planes improves the thermal performance and lowers the operating temperature of the device.

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10.2 Layout Example

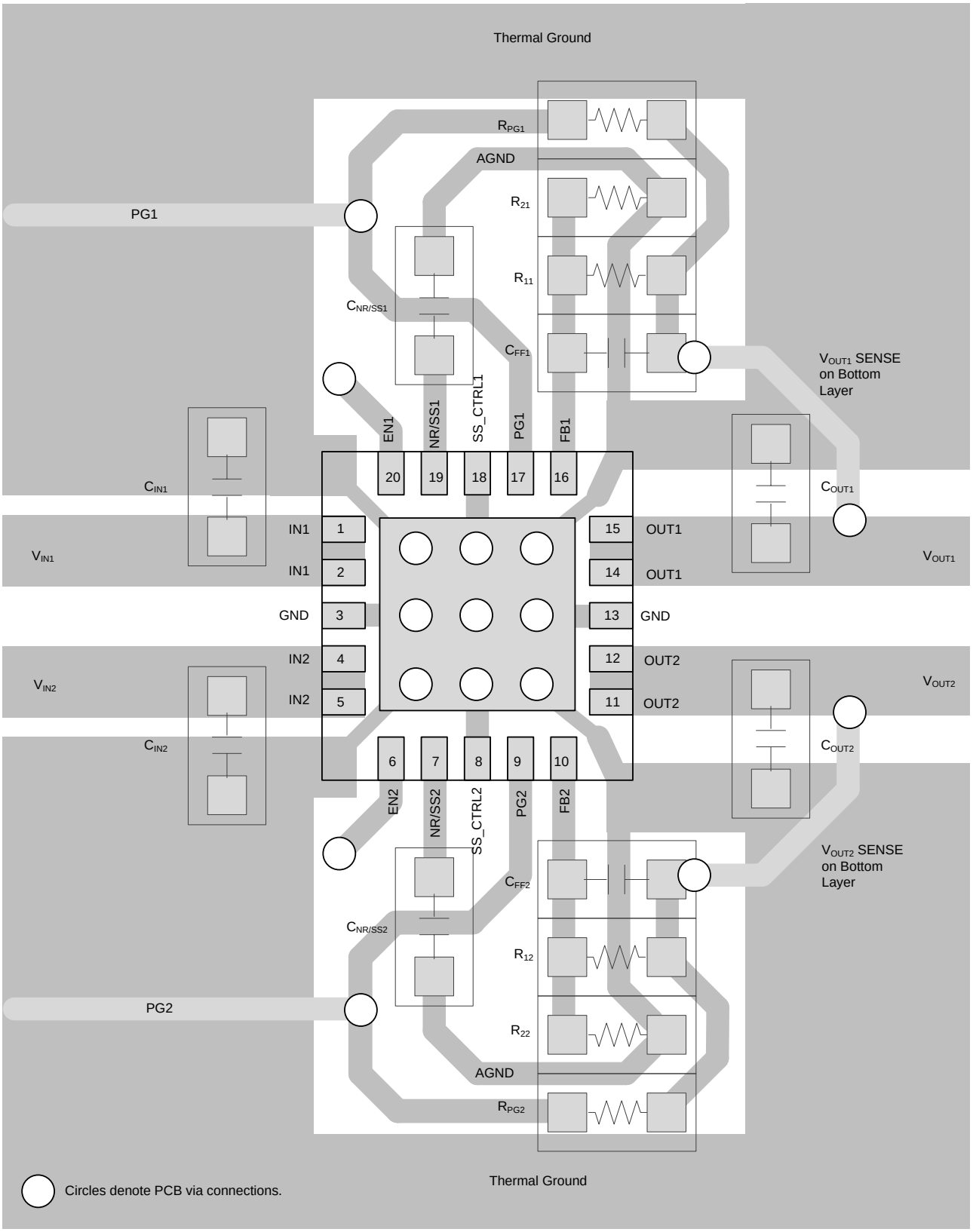


图 68. TPS7A89 Example Layout

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 评估模块

评估模块 (EVM) 可与 TPS7A89 配套使用，帮助评估初始电路性能。有关此固定装置的相关摘要信息，请参见表 11。

表 11. 设计套件与评估模块(1)

名称	部件号
TPS7A88 评估模块	《TPS7A88EVM 用户指南》

(1) 欲获得最新的封装和订货信息，请参阅本文档末尾的封装选项附录，或者访问 www.ti.com 查看器件产品文件夹。

在德州仪器 (TI) 网站 (www.ti.com) 上，可通过 TPS7A89 产品文件夹获取 EVM。

11.1.1.2 SPICE 模型

分析模拟电路和系统的性能时，使用 SPICE 模型对电路性能进行计算机仿真非常有用。您可以从 TPS7A89 产品文件夹中的仿真模型下获取 TPS7A89 的 SPICE 模型。

11.1.2 器件命名规则

表 12. 订购信息(1)

产品	说明
TPS7A89**XXYYYZ**	**XX** 表示输出电压。01 为可调输出版本。 **YYY** 为封装标识符。 **Z** 为封装数量。

(1) 欲获得最新的封装和订货信息，请参阅本文档末尾的封装选项附录，或者访问 www.ti.com 查看器件产品文件夹。

11.2 文档支持

11.2.1 相关文档

相关文档如下：

- *数据表《TPS37xx 双通道、低功耗、高精度电压检测器》*（文献编号：SBVS250）
- *用户指南《TPS7A88 评估模块》*（文献编号：SBVU027）
- *应用报告《使用前馈电容器和低压降稳压器的优缺点》*（文献编号：SBVA042）
- *白皮书《如何测量 LDO 噪声》*（文献编号：SLYY076）

11.3 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

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11.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A8901RTJR	ACTIVE	QFN	RTJ	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS7A89	Samples
TPS7A8901RTJT	ACTIVE	QFN	RTJ	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS7A89	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

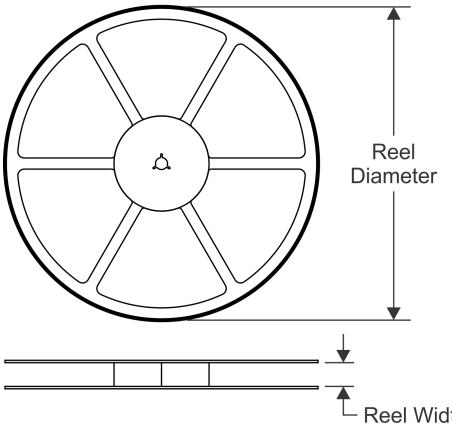
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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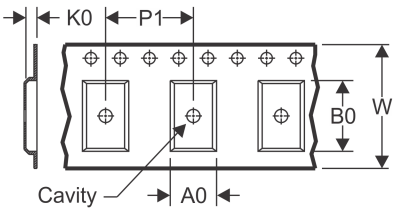
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

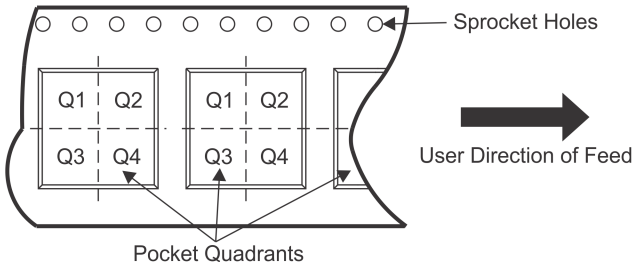


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

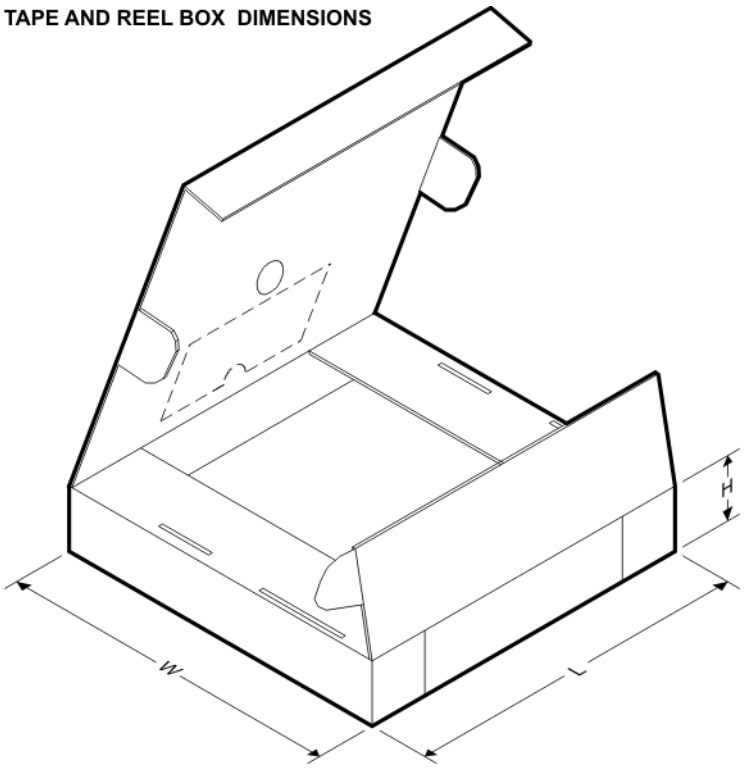
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A8901RTJR	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS7A8901RTJT	QFN	RTJ	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A8901RTJR	QFN	RTJ	20	3000	367.0	367.0	35.0
TPS7A8901RTJT	QFN	RTJ	20	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

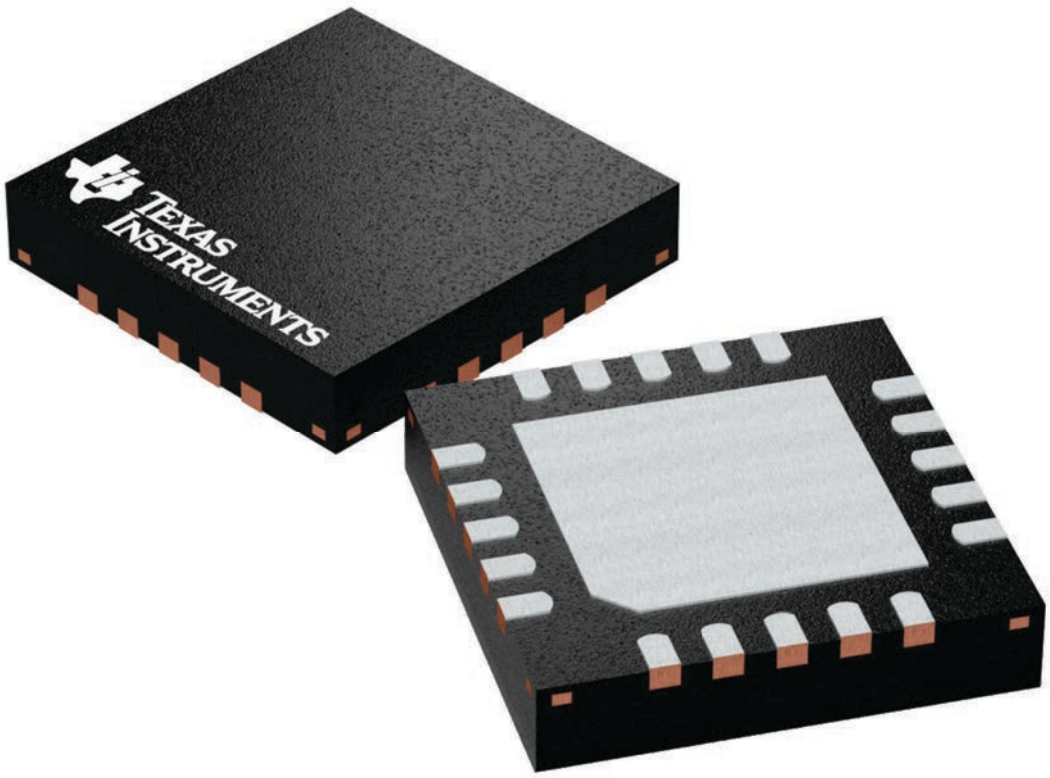
RTJ 20

WQFN - 0.8 mm max height

4 x 4, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224842/A

DATA BOOK
PACKAGE OUTLINE

LEADFRAME EXAMPLE
4222370

DRAFTSMAN: H. DENG	DATE: 09/12/2016		DIMENSIONS IN MILLIMETERS
DESIGNER: H. DENG	DATE: 09/12/2016	TEXAS INSTRUMENTS SEMICONDUCTOR OPERATIONS	CODE IDENTITY NUMBER 01295
CHECKER: V. PAKU & T. LEQUANG	DATE: 09/12/2016	ePOD, RTJ0020D / WQFN, 20 PIN, 0.5 MM PITCH	
ENGINEER: T. TANG	DATE: 09/12/2016		
APPROVED: E. REY & D. CHIN	DATE: 10/06/2016		
RELEASED: WDM	DATE: 10/24/2016		
TEMPLATE INFO: EDGE# 4218519	DATE: 04/07/2016		

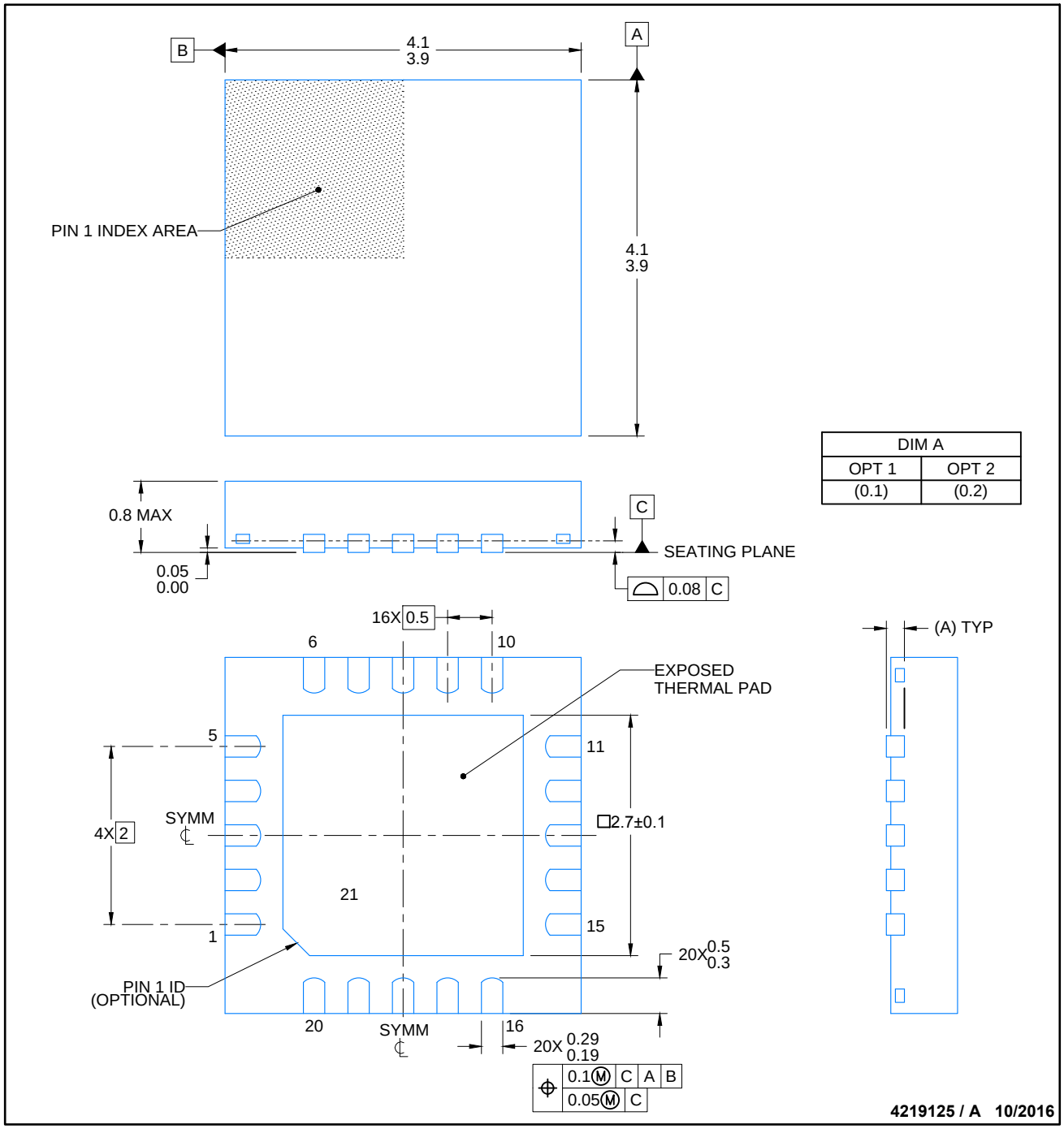
SCALE	SIZE		REV	PAGE
15X	A	4219125	A	1 OF 5

PACKAGE OUTLINE

RTJ0020D

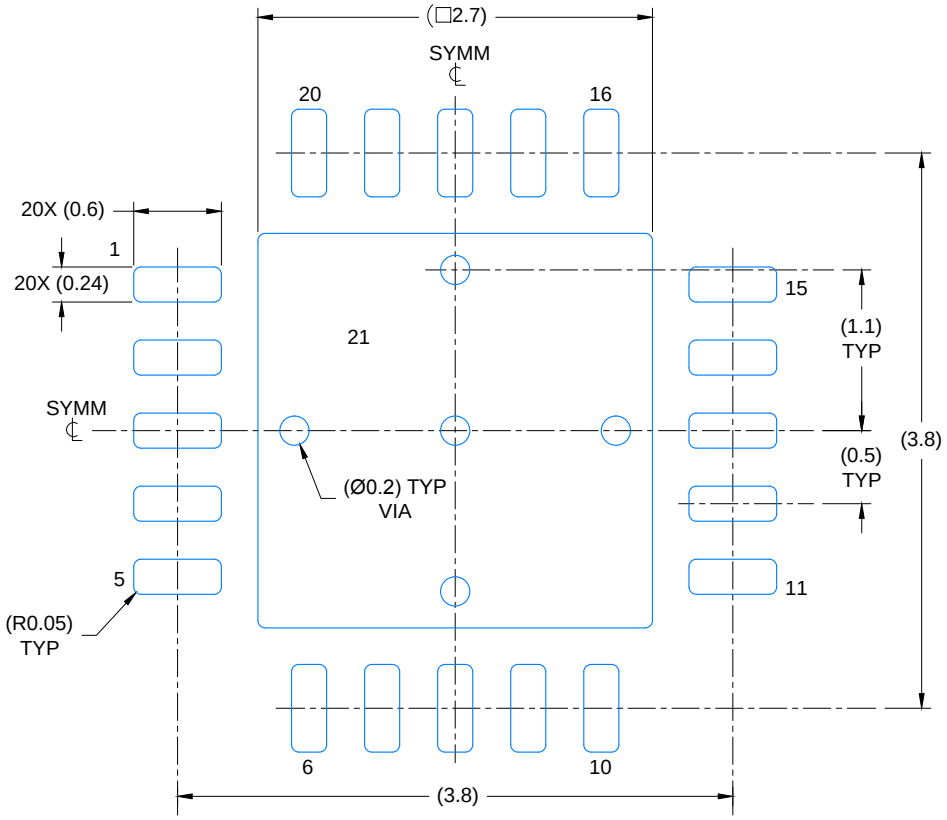
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



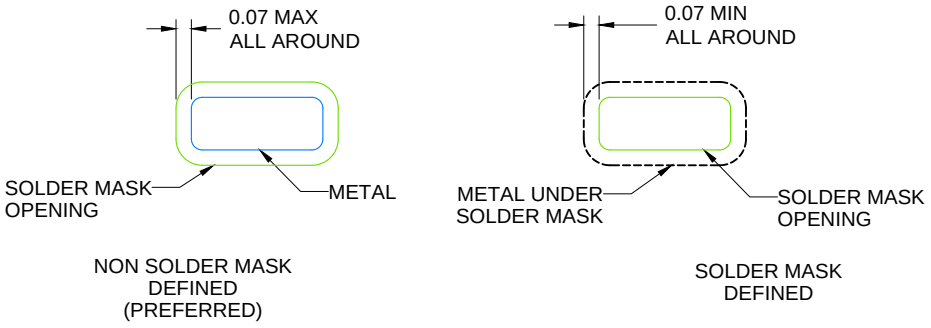
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X

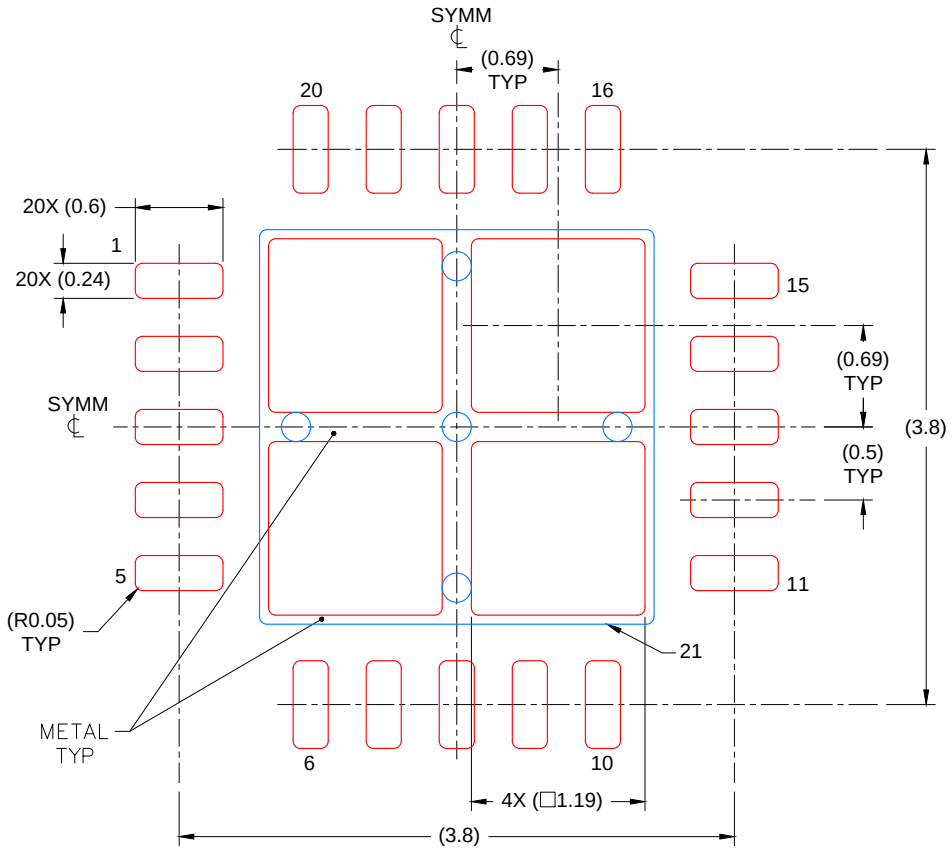


SOLDER MASK DETAILS

4219125 / A 10/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

4219125 / A 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTSMAN
A	RELEASE NEW DRAWING	2160736	10/24/2016	T. TANG / H. DENG

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