# 2.4 GHz RF SoC FOR WIRELESS DIGITAL AUDIO STREAMING CC8520, CC8521, CC8530 & CC8531 - PurePath™ Wireless

## APPLICATIONS

- Wireless high-quality digital audio
- Wireless point-to-point audio link
- Wireless (USB) headphones / headsets
- Wireless (USB) loudspeakers
- Wireless (USB) microphones
- Wireless 2.1 speaker systems
- CC852x supports up to 2 channels
- CC853x supports up to 4 channels
- CC85x1 supports USB

## FEATURES

### Built-in audio protocol

- CD-quality uncompressed audio
- Excellent robustness and co-existence through multiple techniques
  - Adaptive Frequency Hopping
  - Forward Error Correction
  - Buffering and Retransmission
  - Error Concealment
  - Optional high quality audio compression
- No software development needed when used in autonomous mode

### External system

- Can be used autonomously, or can be controlled by an external host MCU for greatest flexibility
- Seamless connection and control of external audio codecs, DACs/ADCs and digital audio amplifiers using I2S and I2C
- HID functions like power control, pairing, volume control, audio channel selection etc. can be mapped to I/Os
- RoHS compliant 6mm x 6mm QFN-40 package

### RF section

- 5 or 2 Mbps over-the-air data rate
- Bandwidth-efficient modulation format
- Excellent link budget with programmable output power up to +3.5 dBm and -83/-86 dBm sensitivity
- Seamless support for CC2590 range extender (+11dBm output power, -87dBm sensitivity)
- Suited for systems targeting compliance with worldwide radio frequency regulations: ETSI EN 300 328 and EN 300 440 class 2 (Europe), FCC CFR47 Part 15 (US) and ARIB STD-T66 (Japan)

### Digital audio support

- Digital I2S audio interface supports 1 or 2 audio channels for the CC8520 and 1 to 4 audio channels for the CC8530 at sample rates of 32, 40.275, 44.1 and 48 kHz, and supports 16 and 24 bit word-widths
- USB audio support for 32, 44.1 and 48 kHz, and supports 16 and 24 bit word-widths
- Audio latency down to 10.7 ms
- Data side-channel allows data to be sent alongside the audio between external host processors

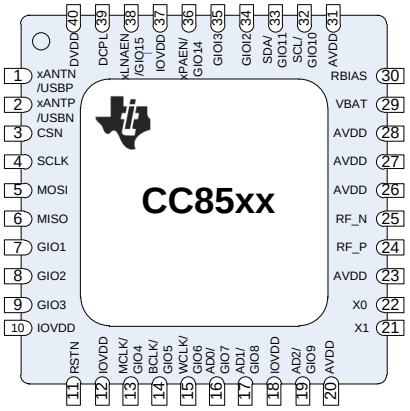
### USB

- Full-speed USB Audio device
- USB Basic Audio Device Class: HT1, HS1 and MT topologies (headphone, headset and microphone)
- USB Audio Device Class.
- Basic USB HID device class support for remote control, mouse and keyboard functionality
- Autonomous operation only.

### Development tools

- PC-based PurePath™ Wireless Configurator for CC85xx configuration
- CC85xx Family User Guide
- CC85XXDK audio development kit
- CC85XXDK-HEADSET development kit

### QFN-40 PIN CONFIGURATION (TOP VIEW)



## DESCRIPTION

**The PurePath™ Wireless platform is a cost-effective and low-power solution optimized for wireless transmission of high-quality digital audio.**

**The CC85xx includes a robust built-in wireless audio transmission protocol and can control selected external audio devices. Utilizing numerous coexistence mechanisms allows the CC85xx to avoid interfering with, or being interfered by other 2.4 GHz radio systems.**

**The CC85xx operates autonomously, and can be used with or without an external MCU. An external host processor can be connected through SPI and control some aspects of its operation. The CC85xx interfaces easily with other TI audio ICs and DSPs (using I2S and DSP/TDM interfaces). More details can be found in the CC85xx Family User Guide [2].**

## ABBREVIATIONS

| | | | |
|---|---|---|---|
| ADC | Analog to Digital Converter | LED | Light Emitting Diode |
| ARIB | Association of Radio Industries and Businesses | LNA | Low Noise Amplifier |
| BER | Bit Error Rate | MISO | Master In Slave Out |
| CODEC | Coder/Decoder | MOSI | Master Out Slave In |
| DAC | Digital to Analog Converter | MCU | Microcontroller |
| DSP | Digital Signal Processor | PA | Power Amplifier |
| EHIF | External Host Interface | PCM | Pulse Code Modulation |
| ESD | Electro Static Discharge | PER | Packet Error Rate |
| ETSI | European Telecommunications Standard Institute | PLL | Phase Lock Loop |
| FCC | Federal Communications Commission | PM | Protocol Master |
| FEC | Forward Error Correction | PPW | PurePath™ Wireless |
| FSK | Frequency Shift Keying | PS | Protocol Slave |
| FW | Firmware | RoHS | Restriction of Hazardous Substances |
| HID | Human Interface Device | RF | Radio Frequency |
| I2C | Inter-Integrated Circuit (serial communications bus) | SLAC | Slightly Lossy Compression Algorithm |
| I2S | Inter-IC Sound (serial bus for digital audio signals) | SPI | Serial Peripheral Interface |
| IEEE | Institute of Electrical and Electronics Engineers | SoC | System-on-Chip |
| ISM | Industrial, Scientific, Medical | STD | Standard |
| JEDEC | Joint Electron Device Engineering Council | TDM | Time-Division Multiplexing |
| LDO | Low-Dropout Regulator | | |

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS(1)

| PARAMETER | TEST CONDITIONS | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage (2) | All supply pins must have the same voltage | –0.3 | 3.9 | V |
| Voltage on any digital pin | | –0.3 | min(VDD + 0.3, 3.9) | V |
| Input RF level | | | 10 | dBm |
| Storage temperature range | | -40 | 125 | °C |
| ESD (3) | All pads, according to human-body model (HBM), JEDEC STD 22, method A114 | | 2000 | V |
| | According to charged-device model (CDM), JEDEC STD 22, method C101E | | 400 | V |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) For CC8521 and CC8531 running on USB power, a LDO is needed to comply with these ratings.

(3) CAUTION: ESD sensitive device. Precaution should be used when handing the device in order to prevent permanent damage.

## RECOMMENDED OPERATING CONDITIONS, CC8520/CC8530

| PARAMETER | TEST CONDITIONS | Min | Max | Unit |
|---|---|---|---|---|
| Operating ambient temperature range, $T_A$ | | -40 | +85 | °C |
| Operating supply voltage | | 2.0 | 3.6 | V |

## RECOMMENDED OPERATING CONDITIONS, CC8521/CC8531

| PARAMETER | TEST CONDITIONS | Min | Max | Unit |
|---|---|---|---|---|
| Operating ambient temperature range, $T_A$ | | -40 | +85 | °C |
| Operating supply voltage (1) | | 3.0 | 3.6 | V |

(1) For CC8521 and CC8531 running on USB power, an LDO is needed to comply with these ratings.

## GENERAL CHARACTERISTICS

Measured on Texas Instruments CC85xxEM reference designs with $T_A$ = 25°C and VDD = 3.3 V, unless otherwise noted.

| PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| RF frequency range | | 2400 | | 2483.5 | MHz |
| Data rate | Shaped 8FSK<br>Shaped 2FSK | | 5<br>2 | | Mbps |
| Audio latency | Latency between I2S interface on audio source and I2S interface on audio sink. Uncompressed 16 or 24 bit. Audio latency is programmable using the PurePath Wireless Configurator [1]. | 512(1) | | 2048 | Samples |
| Audio sample rate | Audio sample rate is programmable using the PurePath Wireless Configurator [1] (2) | | 48<br>44.1<br>40.275(3)<br>32 | | kHz |

(1) Latencies below 768 samples only supported for some configurations

(2) ±2000ppm tolerance

(3) Not supported in USB mode. For USB Headset, dynamic sample rate change is not allowed.

## ELECTRICAL CHARACTERISTICS, CC8520/CC8521/CC8530/CC8531

Measured on Texas Instruments CC85xxEM reference designs with $T_A$ = 25°C and VDD = 3.3 V, unless otherwise noted.

| PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Current consumption, power down state | Voltage regulator / crystal oscillator off – status lost (POWERED_DOWN state) | | 1 | | μA |
| Current consumption, headphone master(1) | Average current for a PurePath Wireless master with I2S interface active, sourcing two PCM16 channels with maximum output power. | | 29 | | mA |
| Current consumption, headphone slave(1) | Average current for a PurePath Wireless slave with I2S interface active, sinking two PCM16 channels with maximum output power | | 25 | | mA |

(1) Measured on Texas Instruments CC85xx EM reference designs and CC85XXDK. Sample rate 48 kHz, MCLK disabled. 5 Mbit mode

## RF CHARACTERISTICS, CC8520/CC8521/CC8530/CC8531

Measured on Texas Instruments CC85xx EM reference designs with $T_A$ = 25°C and VDD = 3.3 V, unless otherwise noted.

| PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Output power | Maximum output power setting | | 3.5 | | dBm |
| Receiver sensitivity(1) | 5 Mbps<br>2 Mbps(2) | | -83<br>-86 | | dBm |
| Saturation (maximum input level) (1) | 5 Mbps<br>2 Mbps(2) | | -2<br>6 | | dBm |
| Selectivity | Adjacent channel, ±4MHz, wanted 3dB above sensitivity. 5 Mbps<br>Adjacent channel, ±4MHz, wanted 3dB above sensitivity. 2 Mbps(2) | | 8<br>20 | | dB |
| | Alternate channel, ±8MHz, wanted 3dB above sensitivity. 5 Mbps<br>Alternate channel, ±8MHz, wanted 3dB above sensitivity. 2 Mbps(2) | | 35<br>43 | | dB |
| Occupied bandwidth | 99% energy bandwidth. 5 Mbps<br>99% energy bandwidth. 2 Mbps(2) | | 3.8<br>3.2 | | MHz |
| Optimum load impedance | Differential impedance seen from the RF port (RF_P and RF_N) towards the antenna | | 70 + j30 | | Ω |
| Spurious emission | Suitable for systems targeting compliance with EN 300 328, EN 300 440(3), FCC CFR47 Part 15 and ARIB STD-T-66 | | | | |

(1) Measured using data packets with 40 byte payload, 0.1% BER for 5 Mbit and 125 byte payload, 0.001% BED for 2 Mbit

(2) Typical data measured across 6 devices at room temperature.

(3) Systems with external antenna connector: Margins for passing conducted requirements at sub 1GHz frequencies can be improved by using a simple band-pass filter connected between matching network and RF connector (1.6 pF in parallel with 1.6 nH); this filter must be connected to a good RF ground.

## ELECTRICAL CHARACTERISTICS, CC8520/CC8521/CC8530/CC8531+CC2590

Measured on Texas Instruments CC85xx+CC2590 EM reference designs with $T_A$ = 25°C and VDD = 3.3 V, unless otherwise noted.

| PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Current consumption, power down state(1) | Voltage regulator / crystal oscillator off – status lost (POWERED_DOWN state) | | 1 | | µA |
| Current consumption, headphone master(2) | Average current for a PurePath Wireless master with I2S interface active, sourcing two PCM16 channels. | | 38 | | mA |
| Current consumption, headphone slave(2) | Average current for a PurePath Wireless slave with I2S interface active, sinking two PCM16 channels | | 28 | | mA |

(1) CC2590 power down current is 100 nA[4]

(2) Measured on Texas Instruments CC85xx+CC2590 EM reference designs and CC85XXDK. Sample rate 48 kHz, MCLK disabled. 5 Mbit mode

## RF CHARACTERISTICS, CC8520/CC8521/CC8530/CC8531+CC2590

Measured on Texas Instruments CC85xx+CC2590 EM reference designs with $T_A$ = 25°C and VDD = 3.3 V, unless otherwise noted.

| PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Output power | Maximum output power setting | | 11 | | dBm |
| Receiver sensitivity(1) | 5 Mbps<br>2 Mbps(2) | | -87<br>-90 | | dBm |
| Saturation (maximum input level)(1) | 5 Mbps | | -12 | | dBm |
| Selectivity | Adjacent channel, ±4MHz, wanted 3dB above sensitivity. 5 Mbps | | 9 | | dB |
| | Alternate channel, ±8MHz, wanted 3dB above sensitivity. 5 Mbps | | 34 | | |
| Spurious emission | Suitable for systems targeting compliance with EN 300 328, EN 300 440(3), FCC CFR47 Part 15 and ARIB STD-T-66 | | | | |

(1) Measured using data packets with 40 byte payload, 0.1% BER for 5 Mbit and 125 byte payload, 0.001% BER for 2 Mbit

(2) Typical data measured across 6 devices at room temperature.

(3) Systems with external antenna connector: Margins for passing conducted requirements at sub 1GHz frequencies can be improved by using a simple band-pass filter connected between matching network and RF connector (1.6 pF in parallel with 1.6 nH); this filter must be connected to a good RF ground.

## 48-MHz CRYSTAL REQUIREMENTS

General parameters with $T_A$ = 25°C and VDD = 3.3 V, unless otherwise noted.

| PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Crystal frequency | | | 48 | | MHz |
| Crystal frequency accuracy requirement(1) | | -50 | | 50 | ppm |
| ESR Equivalent series resistance | | - | | 60 | ohm |
| $C_0$ Crystal shunt capacitance | | - | | 3 | pF |
| $C_L$ Crystal load capacitance | | 15 | 16 | 17 | pF |

(1) Including aging and temperature dependency

## AUDIO CLOCK CHARACTERISTICS

$T_A$ = 25°C and VDD = 3.3 V, unless otherwise noted.

| PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| MCLK Frequency range | Programmable using the PurePath Wireless Configurator [1] | $32 \cdot F_{WCLK}$ | | $512 \cdot F_{WCLK}$ | |
| BCLK Frequency range | Programmable using the PurePath Wireless Configurator [1] | $32 \cdot F_{WCLK}$ | | $256 \cdot F_{WCLK}$ | |
| WCLK Frequency range | | 31.936 | | 48.096 | kHz |
| RMS jitter **(Output clocks)** | RMS period jitter for 1000 periods | | 80 | 200 | ps |

## SPI INTERFACE CHARACTERISTICS

$T_A$ = 25°C and VDD = 3.3 V, unless otherwise noted.

| PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| SCLK frequency | | 0 | | 20 | MHz |
| SCLK low | | 25 | | | ns |
| SCLK high | | 25 | | | ns |
| CSN high | Minimum time CSN must be high, if brought high, between commands (it is not necessary to bring CSN high between commands). | 50 | | | ns |
| CSN falling edge to SCLK rising edge | Distance from CSN asserted until first rising edge on SCLK. | 25 | | | ns |
| SCLK falling edge to CSN rising edge | Distance from last negative edge of SCLK in last word until CSN can be de-asserted. | 100 | | | ns |
| Inter-word spacing | Minimum distance in time from rising edge of SCLK for last bit in word *n* and the rising edge of SCLK for the first bit in word *n*+1.<br>Properly handles abutting words. | 50 | | | ns |
| Hysteresis on SCLK | Hysteresis around trigger point of input buffer using a Schmitt trigger | | 100 | | mV |
| Slew rate on SCLK | Slew rate from 0.1·IOVDD to 0.9·IOVDD | 10 | | | V/µs |

## VBAT CHARACTERISTICS

$T_A$ = 25°C and VDD = 3.3 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | Min | Max | Unit |
|---|---|---|---|---|
| Input voltage | | 0 | 4.5 | V |

## FLASH CHARACTERISTICS

$T_A$ = 25°C and VDD = 3.3 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | Min | TYP | Max | Unit |
|---|---|---|---|---|---|
| Program/erase endurance | | | | 1000 | Cycles |

# 1 PIN DESCRIPTION

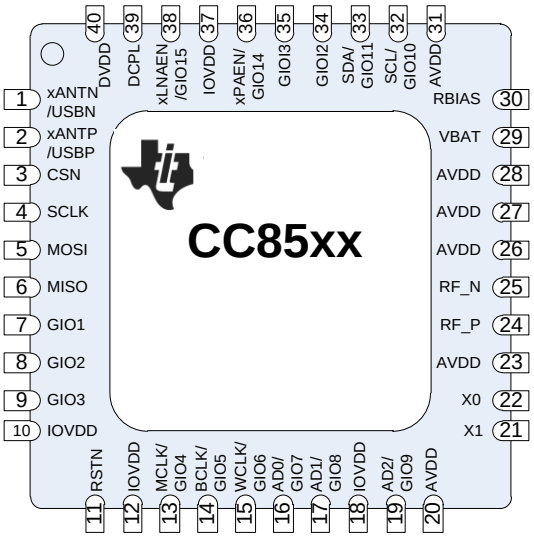



**Figure 1 - CC85xx QFN-40 PIN CONFIGURATION**

| PIN | PIN NAME | PIN TYPE | DESCRIPTION |
|---|---|---|---|
| - | GND | Ground | The exposed die attach pad must be connected to a solid ground plane underneath the chip |
| 1 | xANTN<br>USBN | Digital I/O[1] | CC85x0 Slaves: External antenna switch control<br>CC85x1: USB D- data line |
| 2 | xANTP<br>USBP | Digital I/O[1] | CC85x0 Slaves: External antenna switch control<br>CC85x1: USB D+ data line |
| 3 | CS_N | Digital Input<br>(pull-up) | Serial SPI configuration interface, active low chip select |
| 4 | SCLK | Digital I/O[1] | Serial SPI configuration interface, clock input/output |
| 5 | MOSI | Digital I/O[1] | Serial SPI configuration interface, master data output, slave data input |
| 6 | MISO | Digital I/O[1] | Serial SPI configuration interface, master data input, slave data output. |
| 7 | GIO1 | Digital I/O[1] | General-purpose digital I/O pin 1<br>Configurable with PurePath™ Wireless Configurator |
| 8 | GIO2 | Digital I/O[1] | General-purpose digital I/O pin 2 |
| 9 | GIO3 | Digital I/O[2] | General-purpose digital I/O pin 3<br>Configurable with PurePath™ Wireless Configurator |
| 10 | IOVDD | Power<br>(I/O pads) | Digital power supply for the digital I/Os in the SPI interface and GIO1-GIO3. |
| 11 | RSTN | Digital Input<br>(pull-up) | Active-low device reset |
| 12 | IOVDD | Power<br>(I/O pins) | Digital power supply for the RSTN and MCLK digital I/O pins. |
| 13 | MCLK<br>GIO4 | Digital I/O[1] | Master clock output for external audio devices<br>General-purpose digital I/O pin 4 |

| PIN | PIN NAME | PIN TYPE | DESCRIPTION |
|---|---|---|---|
| 14 | BCLK<br>GIO5 | Digital I/O[1] | I2S/DSP audio interface bit clock (in/out)<br>General-purpose digital I/O pin 5 |
| 15 | WCLK<br>GIO6 | Digital I/O[1] | I2S/DSP audio interface word clock (in/out)<br>General-purpose digital I/O pin 6 |
| 16 | AD0<br>GIO7 | Digital I/O[1] | I2S/DSP audio interface data line 0 (in/out)<br>General-purpose digital I/O pin 7 |
| 17 | AD1<br>GIO8 | Digital I/O[1] | I2S/DSP audio interface data line 1 (in/out)<br>General-purpose digital I/O pin 8 |
| 18 | IOVDD | Power<br>(I/O pins) | Digital power supply for the digital I/Os in audio interface (BCLK-AD2). |
| 19 | AD2<br>GIO9 | Digital I/O[2] | I2S/DSP audio interface data line 2 (in/out)<br>Configurable with PurePath™ Wireless Configurator |
| 20 | AVDD | Power (Analog) | 2.0-3.6V analog power supply connection |
| 21 | X1 | Analog I/O | Crystal oscillator pin input, or external clock input (48 MHz) |
| 22 | X0 | Analog I/O | Crystal oscillator pin output (48 MHz) |
| 23 | AVDD | Power (Analog) | Analog power supply connection |
| 24 | RF_P | RF I/O | Positive differential RF input signal to LNA in receive mode<br>Positive differential RF output signal from PA in transmit mode |
| 25 | RF_N | RF I/O | Negative differential RF input signal to LNA in receive mode<br>Negative differential RF output signal from PA in transmit mode |
| 26 | AVDD | Power (Analog) | Analog power supply connection |
| 27 | AVDD | Power (Analog) | Analog power supply connection |
| 28 | AVDD | Power (Analog) | Analog power supply connection |
| 29 | VBAT | Analog input | Battery voltage supervisor (threshold level programmable by external resistor to positive battery terminal) |
| 30 | RBIAS | Analog output | External precision bias resistor for reference current. 56 kΩ, ±1% |
| 31 | AVDD | Power (Analog) | Analog power supply connection (Guard ring AVDD connection for digital noise isolation) |
| 32 | SCL<br>GIO10 | Digital I/O[1] | I2C master clock line. Must be connected to external pull-up<br>General-purpose digital I/O pin 10 |
| 33 | SDA<br>GIO11 | Digital I/O[1] | I2C master data line. Must be connected to external pull-up<br>General-purpose digital I/O pin 11 |
| 34 | GIO12 | Digital I/O[1] | General-purpose digital I/O pin 12 |
| 35 | GIO13 | Digital I/O[1] | General-purpose digital I/O pin 13 |
| 36 | xPAEN<br>GIO14 | Digital I/O[2] | Control external PA<br>General-purpose digital I/O pin 14 |
| 37 | IOVDD | Power (I/O pads) | Digital power supply for SCL-GIO15 pins. |
| 38 | xLNAEN<br>GIO15 | Digital I/O[2] | Control external LNA<br>General-purpose digital I/O pin 15 |
| 39 | DCPL | Power (Digital) | 1.7V-1.85 V linear voltage regulator output to which a 1 uF decoupling capacitor should be attached. For test-purposes an external digital supply voltage (1.62-1.98 V) can be applied here, bypassing the voltage regulator.<br>NOTE: The voltage regulator is intended for use with the CC85xx chip only. It cannot be used to provide supply voltage to other devices. |
| 40 | DVDD | Power (Digital) | Digital power supply for the linear voltage regulator. |

[1] Digital I/O pad with 4 mA source/sink capability.

[2] Digital I/O pad with 20 mA source/sink capability.

## 2 APPLICATION CIRCUIT

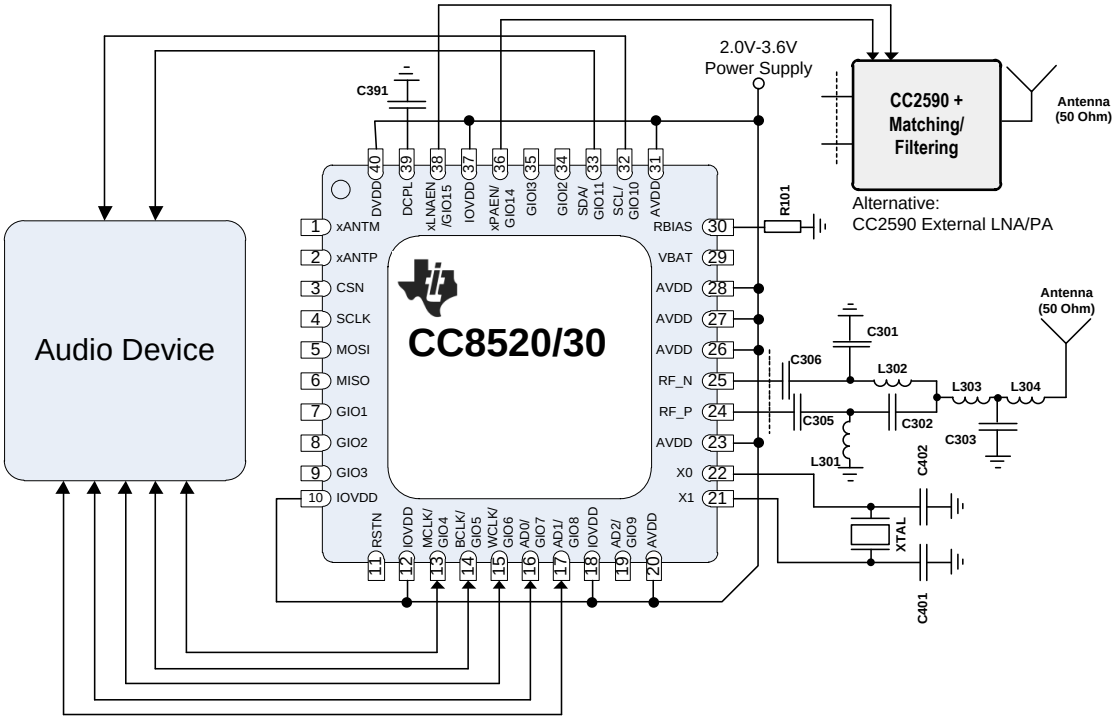



**Figure 2 - CC8520/CC8530 Application Circuit**

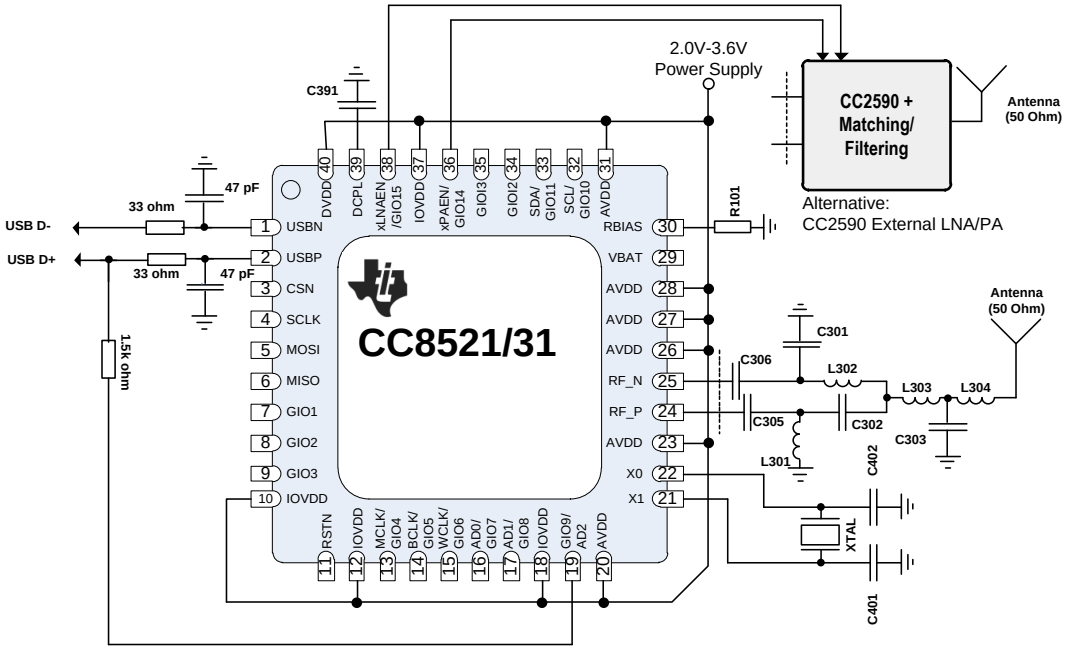



**Figure 3 - CC8521/CC8531 Application Circuit**

# 3 SYSTEM DESCRIPTION

By employing proprietary technology, referred to as PurePath Wireless, the CC85xx device family provides robust, high-quality, short-range 2.4 GHz wireless digital audio streaming in low-cost single chip solutions.

Two or more devices form a PurePath Wireless audio network. Great care has been taken to ensure that this audio network provides gap-less and robust audio streaming in varied environments and that it can coexist amicably with existing wireless technologies in the crowded 2.4 GHz ISM band.

Most applications can be implemented without any software development and only require the CC85xx to be connected to an external audio source or sink (such as an audio codec, S/PDIF interface or class-D amplifier) and a few push buttons, switches or LED for human interaction. Advanced applications can interface a host processor or DSP directly to the CC85xx and directly stream audio and control most aspects of device and audio network operation. The complete list of supported audio devices can be found in the PurePath Wireless Configurator [1].

The PurePath Wireless Configurator [1], a PC-based configuration tool, is used to set up the desired functionality and parameters of the target system and then produces firmware images that subsequently must be programmed into the embedded flash memory of each CC85xx.

All devices in the CC85xx family interface seamlessly with the CC2590 RF range extender device to allow for even wider RF coverage and improved robustness in difficult environments.

# 4 DOCUMENT HISTORY

| Revision | Date | Description/Changes |
|---|---|---|
| SWRS091F | June 2012 | Added 2 Mbit mode (throughout document) and flash endurance numbers. Lowered minimum latency. Added support for 24 bit data width . Updated pin description. |
| SWRS091E | Dec 2011 | Added VBAT voltage info |
| SWRS091D | July 2011 | Added info on CC8521 and CC8531 |
| SWRS091C | March 2011 | Added info on CC8530. Updated current consumption numbers and how they are measured. Storage temperature updated. Info on supported codecs now in PurePath Wireless Configurator. |
| SWRS091B | Sept 2010 | Add RF Characteristics for CC8520+CC2590EM. Moved the sections; Network topology, Coexistence, Audio Interface, Human Interaction drivers and external host interface to the **CC85xx Family User's Guide [2].** Updated pin-out table and fig 1. |
| SWRS091A | March 2010 | First release |

# 5 REFERENCES

[1] PurePath™ Wireless Configurator

[2] CC85xx Family User Guide

[3] CC-Debugger

[4] CC2590 Product folder

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CC8520RHAR | ACTIVE | VQFN | RHA | 40 | 2500 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | CC8520 | Samples |
| CC8520RHAT | ACTIVE | VQFN | RHA | 40 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | CC8520 | Samples |
| CC8521RHAR | ACTIVE | VQFN | RHA | 40 | 2500 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | CC8521 | Samples |
| CC8521RHAT | ACTIVE | VQFN | RHA | 40 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | CC8521 | Samples |
| CC8530RHAR | ACTIVE | VQFN | RHA | 40 | 2500 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | CC8530 | Samples |
| CC8530RHAT | ACTIVE | VQFN | RHA | 40 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | CC8530 | Samples |
| CC8531RHAR | ACTIVE | VQFN | RHA | 40 | 2500 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | CC8531 | Samples |
| CC8531RHAT | ACTIVE | VQFN | RHA | 40 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | CC8531 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

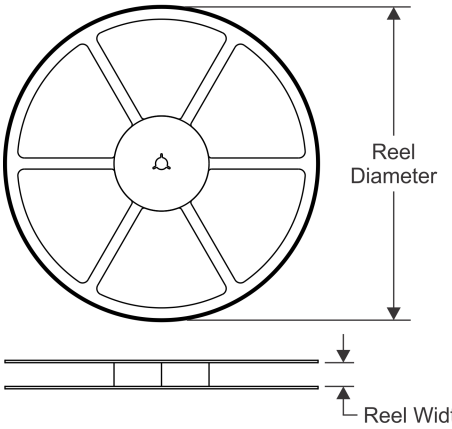
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

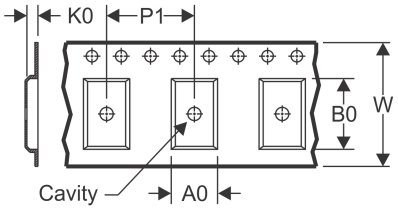
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

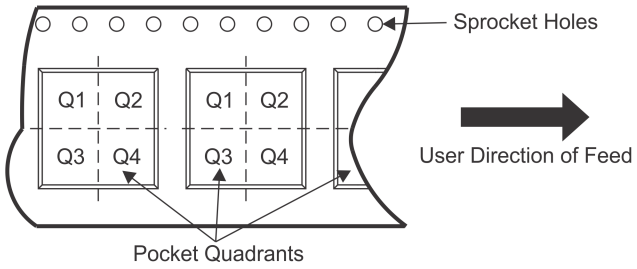



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

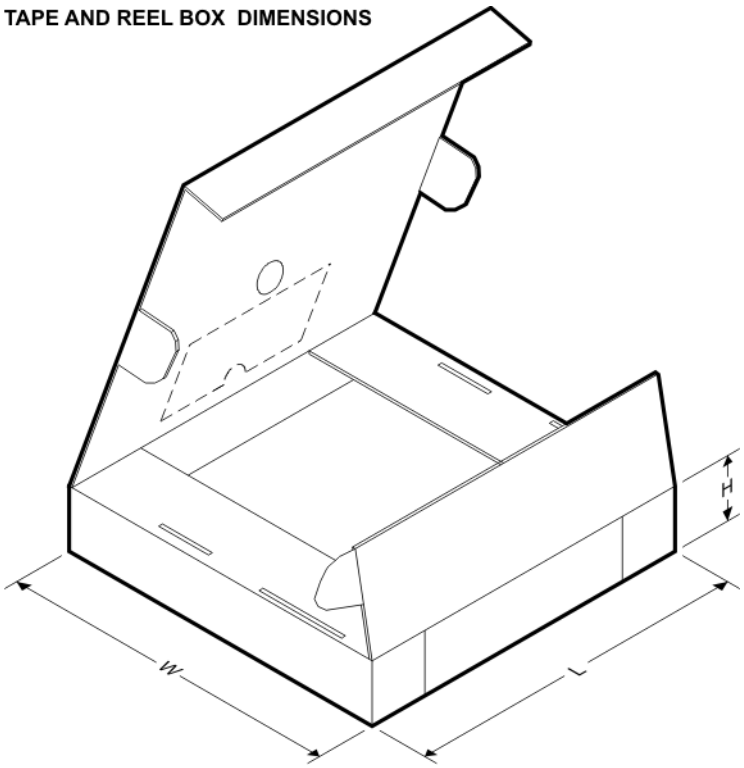
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CC8520RHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.5 | 12.0 | 16.0 | Q2 |
| CC8521RHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.5 | 12.0 | 16.0 | Q2 |
| CC8530RHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.5 | 12.0 | 16.0 | Q2 |
| CC8531RHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.5 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CC8520RHAR | VQFN | RHA | 40 | 2500 | 350.0 | 350.0 | 43.0 |
| CC8521RHAR | VQFN | RHA | 40 | 2500 | 350.0 | 350.0 | 43.0 |
| CC8530RHAR | VQFN | RHA | 40 | 2500 | 350.0 | 350.0 | 43.0 |
| CC8531RHAR | VQFN | RHA | 40 | 2500 | 350.0 | 350.0 | 43.0 |

# GENERIC PACKAGE VIEW

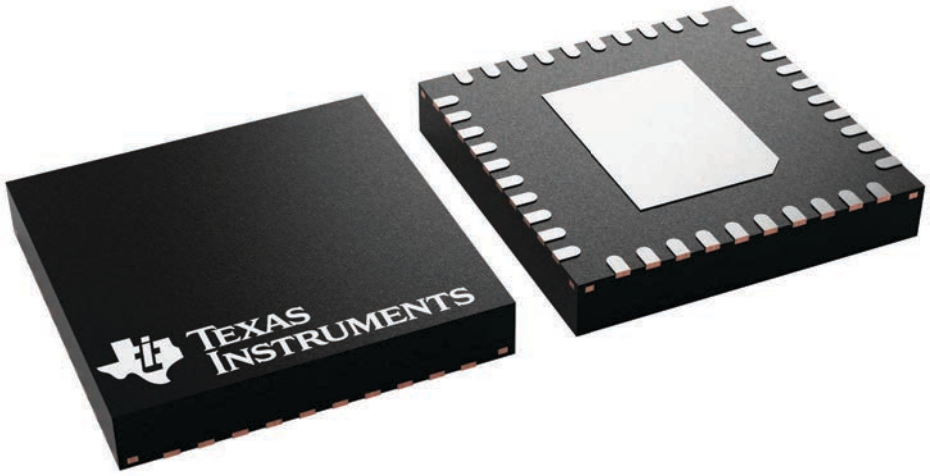
## RHA 40

## VQFN - 1 mm max height

**6 x 6, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



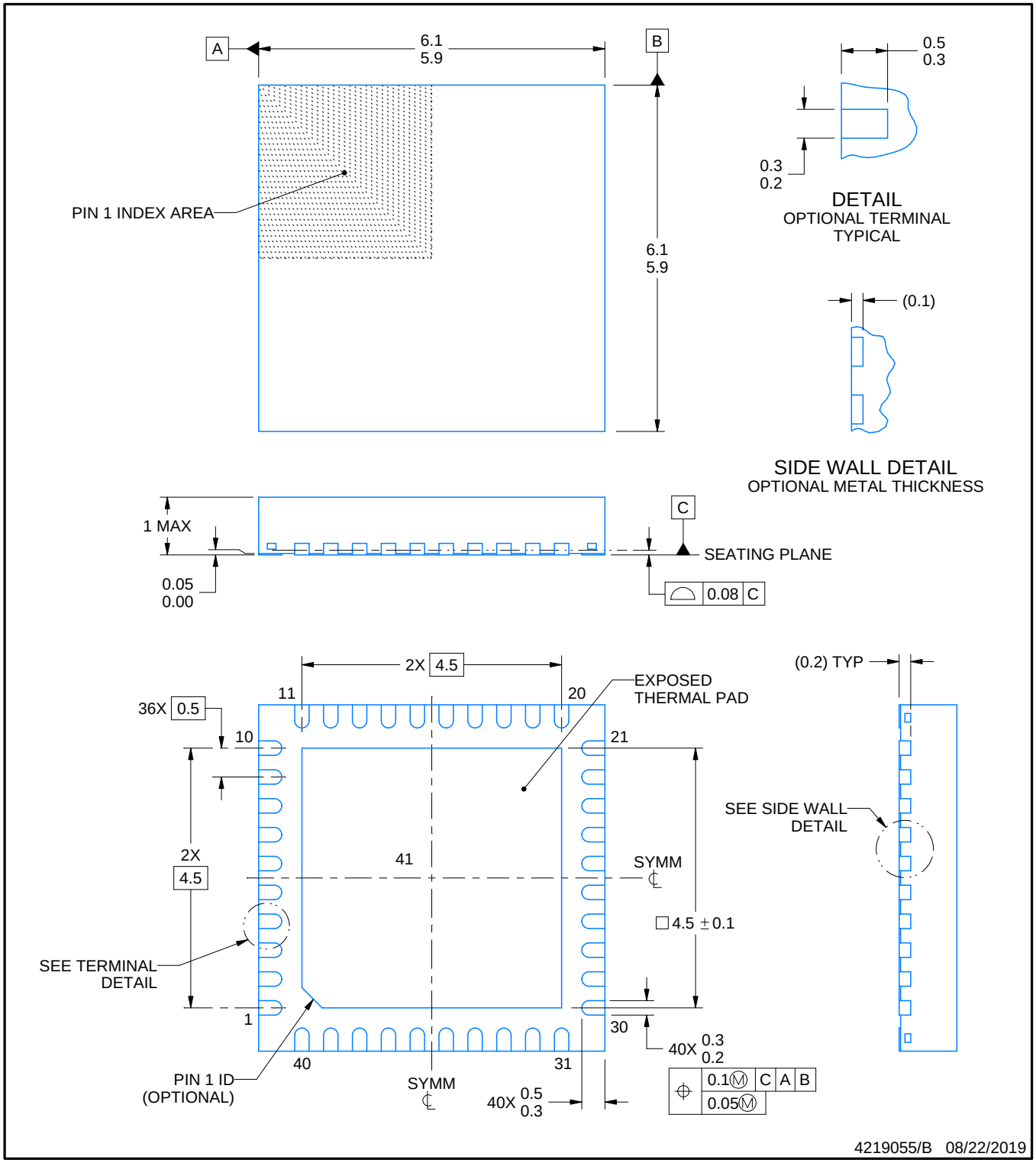

4225870/A

# PACKAGE OUTLINE

## RHA0040H

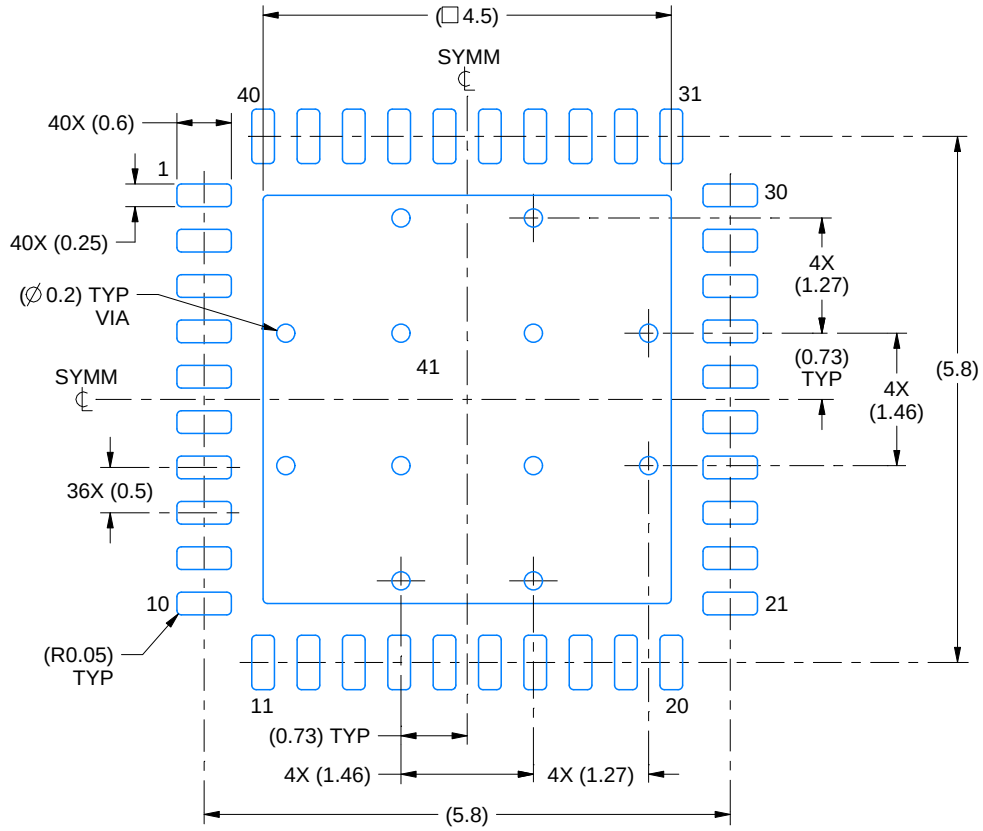
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

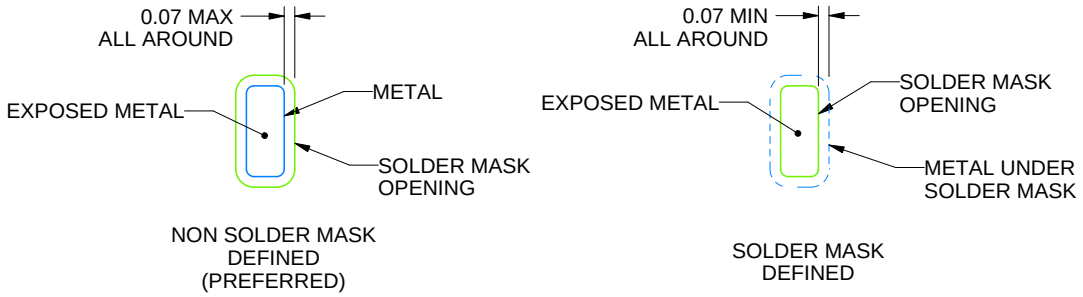



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X




SOLDER MASK DETAILS

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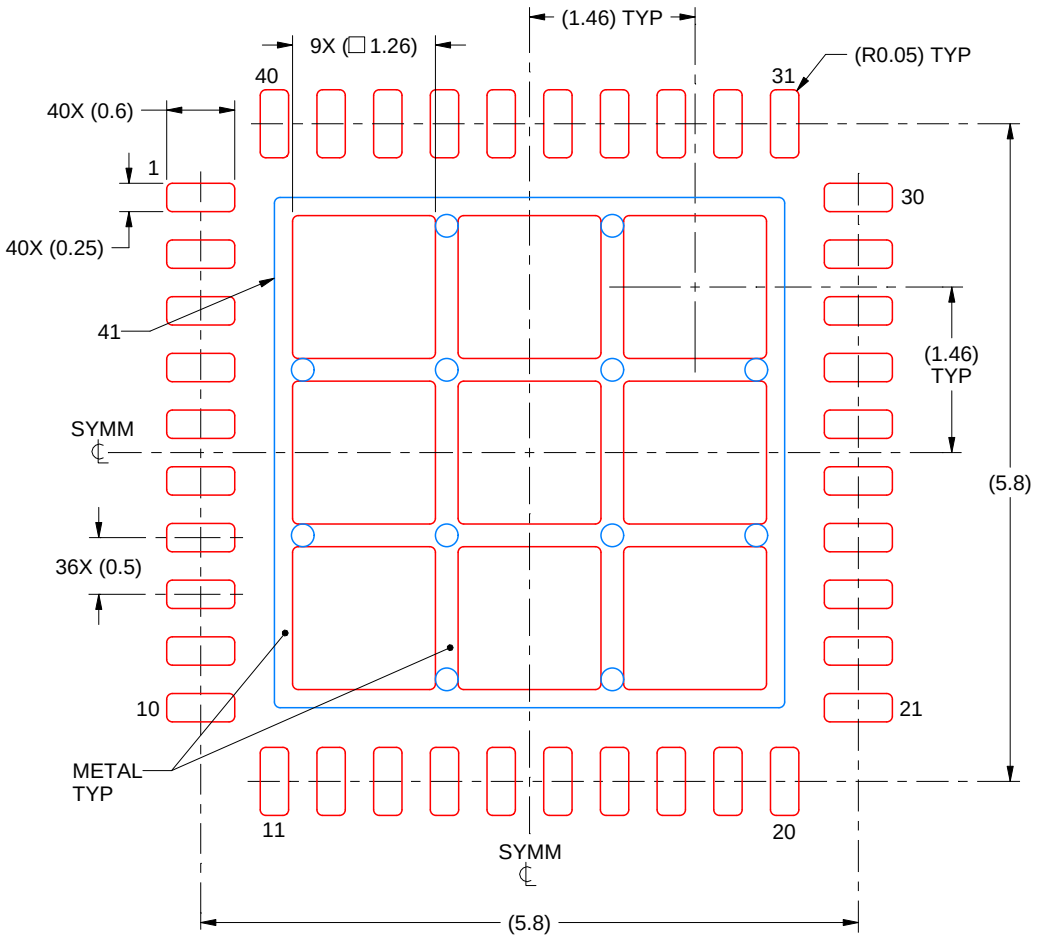
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
70% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265