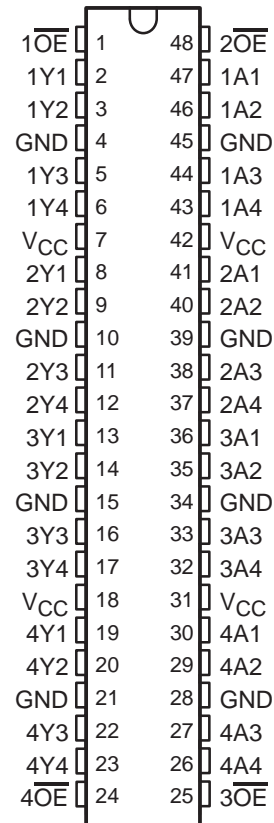


# SN54ABTH16244, SN74ABTH16244 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS677D – SEPTEMBER 1996 – REVISED MARCH 2000

- **Members of the Texas Instruments Widebus™ Family**
- **State-of-the-Art EPIC-II B™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **Typical  $V_{OLP}$  (Output Ground Bounce) <1 V at  $V_{CC} = 5 V$ ,  $T_A = 25^\circ C$**
- **Distributed  $V_{CC}$  and GND Pins Minimize High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200 \text{ pF}$ ,  $R = 0$ )**
- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Packages**

SN54ABTH16244 . . . WD PACKAGE  
SN74ABTH16244 . . . DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



## description

The 'ABTH16244 devices are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ABTH16244 is characterized for operation over the full military temperature range of  $-55^\circ C$  to  $125^\circ C$ . The SN74ABTH16244 is characterized for operation from  $-40^\circ C$  to  $85^\circ C$ .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus and EPIC-II B are trademarks of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2000, Texas Instruments Incorporated  
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54ABTH16244, SN74ABTH16244

## 16-BIT BUFFERS/DRIVERS

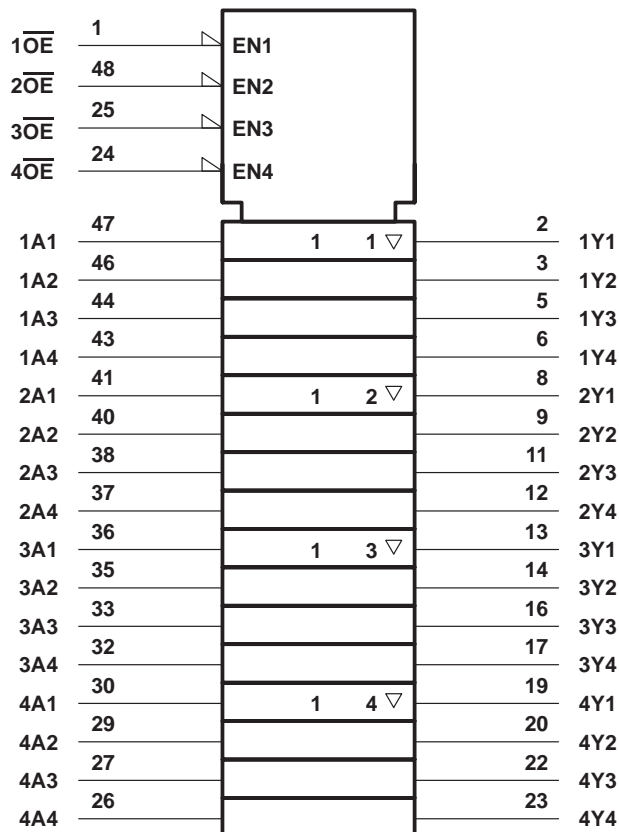
### WITH 3-STATE OUTPUTS

SCBS677D – SEPTEMBER 1996 – REVISED MARCH 2000

FUNCTION TABLE  
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



# SN54ABTH16244, SN74ABTH16244

## 16-BIT BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

SCBS677D – SEPTEMBER 1996 – REVISED MARCH 2000

#### recommended operating conditions (see Note 3)

		SN54ABTH16244		SN74ABTH16244		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-24		-32	mA
I <sub>OL</sub>	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABTH16244		SN74ABTH16244		UNIT
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA	2.5			2.5		2.5		V
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA	3			3		3		
	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -24 mA	2			2			
I <sub>OH</sub> = -32 mA		2*					2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA		0.55		0.55			V
		I <sub>OL</sub> = 64 mA		0.55*			0.55		
V <sub>hys</sub>			100					mV	
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND			±1		±1		±1	μA
I <sub>I</sub> (hold)	V <sub>CC</sub> = 4.5 V	V <sub>I</sub> = 0.8 V	100		100		100		μA
		V <sub>I</sub> = 2 V	-40		-40		-40		
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V			10		10		10	μA
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V			-10		-10		-10	μA
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100				±100	μA
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	Outputs high		50		50		50	μA
I <sub>O‡</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V	-50	-100	-180	-50	-180	-50	-180	mA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high		3		3		3	mA
		Outputs low		32		32		32	
		Outputs disabled		3		3		3	
ΔI <sub>CC</sub> §	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			1.5		1.5		1.5	mA
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V		3						pF
C <sub>o</sub>	V <sub>O</sub> = 2.5 V or 0.5 V		8						pF

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.



**SN54ABTH16244, SN74ABTH16244**  
**16-BIT BUFFERS/DRIVERS**  
**WITH 3-STATE OUTPUTS**

SCBS677D – SEPTEMBER 1996 – REVISED MARCH 2000

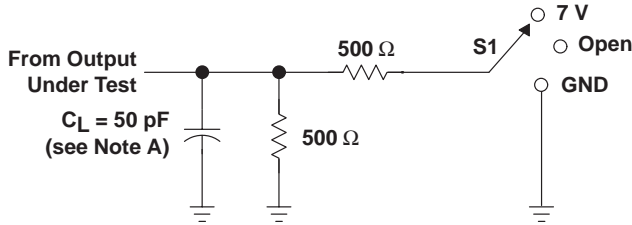
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54ABTH16244		SN74ABTH16244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	1	2.3	3.2	0.7	3.6	1	3.5	ns
$t_{PHL}$			1	2.6	3.7	0.5	4.2	1	4.1	
$t_{PZH}$	$\overline{OE}$	Y	1	3	3.8	0.7	4.9	1	4.8	ns
$t_{PZL}$			1	3.2	4	0.9	5.3	1	4.8	
$t_{PHZ}$	$\overline{OE}$	Y	1	3.6	4.4	0.7	5.3	1	4.8	ns
$t_{PLZ}$			1	2.9	3.7	1	4.6	1	4.1	

**SN54ABTH16244, SN74ABTH16244**  
**16-BIT BUFFERS/DRIVERS**  
**WITH 3-STATE OUTPUTS**

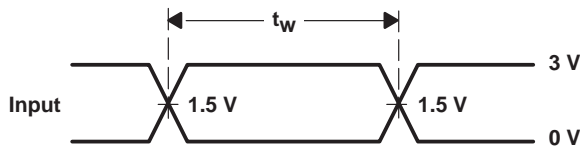
SCBS677D – SEPTEMBER 1996 – REVISED MARCH 2000

**PARAMETER MEASUREMENT INFORMATION**

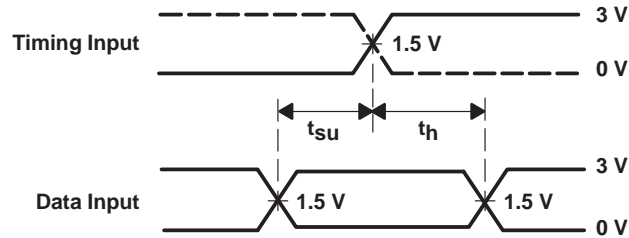


**LOAD CIRCUIT**

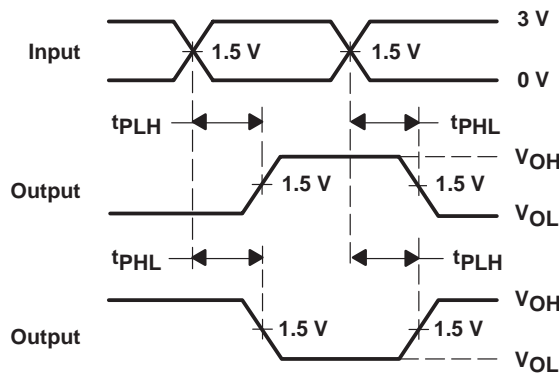
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



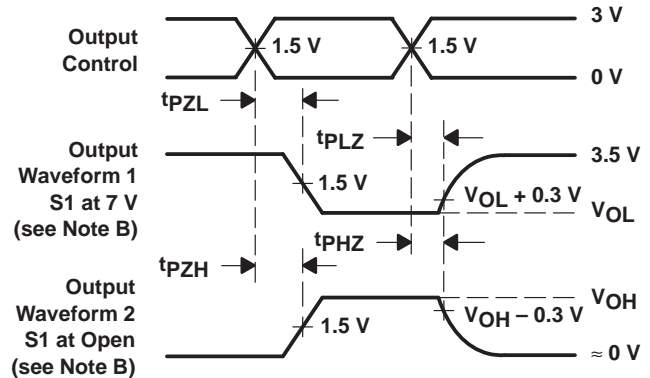
**VOLTAGE WAVEFORMS  
 PULSE DURATION**



**VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES  
 INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES  
 LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ABTH16244DGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH16244	<a href="#">Samples</a>
SN74ABTH16244DL	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH16244	<a href="#">Samples</a>
SN74ABTH16244DLG4	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH16244	<a href="#">Samples</a>
SN74ABTH16244DLR	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH16244	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABTH16244DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74ABTH16244DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABTH16244DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74ABTH16244DLR	SSOP	DL	48	1000	367.0	367.0	55.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ABTH16244DL	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74ABTH16244DLG4	DL	SSOP	48	25	473.7	14.24	5110	7.87

# MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.



4214859/B 11/2020

NOTES:

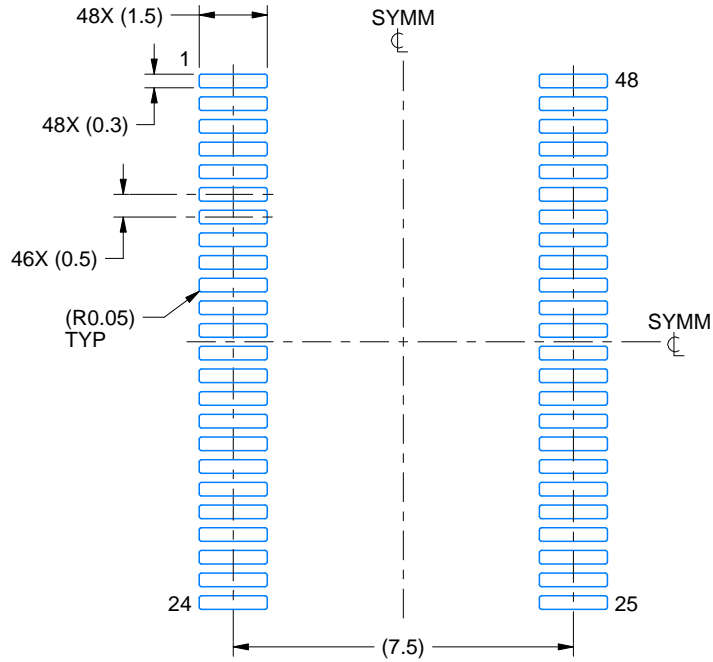
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated