1.5A, 24V, 17MHz 功率运算放大器

查询样品: **OPA564-Q1**

特性

- 符合汽车应用要求
- 高输出电流：**1.5A**
- 宽电源范围：
  - 单电源：**+7V to +24V**
  - 数字电源：**±3.5V** 至 **±12V**
- 大输出摆幅：**20V_{PP}**（在 **1.5A** 电流下）
- 得到了全面的保护：
  - 热关断
  - 可调电流限值
- 诊断标记：
  - 过流
  - 热关断
- 输出启用/关断 控制
- 高速：
  - 增益带宽乘积：**17MHz**
  - 满功率带宽（在 **10V_{PP}** 时）**: 1.3MHz**
  - 转换速率：**40V/μs**
- 用于结温监视的二极管
- **HSOP-20 PowerPAD™** 封装
  （底部和顶部散热焊盘版本）

应用

- 电力线通信
- 阀门、执行器驱动器
- **V_{COM}** 驱动器
- 电机驱动器
- 音频功率放大器
- 电源输出放大器
- 测试设备放大器
- 传感器激励
- 激光二极管驱动器
- 通用型线性功率升高器

说明

OPA564-Q1 是一款低成本、高电流运算放大器，非常适合向电抗性负载输送高达 1.5A 的驱动电流。 高转换速率提供了 1.3MHz 的满功率带宽和卓越的线性。 这些单片式集成电路可在要求苛刻的电力线通信及电机控制应用中提供高可靠性。

OPA564-Q1 采用 7V 至 24V 的单工作电源，或 ±3.5V 至 ±12V 的双工作电源。 在单电源操作中，输入共模范围扩展至负电源。 在最大输出电流条件下，宽输出摆幅可提供一个 20V_{PP}（在 I_{OUT} = 1.5A 时）的电压输出能力（在采用一个标称值为 24V 的电源时）。

OPA564-Q1 在内部提供了针对过热情况及电流过载的保护功能。 它专为提供一个准确、由用户选择的电流限值而设计。 提供了两个标记输出；一个用于指示电流限值，另一个则指示过热情况。 该器件还具有一个启用/关断 引脚，可强制该引脚为低电平以关断输出，从而实际上将负载断接。

OPA564-Q1 内置于耐热增强型的表面贴装 PowerPAD™ 封装 (HSOP-20)，并提供了在封装的顶部或底部安装散热焊盘的选项。

OPA564-Q1相关产品

特性	器件
具有两通道输入多路复用器和 SPI 的零漂移可编程增益放大器 (PGA)	PGA112
零漂移运算放大器、50MHz、轨至轨输入/输出 (RRI/O)、单电源	OPA365
四通道运算放大器、JFET 输入、低噪声	TL074
功率运算放大器、1.2A、15V、17MHz、50V/μs	OPA561

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA564-Q1	HSOP-20 (PowerPAD on bottom)	DWP	OPA564AQ
	HSOP-20 (PowerPAD on top)	DWD	PREVIEW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		OPA564-Q1	UNIT
Supply Voltage, V_S = (V+) – (V–)		+26	V
Signal Input Terminals	Voltage(2)	(V–)–0.4 to (V+)+0.4	V
	Current Through ESD Diodes(2)	±10	mA
	Maximum Differential Voltage Across Inputs(3)	0.5	V
Signal Output Terminals	Voltage	(V–)–0.4 to (V+)+0.4	V
	Current(4)	±10	mA
Output Short-Circuit(5)		Continuous	
Operating Junction Temperature, T_J		–40 to +125	°C
Storage Temperature, T_A		–55 to +150	°C
Junction Temperature, T_J		+150	°C
Latch-up per JESD78B		Class 1 Level B	

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input terminals are diode-clamped to the power-supply rails. Signals that can swing more than 0.4V beyond the supply rails should be current limited to 10mA or less.
(3) Refer to Figure 43 for information on input protection. See *Input Protection* section.
(4) Output terminals are diode-clamped to the power-supply rails. Input signals forcing the output terminal more than 0.4V beyond the supply rails should be current limited to 10mA or less.
(5) Short-circuit to ground within SOA. See *Power Dissipation and Safe Operating Area* for more information.

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ELECTRICAL CHARACTERISTICS

At T_{CASE} = +25°C, V_S = ±12V, R_{LOAD} = 20kΩ to GND, R_{SET} = 7.5kΩ, and E/$\overline{S}$ pin enabled, unless otherwise noted.

PARAMETERS		CONDITIONS	OPA564-Q1 MIN	OPA564-Q1 TYP	OPA564-Q1 MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_{CM} = 0V		±2	±20	mV
vs Temperature	dV_{OS}/dT	T_A = –40°C to 125°C		±10		µV/°C
vs Power Supply	PSRR	V_{CM} = 0V, V_S = ±3.5V to ±13V		10	150	µV/V
INPUT BIAS CURRENT						
Input Bias Current(1)	I_B	V_{CM} = 0V		10	100	pA
vs Temperature		T_A = –40°C to 125°C	See Figure 10, Typical Characteristics			
Input Offset Current(1)	I_{OS}			10	100	pA
NOISE						
Input Voltage Noise Density	e_n	f = 1kHz		102.8		nV/√Hz
		f = 10kHz		20		nV/√Hz
		f = 100kHz		8		nV/√Hz
Input Current Noise	I_n	f = 1kHz		4		fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range:	V_{CM}	Linear Operation	(V–)		(V+)–3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = (V–) to (V+)–3V	70	80		dB
vs Temperature		T_A = –40°C to 125°C	See Figure 9, Typical Characteristics			
INPUT IMPEDANCE						
Differential				10^{12} || 16		Ω || pF
Common-Mode				10^{12} || 9		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	V_{OUT} = 20V_{PP}, R_{LOAD} = 1kΩ	80	108		dB
		V_{OUT} = 20V_{PP}, R_{LOAD} = 10Ω		93		dB
FREQUENCY RESPONSE						
Gain-Bandwidth Product(1)	GBW	R_{LOAD} = 5Ω		17		MHz
Slew Rate	SR	G = 1, 10V Step		40		V/µs
Full Power Bandwidth		G = +2, V_{OUT} = 10V_{PP}		1.3		MHz
Settling Time ±0.1%		G = +1, 10V Step, C_{LOAD} = 100pF		0.6		µs
±0.01%		G = +1, 10V Step, C_{LOAD} = 100pF		0.8		µs
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, R_{LOAD} = 5Ω, G = +1, V_{OUT} = 5V_P		0.003		%
OUTPUT						
Voltage Output:	V_{OUT}					
Positive		I_{OUT} = 0.5A	(V+)–1	(V+)–0.4		V
Negative		I_{OUT} = –0.5A	(V–)+1	(V–)+0.3		V
Positive		I_{OUT} = 1.5A	(V+)–2	(V+)–1.5		V
Negative		I_{OUT} = –1.5A	(V–)+2	(V–)+1.1		V

(1) See Typical Characteristics.

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ELECTRICAL CHARACTERISTICS (continued)

At T_{CASE} = +25°C, V_S = ±12V, R_{LOAD} = 20kΩ to GND, R_{SET} = 7.5kΩ, and E/$\overline{S}$ pin enabled, unless otherwise noted.

PARAMETERS		CONDITIONS	OPA564-Q1 MIN	OPA564-Q1 TYP	OPA564-Q1 MAX	UNIT
OUTPUT, continued						
Maximum Continuous Current, dc	I_{OUT}			1.5(2)		A
Output Impedance, closed loop	R_O	f = 100kHz		10		Ω
Output Impedance, open loop	Z_O	G = +2, f = 100kHz	See Figure 24, Typical Characteristics			
Output Current Limit Range(3)				±0.4 to ±2.0		A
Current Limit Equation	I_{LIM}		$I_{LIM} \cong 20000 \times \left[\frac{1.2V}{5000 + R_{SET}}\right]$ (4) (5)			A
		Solved for R_{SET} (Current Limit)	$R_{SET} \cong (24k/I_{LIM}) - 5k\Omega$			Ω
Current Limit Accuracy		I_{LIM} = 1.5A		10		%
Current Limit Overshoot(6) (7)		V_{IN} = 5V Pulse (200ns t_r), G = +2		50		%
Output Shut Down						
Output Impedance(8)				6 || 120		GΩ || pF
Capacitive Load Drive	C_{LOAD}		See Figure 6, Typical Characteristics			
DIGITAL CONTROL						
Enable/$\overline{\text{Shutdown}}$ Mode INPUT		V_{DIG} = +3.3V to +5.5V referenced to V–				
$V_{E/\overline{S}}$ High (output enabled)		E/$\overline{S}$ Pin Open or Forced High	(V–)+2		(V–)+V_{DIG}	V
$V_{E/\overline{S}}$ Low (output shut down)		E/$\overline{S}$ Pin Forced Low	(V–)		(V–)+0.8	V
$I_{E/\overline{S}}$ High (output enabled)		E/$\overline{S}$ Pin Indicates High		10		µA
$I_{E/\overline{S}}$ Low (output shut down)		E/$\overline{S}$ Pin Indicates Low		1		µA
Output Shutdown Time				1		µs
Output Enable Time				3		µs
Current Limit Flag Output						
Normal Operation		Sinking 10µA		0	(V–)+0.8	V
Current-Limited		Sourcing 20µA	(V–)+2	V_{DIG}		V
Thermal Shutdown						
Normal Operation		Sinking 200µA		0	(V–)+0.8	V
Thermally Shutdown(9)		Sourcing 200µA	(V–)+2	V_{DIG}		V
Junction Temperature at Shutdown(10)				+140 to +157		°C
Hysteresis(10)				15 to 19		°C
T_{SENSE}						
Diode Ideality Factor	η			1.033		

(2) Under safe operating conditions. See *Power Dissipation and Safe Operating Area* for safe operating area (SOA) information.
(3) Minimum current limit is 0.4A. See *Adjustable Current Limit* in the *Applications* section.
(4) Quiescent current increases when the current limit is increased (see Typical Characteristics).
(5) R_{SET} (current limit) can range from 55kΩ (I_{OUT} = 400mA) to 10kΩ (I_{OUT} = 1.6A typ). See *Adjustable Current Limit* in the *Applications* section.
(6) See Typical Characteristics.
(7) Transient load transition time must be ≥ 200ns.
(8) See *Enable/Shutdown (E/S) Pin* in the *Applications* section.
(9) When sourcing, the V_{DIG} supply must be able to supply the current.
(10) Characterized, but not production tested.

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ELECTRICAL CHARACTERISTICS (continued)

At T_{CASE} = +25°C, V_S = ±12V, R_{LOAD} = 20kΩ to GND, R_{SET} = 7.5kΩ, and E/$\overline{S}$ pin enabled, unless otherwise noted.

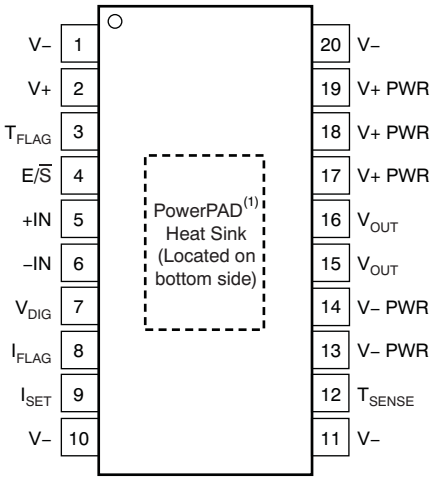
PARAMETERS		CONDITIONS	OPA564-Q1 MIN	OPA564-Q1 TYP	OPA564-Q1 MAX	UNIT
POWER SUPPLY(11)						
Specified Voltage Range	V_S			±12		V
Operating Voltage Range			7		24	V
Quiescent Current(12)	I_Q	I_{OUT} = 0		39	50	mA
Over Temperature		T_A = –40°C to 125°C			50	mA
Quiescent Current in Shutdown Mode	I_{QSD}				5	mA
Specified Voltage for Digital	V_{DIG}		(V–) + 3.0		(V–) + 5.5	V
Digital Quiescent Current	I_{DIG}	V_{DIG} = 5V		43	100	µA
TEMPERATURE RANGE						
Operating Range			–40		+125(13)	°C
Thermal Resistance						
HSOP-20 DWP PowerPAD (Pad Down)	θ_{JA}	High K Board		33		°C/W
	θ_{JC}			50		°C/W
	θ_{JP}			1.83		°C/W
	θ_{JB}			22		°C/W
HSOP-20 DWD PowerPAD (Pad Up)(14)	θ_{JA}	High K Board		45.5		°C/W
	θ_{JC}			6.3		°C/W
	θ_{JB}			22		°C/W

(11) Power-supply sequencing requirements must be observed. See *Power Supplies* section for more information.
(12) Quiescent current increases when the current limit is increased (see Typical Characteristics).
(13) The OPA564-Q1 typically goes into thermal shutdown at a junction temperature above +140°C.
(14) Thermal modeling of the DWD-20 package was done based on a 1-inch AAVID Thermalloy heatsink (Thermalloy part no. 65810).

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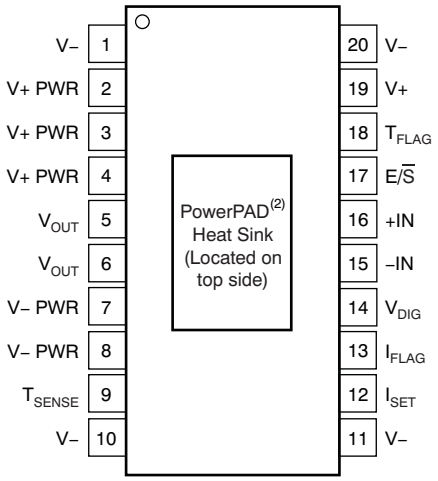
PIN CONFIGURATIONS

DWP PACKAGE
PowerPAD on Bottom



(1) PowerPAD is internally connected to V–, Soldering the PowerPAD to the PCB is always required, even with applications that have low power dissipation.

DWD PACKAGE
PowerPAD on Top



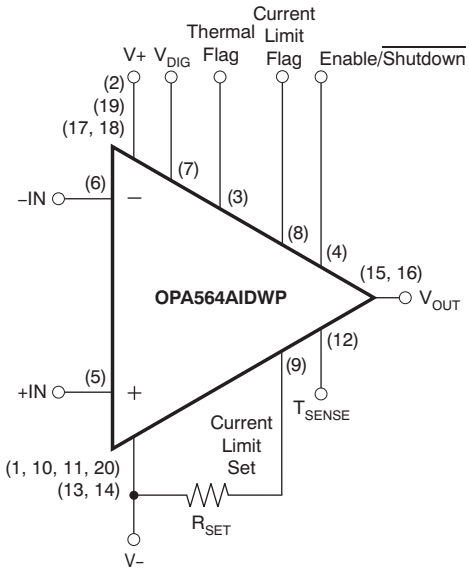
(2) PowerPAD is internally connected to V–.

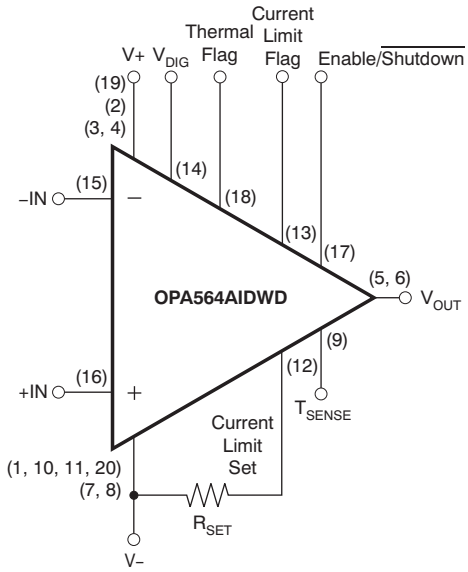
PIN DESCRIPTIONS

DWP (PAD DOWN) PIN NO.	DWD (PAD UP) PIN NO.	NAME	DESCRIPTION
1, 10, 11, 20	1, 10, 11, 20	V–	–Supply for Amplifier, PWR Out, and Metal PowerPAD
2	19	V+	+Supply for Signal Amplifier
3	18	T_{FLAG}	Thermal Over Temperature Flag; flag is high when alarmed and device has gone into thermal shutdown.
4	17	E/$\overline{S}$	Enable/$\overline{\text{Shutdown}}$ Output Stage; take E/$\overline{S}$ low to shut down output
5	16	+IN	Noninverting Op Amp Input
6	15	–IN	Inverting Op Amp Input
7	14	V_{DIG}	+Supply for Digital Flag and E/$\overline{S}$ (referenced to V–). Valid Range is (V–) + 3.0V ≤ V_{DIG} ≤ (V–) + 5.5V.
8	13	I_{FLAG}	Current Limit Flag; Active High
9	12	I_{SET}	Current Limit Set (see *Applications* Section)
12	9	T_{SENSE}	Temperature Sense Pin for use with TMP411
13, 14	7, 8	V– PWR	–Supply for Power Output Stage
15, 16	5, 6	V_{OUT}	Output Voltage; R_O is high impedance when shut down
17, 18, 19	3, 4, 2	V+ PWR	+Supply for Power Output Stage

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FUNCTIONAL PIN DIAGRAM





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TYPICAL CHARACTERISTICS

At T_{CASE} = +25°C, V_S = ±12V, R_{LOAD} = 20kΩ to GND, R_{SET} = 7.5kΩ, and E/$\overline{S}$ pin enabled, unless otherwise noted.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

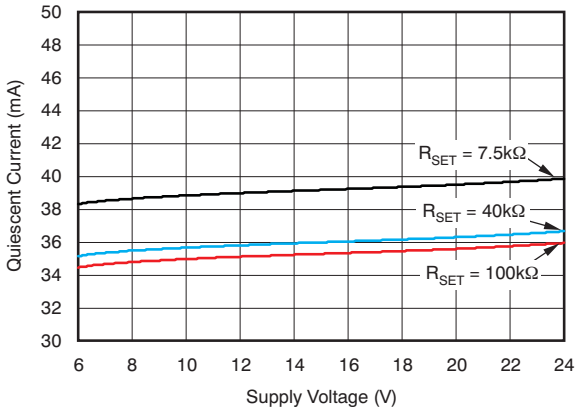


Figure 1.

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

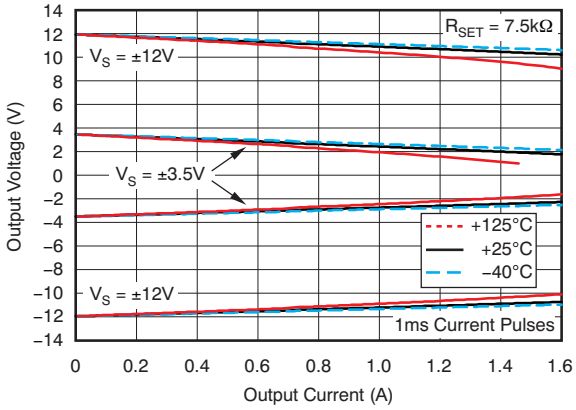


Figure 2.

LARGE−SIGNAL STEP RESPONSE, NO LOAD

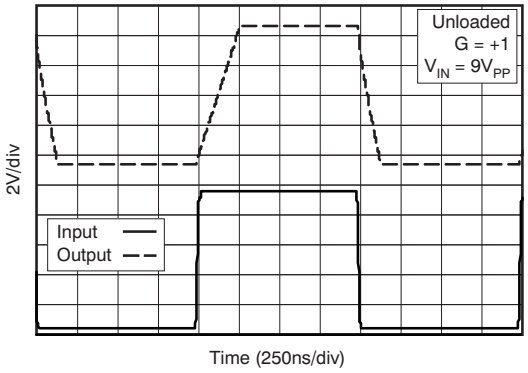


Figure 3.

LARGE−SIGNAL STEP RESPONSE

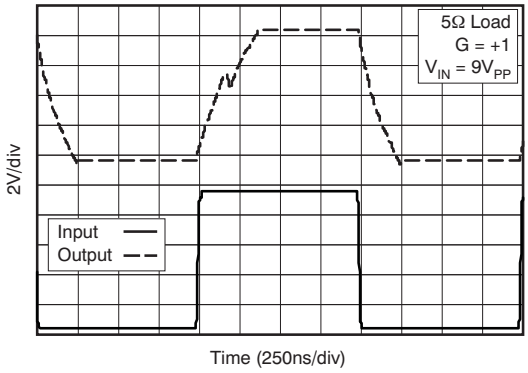


Figure 4.

SMALL−SIGNAL STEP RESPONSE

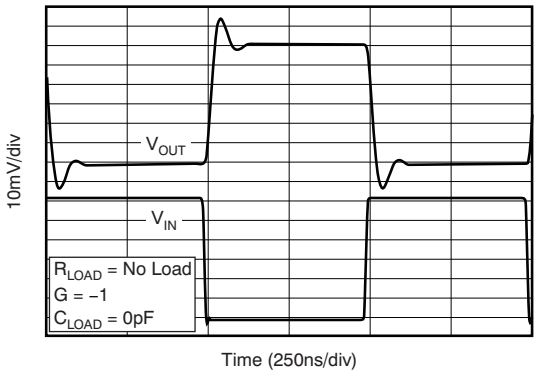


Figure 5.

SMALL−SIGNAL OVERSHOOT vs LOAD CAPACITANCE

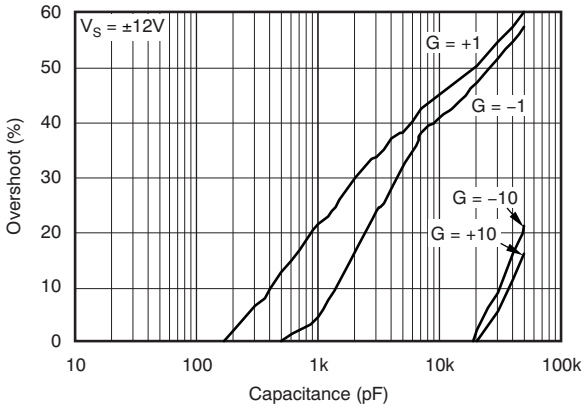


Figure 6.

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TYPICAL CHARACTERISTICS (continued)

At T_{CASE} = +25°C, V_S = ±12V, R_{LOAD} = 20kΩ to GND, R_{SET} = 7.5kΩ, and E/$\overline{S}$ pin enabled, unless otherwise noted.

I_Q vs TEMPERATURE

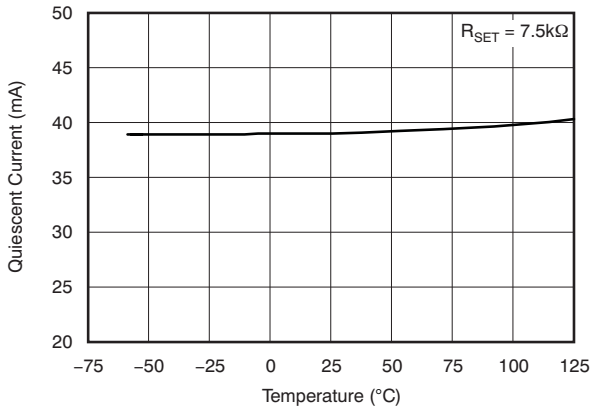


Figure 7.

OFFSET VOLTAGE vs TEMPERATURE

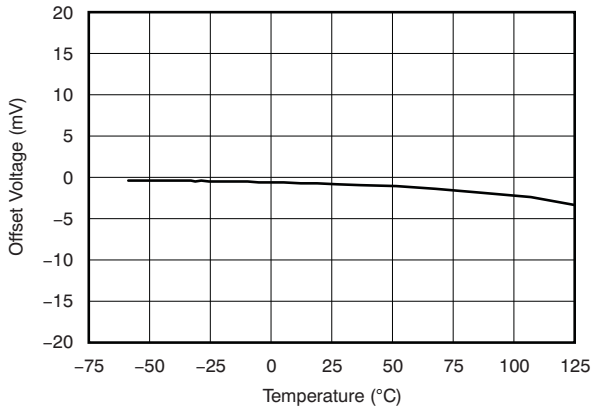


Figure 8.

A_{OL}, PSRR, AND CMRR vs TEMPERATURE

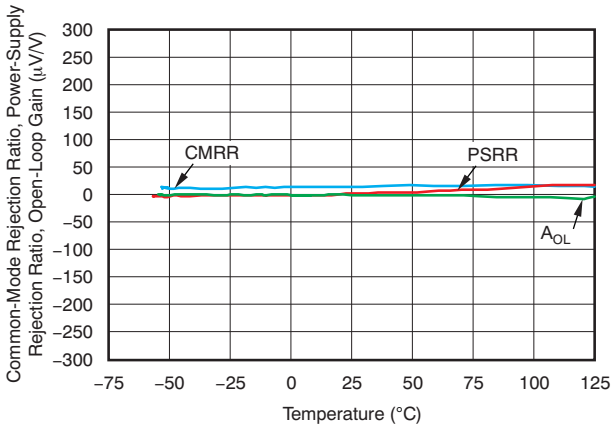


Figure 9.

I_B vs TEMPERATURE

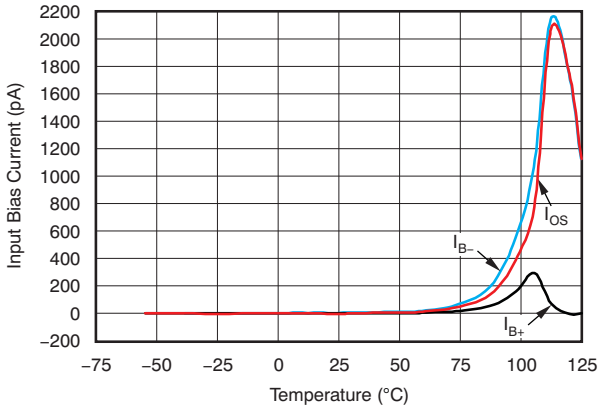


Figure 10.

I_Q, SHUTDOWN vs TEMPERATURE

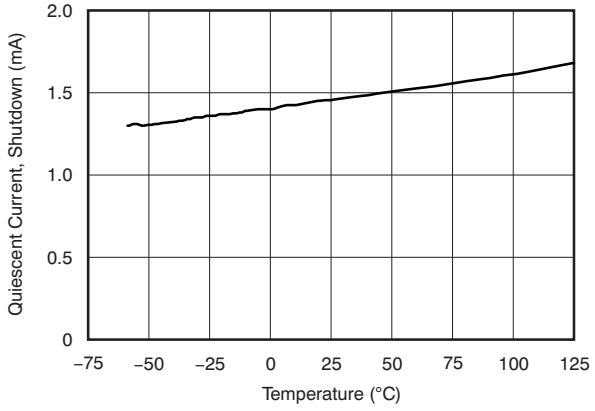


Figure 11.

I_{DIG} vs TEMPERATURE

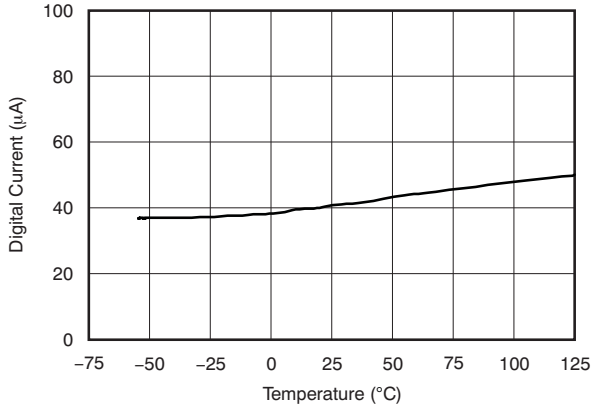


Figure 12.

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TYPICAL CHARACTERISTICS (continued)

At T_{CASE} = +25°C, V_S = ±12V, R_{LOAD} = 20kΩ to GND, R_{SET} = 7.5kΩ, and E/$\overline{S}$ pin enabled, unless otherwise noted.

GAIN AND PHASE vs FREQUENCY

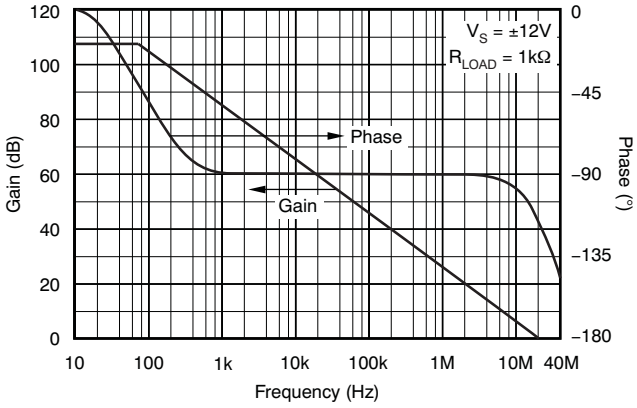


Figure 13.

COMMON-MODE REJECTION RATIO AND POWER-SUPPLY REJECTION RATIO vs FREQUENCY

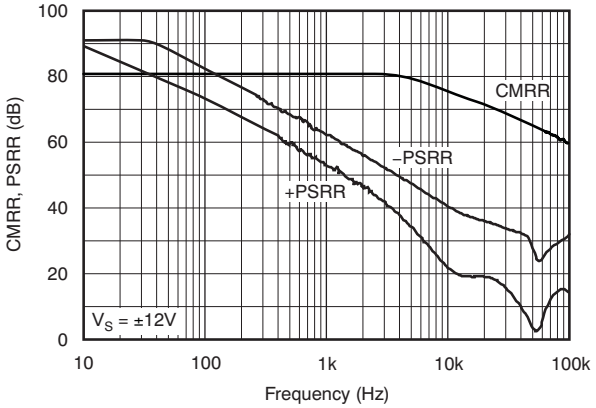


Figure 14.

OUTPUT VOLTAGE SWING vs FREQUENCY

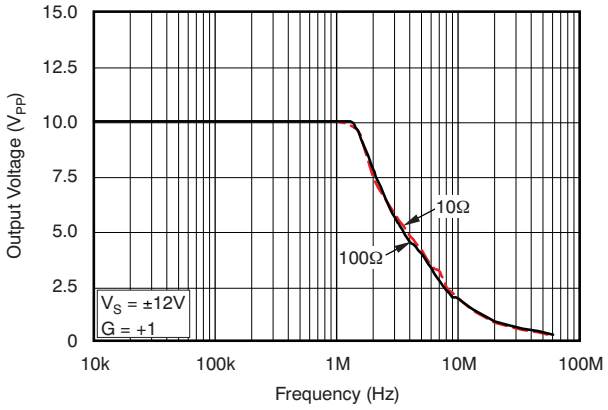


Figure 15.

OUTPUT VOLTAGE SWING vs FREQUENCY

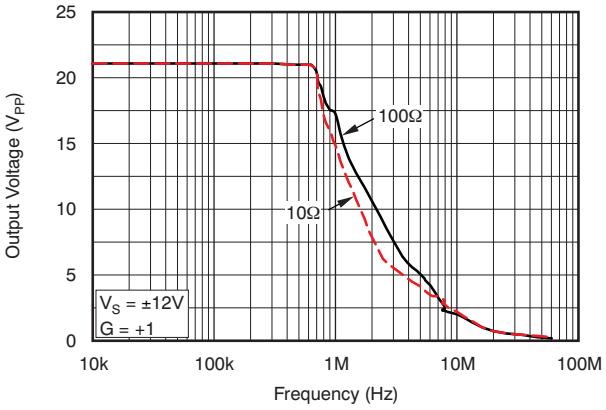


Figure 16.

TOTAL HARMONIC DISTORTION + NOISE vs AMPLITUDE

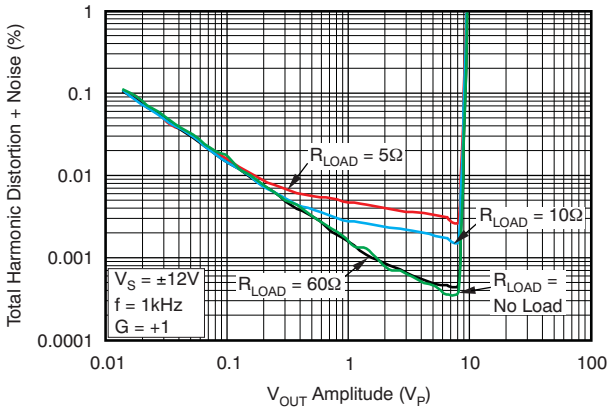


Figure 17.

TOTAL HARMONIC DISTORTION + NOISE vs AMPLITUDE

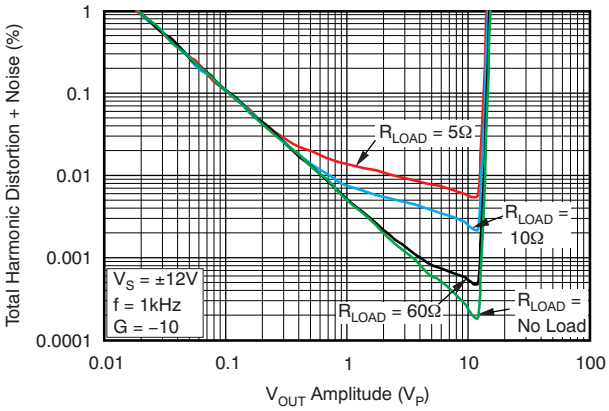


Figure 18.

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TYPICAL CHARACTERISTICS (continued)

At T_{CASE} = +25°C, V_S = ±12V, R_{LOAD} = 20kΩ to GND, R_{SET} = 7.5kΩ, and E/$\overline{S}$ pin enabled, unless otherwise noted.

TOTAL HARMONIC DISTORTION + NOISE vs AMPLITUDE

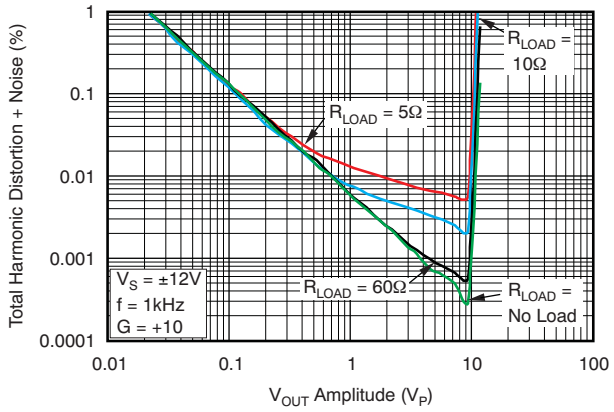


Figure 19.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

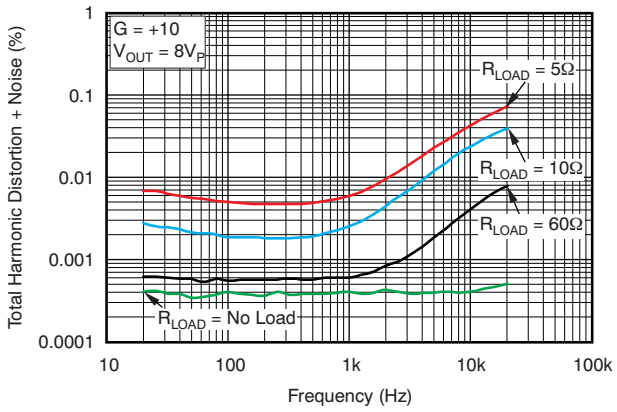


Figure 20.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

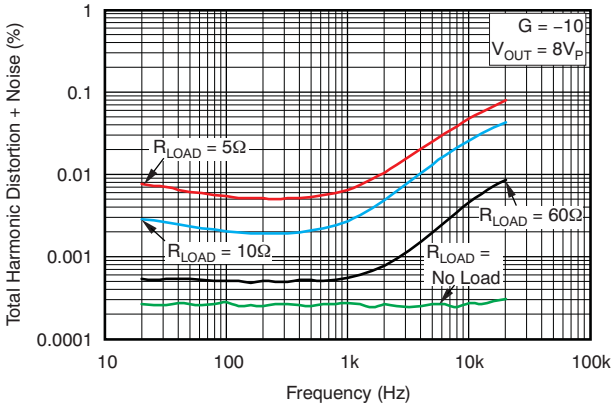


Figure 21.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

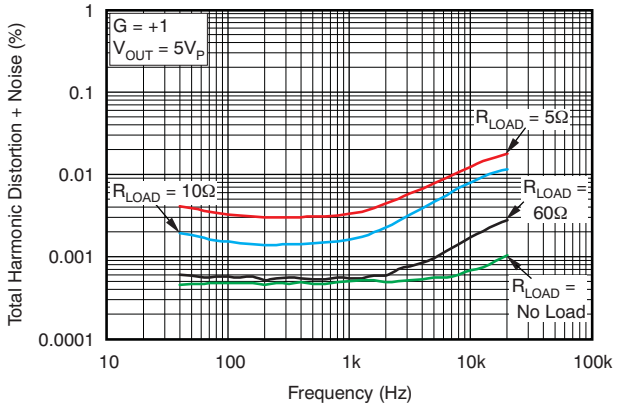


Figure 22.

INPUT VOLTAGE SPECTRAL NOISE AND CURRENT NOISE vs FREQUENCY

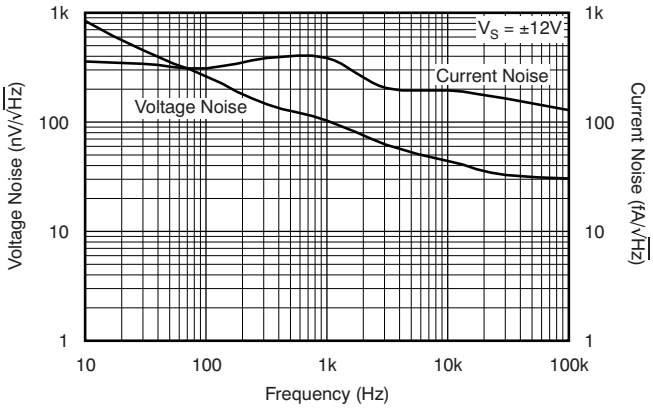


Figure 23.

OPEN-LOOP OUTPUT IMPEDANCE (No Load)

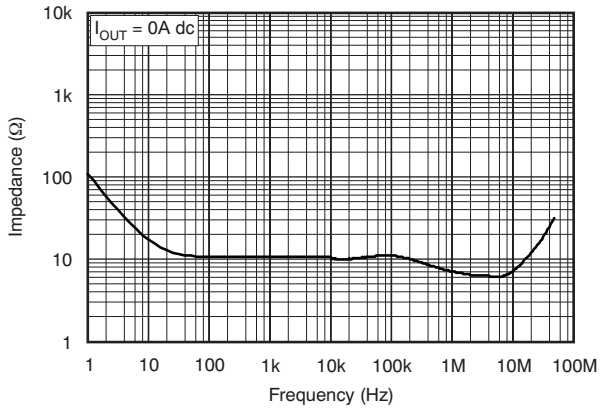


Figure 24.

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TYPICAL CHARACTERISTICS (continued)

At T_{CASE} = +25°C, V_S = ±12V, R_{LOAD} = 20kΩ to GND, R_{SET} = 7.5kΩ, and E/$\overline{S}$ pin enabled, unless otherwise noted.

CLOSED-LOOP OUTPUT IMPEDANCE (No Load)

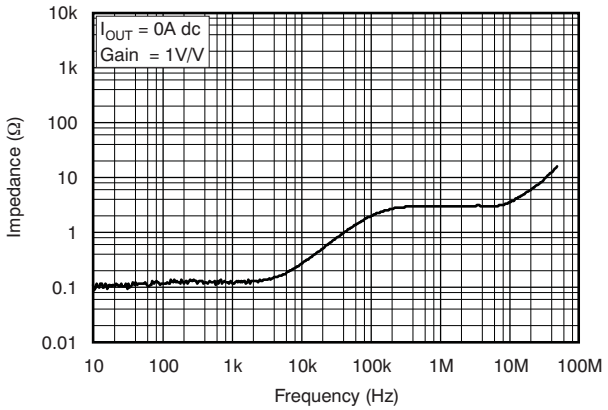


Figure 25.

INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

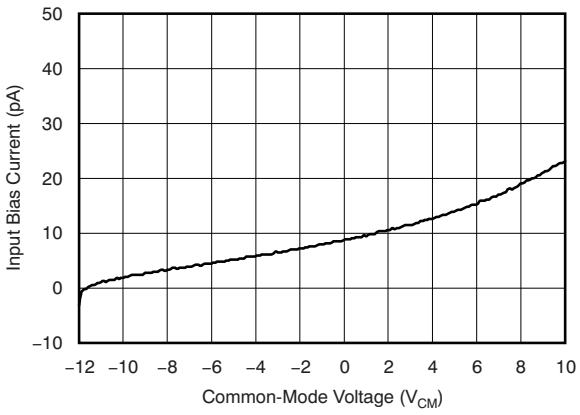


Figure 26.

ENABLE RESPONSE
R_{LOAD} = 100Ω

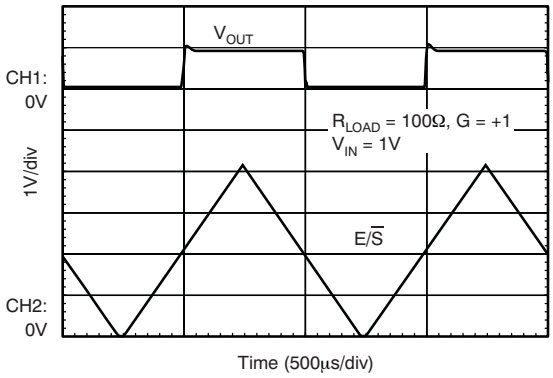


Figure 27.

SHUTDOWN TIME (INVERTING CONFIGURATION)

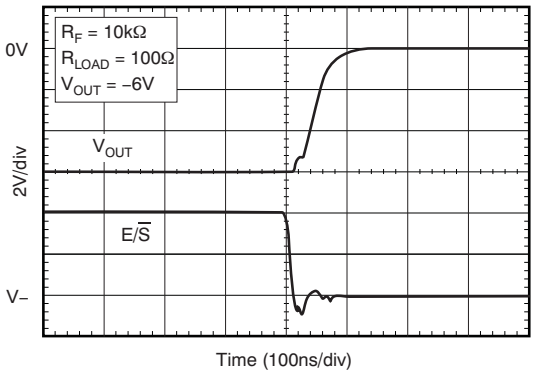


Figure 28.

ENABLE TIME (INVERTING CONFIGURATION)

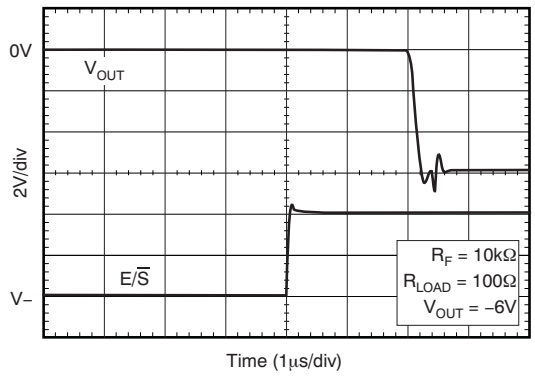


Figure 29.

CURRENT LIMIT PERCENT ERROR vs R_{SET}

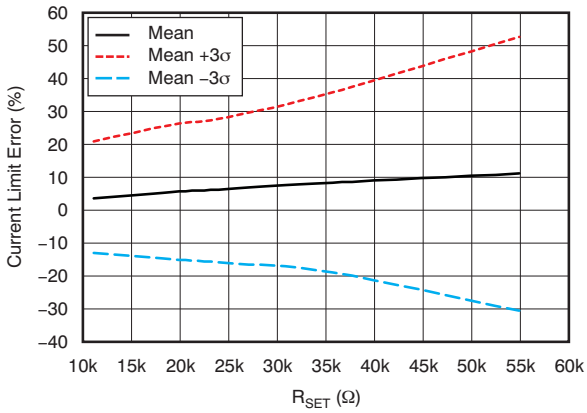


Figure 30.

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TYPICAL CHARACTERISTICS (continued)

At T_{CASE} = +25°C, V_S = ±12V, R_{LOAD} = 20kΩ to GND, R_{SET} = 7.5kΩ, and E/$\overline{S}$ pin enabled, unless otherwise noted.

OUTPUT CURRENT LIMIT vs R_{SET} (SOURCING CURRENT)

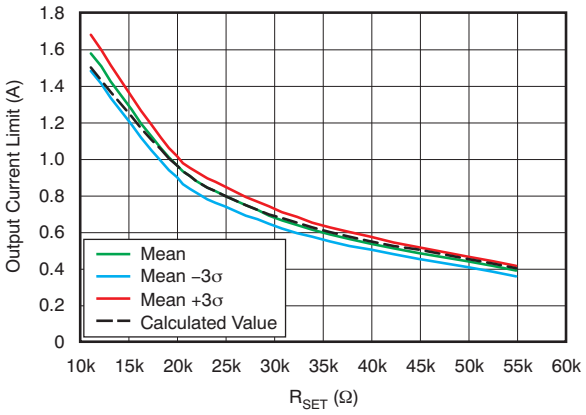


Figure 31.

OUTPUT CURRENT LIMIT vs R_{SET} (SINKING CURRENT)

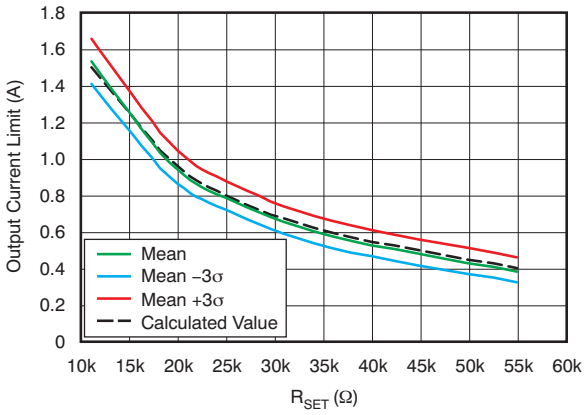


Figure 32.

QUIESCENT CURRENT INCREASE vs R_{SET}

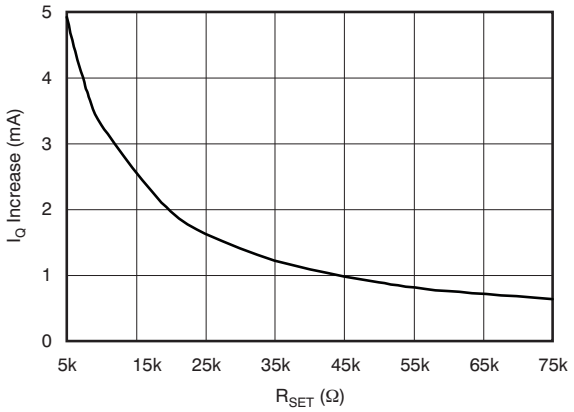


Figure 33.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

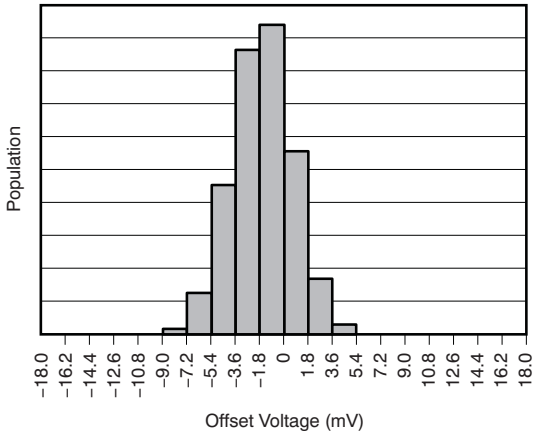


Figure 34.

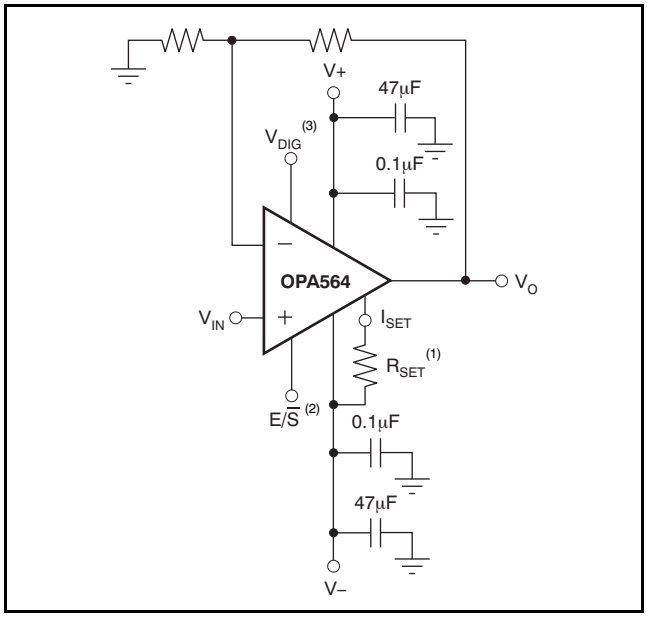
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APPLICATION INFORMATION

BASIC CONFIGURATION

Figure 35 shows the OPA564-Q1 connected as a basic noninverting amplifier. However, the OPA564-Q1 can be used in virtually any op amp configuration.

Power-supply terminals should be bypassed with low series impedance capacitors. The technique of using ceramic and tantalum capacitors in parallel is recommended. Power-supply wiring should have low series impedance.



(1) R_{SET} sets the current limit value from 0.4A to 1.5A.

(2) E/$\overline{S}$ pin forced low shuts down the output.

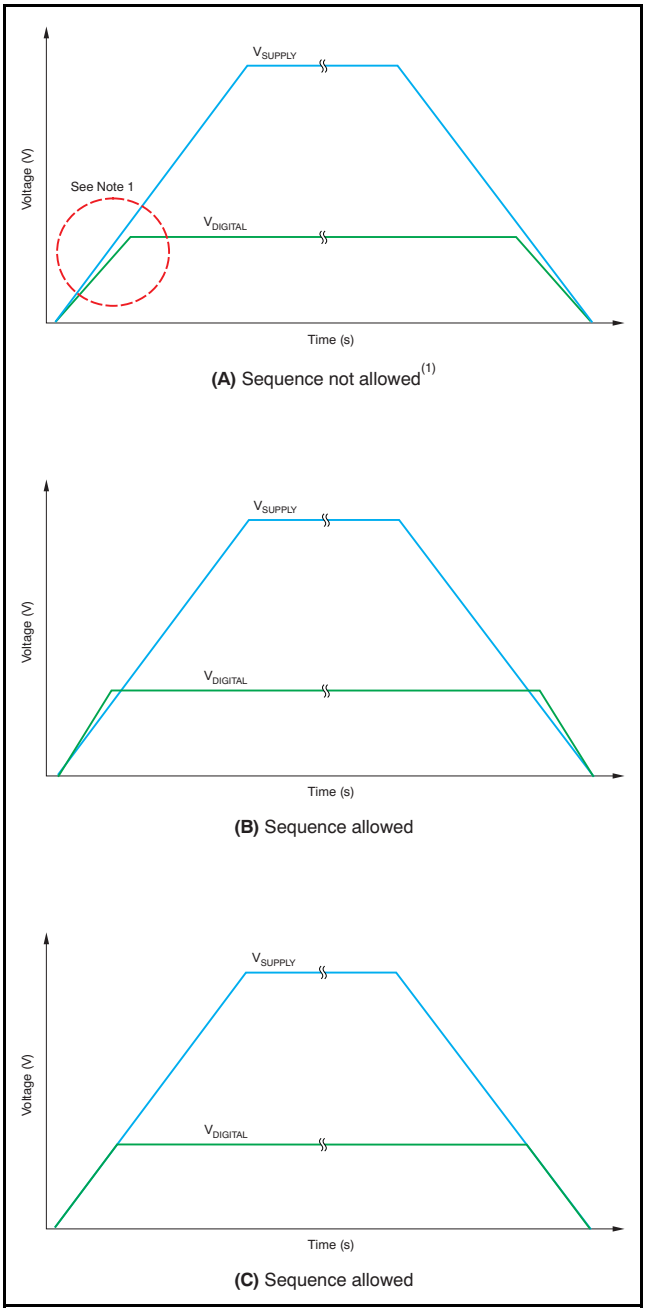
(3) V_{DIG} must not exceed (V–) + 5.5V; see Figure 56 for examples of generating a signal for V_{DIG}.

Figure 35. Basic Noninverting Amplifier

POWER SUPPLIES

The OPA564-Q1 operates with excellent performance from single (+7V to +24V) or dual (±3.5V to ±12V) analog supplies and a digital supply of +3.3V to +5.5V (referenced to the V– pin). Note that the analog power-supply voltages do not need to be symmetrical, as long as the total voltage remains below 24V. For example, the positive supply could be set to 14V with the negative supply at –10V. Most behaviors remain constant across the operating voltage range. Parameters that vary significantly with operating voltage are shown in the Typical Characteristics.

Sequencing of power supplies must assure that the digital supply voltage (V_{DIG}) be applied before the supply voltage to prevent damage to the OPA564-Q1. Figure 36 shows acceptable versus unacceptable power-supply sequencing.



(1) The power-supply sequence illustrated in (A) is not allowed. This power-supply sequence causes damage to the device.

Figure 36. Power-Supply Sequencing

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ADJUSTABLE CURRENT LIMIT

The OPA564-Q1 provides over-current protection to the load through its accurate, user-adjustable current limit (I_{SET} pin). The current limit value, I_{LIM}, can be set from 0.4A to 1.5A by controlling the current through the I_{SET} pin. Setting the current limit does not require special power resistors. The output current does not flow through the I_{SET} pin.

A simple resistor to the negative rail is sufficient for a general, coarse limit of the output current. Figure 30 exhibits the percent of error in the transfer function between I_{SET} and I_{OUT} versus the current limit set resistor, R_{SET}; Figure 31 and Figure 32 show how this error translates to variation in I_{OUT} versus R_{SET}. The dotted line represents the ideal output current setting which is determined by the following equation:

$$I_{LIM} \cong 20000 \times \left(\frac{1.2V}{5000 + R_{SET}} \right) \quad (1)$$

The mismatch errors between the current limit set mirror and the output stage are primarily a result of variations in the ~1.2V bandgap reference, an internal 5kΩ resistor, the mismatch between the current limit and the output stage mirror, and the tolerance and temperature coefficient of the R_{SET} resistor referenced to the negative rail. Additionally, an increase in junction temperature can induce added mismatch in accuracy between the I_{SET} and I_{OUT} mirror. See Figure 53 for a method that can be used to dynamically change the current limit setting using a simple, zero drift current source. This approach simplifies the current limit equation to the following:

$$I_{LIM} \cong 20{,}000 \times I_{SET} \quad (2)$$

The current into the I_{SET} pin is determined by the NPN current source. Therefore, the errors contributed by the internal 1.2V bandgap reference and the 5kΩ resistor mismatch are eliminated, thus improving the overall accuracy of the transfer function. In this case, the primary source of error in I_{SET} is the R_{SET} resistor tolerance and the beta of the NPN transistor.

It is important to note that the primary intent of the current limit on the OPA564-Q1 is coarse protection of the output stage; therefore, the user should exercise caution when attempting to control the output current by dynamically toggling the current limit setting. Predictable performance is better achieved by controlling the output voltage through the feedback loop of the OPA564-Q1.

Setting the Current Limit

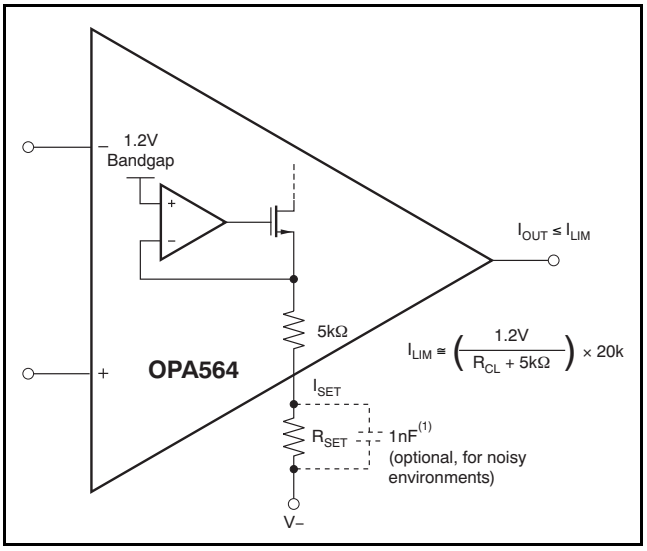
Leaving the I_{SET} pin unconnected damages the device. Connecting I_{SET} directly to V– is not recommended because it programs the current limit far beyond the 1.5A capability of the device and causes excess power dissipation. The minimum recommended value for R_{SET} is 7.5kΩ, which programs the maximum current limit to approximately 1.9A. The maximum value for R_{SET} is 55kΩ, which programs the minimum current limit to approximately 0.4A. The simplest method for adjusting the current limit (I_{LIM}) uses a resistor or potentiometer connected between the I_{SET} pin and V–, according to Equation 1.

If I_{LIM} has been defined, R_{SET} can be solved by rearranging Equation 1 into Equation 3:

$$R_{SET} \cong \left(\frac{24k\Omega}{I_{LIM}} \right) - 5k\Omega \quad (3)$$

R_{SET} in combination with a 5kΩ internal resistor determines the magnitude of a small current that sets the desired output current limit.

Figure 37 shows a simplified schematic of the OPA564-Q1 current limit architecture.



(1) At power-on, this capacitor is not charged. Therefore, the OPA564-Q1 is programmed for maximum output current. Capacitor values > 1nF are not recommended.

Figure 37. Adjustable Current Limit

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ENABLE/SHUTDOWN (E/$\overline{S}$) PIN

The output of the OPA564-Q1 shuts down when the E/$\overline{S}$ pin is forced low. For normal operation (output enabled), the E/$\overline{S}$ pin must be pulled high (at least 2V above V–). To enable the OPA564-Q1 permanently, the E/$\overline{S}$ pin can be left unconnected. The E/$\overline{S}$ pin has an internal 100kΩ pull-up resistor. When the output is shut down, the output impedance of the OPA564-Q1 is 6GΩ || 120pF. The output shutdown output voltage versus output current is shown in Figure 42. Although the output is high-impedance when shut down, there is still a path through the feedback network into the input stage to ground; see Figure 43. To prevent damage to the OPA564-Q1, ensure that the voltage across the input terminals +IN and –IN does not exceed 0.5V, and that the current flowing through the input terminals does not exceed 10mA when operated beyond the supply rails, V– and V+. Refer to the *Input Protection* section.

Input Protection

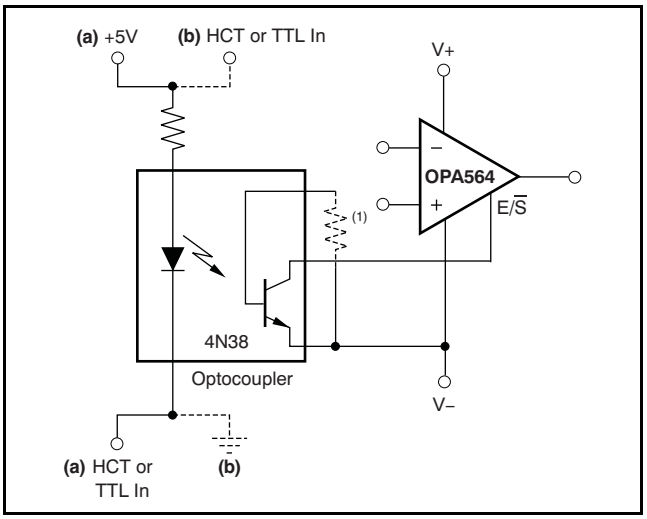
Electrostatic discharge (ESD) protection followed by back-to-back diodes and input resistors (see Figure 43) are used for input protection on the OPA564-Q1. Exceeding the turn-on threshold of these diodes, as in a pulse condition, can cause current to flow through the input protection diodes because of the finite slew rate of the amplifier. If the input current is not limited, the back-to-back diodes and the input devices can be destroyed. Sources of high input current can also cause subtle damage to the amplifier. Although the unit may still be functional, important parameters such as input offset voltage, drift, and noise may shift.

When using the OPA564-Q1 as a unity-gain buffer (follower), as an inverting amplifier, or in shutdown mode, the input voltage between the input terminals (+IN and –IN) must be limited so that the voltage does not exceed 0.5V. This condition must be maintained across the entire common-mode range from V– to V+. If the inputs are taken above either supply rail, the current must be limited to 10mA through the ESD protection diodes. During excursions past the rails, it is still necessary to limit the voltage across the input terminals. If necessary, external back-to-back diodes should be added between +IN and –IN to maintain the 0.5V requirement between these connections.

Output Shutdown

The shutdown pin (E/$\overline{S}$) is referenced to the negative supply (V–). Therefore, shutdown operation is slightly different in single-supply and dual-supply applications. In single-supply operation, V– typically equals common ground. Therefore, the shutdown logic signal and the OPA564-Q1 shutdown pin are referenced to the same potential. In this configuration, the logic pin and the OPA564-Q1 enable can simply be connected together. Shutdown occurs for voltage levels of less than 0.8V. The OPA564-Q1 is enabled at logic levels greater than 2V. In dual-supply operation, the logic pin remains referenced to a logic ground. However, the shutdown pin of the OPA564-Q1 continues to be referenced to V–.

Thus, in a dual-supply system, to shut down the OPA564-Q1 the voltage level of the logic signal must be level-shifted by some means. One way to shift the logic signal voltage level is by using an optocoupler, as Figure 38 shows.



(1) Optional; may be required to limit leakage current of optocoupler at high temperatures.

Figure 38. Shutdown Configuration for Dual Supplies (Using Optocoupler)

To shut down the output, the E/$\overline{S}$ pin is pulled low, no greater than 0.8V above V–. This function can be used to conserve power during idle periods. To return the output to an enabled state, the E/$\overline{S}$ pin should be pulled to at least 2.0V above V–. Figure 27 shows the typical enable and shutdown response times. It should be noted that the E/$\overline{S}$ pin does not affect the internal thermal shutdown.

When the OPA564-Q1 will be used in applications where the device shuts down, special care should be taken with respect to input protection. Consider the following two examples.

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Figure 39 shows the amplifier in a follower configuration. The load is connected midway between the supplies, V+ and V–.

When the device shuts down in this situation, the load pulls V_{OUT} to ground. Little or no current then flows through the input of the OPA564-Q1.

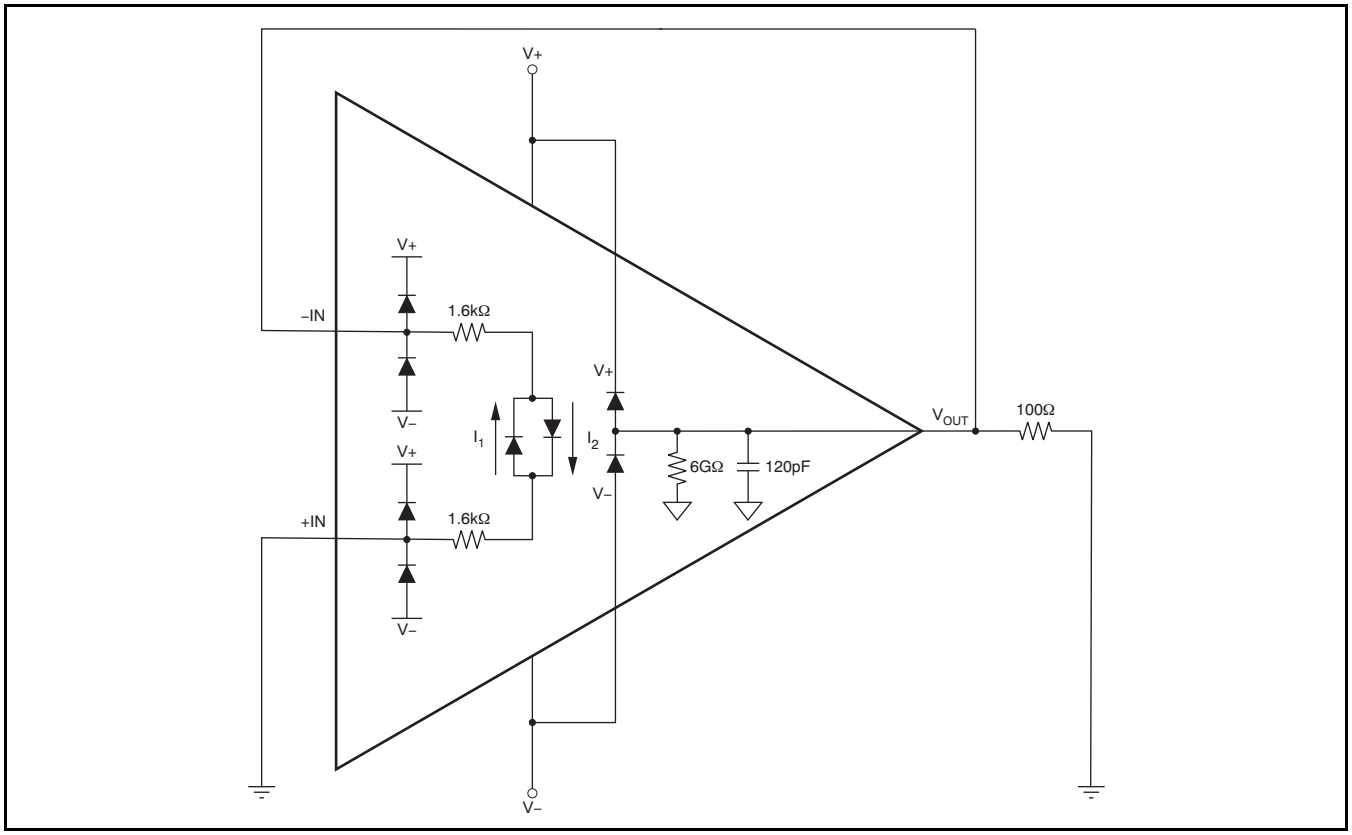


Figure 39. Shutdown Equivalent Circuit with Load Connected Midway Between Supplies

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Now consider Figure 40. Here, the load is connected to V–. When the device shuts down, current flows from the positive input +IN through the first 1.6kΩ resistor through an input protection diode, then through the second 1.6kΩ resistor, and finally through the 100Ω resistor to V–.

This current flow produces a voltage across the inputs which is much greater than 0.5V, which damages the OPA564-Q1. A similar problem would occur if the load is connected to the positive supply.

CAUTION

This configuration damages the device.

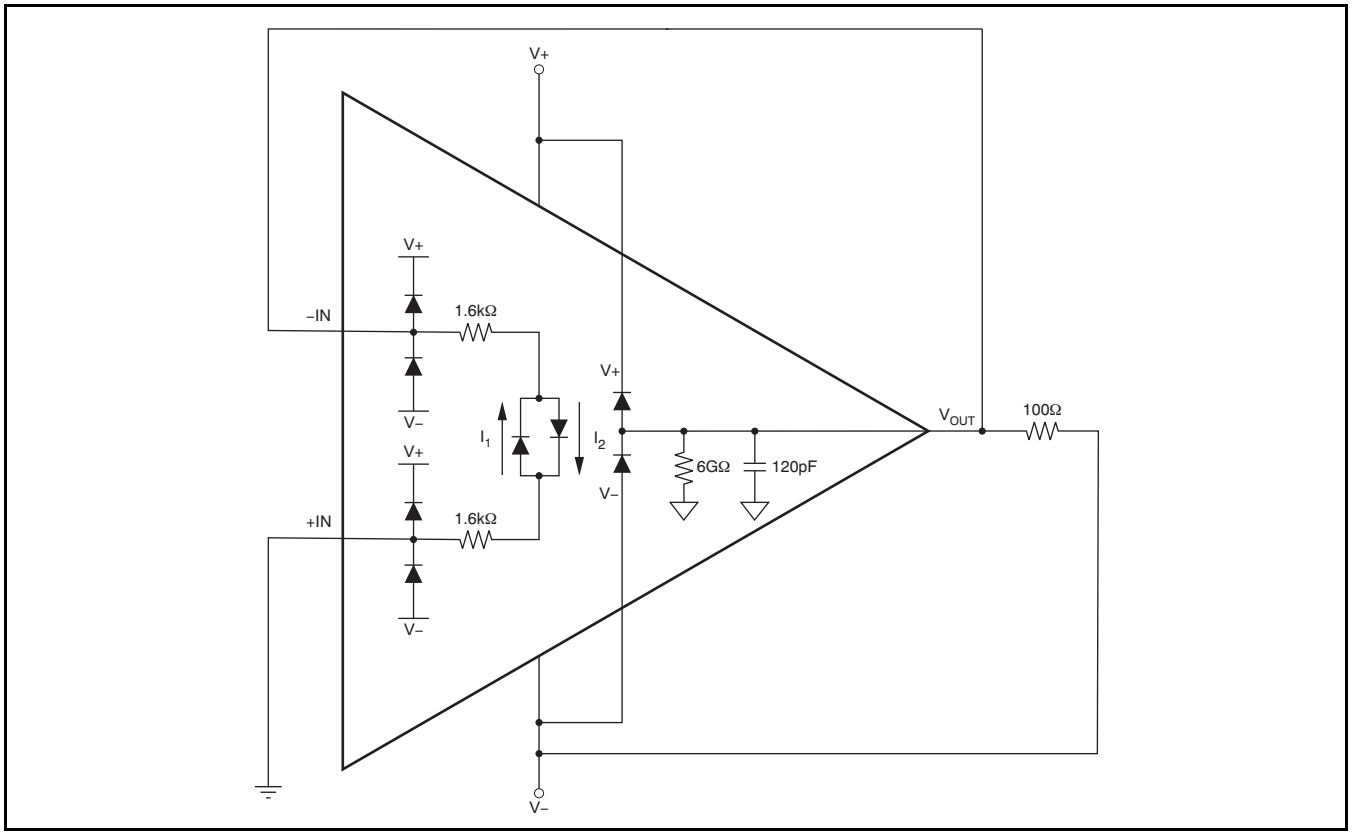


Figure 40. Shutdown Equivalent Circuit with Load Connected to V–: Voltage Across Inputs During DIsable Exceeds Input Requirements

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The solution is to place external protection diodes across the OPA564-Q1 input. Figure 41 illustrates this configuration.

NOTE

This configuration protects the input during shutdown.

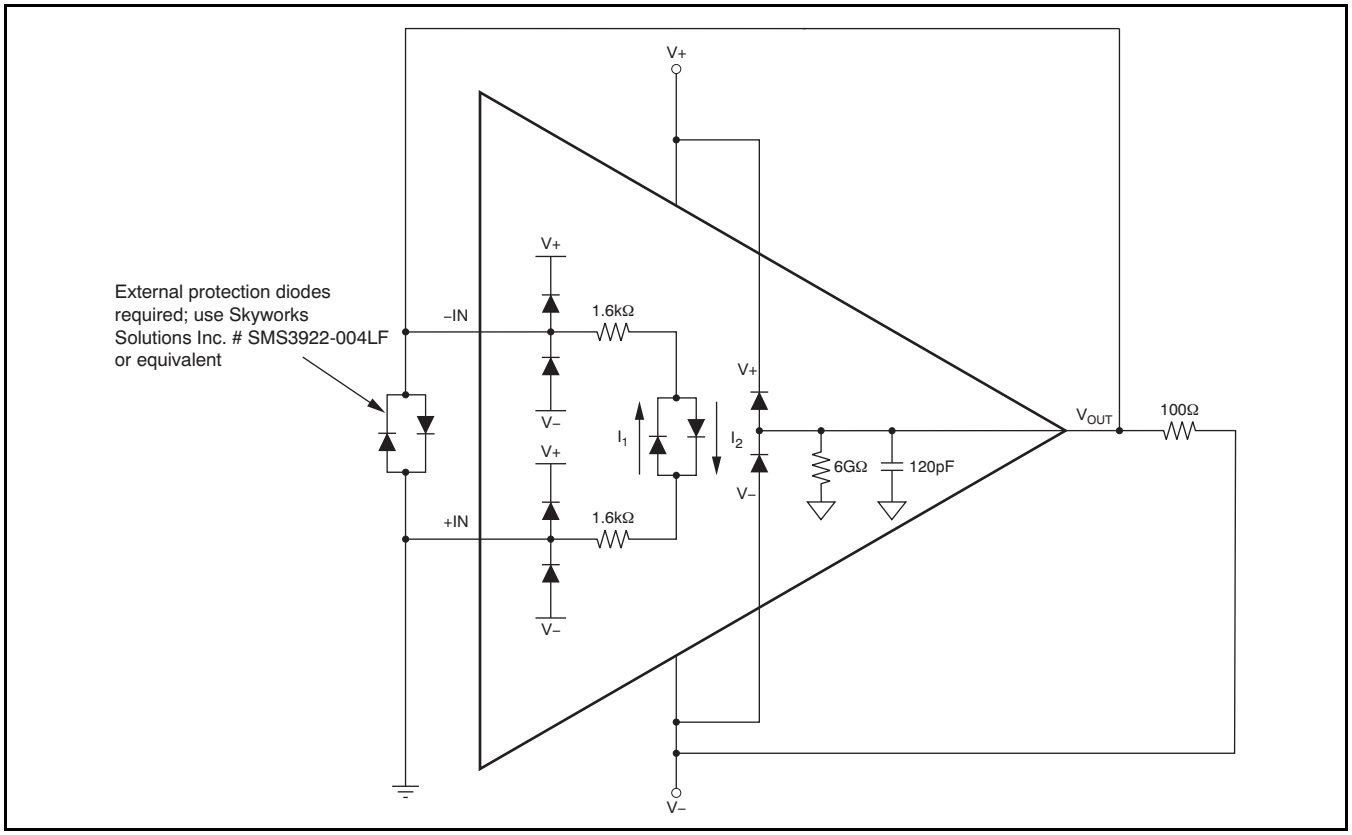


Figure 41. Shutdown Equivalent Circuit with Load Connected to V–: Protected Input Configuration

Ensuring Microcontroller Compatibility

Not all microcontrollers output the same logic state after power-up or reset. 8051-type microcontrollers, for example, output logic high levels while other models power up with logic low levels after reset. In the configuration of Figure 38**(a)**, the shutdown signal is applied on the cathode side of the photodiode within the optocoupler. A high logic level causes the OPA564-Q1 to be enabled, and a low logic level shuts the OPA564-Q1 down. In the configuration of Figure 38**(b)**, with the logic signal applied on the anode side, a high level causes the OPA564-Q1 to shut down, and a low level enables the op amp.

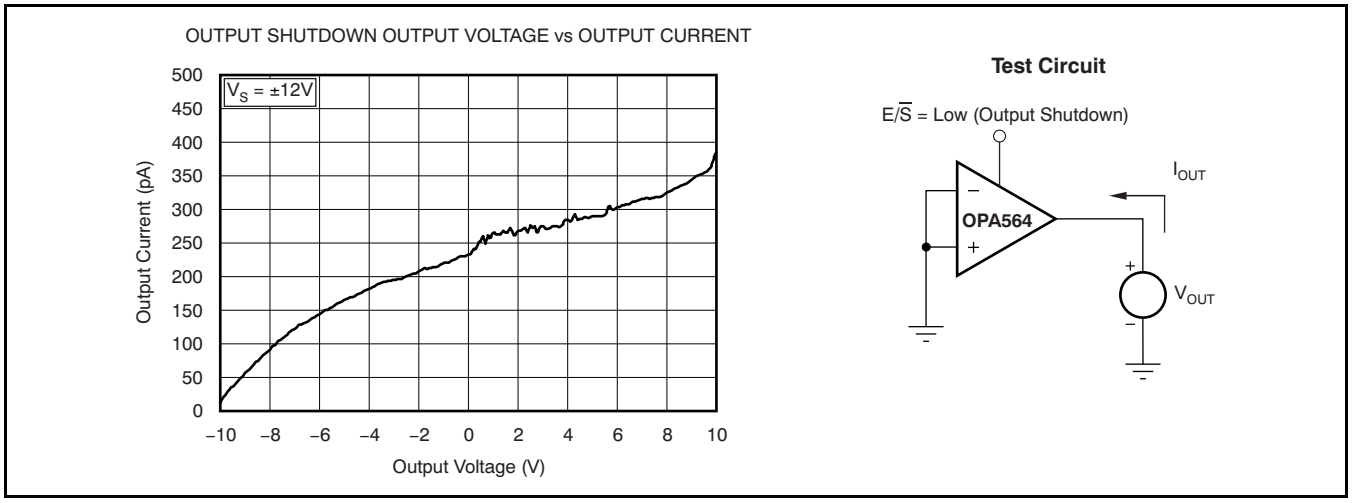


Figure 42. Output Shutdown Output Impedance

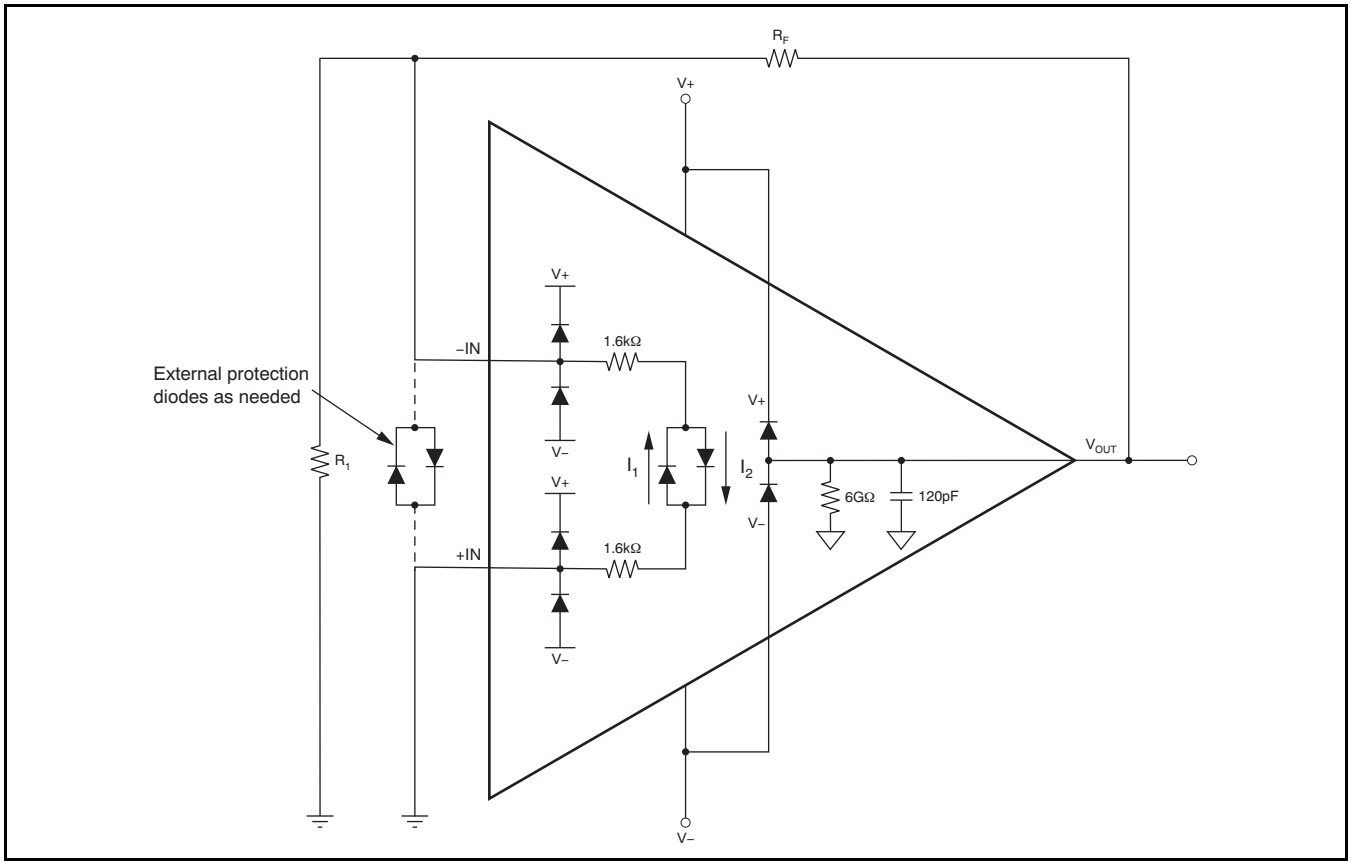


Figure 43. OPA564-Q1: Output Shutdown Equivalent Circuit (with External Feedback)

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CURRENT LIMIT FLAG

The OPA564-Q1 features a current limit flag (I_{FLAG}) that can be monitored to determine if the load current is operating within or exceeding the current limit set by the user. The output signal of I_{FLAG} is compatible with standard CMOS logic and is referenced to the negative supply pin (V–). A voltage level of + 0.8V or less with respect to V– indicates that the amplifier is operating within the limits set by the user. A voltage level of +2.0V or greater with respect to V– indicates that the OPA564-Q1 is operating above (exceeds) the current limit set by the user. See *Setting the Current Limit* for proper current limit operation.

OUTPUT STAGE COMPENSATION

The complex load impedances common in power op amp applications can cause output stage instability. For normal operation, output compensation circuitry is typically not required. However, if the OPA564-Q1 is intended to be driven into current limit, an R/C network (snubber) may be required. A snubber circuit such as the one shown in Figure 54 may also enhance stability when driving large capacitive loads (greater than 1000pF) or inductive loads (for example, motors or loads separated from the amplifier by long cables). Typically, 3Ω to 10Ω in series with 0.01μF to 0.1μF is adequate. Some variations in circuit value may be required with certain loads.

OUTPUT PROTECTION

The output structure of the OPA564-Q1 includes ESD diodes (see Figure 43). Voltage at the OPA564-Q1 output must not be allowed to go more than 0.4V beyond either supply rail to avoid damaging the device. Reactive and electromagnetic field (EMF)-generation loads can return load current to the amplifier, causing the output voltage to exceed the power-supply voltage. This damaging condition can be avoided with clamping diodes from the output terminal to the power supplies, as Figure 54 and Figure 55 illustrate. Schottky rectifier diodes with a 3A or greater continuous rating are recommended.

THERMAL PROTECTION

The OPA564-Q1 has thermal sensing circuitry that helps protect the amplifier from exceeding temperature limits. Power dissipated in the OPA564-Q1 causes the junction temperature to rise. Internal thermal shutdown circuitry disables the output when the die temperature reaches the thermal shutdown temperature limit. The OPA564-Q1 output remains shut down until the die has cooled sufficiently; see the Electrical Characteristics, *Thermal Shutdown* section.

Depending on load and signal conditions, the thermal protection circuit may cycle on and off. This cycling limits the amplifier dissipation, but may have undesirable effects on the load. Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable, long-term, continuous operation, with I_{OUT} at the maximum output of 1.5A, the junction temperature should be limited to +85°C maximum. Figure 44 shows the maximum output current versus junction temperature for dc and RMS signal outputs. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection triggers. Use worst-case loading and signal conditions. For good, long-term reliability, thermal protection should trigger more than 35°C above the maximum expected ambient condition of the application.

The internal protection circuitry of the OPA564-Q1 was designed to protect against overload conditions; it was not intended to replace proper heatsinking. Continuously running the OPA564-Q1 into thermal shutdown degrades reliability.

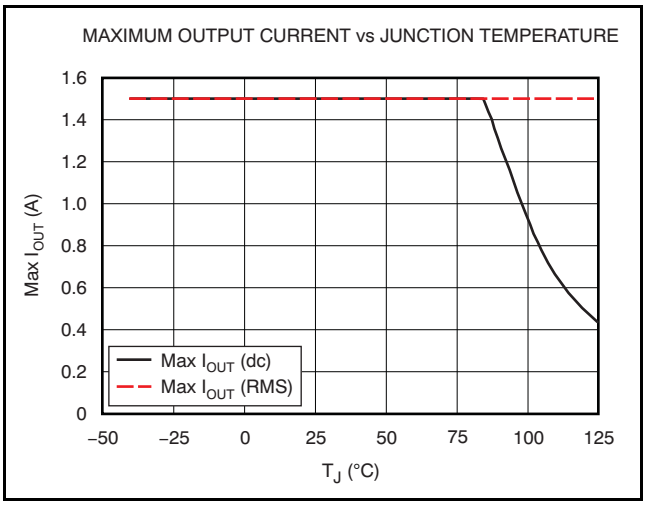


Figure 44. Maximum Output Current vs Junction Temperature

USING T_{SENSE} FOR MEASURING JUNCTION TEMPERATURE

The OPA564-Q1 includes an internal diode for junction temperature monitoring. The η-factor of this diode is 1.033. Measuring the OPA564-Q1 junction temperature can be accomplished by connecting the T_{SENSE} pin to a remote-junction temperature sensor, such as the TMP411 (see Figure 57).

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POWER DISSIPATION AND SAFE OPERATING AREA

Power dissipation depends on power supply, signal, and load conditions. For dc signals, power dissipation is equal to the product of output current (I_{OUT}) and the voltage across the conducting output transistor [(V+) – V_{OUT} when sourcing; V_{OUT} – (V–) when sinking]. Dissipation with ac signals is lower. Application Bulletin AB-039, *Power Amplifier Stress and Power Handling Limitations* (SBOA022, available for download from www.ti.com) explains how to calculate or measure power dissipation with unusual signals and loads.

Figure 45 shows the safe operating area at room temperature with various heatsinking efforts. Note that the safe output current decreases as (V+) – V_{OUT} or V_{OUT} – (V–) increases. Figure 46 shows the safe operating area at various temperatures with the PowerPAD being soldered to a 2oz copper pad.

The power that can be safely dissipated in the package is related to the ambient temperature and the heatsink design. The PowerPAD package was specifically designed to provide excellent power dissipation, but board layout greatly influences the heat dissipation of the package. Refer to the *Thermally-Enhanced PowerPAD Package* section for further details.

The relationship between thermal resistance and power dissipation can be expressed as:

$T_J = T_A + T_{JA}$

$T_{JA} = P_D \times \theta_{JA}$

Combining these equations produces:

$T_J = T_A + P_D \times \theta_{JA}$

where:

T_J = Junction temperature (°C)

T_A = Ambient temperature (°C)

θ_{JA} = Junction-to-ambient thermal resistance (°C/W)

P_D = Power dissipation (W)

To determine the required heatsink area, required power dissipation should be calculated and the relationship between power dissipation and thermal resistance should be considered to minimize shutdown conditions and allow for proper long-term operation (junction temperature of +85°C or less).

Once the heatsink area has been selected, worst-case load conditions should be tested to ensure proper thermal protection.

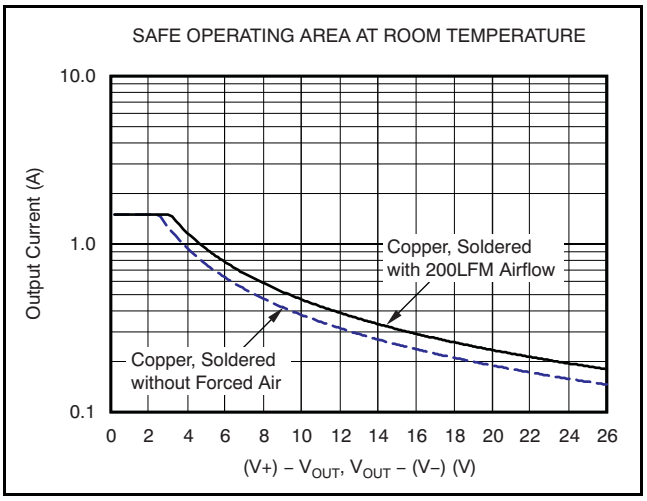
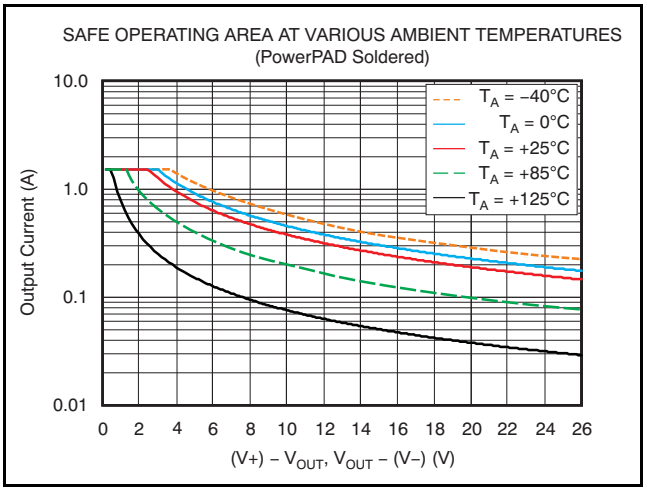


Figure 45. Safe Operating Area at Room Temperature



PowerPAD soldered to a 2oz copper pad.

Figure 46. Safe Operating Area at Various Ambient Temperatures

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For applications with limited board size, refer to Figure 47 for the approximate thermal resistance relative to heatsink area. Increasing heatsink area beyond $2in^2$ provides little improvement in thermal resistance. To achieve the 33°C/W shown in the Electrical Characteristics, a 2oz copper plane size of $9in^2$ was used. The PowerPAD package is well-suited for continuous power levels from 2W to 4W, depending on ambient temperature and heatsink area. The addition of airflow also influences maximum power dissipation, as Figure 48 illustrates. Higher power levels may be achieved in applications with a low on/off duty cycle, such as remote meter reading.

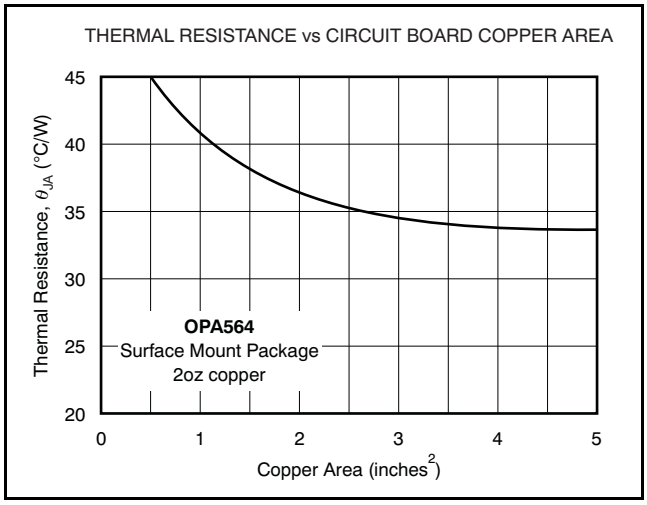


Figure 47. Thermal Resistance vs Circuit Board Copper Area

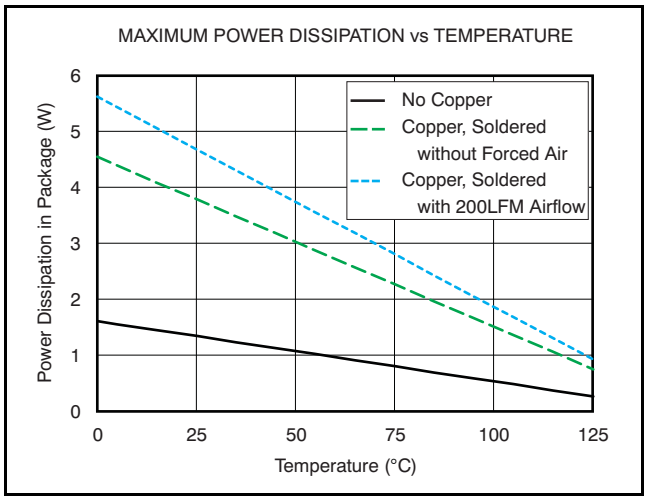


Figure 48. Maximum Power Dissipation vs Temperature

THERMALLY-ENHANCED PowerPAD PACKAGE

The OPA564-Q1 uses the HSOP-20 PowerPAD DWP and DWD packages, which are thermally-enhanced, standard size IC packages. These packages enhance power dissipation capability significantly and can be easily mounted using standard printed circuit board (PCB) assembly techniques, and can be removed and replaced using standard repair procedures.

The DWP PowerPAD package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the IC, as shown in Figure 49**a**; the DWD PowerPAD package has the exposed pad on the top side of the package, as shown in Figure 49**b**. The thermal pad provides an extremely low thermal resistance (θ_{JC}) path between the die and the exterior of the package.

PowerPAD packages with exposed pad down are designed to be soldered directly to the PCB, using the PCB as a heatsink. Texas Instruments does not recommend the use of the of a PowerPAD package without soldering it to the PCB because of the risk of lower thermal performance and mechanical integrity. In addition, through the use of thermal vias, the bottom-side thermal pad can be directly connected to a power plane or special heatsink structure designed into the PCB. The PowerPAD should be at the same voltage potential as V–. Soldering the bottom-side PowerPAD to the PCB is always required, even with applications that have low power dissipation. It provides the necessary thermal and mechanical connection between the leadframe die and the PCB.

Pad-up PowerPAD packages should have appropriately designed heatsinks attached. Because of the variation and flexible nature of this type of heat sink, additional details should come from the specific manufacturer of the heatsink.

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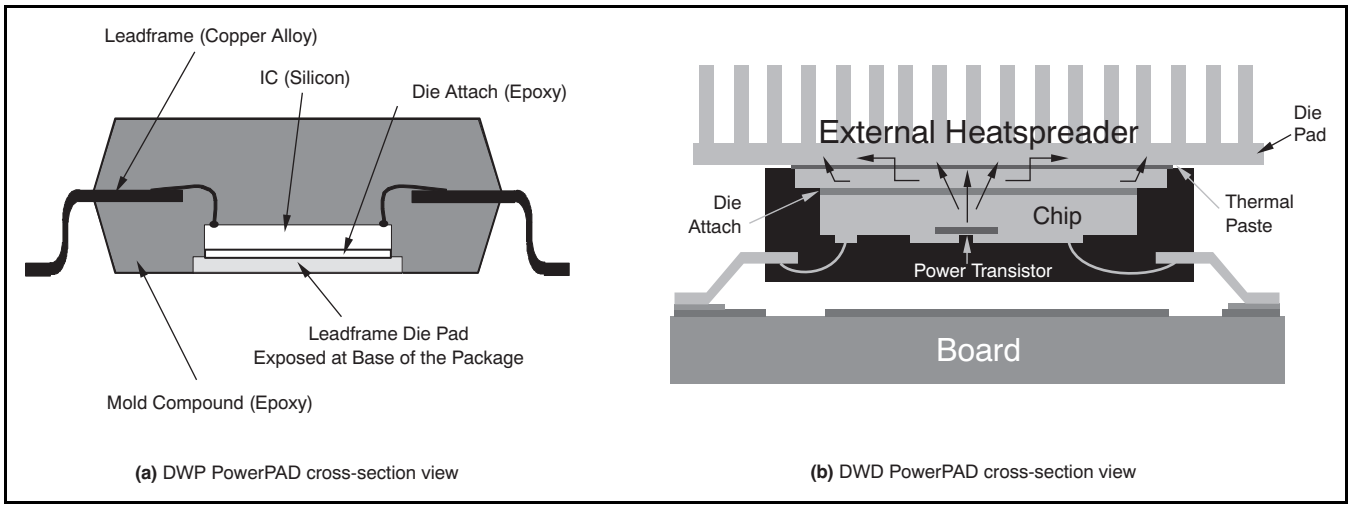


Figure 49. Cross-Section Views

Bottom-Side PowerPAD Assembly Process

1. The PowerPAD must be connected to the most negative supply of the device, V–.
2. Prepare the PCB with a top side etch pattern, as shown in the attached thermal land pattern mechanical drawing. There should be etch for the leads as well as etch for the thermal land.
3. Place the recommended number of holes (or thermal vias) in the area of the thermal pad, as seen in the attached thermal land pattern mechanical drawing. These holes should be 13mils (.013in, or 330.2µm) in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow.
4. It is recommended, but not required, to place a small number of the holes under the package and outside the thermal pad area. These holes provide an additional heat path between the copper land and ground plane and are 25mils (.025in, or 635µm) in diameter. They may be larger because they are not in the area to be soldered, so wicking is not a problem. This configuration is illustrated in the attached thermal land pattern mechanical drawing.
5. Connect all holes, including those within the thermal pad area and outside the pad area, to the internal plane that is at the same voltage potential as V–.
6. When connecting these holes to the internal plane, do not use the typical web or spoke via connection methodology (as Figure 50 shows). Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This configuration makes the soldering of vias that have plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the PowerPAD package should be connected to the internal plane with a complete connection around the entire circumference of the plated through-hole.
7. The top-side solder mask should leave exposed the terminals of the package and the thermal pad area. The thermal pad area should leave the 13mil holes exposed. The larger 25mil holes outside the thermal pad area should be covered with solder mask.
8. Apply solder paste to the exposed thermal pad area and all of the package terminals.
9. With these preparatory steps completed, the PowerPAD IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This processing results in a part that is properly installed.

For detailed information on the PowerPAD package including thermal modeling considerations and repair procedures, see Technical Brief SLMA002, *PowerPAD Thermally Enhanced Package*, available at www.ti.com.

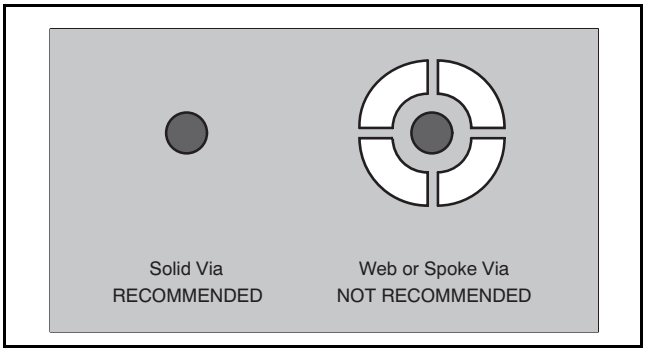
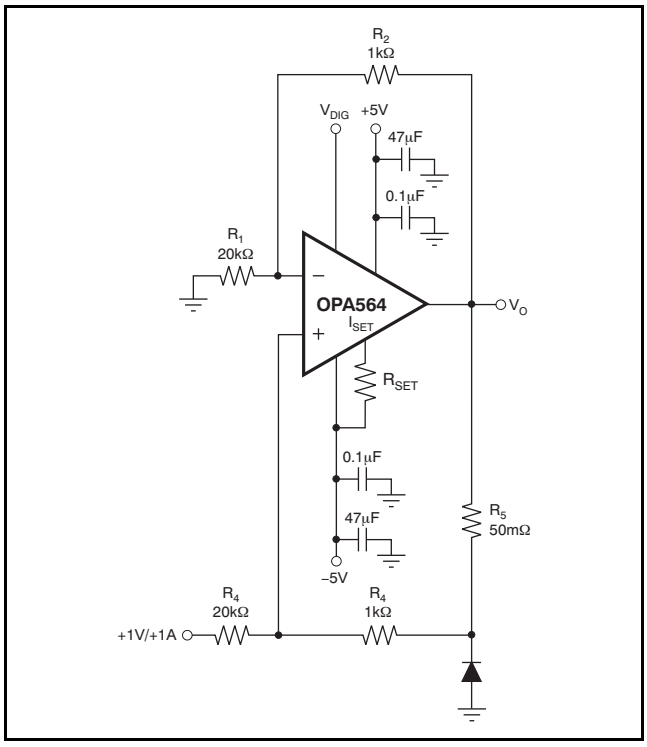


Figure 50. Via Connection Methods

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(1) See Figure 35 for an example of a basic noninverting amplifier with V_{DIG} not exceeding 5.5V.

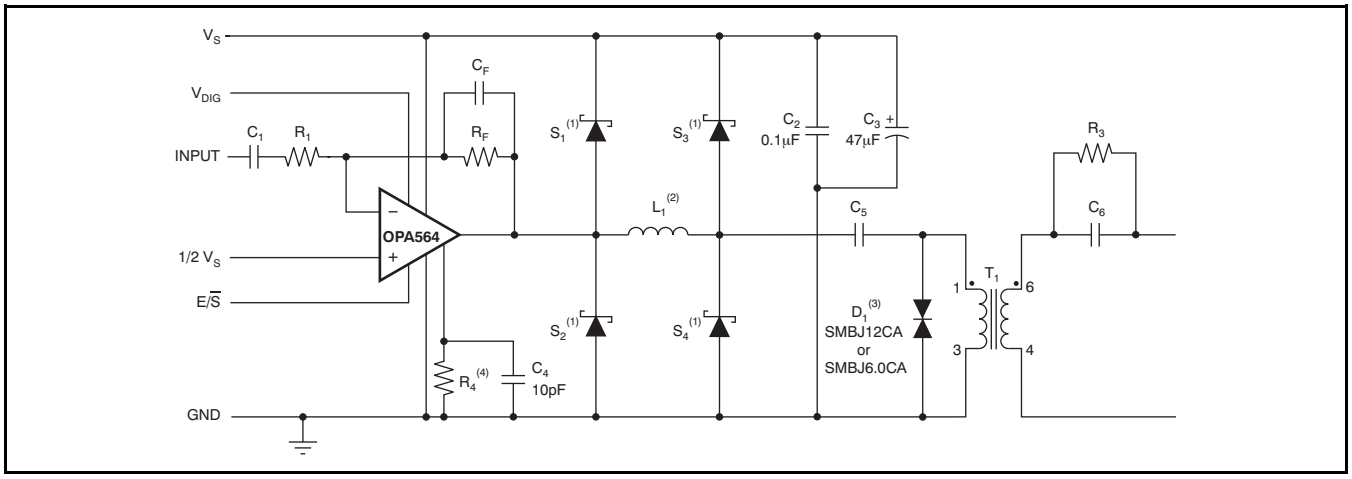
Figure 51. Improved Howland Current Pump

APPLICATIONS CIRCUITS

The high output current and low supply of the OPA564-Q1 make it a good candidate for driving laser diodes and thermoelectric coolers. Figure 51 shows an improved Howland current pump circuit.

POWERLINE COMMUNICATION

Powerline communication (PLC) applications require some form of signal transmission over an existing ac power line. A common technique used to couple these modulated signals to the line is through a signal transformer. A power amplifier is often needed to provide adequate levels of current and voltage to drive the varying loads that exist on today's powerlines. One such application is shown in Figure 52. The OPA564-Q1 is used to drive signals used in frequency modulation schemes such as FSK (Frequency-Shift Keying) or OFDM (Orthogonal Frequency-Division Multiplexing) to transmit digital information over the powerline. The power output capabilities of the OPA564-Q1 are needed to drive the current requirements of the transformer that is shown in the figure, coupled to the ac power line via a coupling capacitor. Circuit protection is often needed or required to prevent excessive line voltages or current surges from damaging the active circuitry in the power amplifier and application circuitry.



(1) S_1, S_2, S_3, and S_4 are Schottky diodes. S_1 and S_2 are B350 or equivalent. S_3 and S_4 are BAV99T or equivalent.

(2) L_1 should be small enough so that it does not interfere with the bandwidth of interest but large enough to suppress transients that could damage the OPA564-Q1.

(3) D_1 is a transient suppression diode. For 24V supplies, use SMBJ12CA. For 12V supplies, use SMBJ6.0CA. Voltage rating of transient voltage suppressor should be half the supply rating or less.

(4) The minimum recommended value for R_4 is 7.5kΩ.

Figure 52. Powerline Communication Line Coupling

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PROGRAMMABLE POWER SUPPLY

Figure 53 shows the OPA333 used to control I_{SET} in order to adjust the current limit of the OPA564-Q1.

Figure 54 shows a basic motor speed driver but does not include any control over the motor speed. For applications where good control of the speed of the motor is desired, but the precision of a tachometer control is not required, the circuit in Figure 55 provides control by using feedback of the current consumption to adjust the motor drive.

For more information on this circuit, see the Application Bulletin *DC Motor Speed Controller: Control a DC Motor without Tachometer Feedback* (SBOA043), available for download at the TI web site.

Figure 56 shows two examples of generating the signal for V_{DIG}. Figure 56**a** uses an 1N4732A zener to bias the V_{DIG} to precisely 4.7V above V–. Figure 56**b** uses a high-voltage subregulator to derive the V_{DIG} voltage. Figure 58 illustrates a detailed powerline communication circuit.

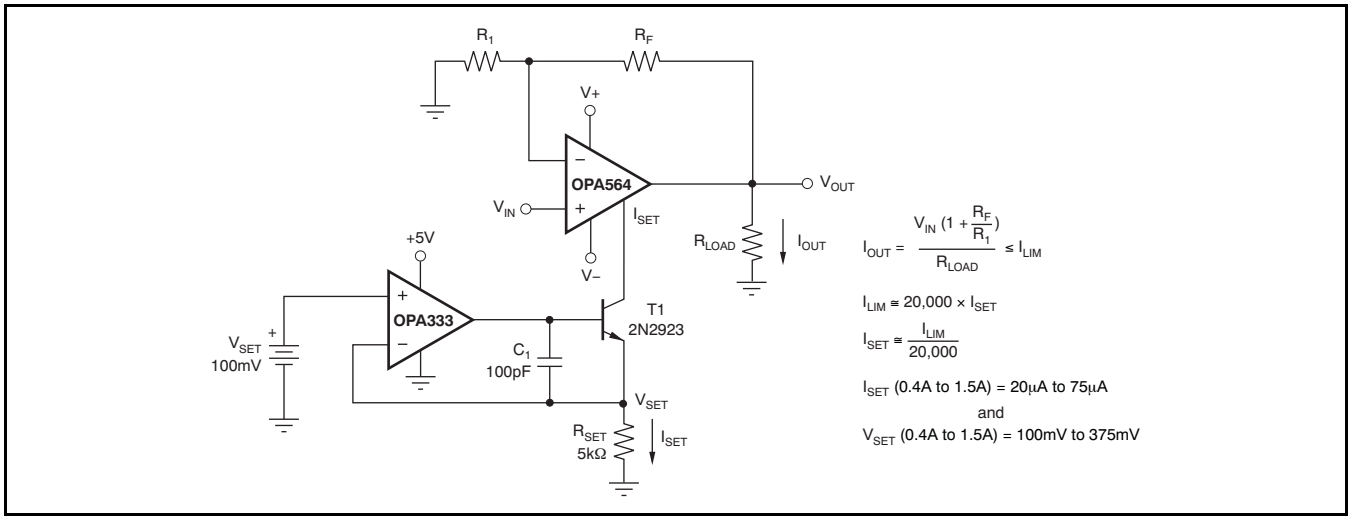
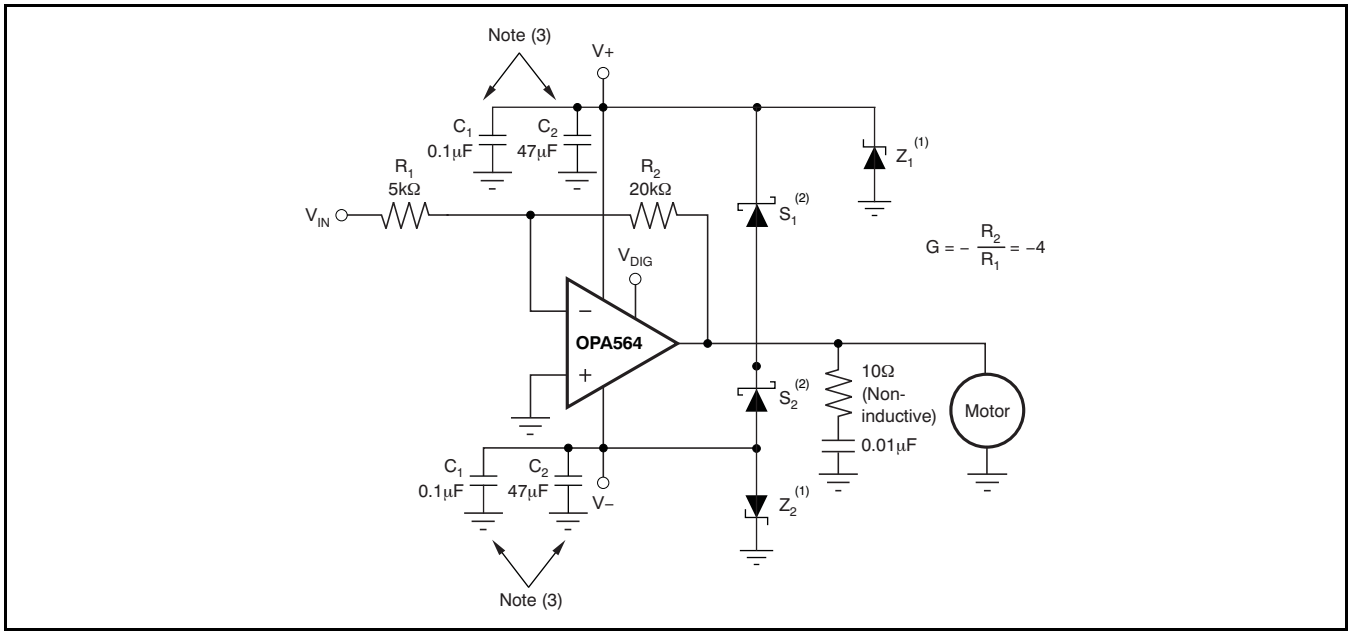


Figure 53. Programmable Current Limit Option



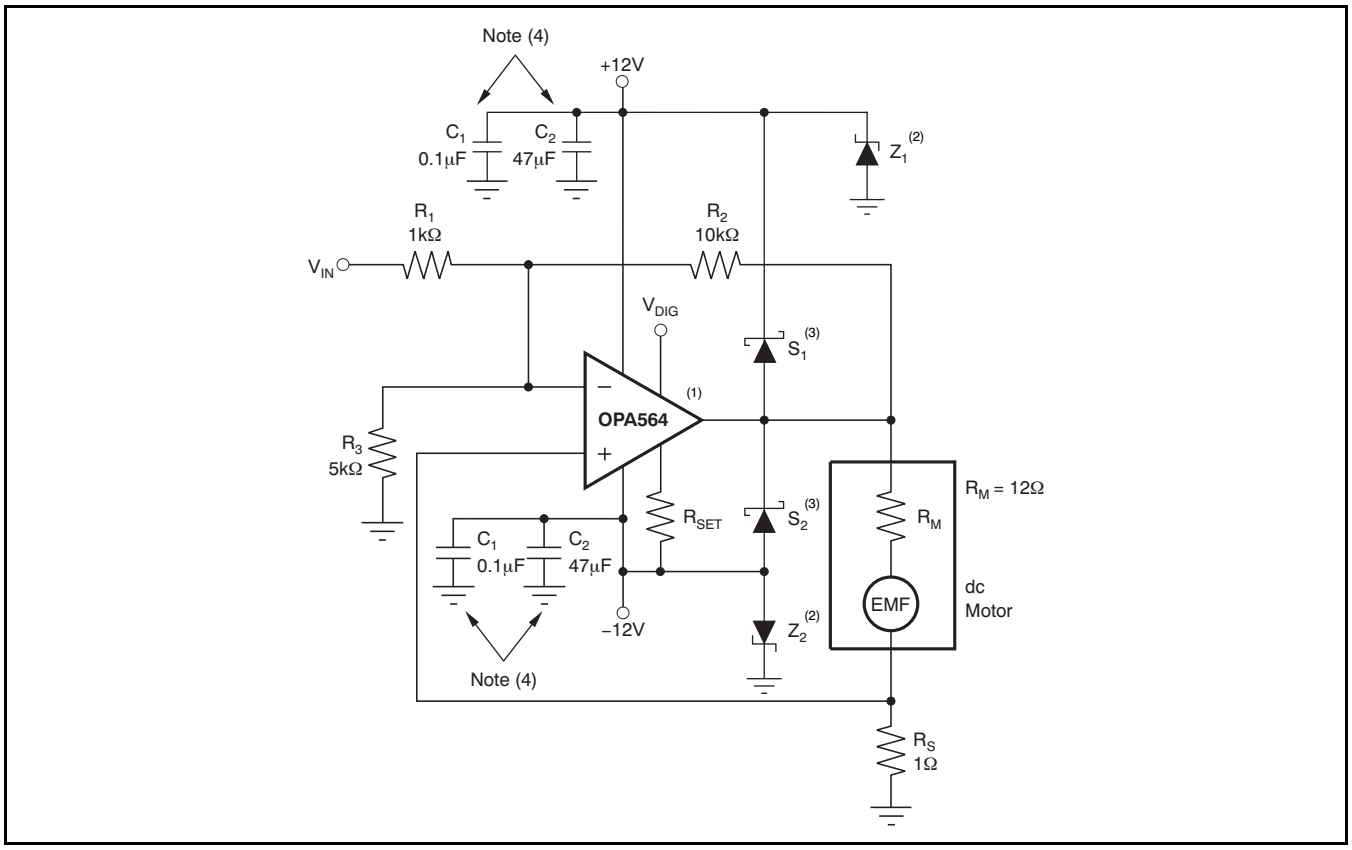
(1) Z_1, Z_2 = zener diodes (IN5246 or equivalent). Select Z_1 and Z_2 diodes that are capable of the maximum anticipated surge current.

(2) S_1, S_2 = Schottky diodes (STPS1L40 or equivalent).

(3) C_1 = high-frequency bypass capacitors; C_2 = low-frequency bypass capacitors (minimum of 10µF for every 1A peak current)

Figure 54. Motor Drive Circuit

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(1) I_{FLAG} and T_{FLAG} connections are not shown.

(2) Z_1, Z_2 = zener diodes (IN5246 or equivalent). Select Z_1 and Z_2 diodes that are capable of the maximum anticipated surge current.

(3) S_1, S_2 = Schottky diodes (STPS1L40 or equivalent).

(4) C_1 = high-frequency bypass capacitors; C_2 = low-frequency bypass capacitors (minimum of 10µF for every 1A peak current).

Figure 55. DC Motor Speed Controller (without Tachometer)

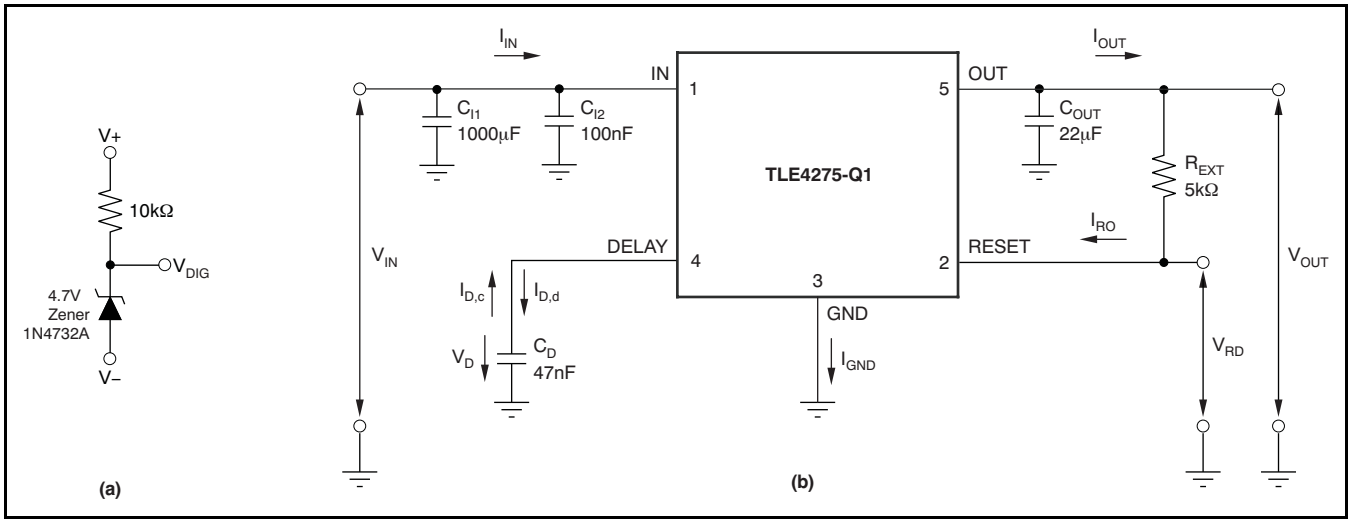


Figure 56. Circuits for Generating V_{DIG}

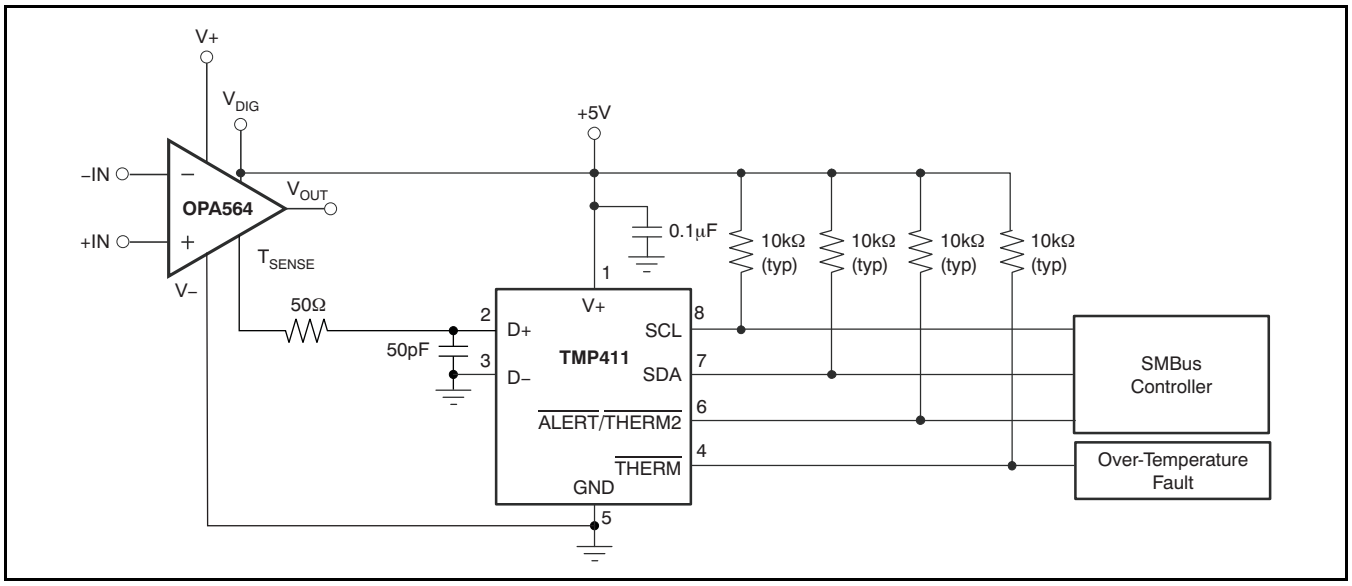


Figure 57. Temperature Measurement Using T_{SENSE} and TMP411

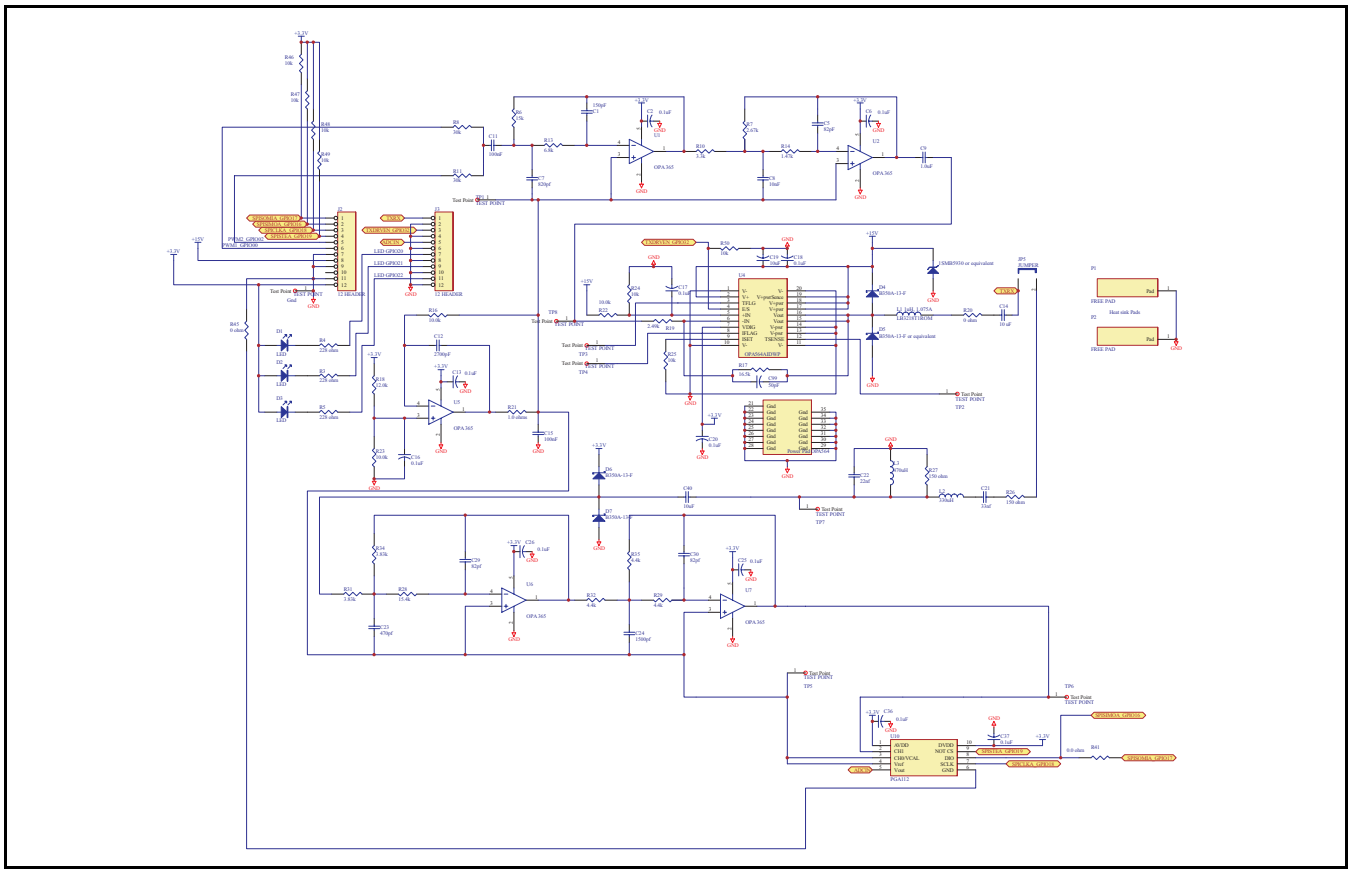


Figure 58. Detailed Powerline Communication Circuit

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数据转换器	http://www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
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时钟和计时器	http://www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	http://www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	http://www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	http:///www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA564AQDWPRQ1	ACTIVE	SO PowerPAD	DWP	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA564AQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

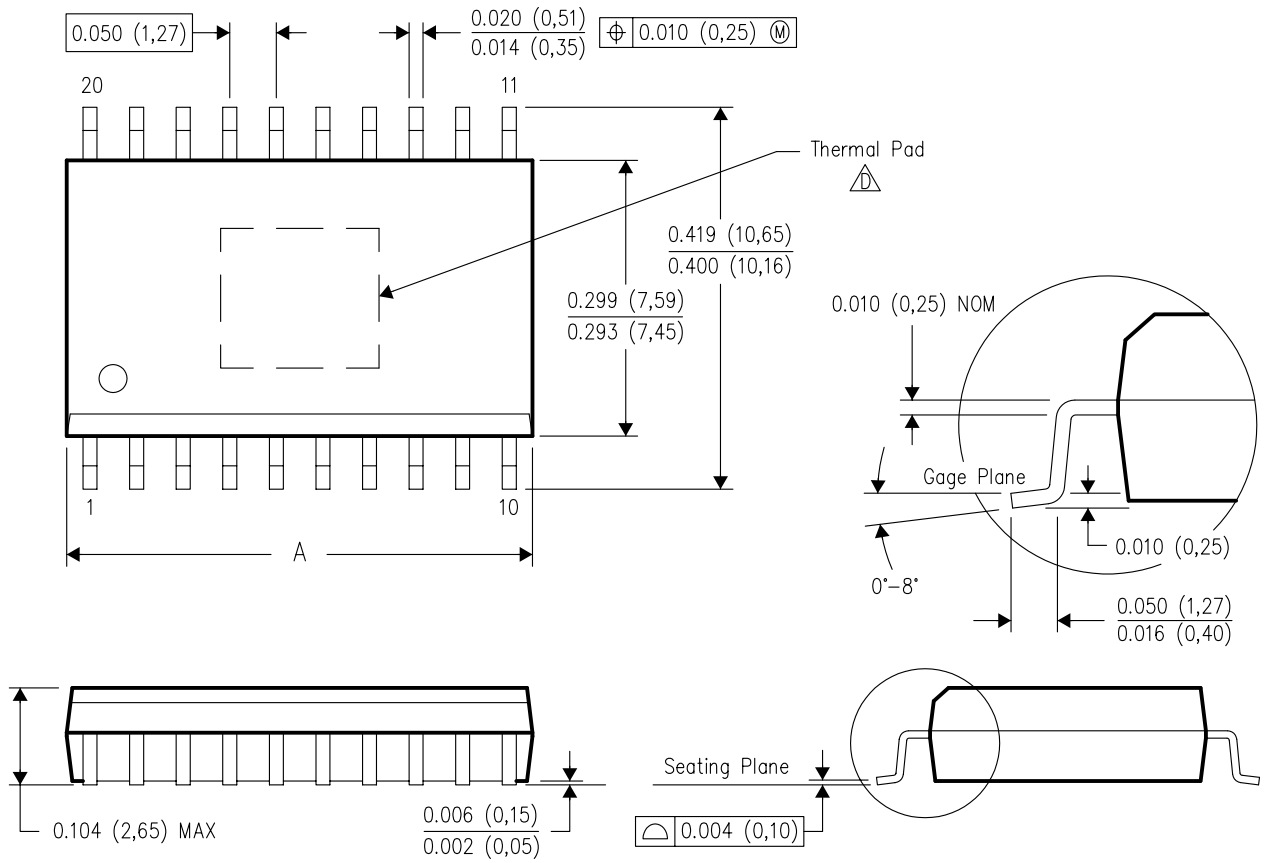
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DWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PINS SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4147575/C 02/05

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.

PowerPAD is a trademark of Texas Instruments.

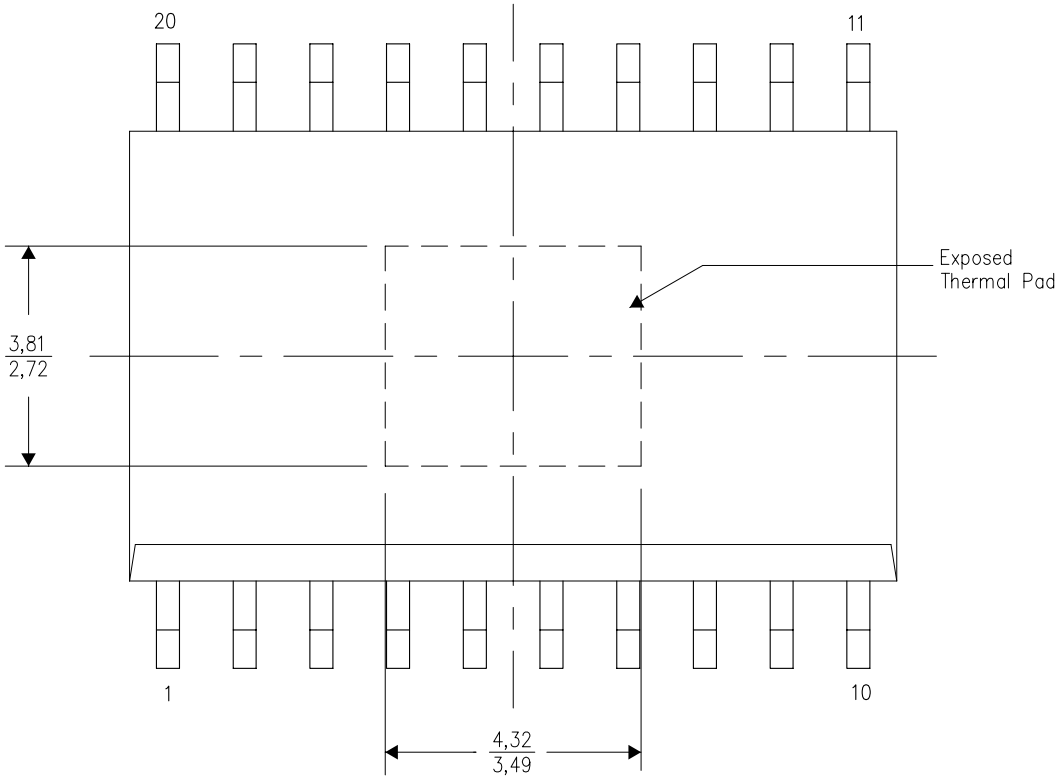
DWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206325–2/E 12/10

NOTE: A. All linear dimensions are in millimeters

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