

# 具有超低 $I_Q$ 的 TPS7A63-Q1、TPS7A6401-Q1 300mA、40V 低压降稳压器

## 1 特性

- 符合面向汽车应用的 AEC-Q100 标准:
  - 温度等级 1:  $-40^\circ\text{C}$  至  $125^\circ\text{C}$ ,  $T_A$
  - 结温范围:  $-40^\circ\text{C}$  至  $150^\circ\text{C}$ ,  $T_J$
- 低压降:
  - 在  $I_{\text{OUT}} = 150\text{mA}$  时为 300mV
- 7V 至 40V 的宽输入电压范围, 瞬态电压高达 45V
- 最大输出电流为 300mA
- 超低静态电流:
  - 轻负载时  $I_{\text{QUIESCENT}} = 35\mu\text{A}$  (典型值)
  - $\text{EN} = \text{低电平时 } I_{\text{SLEEP}} < 2\mu\text{A}$
- 3.3V 和 5V 固定电压, 可调节电压范围为 2.5V 至 7V
- 具有故障/标志的集成看门狗
- 与低 ESR 陶瓷输出电容器搭配使用时可保持稳定
- 集成上电复位:
  - 可编程延迟
  - 开漏复位输出
- 集成故障保护:
  - 短路和过流保护
  - 热关断
- 低输入电压跟踪
- 耐热增强型 14 引脚 HTSSOP-PWP 封装和 10 引脚 VSON-DRK 封装

## 2 应用

- 汽车音响主机
- 前照灯
- 直流/直流转换器
- 汽车中心信息显示屏

## 3 说明

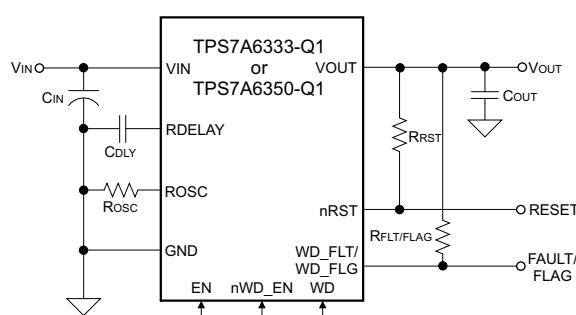
TPS7A63-Q1 和 TPS7A6401-Q1 是低压降线性稳压器系列产品, 专为在轻负载应用中实现低功耗和小于 35 $\mu\text{A}$  的静态电流而设计。这类器件具有集成的可编程窗口看门狗和过流保护功能, 即使与低 ESR 陶瓷输出电容器搭配使用, 也能实现稳定运行。设计人员可使用外部电阻器来设定输出电压。低压跟踪特性允许使用更小的输入电容器并且有可能在冷启动期间无需使用升压转换器。加电复位延迟固定 (典型值 250 $\mu\text{s}$ ), 或者使用一个外部电容器可设定延迟。凭借这些特性, 这些器件非常适合用于各种汽车应用的电源。

### 器件信息<sup>(1)</sup>

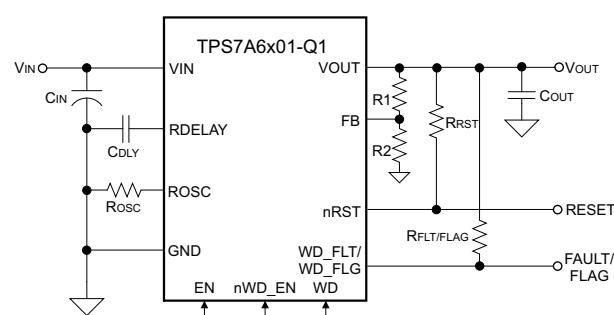
器件型号	封装	封装尺寸 (标称值)
TPS7A63-Q1、 TPS7A6401-Q1	HTSSOP (14)	5.00mm × 4.40mm
TPS7A63-Q1	VSON (10)	4.00mm × 3.00mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品目录。

### 固定输出电压选项



### 可调输出电压选项



## 目录

1	特性 .....	1	7.4	Device Functional Modes.....	20
2	应用 .....	1	8	<b>Application and Implementation .....</b>	21
3	说明 .....	1	8.1	Application Information.....	21
4	修订历史记录 .....	2	8.2	Typical Applications .....	21
5	<b>Pin Configuration and Functions .....</b>	4	9	<b>Power Supply Recommendations .....</b>	24
6	<b>Specifications.....</b>	5	10	<b>Layout.....</b>	24
6.1	Absolute Maximum Ratings .....	5	10.1	Layout Guidelines .....	24
6.2	ESD Ratings.....	5	10.2	Layout Example .....	27
6.3	Recommended Operating Conditions .....	5	11	器件和文档支持 .....	28
6.4	Thermal Information .....	6	11.1	相关链接.....	28
6.5	Electrical Characteristics.....	6	11.2	接收文档更新通知 .....	28
6.6	Typical Characteristics .....	8	11.3	社区资源.....	28
7	<b>Detailed Description .....</b>	10	11.4	商标 .....	28
7.1	Overview .....	10	11.5	静电放电警告 .....	28
7.2	Functional Block Diagrams .....	10	11.6	Glossary .....	28
7.3	Feature Description.....	12	12	机械、封装和可订购信息 .....	28

## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

### Changes from Revision F (June 2018) to Revision G

	Page
• 已更改 将 AEC-Q100 特性项目符号更改为符合新标准 .....	1
• 已更改 将整个文档中的输入电压范围从 11V 更改为 7V.....	1
• 已更改 更改了应用部分 .....	1
• Added footnote to $V_{IN}$ row in <i>Recommended Operating Conditions</i> table .....	5
• Added footnote to $V_{IN}$ row in <i>Electrical Characteristics</i> table .....	6

### Changes from Revision E (September 2015) to Revision F

	Page
• 已更改 将器件名称更改为 TPS7A63-Q1、TPS7A6401-Q1 .....	1
• 已更改 将 4V 更改为 11V（位于第四个特性项目符号） .....	1
• Changed $V_{IN}$ , $V_{EN}$ parameter row in <i>Recommended Operating Conditions</i> table: separated $V_{IN}$ and $V_{EN}$ into different rows, changed $V_{IN}$ minimum specification from 4 V to 11 V .....	5
• Changed $V_{IN}$ minimum specification from $V_{OUT} + 0.3$ V to 11 V in <i>Electrical Characteristics</i> table .....	6
• Changed 4 V to 11 V in <i>Example values</i> column of <i>Input voltage range</i> row of <i>Design Parameters</i> table .....	22
• Changed 4 V to 11 V in <i>Example values</i> column of <i>Input voltage range</i> row of <i>Design Parameters</i> table .....	23
• Changed 4 V to 11 V in first sentence of <i>Power Supply Recommendations</i> section .....	24

### Changes from Revision D (July 2012) to Revision E

	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	5

### Changes from Revision C (April 2012) to Revision D

	Page
• 更正了整个数据表多处位置的器件型号 .....	1
• 向“特性”列表顶部添加了新的项目符号 .....	1
• Deleted the NO. column from the electrical tables .....	5

---

- Deleted two Typical Characteristics graphs ..... 8

---

**Changes from Revision B (December 2011) to Revision C** Page

---

- Changed regulated output voltage (6.1), added text to the test conditions (10mA to 200mA,  $V_{IN} = V_{OUT} + 1V$  to 16V) ..... 6

---

**Changes from Revision A (August 2011) to Revision B** Page

---

- 删除了器件 TPS7A64333-Q1 和 TPSA6450-Q1 ..... 1

---

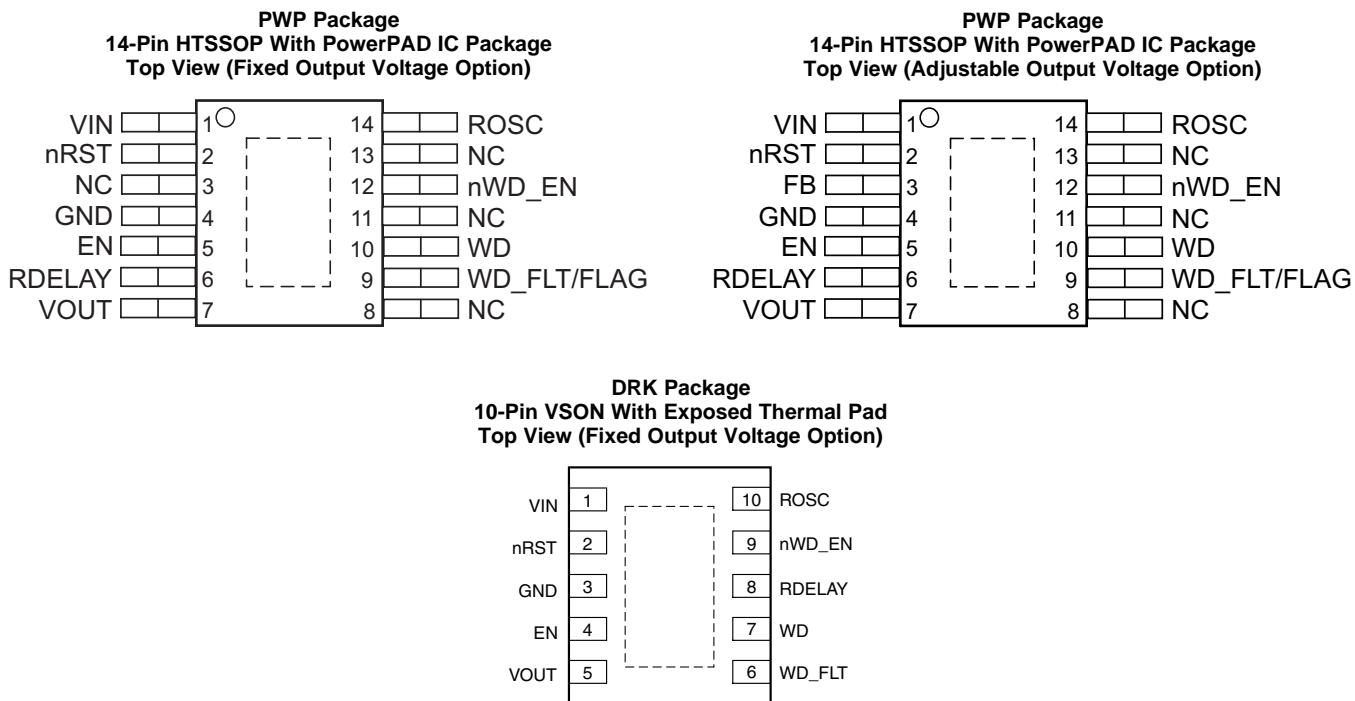
**Changes from Original (June 2011) to Revision A** Page

---

- Deleted the Ordering Information Table ..... 4
- Changed values for  $V_{IL}$  and  $V_{IH}$  in the Watchdog Enable Input (nWD\_EN pin) section ..... 7
- Changed values for  $V_{IL}$  and  $V_{IH}$  in the Watchdog Input Pulse (WD pin) section ..... 7

---

## 5 Pin Configuration and Functions



### Pin Functions

PIN			I/O	DESCRIPTION
NAME	PWP	DRK		
EN	5	4	I	Chip enable pin: This is a high-voltage-tolerant input pin with an internal pulldown. A high input to this pin activates the device and turns the regulator ON. Connect this input to the VIN terminal for self-bias applications. If this pin remains unconnected, the device stays disabled.
FB	3	—	I	Feedback pin (only applicable for TPS7A6x01-Q1): Sense voltage for error amplifier
GND	4	3	I/O	Ground pin: This is signal ground pin of the device.
NC	3	—	—	Not connected (only applicable for TPS7A6333-Q1 and TPS7A6350-Q1)
NC	8	—	—	Not connected
NC	11	—	—	Not connected
NC	13	—	—	Not connected
nRST	2	2	O	Reset pin: This is an open-drain reset output pin with an external pullup resistor connected to the VOUT pin.
nWD_EN	12	9	I	Watchdog enable pin: A high input to this pin disables the watchdog, and vice versa. This is an active-low input pin with an internal pulldown. Leaving this pin unconnected and floating keeps the watchdog enabled. An external microcontroller can pull this pin high momentarily to disable and reinitialize the watchdog.
RDELAY	6	8	O	Reset delay timer pin: This pin programs the reset delay timer using an external capacitor ( $C_{DLY}$ ) to ground.
ROSC	14	10	O	ROscillator pin: This pin programs the internal oscillator frequency (and hence the duration of the watchdog window) by connecting an external resistor to ground.
WD	10	7	I	Watchdog service pin: This is an input pin to provide a service signal to the watchdog.
WD_FLAG	9	6	O	Watchdog flag pin (for TPS7A6401-Q1 only): This is an active-high latched fault (that is, flag) output pin with an external pullup resistor connected to VOUT pin.
WD_FLT	9	6	O	Watchdog fault pin (for TPS7A63-Q1 only): This is an active-low fault output pin with an external pullup resistor connected to the VOUT pin.
VIN	1	1	I	Input voltage pin: The unregulated input voltage is supplied to this pin. A bypass capacitor connected between the VIN pin and GND pin dampens line transients on the input.
VOUT	7	5	O	Regulated output voltage pin: This is a regulated voltage output ( $V_{OUT} = 3.3$ V or 5 V or a programmed value) pin with a limitation on maximum output current. For devices with adjustable output voltage (TPS7A6x01-Q1), connecting an external resistor network programs the output voltage. In order to achieve stable operation and prevent oscillation, connect an external output capacitor ( $C_{OUT}$ ) with low ESR between this pin and GND pin.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

DESCRIPTION		MIN	MAX	UNIT
$V_{IN}$ , $V_{EN}$	Unregulated inputs <sup>(2)(3)</sup>		45	V
$V_{OUT}$	Regulated output		7	V
FB	Sense voltage for error amplifier <sup>(2)</sup>		7	V
ROSC	Constant-voltage reference <sup>(2)</sup>		7	V
nWD_EN, WD, WD_FLAG, WD_FLT	Watchdog inputs and outputs <sup>(2)</sup>		7	V
nRST	Open-drain reset output <sup>(2)</sup>		7	V
RDELAY	Reset delay timer output <sup>(2)</sup>		7	V
$T_A$	Operating ambient temperature		125	°C
$T_{stg}$	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to GND.

(2) Absolute negative voltage on these pins not to go below -0.3 V.  
 (3) Absolute maximum voltage for duration less than 480 ms.

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	$\pm 4000$	V
		Charged device model (CDM), per AEC Q100-011	$\pm 1500$	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{IN}$	Unregulated input voltage	7 <sup>(1)</sup>	40	V
$V_{EN}$	Enable pin voltage	4	40	V
nRST, RDELAY, nWD_EN, WD_FLT <sup>(2)</sup> , WD_FLAG <sup>(3)</sup> , WD, FB <sup>(4)</sup>	Low voltage input or output	0	5.25	V
$T_J$	Operating junction temperature range	-40	150	°C

(1)  $V_{IN}$  can go down to 4 V for 130 ms or less and remain functional. If  $V_{IN}$  is less than 7 V for longer than 130 ms, then some devices can turn off until the input voltage rises above 7 V.  
 (2) Applicable for TPS7A63-Q1 only  
 (3) Applicable for TPS7A6401-Q1 only  
 (4) Applicable for TPS7A6301-Q1 and TPS7A6401-Q1 only

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS7A6401-Q1 TPS7A63-Q1		UNIT
		PWP (HTTSOP)	DRK (VSON)	
		14 PINS	10 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	46	36.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	32.6	36.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	27.4	11.6	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.2	0.5	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	27.2	11.7	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	2.5	3.8	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

V<sub>IN</sub> = 14 V, T<sub>J</sub> = –40°C to 150°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT VOLTAGE (VIN PIN)</b>					
V <sub>IN</sub>	Input voltage	V <sub>OUT</sub> = 2.5 V to 7 V, I <sub>OUT</sub> = 1 mA	7 <sup>(1)</sup>	40	V
I <sub>QUIESCENT</sub>	Quiescent current	V <sub>IN</sub> = 8.2 V to 18 V, V <sub>EN</sub> = 5 V, I <sub>OUT</sub> = 0.01 mA to 0.75 mA	35		µA
I <sub>SLEEP</sub>	Sleep or shutdown current	V <sub>IN</sub> = 8.2 V to 18 V, V <sub>EN</sub> < 0.8 V, I <sub>OUT</sub> = 0 mA (no load), T <sub>A</sub> = 125°C	3		µA
V <sub>IN-UVLO</sub>	Undervoltage lockout voltage	Ramp V <sub>IN</sub> down until output is turned OFF	3.16		V
V <sub>IN(POWERUP)</sub>	Power-up voltage	Ramp V <sub>IN</sub> up until output is turned ON	3.45		V
<b>DEVICE ENABLE INPUT (EN PIN)</b>					
V <sub>IL</sub>	Logic-input low level		0	0.8	V
V <sub>IH</sub>	Logic-input high level		2.5	40	V
<b>REGULATED OUTPUT VOLTAGE (VOUT PIN)</b>					
V <sub>OUT</sub>	Regulated output voltage	Fixed V <sub>OUT</sub> value (3.3 V, 5 V or a programmed value), I <sub>OUT</sub> = 10 mA to 200 mA, V <sub>IN</sub> = V <sub>OUT</sub> + 1 V to 16 V	–2%	2%	
ΔV <sub>LINE-REG</sub>	Line regulation	V <sub>IN</sub> = 6 V to 28 V, I <sub>OUT</sub> = 10 mA, V <sub>OUT</sub> = 5 V	15		mV
		V <sub>IN</sub> = 6 V to 28 V, I <sub>OUT</sub> = 10 mA, V <sub>OUT</sub> = 3.3 V	20		
ΔV <sub>LOAD-REG</sub>	Load regulation	I <sub>OUT</sub> = 10 mA to 200 mA, V <sub>IN</sub> = 14 V, V <sub>OUT</sub> = 5 V	25		mV
		I <sub>OUT</sub> = 10 mA to 200 mA, V <sub>IN</sub> = 14 V, V <sub>OUT</sub> = 3.3 V	35		
V <sub>DROPOUT</sub>	Dropout voltage (V <sub>IN</sub> – V <sub>OUT</sub> )	I <sub>OUT</sub> = 200 mA	500		mV
		I <sub>OUT</sub> = 150 mA	300		
R <sub>SW</sub> <sup>(2)</sup>	Switch resistance	VIN to VOUT resistance	2		Ω
I <sub>OUT</sub>	Output current	V <sub>OUT</sub> in regulation	0	200	mA
		[V <sub>OUT</sub> in regulation, V <sub>OUT</sub> = 3.3 V, V <sub>IN</sub> = 6 V] <sup>(3)</sup>	0	300	
I <sub>CL</sub>	Output current limit	V <sub>OUT</sub> = 0 V (VOUT pin is shorted to ground)	350	1000	mA
PSRR <sup>(4)</sup>	Power-supply ripple rejection	V <sub>IN-RIPPLE</sub> = 0.5 Vpp, I <sub>OUT</sub> = 200 mA, frequency = 100 Hz, V <sub>OUT</sub> = 5 V and V <sub>OUT</sub> = 3.3 V	60		dB
		V <sub>IN-RIPPLE</sub> = 0.5 Vpp, I <sub>OUT</sub> = 200 mA, frequency = 150 kHz, V <sub>OUT</sub> = 5 V and V <sub>OUT</sub> = 3.3 V	30		

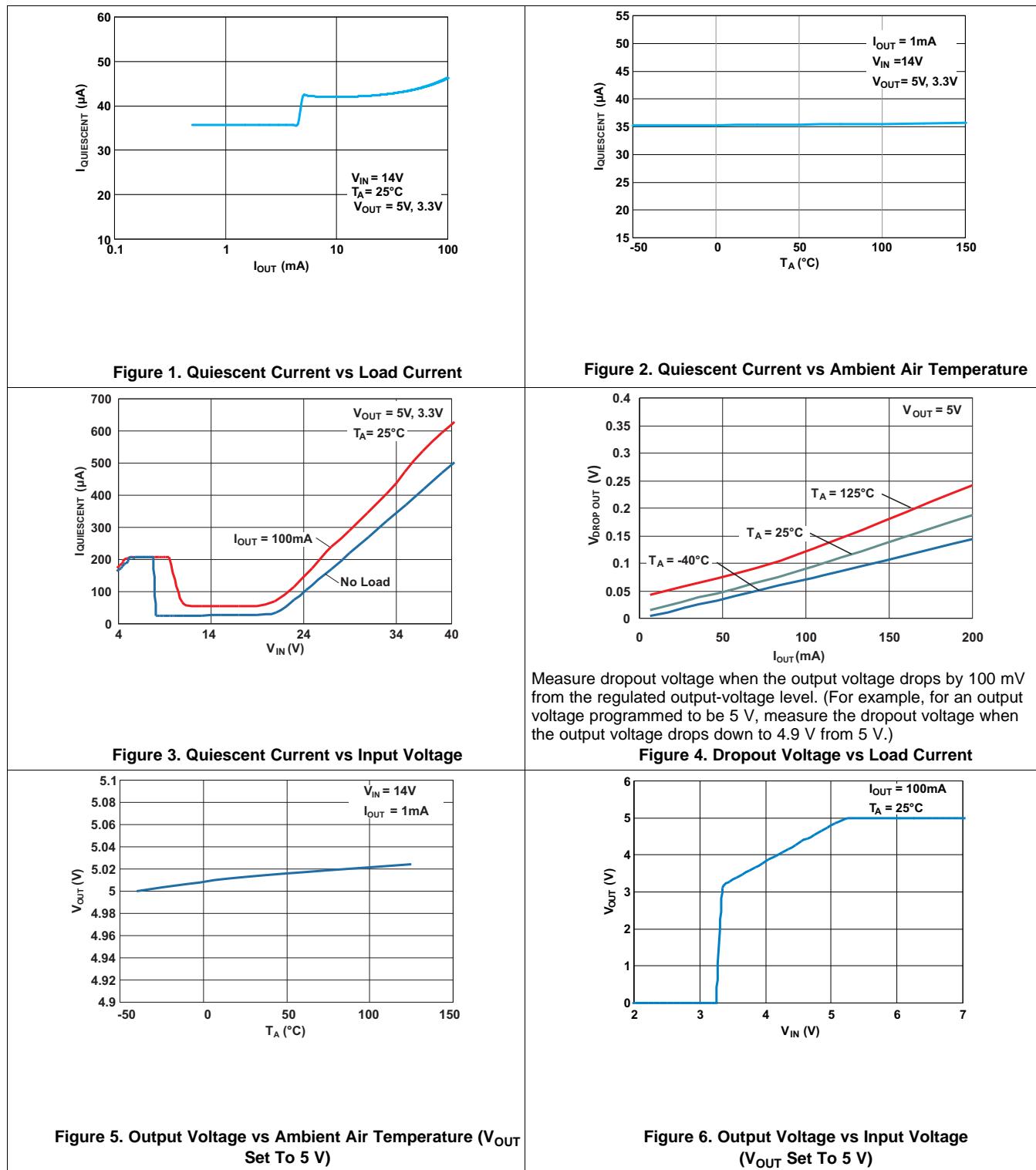
- (1) V<sub>IN</sub> can go down to 4 V for 130 ms or less and remain functional. If V<sub>IN</sub> is less than 7 V for longer than 130 ms, then some devices can turn off until the input voltage rises above 7 V.
- (2) This test is done with V<sub>OUT</sub> in regulation, measuring the V<sub>IN</sub> – V<sub>OUT</sub> parameter when V<sub>OUT</sub> drops by 100 mV from the programmed value (of V<sub>OUT</sub>) at specified loads.
- (3) Design Information - not tested; specified by characterization.
- (4) Specified by design - not tested.

## Electrical Characteristics (continued)

$V_{IN} = 14 \text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>RESET (nRST PIN)</b>						
$V_{OL}$	Reset pulled low	$I_{OL} = 5 \text{ mA}$			0.4	V
$I_{OH}$	Leakage current	Reset pulled to $V_{OUT}$ through a $5\text{-k}\Omega$ resistor			1	$\mu\text{A}$
$V_{TH(POR)}$	Power-on-reset threshold	$V_{OUT}$ powered up above internally set tolerance, $V_{OUT} = 5 \text{ V}$	4.5	4.65	4.77	V
		$V_{OUT}$ powered up above internally set tolerance, $V_{OUT} = 3.3 \text{ V}$			3.07	
$UV_{THRES}$	Reset threshold	$V_{OUT}$ falling below internally set tolerance, $V_{OUT} = 5 \text{ V}$	4.5	4.65	4.77	V
		$V_{OUT}$ falling below internally set tolerance, $V_{OUT} = 3.3 \text{ V}$			3.07	
$t_{POR}^{(3)}$	Power-on-reset delay	$C_{DLY} = 100 \text{ pF}$			300	$\mu\text{s}$
		$C_{DLY} = 100 \text{ nF}$			300	ms
$t_{POR-PRESET}$	Internally preset Power-on-reset delay	$C_{DLY}$ not connected, $V_{OUT} = 5 \text{ V}$ and $V_{OUT} = 3.3 \text{ V}$			250	$\mu\text{s}$
$t_{DEGLITCH}$	Reset deglitch time				5.5	$\mu\text{s}$
<b>RESET DELAY (RDELAY PIN)</b>						
$V_{TH(RDELAY)}$	Threshold to release nRST high	Voltage at RDELAY pin is ramped up	3	3.3		V
$I_{DLY}$	Delay capacitor charging current		0.75	1	1.25	$\mu\text{A}$
$I_{OL}$	Delay capacitor discharging current	Voltage at RDELAY pin = 1 V	5			mA
<b>CURRENT VOLTAGE REFERENCE (ROSC PIN)</b>						
$V_{ROSC}$	Voltage reference		0.95	1	1.05	V
<b>WATCHDOG FAULT / FLAG OUTPUT (WD_FLT / WD_FLAG Pin)</b>						
$V_{OL}$	Logic output low level	$I_{OL} = 5 \text{ mA}$			0.4	V
$I_{OH}$	Leakage current	WD_FLT/WD_FLAG pulled to $V_{OUT}$ through $5\text{-k}\Omega$ resistor			1	$\mu\text{A}$
<b>WATCHDOG ENABLE INPUT (nWD_EN PIN)</b>						
$V_{IL}$	Logic input low level				0.8	V
$V_{IH}$	Logic input high level	$3 \text{ V} < V_{DD} < 5.25 \text{ V}$			2.5	V
<b>WATCHDOG INPUT PULSE (WD PIN)</b>						
$V_{IL}$	Logic input low level				0.8	V
$V_{IH}$	Logic input high level	$3 \text{ V} < V_{DD} < 5.25 \text{ V}$			2.5	V
$t_{WD}$	Watchdog window duration	$R_{OSC} = 10 \text{ k}\Omega \pm 1\%$			10	ms
		$R_{OSC} = 20\text{k}\Omega \pm 1\%$			20	
$t_{WD-tol}$	Tolerance of watchdog period using external resistor	Excludes tolerance of $R_{OSC}$ (external resistor connected to ROSC pin)			-10% 10%	
$t_{WD-DEFAULT}$	Default watchdog period	External resistor not connected, ROSC pin is floating or open	108	164	254	ms
$t_{WD-HOLD}$	Minimum pulse width for resetting watch dog timer				1.65	$\mu\text{s}$
<b>OPERATING TEMPERATURE RANGE</b>						
$T_J$	Operating junction temperature		-40		150	$^\circ\text{C}$
$T_{SHUTDOWN}$	Thermal shutdown trip point				165	$^\circ\text{C}$
$T_{HYST}$	Thermal shutdown hysteresis				10	$^\circ\text{C}$

## 6.6 Typical Characteristics

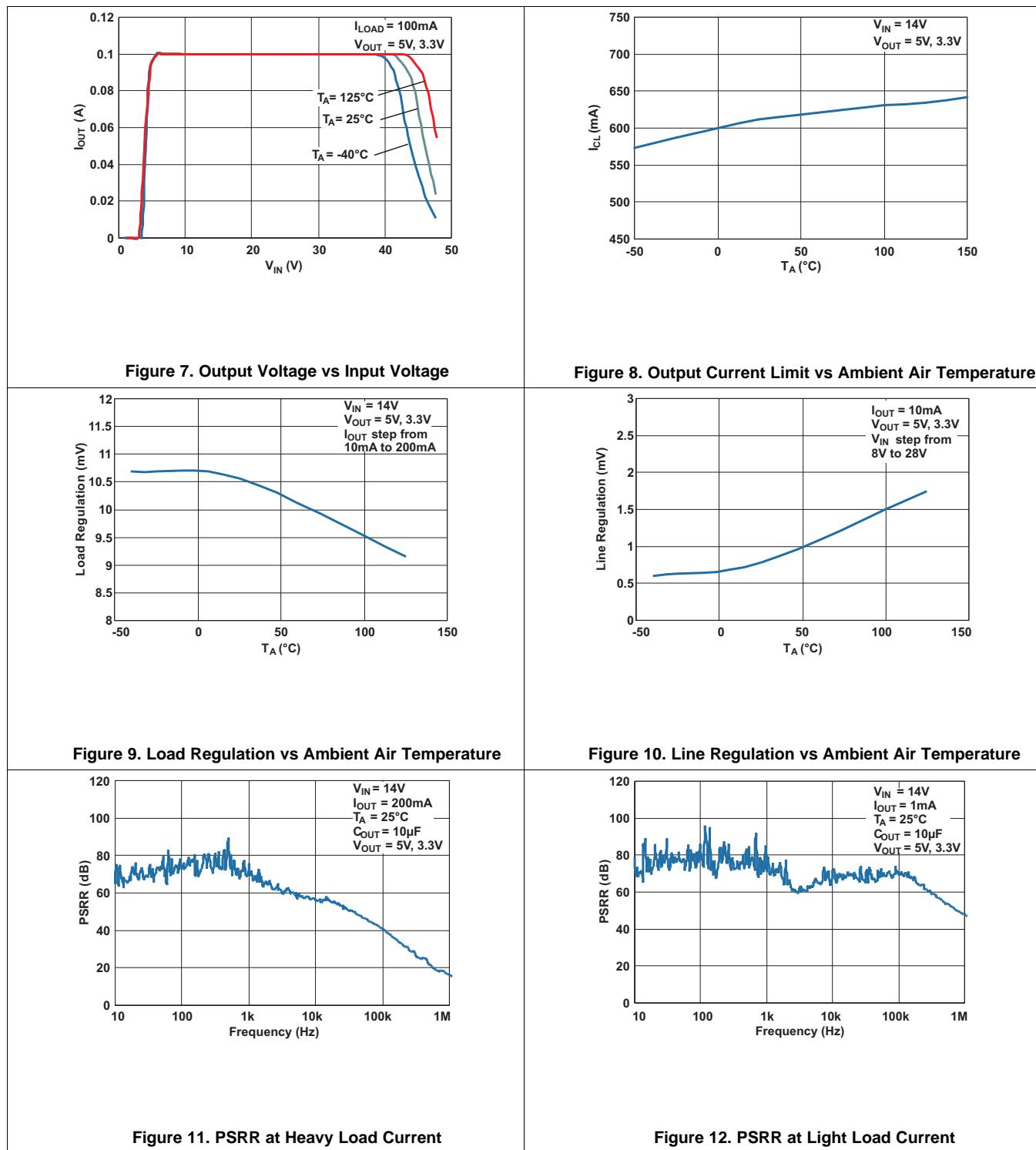


Measure dropout voltage when the output voltage drops by 100 mV from the regulated output-voltage level. (For example, for an output voltage programmed to be 5 V, measure the dropout voltage when the output voltage drops down to 4.9 V from 5 V.)

**Figure 5. Output Voltage vs Ambient Air Temperature (V<sub>OUT</sub> Set To 5 V)**

**Figure 6. Output Voltage vs Input Voltage (V<sub>OUT</sub> Set To 5 V)**

## Typical Characteristics (continued)



## 7 Detailed Description

### 7.1 Overview

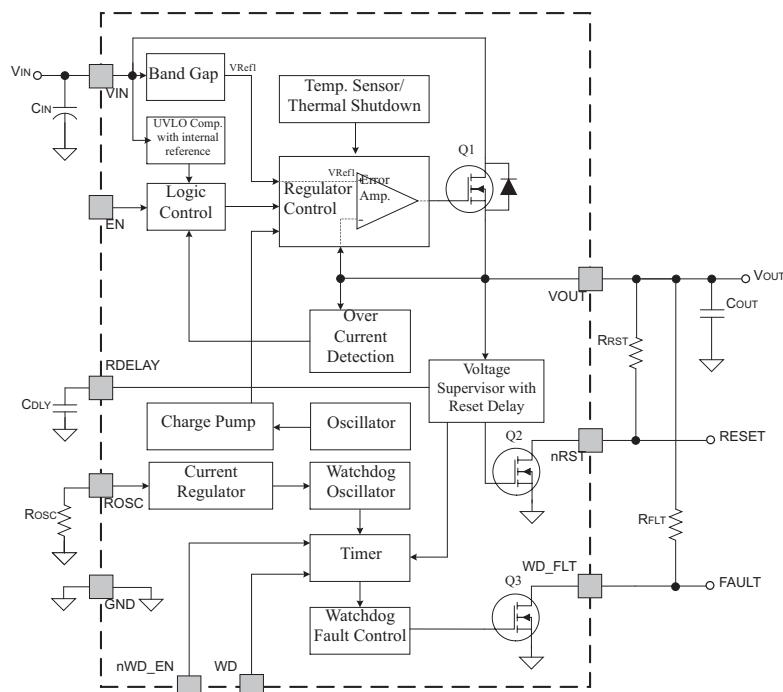
The TPS7A63-Q1 and TPS7A6401-Q1 are a family of monolithic low-dropout linear voltage regulators with integrated watchdog and reset functionality. These voltage regulators are designed for low power consumption and quiescent current less than 25  $\mu$ A in light-load applications. Because of a programmable reset delay (also called power-on-reset delay), these devices are well-suited in power supplies for microprocessors and microcontrollers.

These devices are available in two fixed and adjustable output-voltage versions as follows:

- Fault (WD\_FLT) output version: TPS7A63-Q1
- Flag (WD\_FLAG) output version: TPS7A6401-Q1

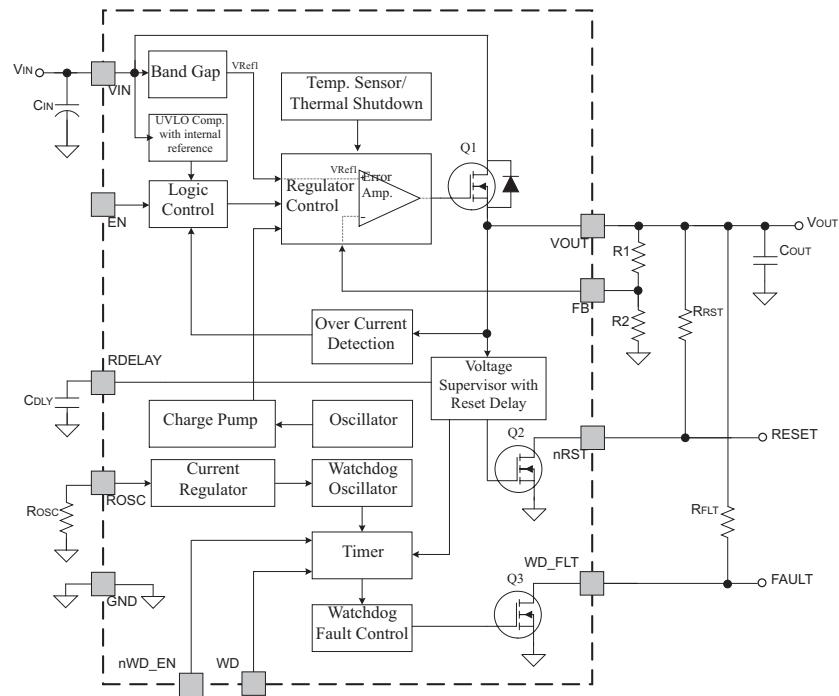
*Feature Description* describes the features of the TPS7A63-Q1 and TPS7A6401-Q1 voltage regulators in detail.

### 7.2 Functional Block Diagrams

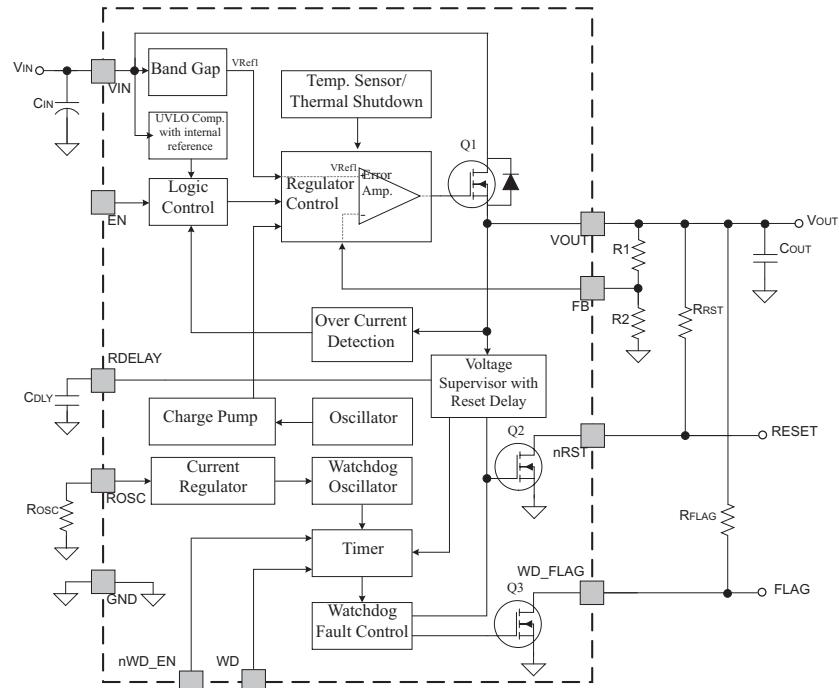


**Figure 13. TPS7A6333-Q1 and TPS7A6350-Q1 (Fixed Output Voltage With Fault Output)**

## Functional Block Diagrams (continued)



**Figure 14. TPS7A6301 (Adjustable Output Voltage With Fault Output)**



**Figure 15. TPS7A6401-Q1 (Adjustable Output Voltage With Flag Output)**

## 7.3 Feature Description

### 7.3.1 Power Up, Reset Delay, and Reset Output

During power up, the regulator incorporates a protection scheme to limit the current through the pass element and output capacitor. When the input voltage exceeds a certain threshold ( $V_{IN(POWERUP)}$ ) level, the output voltage begins to ramp up as shown in [Figure 16](#).

When starting up, and also when the output recovers from a negative voltage spike due to a load step or a dip in the input voltage for a specified duration, the device implements reset delay to indicate that output voltage is stable and in regulation.

When the output voltage reaches the power-on-reset threshold ( $V_{TH(POR)}$ ) level, that is, 93% of regulated output voltage (3.3 V or 5 V, or a programmed value), a constant output current charges an external capacitor ( $C_{DLY}$ ) to an internal threshold ( $V_{TH(RDELAY)}$ ) voltage level. Then, nRST asserts high and  $C_{DLY}$  discharges through an internal load. This allows  $C_{DLY}$  to charge from approximately 0 V during the next power cycle.

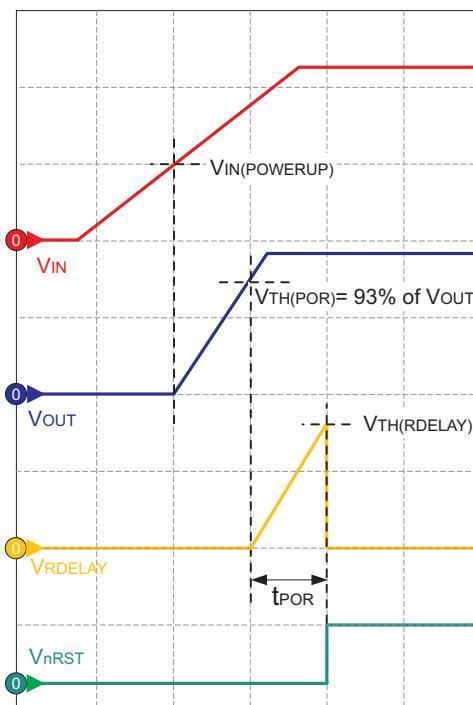
Program the reset delay time by connecting an external capacitor ( $C_{DLY}$ , 100 pF to 100 nF) to the RDELAY pin. [Equation 1](#) gives the delay time:

$$t_{POR} = \frac{C_{DLY} \times 3}{1 \times 10^{-6}}$$

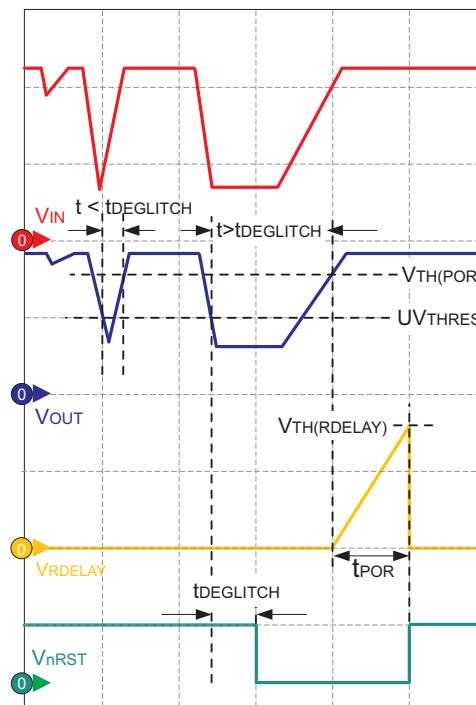
where

- $t_{POR}$  = reset delay time in seconds
- $C_{DLY}$  = reset delay capacitor value in farads

(1)



**Figure 16. Power Up and Conditions for Activation of Reset**



**Figure 17. Reset Delay and Deglitch Filter**

As [Figure 17](#) shows, if the regulated output voltage falls below 93% of the set level, nRST asserts low after a short de-glitch time of approximately 5.5  $\mu$ s (typical). In case of negative transients in the input voltage ( $V_{IN}$ ), the reset signal asserts low only if the output ( $V_{OUT}$ ) drops and stays below the reset threshold level ( $V_{TH(POR)}$ ) for more than the deglitch time ( $t_{DEGLITCH}$ ), as [Figure 17](#) and [Figure 20](#) illustrate. While nRST is low, if the input voltage returns to the nominal operating voltage, the normal power-up sequence ensues. nRST asserts high only if the output voltage exceeds the reset threshold voltage ( $V_{TH(POR)}$ ) and the reset delay time ( $t_{POR}$ ) has elapsed.

## Feature Description (continued)

### 7.3.2 Adjustable Output Voltage

Program the regulated output voltage ( $V_{OUT}$ ) by connecting external resistors to FB pin. Calculate the feedback resistor values using [Equation 2](#).

$$V_{OUT} = V_{REF} \left[ 1 + \frac{R1}{R2} \right]$$

where

- $V_{OUT}$  = desired output voltage
- $V_{REF}$  = reference voltage ( $V_{REF} = 1.23$  V, typically)
- $R1, R2$  = feedback resistors (see [Figure 15](#))

(2)

[Equation 3](#) gives the overall tolerance of the regulated output.

$$tol_{V_{OUT}} = tol_{V_{REF}} + \left[ \frac{R1}{R1 + R2} \right] [tol_{R1} + tol_{R2}]$$

where

- $tol_{V_{OUT}}$  = tolerance of the output voltage
- $tol_{V_{REF}}$  = tolerance of the internal reference voltage ( $tol_{V_{REF}} = \pm 1.5\%$  typically)
- $tol_{R1}, tol_{R2}$  = tolerance of feedback resistors  $R1, R2$

(3)

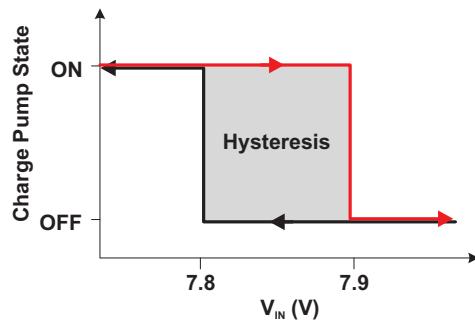
For a tighter tolerance on  $V_{OUT}$ , select lower-value feedback resistors. TI recommends to select feedback resistors such that the sum of  $R1$  and  $R2$  is from  $20\text{ k}\Omega$  to  $200\text{ k}\Omega$ .

### 7.3.3 Chip Enable

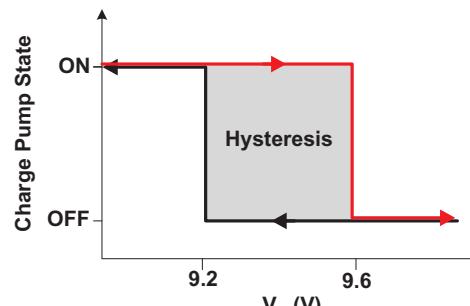
These devices have a high-voltage-tolerant EN pin that an external microcontroller or a digital control circuit can use to enable and disable them. A high input to this pin activates the device and turns the regulator on. For self bias applications, connect this input to the VIN terminal. An internal pulldown resistor is connected to this pin, and therefore if this pin remains unconnected, the device stays disabled.

### 7.3.4 Charge Pump Operation

These devices have an internal charge pump which turns on or off depending on the input voltage and the output current. The charge pump switching circuitry must not cause conducted emissions to exceed required thresholds on the input voltage line. For a given output current, the charge pump stays on at lower input voltages and turns off at higher input voltages. The charge pump switching thresholds are hysteretic. [Figure 18](#) and [Figure 19](#) show typical switching thresholds for the charge pump at light ( $I_{OUT} <$  approximately  $2\text{ mA}$ ) and heavy ( $I_{OUT} >$  approximately  $2\text{ mA}$ ) loads, respectively.



**Figure 18. Charge Pump Operation at Light Loads**



**Figure 19. Charge Pump Operation at Heavy Loads**

### 7.3.5 Low-Power Mode

At light loads and high input voltages ( $V_{IN} >$  approximately 8 V, such that the charge pump is off), the device operates in low-power mode and the quiescent current consumption is reduced to 25  $\mu$ A (typical) as shown in Table 1.

**Table 1. Typical Quiescent Current Consumption**

$I_{OUT}$	Charge Pump ON	Charge Pump OFF
$I_{OUT} <$ approximately 2 mA (Light load)	250 $\mu$ A	35 $\mu$ A (Low-power mode)
$I_{OUT} >$ approximately 2 mA (Heavy load)	280 $\mu$ A	70 $\mu$ A

### 7.3.6 Undervoltage Shutdown

These devices have an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage ( $V_{IN}$ ) falls below an internally fixed UVLO threshold level ( $V_{IN-UVLO}$ ). This ensures that the regulator does not latch into an unknown state during low input voltage conditions. The regulator powers up when the input voltage exceeds the  $V_{IN(POWERUP)}$  level, as Figure 20 shows.

### 7.3.7 Low-Voltage Tracking

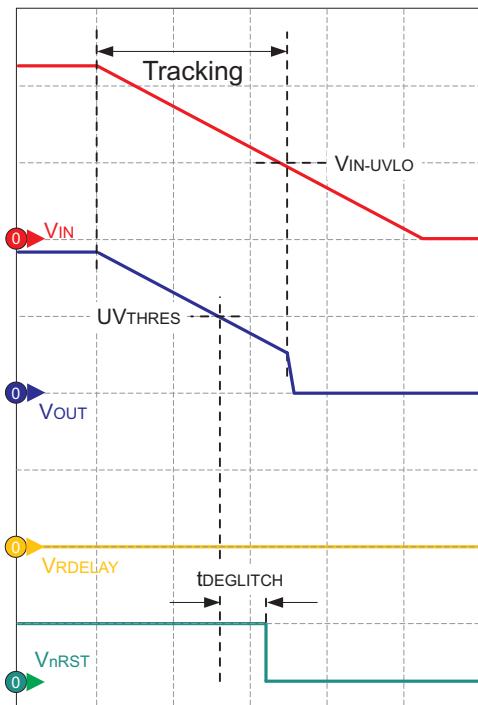
At low input voltages, the regulator drops out of regulation, and the output voltage tracks the input minus a voltage based on the load current ( $I_{OUT}$ ) and switch resistance ( $R_{SW}$ ), as Figure 20 shows. This feature allows for a smaller input capacitor and can possibly eliminate the need of using a boost convertor during cold crank conditions, as Figure 20 shows.

### 7.3.8 Integrated Fault Protection

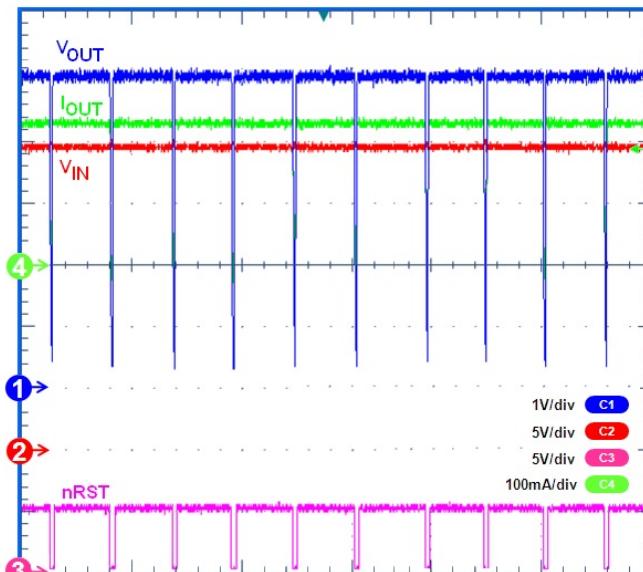
These devices feature integrated fault protection to make them ideal for use in automotive applications. In order to remain in a safe area of operation during certain fault conditions, the devices use internal current-limit protection and current-limit foldback to limit the maximum output current. This protects them from excessive power dissipation. For example, during a short-circuit condition on the output, fault protection limits the current through the pass element to  $I_{CL}$  to protect the device from excessive power dissipation.

### 7.3.9 Thermal Shutdown

These devices incorporate a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. The junction temperature exceeding the TSD trip point causes the output to turn off. When the junction temperature falls below TSD trip point, the output turns on again, as Figure 21 shows.



**Figure 20. Low-Voltage Tracking and Undervoltage Lockout**



**Figure 21. Thermal Cycling Waveform for TPS7A6350-Q1 ( $V_{IN} = 24$  V,  $I_{OUT} = 200$  mA,  $V_{OUT} = 5$  V)**

### 7.3.10 Integrated Window Watchdog

These devices have an integrated watchdog with fault (WD\_FLT) and flag (WD\_FLAG) output options. Both device options are available in fixed- and adjustable-output versions. The watchdog operation, service fault conditions, and difference between fault (TPS7A63-Q1) and flag (TPS7A6401-Q1) output versions are described as follows.

#### 7.3.10.1 Programmable-Window Watchdog

Program the duration of the watchdog window by connecting an external resistor ( $R_{OSC}$ ) to ground at the ROSC pin. The current through the resistor sets the clock frequency of the internal oscillator. The user can adjust the duration of the watchdog window (that is, the watchdog timer period) by changing the resistor value. The duration of the watchdog window and the duration of the fault output are multiples of the internal oscillator frequency and are given by the following equations:

$$t_{WD} = 10^{-6} \times R_{OSC} = 5000 \times 1 / f_{OSC} \quad (4)$$

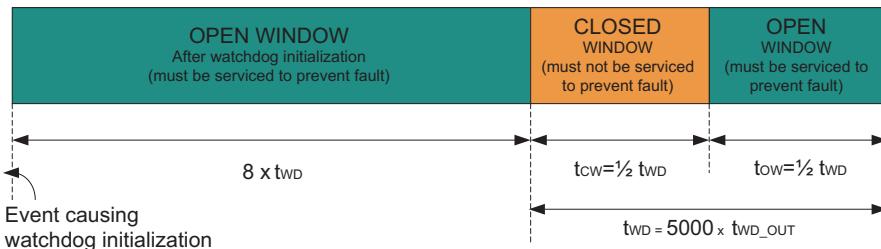
$$t_{WD\_OUT} = 1 / f_{OSC} \quad (5)$$

$$t_{CW} = t_{OW} = 1 / 2 t_{WD}$$

where

- $t_{WD}$  = width of watchdog window
- $R_{OSC}$  = resistor connected at ROSC pin
- $t_{WD\_OUT}$  = duration of fault output
- $f_{OSC}$  = frequency of internal oscillator
- $t_{CW}$  = duration of closed window
- $t_{OW}$  = duration of open window

As shown in Figure 22, each watchdog window consists of an open window and a closed window, each having a width approximately 50% of the watchdog window. However, there is an exception to this; the first open window after watchdog initialization is eight times the duration of the watchdog window. All open windows except the one after watchdog initialization are one-half the width of the watchdog window. On initialization, the watchdog must receive service (by software, external microcontroller, and so forth) only during an open window. A watchdog serviced during a closed window, or not serviced during a open window, creates a watchdog fault condition.



**Figure 22. Watchdog Window Duration**

### 7.3.10.2 Watchdog Enable

An external microcontroller or a digital circuit can apply an appropriate signal to the nWD\_EN pin to enable or disable the watchdog. A low input to this pin turns the watchdog on. Because of an internal pulldown resistor connected to this pin, leaving the pin unconnected keeps the watchdog enabled.

### 7.3.10.3 Watchdog Service Signal

In order for the watchdog service signal (WD) to service an open window correctly, the service signal must stay high for a duration of at least  $t_{WD\_HOLD}$ . The recommended value of  $t_{WD\_HOLD}$  is given by [Equation 7](#):

$$t_{WD\_HOLD} = 3 \times t_{WD\_OUT} \quad (7)$$

### 7.3.10.4 Watchdog Fault Outputs

The WD\_FLT pin and WD\_FLAG pin are fault output terminals for the TPS7A63-Q1 and TPS7A6401-Q1 devices, respectively. Typically, one pulls these fault outputs high to a regulated output supply. In the case of a watchdog fault condition, the TPS7A63-Q1 momentarily pulls WD\_FLT low for a duration of  $t_{WD\_OUT}$ , whereas the TPS7A6401-Q1 latches the WD\_FLAG high and momentarily pulls nRST low for a duration of  $t_{WD\_OUT}$ .

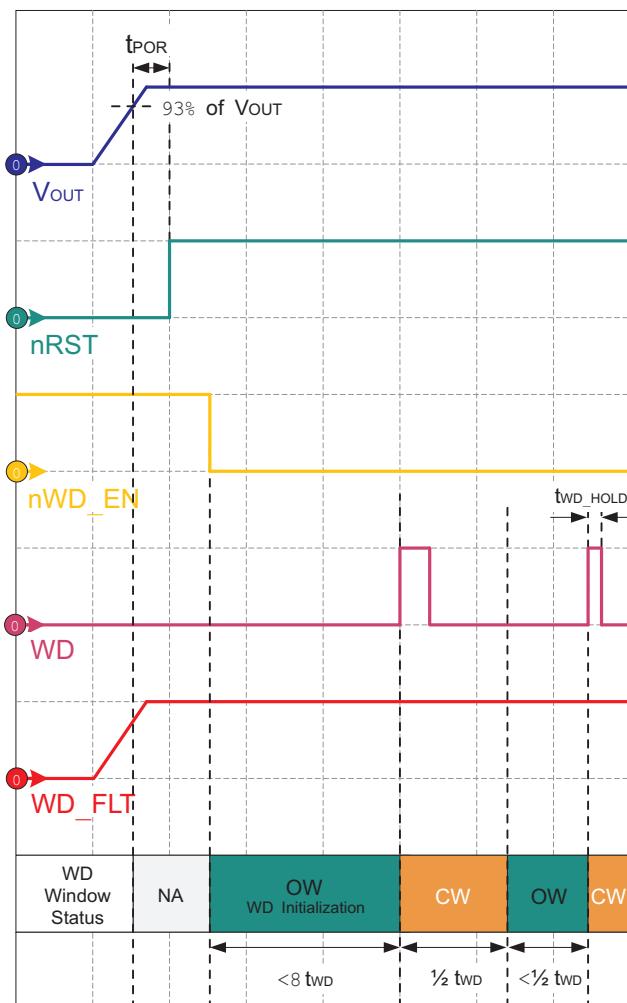
### 7.3.10.5 Watchdog Initialization

On power up and during normal operation, the watchdog initializes under the conditions shown in [Table 2](#). The normal operation of the watchdog for the WD\_FLT and WD\_FLAG output device options is shown in [Figure 23](#) and [Figure 24](#), respectively.

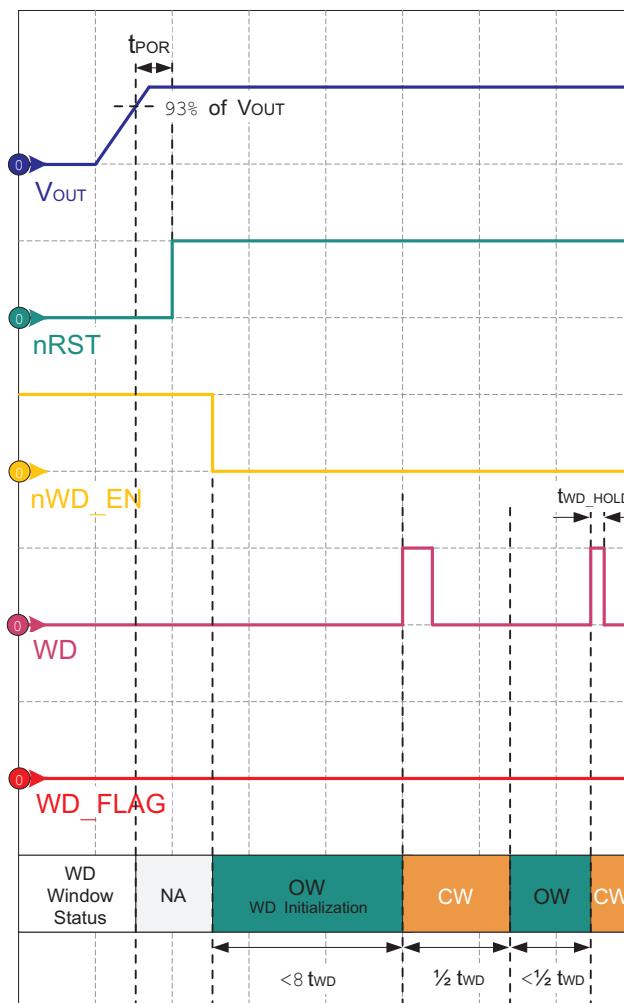
**Table 2. Conditions For Watchdog Initialization**

Edge	What causes watchdog to initialize?	TPS7A63-Q1 (FAULT Option)	TPS7A6401-Q1 (FLAG Option)
	Rising edge of nRST (when $V_{OUT}$ exceeds $V_{TH(POR)}$ ) while the watchdog is in the enabled state, for example, during soft power up	✓	✓
	Falling edge of nWD_EN while the nRST is already high, for example, when the microprocessor enables the watchdog after the device is powered up	✓	✓
	Rising edge of WD_FLT while the nRST is already high and the watchdog is in the enabled state, for example, right after a closed window is serviced	✓	X

### 7.3.10.6 Watchdog Operation



**Figure 23. Power Up, Initialization, and Normal Operation for TPS7A63-Q1**



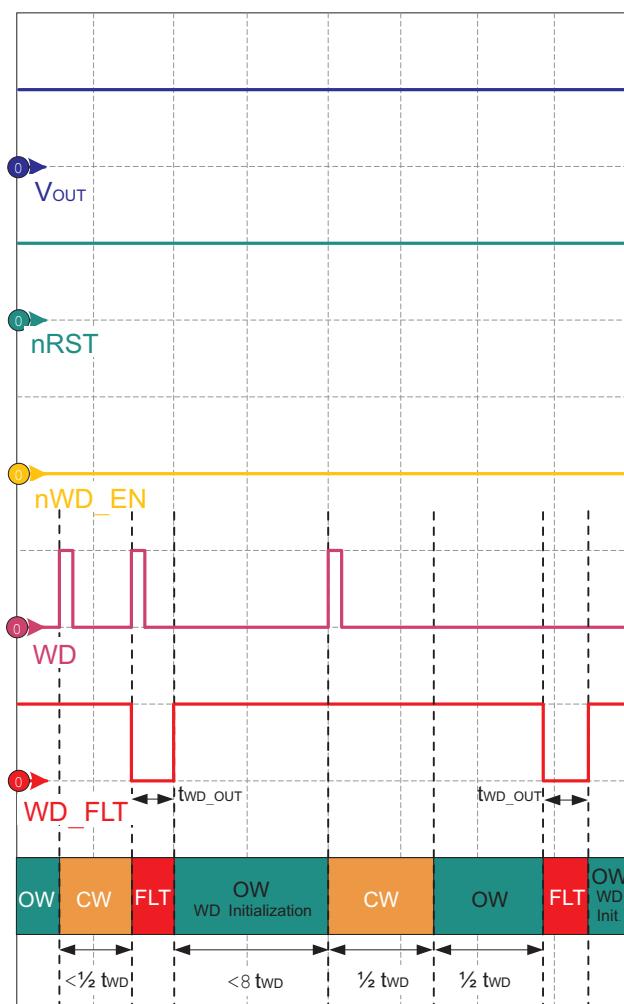
**Figure 24. Power Up, Initialization, and Normal Operation for TPS7A6401-Q1**

Figure 23 shows watchdog initialization and operation for the TPS7A63-Q1. After output voltage is in regulation and reset asserts high (clearly the chip-enable pin is high), the watchdog becomes enabled when an external signal pulls nWD\_EN (the watchdog enable pin) low. This causes the watchdog to initialize and wait for a service signal during the first open window for 8x the duration of tWD. A service signal applied to the WD pin during the first open window resets the watchdog counter and a closed window starts. To prevent a fault condition from occurring, watchdog service must not occur during the closed window. Watchdog service must occur during the following open window to prevent fault condition from occurring. The fault output (WD\_FLT), externally pulled up to VOUT (typically), stays high as long as the watchdog receives proper serviced and there is no fault condition.

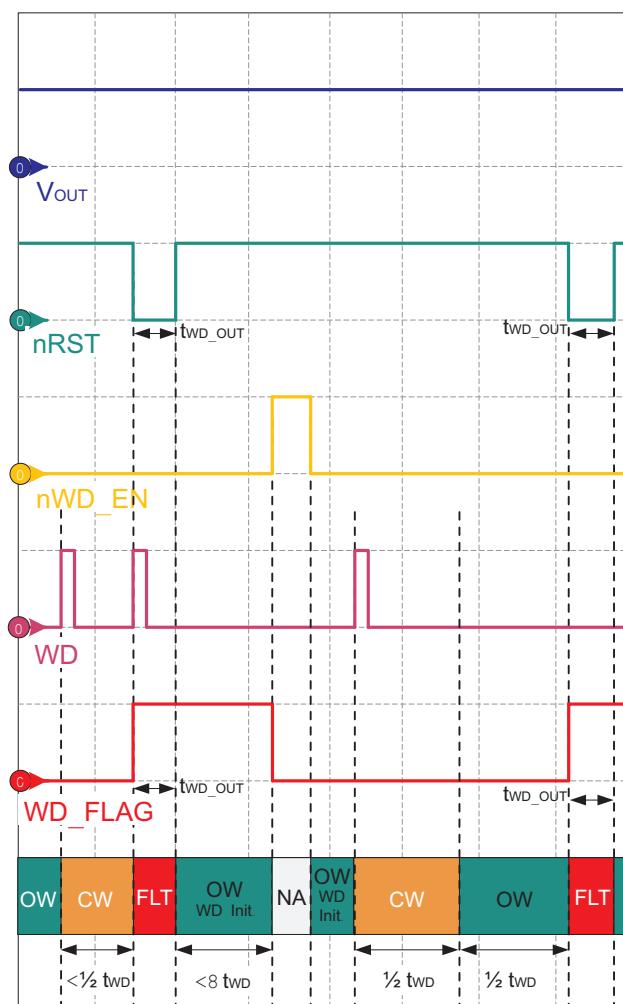
Figure 24 shows watchdog initialization and operation for FLAG output version (TPS7A6401-Q1). The fault output (WD\_FLAG), externally pulled up to VOUT (typically), stays low as long as the watchdog receives proper service and there is no fault condition.

Likewise, enabling the watchdog before powering the device on (that is, pulling the nWD\_EN pin low before power up), the watchdog initializes as soon as the output voltage is in regulation and reset asserts high (see Table 2 for Conditions for Watchdog Initialization).

### 7.3.10.7 Watchdog Fault Conditions



**Figure 25. Watchdog Service Fault Conditions for TPS7A63-Q1**



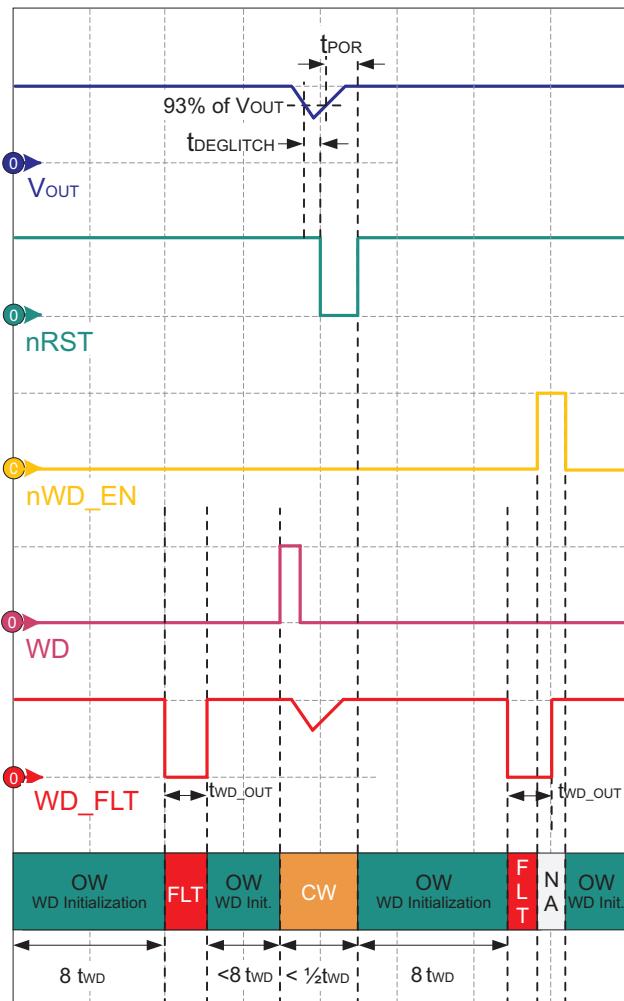
**Figure 26. Watchdog Service Fault Conditions for TPS7A6401-Q1**

For both device options, a watchdog fault condition occurs in following (non-exhaustive) cases:

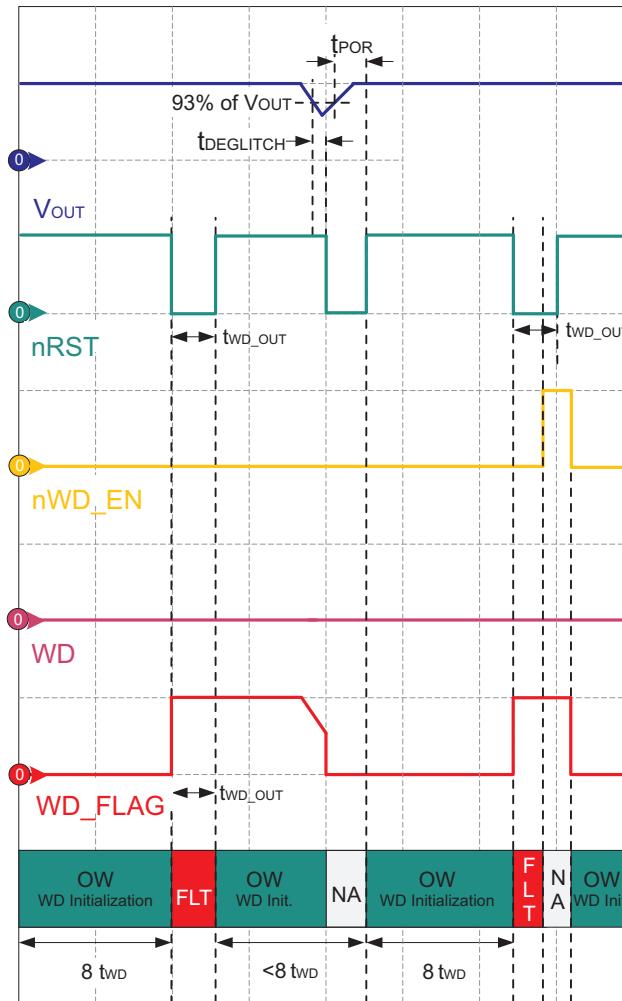
- When the watchdog receives service during a closed window.
- When watchdog does not receive service during an open window (this open window could be the one after watchdog initialization, or the one following a closed window).

As shown in [Figure 25](#), for TPS7A63-Q1 the first watchdog fault registers when the watchdog receives service during a closed window. This causes the watchdog fault pin (WD\_FLT) to go low temporarily for a duration of  $t_{WD\_OUT}$ . Following the fault, the watchdog reinitializes. Likewise, the second fault registers when the watchdog does not receive service during an open window (following a closed window). Again, the fault pin (WD\_FLT) asserts low for a duration of  $t_{WD\_OUT}$ .

As shown in [Figure 26](#), for TPS7A6401-Q1 the first watchdog fault registers when watchdog receives service during a closes window. This causes the watchdog flag pin (WD\_FLAG) to become high and stay latched. At the same time, nRST pin goes low temporarily for the duration of  $t_{WD\_OUT}$ . WD\_FLAG remains high until toggling the nWD\_EN pin disables and re-enables the watchdog or the watchdog receives service properly (while nWD\_EN is low and nRST is high). The second fault registers when the watchdog does not receive service during an open window (following a closed window). While WD\_FLAG is high (that is, during a fault condition), if the watchdog stays enabled, and reset is high; a watchdog service signal can also bring WD\_FLAG low (about 5  $\mu$ s after the watchdog receives service).



**Figure 27. Watchdog Fault During Initialization, and Reinitialization During Reset for TPS7A63-Q1**



**Figure 28. Watchdog Fault During Initialization, and Reinitialization During Reset for TPS7A6401-Q1**

As shown in [Figure 27](#) for the TPS7A6401-Q1, the watchdog fault condition also occurs if the watchdog does not receive service during the open window after watchdog initialization. That is, if the watchdog does not receive service during the first  $8 \times t_{WD\_OUT}$  period after initialization, a fault condition occurs. This causes the watchdog fault pin (WD\_FLT) to go low temporarily for a duration of  $t_{WD\_OUT}$ . In case of a load transient, if the regulated output voltage drops down causing reset (nRST) to go low, the rising edge on nRST causes the watchdog to reinitialize (that is, when reset becomes high with the watchdog still enabled). During a fault condition (that is, WD\_FLT is low) with the watchdog disabled, the fault output continues to stay low until  $t_{WD\_OUT}$  is elapsed. A falling edge on nWD\_EN pin causes the watchdog to reinitialize while nRST is still high.

As shown in [Figure 28](#) for the TPS7A6401-Q1, the watchdog fault condition also occurs if the watchdog does not receive service during the open window after watchdog initialization. That is, if the watchdog does not receive service in first  $8 \times t_{WD\_OUT}$  period after initialization, a fault condition occurs. This causes the watchdog flag pin (WD\_FLAG) to become high and stay latched. At the same time, the nRST pin goes low temporarily for a duration of  $t_{WD\_OUT}$ . In the case of a load transient, if the regulated output voltage drops down causing the reset output to go low, the WD\_FLAG asserts low, and the rising edge on nRST causes the watchdog to reinitialize (while the watchdog remains enabled). During a fault condition (that is, WD\_FLAG is high), and with a disabled watchdog, the flag output continues to stay high as long as the watchdog remains enabled or receives proper service. However, nRST stays low until  $t_{WD\_OUT}$  elapses. Re-enabling the watchdog causes watchdog to reinitialize (while nRST is still high).

## 7.4 Device Functional Modes

### 7.4.1 Operation With $V_{IN}$ Lower Than 4 V

The TPS7A63-Q1 and TPS7A6401-Q1 family devices operate with input voltage above 4 V. The typical UVLO voltage is 3.16 V. The device can operate at input voltage lower than 4 V, but at input voltage below the actual UVLO, the device will shut down.

### 7.4.2 Operation With $V_{IN}$ Larger Than 4 V

When  $V_{IN}$  is greater than 4 V, if the input voltage is higher than  $V_{OUT}$  plus the dropout voltage, the output voltage is equal to the set value. Otherwise, the output voltage is equal to  $V_{IN}$  minus the dropout voltage.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

Typical application circuits for TPS76333-Q1/TPS76350-Q1 and TPS7A6401-Q1 are shown in [Figure 29](#) and [Figure 32](#). Depending on the end application, one may use different values of external components. Carefully select feedback resistors (R1 and R2), used to program the output voltage. Using smaller resistors results in higher current consumption, whereas using very large resistors impacts the sensitivity of the regulator. Therefore, TI recommends selecting feedback resistors such that the sum of R1 and R2 is from 20 k $\Omega$  to 200 k $\Omega$ .

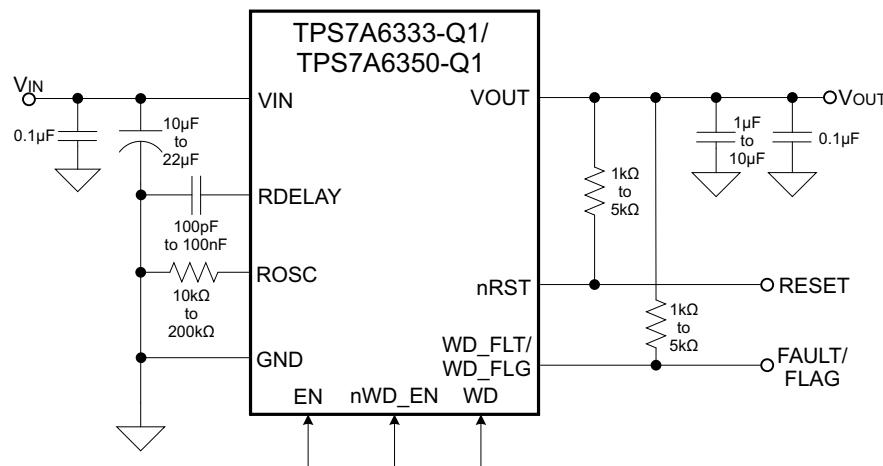
#### 8.1.1 Example

If the desired regulated output voltage is 5 V, after selecting R2 then one can calculate R1 using (or vice versa) [Equation 2](#). Knowing  $V_{REF} = 1.23$  V (typical),  $V_{OUT} = 5$  V, selecting  $R2 = 20$  k $\Omega$ , the calculated value of R1 is 61.3 k $\Omega$ .

During fast load steps, an application may require a larger output capacitor to prevent the output from temporarily dropping down. TI recommends a low-ESR ceramic capacitor with dielectric of type X5R or X7R. One can also connect a bypass capacitor at the output to decouple high-frequency noise as per the end application.

### 8.2 Typical Applications

#### 8.2.1 Typical Application Using the TPS7A6333-Q1 or TPS7A6350-Q1



**Figure 29. Typical Application Schematic, TPS7A6333-Q1/6350-Q1**

## Typical Applications (continued)

### 8.2.1.1 Design Requirements

For this design example, use the parameters listed in [Table 3](#).

**Table 3. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUES
Input voltage range	7 V - 40 V
Input capacitor range	10 $\mu$ F - 22 $\mu$ F
Output voltage	3.3 V, 5 V
Output current rating	300 mA maximum
Output capacitor range	1 $\mu$ F-10 $\mu$ F

### 8.2.1.2 Detailed Design Procedure

When using the TPS7A6333-Q1, TPS7A6350-Q1, TI recommends adding a 10- $\mu$ F to 22- $\mu$ F capacitor to the input to keep the input voltage stable. TI also recommends adding a 1- $\mu$ F to 10- $\mu$ F low ESR ceramic capacitor to get a stable output.

The reset delay time is set by an external capacitor (CDLY) to ground, capacitor value typical from 100 pF to 100 nF. [Equation 1](#) provides the method for the calculation.

Connecting an external resistor to ground at the ROSC pin can set the duration of the watchdog window. [Equation 4](#) provides the method for the calculation. Usually a 10-k $\Omega$  to 200-k $\Omega$  resistor can be used to set the time.

### 8.2.1.3 Application Curves

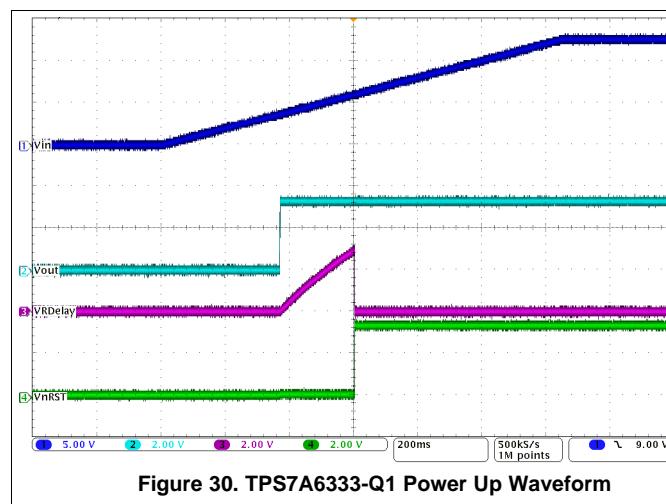


Figure 30. TPS7A6333-Q1 Power Up Waveform

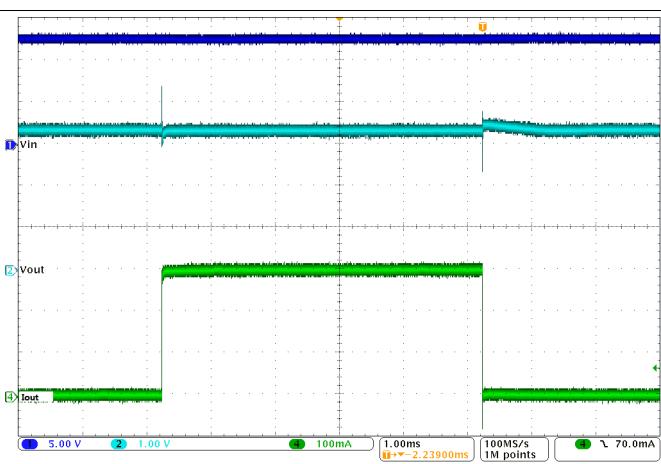
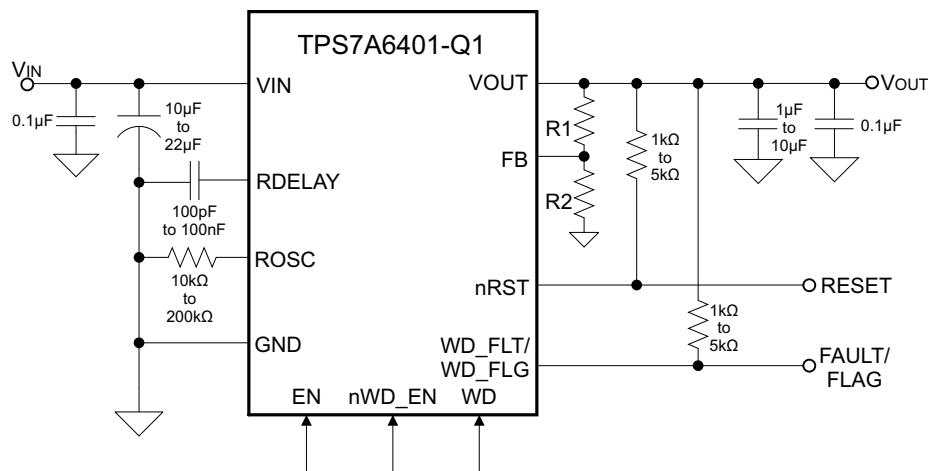


Figure 31. TPS7A6333-Q1 Load Transient Waveform

## 8.2.2 Typical Application Using the TPS7A6401-Q1



**Figure 32. Typical Application Schematic TPS7A6401-Q1**

### 8.2.2.1 Design Requirements

For this design example, use the parameters listed in [Table 4](#).

**Table 4. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUES
Input voltage range	7 V - 40 V
Input capacitor range	10 µF-22 µF
Output voltage	2.5 V - 7 V
Output current rating	300 mA maximum
Output capacitor range	1 µF-10 µF

### 8.2.2.2 Detailed Design Procedure

When using TPS7A6401-Q1, TI recommends adding a 10-µF to 22-µF capacitor to the input to keep the input voltage stable. TI also recommends adding a 1-µF to 10-µF low ESR ceramic capacitor to get a stable output.

The output voltage is set by the R1 and R2 resistor network. Output voltage can be calculated by [Equation 2](#).

The reset delay time is set by an external capacitor (CDLY) to ground, capacitor value typical from 100 pF to 100 nF. [Equation 1](#) provides the method for the calculation. Connecting an external resistor to ground at the ROSC pin can set the duration of the watchdog window. [Equation 4](#) provides the method for the calculation. Usually a 10-kΩ to 200-kΩ resistor can be used to set the time.

### 8.2.2.3 Application Curves

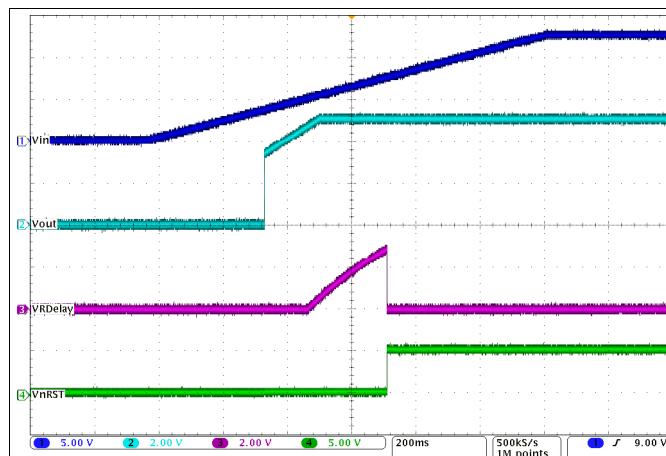


Figure 33. TPS7A6401-Q1 Power Up Waveform

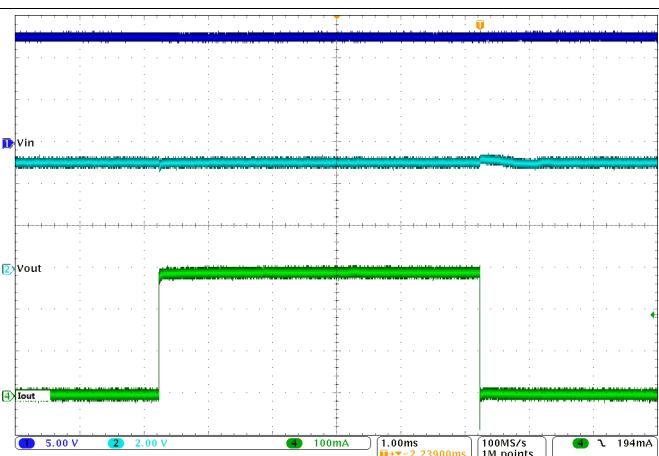


Figure 34. TPS7A6401-Q1 Load Transient Waveform

## 9 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range from 7 V to 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7A63XX-Q1 or TPS7A64XX-Q1 device, TI recommends adding an electrolytic capacitor with a value of 10  $\mu$ F and a ceramic bypass capacitor at the input.

## 10 Layout

### 10.1 Layout Guidelines

For the LDO power supply, especially these high voltage and large current ones, layout is an important step. If layout is not carefully designed, the regulator could not deliver enough output current because of the thermal limitation. To improve the thermal performance of the device, and maximize the current output at high ambient temperature, it is recommended to spread the thermal pad as large as possible and put enough thermal vias on the thermal pad. [Figure 37](#) shows an example layout.

#### 10.1.1 Power Dissipation and Thermal Considerations

Calculated the power dissipated in the device using [Equation 8](#).

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + I_{QUIESCENT} \times V_{IN}$$

where

- $P_D$  = continuous power dissipation
- $I_{OUT}$  = output current
- $V_{IN}$  = input voltage
- $V_{OUT}$  = output voltage
- $I_{QUIESCENT}$  = quiescent current

(8)

As  $I_{QUIESCENT} \ll I_{OUT}$ , therefore, ignore the term  $I_{QUIESCENT} \times V_{IN}$  in [Equation 8](#).

For a device in operation at a given ambient air temperature ( $T_A$ ), calculate the junction temperature ( $T_J$ ) using [Equation 9](#).

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where

- $R_{\theta JA}$  = junction-to-ambient-air thermal impedance

(9)

Calculate the rise in junction temperature due to power dissipation using [Equation 10](#).

## Layout Guidelines (continued)

$$\Delta T = T_J - T_A = (R_{\theta JA} \times P_D) \quad (10)$$

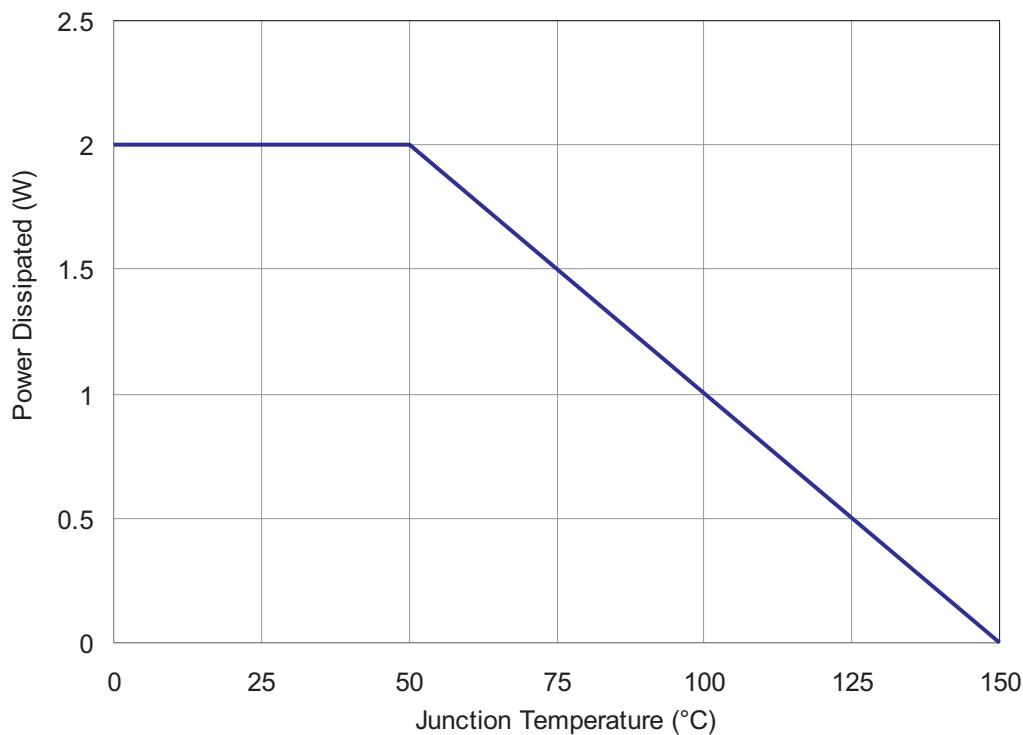
For a given maximum junction temperature ( $T_{J\text{-Max}}$ ), calculate the maximum ambient air temperature ( $T_{A\text{-Max}}$ ) at which the device can operate using [Equation 11](#).

$$T_{A\text{-Max}} = T_{J\text{-Max}} - (R_{\theta JA} \times P_D) \quad (11)$$

### 10.1.1.1 Example

If  $I_{OUT} = 100$  mA,  $V_{OUT} = 5$  V,  $V_{IN} = 14$  V,  $I_{QUIESCENT} = 250$   $\mu$ A, and  $R_{\theta JA} = 50^\circ\text{C}/\text{W}$ , the continuous power dissipated in the device is 0.9 W. The rise in junction temperature due to power dissipation is  $45^\circ\text{C}$ . For a maximum junction temperature of  $150^\circ\text{C}$ , the maximum ambient air temperature at which the device can operate is  $105^\circ\text{C}$ .

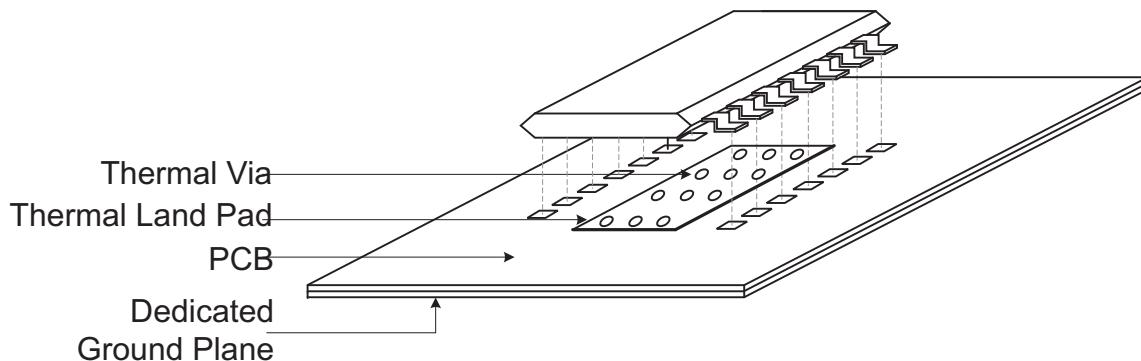
For adequate heat dissipation, TI recommends soldering the thermal pad (exposed heat sink) to the thermal land pad on the PCB. Doing this provides a heat conduction path from the die to the PCB and reduces overall package thermal resistance. Power derating curves for the TPS7A63-Q1 and TPS7A6401-Q1 PWP package and TPS7A6333-Q1 DRK are comparable; see [Figure 35](#).



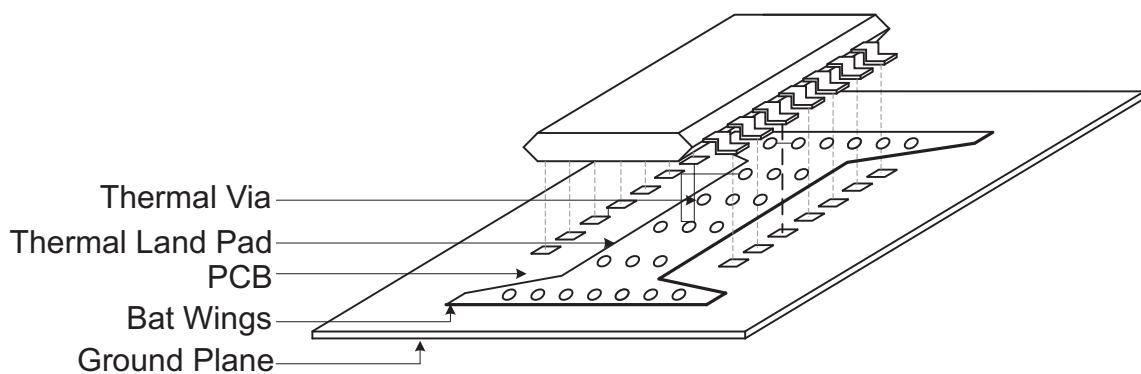
**Figure 35. Power Derating Curve**

For optimum thermal performance, TI recommends using a high-K PCB with thermal vias between the ground plane and solder pad or thermal land pad; see [Figure 36](#) (a) and (b). Further, use a thicker ground plane and a thermal land pad with a larger surface area to improve considerably the heat-spreading capabilities of a PCB. For a two-layer PCB, a bat wing layout can enhance the heat-spreading capabilities.

## Layout Guidelines (continued)



(a) Multilayer PCB with a dedicated ground plane



(b) Dual layer PCB with Bat wings for enhanced heat spreading

**Figure 36. Using Multilayer PCB and Thermal Vias for Adequate Heat Dissipation**

Keeping other factors constant, surface area of the thermal land pad contributes to heat dissipation only to a certain extent.

## 10.2 Layout Example

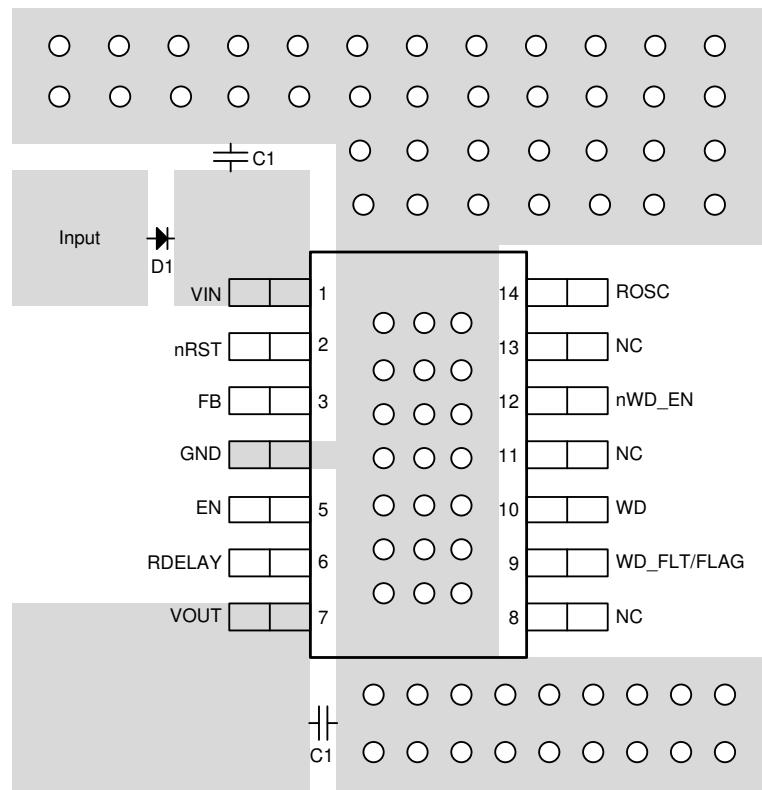


Figure 37. Layout Recommendation

## 11 器件和文档支持

### 11.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 5. 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
TPS7A63-Q1	<a href="#">单击此处</a>				
TPS7A6401-Q1	<a href="#">单击此处</a>				

### 11.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com.cn](http://ti.com.cn) 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 11.3 社区资源

[TI E2ETM support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 11.4 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 11.5 静电放电警告

 ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

 ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能导致器件与其发布的规格不相符。

### 11.6 Glossary

[SLYZ022 — TI Glossary](#).

This glossary lists and explains terms, acronyms, and definitions.

## 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

## 重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及ti.com.cn 上或随附TI 产品提供的其他可适用条款的约束。TI 提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122  
Copyright © 2020 德州仪器半导体技术（上海）有限公司

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A6301QPWPRQ1	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	7A6301	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TPS7A6333QDRKRQ1	ACTIVE	VSON	DRK	10	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	PRGQ	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TPS7A6333QPWPRQ1	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	7A6333	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TPS7A6350QPWPRQ1	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	7A6350	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TPS7A6401QPWPRQ1	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	7A6401	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



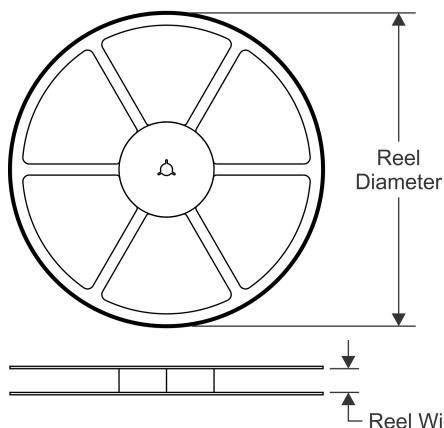
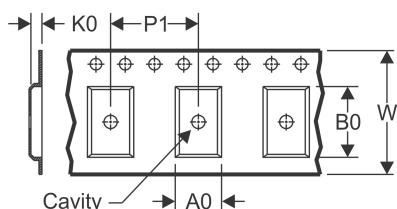
www.ti.com

## PACKAGE OPTION ADDENDUM

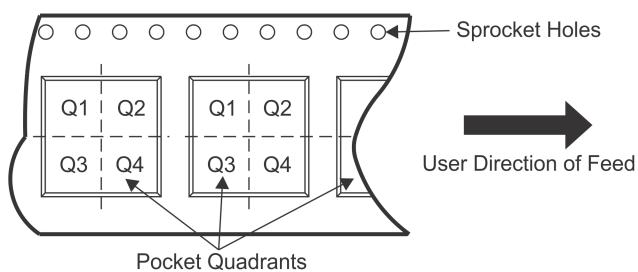
10-Dec-2020

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A6301QPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7A6333QDRKRQ1	VSON	DRK	10	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
TPS7A6333QPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7A6350QPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7A6401QPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

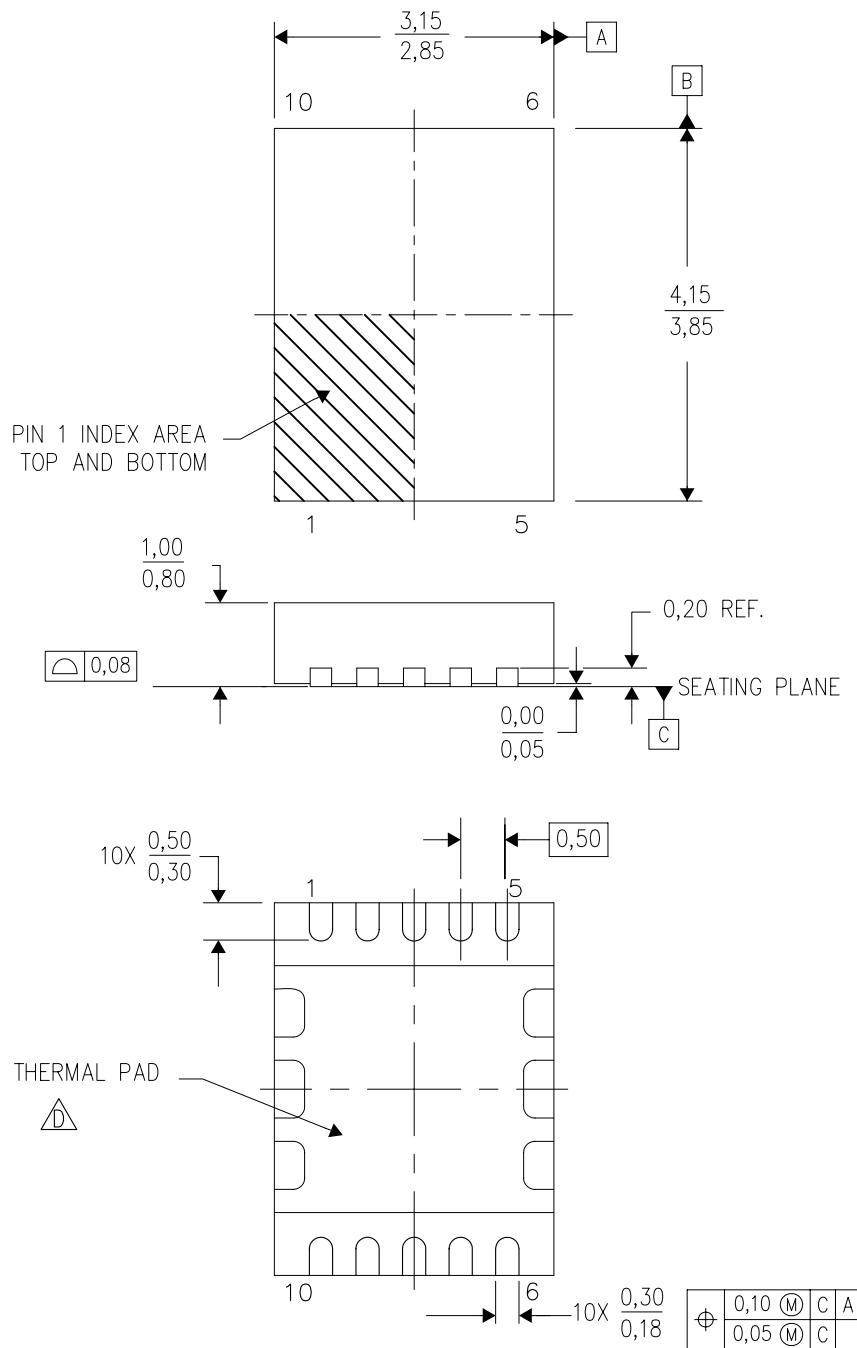

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A6301QPWPRQ1	HTSSOP	PWP	14	2000	350.0	350.0	43.0
TPS7A6333QDRKRQ1	VSON	DRK	10	3000	367.0	367.0	35.0
TPS7A6333QPWPRQ1	HTSSOP	PWP	14	2000	350.0	350.0	43.0
TPS7A6350QPWPRQ1	HTSSOP	PWP	14	2000	350.0	350.0	43.0
TPS7A6401QPWPRQ1	HTSSOP	PWP	14	2000	350.0	350.0	43.0

## MECHANICAL DATA

DRK (S-PVSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



4205621/D 02/11

NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No-Lead (SON) package configuration.

The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

# THERMAL PAD MECHANICAL DATA

DRK (S-PVSON-N10)

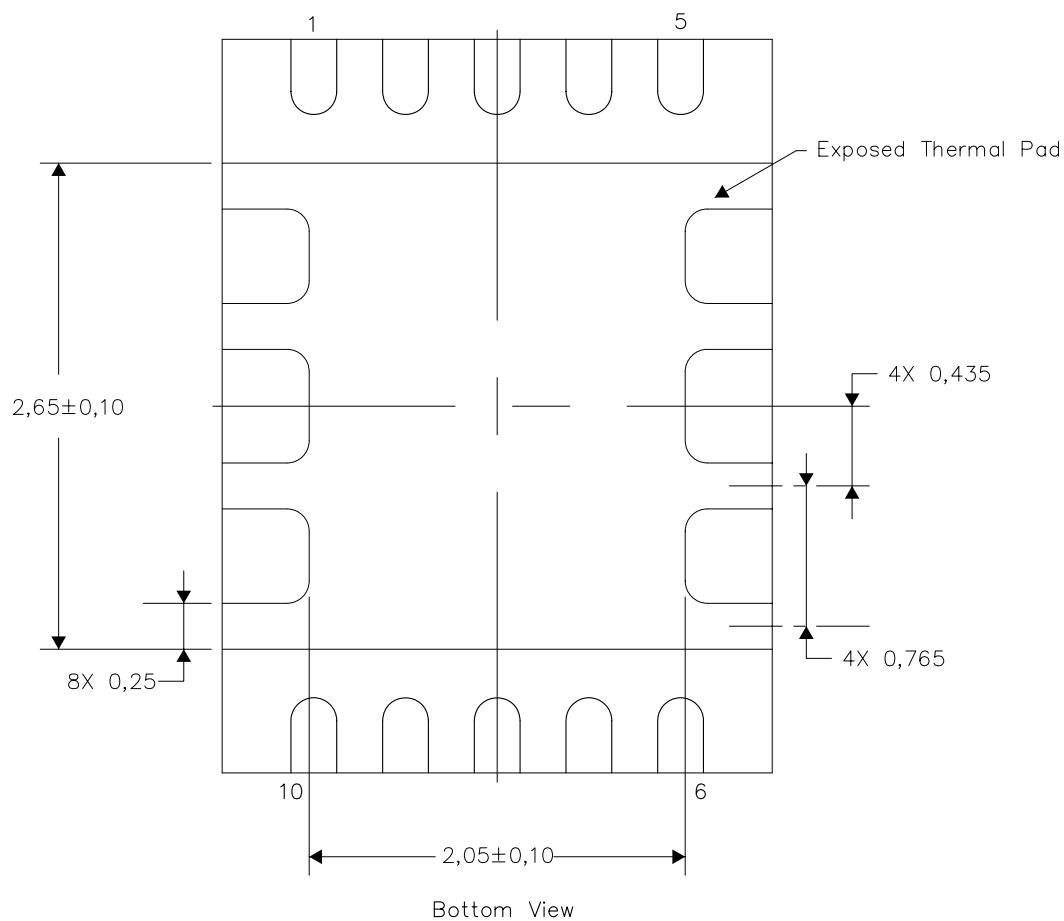
PLASTIC SMALL OUTLINE NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



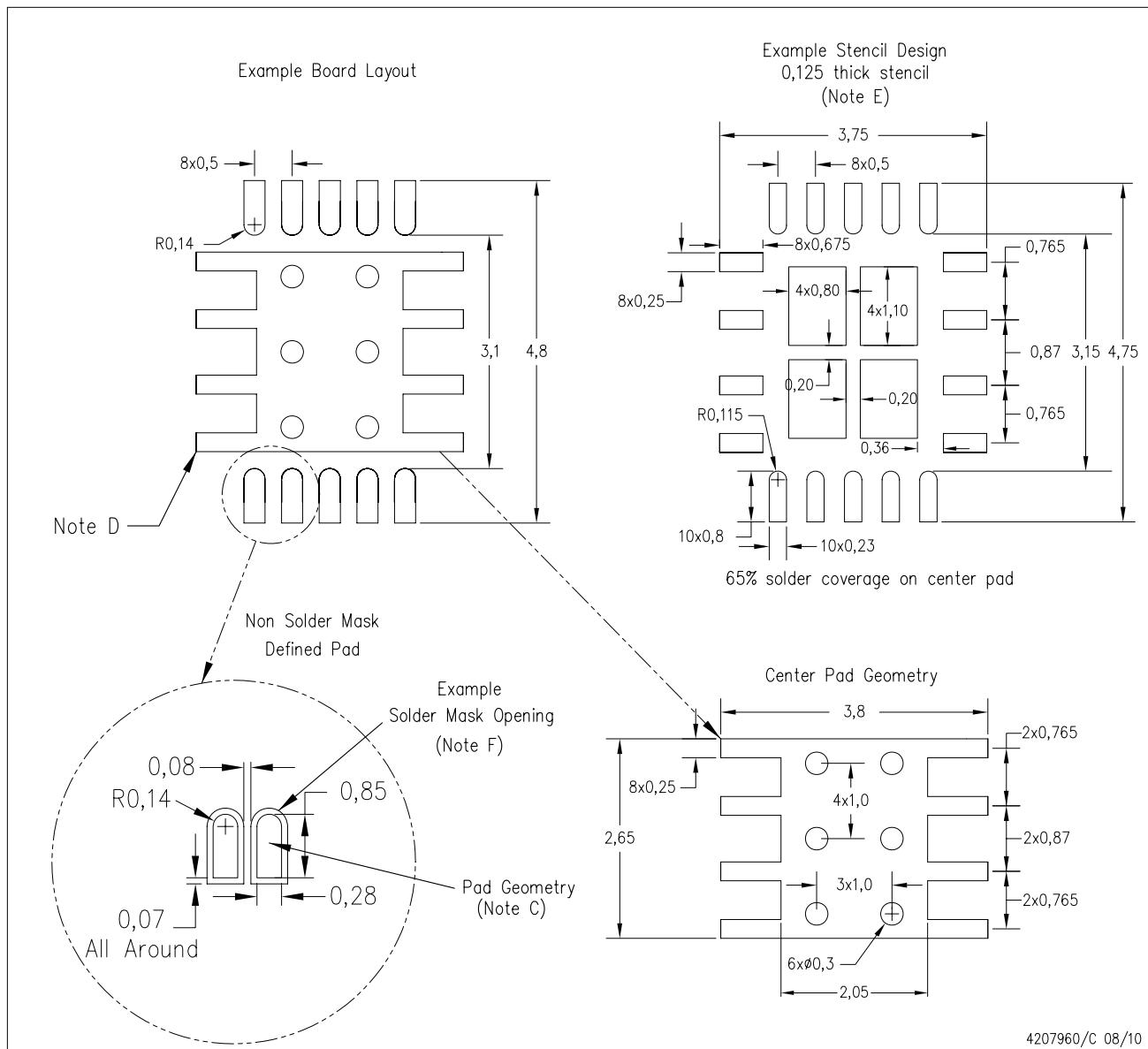
NOTE: A. All linear dimensions are in millimeters

4206317/F 08/10

# LAND PATTERN DATA

DRK (S-PVSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD

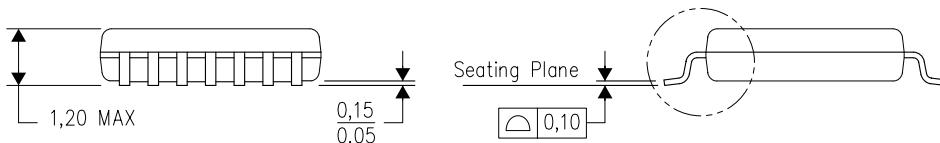
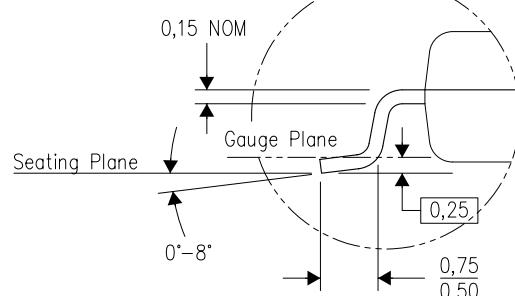
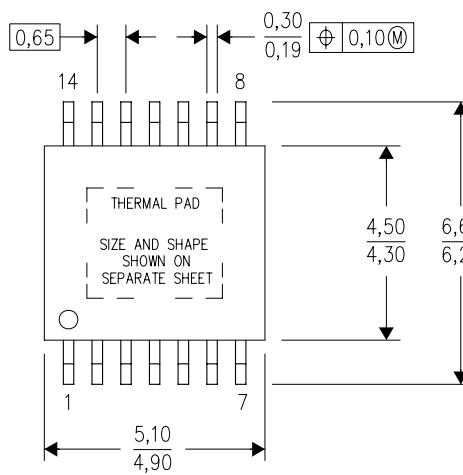


NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

PWP (R-PDSO-G14)

PowerPAD™ PLASTIC SMALL OUTLINE



4073225-2/1 05/11

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
- This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
- See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

# THERMAL PAD MECHANICAL DATA

PWP (R-PDSO-G14)

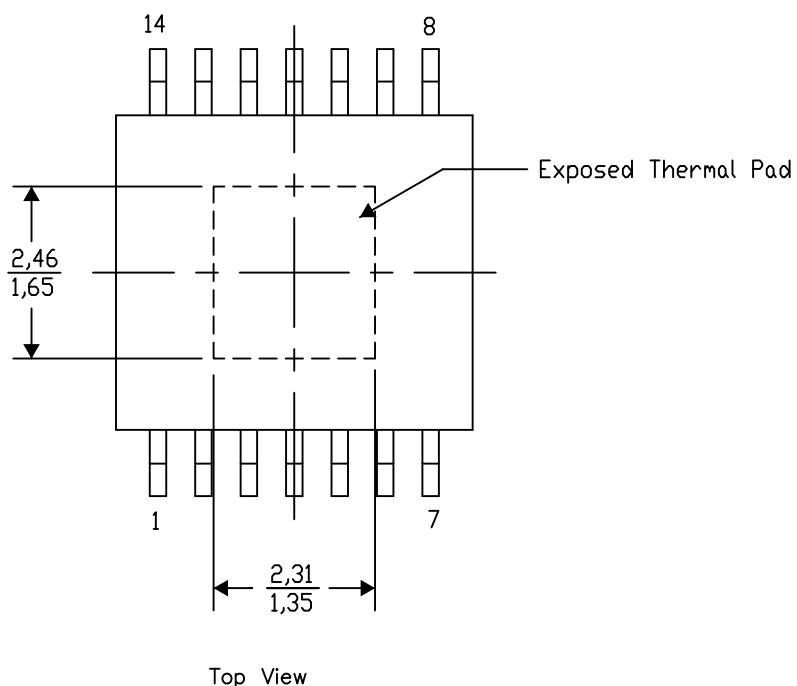
PowerPAD™ SMALL PLASTIC OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

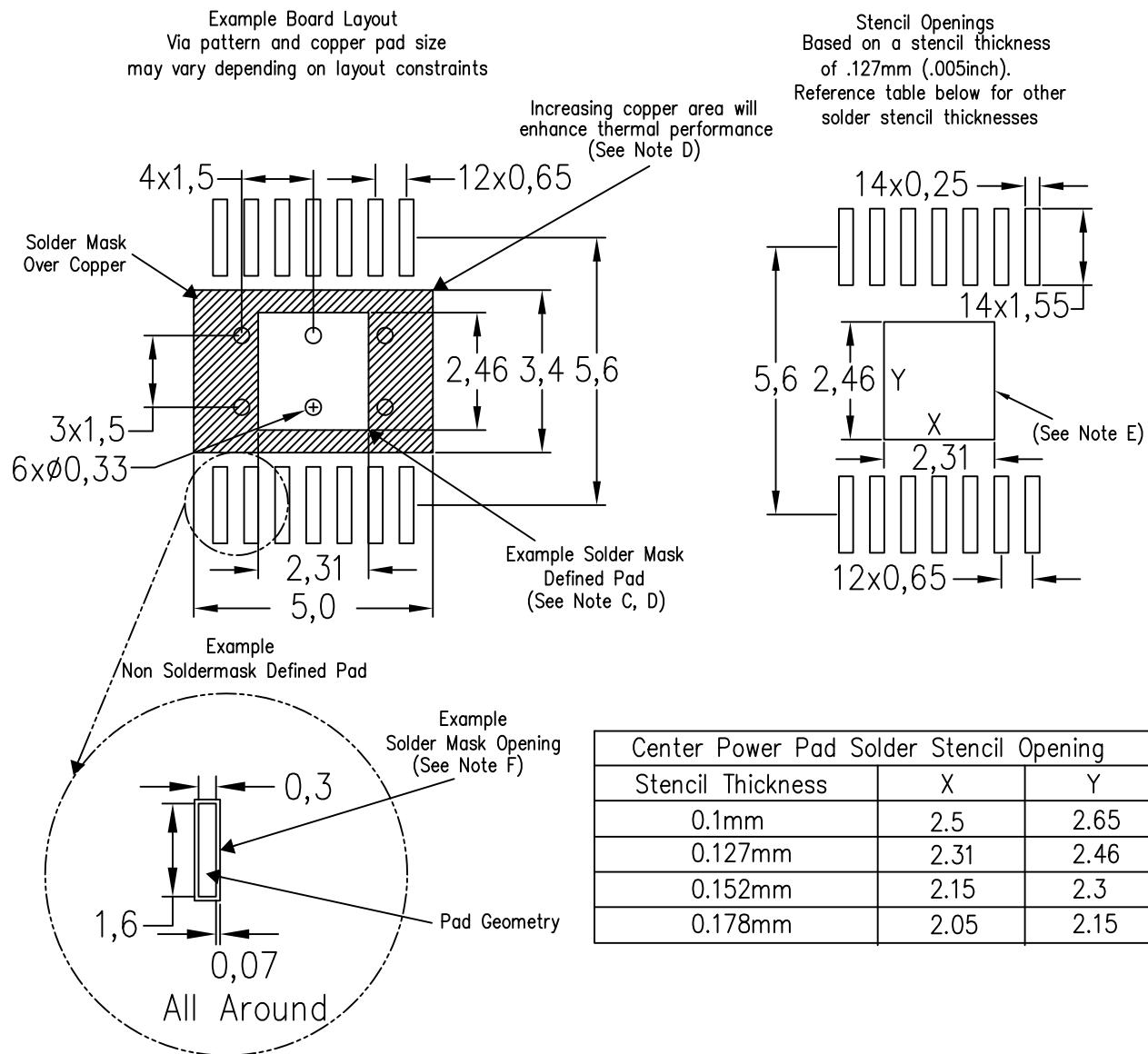
4206332-2/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

## PWP (R-PDSO-G14)

## PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# THERMAL PAD MECHANICAL DATA

PWP (R-PDSO-G14)

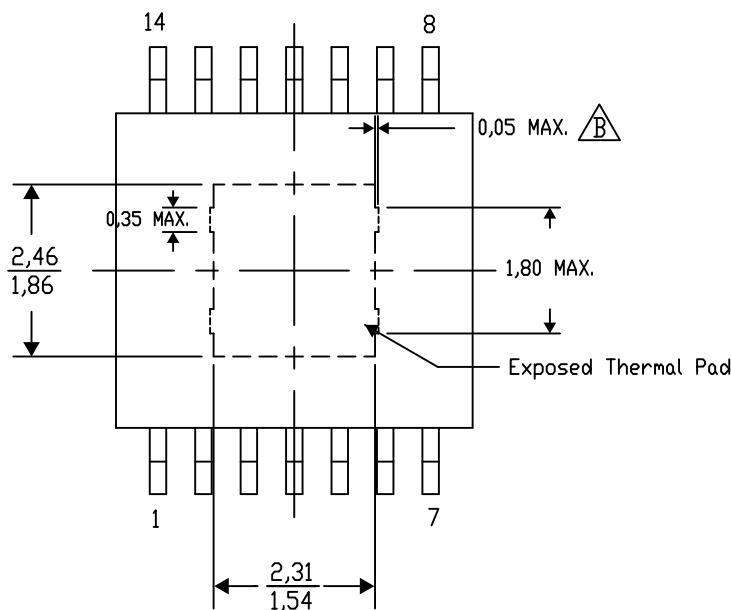
PowerPAD™ SMALL PLASTIC OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-44/AO 01/16

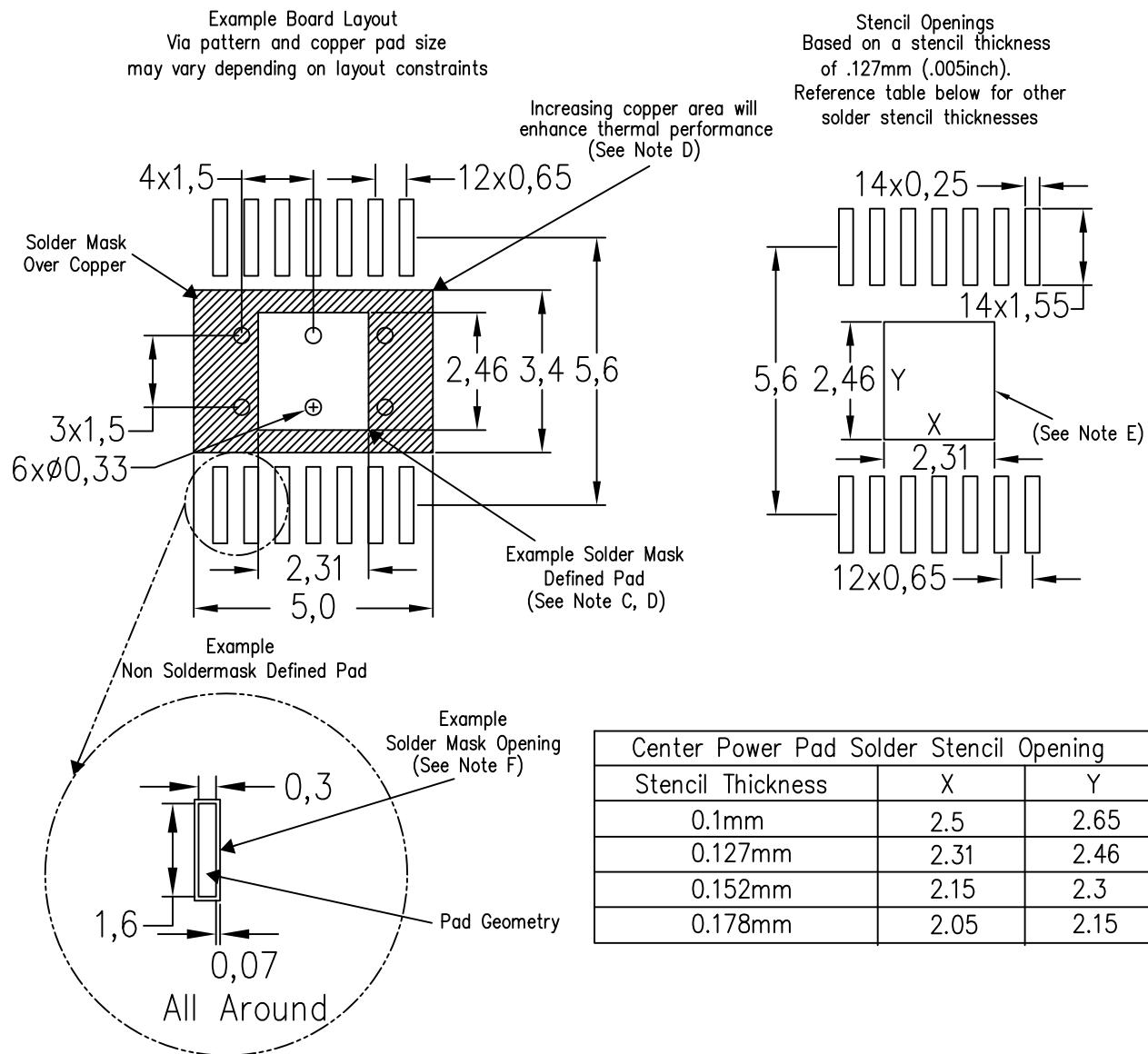
NOTE: A. All linear dimensions are in millimeters

 Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

## PWP (R-PDSO-G14)

## PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## 重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及ti.com.cn 上或随附TI 产品提供的其他可适用条款的约束。TI 提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122  
Copyright © 2020 德州仪器半导体技术（上海）有限公司