# TLV767-Q1 1A、16V 线性稳压器

## 1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 1：–40ºC 至 +125ºC，$T_A$
  - 结温范围：–40ºC 至 +150ºC，$T_J$
- 输入电压范围：2.5V 至 16V（最大值 18V）
- 输出电压范围：
  - 0.8V 至 14.6V（可调节）
  - 1.2V 至 12V（固定值，100mV 阶跃）
- 在整个负载和温度范围内的输出精度为 1%
- 低静态电流 ($I_Q$)：
  - 空载时典型值为 50µA
  - 禁用时最大值为 3µA
- 高 PSRR：1kHz 频率下为 70dB，1MHz 频率下为 46dB
- 内部软启动时间：500µs（典型值）
- 折返电流限制和热保护
- 与 1µF 或更大的电容器搭配使用时可保持稳定
- 封装：具有可湿性侧面的 8 引脚、3mm × 3mm WSON 封装
  - 低热阻 ($R_{\theta JA}$)：56.2°C/W

## 2 应用

- 直流/直流转换器
- 逆变器和电机控制
- 车载充电器 (OBC) 和无线充电器
- 汽车音响主机

## 3 说明

TLV767-Q1 是一款具有宽输入范围的线性稳压器，支持 2.5V 至 16V 的输入电压和高达 1A 的负载电流。输出范围为 0.8V 至 12V，在可调节版本中输出可高达 14.6V。

该器件具有宽输入电压范围，因此可由变压器次级绕组和 10V 或 12V 的稳压电源轨供电。此外，该器件还具有宽输出电压范围，不仅可为 SiC 栅极驱动器和麦克风产生偏置电压，还能为微控制器 (MCU) 和处理器供电。

TLV767-Q1 具有 1% 的输出精度，可为电源要求严格的数字负载供电。

内部软启动电路可减小启动期间的浪涌电流，从而降低输入电容。

高带宽 PSRR 性能在 1kHz 时大于 70dB，在 1MHz 时大于 46dB，因此有助于衰减上游直流/直流转换器的开关频率，并最大限度减少后置稳压器滤波。该器件具有 20Hz 至 20kHz 的高纹波抑制，是为音频组件供电的理想选择。

TLV767-Q1 采用具有可湿性侧面和低热阻的 8 引脚、3mm × 3mm VSON (DRB) 封装。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| TLV767-Q1 | VSON (8) | 3.00mm × 3.00mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

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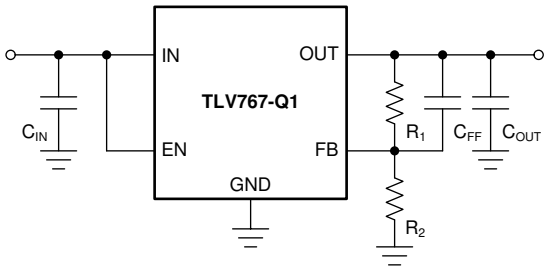
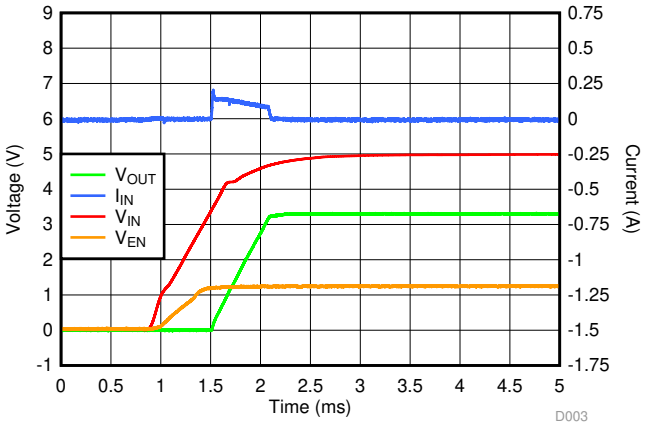
典型应用电路




$C_{OUT}$ 为 22µF 时减小的浪涌电流



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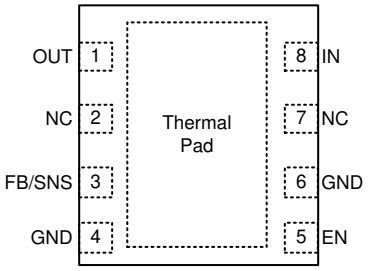
## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

| 日期 | 修订版本 | 说明 |
|---|---|---|
| 2020 年 4 月 | * | 初始发行版。 |

# 5 Pin Configuration and Functions

**DRB Package**
**8-Pin WSON**
**Top View**




**Pin Functions**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | DRB (Adjustable) | DRB (Fixed) | | |
| EN | 5 | 5 | Input | Enable pin. Driving the enable pin high enables the device. Driving this pin low disables the device. High and low thresholds are listed in the *Electrical Characteristics* table. This pin has an internal pullup resistor and can be left floating to enable the device or the pin can be connected to the input pin. |
| FB | 3 | — | Input | Feedback pin. Input to the control-loop error amplifier. This pin is used to set the output voltage of the device with the use of external resistors. Do not float this pin. For adjustable-voltage version devices only. |
| GND | 4, 6 | 4, 6 | — | Ground pin. All ground pins must be grounded. |
| NC | 2, 7 | 2, 7 | — | NC pin. Not internally connected. This pin can be either floated or connected to GND for best thermal performance. |
| IN | 8 | 8 | Input | Input pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the IN and GND pins of the device as possible. |
| OUT | 1 | 1 | Output | Output pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the OUT and GND pins of the device as possible. |
| SNS | — | 3 | Input | Output sense pin. Connect the SNS pin to the OUT pin, or to remotely sense the output voltage at the load, connect the SNS pin to the load. Do not float this pin. For fixed-voltage version devices only. |
| Thermal pad | | | — | Exposed pad of the package. Connect this pad to ground or leave floating. Connect the thermal pad to a large-area ground plane for best thermal performance. |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage(2) | Input voltage, $V_{IN}$ | –0.3 | 18 | V |
| | Output voltage, $V_{OUT}$(3) | –0.3 | $V_{IN}$ + 0.3 | |
| | Sense pin voltage, $V_{SNS}$(3) | –0.3 | $V_{IN}$ + 0.3 | |
| | Feedback voltage, $V_{FB}$ | –0.3 | 3 | |
| | Enable voltage, $V_{EN}$ | –0.3 | 18 | |
| Current | Maximum output current | Internally limited | | A |
| Temperature | Operating junction ($T_J$) | –50 | 150 | °C |
| | Storage ($T_{stg}$) | –65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.
(3) $V_{IN}$ + 0.3 V or 18 V (whichever is smaller).

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | 2.5 | | 16 | V |
| $V_{EN}$ | Enable voltage | 0 | | 16 | V |
| $V_{OUT}$ | Output voltage | 0.8 | | 14.6 | V |
| $I_{OUT}$ | Output current (2.5 V ≤ $V_{IN}$ < 3 V) | 0 | | 0.8 | A |
| $I_{OUT}$ | Output current ($V_{IN}$ ≥ 3 V) | 0 | | 1 | A |
| $C_{OUT}$ | Output capacitor(1) | 1 | 2.2 | 220 | µF |
| $C_{OUT}$ ESR | Output capacitor ESR | 2 | | 500 | mΩ |
| $C_{IN}$ | Input capacitor | | 1 | | µF |
| $C_{FF}$ | Feed-forward capacitor (optional(2), for adjustable device only) | | 10 | | pF |
| $I_{FB\_DIVIDER}$ | Feedback divider current(2) | 5 | | | µA |
| $T_J$ | Junction temperature | –40 | | 125 | °C |

(1) Effective output capacitance of 0.5 µF minimum required for stability.
(2) $C_{FF}$ required for stability if the feedback divider current < 5 µA. Feedback divider current = $V_{OUT}$ / ($R_1$ + $R_2$). See *Feed-Forward Capacitor ($C_{FF}$)* section for details.

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## 6.4 Thermal Information

| THERMAL METRIC(1) | | TLV767-Q1 DRB (WSON) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 56.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 68.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 28.9 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 3.8 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 28.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 12.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics

specified at $T_J$ = –40°C to 125°C, $V_{IN}$ = $V_{OUT(nom)}$ + 1.5 V or $V_{IN}$ = 2.5 V (whichever is greater), FB/SNS tied to OUT, $I_{OUT}$ = 10 mA, $V_{EN}$ = 2 V, $C_{IN}$ = 1.0 µF, $C_{OUT}$ = 1.0 µF (unless otherwise noted); typical values are at $T_J$ = 25ºC

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OUT}$ | Nominal output accuracy | $T_J$ = 25°C | –0.5 | | 0.5 | % |
| $V_{OUT}$ | Output accuracy over temperature | $V_{IN}$ ≥ 3.0 V, 1 mA ≤ $I_{OUT}$ ≤ 1 A | –1 | | 1 | % |
| | | 2.5 V ≤ $V_{IN}$ < 3.0 V, 1 mA ≤ $I_{OUT}$ ≤ 800 mA | –1 | | 1 | |
| $V_{FB}$ | Feedback voltage | | | 0.8 | | V |
| $V_{REF}$ | Internal reference (adjustable device) | $T_J$ = 25ºC | –0.5 | | 0.5 | % |
| | | | –1 | | 1 | |
| $I_{FB}$ | Feedback pin current | $V_{FB}$ = 1 V | | 10 | 50 | nA |
| $\Delta V_{OUT(\Delta VIN)}$ | Line regulation(1) | $V_{OUT(NOM)}$ +1.5 V ≤ $V_{IN}$ ≤ 16 V, $I_{OUT}$ = 10 mA | | | 0.02 | %/V |
| $\Delta V_{OUT(\Delta IOUT)}$ | Load regulation | 1 mA ≤ $I_{OUT}$ ≤ 1 A, $V_{IN}$ ≥ 3.0 V | | 0.1 | 0.5 | %/A |
| | | 1 mA ≤ $I_{OUT}$ ≤ 800 mA, 2.5 V ≤ $V_{IN}$ < 3.0 V | | 0.1 | 0.5 | |
| $V_{DO}$ | Dropout voltage(2) | $V_{IN}$ ≥ 3.0V, $I_{OUT}$ = 1 A | | 0.9 | 1.4 | V |
| | | 2.5 V ≤ $V_{IN}$ < 3.0 V, $I_{OUT}$ = 800 mA | | 0.8 | 1.3 | |
| $I_{CL}$ | Output current limit | $V_{OUT}$ = 0.9 x $V_{OUT(NOM)}$, $V_{IN}$ ≥ 3.0 V | 1.1 | | 1.6 | A |
| | | $V_{OUT}$ = 0.9 x $V_{OUT(NOM)}$, 2.5 V ≤ $V_{IN}$ < 3.0 V | 0.81 | | 1.6 | |
| $I_{SC}$ | Short-circuit current limit | $V_{OUT}$ = 0 V | 150 | 250 | 350 | mA |
| $I_Q$ | Quiescent current | $I_{OUT}$ = 0 mA | | 50 | 80 | µA |
| $I_Q$ | Quiescent current (fixed output device) | $I_{OUT}$ = 0 mA | | 60 | 95 | µA |
| $I_{GND}$ | Ground current | $I_{OUT}$ = 1 A, $V_{IN}$ ≥ 3.0 V | | 1.5 | | mA |
| $I_{SHUTDOWN}$ | Shutdown current | $V_{EN}$ ≤ 0.4 V, $V_{IN}$ = 16 V | | 1.5 | 3 | µA |
| $V_{EN(HIGH)}$ | Enable pin logic high | 2.5 V ≤ $V_{IN}$ ≤ 16 V | 1.2 | | | V |
| $V_{EN(LOW)}$ | Enable pin logic low | 2.5 V ≤ $V_{IN}$ ≤ 16 V | | | 0.4 | V |
| $I_{EN}$ | Enable pullup current | $V_{EN}$ = 0 V | | 400 | | nA |
| $I_{PULLDOWN}$ | Output pulldown current | $V_{IN}$ = 16 V, $V_{OUT}$ = 2.5 V | | 1.2 | | mA |
| PSRR | Power-supply rejection ratio | $V_{IN}$ = 3.3 V, $V_{OUT}$ = 1.8 V, $I_{OUT}$ = 300 mA, f = 120 Hz | | 70 | | dB |
| $V_n$ | Output noise voltage | BW = 10 Hz to 100 KHz, $V_{IN}$ = 3.3 V, $V_{OUT}$ = 0.8 V, $I_{OUT}$ = 100 mA | | 60 | | $\mu V_{RMS}$ |
| $V_{UVLO+}$ | UVLO threshold rising | $V_{IN}$ rising | | 2.2 | 2.4 | V |

(1) Line regulation is measured with $V_{IN}$ = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater).
(2) $V_{DO}$ is measured with $V_{IN}$ = 95% x $V_{OUT(nom)}$ for fixed output devices. $V_{DO}$ is not measured for fixed output devices when $V_{OUT}$ < 2.5 V. For adjustable output device, $V_{DO}$ is measured with $V_{FB}$ = 95% x $V_{FB(nom)}$.

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## Electrical Characteristics (continued)

specified at $T_J$ = –40°C to 125°C, $V_{IN}$ = $V_{OUT(nom)}$ + 1.5 V or $V_{IN}$ = 2.5 V (whichever is greater), FB/SNS tied to OUT, $I_{OUT}$ = 10 mA, $V_{EN}$ = 2 V, $C_{IN}$ = 1.0 µF, $C_{OUT}$ = 1.0 µF (unless otherwise noted); typical values are at $T_J$ = 25ºC

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{UVLO(HYS)}$ | UVLO hysteresis | | | 130 | | mV |
| $V_{UVLO-}$ | UVLO threshold falling | $V_{IN}$ falling | 1.9 | | | V |
| $T_{SD(shutdown)}$ | Thermal shutdown temperature | Temperature increasing | | 180 | | ºC |
| $T_{SD(reset)}$ | Thermal shutdown reset temperature | Temperature falling | | 160 | | |

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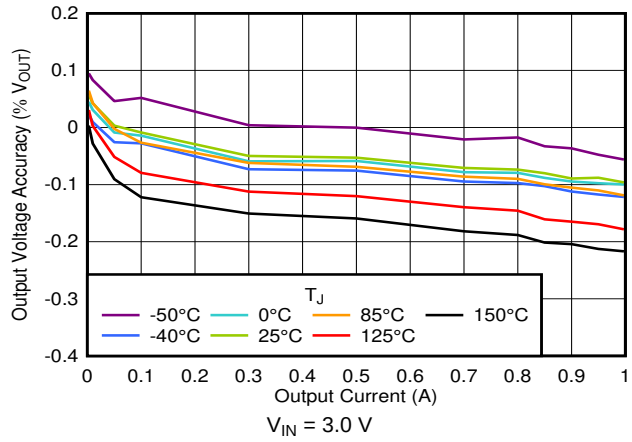
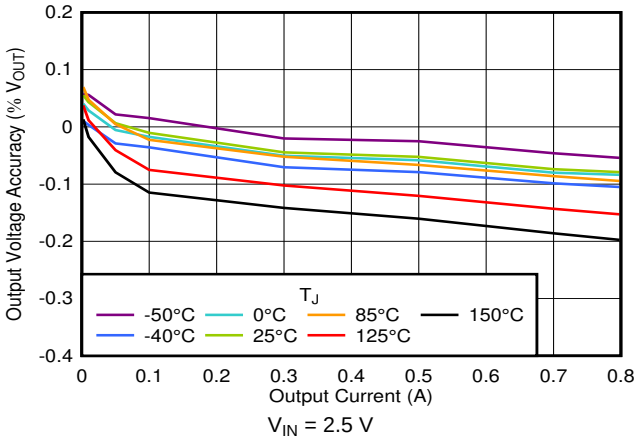
## 6.6 Typical Characteristics

at operating temperature $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), $I_{OUT}$ = 10 mA, $V_{EN}$ = 2.0 V, $C_{IN}$ = 1.0 µF, and $C_{OUT}$ = 1.0 µF (unless otherwise noted)



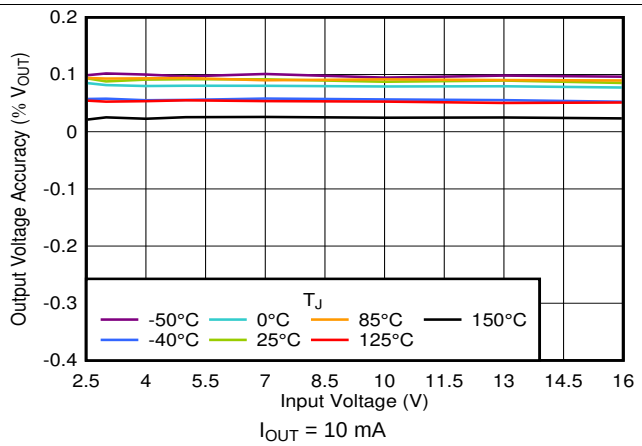

$V_{IN}$ = 3.0 V

**图 1. $V_{OUT}$ Accuracy vs $I_{OUT}$**




$V_{IN}$ = 2.5 V

**图 2. $V_{OUT}$ Accuracy vs $I_{OUT}$**




$I_{OUT}$ = 10 mA

**图 3. $V_{OUT}$ Accuracy vs $V_{IN}$**

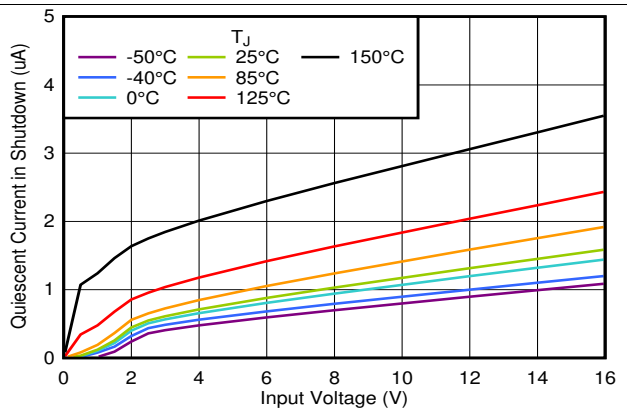
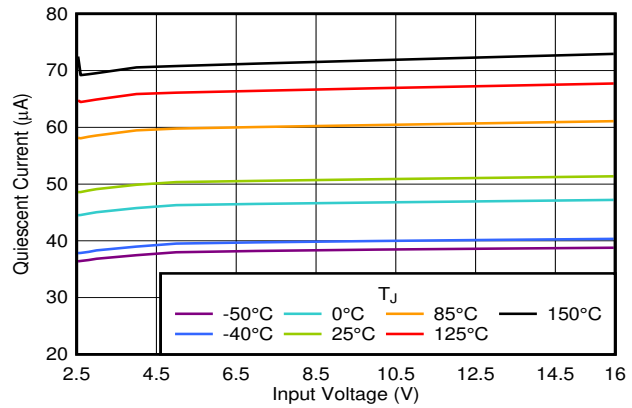
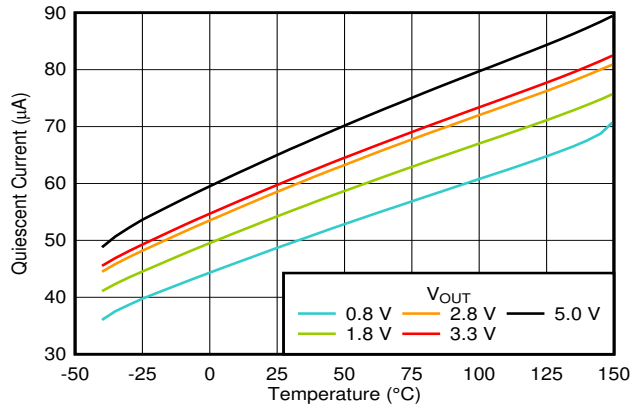



**图 4. $I_{SHUTDOWN}$ vs $V_{IN}$**




$I_{OUT}$ = 0 mA, adjustable-voltage version devices

**图 5. $I_Q$ vs $V_{IN}$**




$I_{OUT}$ = 0 mA, fixed-voltage version devices

**图 6. $I_Q$ vs Temperature**

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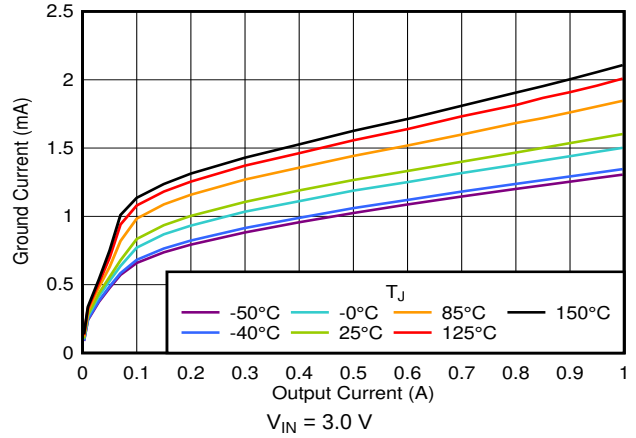
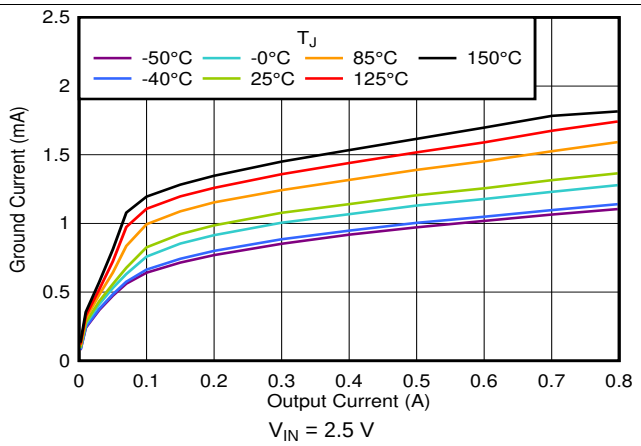
## Typical Characteristics (接下页)

at operating temperature $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), $I_{OUT}$ = 10 mA, $V_{EN}$ = 2.0 V, $C_{IN}$ = 1.0 µF, and $C_{OUT}$ = 1.0 µF (unless otherwise noted)



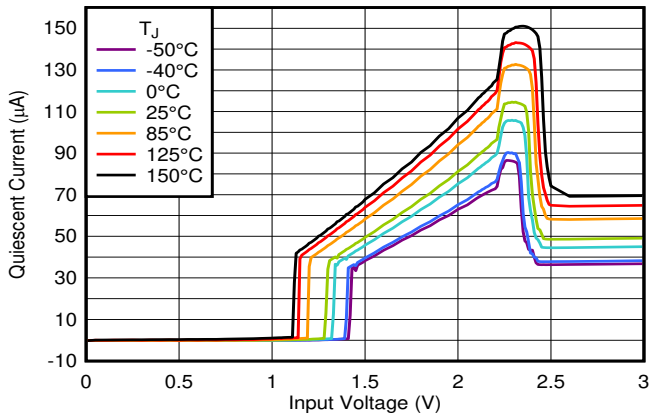

$V_{IN}$ = 3.0 V

**图 7. $I_{GND}$ vs $I_{OUT}$**



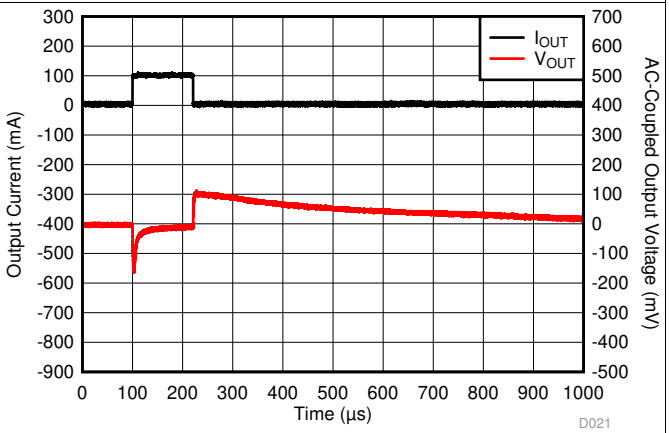

$V_{IN}$ = 2.5 V

**图 8. $I_{GND}$ vs $I_{OUT}$**



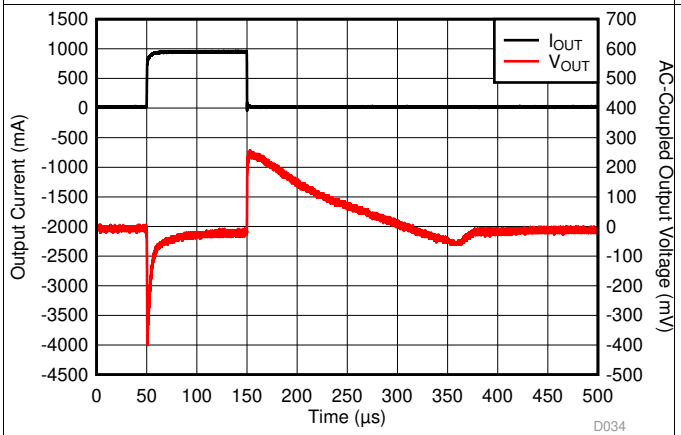

$I_{OUT}$ = 0 mA

**图 9. $I_Q$ Increase Below Minimum $V_{IN}$**



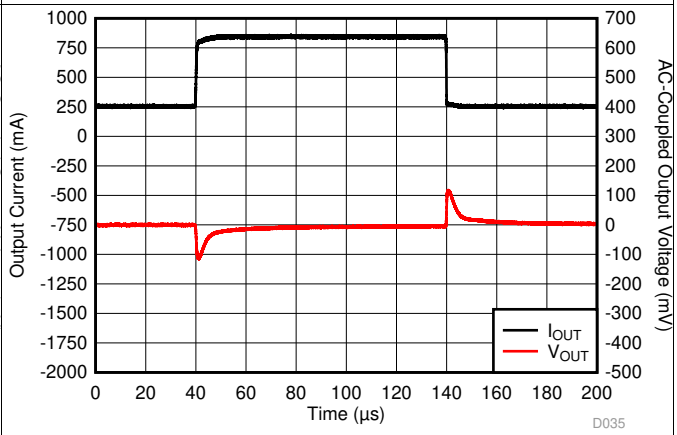

$V_{IN}$ = 5 V, $V_{OUT}$ = 3.3 V, $C_{FF}$ = 10 pF, ramp rate = 0.4 A/µs

**图 10. $I_{OUT}$ Transient From 0 mA to 100 mA**




$V_{IN}$ = 5 V, $V_{OUT}$ = 3.3 V, $C_{FF}$ = 10 pF, ramp rate = 0.5 A/µs

**图 11. $I_{OUT}$ Transient From 1 mA to 1 A**




$V_{IN}$ = 5 V, $V_{OUT}$ = 3.3 V, ramp rate = 0.8 A/µs

**图 12. $I_{OUT}$ Transient From 250 mA to 850 mA**

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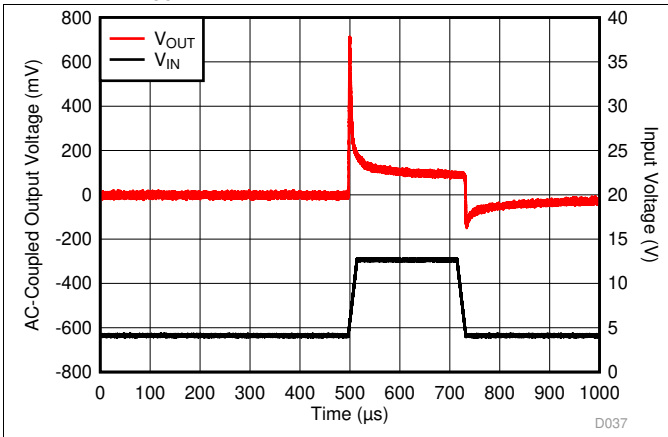
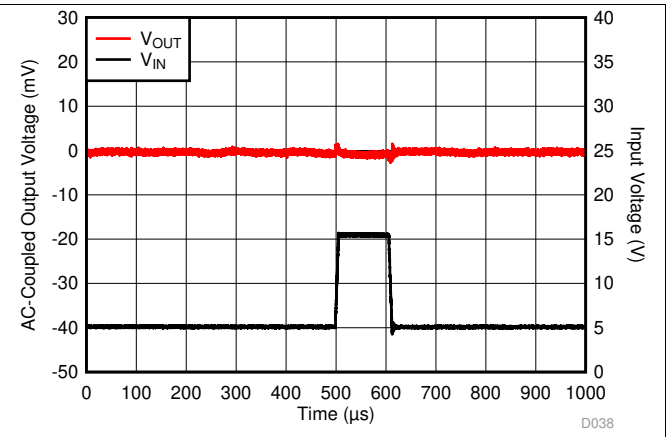
## Typical Characteristics (接下页)

at operating temperature $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), $I_{OUT}$ = 10 mA, $V_{EN}$ = 2.0 V, $C_{IN}$ = 1.0 µF, and $C_{OUT}$ = 1.0 µF (unless otherwise noted)



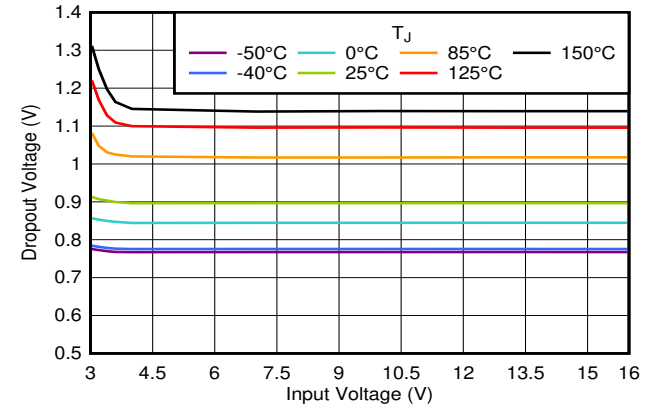

$V_{OUT}$ = 3.3 V, $I_{OUT}$ = 1 A, $V_{IN}$ ramp rate = 0.6 V/µs

**图 13. $V_{IN}$ Transient in Dropout From 4 V to 13 V**



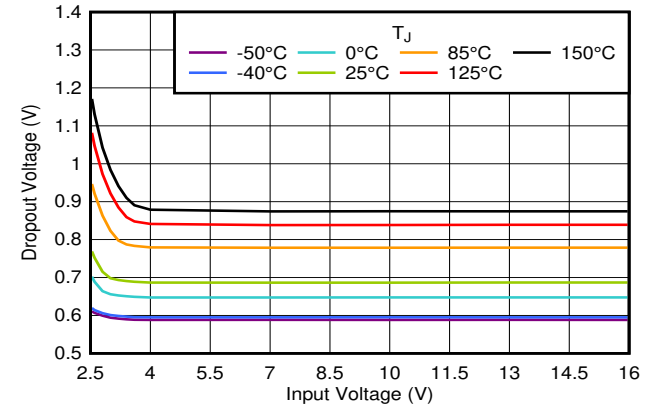

$V_{OUT}$ = 3.3 V, $I_{OUT}$ = 33 µA, $V_{IN}$ ramp rate = 1.6 V/µs

**图 14. $V_{IN}$ Transient From 5 V to 16 V**



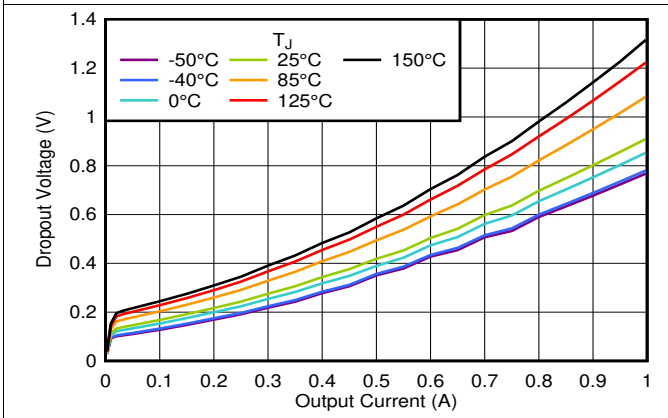

$I_{OUT}$ = 1.0 A

**图 15. $V_{DO}$ vs $V_{IN}$**



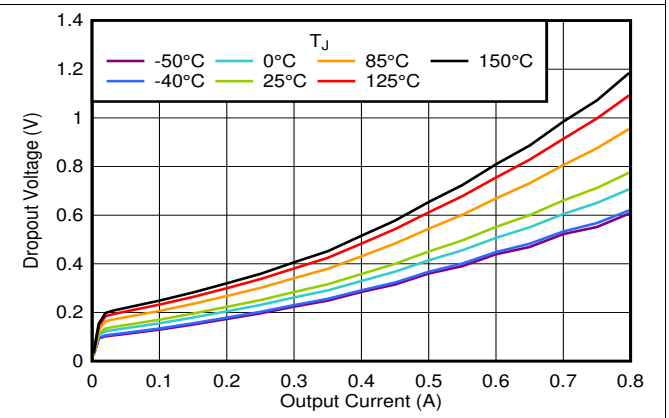

$I_{OUT}$ = 0.8 A

**图 16. $V_{DO}$ vs $V_{IN}$**




$V_{IN}$ = 3.0 V

**图 17. $V_{DO}$ vs $I_{OUT}$**




$V_{IN}$ = 2.5 V

**图 18. $V_{DO}$ vs $I_{OUT}$**

ADVANCE INFORMATION

## Typical Characteristics (接下页)

at operating temperature $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), $I_{OUT}$ = 10 mA, $V_{EN}$ = 2.0 V, $C_{IN}$ = 1.0 µF, and $C_{OUT}$ = 1.0 µF (unless otherwise noted)

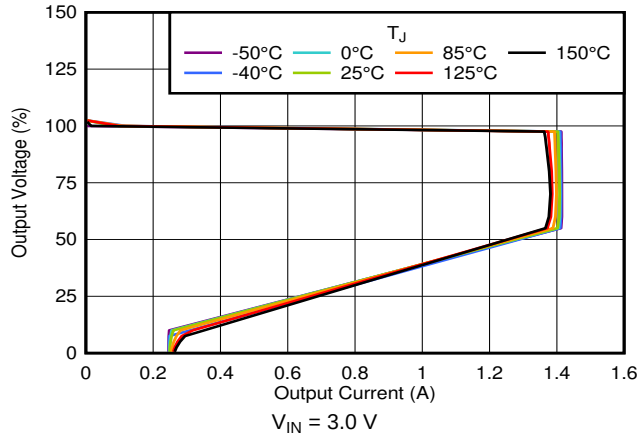



图 19. Foldback Current Limit vs $I_{OUT}$ and Temperature

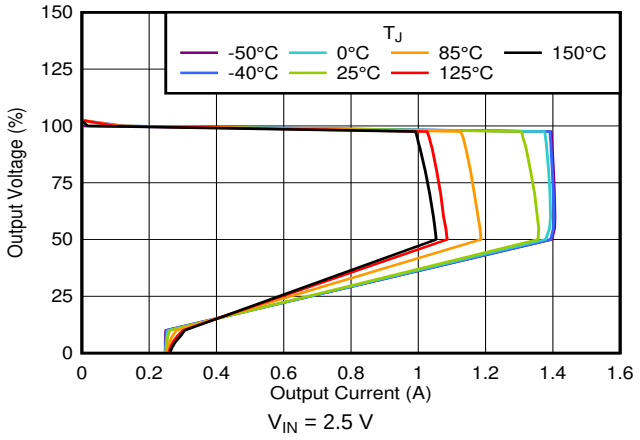



图 20. Foldback Current Limit vs $I_{OUT}$ and Temperature

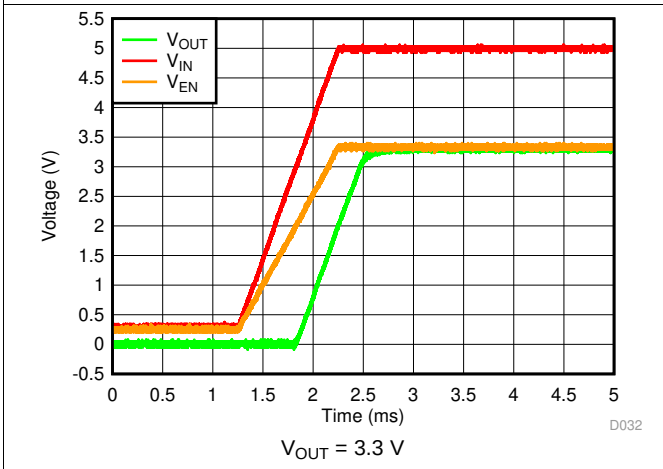



图 21. Startup With Separate $V_{EN}$ and $V_{IN}$

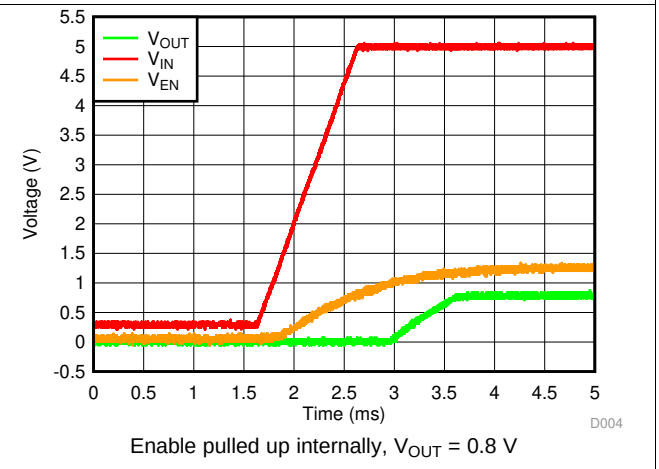



图 22. Startup With $V_{EN}$ Floating

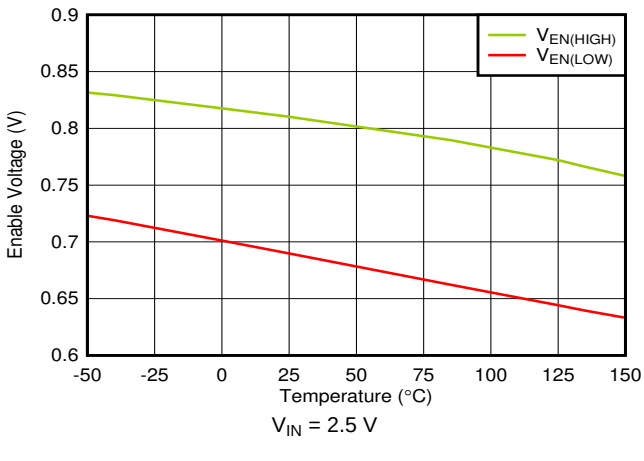



图 23. $V_{EN}$ Thresholds vs Temperature

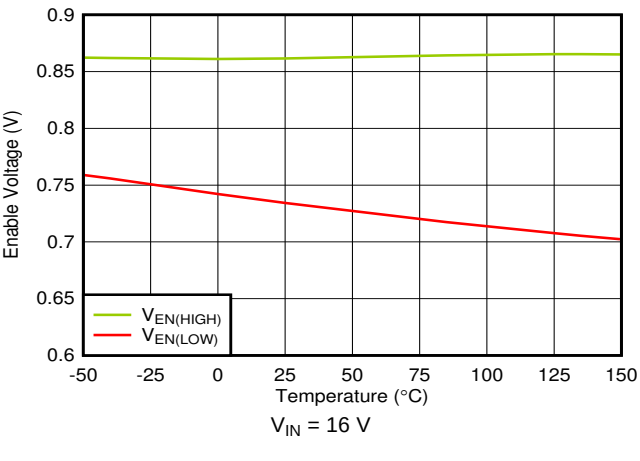



图 24. $V_{EN}$ Thresholds vs Temperature

ADVANCE INFORMATION

## Typical Characteristics (接下页)

at operating temperature $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), $I_{OUT}$ = 10 mA, $V_{EN}$ = 2.0 V, $C_{IN}$ = 1.0 µF, and $C_{OUT}$ = 1.0 µF (unless otherwise noted)

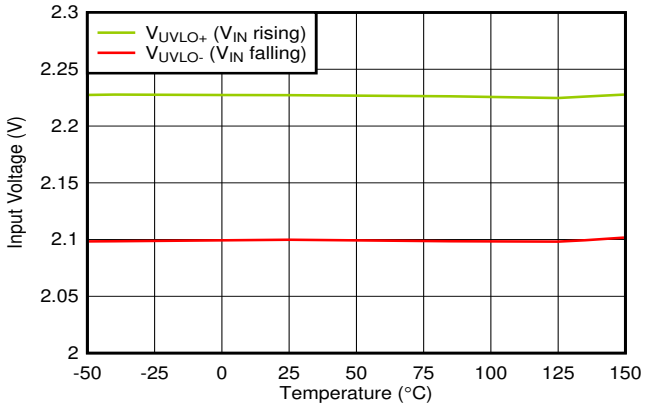
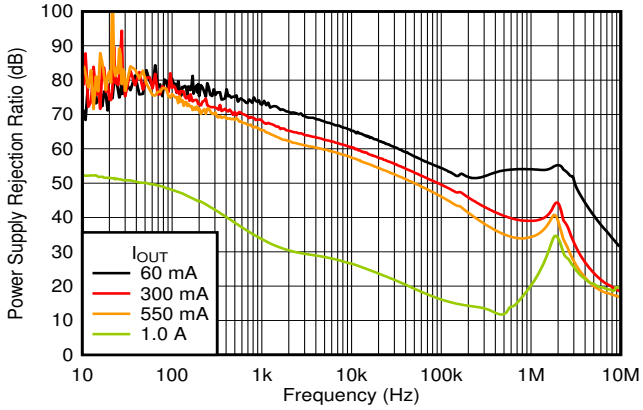
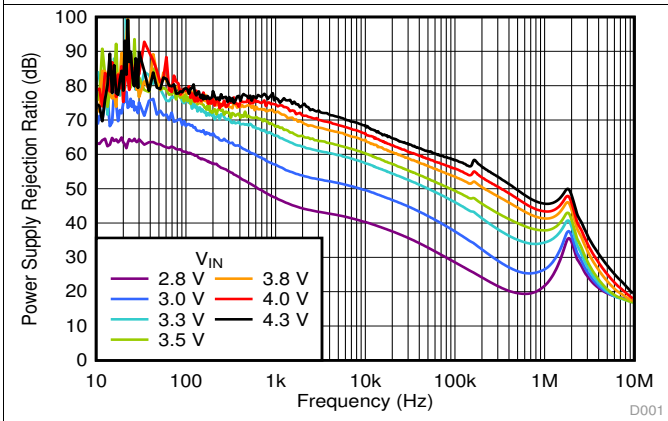



图 25. UVLO Thresholds vs Temperature



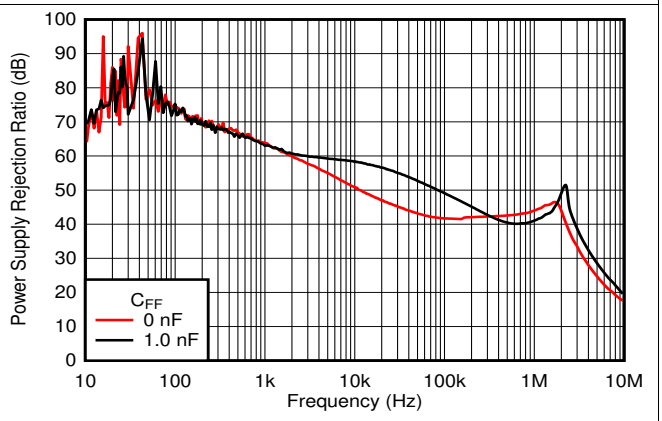

$V_{OUT}$ = 1.8 V, $V_{IN}$ = 3.3 V, $C_{FF}$ = 1 nF

图 26. PSRR vs Frequency and $I_{OUT}$



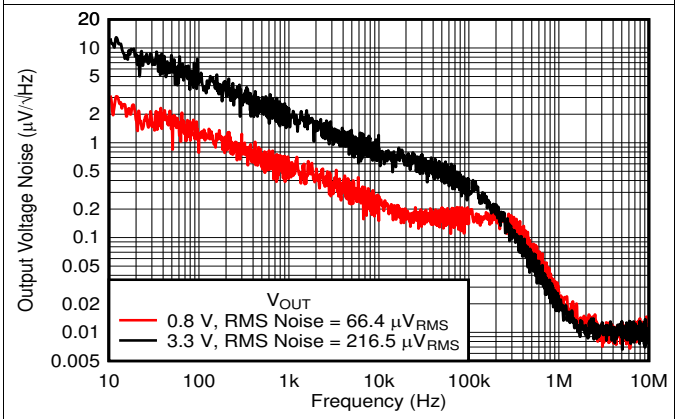

$V_{OUT}$ = 1.8 V, $I_{OUT}$ = 0.55 A, $C_{FF}$ = 1 nF

图 27. PSRR vs Frequency and $V_{IN}$



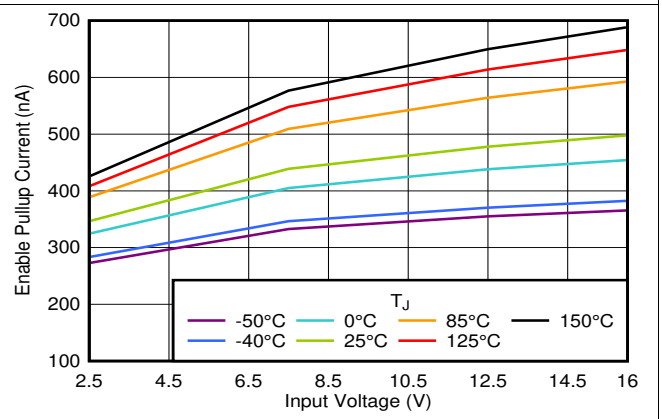

$V_{OUT}$ = 3.3 V, $V_{IN}$ = 4.8 V, $I_{OUT}$ = 0.33 A

图 28. PSRR vs Frequency and $C_{FF}$




$C_{FF}$ = 0 nF, $I_{OUT}$ = 0.1 A, RMS noise BW = 10 Hz to 100 kHz

图 29. Output Noise ($V_n$) vs Frequency and $V_{OUT}$




$V_{EN}$ = 0 V

图 30. $I_{EN}$ vs $V_{IN}$

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## Typical Characteristics (接下页)

at operating temperature $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), $I_{OUT}$ = 10 mA, $V_{EN}$ = 2.0 V, $C_{IN}$ = 1.0 µF, and $C_{OUT}$ = 1.0 µF (unless otherwise noted)

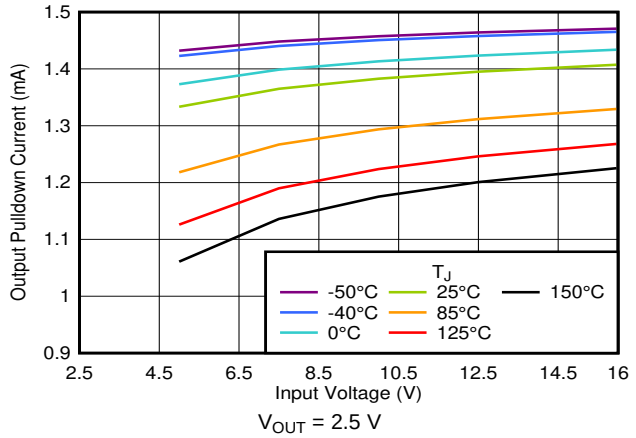


图 31. $I_{PULLDOWN}$ vs $V_{IN}$

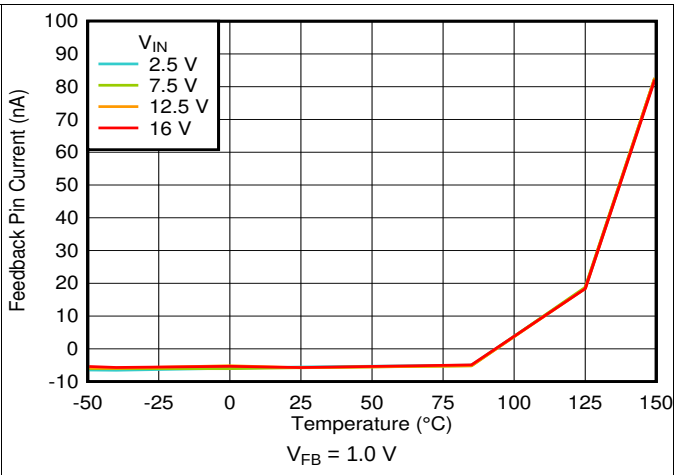


图 32. $I_{FB}$ vs Temperature

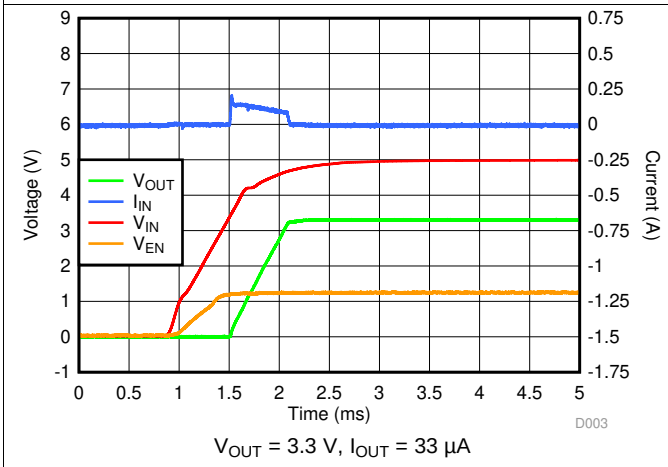


图 33. Startup Inrush Current With $C_{OUT}$ = 22 µF

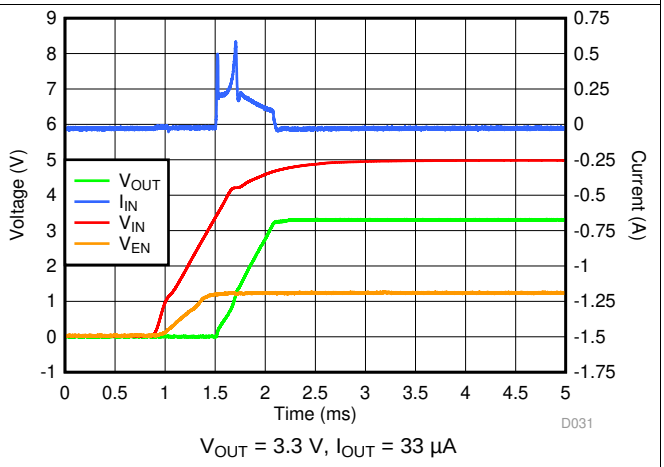


图 34. Startup Inrush Current With $C_{OUT}$ = 47 µF

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# 7 Detailed Description

## 7.1 Overview

The TLV767-Q1 is a low quiescent current, high PSRR linear regulator capable of handling up to 1 A of load current. Unlike typical high current linear regulators, the TLV767-Q1 consumes significantly less quiescent current. This device is ideal for high current applications that require very sensitive power-supply rails.

This device features an integrated foldback current limit, thermal shutdown, output enable, internal output pulldown, and undervoltage lockout (UVLO). This device delivers excellent line and load transient performance. This device is low noise and exhibits very good PSRR. The operating ambient temperature range of the device is –40°C to +125°C.

## 7.2 Functional Block Diagrams

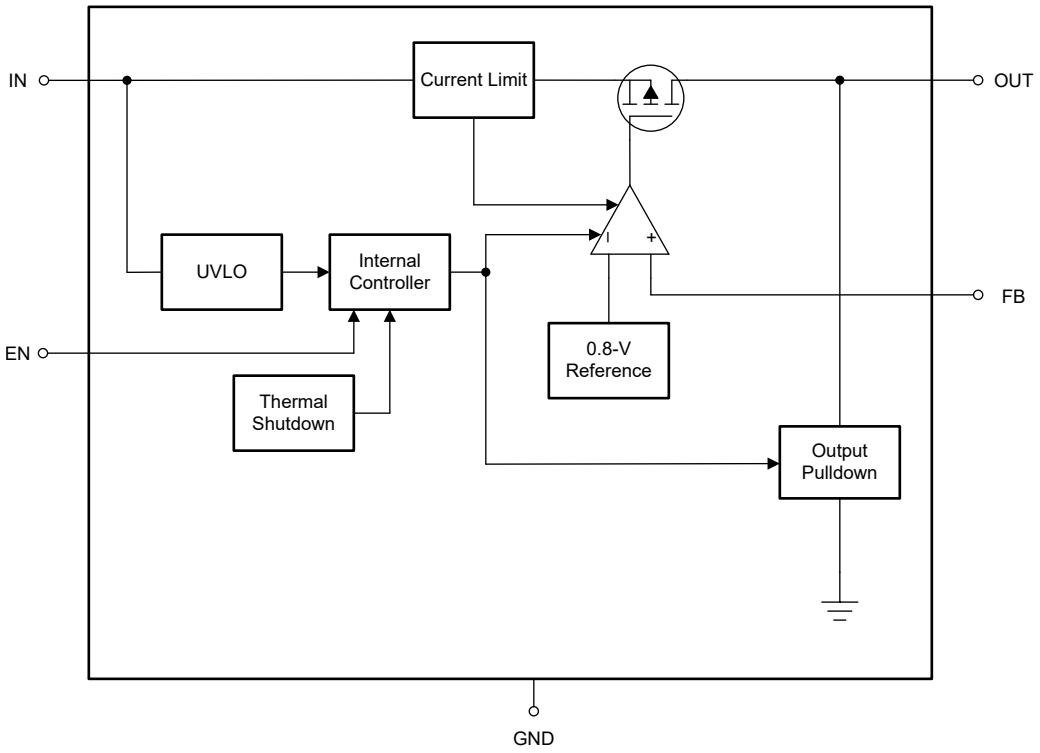


**图 35. Adjustable-Version Block Diagram**

## Functional Block Diagrams (continued)

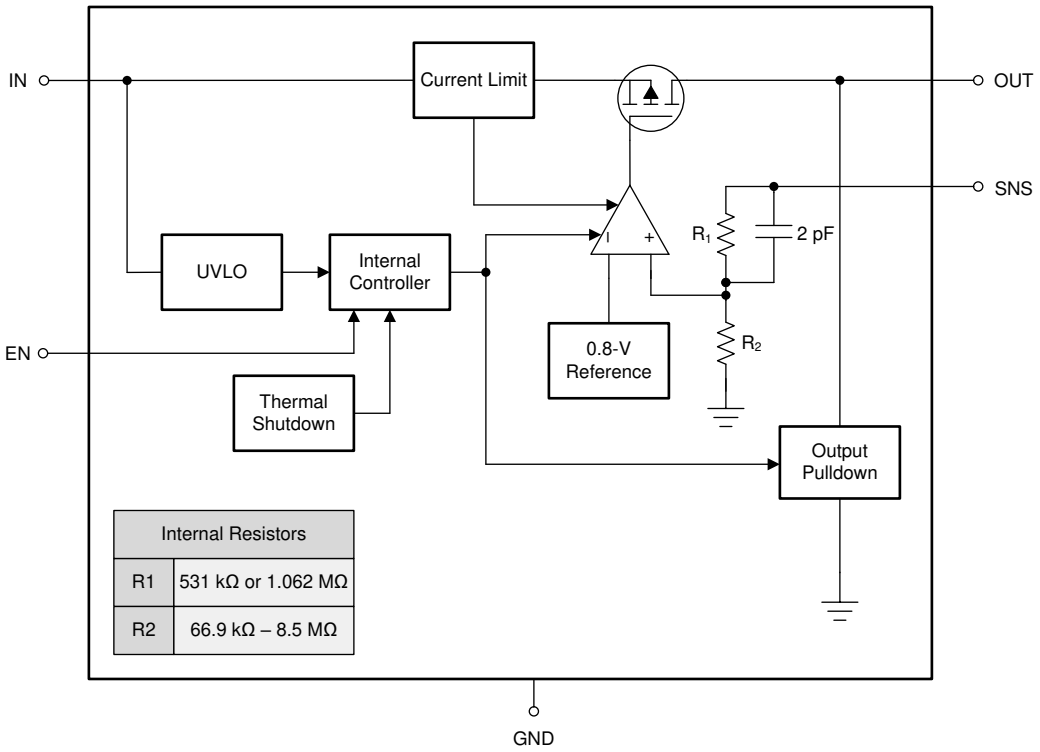


**图 36. Fixed-Version Block Diagram**

## 7.3 Feature Description

### 7.3.1 Output Enable

The enable pin for the device is an active-high pin. The output voltage is enabled when the voltage of the enable pin is greater than the high-level input voltage of the EN pin and disabled with the enable pin voltage is less than the low-level input voltage of the EN pin. If independent control of the output voltage is not needed, connect the enable pin to the input of the device.

This device has an internal pullup current on the EN pin. The EN pin can be left floating to enable the device.

The device has an internal pulldown circuit that activates when the device is disabled to actively discharge the output voltage.

### 7.3.2 Dropout Voltage

Dropout voltage ($V_{DO}$) is defined as the input voltage minus the output voltage ($V_{IN} – V_{OUT}$) at the rated output current ($I_{RATED}$), where the pass transistor is fully on. $I_{RATED}$ is the maximum $I_{OUT}$ listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. Use Equation 1 to calculate the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

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## Feature Description (continued)

### 7.3.3 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brickwall scheme limits the output current to the current limit ($I_{CL}$). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit ($I_{SC}$). $I_{CL}$ and $I_{SC}$ are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK}$ = 50% × $V_{OUT(nom)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power [($V_{IN}$ – $V_{OUT}$) × $I_{CL}$]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [($V_{IN}$ – $V_{OUT}$) × $I_{SC}$]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application report.

Figure 37 shows a diagram of the foldback current limit.

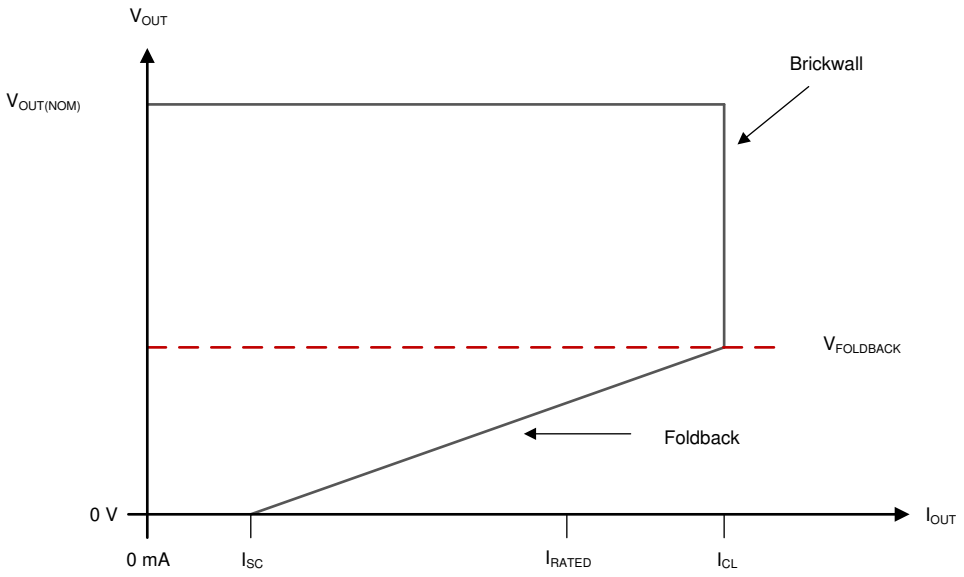


**Figure 37. Foldback Current Limit**

### 7.3.4 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

### 7.3.5 Output Pulldown

The device has an output pulldown circuit. $V_{OUT}$ pulldown sink to ground capability is listed in the *Electrical Characteristics* table. The output pulldown activates under the following conditions:

- Device disabled
- 1.0 V < $V_{IN}$ < $V_{UVLO}$

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## Feature Description (continued)

The output pulldown current for this device is 1.2 mA typical, as listed in the *Electrical Characteristics* table of the *Specifications* section.

Do not rely on the output pulldown circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can flow from the output to the input. This reverse current flow can cause damage to the device. See the *Reverse Current* section for more details.

### 7.3.6 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature ($T_J$) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup can be high from large $V_{IN}$ – $V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

## 7.4 Device Functional Modes

### 7.4.1 Device Functional Mode Comparison

The *Device Functional Mode Comparison* table shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

**Table 1. Device Functional Mode Comparison**

| OPERATING MODE | PARAMETER | | | |
|---|---|---|---|---|
| | $V_{IN}$ | $V_{EN}$ | $I_{OUT}$ | $T_J$ |
| Normal operation | $V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$ | $V_{EN} > V_{EN(HI)}$ | $I_{OUT} < I_{OUT(max)}$ | $T_J < T_{SD(shutdown)}$ |
| Dropout operation | $V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$ | $V_{EN} > V_{EN(HI)}$ | $I_{OUT} < I_{OUT(max)}$ | $T_J < T_{SD(shutdown)}$ |
| Disabled (any true condition disables the device) | $V_{IN} < V_{UVLO}$ | $V_{EN} < V_{EN(LOW)}$ | Not applicable | $T_J > T_{SD(shutdown)}$ |

### 7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

### 7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

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When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

### 7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

## 8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

#### 8.1.1 Adjustable Device Feedback Resistors

The adjustable-version device requires external feedback divider resistors to set the output voltage. $V_{OUT}$ is set using the feedback divider resistors, $R_1$ and $R_2$, according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (2)$$

To ignore the FB pin current error term in the $V_{OUT}$ equation, set the feedback divider current to 100x the FB pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100) \quad (3)$$

#### 8.1.2 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a rule of thumb, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

#### 8.1.3 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is recommended if the source impedance is more than 0.5 Ω. A higher value capacitor may be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

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## Application Information (continued)

### 8.1.4 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3$ V.

- If the device has a large $C_{OUT}$ and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

Figure 38 shows one approach for protecting the device.

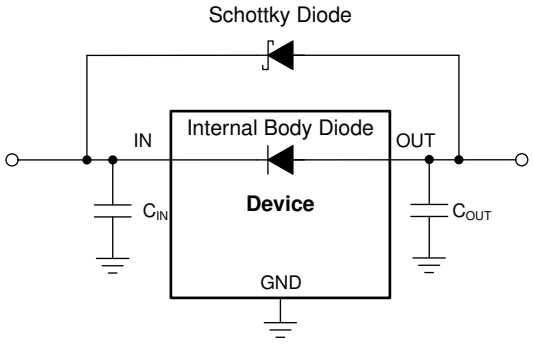


**Figure 38. Example Circuit for Reverse Current Protection Using a Schottky Diode**

### 8.1.5 Feed-Forward Capacitor ($C_{FF}$)

For the adjustable-voltage version device, a feed-forward capacitor ($C_{FF}$) can be connected from the OUT pin to the FB pin. $C_{FF}$ improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended $C_{FF}$ values are listed in the *Recommended Operating Conditions* table. A higher capacitance $C_{FF}$ can be used; however, the startup time increases. For a detailed description of $C_{FF}$ tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report.

$C_{FF}$ and $R_1$ form a zero in the loop gain at frequency $f_Z$, while $C_{FF}$, $R_1$, and $R_2$ form a pole in the loop gain at frequency $f_P$. $C_{FF}$ zero and pole frequencies can be calculated from the following equations:

$$f_Z = 1 / (2 \times \pi \times C_{FF} \times R_1) \quad (4)$$

$$f_P = 1 / (2 \times \pi \times C_{FF} \times (R_1 \parallel R_2)) \quad (5)$$

$C_{FF} \geq 10$ pF is required for stability if the feedback divider current is less than 5 µA. 公式 6 calculates the feedback divider current.

$$I_{FB\_Divider} = V_{OUT} / (R_1 + R_2) \quad (6)$$

To avoid startup time increases from $C_{FF}$, limit the product $C_{FF} \times R_1 < 50$ µs.

For an output voltage of 0.8 V with the FB pin tied to the OUT pin, no $C_{FF}$ is used.

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## Application Information (continued)

### 8.1.6 Power Dissipation ($P_D$)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Equation 7 calculates power dissipation ($P_D$).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (7)$$

**NOTE**

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature ($T_A$) for the device. According to Equation 8, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air ($T_A$).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (8)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

### 8.1.7 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi ($\Psi$) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter ($\psi_{JT}$) and junction-to-board characterization parameter ($\psi_{JB}$). These parameters provide two methods for calculating the junction temperature ($T_J$). As described in , use the junction-to-top characterization parameter ($\psi_{JT}$) with the temperature at the center-top of device package ($T_T$) to calculate the junction temperature. As described in , use the junction-to-board characterization parameter ($\psi_{JB}$) with the PCB surface temperature 1 mm from the device package ($T_B$) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D$$

where:

- $P_D$ is the dissipated power
- $T_T$ is the temperature at the center-top of the device package (9)

$$T_J = T_B + \psi_{JB} \times P_D$$

where

- $T_B$ is the PCB surface temperature measured 1 mm from the device package and centered on the package edge (10)

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application report.

ADVANCE INFORMATION

## 8.2 Typical Application

This section discusses implementing this device for a typical application. 图 39 shows the application circuit.

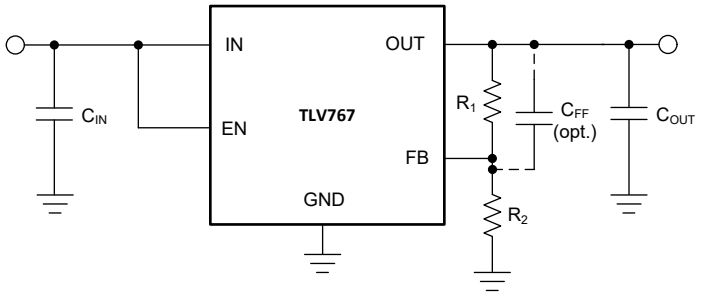



**图 39. Typical Application Circuit**

### 8.2.1 Design Requirements

表 2 summarizes the design requirements for this application.

**表 2. Design Parameters**

| PARAMETER | DESIGN REQUIREMENT |
|---|---|
| Input voltage | 5 V |
| Output voltage | 3.3 V |
| Output current | 100 mA |

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 Transient Response*

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude. If load transients are expected with ramp rates greater than 0.5 A/µs, use a 2.2-µF or larger output capacitor.

### 8.2.3 Choose Feedback Resistors

For this design example, $V_{OUT}$ is set to 3.3 V. The following equations set the feedback divider resistors for the desired output voltage:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (11)$$

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100) \quad (12)$$

For improved output accuracy, use Equation 12 and $I_{FB}$ = 50 nA as listed in the *Electrical Characteristics* table of the *Specifications* section to calculate the upper limit for series feedback resistance ($R_1 + R_2 \leq 660$ kΩ).

The control-loop error amplifier drives the FB pin to the same voltage as the internal reference ($V_{FB}$ = 0.8 V, as listed in the *Electrical Characteristics* table). Use Equation 11 to determine the ratio of $R_1 / R_2 = 3.125$. Use this ratio and solve Equation 12 for $R_2$. Now calculate the upper limit for $R_2 \leq 160$ kΩ. Select a standard value resistor for $R_2$ = 160 kΩ.

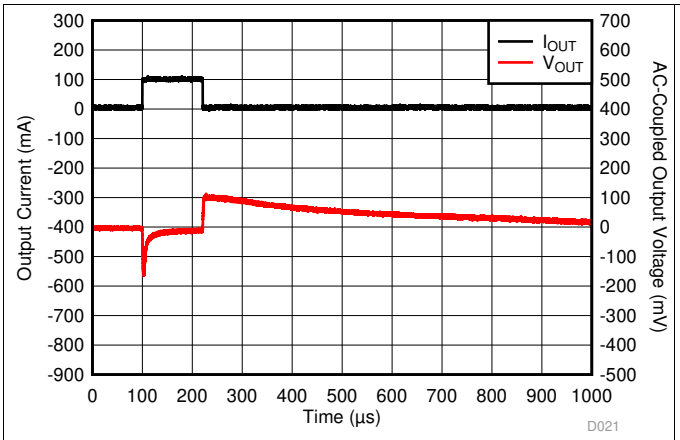
Reference Equation 11 and solve for $R_1$:

$$R_1 = (V_{OUT} / V_{FB} - 1) \times R_2 \quad (13)$$

From 公式 13, $R_1$ = 500 kΩ can be determined. Select a standard value resistor for $R_1$ = 499 kΩ. $V_{OUT}$ = 3.3 V (as determined by Equation 11).

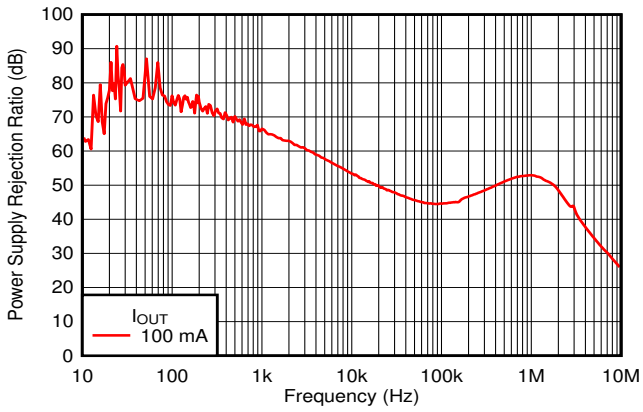
ADVANCE INFORMATION

### 8.2.4 Application Curves




$V_{IN}$ = 5 V, $V_{OUT}$ = 3.3 V, $C_{OUT}$ = 1 µF, $C_{FF}$ = 10 pF

**图 40. Load Transient Response, $I_{OUT}$ 0 mA to 100 mA**




$V_{IN}$ = 5 V, $V_{OUT}$ = 3.3 V, $C_{OUT}$ = 1 µF, $C_{FF}$ = 0 pF

**图 41. PSRR Performance**

## 9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 2.5 V to 16 V. To ensure that the output voltage is well regulated and dynamic performance is optimum, the input supply must be at least $V_{OUT(nom)}$ + 1.5 V. For a 1-A output current operation, the input supply must be 3 V or greater. Connect a low output impedance power supply directly to the input pin of the TLV767-Q1.

ADVANCE INFORMATION

# 10 Layout

## 10.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible
- Use copper planes for device connections to IN, OUT, and GND pins to optimize thermal performance
- Place thermal vias around the device to distribute heat

## 10.2 Layout Examples


**图 42. Layout Example for the Adjustable Version**


**图 43. Layout Example for the Fixed Version**

# 11 器件和文档支持

## 11.1 器件支持

### 11.1.1 器件命名规则

表 3. 提供的选项(1)

| 产品 | $V_{OUT}$ |
|---|---|
| TLV767**xx(x)QWyyyRQ1** | **xx(x)** 为标称输出电压。对于分辨率为 100mV 的输出电压，订购编号中使用两位数字；否则，使用三位数字（例如，33 = 3.3V；125 = 1.25V）。01 表示可调节输出版本。<br>**yyy** 是封装符号。<br>**R** 为封装数量。R 表示大数量卷带。 |

(1) 要获得最新的封装和订货信息，请参阅本文档末尾的封装选项附录，或者访问www.ti.com.cn上的器件产品文件夹。

## 11.2 文档支持

### 11.2.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《TLV767EVM-014 评估模块》* 用户指南
- 德州仪器 (TI)，*《使用前馈电容器和低压降稳压器的优缺点》* 应用报告
- 德州仪器 (TI)，*《了解限制》* 应用报告
- 德州仪器 (TI)，*《通用低压降 (LDO) 线性稳压器 MultiPkgLDOEVM-823 评估模块》* 用户指南

## 11.3 接收文档更新通知

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## 11.4 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

## 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV76701QWDRBRQ1 | ACTIVE | SON | DRB | 8 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | V76701 | Samples |
| TLV76733QWDRBRQ1 | ACTIVE | SON | DRB | 8 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | V76733 | Samples |
| TLV76750QWDRBRQ1 | ACTIVE | SON | DRB | 8 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | V76750 | Samples |
| TLV76760QWDRBRQ1 | ACTIVE | SON | DRB | 8 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | V76760 | Samples |
| TLV76780QWDRBRQ1 | ACTIVE | SON | DRB | 8 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | V76780 | Samples |
| TLV76790QWDRBRQ1 | ACTIVE | SON | DRB | 8 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | V76790 | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## GENERIC PACKAGE VIEW

# DRB 8

# VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

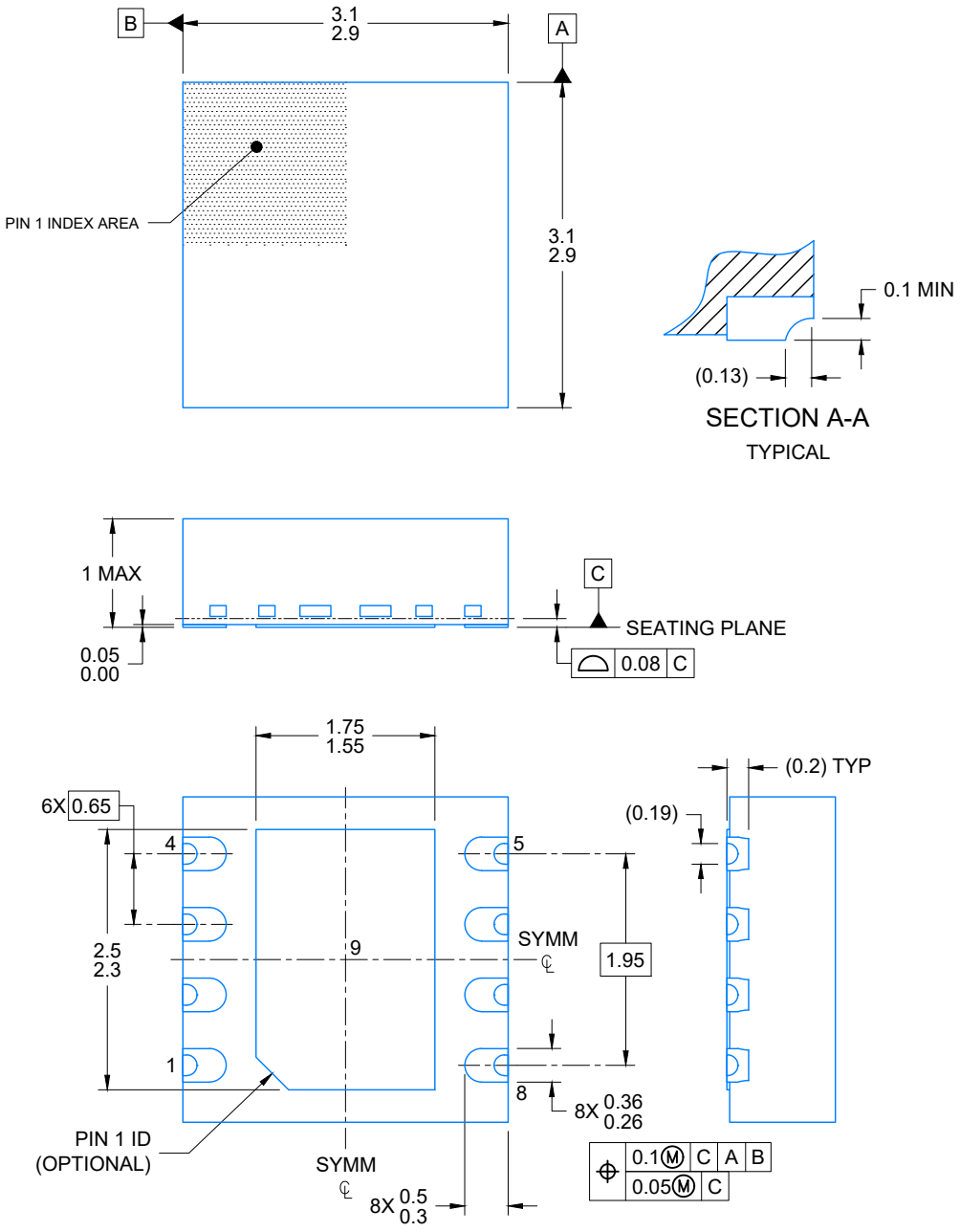
4203482/L

# PACKAGE OUTLINE

## DRB0008J

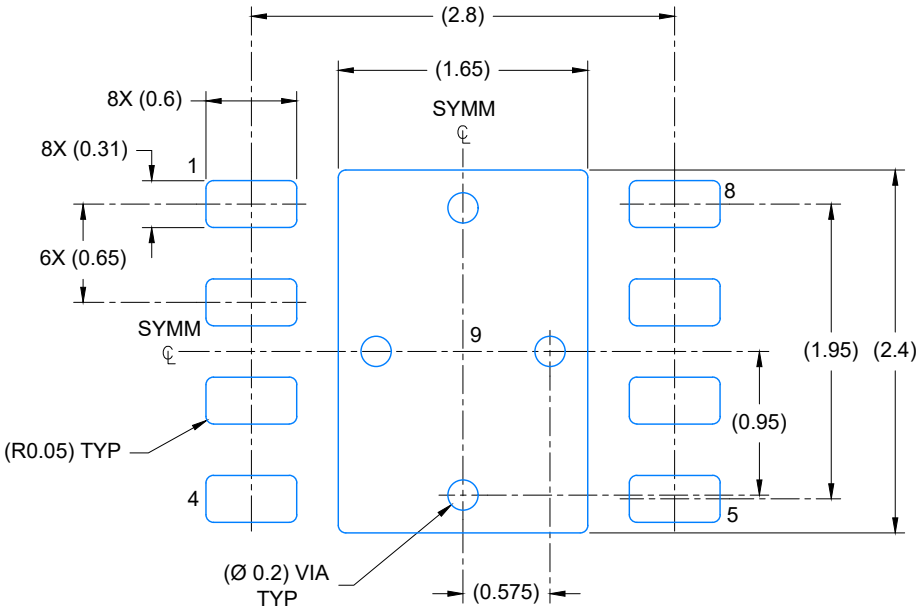
## VSON - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

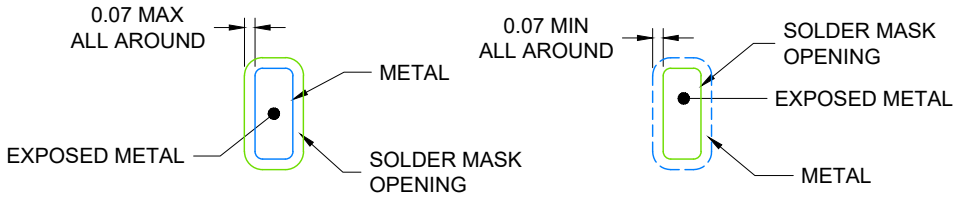



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X




NON- SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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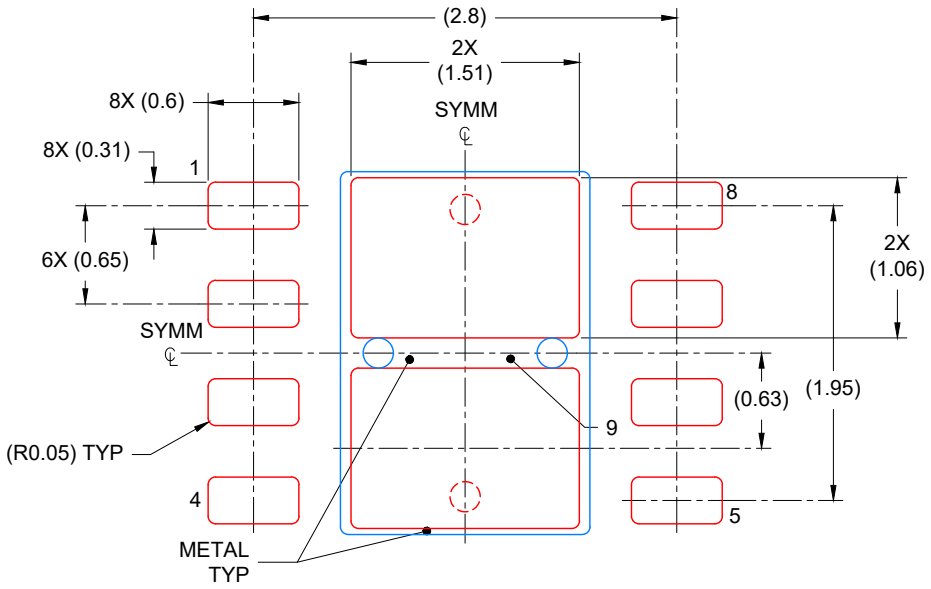
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

4225036/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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