DS90UA102-Q1 多通道数字音频链路

查询样品: DS90UA102-Q1

特性

- 数字音频解串器
- 灵活的数字音频输出，支持 **I²S**（立体声）和时分复用 **(TMD)** （多通道）格式
- 同轴或单个差分对互连
- 高速串行输入接口
- 极低延迟 **(< 15µs)**
- 具有 **I²C** 兼容串行控制总线的双向控制接口通道
- 支持多达 **8** 个立体声 **I²S** 或 **TDM** 音频输出
- 支持 **10MHz** 至 **50MHz** 的音频系统时钟
- 单个 **1.8V** 电源
- **1.8V** 或 **3.3V I/O** 接口
- **4/4** 个专用通用输入/输出
- 长达 **15m** 的交流耦合屏蔽双绞线 **(STP)** 或同轴电缆
- 具有嵌入式时钟的直流均衡 **&** 扰频数据
- 自适应电缆均衡
- 全速链路内置自检 **(BIST)** 模式和锁定 **(LOCK)** 状态引脚
- 汽车应用级产品：符合 **AEC-Q100 2** 级要求
- 温度范围：**-40°C** 至 **105°C**
- 符合 **ISO 10605** 以及 **IEC 61000-4-2** 静电放电 **(ESD)** 标准

应用范围

- 汽车信息娱乐系统
- 主动噪声消除系统
- 分布式多通道音频系统

说明

此 DS90UA102-Q1 解串器，与 DS90UA101-Q1 串行器一同使用，为多通道音频系统中数字音频分配提供了一个解决方案。 它在一个单条屏蔽双绞线或同轴电缆上借助一个嵌入式时钟用高速已串化接口接收数据。 这个串行总线系统配置在链路上支持高速数据正向传输和低速双向控制通道。 数字音频、通用 IO 和一个单差分对上控制信号的联合使用减少了互连尺寸和重量，同时也减少了与偏斜和系统延迟相关的设计问题。

此DS90UA102-Q1 解串器提取时钟，并将来自高速低压差分信令的信号电平位移至单端 LVCMOS。 此器件输出多达 8 个数字音频数据通道、字/帧同步、位时钟和系统时钟。

四个专用的通用输入引脚和四个通用输出引脚可灵活地实现与远程器件之间的控制和中断信号传输。

串行输入数据流的自适应均衡为线缆的传输介质损耗提供补偿，并减少了介质引入的确定性抖动。

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Applications Diagram

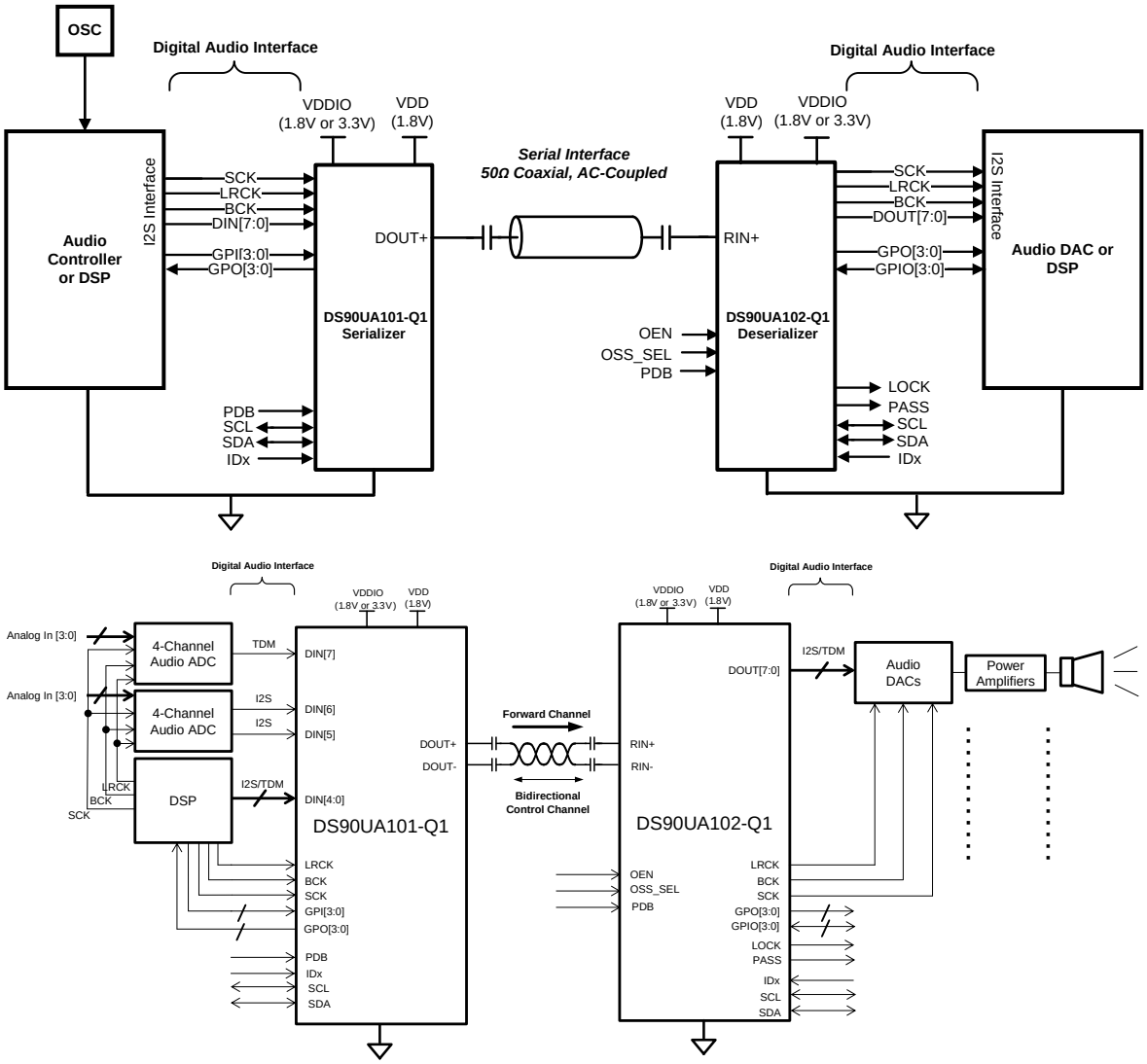


Figure 1. Typical Applications

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Block Diagram

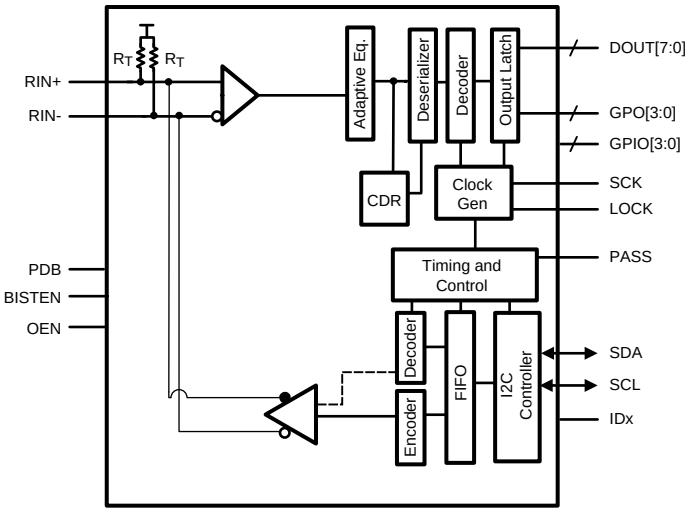


Figure 2. Block Diagram

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DS90UA102-Q1 Pin Diagram

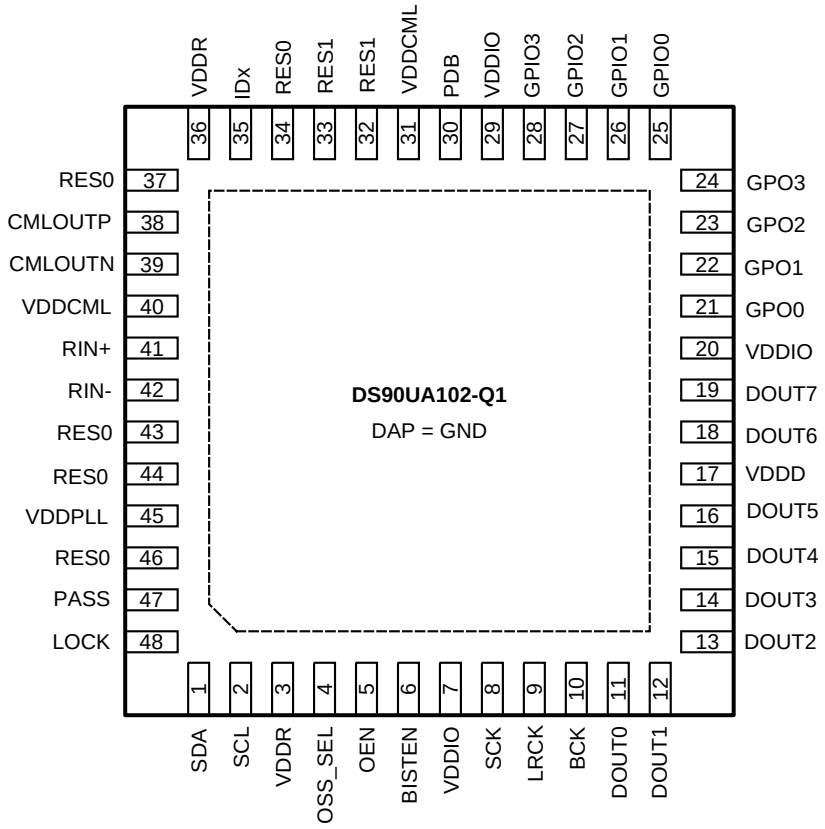


Figure 3. DS90UA102-Q1 — Top View

Pin Descriptions

Pin Name	Pin #	I/O, Type	Description
Digital Audio Interface			
SCK	8	Output, LVCMOS	System clock output. Recovered system clock fed into the Serializer's SCK pin.
LRCK	9	Output, LVCMOS	Word clock output.
BCK	10	Output, LVCMOS	Bit clock output.
DOUT[7:0]	11, 12, 13, 14, 15, 16, 18, 19	Outputs, LVCMOS	Digital audio data outputs.
LVCMOS Parallel Interface			
GPIO[3:0]	28, 27, 26, 25	Inputs/Outputs, LVCMOS w/ pull down	General purpose I/Os. May be configured as inputs to the back-channel (which can be read by the Serializer), or as local register outputs.
GPO[3:0]	24, 23, 22, 21	Outputs, LVCMOS	General purpose outputs, transported over the forward channel from the Serializer.
Control and Configuration			
SDA	1	Input/Output, Open Drain	I^2C data input/output line. Must have an external pull-up to V_{DDIO}. DO NOT FLOAT. Recommended pull-up: 4.7 kΩ.
SCL	2	Input/Output, Open Drain	I^2C clock line. Must have an external pull-up to V_{DDIO}. DO NOT FLOAT. Recommended pull-up: 4.7 kΩ.
OSS_SEL	4	Input, LVCMOS w/ pull down	Output sleep state select. Refer to Table 5.

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Pin Name	Pin #	I/O, Type	Description
OEN	5	Input, LVCMOS w/ pull down	Output enable. Refer to Table 5.
BISTEN	6	Input, LVCMOS w/ pull down	BIST enable pin. BISTEN = H, BIST mode is enabled. BISTEN = L, BIST mode is disabled.
PDB	30	Input, LVCMOS w/ pull down	Power down mode input pin. PDB = H device is enabled and is ON. PDB = L, device is powered down. When the device is in the powered down state, the PLL is shutdown, IDD is minimized, and control registers are RESET.
IDx	35	Input, Analog	Device I^2C address select. The IDx pin on the Deserializer is used to assign its I^2C device address. See Table 2. DO NOT FLOAT.
Serial Interface			
RIN+	41	Input, LVDS	True serial interface input. The interconnection must be AC-coupled to this pin with a 0.1 µF capacitor.
RIN-	42	Input, LVDS	Inverting serial interface input. The interconnection must be AC-coupled to this pin with a 0.1 µF capacitor.
CMLOUTP	38	Output, LVDS	True CML output. Monitor point for equalized input signal.
CMLOUTN	39	Output, LVDS	Inverting CML output. Monitor point for equalized input signal.
Status			
PASS	47	Output, LVCMOS	PASS status output pin. PASS = H: Error-free transmission (applies to BIST and normal operation). PASS = L: One or more parity errors occurred in the received payload. In normal and BIST mode, PASS pin toggles low momentarily for each parity error. In BIST mode only, PASS pin also toggles low momentarily at the end of the BIST if at least one error occurred during the test. Leave open if unused. Otherwise, route to a test point/pad (recommended).
LOCK	48	Output, LVCMOS	LOCK status output pin. LOCK = H: PLL is locked; Deserializer outputs are active. LOCK = L: PLL is unlocked; Deserializer outputs are not valid with respect to Serializer inputs. Leave open if unused. Otherwise, route to a test point/pad (recommended).
Power and Ground			
VDDR	3, 36	Power	1.8V (±5%) analog core power.
VDDIO	7, 20, 29	Power	LVCMOS I/O power. 1.8V (±5%) or 3.3V (±10%).
VDDD	17	Power	1.8V (±5%) digital power.
VDDCML	31, 40	Power	1.8V (±5%) CML receiver and Bidirectional Control Channel power.
VDDPLL	45	Power	1.8V (±5%) PLL power.
GND	DAP	Ground	DAP is the large metal contact located at the bottom center of the LLP package. Connect to the GND plane with at least 9 vias.
Other			
RES0	34, 37, 43, 44, 46	Reserved	Reserved. Tie to GND.
RES1	32, 33	Reserved	Reserved. Leave floating.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage – V_{DDn} (1.8V)	−0.3V to +2.5V
Supply Voltage – V_{DDIO}	−0.3V to +4.0V
LVCMOS I/O Voltage	−0.3V to + (V_{DDIO} + 0.3V)
CML Driver/Receiver I/O Voltage (V_{DDCML})	−0.3V to +(V_{DDCML} + 0.3V)
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Maximum Package Power Dissipation Capacity	$1/\theta_{JA}$ °C/W above +25°
Package Derating: DS90UA102-Q1 48L WQFN	
θ_{JA}*(based on 16 thermal vias)*	26.9°C/W
θ_{JC}*(based on 16 thermal vias)*	4.4°C/W
ESD Rating (IEC 61000-4-2)	R_D = 330Ω, C_S = 150 pF
Air Discharge (RIN+, RIN-)	≥±25 kV
Contact Discharge (RIN+, RIN-)	≥±7 kV
ESD Rating (ISO10605)	R_D = 330Ω, C_S = 150/330 pF
ESD Rating (ISO10605)	R_D = 2KΩ, C_S = 150/330 pF
Air Discharge (RIN+, RIN–)	≥±15 kV
Contact Discharge (RIN+, RIN-)	≥±8 kV
ESD Rating (HBM)	≥±8 kV
ESD Rating (CDM)	≥±1 kV
ESD Rating (MM)	≥±250 V

For soldering specifications: see product folder at www.ti.com and www.ti.com/lit/an/snoa549c/snoa549c.pdf

(1) “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional; the device should not be operated beyond such conditions.

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RECOMMENDED OPERATING CONDITIONS

	Min	Nom	Max	Units
Supply Voltage (V_{DDn})	1.71	1.8	1.89	V
LVCMOS Supply Voltage (V_{DDIO}) OR	1.71	1.8	1.89	V
LVCMOS Supply Voltage (V_{DDIO})	3.0	3.3	3.6	V
Supply Noise(1)				
V_{DDn} (1.8V)			25	mVp-p
V_{DDIO} (1.8V)			25	mVp-p
V_{DDIO} (3.3V)			50	mVp-p
Operating Free Air Temperature (T_A)	–40	+25	+105	°C
SCK Clock Frequency (STP Cable)	10		50	MHz
SCK Clock Frequency (Coaxial Cable)	25		50	MHz

(1) Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC coupled to the V_{DDn} (1.8V) supply with amplitude = 25 mVp-p measured at the device V_{DDn} pins. Bit error rate testing of input to the Ser and output of the Des with 10 meter cable shows no error when the noise frequency on the Ser is less than 1 MHz. The Des on the other hand shows no error when the noise frequency is less than 750 kHz.

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ELECTRICAL CHARACTERISTICS

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2) (3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
LVCMOS DC SPECIFICATIONS 3.3V I/O (DES OUTPUTS, GPIO, GPO, CONTROL INPUTS AND OUTPUTS)							
V_{IH}	High Level Input Voltage	V_{IN} = 3.0V to 3.6V		2.0		V_{IN}	V
V_{IL}	Low Level Input Voltage	V_{IN} = 3.0V to 3.6V		GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0V or 3.6V V_{IN} = 3.0V to 3.6V		-20	±1	+20	µA
V_{OH}	High Level Output Voltage	V_{DDIO} = 3.0V to 3.6V I_{OH} = −4 mA		2.4		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	V_{DDIO} = 3.0V to 3.6V I_{OL} = +4 mA		GND		0.4	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V	Deserializer LVCMOS Outputs		–35		mA
I_{OZ}	TRI-STATE Output Current	PDB = 0V, V_{OUT} = 0V or V_{DD}	LVCMOS Outputs	-20		+20	µA
LVCMOS DC SPECIFICATIONS 1.8V I/O (DES OUTPUTS, GPIO, GPO, CONTROL INPUTS AND OUTPUTS)							
V_{IH}	High Level Input Voltage	V_{IN} = 1.71V to 1.89V		0.65 V_{IN}		V_{IN}	V
V_{IL}	Low Level Input Voltage	V_{IN} = 1.71V to 1.89V		GND		0.35 V_{IN}	
I_{IN}	Input Current	V_{IN} = 0V or 1.89V V_{IN} = 1.71V to 1.89V		-20	±1	+20	µA
V_{OH}	High Level Output Voltage	V_{DDIO} = 1.71V to 1.89V I_{OH} = −4 mA		V_{DDIO} - 0.45		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	V_{DDIO} = 1.71V to 1.89V I_{OL} = +4 mA	Deserializer LVCMOS Outputs	GND		0.45	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V	Deserializer LVCMOS Outputs		-17		mA
I_{OZ}	TRI-STATE Output Current	PDB = 0V, V_{OUT} = 0V or V_{DD}	LVCMOS Outputs	-20		+20	µA
CML RECEIVER DC SPECIFICATIONS (RIN+,RIN-)							
I_{IN}	Input Current	V_{IN} = V_{DD} or 0V, V_{DD} = 1.89V		-20	1	+20	µA
R_T	Differential Internal Termination Resistance	Differential across RIN+ and RIN-		80	100	120	Ω
	Single-ended Termination Resistance	RIN+ or RIN–		40	50	60	
CML RECEIVER AC SPECIFICATIONS (RIN+,RIN–)							
$\|V_{swing}\|$	Minimum allowable swing for 1010 pattern (4)	Line Rate = 1.4 Gbps (Figure 5)		135			mV
CML MONITOR OUTPUT DRIVER SPECIFICATIONS (CMLOUTP, CMLOUTN)							
E_w	Differential Output Eye Opening	R_L = 100Ω Jitter Frequency>ƒ/40 (Figure 10)			0.45		UI
E_H	Differential Output Eye Height				200		mV

(1) The Electrical Characteristics tables list verified specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not verified.

(2) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD}, ΔV_{OD}, V_{TH} and V_{TL} which are differential voltages.

(3) Typical values represent most likely parametric norms at 1.8V or 3.3V, T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not verified .

(4) Specification is verified by characterization and is not tested in production.

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ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.(1) (2) (3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
SUPPLY CURRENT, DIGITAL, PLL, AND ANALOG VDD							
I_{DDIOR}	Deserializer (Rx) V_{DDIO} Supply Current (includes load current)	V_{DDIO} = 1.89V C_L = 8pF Worst Case Pattern	f = 50 MHz		21	32	mA
		V_{DDIO} = 1.8V C_L = 8 pF Random Pattern	f = 24.576 MHz		4		
			f = 12.288 MHz		2		
		V_{DDIO} = 3.6V C_L=8pF Worst Case Pattern	f = 50 MHz		25	38	
		V_{DDIO} = 3.3V C_L = 8pF Random Pattern	f = 24.576 MHz		15		
			f = 12.288 MHz		12		
I_{DDR}	Deserializer (Rx) V_{DDn} Supply Current	V_{DDn}= 1.89V C_L=4pF Worst Case Pattern	f = 50 MHz		63	96	mA
		V_{DDn}= 1.8V C_L=8pF Random Pattern	f = 24.576 MHz		60		
			f = 12.288 MHz		56		
I_{DDRZ}	Deserializer (Rx) V_{DDn} Supply Current Power-down	PDB = 0V All other LVCMOS Inputs = 0V	V_{DDIO} = 1.89V Default Registers		42	900	µA
			V_{DDIO} = 3.6V Default Registers		42	900	
I_{DDIORZ}	Deserializer (Rx) V_{DDIO} Supply Current Power-down	PDB = 0V All other LVCMOS Inputs = 0V	V_{DDIO} = 1.89V		8	40	µA
			V_{DDIO} = 3.6V		360	800	

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ELECTRICAL CHARACTERISTICS: Deserializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2) (3)

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{RCP}	Receiver Output Clock Period	STP Cable	SCK (Figure 9)	20	T	100	ns
		Coaxial Cable		20	T	40	
t_{PDC}	SCK Duty Cycle		SCK	40	50	60	%
t_{CLH}	LVCMOS Low-to-High Transition Time	V_{DDIO}: 1.71V to 1.89V or 3.0V to 3.6V, C_L = 8 pF (lumped load) Default Registers (*Figure 7*), (4)	SCK	1.3	2	2.8	ns
t_{CHL}	LVCMOS High-to-Low Transition Time			1.3	2	2.8	
t_{CLH}	LVCMOS Low-to-High Transition Time	V_{DDIO}: 1.71V to 1.89V or 3.0V to 3.6V, C_L = 8 pF (lumped load) Default Registers (*Figure 7*), (4)	DOUT[7:0], GPO[3:0], BCK, LRCK	1	2.5	4	ns
t_{CHL}	LVCMOS High-to-Low Transition Time			1	2.5	4	
t_{ROS}	Setup Data to SCK	V_{DDIO}: 1.71V to 1.89V or 3.0V to 3.6V, C_L = 8 pF (lumped load) Default Registers (Figure 9)	DOUT[7:0], GPO[3:0], BCK, LRCK	0.38	0.5		T
t_{ROH}	Hold Data to SCK			0.38	0.5		
t_{DD}	Deserializer Delay	Default Registers Register 0x03h b[0] (RRFB = 1) (Figure 8), (4)		109		112	T
t_{DDLT}	Deserializer Data Lock Time	With Adaptive Equalization (Figure 6)			15	22	ms
t_{RCJ}	Receiver Clock Jitter	SCK (4)	SCK = 50 MHz		22	35	ps
t_{DPJ}	Deserializer Period Jitter	SCK (5)(4)	SCK = 50 MHz		180	330	ps
t_{DCCJ}	Deserializer Cycle-to-Cycle Clock Jitter	SCK (6)(4)	SCK = 50 MHz		460	730	ps

(1) The Electrical Characteristics tables list verified specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not verified.
(2) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD}, ΔV_{OD}, V_{TH} and V_{TL} which are differential voltages.
(3) Typical values represent most likely parametric norms at 1.8V or 3.3V, T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not verified .
(4) Specification is verified by characterization and is not tested in production.
(5) t_{DPJ} is the maximum amount the period is allowed to deviate measured over 30,000 samples.
(6) t_{DCCJ} is the maximum amount of jitter between adjacent clock cycles measured over 30,000 samples.

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BIDIRECTIONAL CONTROL BUS TIMING SPECIFICATIONS

Bidirectional Control Bus: AC Timing Specifications (SCL, SDA) - I²C Compliant

Over recommended supply and temperature ranges unless otherwise specified. (Figure 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Recommended Input Timing Requirements						
f_{SCL}	SCL Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	kHz
t_{LOW}	SCL Low Period	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_{HIGH}	SCL High Period	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
$t_{HD:STA}$	Hold time for a start or a repeated start condition	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
$t_{SU:STA}$	Set Up time for a start or a repeated start condition	Standard Mode	4.7			µs
		Fast Mode	0.6			µs
$t_{HD:DAT}$	Data Hold Time	Standard Mode	0		3.45	µs
		Fast Mode	0		900	ns
$t_{SU:DAT}$	Data Set Up Time	Standard Mode	250			ns
		Fast Mode	100			ns
$t_{SU:STO}$	Set Up Time for STOP Condition	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
t_{BUF}	Bus Free time between Stop and Start	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_r	SCL & SDA Rise Time	Standard Mode			1000	ns
		Fast Mode			300	ns
t_f	SCL & SDA Fall Time	Standard Mode			300	ns
		Fast Mode			300	ns

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Bidirectional Control Bus: DC Timing Specifications (SCL, SDA) - I²C Compliant (1)

Over recommended supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Recommended Input Timing Requirements						
V_{IH}	Input High Level	SDA and SCL	0.7*V_{DDIO}		V_{DDIO}	V
V_{IL}	Input Low Level	SDA and SCL	GND		0.3*V_{DDIO}	V
V_{HY}	Input Hysteresis			>50		mV
V_{OL}	Output Low Level	SDA, I_{OL}=0.5mA	0		0.4	V
I_{IN}	Input Current	SDA or SCL, V_{IN}=V_{DDIO} OR GND	—10		10	µA
t_R	SDA Rise Time-READ	SDA, RPU = 10kΩ, Cb ≤ 400pF(Figure 4)		430		ns
t_F	SDA Fall Time-READ			20		ns
$t_{SU;DAT}$		(Figure 4)		560		ns
$t_{HD;DAT}$		(Figure 4)		615		ns
t_{SP}				50		ns
C_{IN}		SDA or SCL		<5		pF

(1) Specification is verified by design.

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TIMING AND CIRCUIT DIAGRAMS

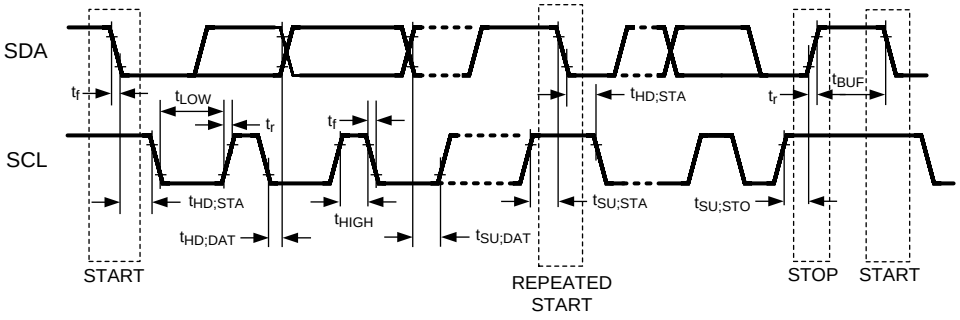


Figure 4. Bi-directional Control Bus Timing

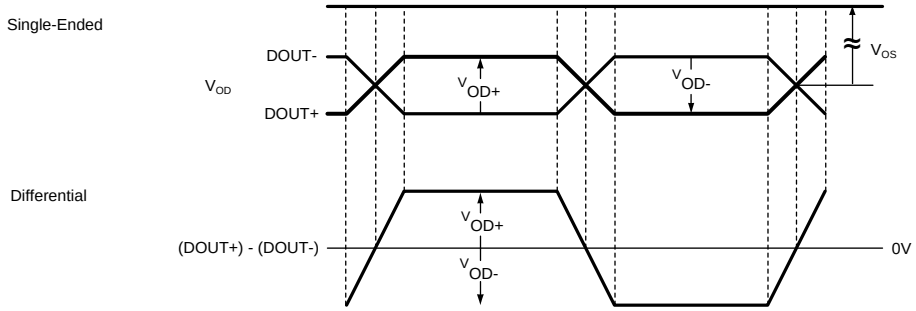


Figure 5. Differential Vswing Diagram

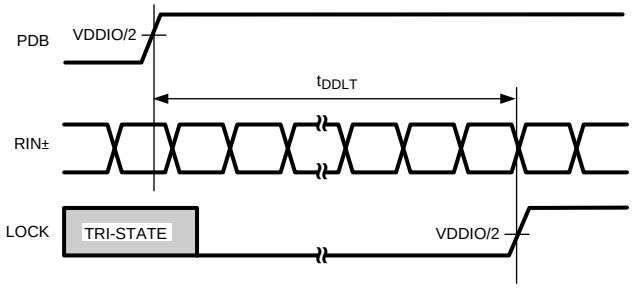


Figure 6. Deserializer Data Lock Time

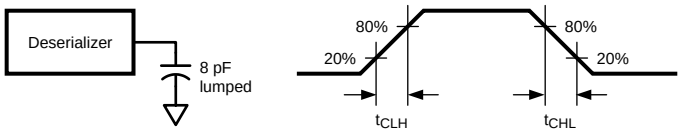


Figure 7. Deserializer LVCMOS Output Load and Transition Times

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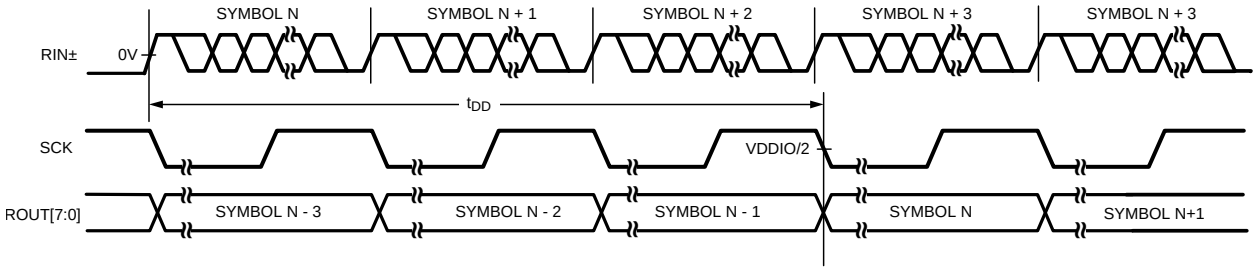


Figure 8. Deserializer Delay

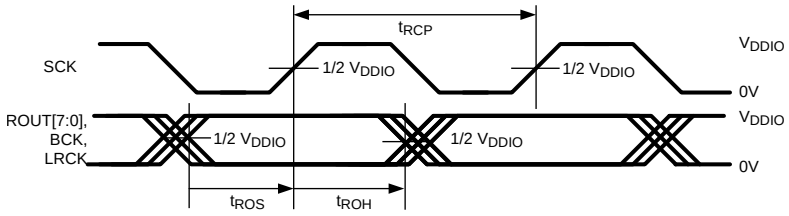


Figure 9. Deserializer Output Setup and Hold Times

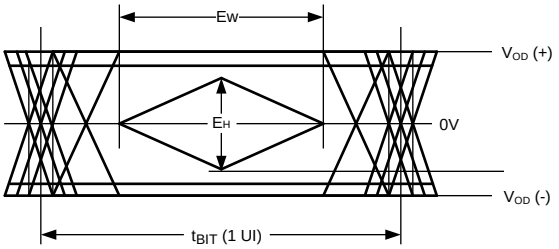


Figure 10. CML Output Driver

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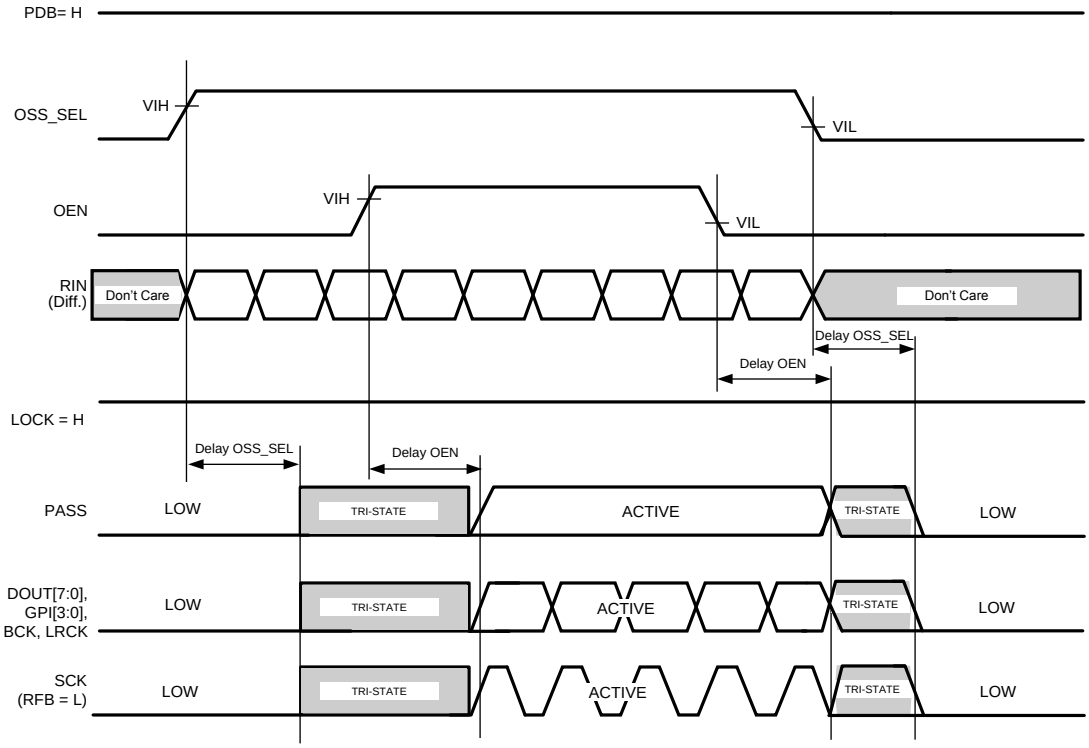


Figure 11. Output States

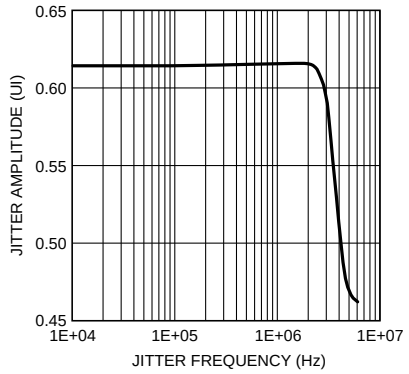


Figure 12. Typical Deserializer Input Jitter Tolerance Curve at 1.4Gbps Line Rate

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DS90UA102-Q1 REGISTER INFORMATION

The table below contains information on the DS90UA102-Q1 control registers. These registers are accessible locally via the I^2C control interface, or remotely via the Bidirectional Control Channel. Addresses not listed are reserved. Fields listed as reserved should not be changed from the listed default value.

Addr (Hex)	Name	Bits	Field	R/W	Default (Hex)	Description
0x00	I^2C Device ID	7:1	DEVICE ID	RW	0xC0	7-bit address of Deserializer. 0x60'h (0110_000X'b) default.
		0	DES ID SEL	RW		0: Deserializer DEVICE ID is from IDx. 1: Register I^2C DEVICE ID overrides IDx.
0x01	Reset	7:6	RSVD		0x04	Reserved.
		5	ANAPWDN	RW		This register can be set only through local I^2C access. 1: Analog power-down : Powers down the analog block in the Deserializer. 0: Analog power-up: Powers up the analog block in the Deserializer.
		4:2	RSVD			Reserved.
		1	Digital Reset 1	RW		1: Resets the digital block except for register values. This bit is self-clearing. 0: Normal operation.
		0	Digital Reset 0	RW		1: Resets the entire digital block including all register values. This bit is self-clearing. 0: Normal operation.
0x02	General Configuration 0	7:6	RSVD		0x00	Reserved.
		5	Auto-Clock	RW		1: Output SCK when LOCKED or internal oscillator clock when not LOCKED. 0: Output SCK when LOCKED only.
		4:0	RSVD			Reserved.

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Addr (Hex)	Name	Bits	Field	R/W	Default (Hex)	Description
0x03	General Configuration 1	7	RX Parity Checker Enable	RW	0xE9	Forward channel Parity Checker enable. 1: Enable. 0: Disable.
		6	TX CRC Checker Enable	RW		Back channel CRC Generator enable. 1: Enable. 0: Disable.
		5	V_{DDIO} Control	RW		Auto voltage control. 1: Enable (auto-detect mode). 0: Disable.
		4	V_{DDIO} Mode	RW		V_{DDIO} voltage set. 1: Sets V_{DDIO} mode to 3.3V. 0: Sets V_{DDIO} mode to 1.8V.
		3	I^2C Pass-Through	RW		I^2C pass-through mode. 1: Pass-through enabled. Refer to I^2C Pass-Through and Multiple Device Addressing. 0: Pass-through disabled.
		2	I^2C Remote Write Auto Acknowledge	RW		Automatically acknowledge I^2C remote writes. This mode should only be used when the system is LOCKED. 1: Enable: When enabled, I^2C writes to the Serializer (or any remote I^2C slave, if I^2C Pass All is enabled) are immediately acknowledged without waiting for the Serializer to acknowledge the write. The accesses are then remapped to address specified in 0x06. 0: Disable.
		1	Parity Error Reset	RW		Clear parity error counters. This bit is self-clearing. 1: Clear parity error counters. 0: Normal operation.
		0	RRFB	RW		SCK clock edge select. 1: Parallel interface data is strobed on the rising clock edge. 0: Parallel interface data is strobed on the falling clock edge.
0x04	EQ Feature Control	7:0	EQ Level	RW	0x00	Equalization gain: When AEQ bypass is enabled EQ setting is provided by this register. 0x00 = ~0.0 dB. 0x01 = ~4.5 dB. 0x03 = ~6.5 dB. 0x07 = ~7.5 dB. 0x0F = ~8.0 dB. 0x1F = ~11.0 dB. 0x3F = ~12.5 dB.

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Addr (Hex)	Name	Bits	Field	R/W	Default (Hex)	Description
0x06	SER ID	7:1	Remote Serializer Device ID	RW		This field stores the 7-bit I²C address of the remote Serializer. If an I²C transaction (originating from the Deserializer side) is addressed to SER Alias, the transaction will be remapped to this address before it is passed across the Bidirectional Control Channel to the remote Serializer. This field is automatically configured by the Bidirectional Control Channel once RX LOCK has been detected. Software may overwrite this value, but the Freeze Device ID bit should also be asserted to prevent overwriting by the Bidirectional Control Channel. A value of 0 in this field disables I²C access to the remote Serializer. Refer to I²C Pass-Through and Multiple Device Addressing.
		0	Freeze Device ID	RW		Freeze Serializer Device ID. 1: Prevents auto-loading of the Serializer Device ID from the forward channel. The ID will be frozen at the value written. 0: Allows auto-loading of the Serializer Device ID from the forward channel.
0x07	SER Alias	7:1	Serializer Alias ID	RW	0x00	This field stores a 7-bit I²C address. Once set, it configures the Deserializer to accept any transaction designated for the I²C address stored in this field. The transaction will then be remapped to the I²C address specified in the SER ID register. A value of 0 in this field disables I²C access to the remote Serializer. Refer to I²C Pass-Through and Multiple Device Addressing.
		0	RSVD			Reserved.
0x08	Slave ID[0]	7:1	Slave ID0	RW	0x00	This field stores the 7-bit I²C address of remote slave 0, attached to the remote Serializer. If an I²C transaction (originating from the Deserializer side) is addressed to Slave Alias0, the transaction will be remapped to this address before it is passed across the Bidirectional Control Channel to the remote Serializer, where it is then passed to remote slave 0. A value of 0 in this field disables I²C access to remote slave 0. Refer to I²C Pass-Through and Multiple Device Addressing.
		0	RSVD			Reserved.
0x09	Slave ID[1]	7:1	Slave ID1	RW	0x00	This field stores the 7-bit I²C address of remote slave 1, attached to the remote Serializer. If an I²C transaction (originating from the Deserializer side) is addressed to Slave Alias1, the transaction will be remapped to this address before it is passed across the Bidirectional Control Channel to the remote Serializer, where it is then passed to remote slave 1. A value of 0 in this field disables I²C access to remote slave 1. Refer to I²C Pass-Through and Multiple Device Addressing.
		0	RSVD			Reserved.

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Addr (Hex)	Name	Bits	Field	R/W	Default (Hex)	Description
0x0A	Slave ID[2]	7:1	Slave ID2	RW	0x00	This field stores the 7-bit I^2C address of remote slave 2, attached to the remote Serializer. If an I^2C transaction (originating from the Deserializer side) is addressed to Slave Alias2, the transaction will be remapped to this address before it is passed across the Bidirectional Control Channel to the remote Serializer, where it is then passed to remote slave 2. A value of 0 in this field disables I^2C access to remote slave 2. Refer to I^2C Pass-Through and Multiple Device Addressing.
		0	RSVD			Reserved.
0x0B	Slave ID[3]	7:1	Slave ID3	RW	0x00	This field stores the 7-bit I^2C address of remote slave 3, attached to the remote Serializer. If an I^2C transaction (originating from the Deserializer side) is addressed to Slave Alias3, the transaction will be remapped to this address before it is passed across the Bidirectional Control Channel to the remote Serializer, where it is then passed to remote slave 3. A value of 0 in this field disables I^2C access to remote slave 3. Refer to I^2C Pass-Through and Multiple Device Addressing.
		0	RSVD			Reserved.
0x0C	Slave ID[4]	7:1	Slave ID4	RW	0x00	This field stores the 7-bit I^2C address of remote slave 4, attached to the remote Serializer. If an I^2C transaction (originating from the Deserializer side) is addressed to Slave Alias4, the transaction will be remapped to this address before it is passed across the Bidirectional Control Channel to the remote Serializer, where it is then passed to remote slave 4. A value of 0 in this field disables I^2C access to remote slave 4. Refer to I^2C Pass-Through and Multiple Device Addressing.
		0	RSVD			Reserved.
0x0D	Slave ID[5]	7:1	Slave ID5	RW	0x00	This field stores the 7-bit I^2C address of remote slave 5, attached to the remote Serializer. If an I^2C transaction (originating from the Deserializer side) is addressed to Slave Alias5, the transaction will be remapped to this address before it is passed across the Bidirectional Control Channel to the remote Serializer, where it is then passed to remote slave 5. A value of 0 in this field disables I^2C access to remote slave 5. Refer to I^2C Pass-Through and Multiple Device Addressing.
		0	RSVD			Reserved.
0x0E	Slave ID[6]	7:1	Slave ID6	RW	0x00	This field stores the 7-bit I^2C address of remote slave 6, attached to the remote Serializer. If an I^2C transaction (originating from the Deserializer side) is addressed to Slave Alias6, the transaction will be remapped to this address before it is passed across the Bidirectional Control Channel to the remote Serializer, where it is then passed to remote slave 6. A value of 0 in this field disables I^2C access to remote slave 6. Refer to I^2C Pass-Through and Multiple Device Addressing.
		0	RSVD			Reserved.

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Addr (Hex)	Name	Bits	Field	R/W	Default (Hex)	Description
0x0F	Slave ID[7]	7:1	Slave ID7	RW	0x00	This field stores the 7-bit I²C address of remote slave 7, attached to the remote Serializer. If an I²C transaction (originating from the Deserializer side) is addressed to Slave Alias7, the transaction will be remapped to this address before it is passed across the Bidirectional Control Channel to the remote Serializer, where it is then passed to remote slave 7. A value of 0 in this field disables I²C access to remote slave 7. Refer to I²C Pass-Through and Multiple Device Addressing.
		0	RSVD			Reserved.
0x10	Slave Alias[0]	7:1	Slave Alias ID0	RW	0x00	This field stores a 7-bit I²C address. Once set, it configures the Deserializer to accept any transaction designated for the I²C address stored in this field. The transaction will then be remapped to the I²C address specified in the Slave ID0 register. A value of 0 in this field disables I²C access to remote slave 0. Refer to I²C Pass-Through and Multiple Device Addressing.
		0	RSVD			Reserved.
0x11	Slave Alias[1]	7:1	Slave Alias ID1	RW	0x00	This field stores a 7-bit I²C address. Once set, it configures the Deserializer to accept any transaction designated for the I²C address stored in this field. The transaction will then be remapped to the I²C address specified in the Slave ID1 register. A value of 0 in this field disables I²C access to remote slave 1. Refer to I²C Pass-Through and Multiple Device Addressing.
		0	RSVD			Reserved.
0x12	Slave Alias[2]	7:1	Slave Alias ID2	RW	0x00	This field stores a 7-bit I²C address. Once set, it configures the Deserializer to accept any transaction designated for the I²C address stored in this field. The transaction will then be remapped to the I²C address specified in the Slave ID2 register. A value of 0 in this field disables I²C access to remote slave 2. Refer to I²C Pass-Through and Multiple Device Addressing.
		0	RSVD			Reserved.
0x13	Slave Alias[3]	7:1	Slave Alias ID3	RW	0x00	This field stores a 7-bit I²C address. Once set, it configures the Deserializer to accept any transaction designated for the I²C address stored in this field. The transaction will then be remapped to the I²C address specified in the Slave ID3 register. A value of 0 in this field disables I²C access to remote slave 3. Refer to I²C Pass-Through and Multiple Device Addressing.
		0	RSVD			Reserved.
0x14	Slave Alias[4]	7:1	Slave Alias ID4	RW	0x00	This field stores a 7-bit I²C address. Once set, it configures the Deserializer to accept any transaction designated for the I²C address stored in this field. The transaction will then be remapped to the I²C address specified in the Slave ID4 register. A value of 0 in this field disables I²C access to remote slave 4. Refer to I²C Pass-Through and Multiple Device Addressing.
		0	RSVD			Reserved.

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Addr (Hex)	Name	Bits	Field	R/W	Default (Hex)	Description
0x15	Slave Alias[5]	7:1	Slave Alias ID5	RW	0x00	This field stores a 7-bit I²C address. Once set, it configures the Deserializer to accept any transaction designated for the I²C address stored in this field. The transaction will then be remapped to the I²C address specified in the Slave ID5 register. A value of 0 in this field disables I²C access to remote slave 5. Refer to I²C Pass-Through and Multiple Device Addressing.
		0	RSVD			Reserved.
0x16	Slave Alias[6]	7:1	Slave Alias ID6	RW	0x00	This field stores a 7-bit I²C address. Once set, it configures the Deserializer to accept any transaction designated for the I²C address stored in this field. The transaction will then be remapped to the I²C address specified in the Slave ID6 register. A value of 0 in this field disables I²C access to remote slave 6. Refer to I²C Pass-Through and Multiple Device Addressing.
		0	RSVD			Reserved.
0x17	Slave Alias[7]	7:1	Slave Alias ID7	RW	0x00	This field stores a 7-bit I²C address. Once set, it configures the Deserializer to accept any transaction designated for the I²C address stored in this field. The transaction will then be remapped to the I²C address specified in the Slave ID7 register. A value of 0 in this field disables I²C access to remote slave 7. Refer to I²C Pass-Through and Multiple Device Addressing.
		0	RSVD			Reserved.
0x18	Parity Errors Threshold	7:0	Parity Error Threshold Byte 0	RW	0x00	Parity errors threshold on the forward channel during normal information. This sets the maximum number of parity errors that can be counted using register 0x1A. Least significant Byte.
0x19	Parity Errors Threshold	7:0	Parity Error Threshold Byte 1	RW	0x01	Parity errors threshold on the forward channel during normal operation. This sets the maximum number of parity errors that can be counted using register 0x1B. Most significant Byte.
0x1A	Parity Errors	7:0	Parity Error Byte 0	RW	0x00	Number of parity errors in the forward channel during normal operation. Least significant Byte.
0x1B	Parity Errors	7:0	Parity Error Byte 1	RW	0x00	Number of parity errors in the forward channel during normal operation. Most significant Byte.
0x1C	General Status	7:4	Rev-ID	R		Revision ID. 0x0000: Production.
		3	RSVD			Reserved.
		2	Parity Error	R		Parity error detector. 1: At least one parity error detected. 0: No parity errors.
		1	Signal Detect	R		1: Serial input detected. 0: Serial input not detected.
		0	Lock	R		Deserializer's LOCK status. 1: Deserializer LOCKED to recovered clock. 0: Deserializer not LOCKED.

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Addr (Hex)	Name	Bits	Field	R/W	Default (Hex)	Description
0x1D	GPIO2 and GPIO3 Config	7	GPIO2 Output Value	RW	0x33	Local GPIO2 Output Value. This value is output on the GPIO2 pin when GPIO2 is enabled, and the local GPIO2 direction is set to output.
		6	RSVD			Reserved.
		5	GPIO2 Direction	RW		Local GPIO2 direction: 1: Input. 0: Output.
		4	GPIO2 Enable	RW		GPIO2 enable: 1: Enable GPIO2 operation. 0: TRI-STATE.
		3	GPIO3 Output Value	RW		Local GPIO3 Output Value. This value is output on the GPIO3 pin when GPIO3 is enabled, and the local GPIO3 direction is set to output.
		2	RSVD			Reserved.
		1	GPIO3 Direction	RW		Local GPIO3 direction: 1: Input. 0: Output.
		0	GPIO3 Enable	RW		GPIO3 enable: 1: Enable GPIO3 operation. 0: TRI-STATE.
0x1E	GPIO0 and GPIO1 Config	7	GPIO0 Output Value	RW	0x33	Local GPIO0 Output Value. This value is output on the GPIO0 pin when GPIO0 is enabled, and the local GPIO0 direction is set to output.
		6	RSVD			Reserved.
		5	GPIO0 Direction	RW		Local GPIO0 direction: 1: Input. 0: Output.
		4	GPIO0 Enable	RW		GPIO0 enable: 1: Enable GPIO0 operation. 0: TRI-STATE.
		3	GPIO1 Output Value	RW		Local GPIO1 Output Value. This value is output on the GPIO1 pin when GPIO1 is enabled, and the local GPIO1 direction is set to output.
		2	RSVD			Reserved.
		1	GPIO1 Direction	RW		Local GPIO1 direction: 1: Input. 0: Output.
		0	GPIO1 Enable	RW		GPIO1 enable: 1: Enable GPIO1 operation. 0: TRI-STATE.
0x1F	OEN and OSS Select	7	OEN_OSS Override	RW	0x00	Allows overriding OEN and OSS_SEL coming from pins. 1: Overrides OEN/OSS_SEL selected by pins. 0: Does NOT override OEN/OSS_SEL selected by pins.
		6	OEN Select	RW		OEN configuration register.
		5	OSS Select	R		OSS_SEL configuration register.
		4:0	RSVD			Reserved.
0x20	BCC Watchdog Control	7:1	BCC Watchdog Timer	RW	0xFE	The BCC Watchdog Timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog timeout value in units of 2ms. This field should not be set to 0.
		0	BCC Watchdog Timer Disable	RW		Bidirectional Control Channel Watchdog Timer enable. 1: Disables BCC Watchdog Timer operation. 0: Enables BCC Watchdog Timer operation.

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Addr (Hex)	Name	Bits	Field	R/W	Default (Hex)	Description
0x21	I²C Control 1	7	I²C Pass All	RW	0x17	Pass-through all I²C transactions. For an explanation of I²C pass-through, refer to I²C Pass-Through and Multiple Device Addressing. 1: Enable pass-through of all I²C accesses to I²C IDs that do not match the Deserializer I²C ID. The I²C accesses are then remapped to the address specified in register 0x06. 0: Enable pass-through only of I²C accesses to I²C IDs matching either the remote Serializer I²C ID or the remote slave I²C ID.
		6:4	I²C SDA Hold Time	RW		Internal SDA hold time. This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50ns.
		3:0	I²C Filter Depth	RW		I²C glitch filter depth. This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 10ns.
0x22	I²C Control 2	7	Forward Channel Sequence Error	R	0x00	Control channel sequence error detector. This bit indicates a sequence error has been detected in the forward control channel. 1: At least one error has occurred in the forward control channel. 0: No errors have been detected in the forward control channel.
		6	Clear Sequence Error	RW		Clears the Forward Channel Sequence Error bit.
		5	RSVD			Reserved.
		4:3	SDA Output Delay	RW		SDA output delay. This field configures the output delay on the SDA output. Setting this value will increase the output delay in units of 50 ns. Nominal output delay values for SCL to SDA are: 00: 350 ns 01: 400 ns 10: 450 ns 11: 500 ns
		2	Local Write Disable	RW		Disable remote writes to local registers. Setting this bit to 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Deserializer registers from an I²C Master attached to the Serializer. Setting this bit does not affect remote access to I²C slaves at the Deserializer.
		1	I²C Bus Timer Speedup	RW		Speed up I²C bus Watchdog Timer. 1: Watchdog Timer expires after approximately 50 microseconds. 0: Watchdog Timer expires after approximately 1 second.
		0	I²C Bus Timer Disable	RW		The I²C Watchdog Timer may be used to detect when the I²C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signaling occurs for approximately 1 second, the I²C bus is assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL. 1: Disable the I²C bus Watchdog Timer. 0: Enable the I²C bus Watchdog Timer.
0x23	General Purpose Control	7:0	GPCR[7:0]	RW	0x00	Scratch Register. Used to write and read 8 bits.

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Addr (Hex)	Name	Bits	Field	R/W	Default (Hex)	Description
0x24	BIST Control	7:4	RSVD		0x08	Reserved.
		3	BIST Pin Configuration	RW		BIST configuration select: 1: BIST configured through pin. 0: BIST configured through register bit 0x24[0].
		2:1	BIST Clock Source	RW		BIST clock source: See (Table 1)
		0	BIST Enable	RW		BIST register enable (active if 0x24[3] is set to 0): 1: Enabled. 0: Disabled.
0x25	Parity Error Count	7:0	BIST Error Count	R	0x00	Number of forward channel parity errors during the BIST.
0x3F	CML Output Enable	7:5	RSVD		0x10	Reserved.
		4	CML OUT Enable	RW		1: CML loop-through driver is powered down. 0: CML loop-through driver is powered up.
		3:0	RSVD			Reserved.
0x40	SCL High Time	7:0	SCL High Time	RW	0x82	I^2C Master SCL high time. This field configures the high pulse width of the SCL output when the Deserializer is the Master on the local I^2C bus. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to satisfy a minimum (4 µs + 0.3 µs of rise time for cases where rise time is very fast) SCL high time with the internal oscillator clock running at 26 MHz rather than the nominal 20 MHz.
0x41	SCL Low Time	7:0	SCL Low Time	RW	0x82	I^2C Master SCL low time. This field configures the low pulse width of the SCL output when the Deserializer is the Master on the local I^2C bus. This value is also used as the SDA setup time by the I^2C slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to satisfy a minimum (4.7 µs + 0.3 µs of fall time for cases where fall time is very fast) SCL low time with the internal oscillator clock running at 26 MHz rather than the nominal 20 MHz.
0x42	CRC Force Error	7:2	RSVD		0x00	Reserved.
		1	Force Back Channel Error	RW		1: This bit introduces multiple errors into the back channel frame. 0: No effect.
		0	Force One Back Channel Error	RW		1: This bit introduces ONLY one error into the back channel frame. This bit is also self clearing. 0: No effect.
0x4D	AEQ Test Mode Select	7	RSVD		0x20	Reserved.
		6	AEQ Bypass	RW		Bypass AEQ and use manual EQ. Set value using register 0x04.
		5:0	RSVD			Reserved.
0x4E	EQ Value	7:0	AEQ / Manual Eq Readback	R		Read back the equalization value (adaptive or manual).

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FUNCTIONAL DESCRIPTION

The DS90UA101-Q1/DS90UA102-Q1 chipset is intended to link digital audio sources with remote audio converters and DSPs. The chipset can operate from a reference clock of 10MHz to 50MHz. The DS90UA101-Q1 device serializes up to an 8 audio inputs and 4 general purpose inputs, along with a bidirectional control channel, into a single high-speed differential pair or single-ended coaxial cable. The high speed serial bit stream contains an embedded clock and DC-balanced information to enhance signal quality and support AC coupling. The DS90UA102-Q1 device receives the single serial data stream and converts it back to digital audio outputs, control channel data, and general purpose outputs (GPOs). The DS90UA101-Q1/DS90UA102-Q1 chipset can accept up to 8 audio data inputs, bit clock (BCK), word clock (LRCK), and an input reference clock (SCK) ranging from 10 MHz to 50 MHz.

The control channel function of the chipset provides bidirectional communication between the two ends of the link, such as a digital signal processor (DSP) on one end and an audio digital-analog converter (DAC) on the other. The integrated Bidirectional Control Channel transfers data bidirectionally over the same differential pair used for audio data interface. This interface offers advantages over other chipsets by eliminating the need for additional wires for programming and control. The Bidirectional Control Channel bus is controlled via an I^2C port, available on both the Serializer and Deserializer.

Transmission Media

The DS90UA101-Q1/DS90UA102-Q1 chipset is intended to be used in a point-to-point data link through a shielded twisted pair (STP) or coaxial (coax) cable. The Serializer and Deserializer provide internal termination to minimize impedance discontinuities. The interconnect (cable and connectors) should have a differential impedance of 100Ω, or a single-ended impedance of 50Ω. The maximum length of cable that can be used is dependent on the quality of the cable (gauge, impedance), connector, board (discontinuities, power plane), and the electrical environment (for example, power stability, ground noise, input clock jitter, SCK frequency, etc). The resulting signal quality at the receiving end of the transmission media may be assessed by monitoring the differential eye opening of the serial data stream. This can be done by measuring the output of the CMLOUTP/N pins. These pins should each be terminated with a 0.1 µF capacitor in series with a 50Ω resistor to GND. Figure 10 illustrates the minimum eye width and eye height that is necessary for bit error free operation.

Operation with Audio System Clock as Reference Clock

The DS90UA101-Q1/DS90UA102-Q1 chipset is operated using the audio system clock (SCK) from the digital audio source. The audio data, LRCK, and BCK inputs are clocked into the Serializer using SCK. Up to 4 GPI inputs are also sampled and transported along with the digital audio inputs. Figure 13 shows the operation of the Serializer and Deserializer with the reference clock.

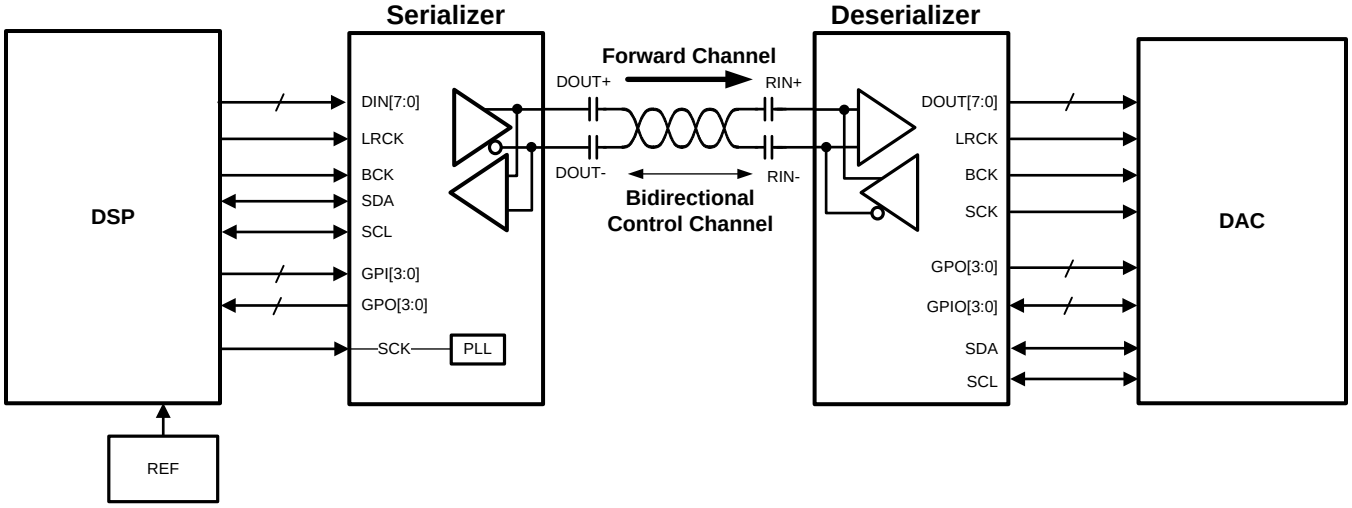


Figure 13. Operation with SCK Reference

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The Serializer switches over to an internal reference clock when SCK is idle or missing. This frequency is selectable via the device control registers, as shown below (Table 1).

Table 1. Internal Oscillator Frequencies for Forward Channel Frame during Normal Operation

DS90UA101-Q1 Reg 0x14 [2:1]	Frequency (MHz)
00	~25
01	~50
10	~25
11	~12.5

Line Rate Calculations for the DS90UA101-Q1/DS90UA102-Q1

The following formula is used to calculate the line rate for the DS90UA101-Q1/DS90UA102-Q1 chipset:

- Line rate = f_{SCK} * 28

For example, for maximum line rate, f_{SCK}= 50 MHz, line rate = 50 * 28 = 1.4 Gbps.

Serial Frame Format

The high speed forward channel is composed of 28 bits of data containing digital audio data, sync signals, I^2C and parity bits. This data payload is optimized for signal transmission over an AC-coupled link. Data is randomized, balanced and scrambled. The Bidirectional Control Channel data is transferred over the single serial link along with the high-speed forward data. This architecture provides a full duplex, low speed control path across the serial link together with the high speed forward channel.

Serial Audio Formats

There are several de-facto industry standards or formats that define the required alignments and signal polarities between the left/right clock (LRCK), bit clock (BCK) and the serial audio data. Hence, this section is dedicated to discussing various serial audio formats.

I^2S Format

An I^2S bus uses three signal lines for data transfer – a frame or word clock (LRCK), a bit clock (BCK), and a single or multiple data lines. The device which generates the appropriate BCK and LRCK signals on the bus is called Master, whereas other devices which accept BCK and LRCK as inputs are all slaves.

Bit Clock (BCK)

The bit clock pulses once for each discrete bit of data on the data lines. The bit clock frequency must be greater than or equal to the product of the sample rate, the number of bits per sample and the number of channels (which is 2 in normal stereo operation).

Word Select (LRCK)

The word select line indicates the channel being transmitted:

- LRCK = 0; channel 1 (left);
- LRCK = 1; channel 2 (right).

The LRCK line changes one clock period before the MSB is transmitted (Figure 14). This allows the slave transmitter to derive synchronous timing of the serial data that will be set up for transmission. Furthermore, it enables the receiver to store the previous word and clear the input for the next word.

Serial Data (DATA)

Serial data is transmitted in two's complement with the MSB first (as shown in Figure 14). The MSB is transmitted first because the transmitter and receiver may have different word lengths.

If the receiver is sent more bits than its word length, the bits after the LSB are ignored. On the other hand, if the receiver is sent fewer bits than its word length, the missing bits are set to zero internally. And so, the MSB has a fixed position, whereas the position of the LSB depends on the word length.

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Serial data sent by the transmitter may be synchronized with either the trailing (HIGH-to-LOW) or the leading (LOW-to-HIGH) edge of the clock signal. However, the serial data must be latched into the receiver on the leading edge of the serial clock signal, and so there are some restrictions when transmitting data that is synchronized with the leading edge.

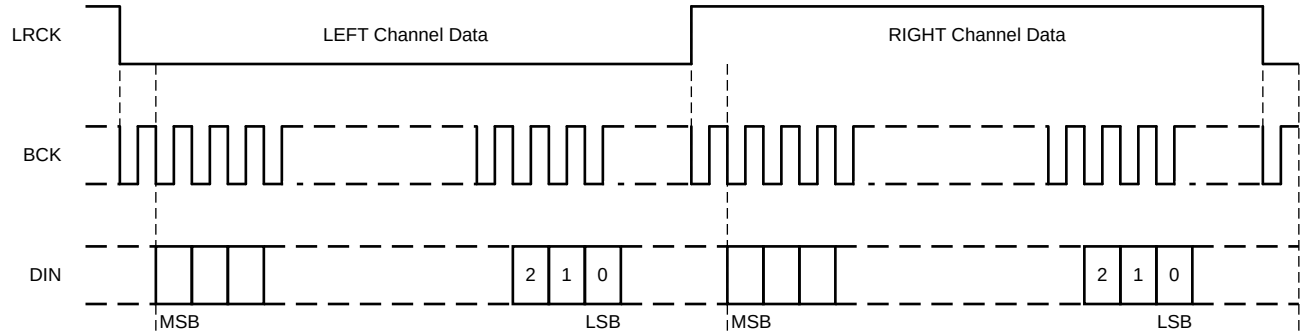


Figure 14. Stereo I²S Format

Left Justified Format

In this format, MSB of the word appears in synchronization with the LRCK edges. Unlike in I²S mode, there is no lag between Data and LRCK. Left channel data word begins at falling edge of LRCK and right channel data word begins on rising edge of the LRCK signal. Hence, as can be seen from below waveforms (Figure 15), data appears to be left justified.

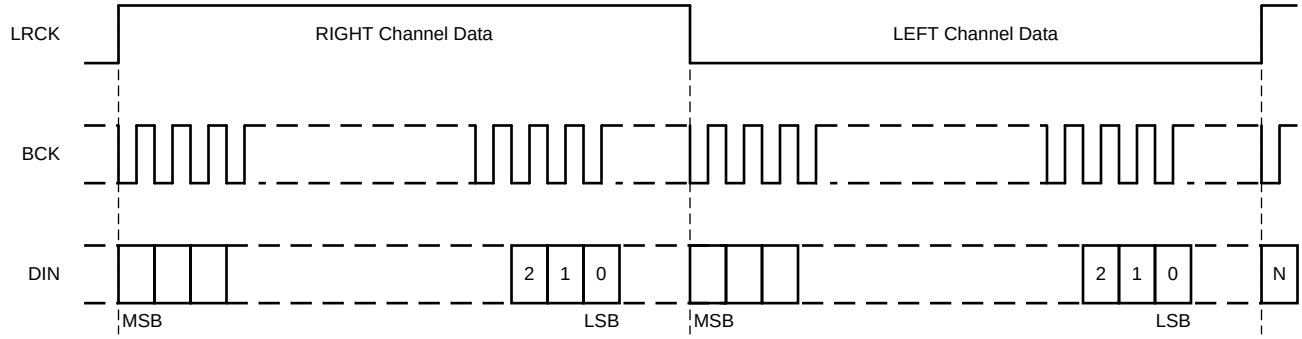


Figure 15. Left-Justified Format

Right Justified Format

In this format, LSB of the word appears just before the LRCK edges. Left channel data word may begin at any point depending upon the word length, but LSB of this data word must appear just before the rising edge of the LRCK signal. Similarly, LSB of the right channel data word must appear just before falling edge of the LRCK signal. Hence, as can be seen from below waveforms(Figure 16), data appears to be right justified.

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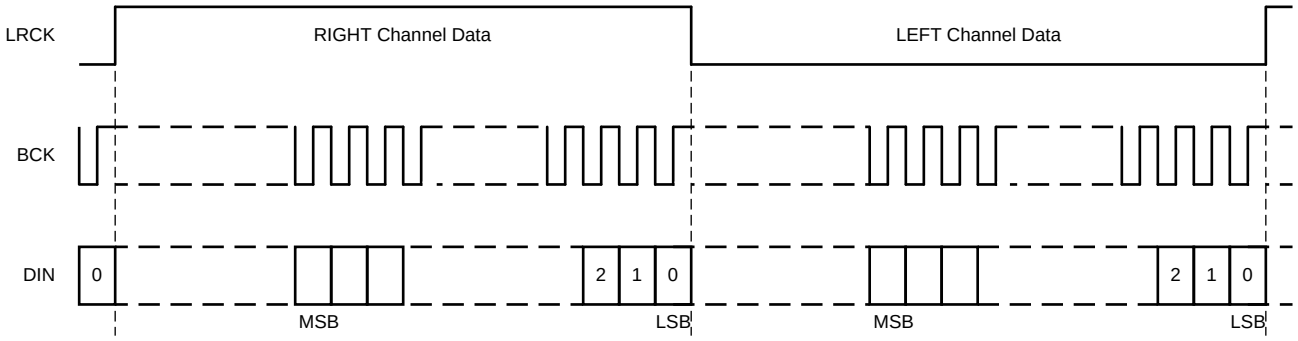


Figure 16. Right-Justified Format

TDM Format

There are no well defined rules for TDM format and it can be implemented in large number of ways depending upon the word length, bit clock, number of channels to be multiplexed, etc. For example, let's assume that word clock signal (LRCK) period = 256 * bit clock (BCK) time period. In this case, we can multiplex 4 channels with maximum word length of 64 bits each, or 8 channels with maximum word length of 32 bits each. Figure 17 illustrates the multiplexing of 8 channels with 24 bit word length, in a format similar to I^2S.

Pulse width of LRCK can be used to define a clock period for BCK or to define a slot period, i.e., the period for which individual channel can be active on the shared data line.

If the number of audio channels is more than 8, DS90UA101-Q1/DS90UA102-Q1 can easily support multiplexed data with additional devices to multiplex and de-multiplex the data. The number of channels multiplexed on each data line must be selected as a power of 2, that is, 2/ 4/ 8.

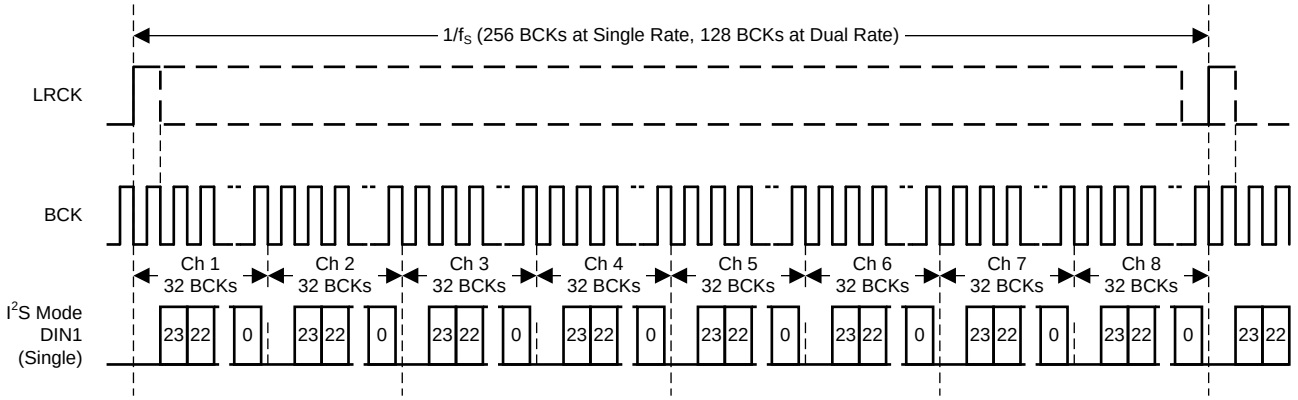


Figure 17. TDM Format

Error Detection

The chipset provides error detection operations for validating data integrity in long distance transmission and reception. The data error detection function offers users flexibility and usability of performing bit-by-bit data transmission error checking. The error detection operating modes support data validation of the following signals:

- Bidirectional Control Channel data across the serial link
- Parallel audio/sync data across the serial link

The chipset provides 1 parity bit on the forward channel and 4 CRC bits on the back channel for error detection purposes. The DS90UA101-Q1/DS90UA102-Q1 chipset checks the forward and back channel serial links for errors and stores the number of detected errors in two 8-bit registers in the Serializer and the Deserializer, respectively.

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To check parity errors on the forward channel, monitor registers 0x1A and 0x1B on the Deserializer. If there is a loss of LOCK, then the counters on registers 0x1A and 0x1B are reset. Whenever there is a parity error on the forward channel, the PASS pin will go low momentarily.

To check CRC errors on the back-channel, monitor registers 0x0A and 0x0B on the Serializer.

Bidirectional Control Bus and I²C

The I²C compatible interface allows programming of the Serializer, Deserializer, or an external remote device through the Bidirectional Control Channel. For example, an audio module connected to the Deserializer can communicate with the ADC connected to the Serializer using the Bidirectional Control Channel. Register programming transactions to/from the chipset are employed through the clock (SCL) and data (SDA) lines. These two signals have open drain I/Os and both lines must be pulled-up to V_{DDIO} by an external resistor. Pull-up resistors or current sources are required on the SCL and SDA busses to pull them high when they are not being driven low. A logic LOW is transmitted by driving the output low. Logic HIGH is transmitted by releasing the output and allowing it to be pulled-up externally. The appropriate pull-up resistor values will depend upon the total bus capacitance and operating speed. The DS90UA101-Q1/DS90UA102-Q1 I²C bus data rate supports up to 400 kbps according to I²C fast mode specifications. Figure 18, Figure 19, Figure 20, Figure 21 show I²C waveforms of read/write bytes, basic operation, and start/stop conditions.

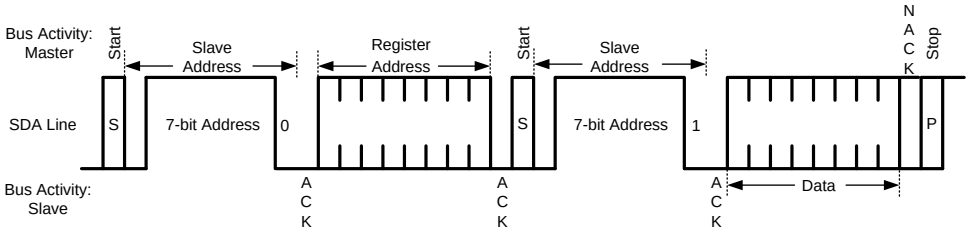


Figure 18. Read Byte

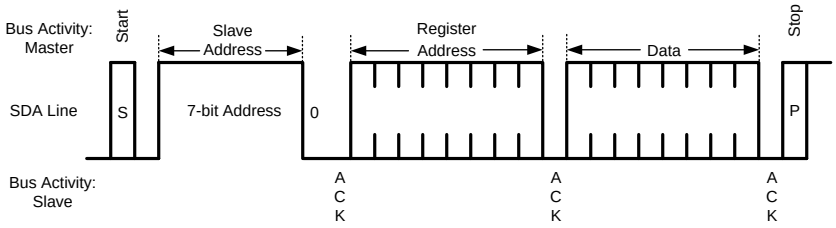


Figure 19. Write Byte

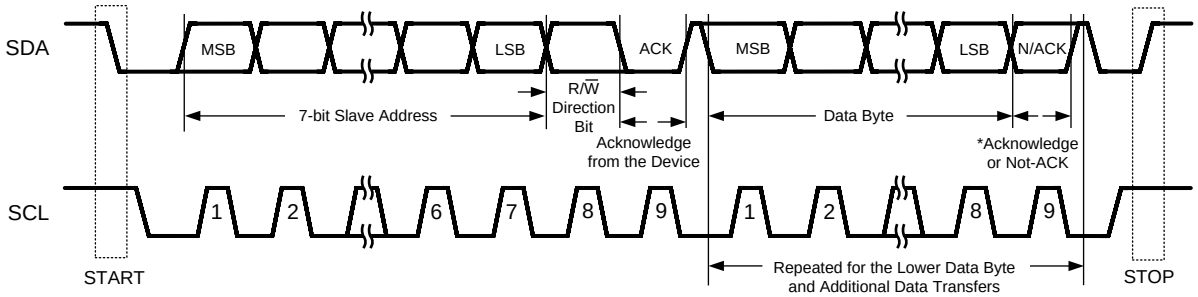


Figure 20. Basic Operation

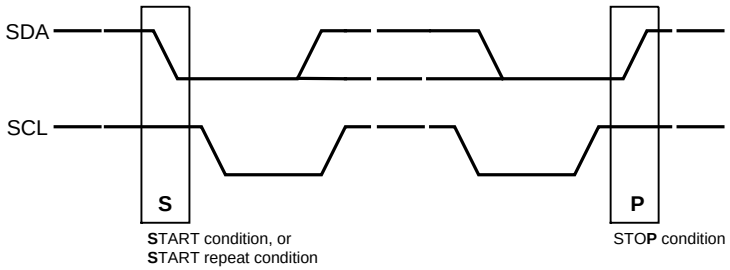


Figure 21. Start and Stop Conditions

IDx Address Decoder on the Deserializer

The IDx pin (Figure 22) on the Deserializer is used to decode and set the I^2C address of the Deserializer. There are 4 possible I^2C addresses that can be set on the Deserializer. The pin must be pulled to V_{DD} (1.8V, not V_{DDIO}) with a 10 kΩ resistor and a pull down resistor R_{ID}) of the recommended value to set the I^2C address of the Deserializer (Table 2). The recommended maximum resistor tolerance is 1%.

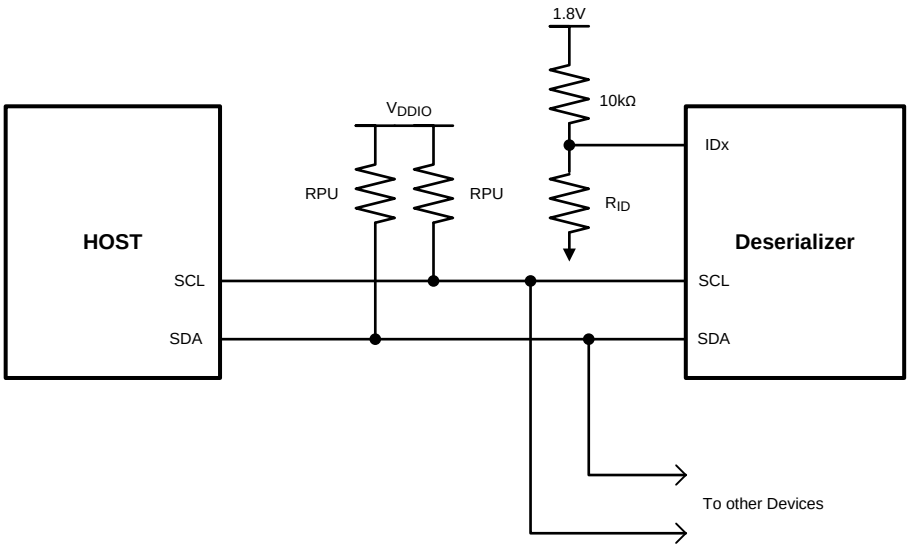


Figure 22. IDx Address Select

Table 2. Resistor Values for IDx on DS90UA102-Q1 Deserializer

IDx Resistor Value		
Resistor RID (kΩ) (1%Tolerance)	**7-Bit Address**	**8-Bit Address (0 appended)**
0	0x60	0xC0
3	0x61	0xC2
11	0x62	0xC4
100	0x63	0xC6

Note: The I^2C address of the Deserializer can also be set using 0x00[7:1] once 0x00[0] is set to 1.

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I²C Pass-Through

I²C pass-through is the feature that provides a way to access remote devices at the other end of the serial interface. For example, when the I²C Master is connected to the Deserializer and I²C pass-through is enabled on the Deserializer, any I²C traffic targeted for the remote Serializer or remote slave will be allowed to pass through the Deserializer to reach those respective devices.

See Figure 23 for an example of this function:

- If Master (DSP) transmits an I²C transaction for SER A, then DES A with I²C pass-through enabled will transfer that I²C command to SER A. Responses from SER A will travel from SER A --> DES A --> DSP.
- If Master transmits an I²C transaction for address 0xA0, then DES A with I²C pass-through enabled will transfer that I²C command to SER A, which will then transfer it to remote slave Device A. Responses from Device A will travel from Device A --> SER A --> DES A --> DSP.
- As for DES B with I²C pass-through disabled, any I²C commands for SER B or Device B will NOT be passed on the I²C bus to SER B/Device B.

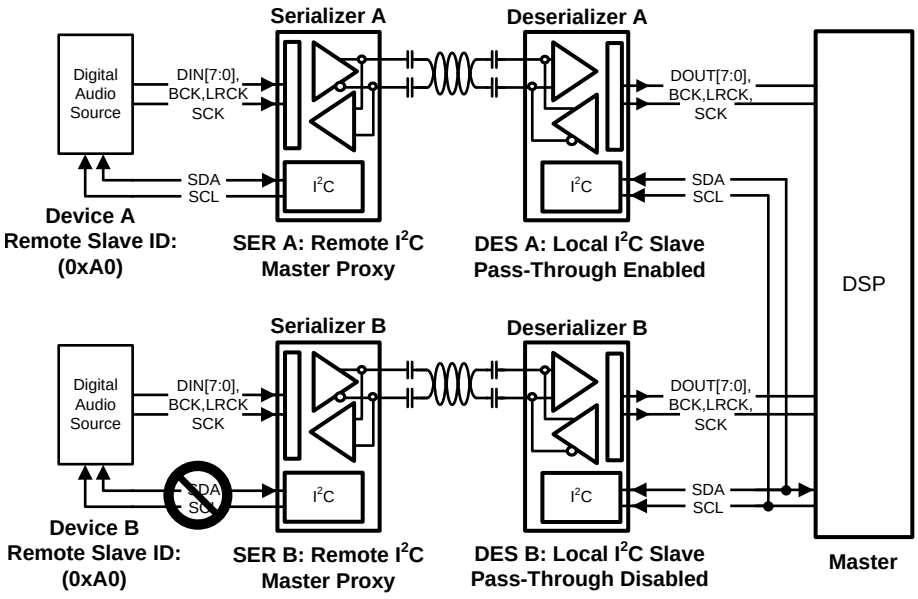


Figure 23. I²C Pass-Through

To setup I²C pass-through on the Serializer, set 0x03[2] = 1 and configure registers 0x06, 0x07, 0x08, and 0x09 as needed (Deserializer I²C ID, Deserializer Alias ID, remote slave I²C ID, remote slave Alias ID, respectively). Refer to Multiple Device Addressing for information about Alias IDs and refer to DS90UA102-Q1 REGISTER INFORMATION for information to set these registers. To communicate with the remote Deserializer from the Serializer side, registers 0x06 and 0x07 must be configured (register 0x06 is auto-loaded by default if there is LOCK). To communicate with the remote slave connected to the remote Deserializer, configure registers 0x08 and 0x09.

To setup I²C pass-through on the Deserializer, set 0x03[3] = 1 and configure registers 0x06 - 0x17 as needed. To communicate with the remote Serializer from the Deserializer side, registers 0x06 and 0x07 must be configured (register 0x06 is auto-loaded by default if there is LOCK). To communicate with one or more remote slaves connected to the remote Serializer, configure 0x08 - 0x17 accordingly.

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Multiple Device Addressing

Some applications require multiple devices with the same fixed address to be accessed on the same I^2C bus. The DS90UA101-Q1/DS90UA102-Q1 provides slave ID aliasing to generate different target slave addresses when connecting two or more identical devices remotely. Instead of addressing their actual I^2C addresses, each remote device can be addressed through a unique alias ID by programming the Slave Alias ID register on the Serializer/Deserializer. By addressing the Slave Alias IDs, I^2C slaves with identical, fixed addresses can now be addressed independently. On the DS90UA101-Q1, up to 1 Slave Alias ID index is supported. On the DS90UA102-Q1, up to 8 Slave Alias IDs can be supported. The Audio Module/DSP (I^2C Master) must keep track of the alias list in order to properly address the correct device.

Refer to Figure 24 for an example of this function:

- There is a local I^2C bus between Audio Module, DES A, and DES B. Audio Module is the I^2C Master, and DES A and DES B are I^2C slaves.
- The I^2C protocol is bridged from DES A to SER A and from DES B to SER B. SER A is the master of its own local I^2C bus, and Source A and its µC/EEPROM are slaves on this bus. SER B is also the master of its local I^2C bus, and Source B and its µC/EEPROM are the slaves.
- Audio Module can now address remote slaves connected to SER A and SER B independently.
- Case 1: If Audio Module transmits to I^2C slave 0xA0, DES A (address 0xC0) will forward the transaction to SER A, which then forwards it to remote slave Source A. Responses from Source A will travel from Source A --> SER A --> DES A --> Audio Module.
- Case 2: If Audio Module transmits to slave address 0xA4, DES B (address 0xC2) will recognize that 0xA4 is mapped to 0xA0 and will transmit the command to SER B, which then forwards it to remote slave Source B. Responses from Source B will travel from Source B --> SER B --> DES B --> Audio Module.
- Case 3: If Audio Module sends command to address 0xA6, DES B (address 0xC2) will forward the transaction to SER B, which then forwards it to Source B's µC/EEPROM. Responses from Source B's µC/EEPROM will travel from Source B's µC/EEPROM --> SER B --> DES B --> Audio Module.

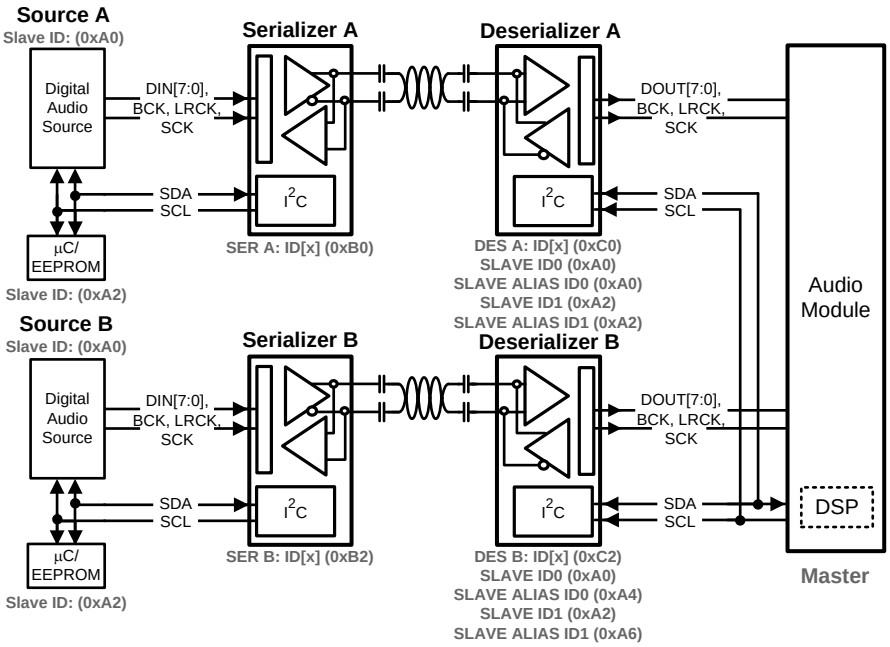


Figure 24. Multiple Device Addressing

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NOTE

Note: The alias ID must be set in order to communicate with any remote device. For example:

- When there is only one SER/DES pair and no remote slaves: if I^2C Master on the DES side wants to communicate with the remote SER, I^2C pass-through must be enabled on the DES and the SER Alias ID must also be set before the I^2C Master can communicate with the remote SER (the SER ID is automatically configured by default if there is LOCK).
- When there is only one SER/DES pair and one remote slave connected to the SER: if I^2C Master on the DES side (with pass-through enabled) wants to communicate with the remote slave, the Slave ID and Slave Alias ID must be set before the I^2C Master can communicate with the remote slave, even if there is only one remote slave.

Slave Clock Stretching

To communicate and synchronize with remote devices on the I^2C bus through the Bidirectional Control Channel, the chipset utilizes bus clock stretching (holding the SCL line low) during data transmission. On the 9th clock of every I^2C transfer (before the ACK signal), the local I^2C slave pulls the SCL line low until a response is received from the remote I^2C bus located on the other end of the serial interface. The slave device will not control the clock and only stretches it until the remote peripheral has responded. The I^2C Master must support slave clock stretching in order to communicate with remote devices.

General Purpose Inputs, Outputs (GPIs, GPOs, GPIOs) Descriptions

There are 4 dedicated general purpose inputs (GPIs) on the DS90UA101-Q1 and 4 dedicated general purpose outputs (GPOs) on the DS90UA102-Q1. Inputs to the GPI pins on the Serializer are fed to the GPO outputs on the Deserializer. The maximum GPI data rate is defined by the SCK source (up to 50 Mbps).

In addition, there are also 4 GPOs on the DS90UA101-Q1 and 4 GPIOs on the DS90UA102-Q1. The GPOs on the Serializer can be configured as outputs for the input signals that are fed into the Deserializer GPIOs. The GPIO maximum data rate is up to 66 kbps when configured for communication between Deserializer GPIO to Serializer GPO. Both the GPOs on the Serializer and GPIOs on the Deserializer can also behave as outputs whose values are set from local registers.

LVCMOS V_{DDIO} Option

1.8V/3.3V Deserializer outputs are user configurable to provide compatibility with 1.8V and 3.3V system interfaces.

Power Up Requirements and PDB Pin

The Deserializer is active when the PDB pin is driven HIGH. Driving the PDB pin LOW powers down the device and clears all control register configurations to default values. The PDB pin must be held low until the power supplies (V_{DDn} and V_{DDIO}) have settled to the recommended operating voltage. This can be done by driving PDB externally, or an external RC network can be connected to the PDB pin to ensure PDB arrives after all the power supplies have stabilized.

Powerdown

The PDB pin's function on the Deserializer is to ENABLE or powerdown the device. This pin can be controlled by the system and can be used to disable the DES to save power. When PDB = HIGH, the DES will lock to the input stream and assert the LOCK pin (HIGH) and output valid data. When PDB = LOW, all outputs are in TRI-STATE.

SCK Clock Edge Select (RRFB)

The RRFB selects which edge of the output clock that the data is strobed on. If RRFB register is 1, data is strobed on the rising edge of SCK. If RRFB register is 0, data is strobed on the falling edge of SCK.

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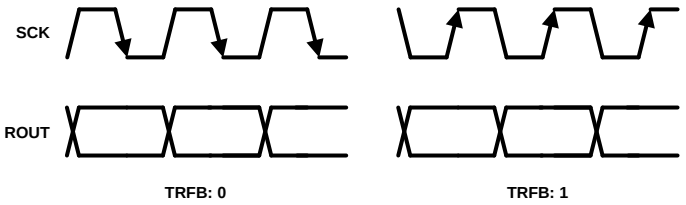


Figure 25. Programmable SCK Strobe Select

Built In Self Test (BIST)

An optional at-speed built in self test (BIST) feature supports the testing of the high speed serial link and low-speed back channel. This is useful in the prototype stage, equipment production, and in-system test and also for system diagnostics.

BIST Configuration and Status

The DS90UA101-Q1/DS90UA102-Q1 chipset can be programmed into BIST mode using either pins or registers. By default BIST configuration is controlled through pins on the DS90UA102-Q1. BIST can be configured via registers using BIST Control Register 0x24, also on the DS90UA102-Q1. Pin based configuration is defined as follows:

- BISTEN (on DS90UA102-Q1) = HIGH: Enable the BIST mode, BISTEN = LOW: Disable the BIST mode.
- GPIO3 and GPIO2 of DS90UA102-Q1: Defines the BIST clock source (SCK vs. various internal oscillator frequencies). See Table 3 below.

Table 3. BIST Pin Configuration on DS90UA102-Q1 Deserializer(1)

DS90UA102-Q1 Deserializer GPIO[3:2]	Oscillator Source	BIST Frequency (MHz)
00	External	SCK
01	Internal	~25
10	Internal	~50
11	Internal	~12.5

(1) Note: These pin settings will only be active when 0x24[3] = 1 and BIST is on.

The BIST mode provides various options for the clock source. Either external pins (GPIO3 and GPIO2 of DES) or register 0x24 on DES can be used to configure the BIST to use SCK or various internal oscillator frequencies as the clock source. Refer to Table 4 below for BIST register settings.

Table 4. BIST Register Configuration on DS90UA102-Q1 Deserializer(1)

DS90UA102-Q1 Deserializer 0x24[2:1]	Oscillator Source	BIST Frequency (MHz)
00	External	SCK
01	Internal	~50
10	Internal	~25
11	Internal	~12.5

(1) Note: These register settings will only be active when 0x24[3] = 0 and BIST is on.

The BIST status can be monitored real time on the PASS pin. For every frame with error(s), the PASS pin toggles low momentarily. If two consecutive frames have errors, PASS will toggle twice to allow counting of frames with errors. Once the BIST is done, the PASS pin reflects the pass/fail status momentarily (pass = no errors, fail = one or more errors). The BIST result can also be read through I^2C for the number of frames that errored. The status register retains results until it is reset by a new BIST session or a device reset. For all practical purposes, the BIST status can be monitored from the BIST Error Count Register 0x25 on the DS90UA102-Q1 Deserializer.

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Sample BIST Sequence (Refer to Figure 26)

Step 1: BIST mode is enabled via the BISTEN pin on the DS90UA102-Q1 Deserializer, or through the Deserializer control registers. The clock source is selected through the GPIO3 and GPIO2 pins as shown in Table 3.

Step 2: The DS90UA101-Q1 Serializer BIST start command is activated through the back channel.

Step 3: The BIST pattern is generated and sent through the serial interface to the Deserializer. Once the Serializer and Deserializer are in the BIST mode and the Deserializer acquires LOCK, the PASS pin of the Deserializer goes high and BIST starts checking the data stream. If an error in the payload is detected the PASS pin will switch low momentarily. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step 4: To stop the BIST mode, the Deserializer BISTEN pin is set low and the Deserializer stops checking the data. The final test result is not maintained on the PASS pin. To check the number of BIST errors, check the BIST Error Count register, 0x25 on the Deserializer. The link returns to normal operation after the Deserializer BISTEN pin is low.

Figure 27 below shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases, it is difficult to generate errors due to the robustness of the link (differential data transmission, adaptive equalization, etc.), thus they may be introduced by greatly extending the cable length, increasing the frequency, or by reducing signal condition enhancements (Rx equalization).

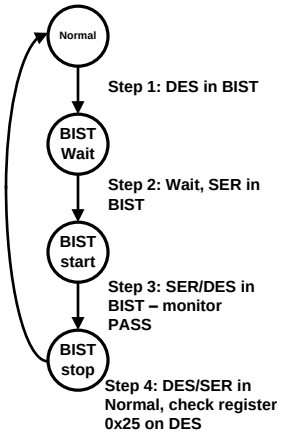


Figure 26. AT-Speed BIST System Flow Diagram

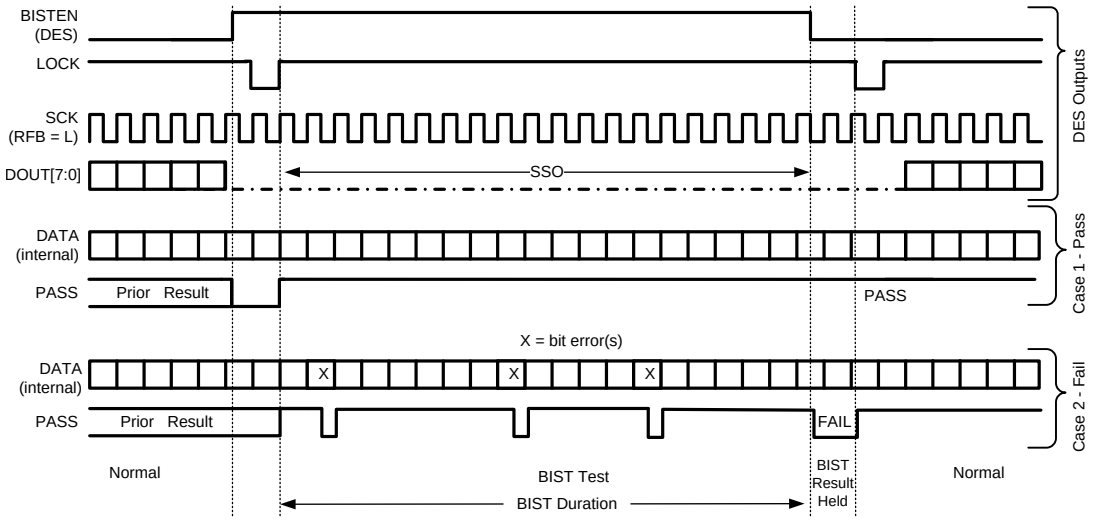


Figure 27. BIST Timing Diagram

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Clock-Data Recovery Status Flag (LOCK), Output Enable (OEN) and Output State Select (OSS_SEL)

When PDB is driven HIGH, the Deserializer's CDR PLL begins locking to the serial input. After the DS90UA102-Q1 completes its LOCK sequence to the input serial data, the LOCK output is driven HIGH, indicating valid data and clock have been recovered from the serial input and are available on the parallel bus and SCK outputs. The states of the outputs are based on the serial interface input to the Deserializer, OEN, and OSS_SEL setting as shown below (Table 5). See Figure 11.

Table 5. Output States(1)(2)

Inputs				Outputs			
Serial Interface Input to DES	**PDB**	**OEN**	**OSS_SEL**	**LOCK**	**PASS**	**DATA**	**SCK**
X	0	X	X	Z	Z	Z	Z
X	1	0	0	L or H	L	L	L
X	1	0	1	L or H	Z	Z	Z
Static	1	1	0	L	L	L	L/Internal Oscillator (Register bit enable 0x02[5])
Static	1	1	1	L	H	L	L
Active	1	1	0	H	L	L	L
Active	1	1	1	H	Valid	Valid	Valid

(1) X: Don't Care.
(2) Z: TRI-STATE.

Deserializer – Adaptive Input Equalization(AEQ)

The receiver inputs provide an adaptive input equalization filter in order to compensate for signal degradation from the interconnect components. The level of equalization can also be manually selected via register controls. The equalized output can be seen using the CMLOUTP/CMLOUTN pins on the Deserializer.

There are limits to the amount of loss that can be compensated. These limits are defined by the gain curve of the equalizer shown in Figure 28. This figure illustrates the maximum allowable interconnect loss for coax/STP cable with the equalizer at various gain settings. In order to determine the maximum cable reach, other factors that affect signal integrity such as jitter, skew, ISI, crosstalk, etc. need to be taken into consideration.

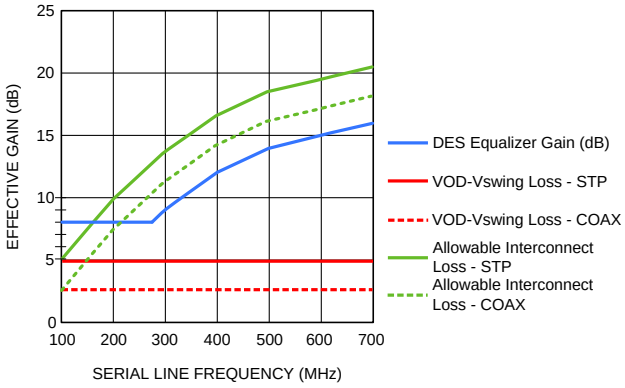


Figure 28. Maximum Equalizer Gain vs. Line Frequency (STP)

EMI Reduction : Deserializer Staggered Output

The receiver staggers output switching to provide a random distribution of transitions within a defined window. Output transitions are distributed randomly. This minimizes the number of outputs switching simultaneously and helps to reduce supply noise. In addition it spreads the noise spectrum out reducing overall EMI.

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APPLICATIONS INFORMATION

AC Coupling

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced coding scheme. External AC coupling capacitors must be placed in series with the serial interface signal path as illustrated in Figure 29 or Figure 30. Applications utilizing STP cable require a 0.1 µF coupling capacitor on both outputs (DOUT+, DOUT–). Applications utilizing single-ended 50Ω coaxial cable require a 0.1 µF capacitor on the true serial interface output (DOUT+). The unused data pin (DOUT-) requires a 0.0 47 µF capacitor coupled to a 50Ω resistor to GND.

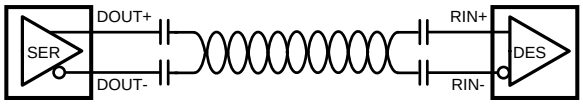


Figure 29. AC-Coupled Connection (STP)

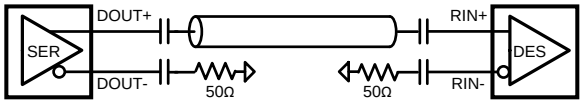


Figure 30. AC-Coupled Connection (Coaxial)

For high-speed serial transmissions, the smallest available package should be used for the AC coupling capacitor. This will help minimize degradation of signal quality due to package parasitics.

Typical Application Connection

Figure 31 and Figure 32 show typical application connections of the DS90UA102-Q1 Deserializer. The serial interface inputs must have external 0.1 µF coupling capacitors connected to the high-speed interconnect. The Deserializer has internal termination.

Bypass capacitors are placed near the power supply pins. Ferrite beads should also be used for effective noise suppression. The digital audio electrical interface is LVCMOS format. The V_{DDIO} pin may be connected to 3.3V or 1.8V. Device I^2C address select is configured via the IDx pin.

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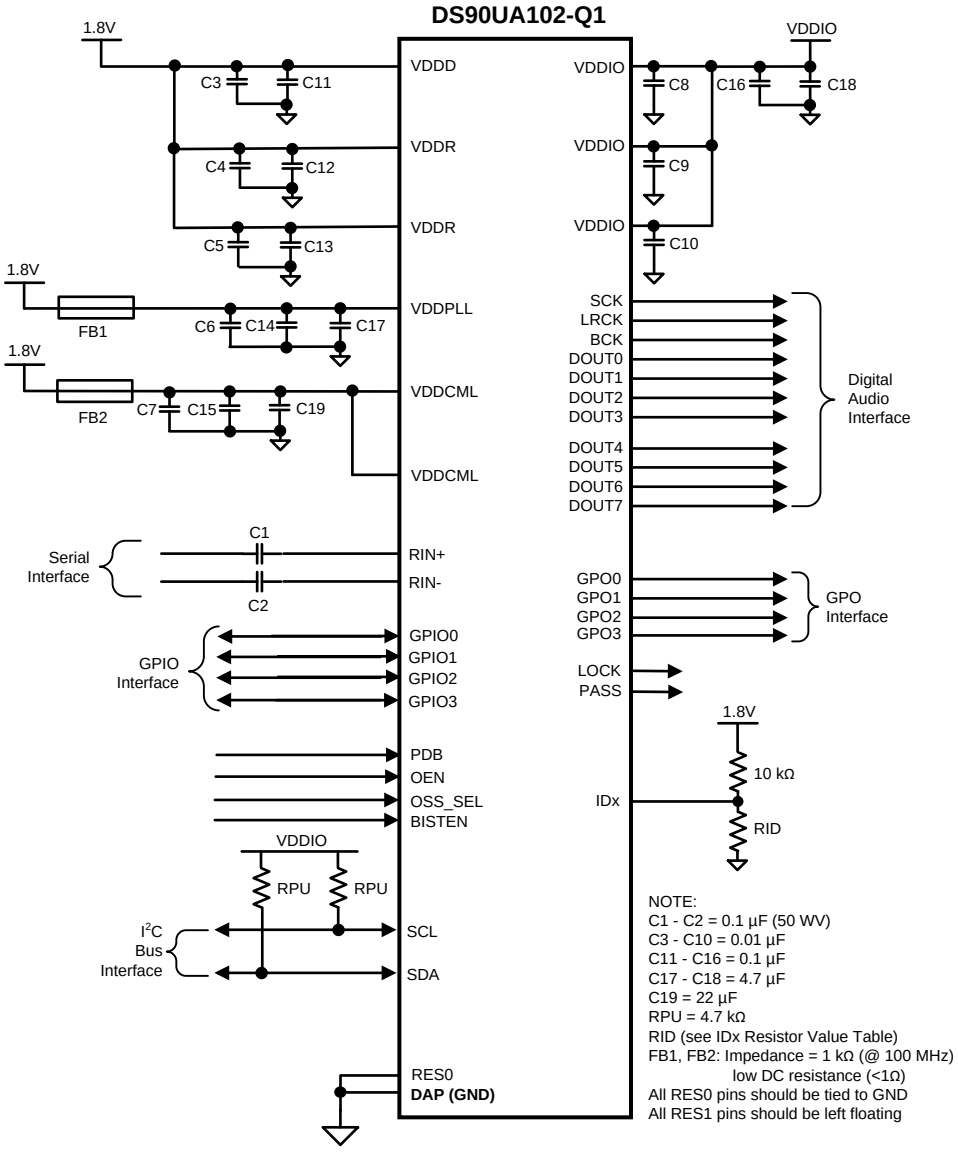


Figure 31. Typical Connection Diagram (STP Cable)

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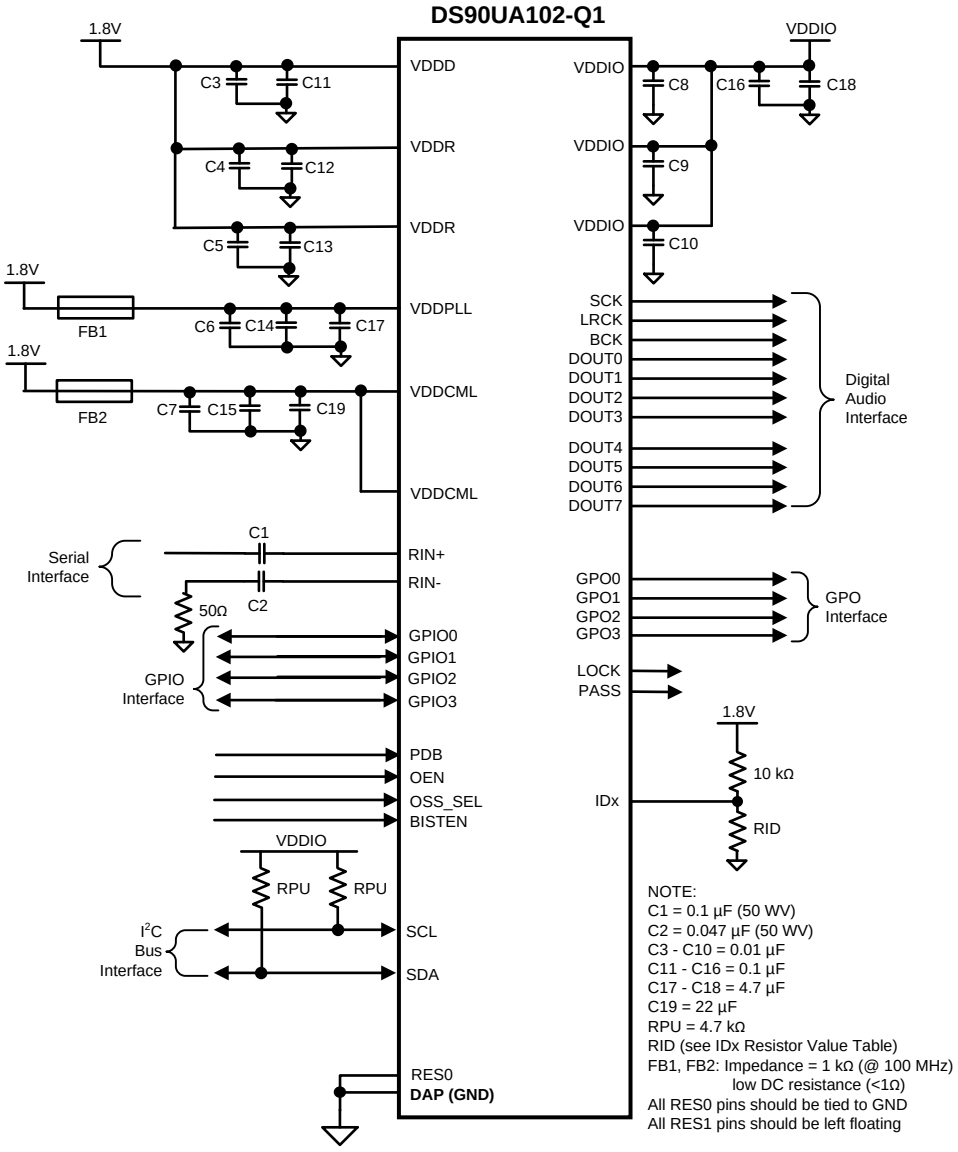


Figure 32. Typical Connection Diagram (Coax Cable)

PCB Layout and Power System Considerations

Circuit board layout and stack-up for the Ser/Des devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 µF to 0.1 µF. Tantalum capacitors may be in the 2.2 µF to 10 µF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

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Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50 µF to 100uF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines. Closely-coupled differential lines of 100Ω are typically recommended for differential interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the LLP style package is provided in TI Application Note AN-1187.

Interconnect Guidelines

See AN-1108 and AN-905 for full details.

- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - – S = space between the pair
  - – 2S = space between pairs
  - – 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500 Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the Texas Instrument web site at: www.ti.com/lvds

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90UA102TRHSJQ1	ACTIVE	WQFN	RHS	48	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UA102Q	Samples
DS90UA102TRHSRQ1	ACTIVE	WQFN	RHS	48	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UA102Q	Samples
DS90UA102TRHSTQ1	ACTIVE	WQFN	RHS	48	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UA102Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

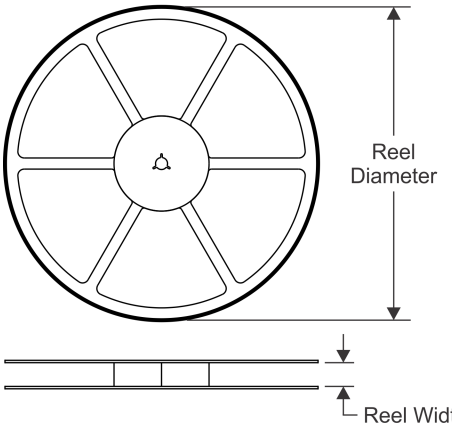
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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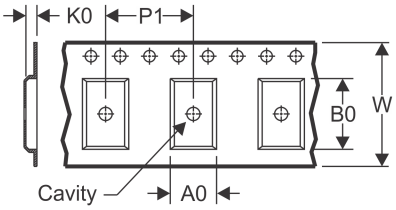
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

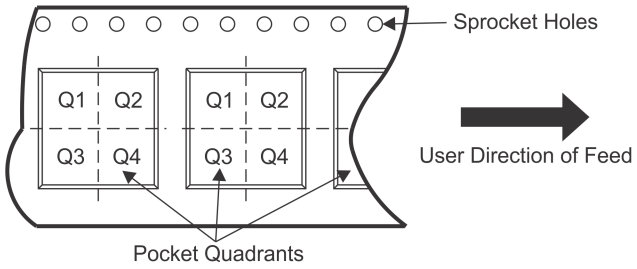


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

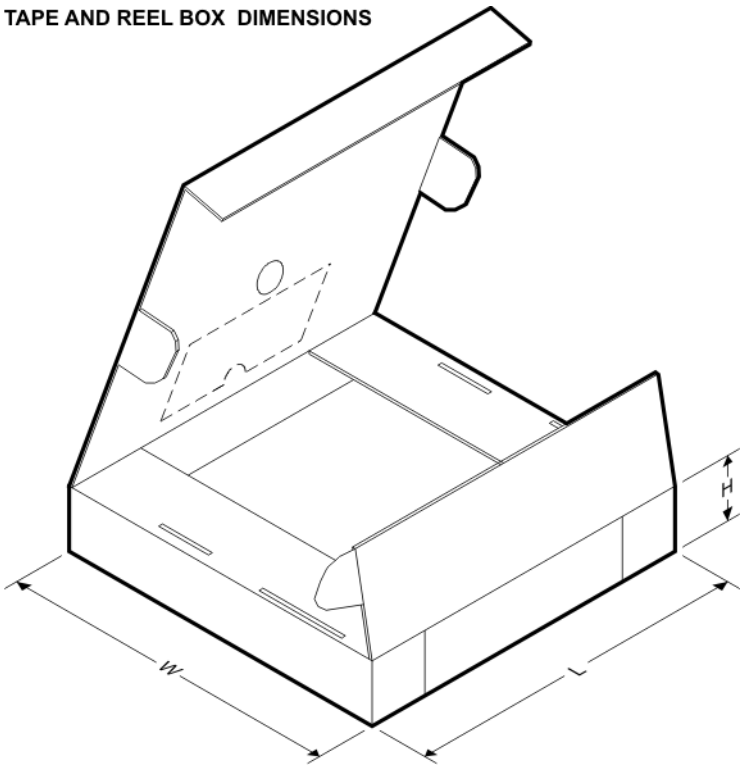
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UA102TRHSJQ1	WQFN	RHS	48	2500	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS90UA102TRHSRQ1	WQFN	RHS	48	1000	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS90UA102TRHSTQ1	WQFN	RHS	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

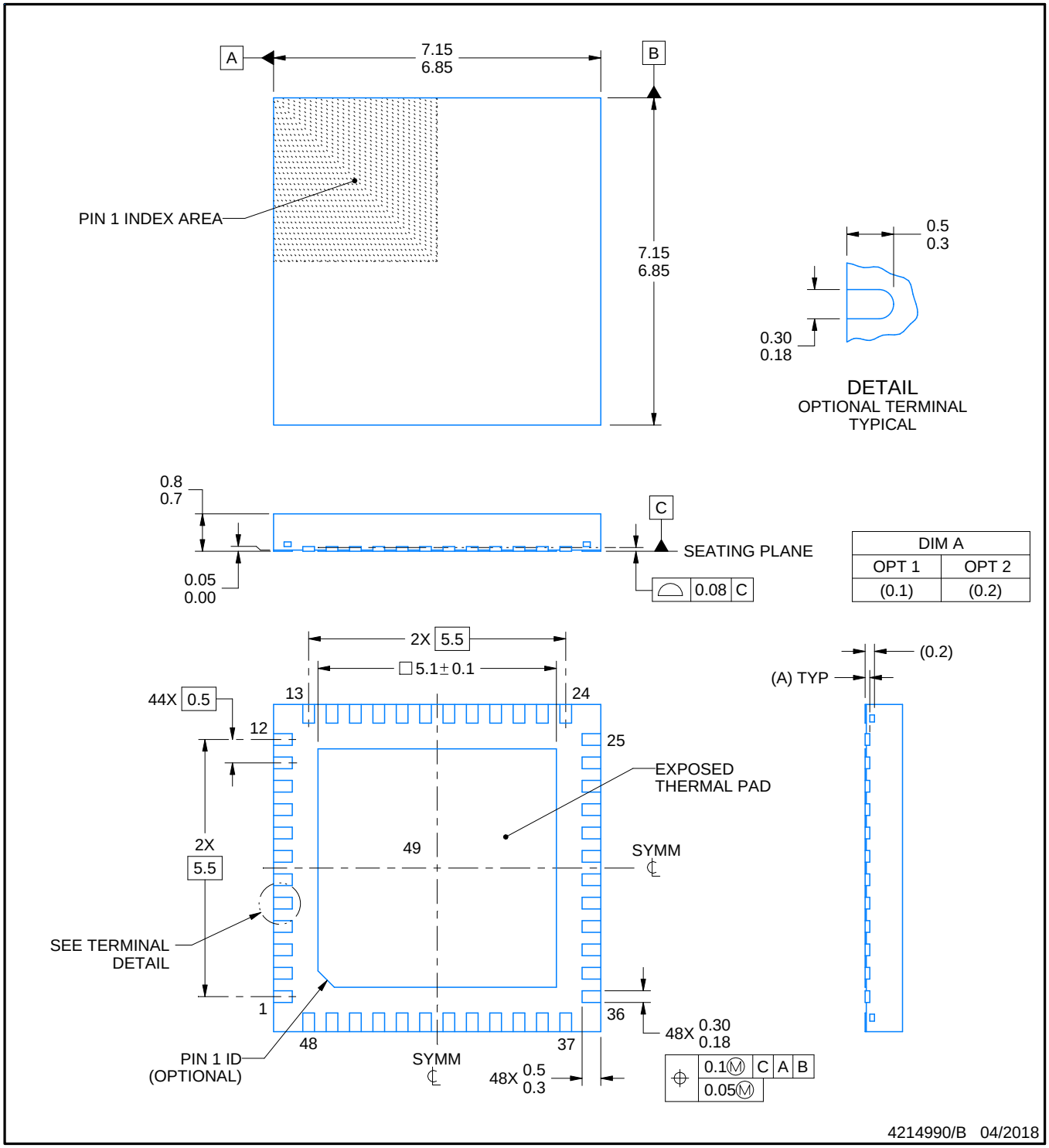
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UA102TRHSJQ1	WQFN	RHS	48	2500	853.0	449.0	35.0
DS90UA102TRHSRQ1	WQFN	RHS	48	1000	853.0	449.0	35.0
DS90UA102TRHSTQ1	WQFN	RHS	48	250	208.0	191.0	35.0

PACKAGE OUTLINE

RHS0048A

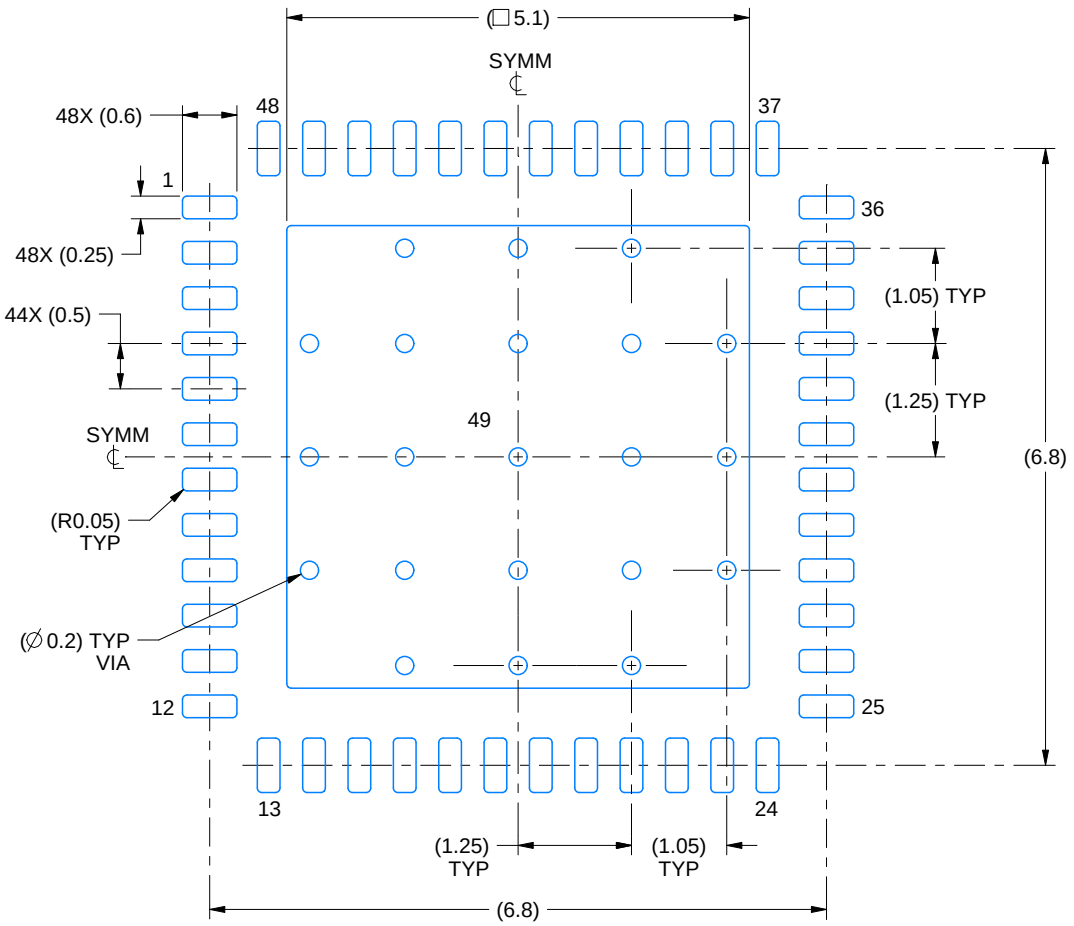
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

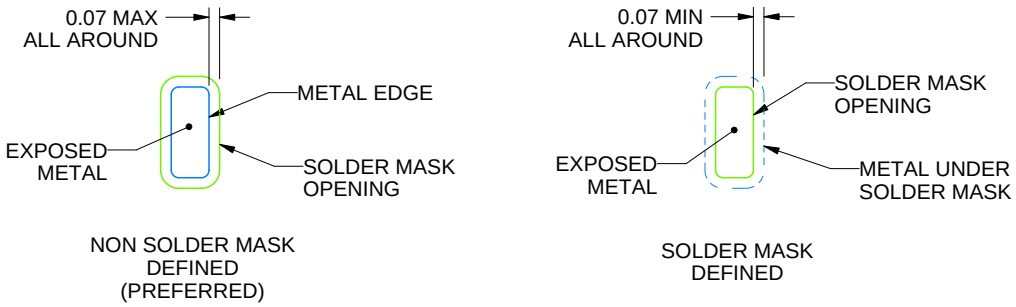


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

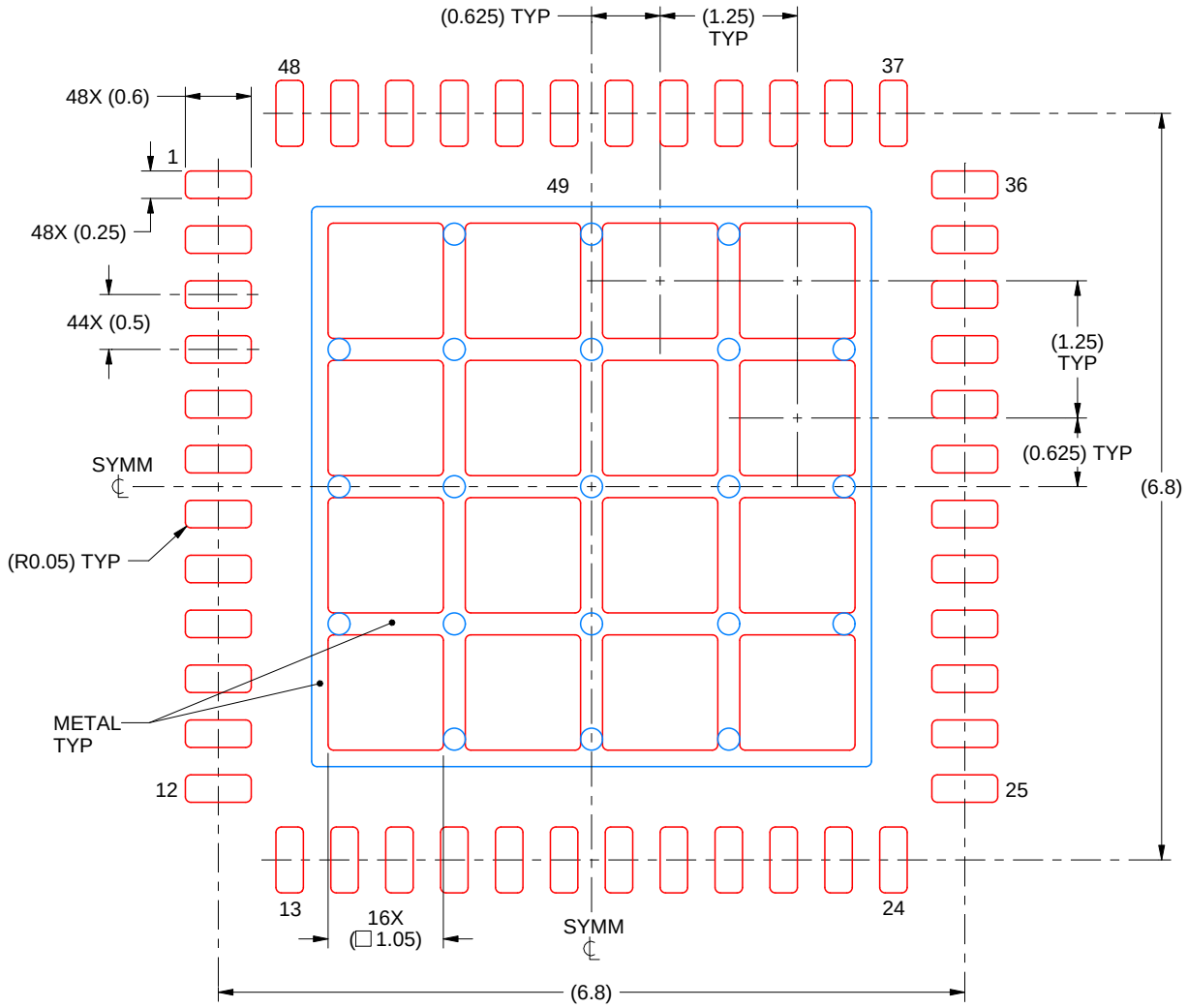


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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