TLV431x 低电压可调节精密并联稳压器

1 特性

- 低电压运行，V_{REF} = 1.24V
- 可调节输出电压，V_O = V_{REF} 至 6V
- 25°C 温度下的基准电压容差
  - TLV431B 为 0.5%
  - TLV431A 为 1%
  - TLV431 为 1.5%
- 温度漂移典型值
  - 4mV（0°C 至 70°C）
  - 6mV（–40°C 至 85°C）
  - 11mV（–40°C 至 125°C）
- 低阴极工作电流，典型值为 80μA
- 0.25Ω 输出阻抗典型值
- 超小型 SC-70 封装可提供比 SOT-23-3 小 40% 的尺寸
- 请参阅 TLVH431 和 TLVH432，以了解以下特性：
  - 更宽的 V_{KA}（1.24V 至 18V）和 I_K (80mA)
  - 额外的 SOT-89 封装
  - 适用于 SOT-23-3 和 SOT-89 封装的多个引脚
- 对于符合 MIL-PRF-38535 标准的产品，所有参数均经过测试，除非另外注明。对于所有其他产品，生产流程不一定包含对所有参数的测试。

2 应用

- 可调节电压和电流基准
- 反激式开关模式电源 (SMPS) 中的二次侧稳压
- 齐纳二极管替代产品
- 电压监视
- 具有集成式基准的比较器

3 说明

TLV431 器件是低电压 3 端子可调节电压基准，在适用的工业和商业级温度范围内具有指定的热稳定性。可以通过两个外部电阻器将输出电压设置为介于 V_{REF} (1.24V) 和 6V 之间的任何值（请参阅*参数测量信息* 部分）。这些器件具有比广泛使用的 TL431 和 TL1431 并联稳压器基准电压更低的工作电压 (1.24V)。

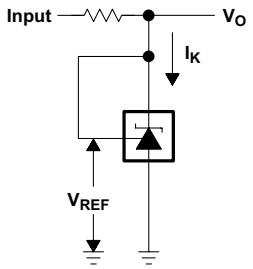
与光耦合器配合使用时，TLV431 器件是适用于 3V 至 3.3V 开关模式电源的隔离式反馈电路中的理想电压基准。其输出阻抗典型值均为 0.25Ω。有源输出电路可提供非常急剧的导通特性，从而使它们在许多 应用中成为低电压齐纳二极管的出色替代产品，这些应用包括板载稳压和可调节电源。

器件信息(1)

器件型号	封装（引脚）	封装尺寸（标称值）
TLV431x	SOT-23 (3)	2.90mm x 1.30mm
	SOT-23 (5)	2.90mm × 1.60mm
	SC70 (6)	2.00mm × 1.25mm
	TO-92 (3)	4.30mm × 4.30mm
	SOIC (8)	4.90mm × 3.90mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

Changes from Revision W (March 2018) to Revision X **Page**

- Changed figure 18 ... 14

Changes from Revision V (January 2015) to Revision W **Page**

- 更改了“说明”部分中的交叉参考链接 *说明* ... 1
- Changed the *Stability Boundary Conditions* graph ... 13
- Added the *Phase Margin vs Capacitive Load* $V_{KA} = V_{REF}$ *(1.25 V),* T_A*= 25°C* graph ... 14
- Added the *Phase Margin vs Capacitive Load* V_{KA} *= 2.50 V,* T_A*= 25°C* graph ... 14
- Added the *Phase Margin vs Capacitive Load* V_{KA} *= 5.00 V,* T_A*= 25°C* graph ... 15
- 添加了 *文档支持* 部分 ... 25
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- 添加了 *社区资源* 部分 ... 25

Changes from Revision U (January 2014) to Revision V **Page**

- 添加了 *应用*、*器件信息* 表、*引脚功能* 表、*ESD 额定值* 表、*热性能信息* 表、*特性* *说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分。 ... 1

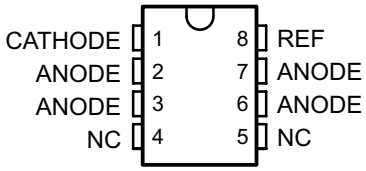
Changes from Revision T (June 2007) to Revision U **Page**

- 将文档更新为新的 TI 数据表格式。 ... 1
- 已删除 删除了 *订购信息* 表。 ... 1
- 已更新 *特性* 部分）。 ... 1

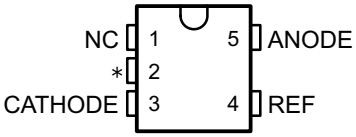
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5 Pin Configuration and Functions

D (SOIC) PACKAGE
(TOP VIEW)

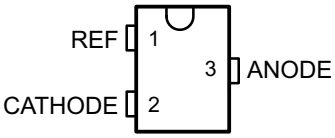


DBV (SOT-23-5) PACKAGE
(TOP VIEW)

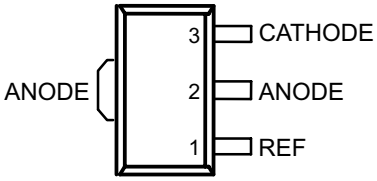


NC − No internal connection
∗ For TLV431, TLV431A: NC − No internal connection
∗ For TLV431B: Pin 2 is attached to Substrate and must be connected to ANODE or left open.

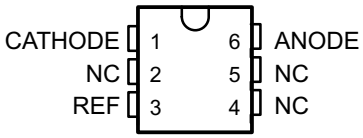
DBZ (SOT-23-3) PACKAGE
(TOP VIEW)



PK (SOT-89) PACKAGE
(TOP VIEW)

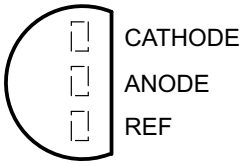


DCK (SC-70) PACKAGE
(TOP VIEW)



NC − No internal connection

LP (TO-92/TO-226) PACKAGE
(TOP VIEW)



Pin Functions

PIN							TYPE	DESCRIPTION
NAME	DBZ	DBV	PK	D	LP	DCK		
CATHODE	2	3	3	1	1	1	I/O	Shunt Current/Voltage input
REF	1	4	1	8	3	3	I	Threshold relative to common anode
ANODE	3	5	2	2, 3, 6, 7	2	6	O	Common pin, normally connected to ground
NC	—	1	—	4, 5	—	2, 4, 5	I	No Internal Connection
*	—	2	—	—	—	—	I	Substrate Connection

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{KA}	Cathode voltage(2)		7	V
I_K	Continuous cathode current	–20	20	mA
I_{ref}	Reference current	–0.05	3	mA
	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to the anode terminal, unless otherwise noted.

6.2 ESD Ratings

PARAMETER		DEFINITION	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{KA}	Cathode voltage		V_{REF}	6	V
I_K	Cathode current		0.1	15	mA
T_A	Operating free-air temperature	TLV431_C	0	70	°C
		TLV431_I	–40	85	
		TLV431_Q	–40	125	

6.4 Thermal Information

THERMAL METRIC(1)		TLV431x						UNIT
		DCK	D	PK	DBV	DBZ	LP	
		6 PINS	8 PINS	3 PINS	5 PINS	3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87	97	52	206	206	140	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	259	39	9	131	76	55	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

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6.5 Electrical Characteristics for TLV431

at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLV431 MIN	TLV431 TYP	TLV431 MAX	UNIT
V_{REF}	Reference voltage	$V_{KA} = V_{REF}$, I_K = 10 mA	T_A = 25°C		1.222	1.24	1.258	V
			T_A = full range(1) (see Figure 22)	TLV431C	1.21		1.27	
				TLV431I	1.202		1.278	
				TLV431Q	1.194		1.286	
$V_{REF(dev)}$	V_{REF} deviation over full temperature range(2)	$V_{KA} = V_{REF}$, I_K = 10 mA(1) (see Figure 22)		TLV431C		4	12	mV
				TLV431I		6	20	
				TLV431Q		11	31	
$\frac{\Delta V_{REF}}{\Delta V_{KA}}$	Ratio of V_{REF} change in cathode voltage change	$V_{KA} = V_{REF}$ to 6 V, I_K = 10 mA (see Figure 23)				–1.5	–2.7	mV/V
I_{ref}	Reference terminal current	I_K = 10 mA, R1 = 10 kΩ, R2 = open (see Figure 23)				0.15	0.5	µA
$I_{ref(dev)}$	I_{ref} deviation over full temperature range(2)	I_K = 10 mA, R1 = 10 kΩ, R2 = open(1) (see Figure 23)		TLV431C		0.05	0.3	µA
				TLV431I		0.1	0.4	
				TLV431Q		0.15	0.5	
$I_{K(min)}$	Minimum cathode current for regulation	$V_{KA} = V_{REF}$ (see Figure 22)		TLV431C/I		55	80	µA
				TLV431Q		55	100	
$I_{K(off)}$	Off-state cathode current	V_{REF} = 0, V_{KA} = 6 V (see Figure 24)				0.001	0.1	µA
$\|z_{KA}\|$	Dynamic impedance(3)	$V_{KA} = V_{REF}$, f ≤ 1 kHz, I_K = 0.1 mA to 15 mA (see Figure 22)				0.25	0.4	Ω

(1) Full temperature ranges are –40°C to 125°C for TLV431Q, –40°C to 85°C for TLV431I, and 0°C to 70°C for TLV431C.

(2) The deviation parameters $V_{REF(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, αV_{REF}, is defined as:

$$\left|\alpha V_{REF}\right|\left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{REF(dev)}}{V_{REF}\left(T_A = 25°C\right)}\right) \times 10^6}{\Delta T_A}$$

where ΔT_A is the rated operating free-air temperature range of the device.

αV_{REF} can be positive or negative, depending on whether minimum V_{REF} or maximum V_{REF}, respectively, occurs at the lower temperature.

(3) The dynamic impedance is defined as $|z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$

When the device is operating with two external resistors (see Figure 23), the total dynamic impedance of the circuit is defined as:

$$|z_{ka}|' = \frac{\Delta V}{\Delta I} \approx |z_{ka}| \times \left(1 + \frac{R1}{R2}\right)$$

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6.6 Electrical Characteristics for TLV431A

at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLV431A			UNIT
					MIN	TYP	MAX	
V_{REF}	Reference voltage	$V_{KA} = V_{REF}$, I_K = 10 mA	T_A = 25°C		1.228	1.24	1.252	V
			T_A = full range[1] (see Figure 22)	TLV431AC	1.221		1.259	
				TLV431AI	1.215		1.265	
				TLV431AQ	1.209		1.271	
$V_{REF(dev)}$	V_{REF} deviation over full temperature range[2]	$V_{KA} = V_{REF}$, I_K = 10 mA[1] (see Figure 22)		TLV431AC		4	12	mV
				TLV431AI		6	20	
				TLV431AQ		11	31	
$\frac{\Delta V_{REF}}{\Delta V_{KA}}$	Ratio of V_{REF} change in cathode voltage change	$V_{KA} = V_{REF}$ to 6 V, I_K = 10 mA (see Figure 23)				–1.5	–2.7	mV/V
I_{ref}	Reference terminal current	I_K = 10 mA, R1 = 10 kΩ, R2 = open (see Figure 23)				0.15	0.5	µA
$I_{ref(dev)}$	I_{ref} deviation over full temperature range[2]	I_K = 10 mA, R1 = 10 kΩ, R2 = open[1] (see Figure 23)		TLV431AC		0.05	0.3	µA
				TLV431AI		0.1	0.4	
				TLV431AQ		0.15	0.5	
$I_{K(min)}$	Minimum cathode current for regulation	$V_{KA} = V_{REF}$ (see Figure 22)		TLV431AC/AI		55	80	µA
				TLV431AQ		55	100	
$I_{K(off)}$	Off-state cathode current	V_{REF} = 0, V_{KA} = 6 V (see Figure 24)				0.001	0.1	µA
$\|z_{KA}\|$	Dynamic impedance[3]	$V_{KA} = V_{REF}$, f ≤ 1 kHz, I_K = 0.1 mA to 15 mA (see Figure 22)				0.25	0.4	Ω

(1) Full temperature ranges are –40°C to 125°C for TLV431Q, –40°C to 85°C for TLV431I, and 0°C to 70°C for TLV431C.

(2) The deviation parameters $V_{REF(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, αV_{REF}, is defined as:

$$\left|\alpha V_{REF}\right|\left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{REF(dev)}}{V_{REF}\left(T_A = 25°C\right)}\right) \times 10^6}{\Delta T_A}$$

where ΔT_A is the rated operating free-air temperature range of the device.

αV_{REF} can be positive or negative, depending on whether minimum V_{REF} or maximum V_{REF}, respectively, occurs at the lower temperature.

(3) The dynamic impedance is defined as $|z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$

When the device is operating with two external resistors (see Figure 23), the total dynamic impedance of the circuit is defined as:

$$|z_{ka}|' = \frac{\Delta V}{\Delta I} \approx |z_{ka}| \times \left(1 + \frac{R1}{R2}\right)$$

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6.7 Electrical Characteristics for TLV431B

at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLV431B MIN	TLV431B TYP	TLV431B MAX	UNIT
V_{REF}	Reference voltage	$V_{KA} = V_{REF}$, I_K = 10 mA	T_A = 25°C		1.234	1.24	1.246	V
			T_A = full range[1] (see Figure 22)	TLV431BC	1.227		1.253	
				TLV431BI	1.224		1.259	
				TLV431BQ	1.221		1.265	
$V_{REF(dev)}$	V_{REF} deviation over full temperature range[2]	$V_{KA} = V_{REF}$, I_K = 10 mA[1] (see Figure 22)		TLV431BC		4	12	mV
				TLV431BI		6	20	
				TLV431BQ		11	31	
$\frac{\Delta V_{REF}}{\Delta V_{KA}}$	Ratio of V_{REF} change in cathode voltage change	$V_{KA} = V_{REF}$ to 6 V, I_K = 10 mA (see Figure 23)				–1.5	–2.7	mV/V
I_{ref}	Reference terminal current	I_K = 10 mA, R1 = 10 kΩ, R2 = open (see Figure 23)				0.1	0.5	µA
$I_{ref(dev)}$	I_{ref} deviation over full temperature range[2]	I_K = 10 mA, R1 = 10 kΩ, R2 = open[3] (see Figure 23)		TLV431BC		0.05	0.3	µA
				TLV431BI		0.1	0.4	
				TLV431BQ		0.15	0.5	
$I_{K(min)}$	Minimum cathode current for regulation	$V_{KA} = V_{REF}$ (see Figure 22)				55	100	µA
$I_{K(off)}$	Off-state cathode current	V_{REF} = 0, V_{KA} = 6 V (see Figure 24)				0.001	0.1	µA
$\lvert z_{KA} \rvert$	Dynamic impedance[4]	$V_{KA} = V_{REF}$, f ≤ 1 kHz, I_K = 0.1 mA to 15 mA (see Figure 22)				0.25	0.4	Ω

(1) Full temperature ranges are –40°C to 125°C for TLV431Q, –40°C to 85°C for TLV431I, and 0°C to 70°C for TLV431C.

(2) The deviation parameters $V_{REF(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, αV_{REF}, is defined as:

$$\left|\alpha V_{REF}\right|\left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{REF(dev)}}{V_{REF}\left(T_A = 25°C\right)}\right) \times 10^6}{\Delta T_A}$$

where ΔT_A is the rated operating free-air temperature range of the device.

αV_{REF} can be positive or negative, depending on whether minimum V_{REF} or maximum V_{REF}, respectively, occurs at the lower temperature.

(3) Full temperature ranges are –40°C to 125°C for TLV431Q, –40°C to 85°C for TLV431I, and 0°C to 70°C for TLV431C.

(4) The dynamic impedance is defined as $\left|z_{ka}\right| = \frac{\Delta V_{KA}}{\Delta I_K}$

When the device is operating with two external resistors (see Figure 23), the total dynamic impedance of the circuit is defined as:

$$\left|z_{ka}\right|' = \frac{\Delta V}{\Delta I} \approx \left|z_{ka}\right| \times \left(1 + \frac{R1}{R2}\right)$$

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6.8 Typical Characteristics

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

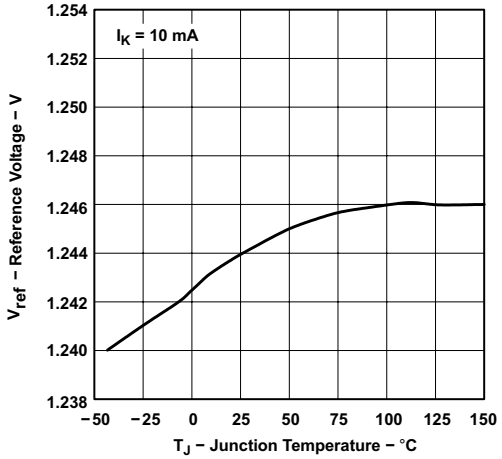


Figure 1. Reference Voltage vs Junction Temperature

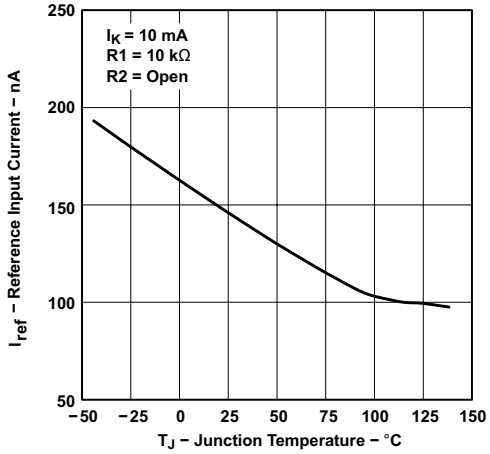


Figure 2. Reference Input Current vs Junction Temperature (for TLV431 and TLV431A)

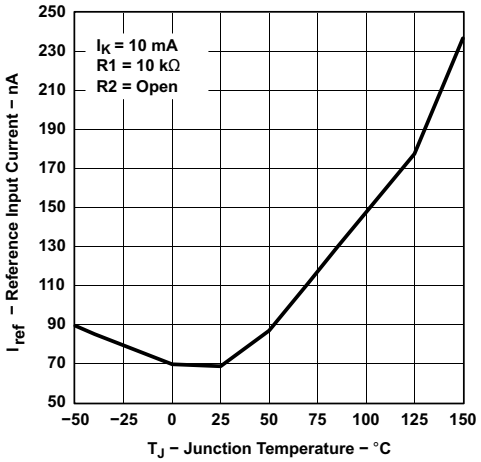


Figure 3. Reference Input Current vs Junction Temperature (for TLV431B)

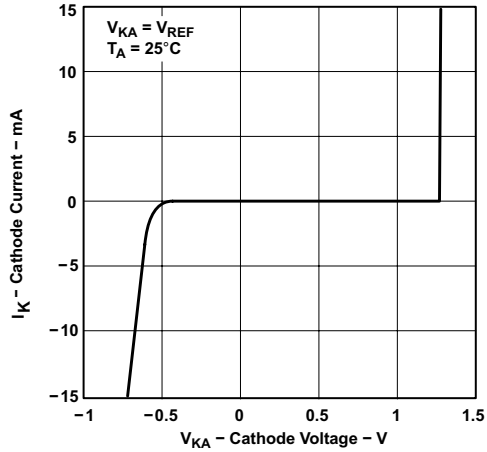


Figure 4. Cathode Current vs Cathode Voltage

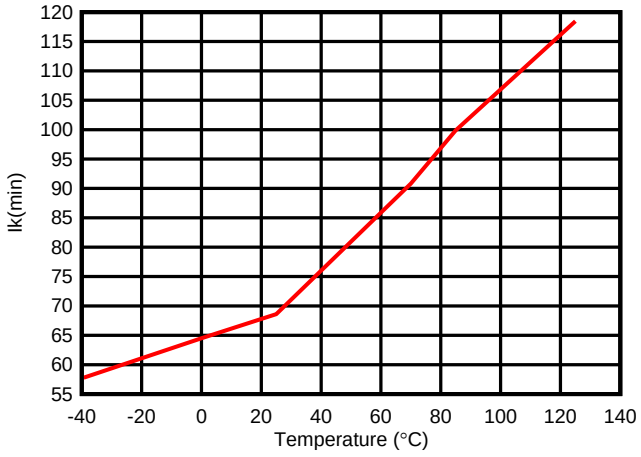


Figure 5. Minimum Cathode Current vs Temperature

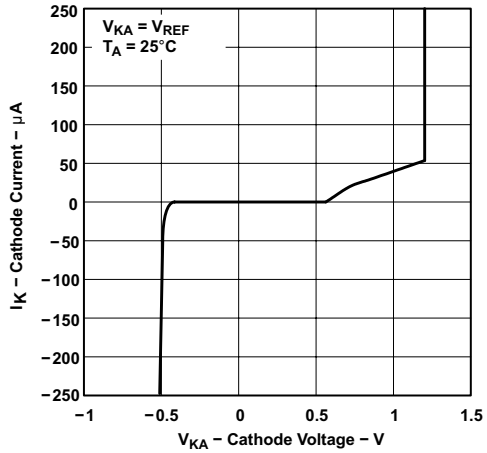


Figure 6. Cathode Current vs Cathode Voltage

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Typical Characteristics (continued)

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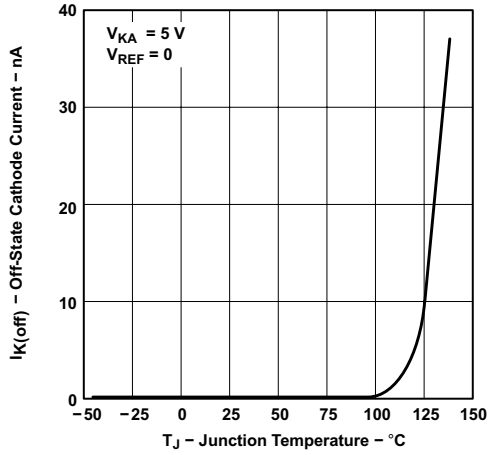


Figure 7. Off-State Cathode Current vs Junction Temperature (for TLV431 and TLV431A)

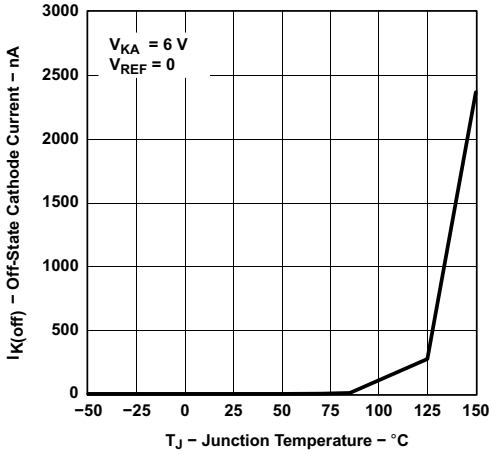


Figure 8. Off-State Cathode Current vs Junction Temperature (for TLV431B)

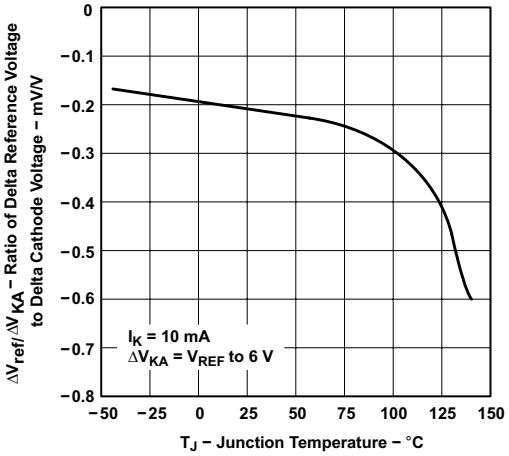


Figure 9. Ratio of Delta Reference Voltage to Delta Cathode Voltage vs Junction Temperature (for TLV431 and TLV431A)

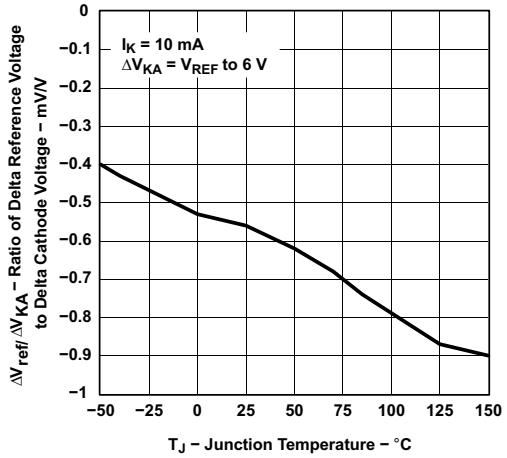
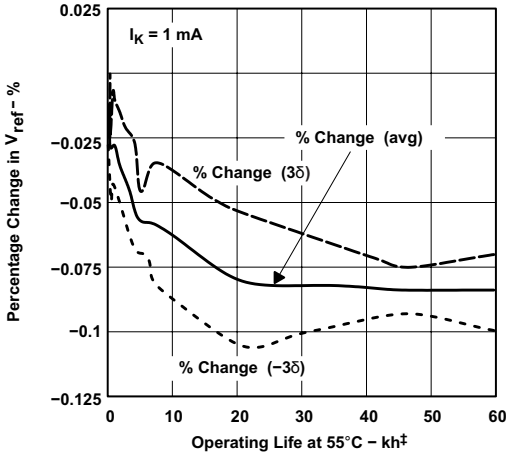


Figure 10. Ratio of Delta Reference Voltage to Delta Cathode Voltage vs Junction Temperature (for TLV431B)

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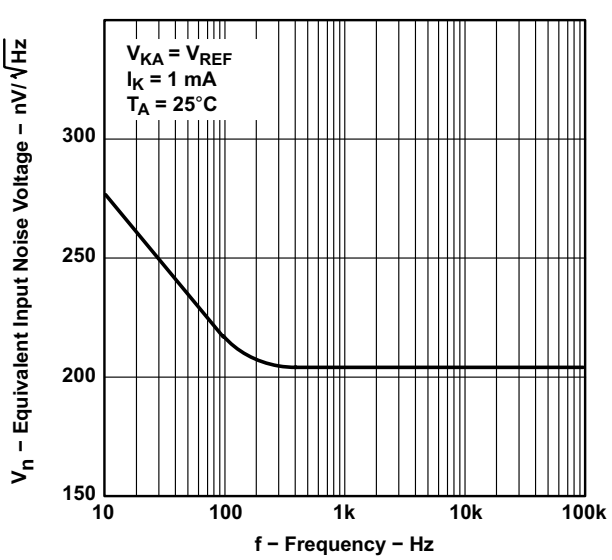
Typical Characteristics (continued)

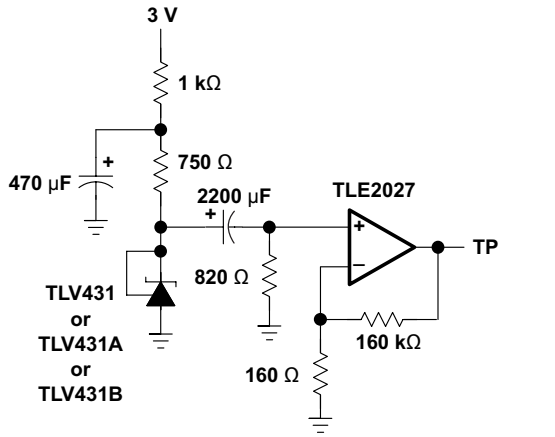
Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.



‡ Extrapolated from life-test data taken at 125°C; the activation energy assumed is 0.7 eV.

Figure 11. Percentage Change in V_{REF} vs Operating Life at 55°C





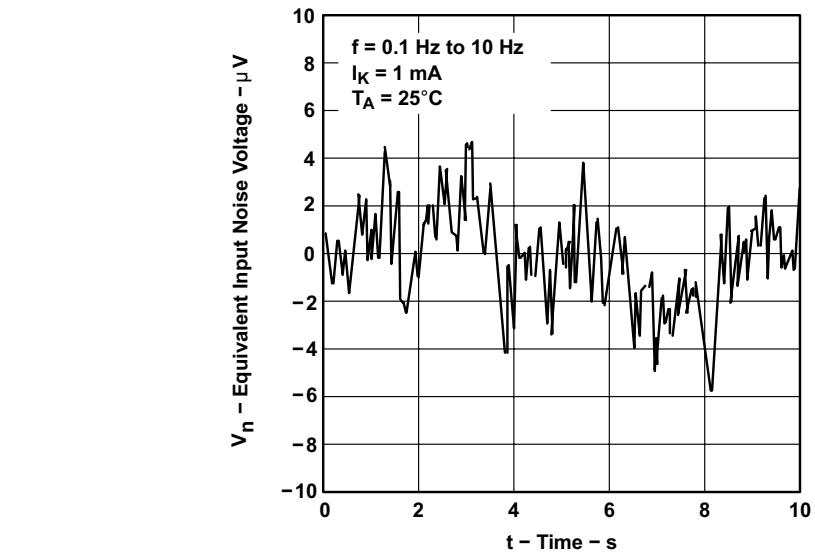
TEST CIRCUIT FOR EQUIVALENT INPUT NOISE VOLTAGE

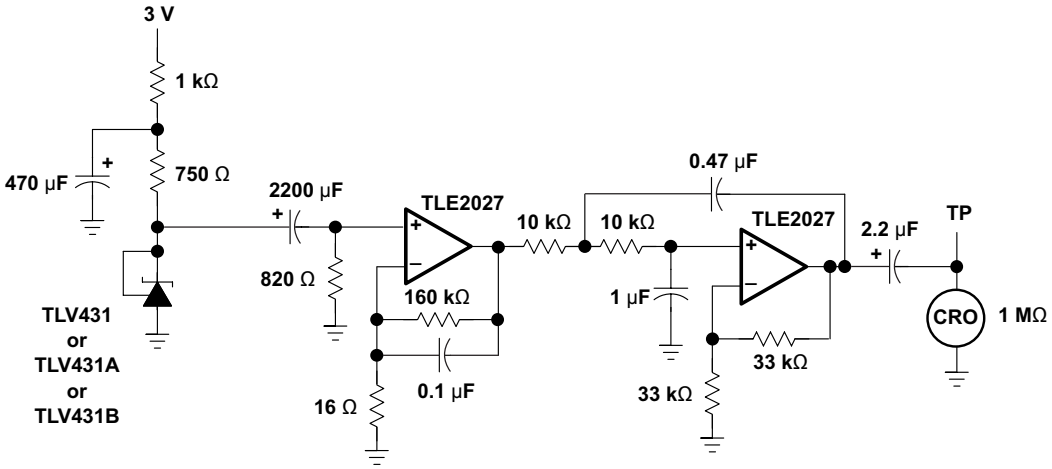
Figure 12. Equivalent Input Noise Voltage

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Typical Characteristics (continued)

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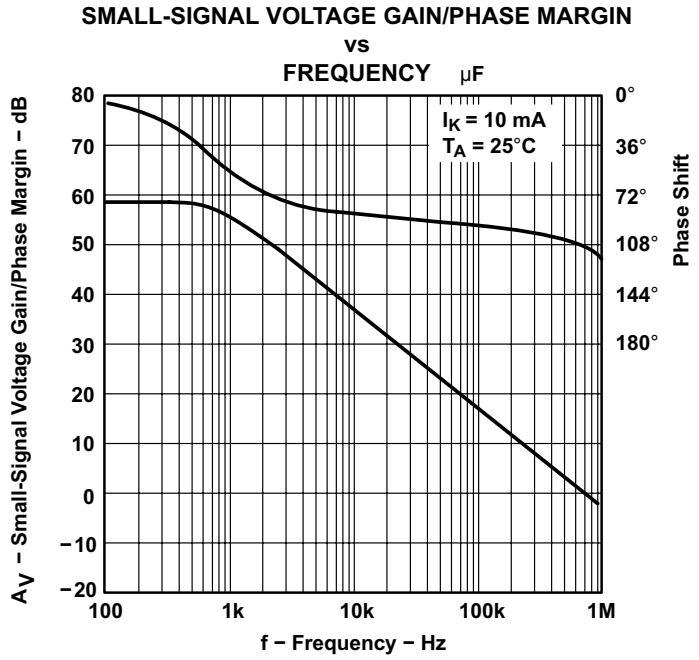
TEST CIRCUIT FOR 0.1-Hz TO 10-Hz EQUIVALENT NOISE VOLTAGE

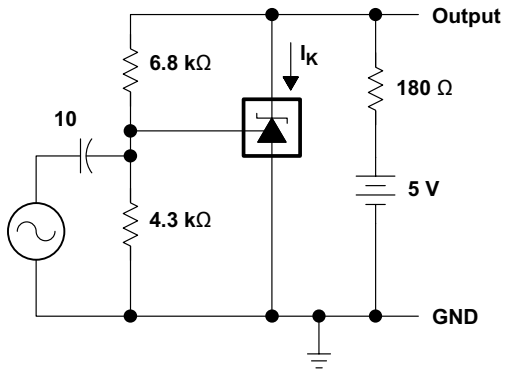
Figure 13. Equivalent Noise Voltage over a 10-s Period

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Typical Characteristics (continued)

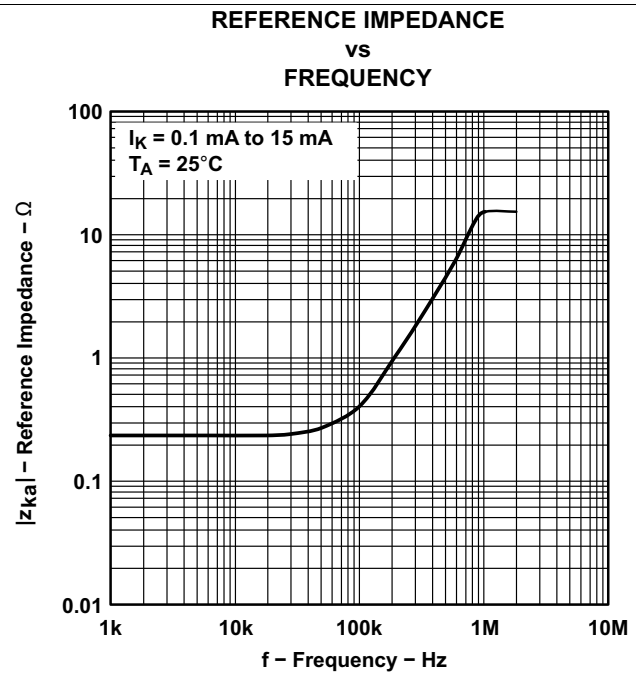
Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

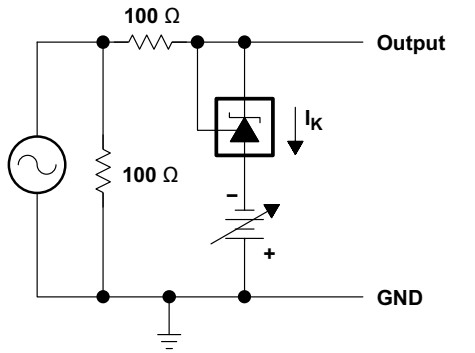




TEST CIRCUIT FOR VOLTAGE GAIN AND PHASE MARGIN

Figure 14. Voltage Gain and Phase Margin





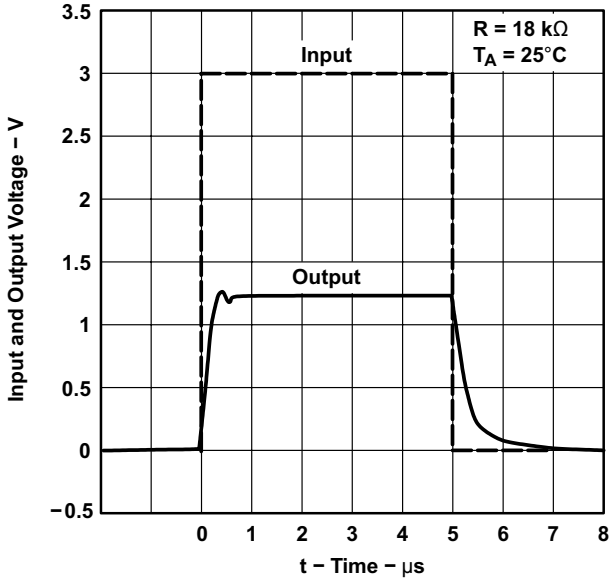
TEST CIRCUIT FOR REFERENCE IMPEDANCE

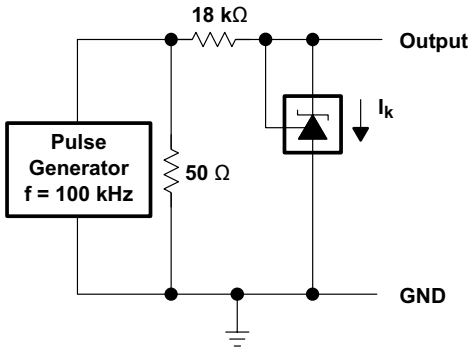
Figure 15. Reference Impedance vs Frequency

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Typical Characteristics (continued)

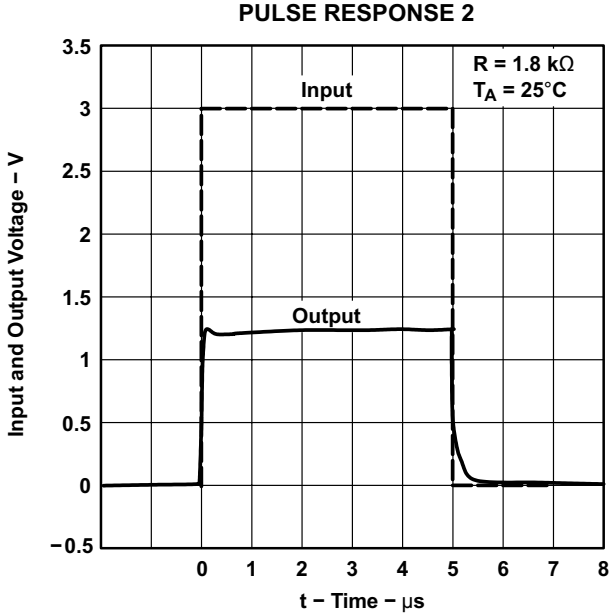
Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

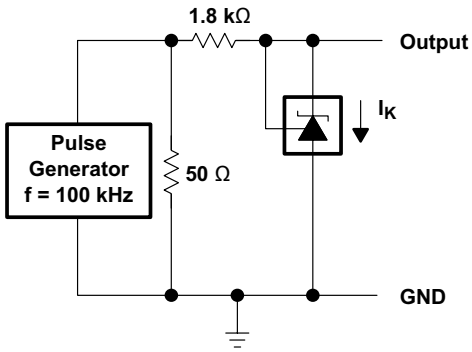




TEST CIRCUIT FOR PULSE RESPONSE 1

Figure 16. Pulse Response 1





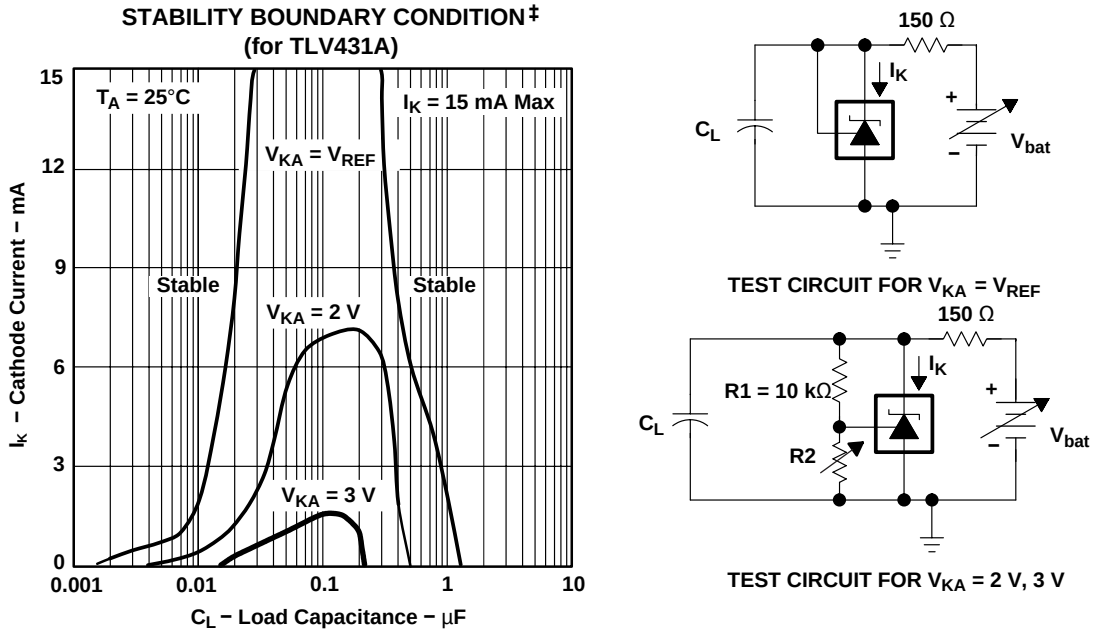
TEST CIRCUIT FOR PULSE RESPONSE 2

Figure 17. Pulse Response 2

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Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.



‡ The areas under the curves represent conditions that may cause the device to oscillate. For V_{KA} = 2-V and 3-V curves, R2 and V_{bat} were adjusted to establish the initial V_{KA} and I_K conditions with C_L = 0. V_{bat} and C_L then were adjusted to determine the ranges of stability.

Figure 18. Stability Boundary Conditions

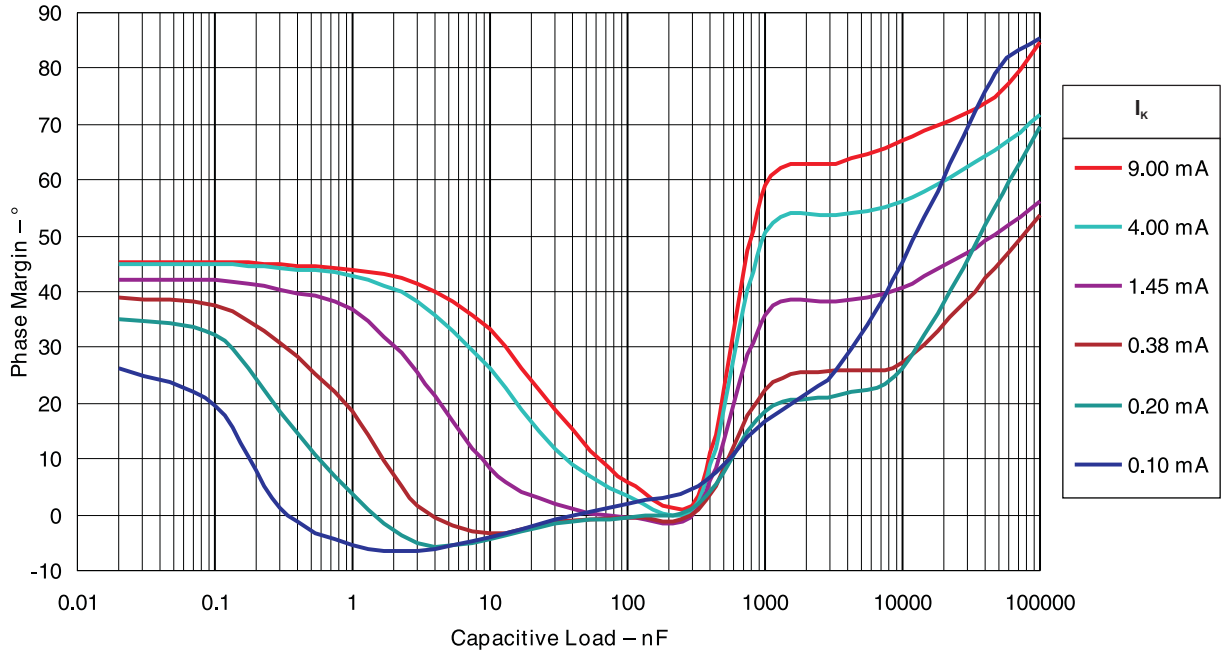


Figure 19. Phase Margin vs Capacitive Load
$V_{KA} = V_{REF}$ (1.25 V), T_A= 25°C

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Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

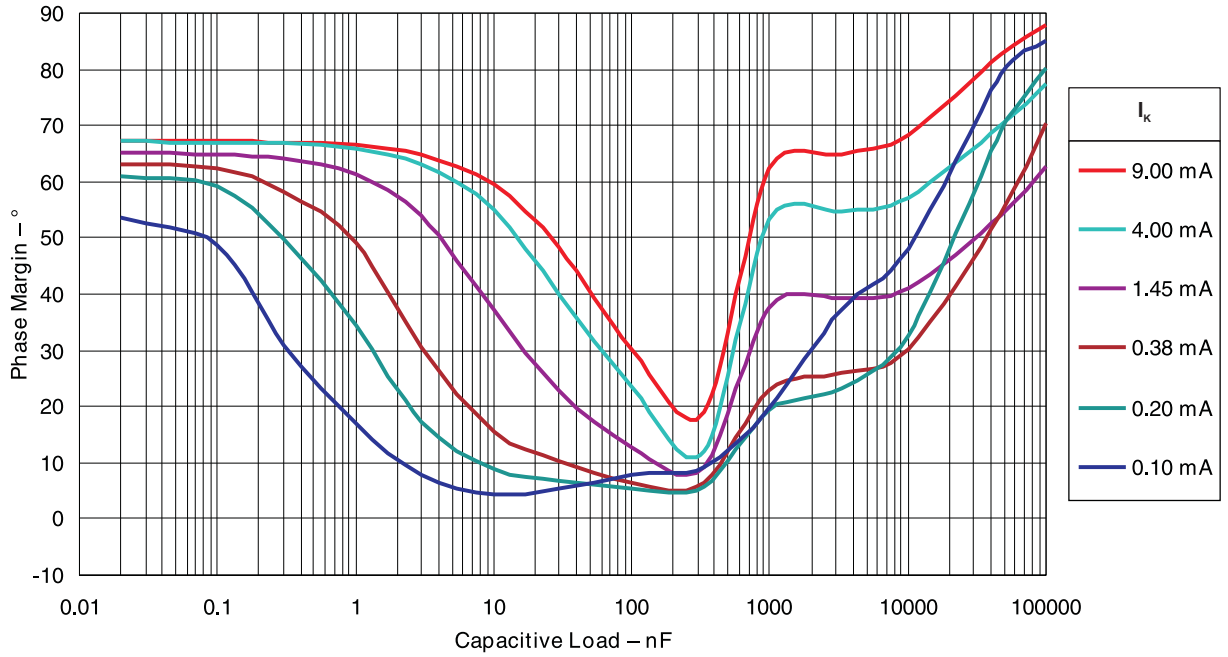


Figure 20. Phase Margin vs Capacitive Load
V_{KA} = 2.50 V, T_A= 25°C

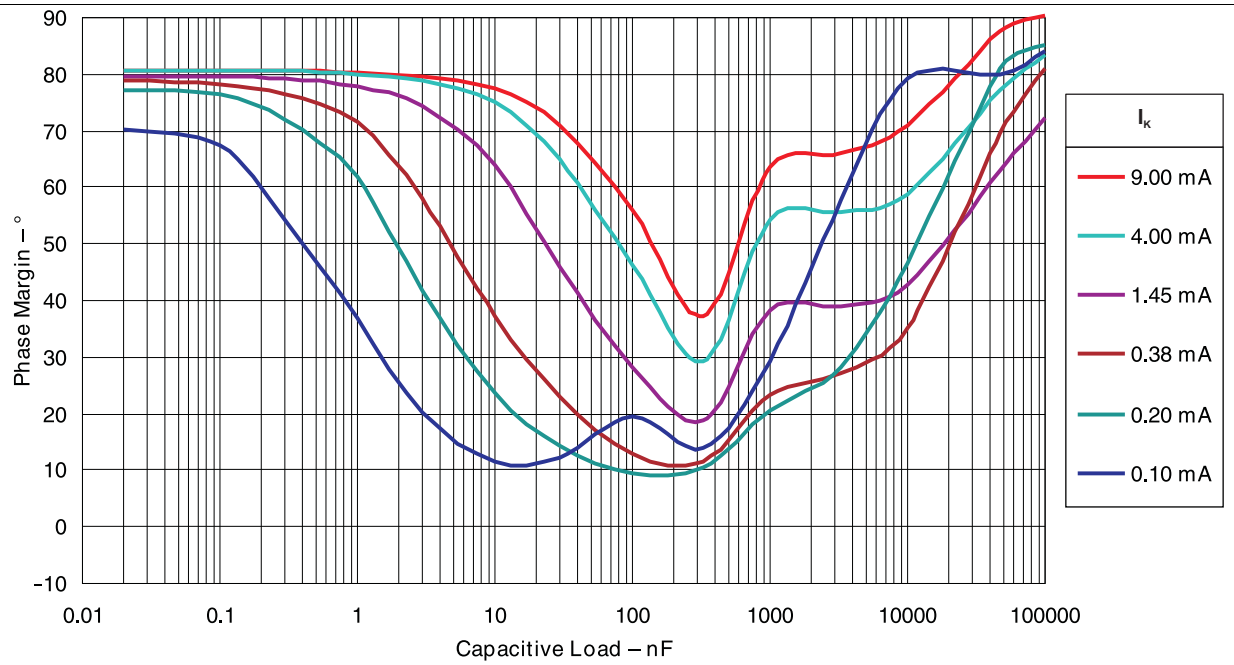


Figure 21. Phase Margin vs Capacitive Load
V_{KA} = 5.00 V, T_A= 25°C

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7 Parameter Measurement Information

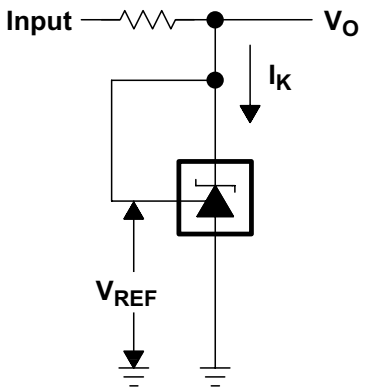


Figure 22. Test Circuit for $V_{KA} = V_{REF}$, $V_O = V_{KA} = V_{REF}$

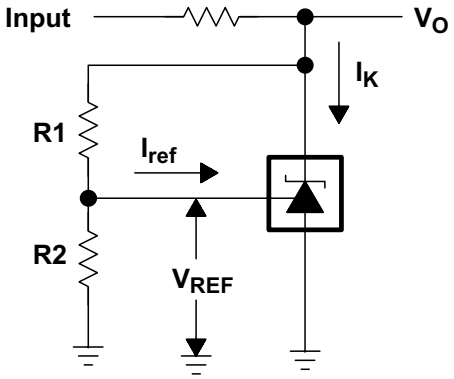


Figure 23. Test Circuit for $V_{KA} > V_{REF}$, $V_O = V_{KA} = V_{REF} \times (1 + R1/R2) + I_{ref} \times R1$

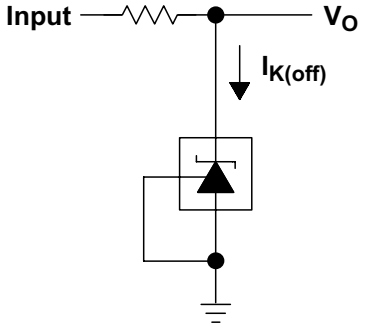


Figure 24. Test Circuit for $I_{K(off)}$

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8 Detailed Description

8.1 Overview

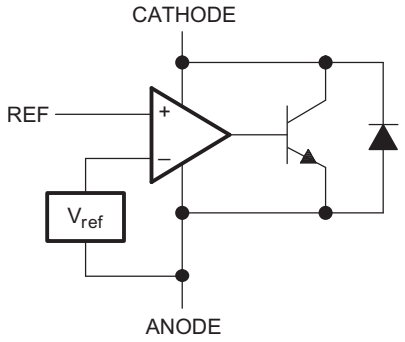
TLV431 is a low power counterpart to TL431, having lower reference voltage (1.24 V vs 2.5 V) for lower voltage adjustability and lower minimum cathode current ($I_{k(min)}$= 100 µA vs 1 mA). Like TL431, TLV431 is used in conjunction with it's key components to behave as a single voltage reference, error amplifier, voltage clamp, or comparator with integrated reference.

TLV431 can be operated and adjusted to cathode voltages from 1.24 V to 6 V, making this part optimum for a wide range of end equipments in industrial, auto, telecom, and computing. For this device to behave as a shunt regulator or error amplifier, > 100 µA (I_{min}(max)) must be supplied in to the cathode pin. Under this condition, feedback can be applied from the Cathode and Ref pins to create a replica of the internal reference voltage.

Various reference voltage options can be purchased with initial tolerances (at 25°C) of 0.5%, 1%, and 1.5%. These reference options are denoted by B (0.5%), A (1.0%), and blank (1.5%) after the TLV431.

The TLV431xC devices are characterized for operation from 0°C to 70°C, the TLV431xI devices are characterized for operation from –40°C to 85°C, and the TLV431xQ devices are characterized for operation from –40°C to 125°C.

8.2 Functional Block Diagram



8.3 Feature Description

TLV431 consists of an internal reference and amplifier that outputs a sink current base on the difference between the reference pin and the virtual internal pin. The sink current is produced by an internal darlington pair.

When operated with enough voltage headroom (≥ 1.24 V) and cathode current (Ika), TLV431 forces the reference pin to 1.24 V. However, the reference pin can not be left floating, as it requires I_{ref} ≥ 0.5 µA (see the *Functional Block Diagram*). This is because the reference pin is driven into an npn, which requires a base current to operate properly.

When feedback is applied from the Cathode and Reference pins, TLV431 behaves as a Zener diode, regulating to a constant voltage dependent on current being supplied into the cathode. This is due to the internal amplifier and reference entering the proper operating regions. The same amount of current required in the above feedback situation must be applied to this device in open-loop, servo, or error-amplifying implementations for it to be in the proper linear region giving TLV431 enough gain.

Unlike many linear regulators, TLV431 is internally compensated to be stable without an output capacitor between the cathode and anode. However, if it is desired to use an output capacitor Figure 18 can be used as a guide to assist in choosing the correct capacitor to maintain stability.

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8.4 Device Functional Modes

8.4.1 Open Loop (Comparator)

When the cathode/output voltage or current of TLV431 is not being fed back to the reference/input pin in any form, this device is operating in open loop. With proper cathode current (Ika) applied to this device, TLV431 will have the characteristics shown in Figure 6. With such high gain in this configuration, TLV431 is typically used as a comparator. With the reference integrated makes TLV431 the preferred choice when users are trying to monitor a certain level of a single signal.

8.4.2 Closed Loop

When the cathode/output voltage or current of TLV431 is being fed back to the reference/input pin in any form, this device is operating in closed loop. The majority of applications involving TLV431 use it in this manner to regulate a fixed voltage or current. The feedback enables this device to behave as an error amplifier, computing a portion of the output voltage and adjusting it to maintain the desired regulation. This is done by relating the output voltage back to the reference pin in a manner to make it equal to the internal reference voltage, which can be accomplished through resistive or direct feedback.

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9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Figure 25 shows the TLV431, TLV431A, or TLV431B used in a 3.3-V isolated flyback supply. Output voltage V_O can be as low as reference voltage V_{REF} (1.24 V ± 1%). The output of the regulator, plus the forward voltage drop of the optocoupler LED (1.24 + 1.4 = 2.64 V), determine the minimum voltage that can be regulated in an isolated supply configuration. Regulated voltage as low as 2.7 Vdc is possible in the topology shown in Figure 25.

The 431 family of devices are prevalent in these applications, being designers go to choice for secondary side regulation. Due to this prevalence, this section will further go on to explain operation and design in both states of TLV431 that this application will see, open loop (Comparator + Vref) and closed loop (Shunt Regulator).

Further information about system stability and using a TLV431 device for compensation can be found in the application note *Compensation Design With TL431 for UCC28600* (SLUA671).

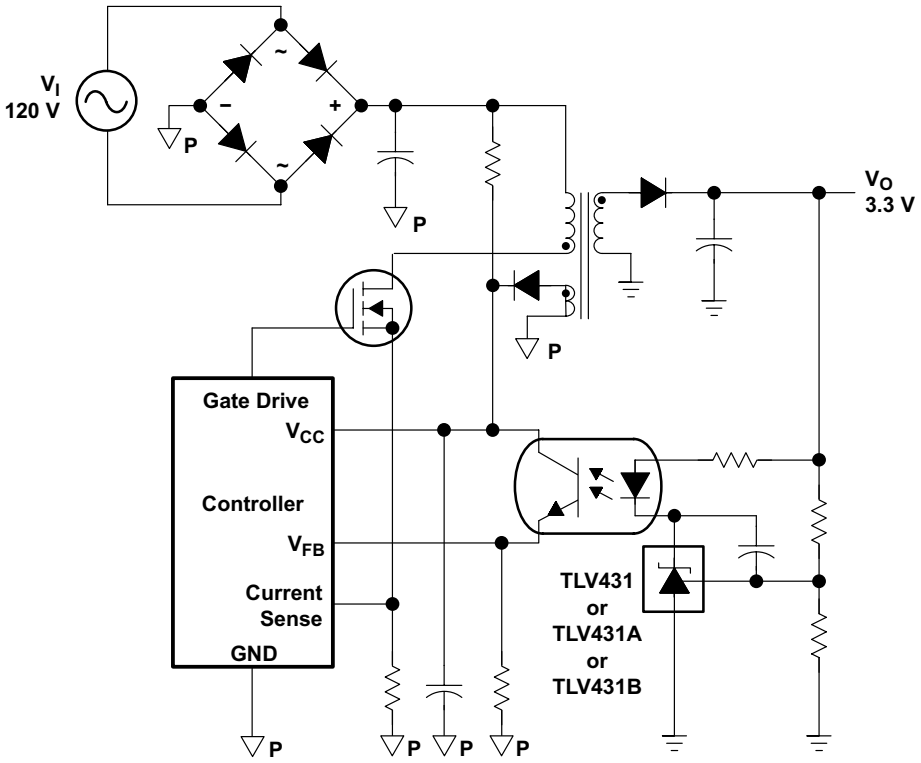


Figure 25. Flyback With Isolation Using TLV431, TLV431A, or TLV431B as Voltage Reference and Error Amplifier

9.2 Typical Applications

9.2.1 Comparator With Integrated Reference (Open Loop)

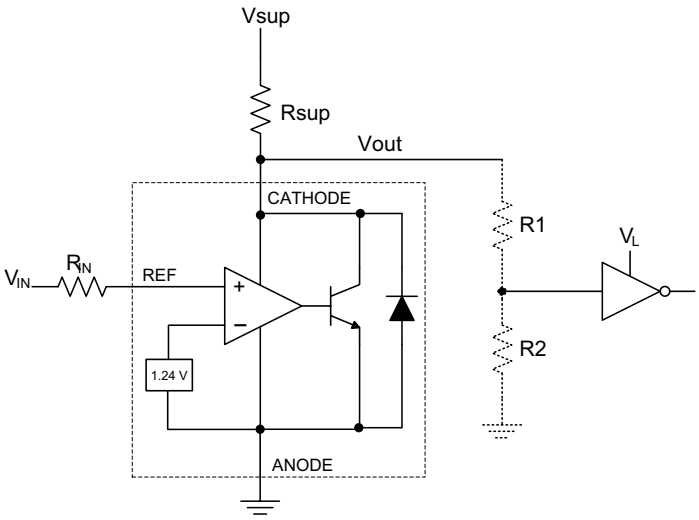


Figure 26. Comparator Application Schematic

9.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0 V to 5 V
Input Resistance	10 kΩ
Supply Voltage	5 V
Cathode Current (Ik)	500 µA
Output Voltage Level	~1 V - Vsup
Logic Input Thresholds VIH/VIL	VL

9.2.1.2 Detailed Design Procedure

When using TLV431 as a comparator with reference, determine the following:

- Input voltage range
- Reference voltage accuracy
- Output logic input high and low level thresholds
- Current source resistance

9.2.1.2.1 Basic Operation

In the configuration shown in Figure 26 TLV431 will behave as a comparator, comparing the V_{ref} pin voltage to the internal virtual reference voltage. When provided a proper cathode current (I_k), TLV431 will have enough open-loop gain to provide a quick response. With the TLV431's maximum operating current (I_{min}(max)) being 100 µA and up to 150 µA over temperature, operation below that could result in low gain, leading to a slow response.

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9.2.1.2.2 Overdrive

Slow or inaccurate responses can also occur when the reference pin is not provided enough overdrive voltage. This is the amount of voltage that is higher than the internal virtual reference. The internal virtual reference voltage will be within the range of 1.24 V ±(0.5%, 1.0%, or 1.5%) depending on which version is being used.

The more overdrive voltage provided, the faster the TLV431 will respond. This can be seen in Figure 27 and Figure 28 where it displays the output responses to various input voltages.

For applications where TLV431 is being used as a comparator, it is best to set the trip point to greater than the positive expected error (that is, +1.0% for the A version). For fast response, setting the trip point to > 10% of the internal V_{ref} should suffice.

For minimal voltage drop or difference from Vin to the ref pin, TI recommends using an input resistor < 10 kΩ to provide I_{ref}.

9.2.1.2.3 Output Voltage and Logic Input Level

In order for TLV431 to properly be used as a comparator, the logic output must be readable by the receiving logic device. This is accomplished by knowing the input high and low level threshold voltage levels, typically denoted by V_{IH} and V_{IL}.

As seen in Figure 27, TLV431's output low level voltage in open-loop/comparator mode is approximately 1 V, which is sufficient for some 3.3-V supplied logic. However, this would not work for 2.5-V or 1.8-V supplied logic. To accommodate this a resistive divider can be tied to the output to attenuate the output voltage to a voltage legible to the receiving low voltage logic device.

TLV431's output high voltage is approximately V_{sup} due to TLV431 being open-collector. If V_{sup} is much higher than the receiving logic's maximum input voltage tolerance, the output must be attenuated to accommodate the outgoing logic's reliability.

When using a resistive divider on the output, be sure to make the sum of the resistive divider (R1 and R2 in Figure 26) is much greater than R_{sup} in order to not interfere with TLV431's ability to pull close to V_{sup} when turning off.

9.2.1.2.3.1 Input Resistance

TLV431 requires an input resistance in this application to source the reference current (I_{ref}) needed from this device to be in the proper operating regions while turning on. The actual voltage seen at the ref pin will be $V_{ref} = V_{in} – I_{ref} \times R_{in}$. Because the I_{ref} can be as high as 0.5 µA, TI recommends using a resistance small enough that will mitigate the error that I_{ref} creates from V_{in}.

9.2.1.3 Application Curves

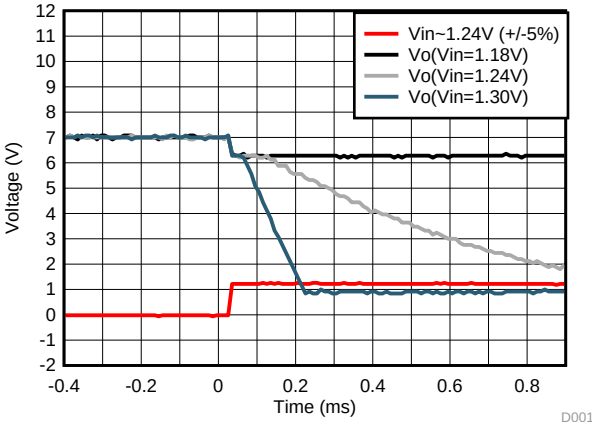


Figure 27. Output Response With Small Overdrive Voltages

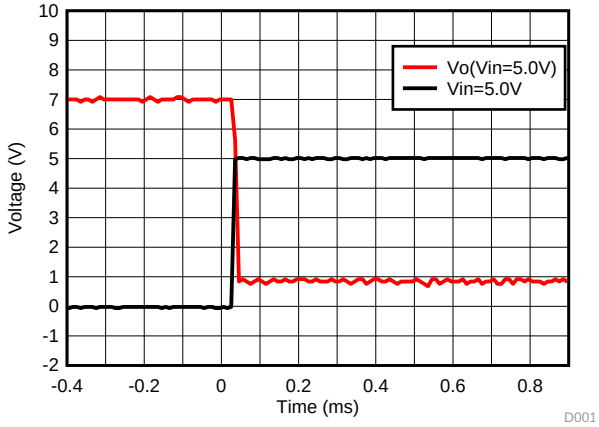


Figure 28. Output Response With Large Overdrive Voltage

9.2.2 Shunt Regulator/Reference

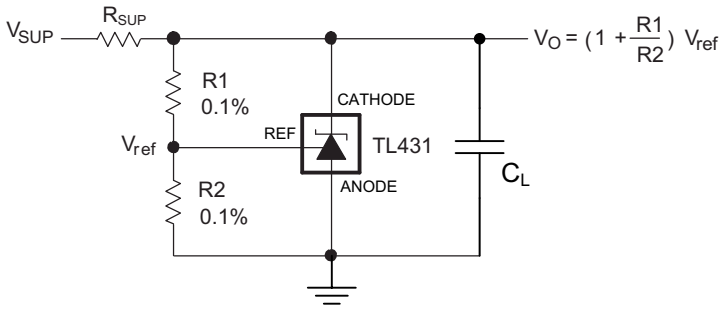


Figure 29. Shunt Regulator Schematic

9.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Reference Initial Accuracy	1.0%
Supply Voltage	6 V
Cathode Current (Ik)	1 mA
Output Voltage Level	1.24 V - 6 V
Load Capacitance	100 nF
Feedback Resistor Values and Accuracy (R1 and R2)	10 kΩ

9.2.2.2 Detailed Design Procedure

When using TLV431 as a Shunt Regulator, determine the following:

- Input voltage range
- Temperature range
- Total accuracy
- Cathode current
- Reference initial accuracy
- Output capacitance

9.2.2.2.1 Programming Output/Cathode Voltage

To program the cathode voltage to a regulated voltage a resistive bridge must be shunted between the cathode and anode pins with the mid point tied to the reference pin. This can be seen in Figure 29, with R1 and R2 being the resistive bridge. The cathode/output voltage in the shunt regulator configuration can be approximated by the equation shown in Figure 29. The cathode voltage can be more accurately determined by taking the cathode current in to account

$$V_O = (1 + R1 / R2) \times V_{ref} – I_{ref} \times R1 \quad (1)$$

For Equation 1 to be valid, TLV431 must be fully biased so that it has enough open-loop gain to mitigate any gain error. This can be done by meeting the I_{min} spec denoted in *Recommended Operating Conditions* table.

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9.2.2.2.2 Total Accuracy

When programming the output above unity gain (Vka = Vref), TLV431 is susceptible to other errors that may effect the overall accuracy beyond V_{ref}. These errors include:

- R1 and R2 accuracies
- $V_{I(dev)}$ – Change in reference voltage over temperature
- ΔV_{ref} / ΔV_{KA} – Change in reference voltage to the change in cathode voltage
- $|z_{KA}|$ – Dynamic impedance, causing a change in cathode voltage with cathode current

Worst-case cathode voltage can be determined taking all of the variables in to account. Application note Setting the Shunt Voltage on an Adjustable Shunt Regulator (SLVA445) assists designers in setting the shunt voltage to achieve optimum accuracy for this device.

9.2.2.2.3 Stability

Though TLV431 is stable with no capacitive load, the device that receives the shunt regulator's output voltage could present a capacitive load that is within the TLV431 region of stability, shown in Figure 18. Also, designers may use capacitive loads to improve the transient response or for power supply decoupling.

9.2.2.3 Application Curve

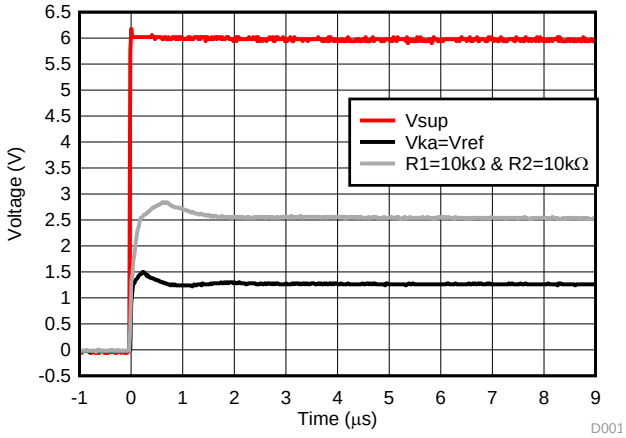


Figure 30. TLV431 Start-Up Response

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10 Power Supply Recommendations

When using TLV431 as a Linear Regulator to supply a load, designers will typically use a bypass capacitor on the output/cathode pin. When doing this, be sure that the capacitance is within the stability criteria shown in Figure 18.

To not exceed the maximum cathode current, be sure that the supply voltage is current limited. Also, be sure to limit the current being driven into the Ref pin, as not to exceed the absolute maximum rating.

For applications shunting high currents, pay attention to the cathode and anode trace lengths, adjusting the width of the traces to have the proper current density.

11 Layout

11.1 Layout Guidelines

Place decoupling capacitors as close to the device as possible. Use appropriate widths for traces when shunting high currents to avoid excessive voltage drops.

11.2 Layout Example

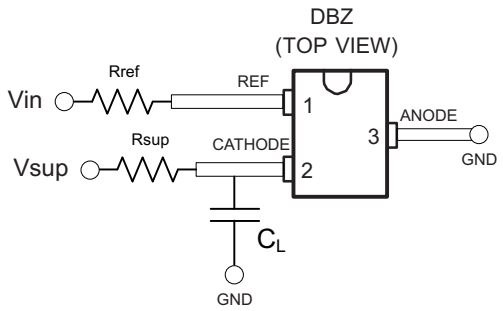


Figure 31. DBZ Layout Example

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12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- *《使用 TL431 针对 UCC28600 进行补偿设计》*(SLUA671)
- 《在可调节并联稳压器上设置并联电压》(SLVA445)

12.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 3. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持和社区
TLV431	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TLV431A	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TLV431B	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV431ACDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	(YAC6, YACC, YACI, YACN) (YACG, YACL, YACS)	Samples
TLV431ACDBVRE4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	YACI	Samples
TLV431ACDBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	YACI	Samples
TLV431ACDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	(YAC6, YACC, YACI) (YACG, YACL, YACS)	Samples
TLV431ACDBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	YACI	Samples
TLV431ACDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(YAC6, YAC8, YACB) (YAC3, YACS, YACU)	Samples
TLV431ACDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(YAC6, YAC8, YACB) (YAC3, YACS, YACU)	Samples
TLV431ACLP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 70	V431AC	Samples
TLV431ACLPE3	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 70	V431AC	Samples
TLV431ACLPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 70	V431AC	Samples
TLV431AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY431A	Samples
TLV431AIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(YAI6, YAIC, YAII, YAIN) (YAIG, YAIL, YAIS)	Samples
TLV431AIDBVRE4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YAII	Samples
TLV431AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YAII	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV431AIDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(YAI6, YAIC, YAII) (YAIG, YAIL, YAIS)	Samples
TLV431AIDBVTE4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YAII	Samples
TLV431AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YAII	Samples
TLV431AIDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(YAI6, YAI8, YAIB) (YAI3, YAIS, YAIU)	Samples
TLV431AIDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(YAI6, YAI8, YAIB) (YAI3, YAIS, YAIU)	Samples
TLV431AIDE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY431A	Samples
TLV431AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY431A	Samples
TLV431AIDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY431A	Samples
TLV431AILP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 85	V431AI	Samples
TLV431AILPE3	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 85	V431AI	Samples
TLV431AILPM	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	-40 to 85	V431AI	Samples
TLV431AILPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	-40 to 85	V431AI	Samples
TLV431AILPRE3	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	-40 to 85	V431AI	Samples
TLV431AQPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	VA	Samples
TLV431AQPKG3	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	VA	Samples
TLV431BCDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	(Y3GG, Y3GJ, Y3GU)	Samples
TLV431BCDBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	Y3GG	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV431BCDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	(Y3GG, Y3GJ, Y3GU)	Samples
TLV431BCDBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	Y3GG	Samples
TLV431BCDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(Y3G3, Y3GS, Y3GU)	Samples
TLV431BCDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(Y3G3, Y3GS, Y3GU)	Samples
TLV431BCDBZT	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(Y3GS, Y3GU)	Samples
TLV431BCDBZTG4	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(Y3GS, Y3GU)	Samples
TLV431BCDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	YEU	Samples
TLV431BCDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	YEU	Samples
TLV431BCLP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 70	TV431B	Samples
TLV431BCLPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 70	TV431B	Samples
TLV431BCPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 70	VE	Samples
TLV431BIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(Y3FJ, Y3FU)	Samples
TLV431BIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(Y3FJ, Y3FU)	Samples
TLV431BIDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(Y3FJ, Y3FU)	Samples
TLV431BIDBVTE4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	(Y3FJ, Y3FU)	Samples
TLV431BIDBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(Y3FJ, Y3FU)	Samples
TLV431BIDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(Y3F3, Y3FS, Y3FU)	Samples
TLV431BIDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(Y3F3, Y3FS, Y3FU)	Samples
TLV431BIDBZT	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(Y3FS, Y3FU)	Samples
TLV431BIDBZTG4	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(Y3FS, Y3FU)	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV431BIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YFU	Samples
TLV431BIDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YFU	Samples
TLV431BIDCKTE4	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YFU	Samples
TLV431BILP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 85	TY431B	Samples
TLV431BILPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	-40 to 85	TY431B	Samples
TLV431BILPRE3	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	-40 to 85	TY431B	Samples
TLV431BIPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	VF	Samples
TLV431BQDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(Y3HJ, Y3HU)	Samples
TLV431BQDBVRE4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	(Y3HJ, Y3HU)	Samples
TLV431BQDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(Y3HJ, Y3HU)	Samples
TLV431BQDBVTE4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	(Y3HJ, Y3HU)	Samples
TLV431BQDBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(Y3HJ, Y3HU)	Samples
TLV431BQDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(Y3H3, Y3HS, Y3HU)	Samples
TLV431BQDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	Y3HS	Samples
TLV431BQDBZT	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(Y3HS, Y3HU)	Samples
TLV431BQDBZTG4	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(Y3HS, Y3HU)	Samples
TLV431BQDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YGU	Samples
TLV431BQDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YGU	Samples
TLV431BQLP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	TQ431B	Samples
TLV431BQLPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	TQ431B	Samples
TLV431BQPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	V6	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV431CDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	(Y3C6, Y3CI) (Y3CG, Y3CS)	Samples
TLV431CDBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	Y3CI	Samples
TLV431CDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	(Y3C6, Y3CI) (Y3CG, Y3CS)	Samples
TLV431CDBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	Y3CI	Samples
TLV431CDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(Y3C6, Y3C8, Y3CB) (Y3C3, Y3CS, Y3CU)	Samples
TLV431CDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(Y3C6, Y3C8, Y3CB) (Y3C3, Y3CS, Y3CU)	Samples
TLV431CLP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 70	V431C	Samples
TLV431CLPE3	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 70	V431C	Samples
TLV431CLPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 70	V431C	Samples
TLV431IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(Y3I6, Y3II) (Y3IG, Y3IS)	Samples
TLV431IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y3II	Samples
TLV431IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(Y3I6, Y3II) (Y3IG, Y3IS)	Samples
TLV431IDBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y3II	Samples
TLV431IDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(Y3I6, Y3IB) (Y3IS, Y3IU)	Samples
TLV431IDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(Y3I6, Y3IB) (Y3IS, Y3IU)	Samples
TLV431ILP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 85	V431I	Samples
TLV431ILPE3	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 85	V431I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV431ILPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	-40 to 85	V431I	Samples
TLV431QPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	VB	Samples
TLV431QPKG3	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	VB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV431A, TLV431B :

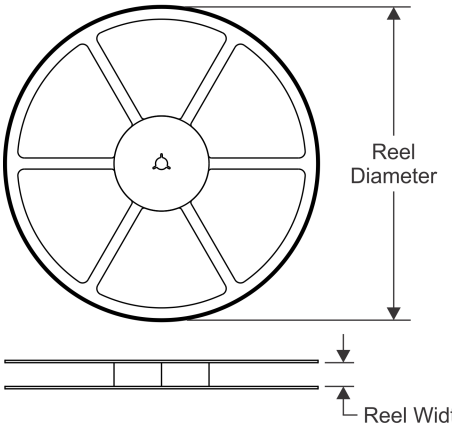
- Automotive : TLV431A-Q1, TLV431B-Q1

NOTE: Qualified Version Definitions:

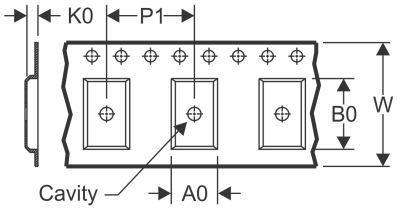
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

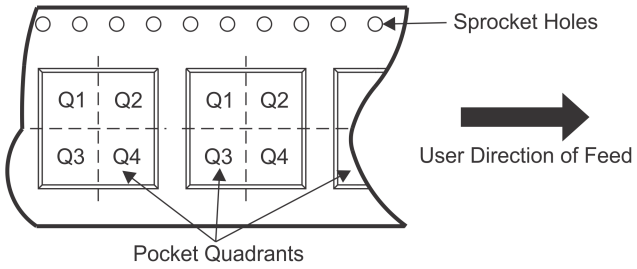


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



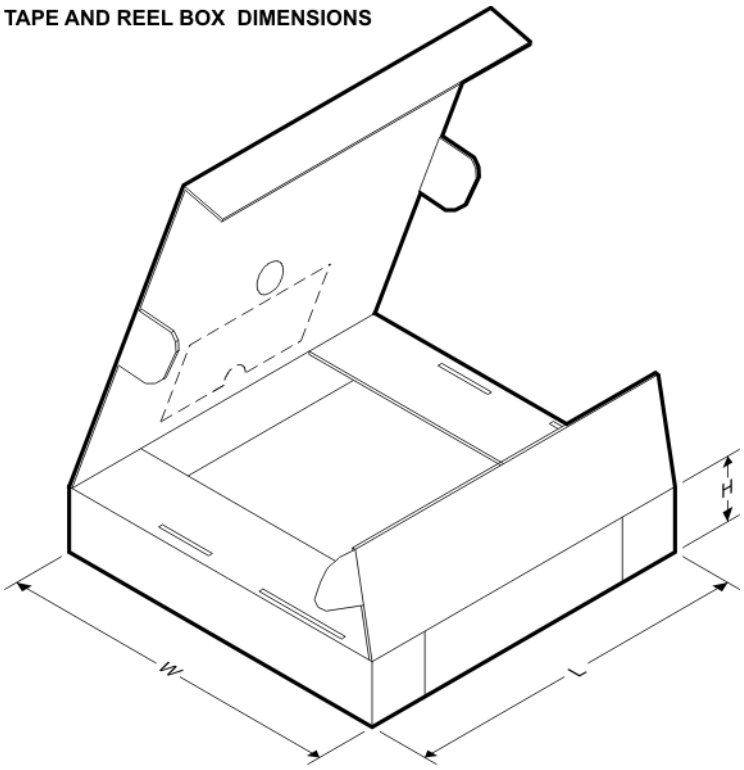
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV431ACDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV431ACDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431ACDBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431ACDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431ACDBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431ACDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431ACDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
TLV431ACDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV431AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV431AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431AIDBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431AIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431AIDBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431AIDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV431AIDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
TLV431AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV431AQPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TLV431BCDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV431BCDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV431BCDBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431BCDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV431BCDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431BCDBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431BCDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV431BCDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BCDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BCDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BCDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV431BCDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV431BCPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TLV431BIDBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431BIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV431BIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431BIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV431BIDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV431BIDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BIDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BIDBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV431BIDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BIDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV431BIDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV431BIPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TLV431BQDBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431BQDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV431BQDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV431BQDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431BQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BQDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BQDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BQDBZTG4	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BQDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV431BQDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV431BQPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TLV431CDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431CDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV431CDBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431CDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431CDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV431CDBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431CDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
TLV431CDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV431CDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV431IDBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV431IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431IDBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431IDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV431QPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS



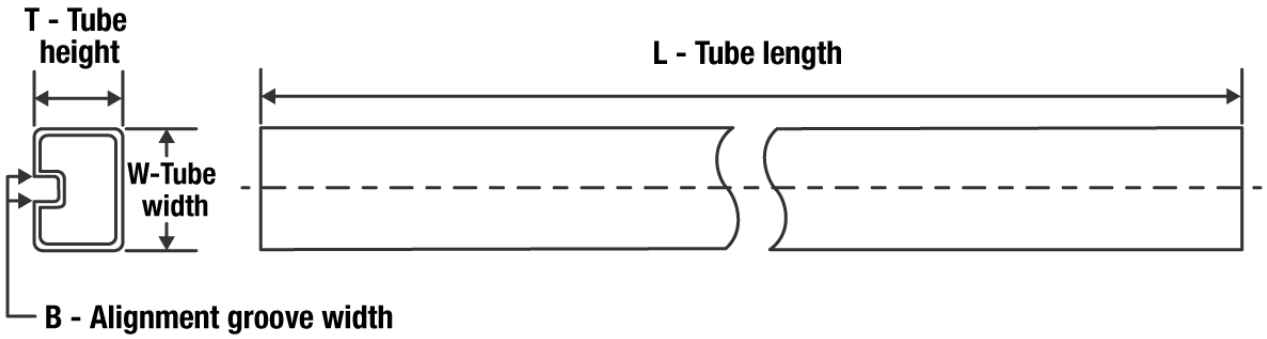
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV431ACDBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV431ACDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431ACDBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431ACDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431ACDBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431ACDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TLV431ACDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV431ACDBZR	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TLV431AIDBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV431AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV431AIDBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431AIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431AIDBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431AIDBZR	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TLV431AIDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV431AIDR	SOIC	D	8	2500	340.5	336.1	25.0
TLV431AQPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TLV431BCDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431BCDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431BCDBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431BCDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431BCDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431BCDBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431BCDBZR	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TLV431BCDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TLV431BCDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV431BCDBZT	SOT-23	DBZ	3	250	183.0	183.0	20.0
TLV431BCDCKR	SC70	DCK	6	3000	203.0	203.0	35.0
TLV431BCDCKT	SC70	DCK	6	250	203.0	203.0	35.0
TLV431BCPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TLV431BIDBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TLV431BIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431BIDBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TLV431BIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431BIDBZR	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TLV431BIDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV431BIDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TLV431BIDBZT	SOT-23	DBZ	3	250	200.0	183.0	25.0
TLV431BIDBZT	SOT-23	DBZ	3	250	183.0	183.0	20.0
TLV431BIDCKR	SC70	DCK	6	3000	203.0	203.0	35.0
TLV431BIDCKT	SC70	DCK	6	250	203.0	203.0	35.0
TLV431BIPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TLV431BQDBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TLV431BQDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431BQDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431BQDBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TLV431BQDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TLV431BQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV431BQDBZT	SOT-23	DBZ	3	250	183.0	183.0	20.0
TLV431BQDBZTG4	SOT-23	DBZ	3	250	183.0	183.0	20.0
TLV431BQDCKR	SC70	DCK	6	3000	200.0	183.0	25.0
TLV431BQDCKT	SC70	DCK	6	250	200.0	183.0	25.0
TLV431BQPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TLV431CDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV431CDBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV431CDBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431CDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431CDBVT	SOT-23	DBV	5	250	183.0	183.0	20.0
TLV431CDBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431CDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV431CDBZR	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TLV431CDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TLV431IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431IDBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431IDBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431IDBZR	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TLV431QPK	SOT-89	PK	3	1000	340.0	340.0	38.0

TUBE



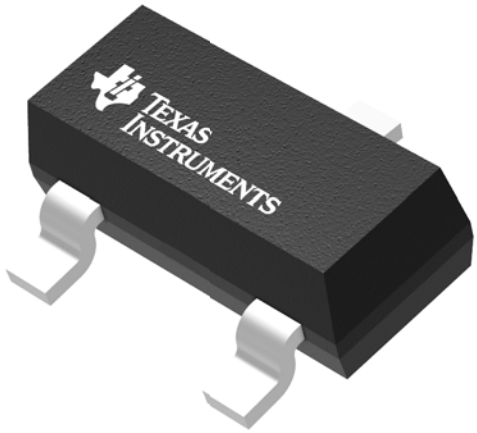
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV431AID	D	SOIC	8	75	507	8	3940	4.32
TLV431AIDE4	D	SOIC	8	75	507	8	3940	4.32

GENERIC PACKAGE VIEW

DBZ 3 SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



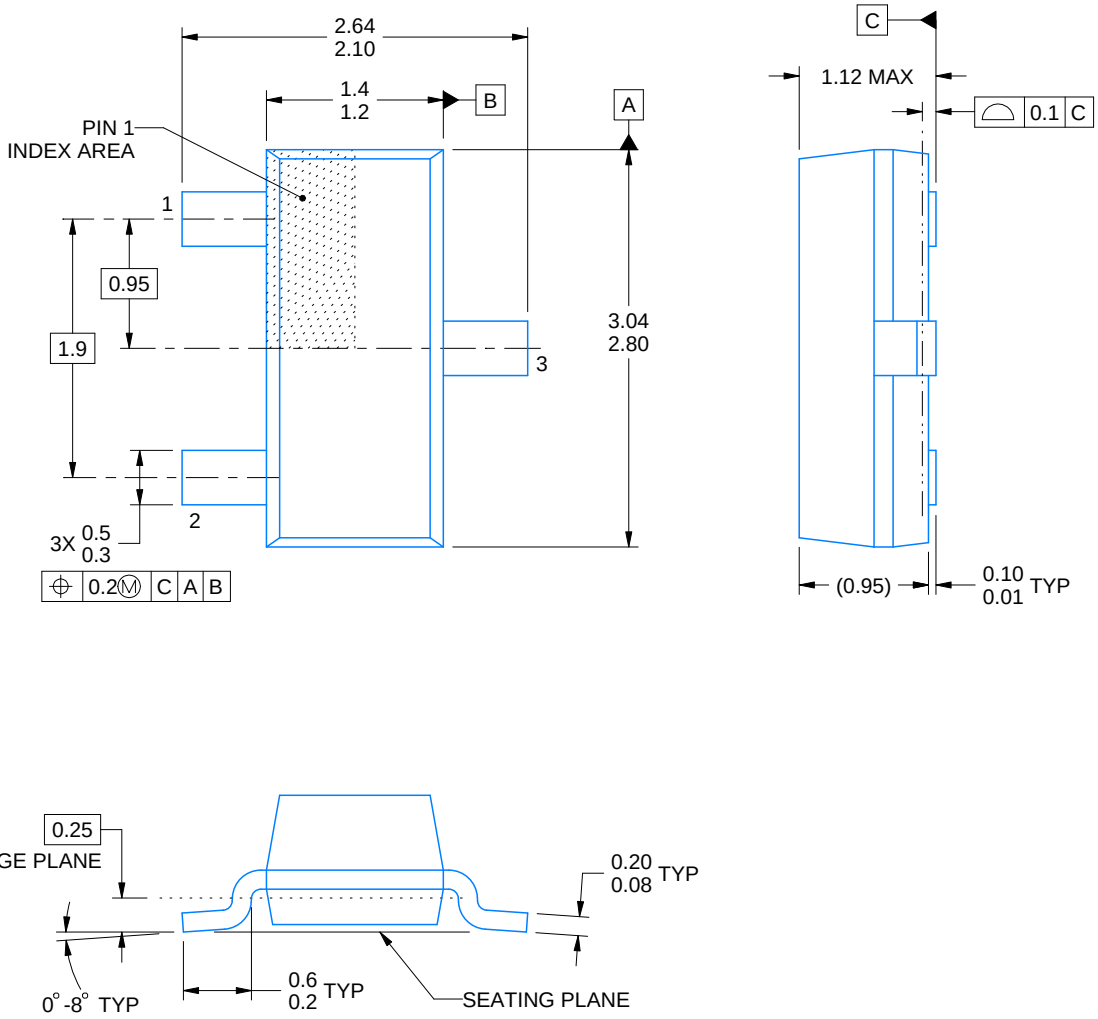
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

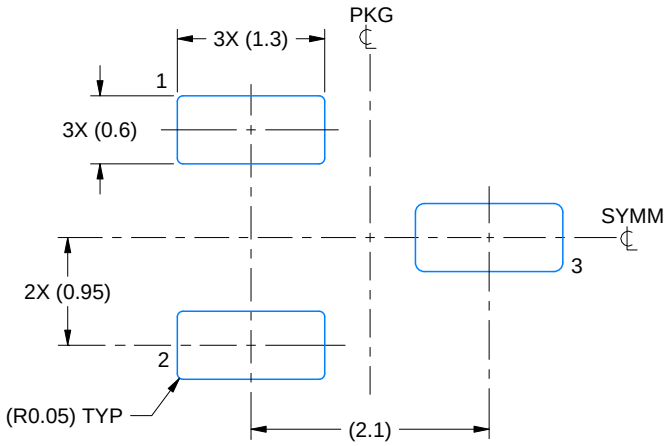
SMALL OUTLINE TRANSISTOR



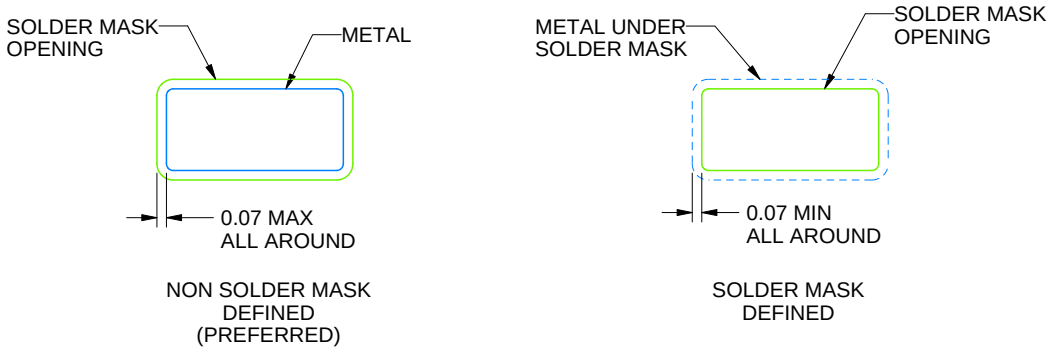
4214838/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.



LAND PATTERN EXAMPLE
SCALE:15X

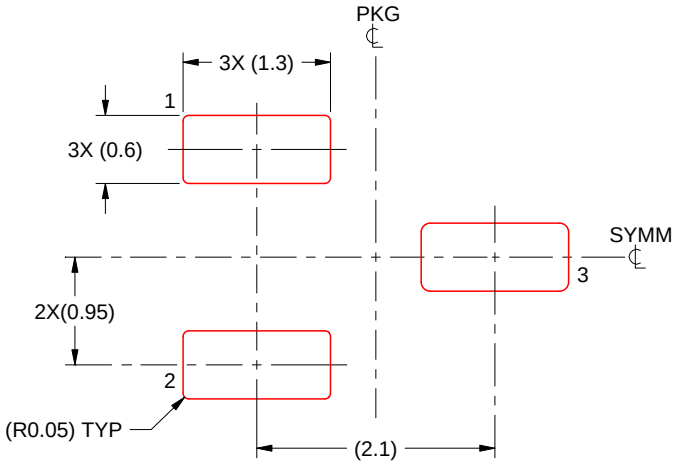


SOLDER MASK DETAILS

4214838/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/C 04/2017

NOTES: (continued)

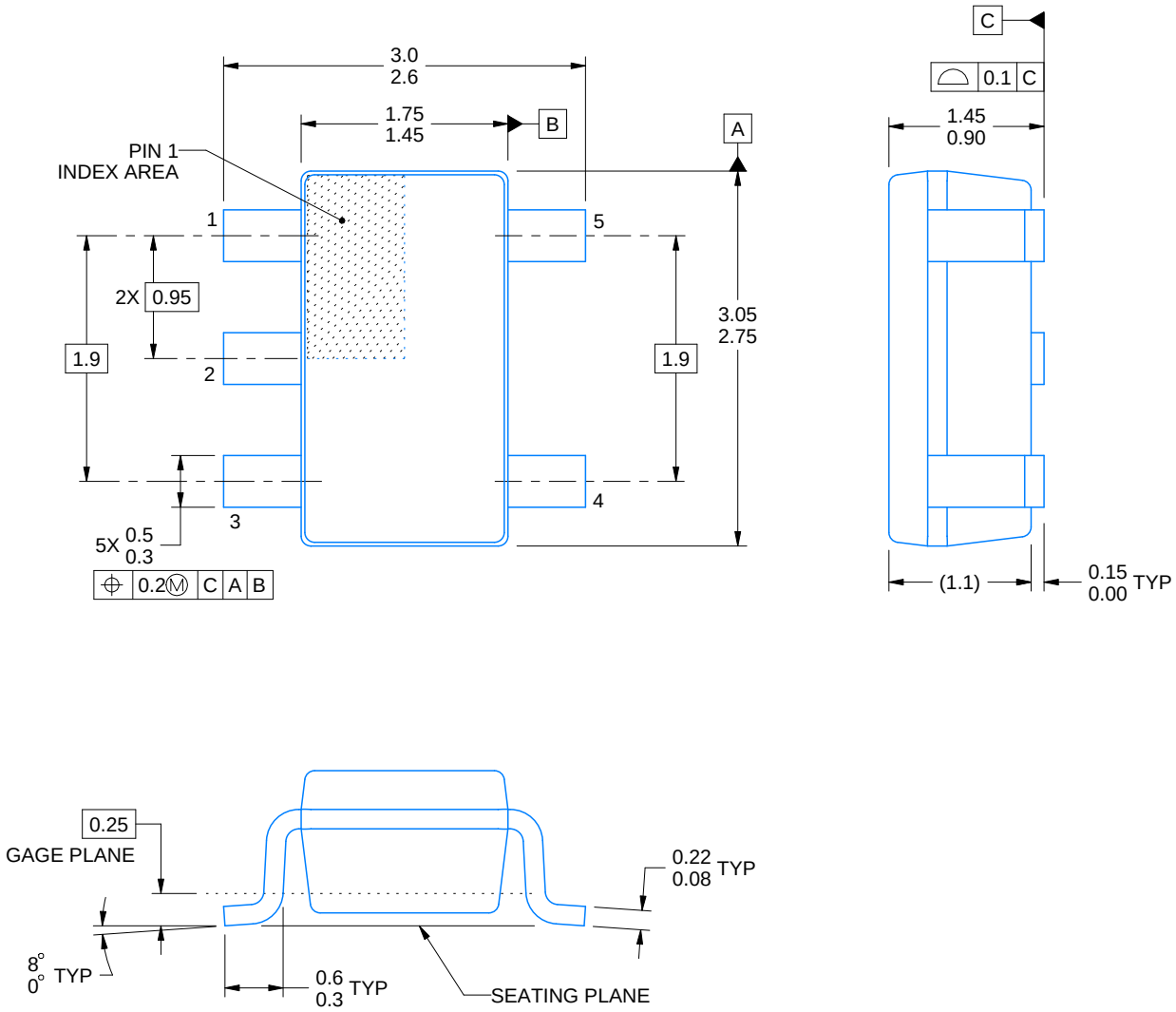
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

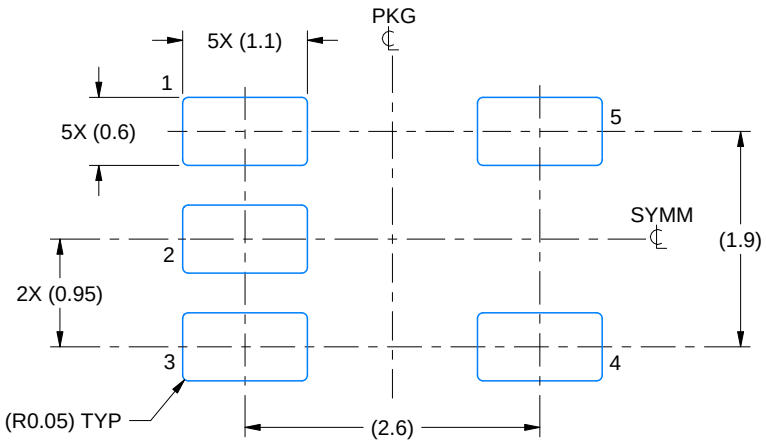
SMALL OUTLINE TRANSISTOR



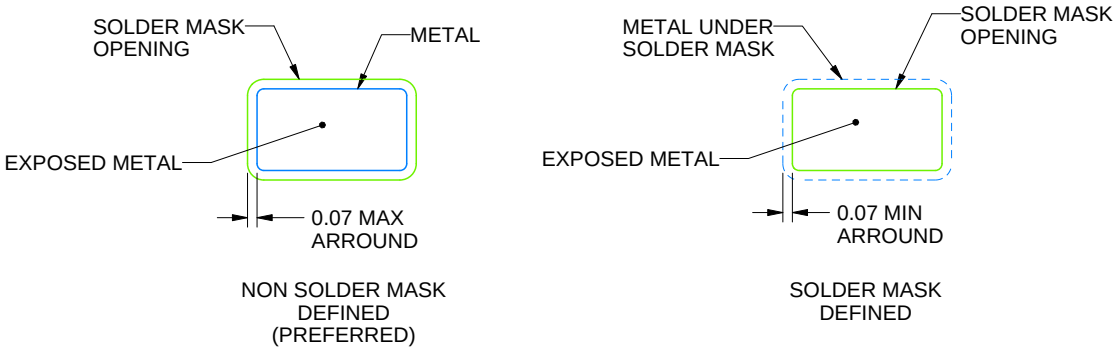
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

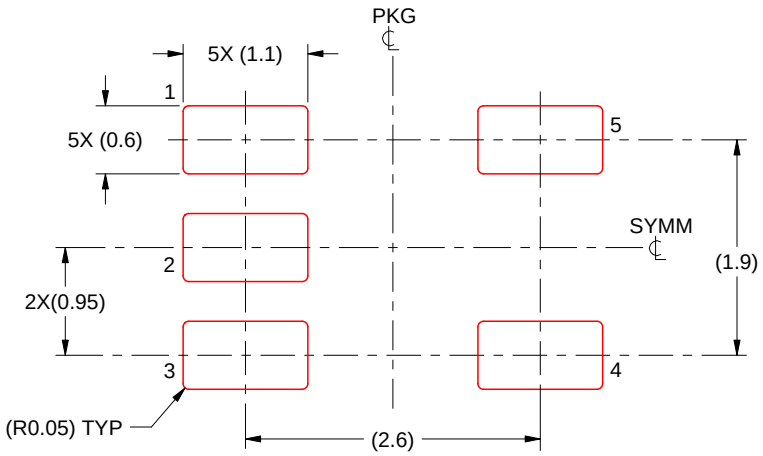


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



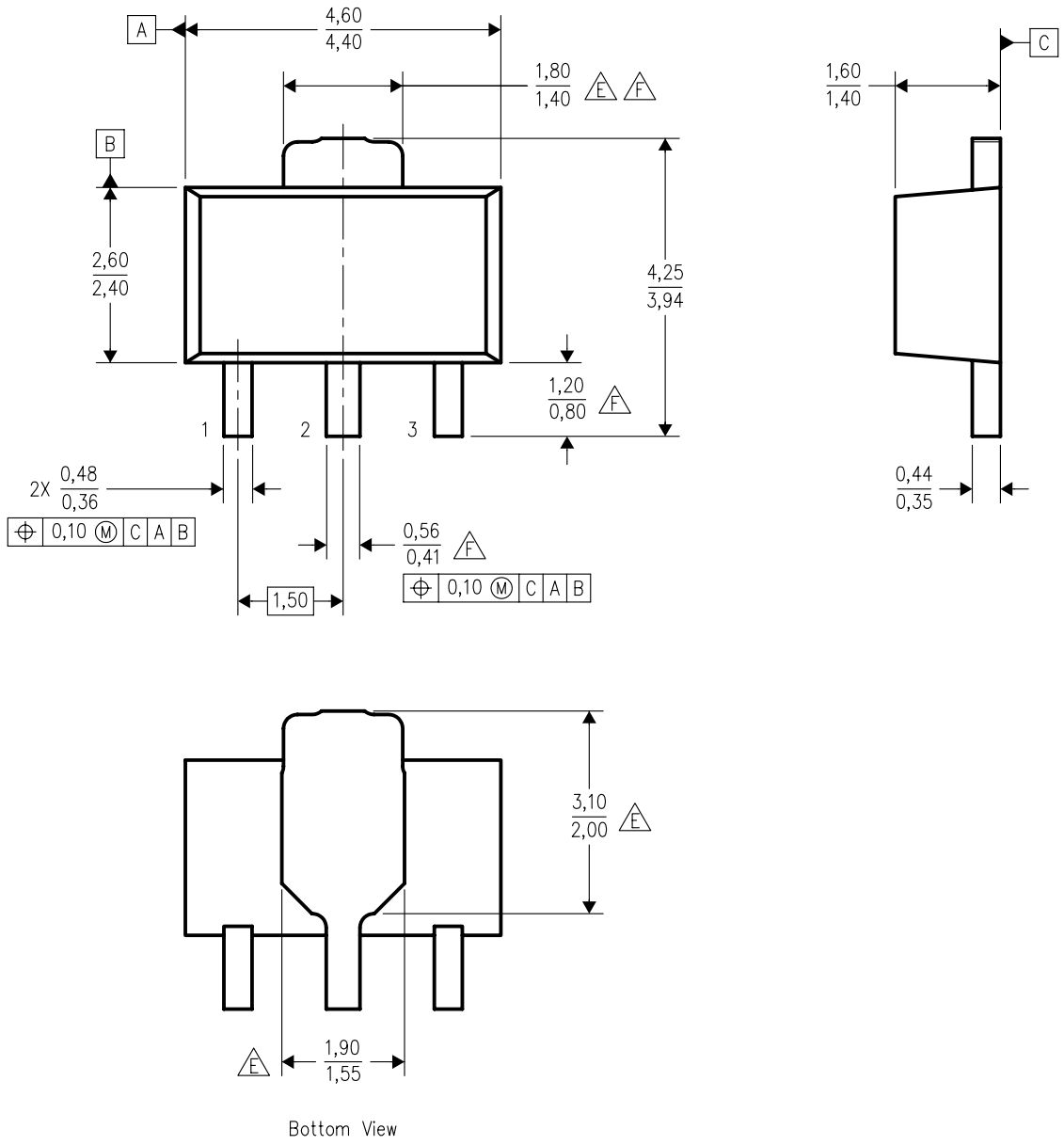
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

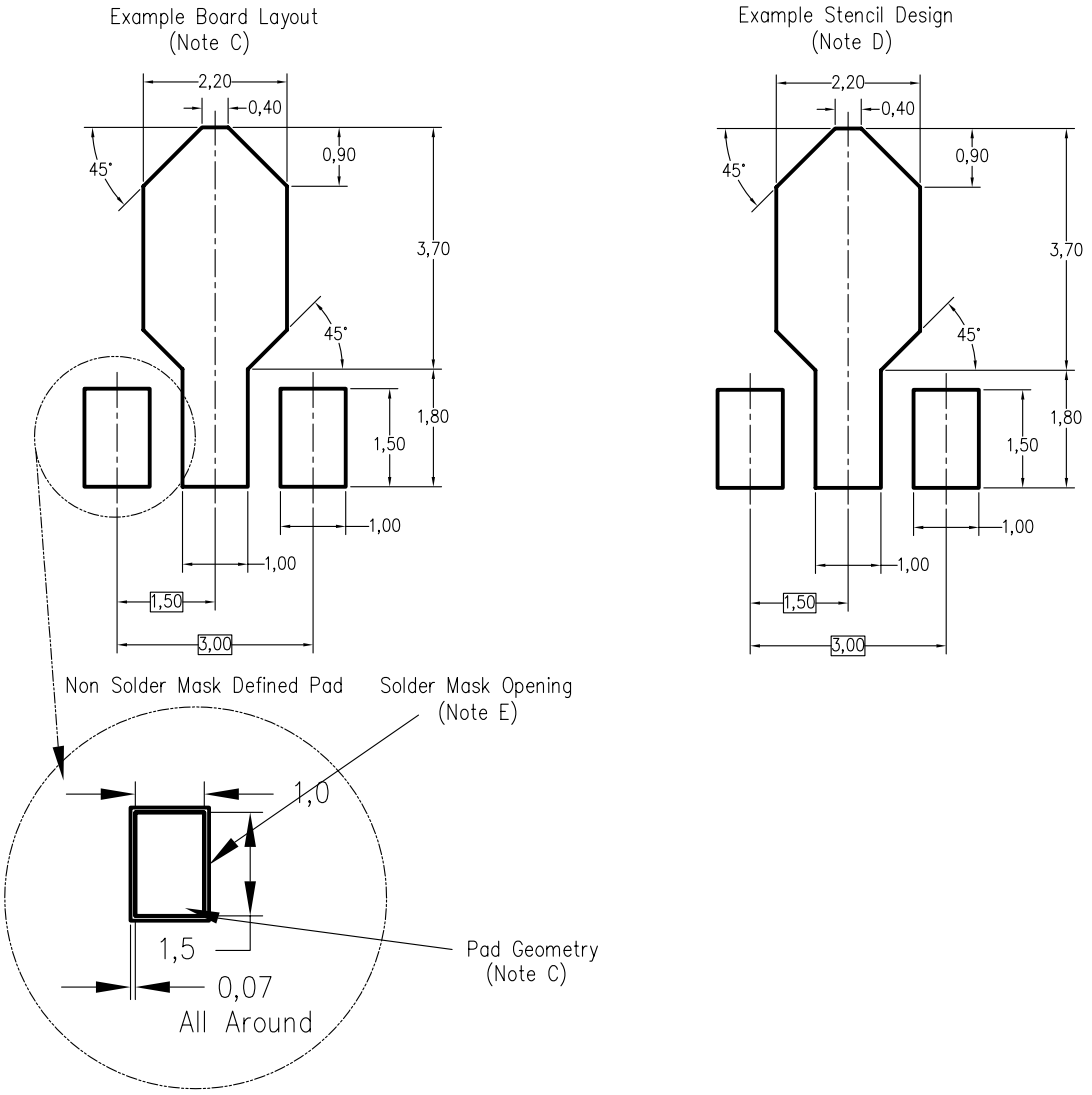
PK (R–PSSO–F3) PLASTIC SINGLE–IN–LINE PACKAGE



4040234/D 02/2006

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the tab.
D. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion not to exceed 0.15 per side.
E. Thermal pad contour optional within these dimensions.
F. Falls within JEDEC TO–243 variation AA, except minimum lead length, pin 2 minimum lead width, minimum tab width.

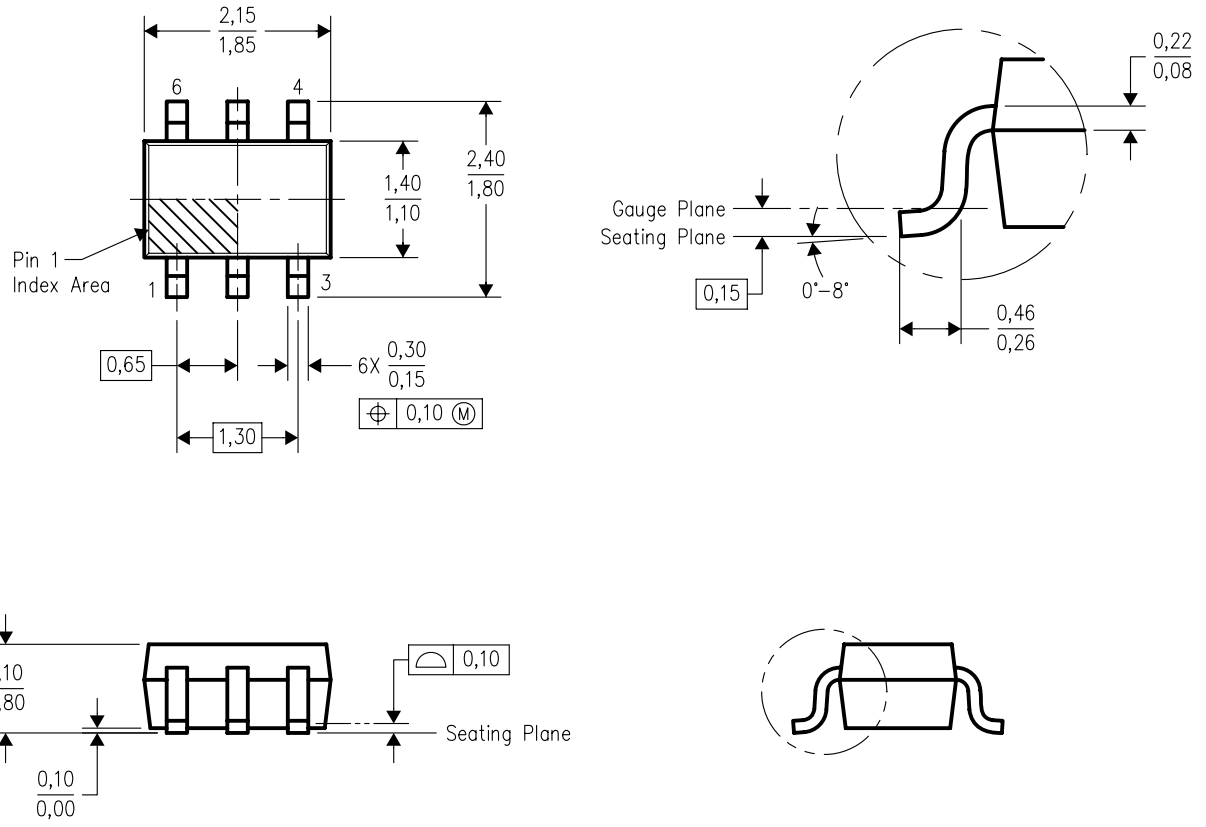
PK (R–PDSO–G3)



4208221/A 09/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

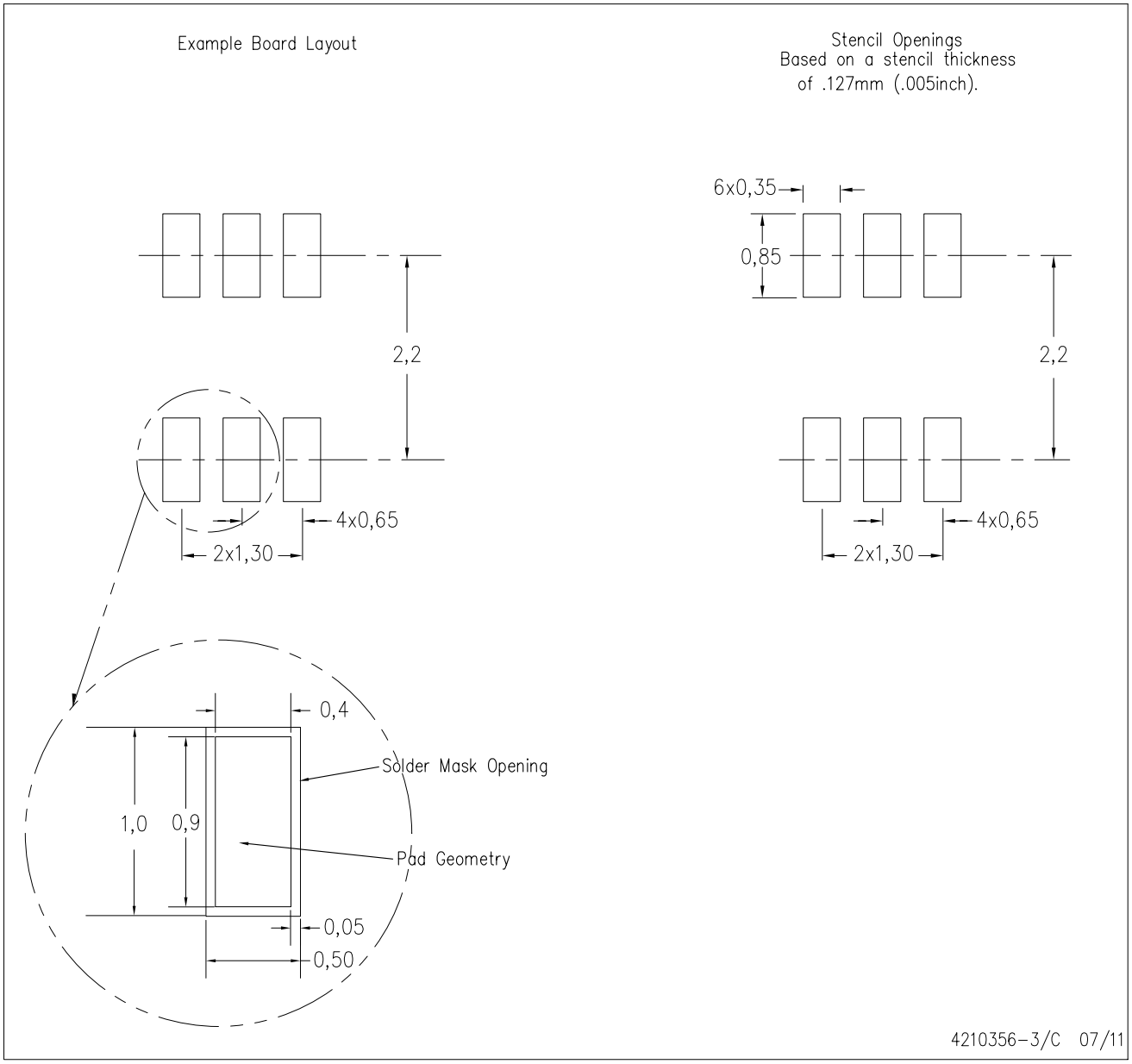
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



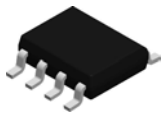
4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

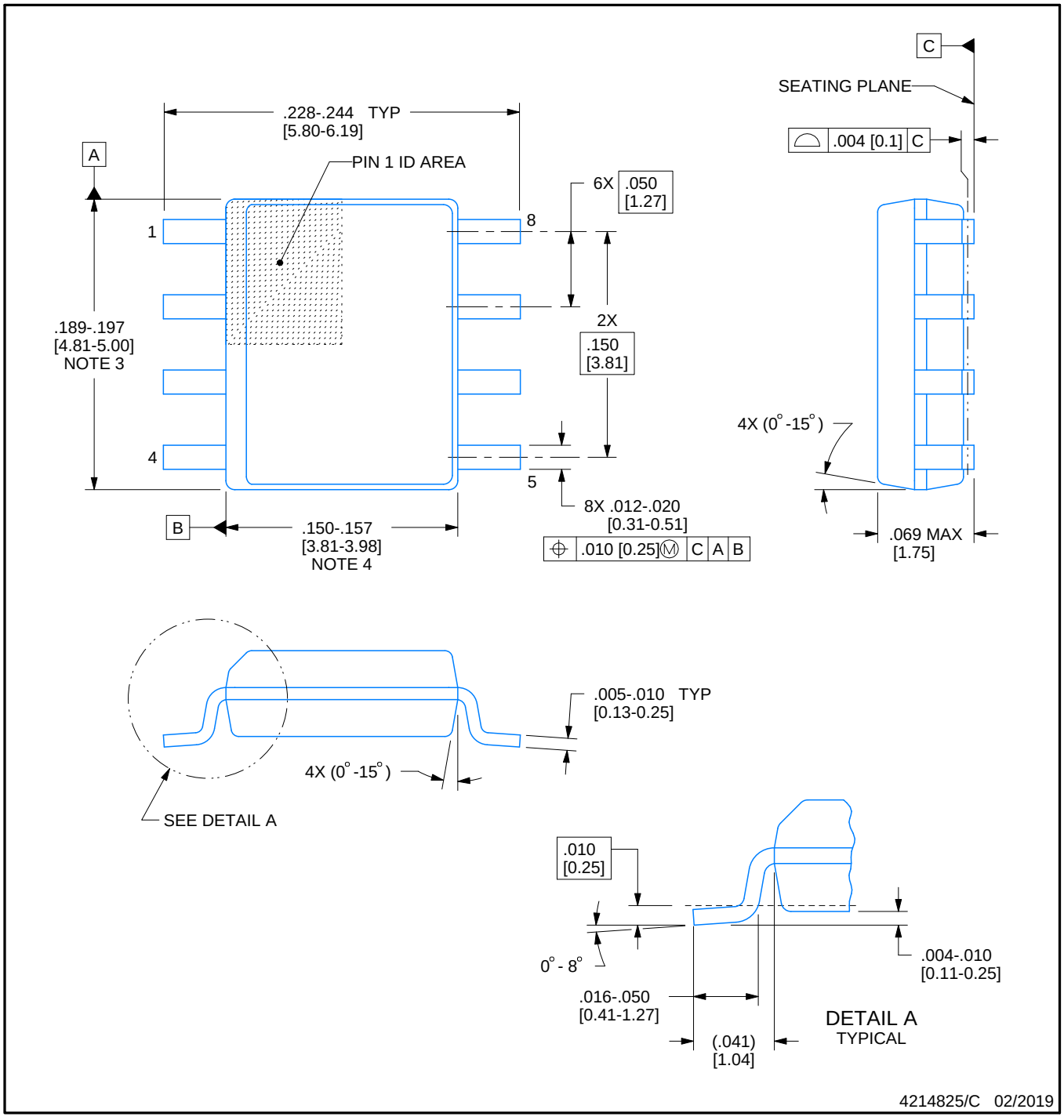


PACKAGE OUTLINE

D0008A

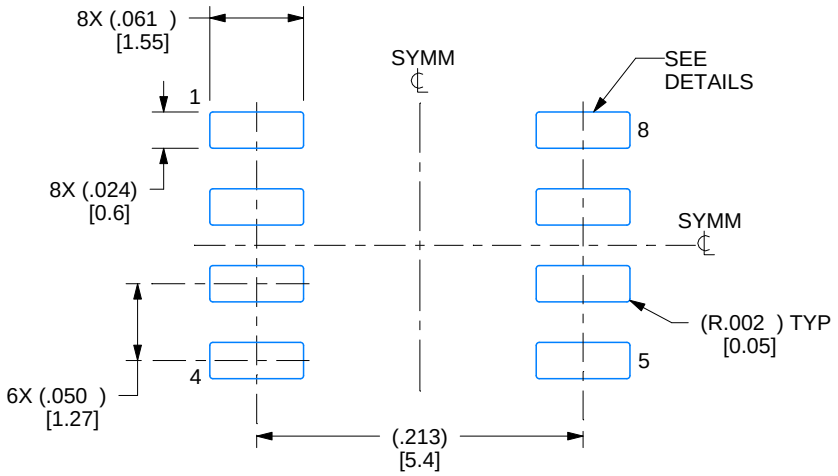
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

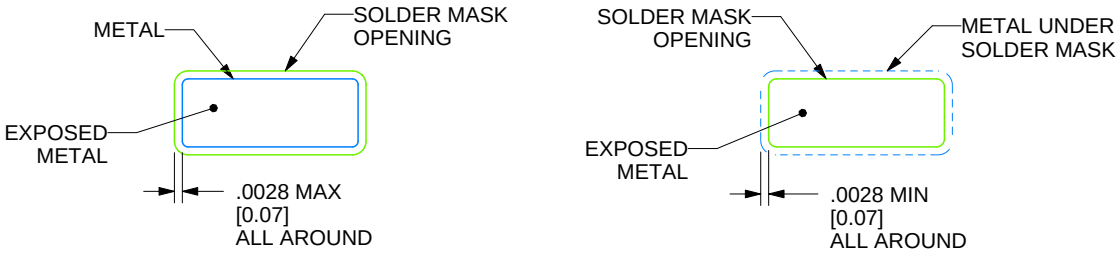


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

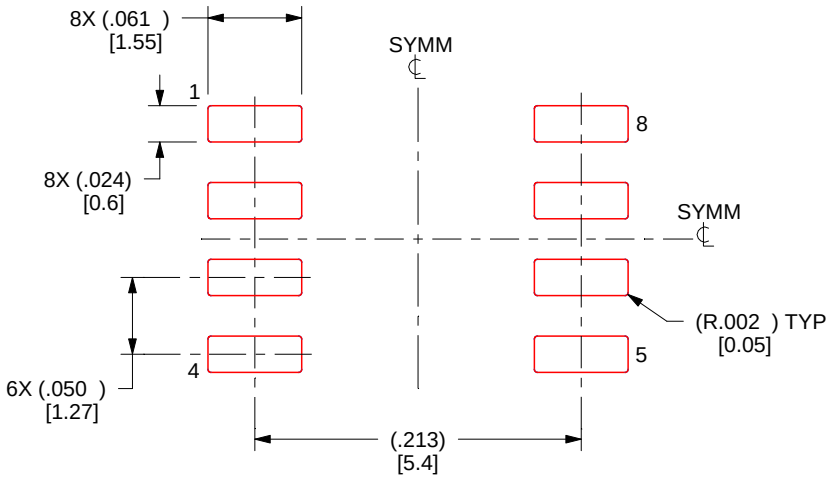
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

LP 3 TO-92 - 5.34 mm max height

TRANSISTOR OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

LP0003A

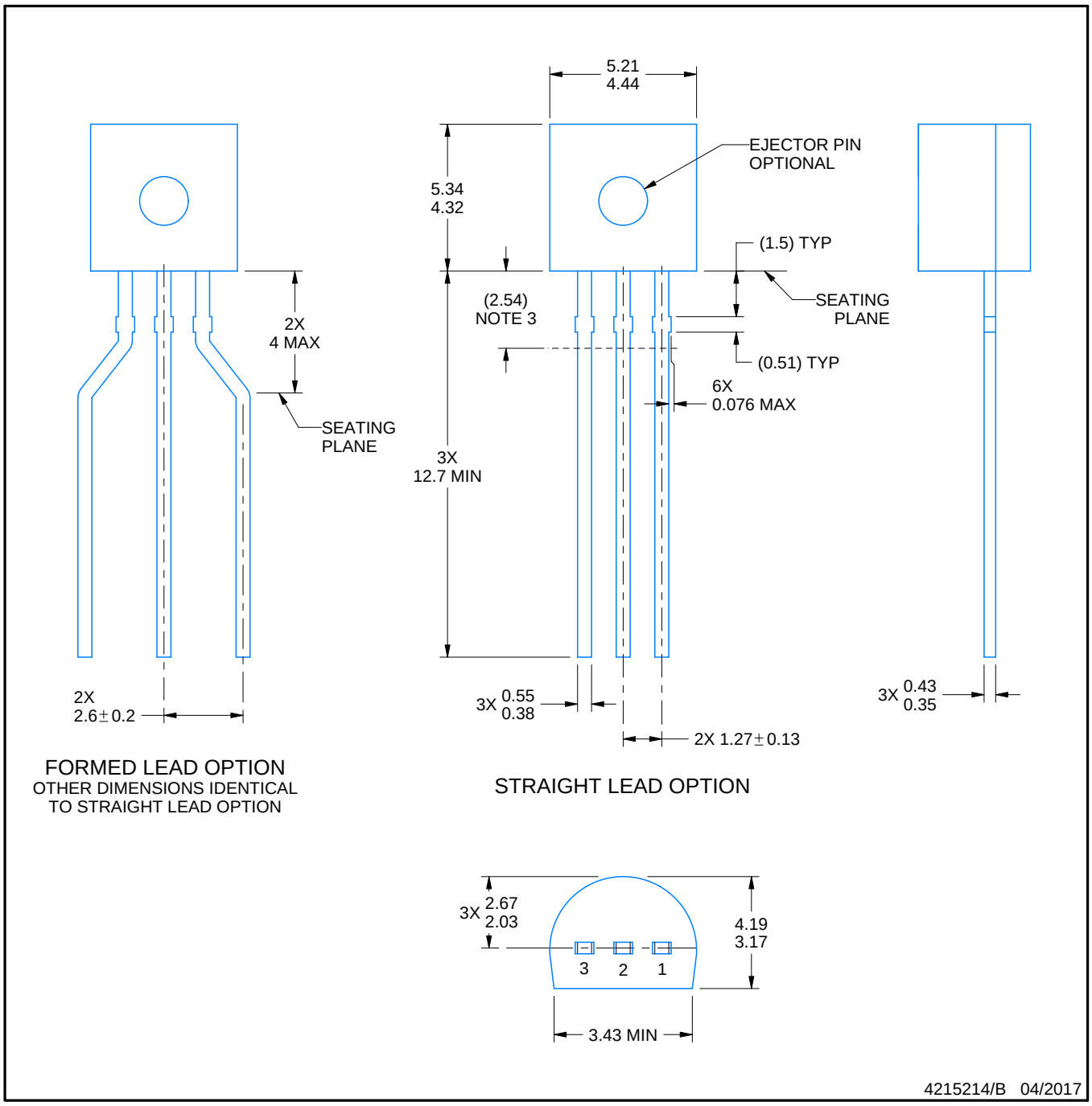




PACKAGE OUTLINE

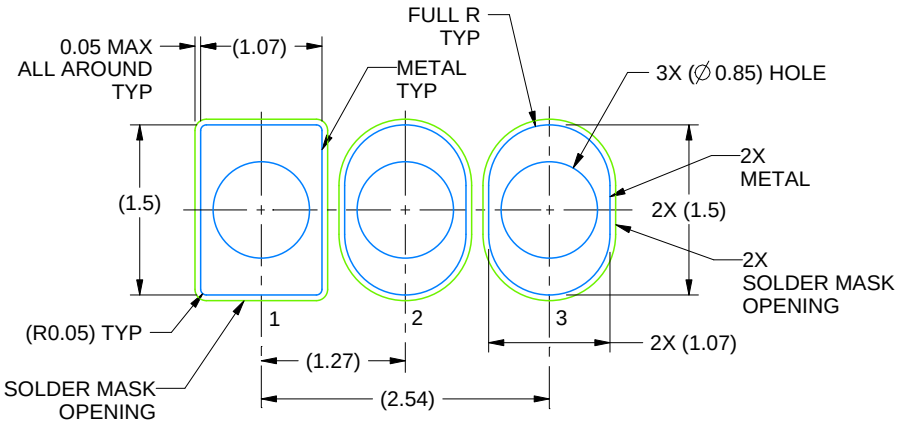
TO-92 - 5.34 mm max height

TO-92

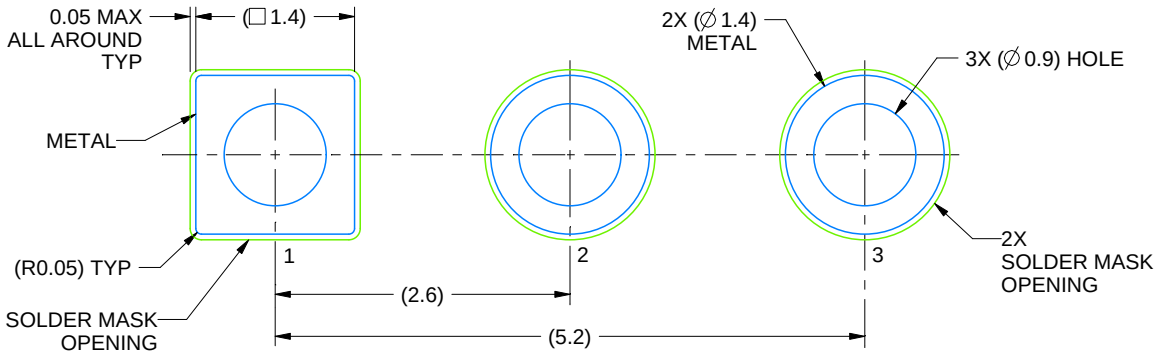


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



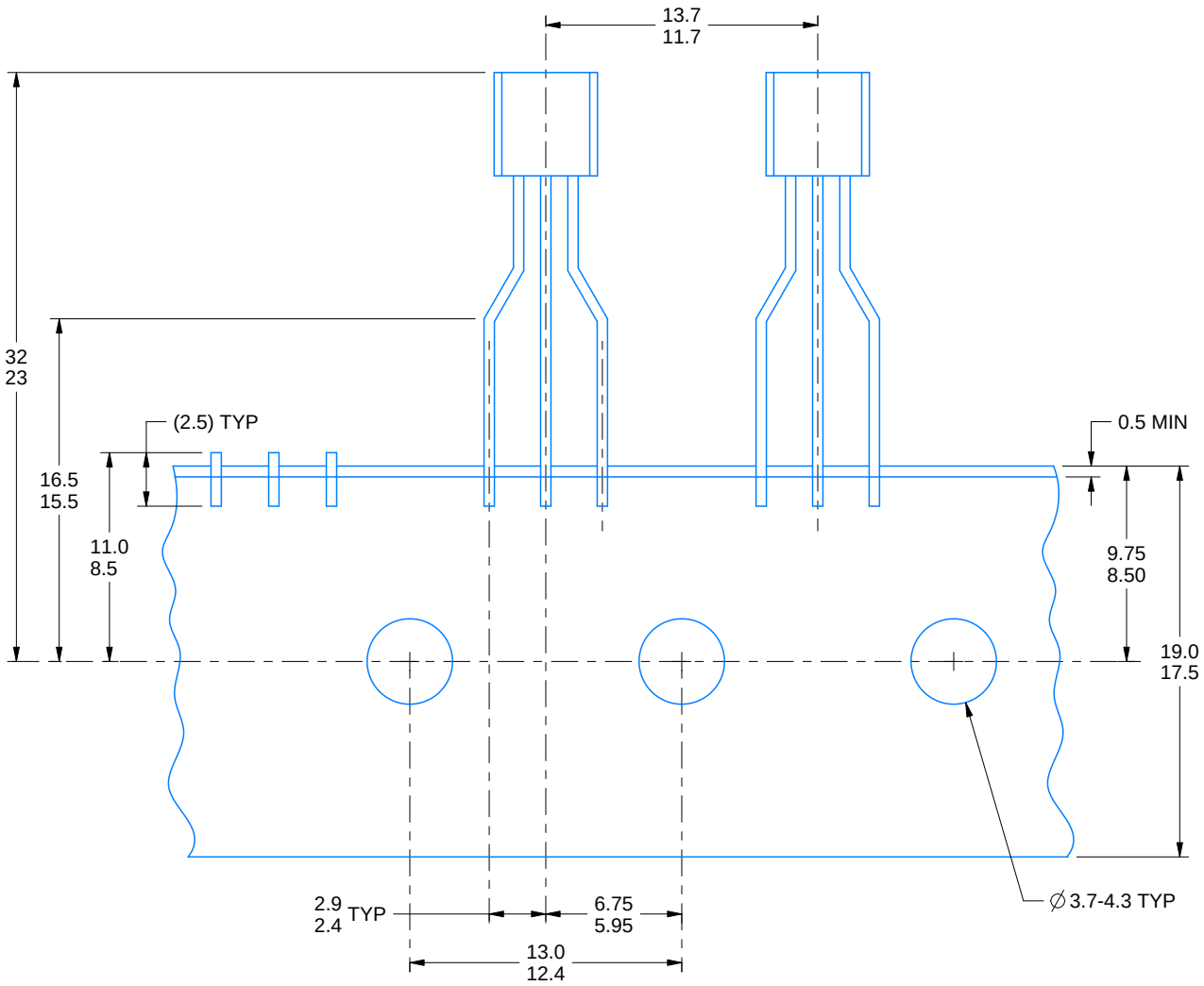
LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/B 04/2017

LP0003A

TO-92 - 5.34 mm max height

TO-92



FOR FORMED LEAD OPTION PACKAGE

4215214/B 04/2017

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