

TPA6211A1 3.1-W Mono Fully Differential Audio Power Amplifier

1 Features

- Designed for Wireless or Cellular Handsets and PDAs
- 3.1 W Into 3 Ω From a 5-V Supply at THD = 10% (Typ)
- Low Supply Current: 4 mA Typ at 5 V
- Shutdown Current: 0.01 μ A Typ
- Fast Startup With Minimal Pop
- Only Three External Components
 - Improved PSRR (–80 dB) and Wide Supply Voltage (2.5 V to 5.5 V) for Direct Battery Operation
 - Fully Differential Design Reduces RF Rectification
 - 63 dB CMRR Eliminates Two Input Coupling Capacitors

2 Applications

- Ideal for Wireless Handsets, PDAs, and Notebook Computers

3 Description

The TPA6211A1 is a 3.1-W mono fully-differential amplifier designed to drive a speaker with at least 3- Ω impedance while consuming only 20 mm² total printed-circuit board (PCB) area in most applications. The device operates from 2.5 V to 5.5 V, drawing only 4 mA of quiescent supply current. The TPA6211A1 is available in the space-saving 3-mm $\times$ 3-mm SON (DRB) and the 8-pin MSOP-PowerPAD™ (DGN) packages.

Features like –80 dB supply voltage rejection from 20 Hz to 2 kHz, improved RF rectification immunity, small PCB area, and a fast startup with minimal pop makes the TPA6211A1 ideal for PDA and smart phone applications.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPA6211A1	MSOP-PowerPAD (8)	3.00 mm $\times$ 3.00 mm
	SON (8)	3.00 mm $\times$ 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Circuit

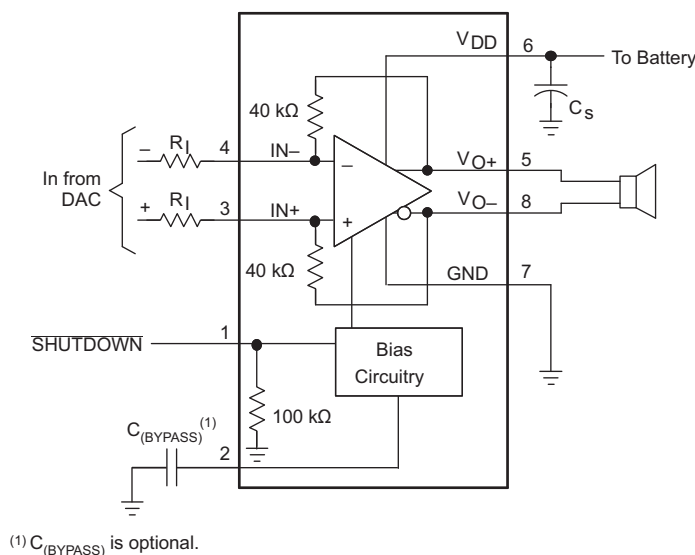


Table of Contents

1 Features	1	9.3 Feature Description.....	12
2 Applications	1	9.4 Device Functional Modes.....	17
3 Description	1	10 Application and Implementation	18
4 Revision History	2	10.1 Application Information.....	18
5 Device Comparison Table	3	10.2 Typical Application	18
6 Pin Configuration and Functions	3	10.3 System Examples	22
7 Specifications	4	11 Power Supply Recommendations	24
7.1 Absolute Maximum Ratings	4	11.1 Power Supply Decoupling Capacitor	24
7.2 ESD Ratings.....	4	12 Layout	24
7.3 Recommended Operation Conditions.....	4	12.1 Layout Guidelines	24
7.4 Thermal Information	4	12.2 Layout Examples.....	24
7.5 Electrical Characteristics.....	4	13 Device and Documentation Support	26
7.6 Operating Characteristics.....	5	13.1 Device Support.....	26
7.7 Dissipation Ratings	6	13.2 Documentation Support	26
7.8 Typical Characteristics.....	6	13.3 Community Resources.....	26
8 Parameter Measurement Information	11	13.4 Trademarks	26
9 Detailed Description	12	13.5 Electrostatic Discharge Caution.....	26
9.1 Overview	12	13.6 Glossary	26
9.2 Functional Block Diagram	12	14 Mechanical, Packaging, and Orderable Information	26

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (June 2011) to Revision E	Page
Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section.	1

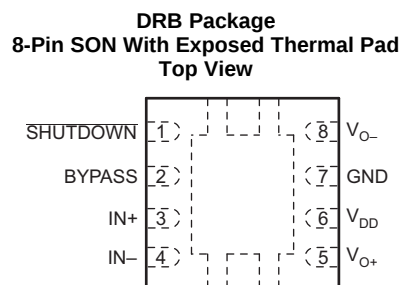
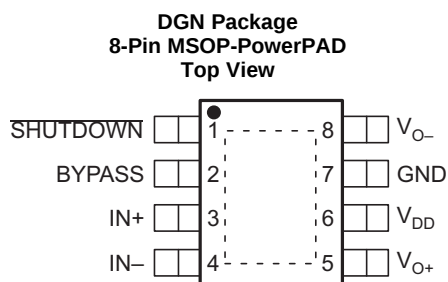
Changes from Revision C (June 2008) to Revision D	Page
Deleted the Lead temperature 1,6 mm (1/16 Inch) from case for 10 seconds row from the Abs Max Table	4

Changes from Revision B (August 2004) to Revision C	Page
Changed Storage temperature From: –65°C to 85°C To: –65°C to 150°C.....	4

5 Device Comparison Table

DEVICE NUMBER	SPEAKER CHANNELS	SPEAKER AMP TYPE	OUTPUT POWER (W)	PSRR (dB)
TPA6211A1	Mono	Class-AB	3.1	85
TPA6203A1	Mono	Class-AB	1.25	90
TPA6204A1	Mono	Class-AB	1.7	85
TPA6205a1	Mono	Class-AB	1.25	90

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BYPASS	2	–	Mid-supply voltage, adding a bypass capacitor improves PSRR
GND	7	I	High-current ground
IN+	3	I	Positive differential input
IN-	4	I	Negative differential input
SHUTDOWN	1	I	Shutdown terminal (active low logic)
V _{DD}	6	I	Power supply
V _{O+}	5	O	Positive BTL output
V _{O-}	8	O	Negative BTL output
Thermal Pad	–	–	Connect to ground. Thermal pad must be soldered down in all applications to properly secure device on the PCB.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted⁽¹⁾

	MIN	MAX	UNIT
V _D Supply voltage	−0.3	6	V
V _I Input voltage	−0.3	V _{DD} + 0.3	V
Continuous total power dissipation	See Dissipation Ratings		
T _A Operating free-air temperature	−40	85	°C
T _J Junction temperature	−40	150	°C
T _{stg} Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operation Conditions

	MIN	NOM	MAX	UNIT
V _{DD} Supply voltage	2.5		5.5	V
V _{IH} High-level input voltage	SHUTDOWN			V
V _{IL} Low-level input voltage	SHUTDOWN			V
T _A Operating free-air temperature	−40		85	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPA6211A1		UNIT
		DGN (MSOP-PowerPAD™)	DRB (SON)	
		8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	62.8	49.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	61.9	24.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	42.1	58.8	°C/W
ψ _{JT}	Junction-to-top characterization parameter	3.3	1.7	°C/W
ψ _{JB}	Junction-to-board characterization parameter	41.9	25	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	11	8.4	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OS} Output offset voltage (measured differentially)	V _I = 0 V differential, Gain = 1 V/V, V _{DD} = 5.5 V	−9	0.3	9	mV
PSRR Power supply rejection ratio	V _{DD} = 2.5 V to 5.5 V		−85	−60	dB
V _{IC} Common mode input range	V _{DD} = 2.5 V to 5.5 V	0.5		V _{DD} − 0.8	V

Electrical Characteristics (continued)

 $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMRR	Common mode rejection ratio	$V_{DD} = 5.5\text{ V}$, $V_{IC} = 0.5\text{ V to } 4.7\text{ V}$		-63	-40	dB
		$V_{DD} = 2.5\text{ V}$, $V_{IC} = 0.5\text{ V to } 1.7\text{ V}$		-63	-40	
Low-output swing		$R_L = 4\ \Omega$, $V_{IN+} = V_{DD}$, $V_{IN-} = 0\text{ V}$, Gain = 1 V/V, $V_{IN-} = 0\text{ V or } V_{DD}$	$V_{DD} = 5.5\text{ V}$	0.45		V
			$V_{DD} = 3.6\text{ V}$	0.37		
			$V_{DD} = 2.5\text{ V}$	0.26	0.4	
High-output swing		$R_L = 4\ \Omega$, $V_{IN+} = V_{DD}$, $V_{IN-} = V_{DD}$, Gain = 1 V/V, $V_{IN-} = 0\text{ V or } V_{DD}$	$V_{DD} = 5.5\text{ V}$	4.95		V
			$V_{DD} = 3.6\text{ V}$	3.18		
			$V_{DD} = 2.5\text{ V}$	2	2.13	
$ I_{IH} $	High-level input current, shutdown	$V_{DD} = 5.5\text{ V}$, $V_I = 5.8\text{ V}$		58	100	μA
$ I_{IL} $	Low-level input current, shutdown	$V_{DD} = 5.5\text{ V}$, $V_I = -0.3\text{ V}$		3	100	μA
I_Q	Quiescent current	$V_{DD} = 2.5\text{ V to } 5.5\text{ V}$, no load		4	5	mA
$I_{(SD)}$	Supply current	$V(\text{SHUTDOWN}) \leq 0.5\text{ V}$, $V_{DD} = 2.5\text{ V to } 5.5\text{ V}$, $R_L = 4\ \Omega$		0.01	1	μA
Gain		$R_L = 4\ \Omega$	$\frac{38\text{ k}\Omega}{R_I}$	$\frac{40\text{ k}\Omega}{R_I}$	$\frac{42\text{ k}\Omega}{R_I}$	V/V
Resistance from shutdown to GND				100		k Ω

7.6 Operating Characteristics

 $T_A = 25^\circ\text{C}$, Gain = 1 V/V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power	THD + N= 1%, $f = 1\text{ kHz}$, $R_L = 3\ \Omega$	$V_{DD} = 5\text{ V}$	2.45		W
			$V_{DD} = 3.6\text{ V}$	1.22		
			$V_{DD} = 2.5\text{ V}$	0.49		
		THD + N= 1%, $f = 1\text{ kHz}$, $R_L = 4\ \Omega$	$V_{DD} = 5\text{ V}$	2.22		
			$V_{DD} = 3.6\text{ V}$	1.1		
			$V_{DD} = 2.5\text{ V}$	0.47		
		THD + N= 1%, $f = 1\text{ kHz}$, $R_L = 8\ \Omega$	$V_{DD} = 5\text{ V}$	1.36		
			$V_{DD} = 3.6\text{ V}$	0.72		
			$V_{DD} = 2.5\text{ V}$	0.33		
THD+N	Total harmonic distortion plus noise	$f = 1\text{ kHz}$, $R_L = 3\ \Omega$	$P_O = 2\text{ W}$, $V_{DD} = 5\text{ V}$	0.045%		
			$P_O = 1\text{ W}$, $V_{DD} = 3.6\text{ V}$	0.05%		
			$P_O = 300\text{ mW}$, $V_{DD} = 2.5\text{ V}$	0.06%		
		$f = 1\text{ kHz}$, $R_L = 4\ \Omega$	$P_O = 1.8\text{ W}$, $V_{DD} = 5\text{ V}$	0.03%		
			$P_O = 0.7\text{ W}$, $V_{DD} = 3.6\text{ V}$	0.03%		
			$P_O = 300\text{ mW}$, $V_{DD} = 2.5\text{ V}$	0.04%		
		$f = 1\text{ kHz}$, $R_L = 8\ \Omega$	$P_O = 1\text{ W}$, $V_{DD} = 5\text{ V}$	0.02%		
			$P_O = 0.5\text{ W}$, $V_{DD} = 3.6\text{ V}$	0.02%		
			$P_O = 200\text{ mW}$, $V_{DD} = 2.5\text{ V}$	0.03%		
k_{SVR}	Supply ripple rejection ratio	$V_{DD} = 3.6\text{ V}$, Inputs ac-grounded with $C_I = 2\ \mu\text{F}$, $V_{(RIPPLE)} = 200\text{ mV}_{pp}$	$f = 217\text{ Hz}$	-80		dB
			$f = 20\text{ Hz to } 20\text{ kHz}$	-70		
SNR	Signal-to-noise ratio	$V_{DD} = 5\text{ V}$, $P_O = 2\text{ W}$, $R_L = 4\ \Omega$		105		dB
V_n	Output voltage noise	$V_{DD} = 3.6\text{ V}$, $f = 20\text{ Hz to } 20\text{ kHz}$, Inputs ac-grounded with $C_I = 2\ \mu\text{F}$	No weighting	15		μV_{RMS}
			A weighting	12		
CMRR	Common mode rejection ratio	$V_{DD} = 3.6\text{ V}$, $V_{IC} = 1\text{ V}_{pp}$	$f = 217\text{ Hz}$	-65		dB
Z_I	Input impedance		38	40	44	k Ω

Operating Characteristics (continued)

 $T_A = 25^{\circ}\text{C}$, Gain = 1 V/V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up time from shutdown	$V_{DD} = 3.6\text{ V}$, No C_{BYPASS}		4		μs
	$V_{DD} = 3.6\text{ V}$, $C_{BYPASS} = 0.1\text{ }\mu\text{F}$		27		ms

7.7 Dissipation Ratings

PACKAGE	$T_A \leq 25^{\circ}\text{C}$ POWER RATING	DERATING FACTOR ⁽¹⁾	$T_A = 70^{\circ}\text{C}$ POWER RATING	$T_A = 85^{\circ}\text{C}$ POWER RATING
DGN	2.13 W	17.1 mW/ $^{\circ}\text{C}$	1.36 W	1.11 W
DRB	2.7 W	21.8 mW/ $^{\circ}\text{C}$	1.7 W	1.4 W

(1) Derating factor based on high-k board layout.

7.8 Typical Characteristics

Table 1. Table of Graphs

			FIGURE
P_O Output power	vs Supply voltage		Figure 1
	vs Load resistance		Figure 2
P_D Power dissipation	vs Output power		Figure 3, Figure 4
THD+N Total harmonic distortion + noise	vs Output power		Figure 5, Figure 6, Figure 7
	vs Frequency		Figure 8, Figure 9, Figure 10, Figure 11, , Figure 12
	vs Common-mode input voltage		Figure 13
K_{SVR} Supply voltage rejection ratio	vs Frequency		Figure 14, Figure 15, Figure 16, Figure 17
K_{SVR} Supply voltage rejection ratio	vs Common-mode input voltage		Figure 18
GSM Power supply rejection	vs Time		Figure 19
GSM Power supply rejection	vs Frequency		Figure 20
CMRR Common-mode rejection ratio	vs Frequency		Figure 21
	vs Common-mode input voltage		Figure 22
Closed loop gain/phase	vs Frequency		Figure 23
Open loop gain/phase	vs Frequency		Figure 24
I_{DD} Supply current	vs Supply voltage		Figure 25
	vs Shutdown voltage		Figure 26
Start-up time	vs Bypass capacitor		Figure 27

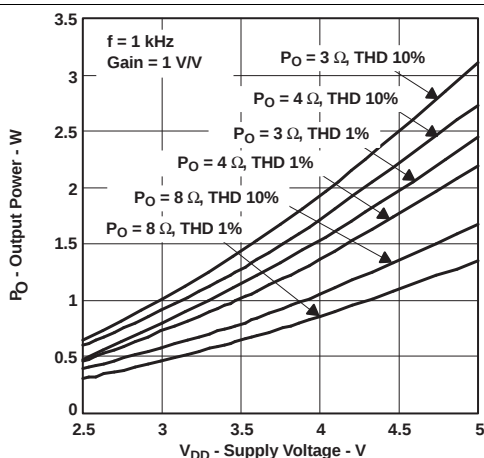


Figure 1. Output Power vs Supply Voltage

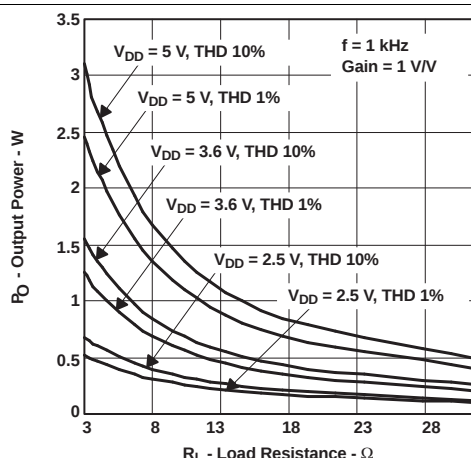


Figure 2. Output Power vs Load Resistance

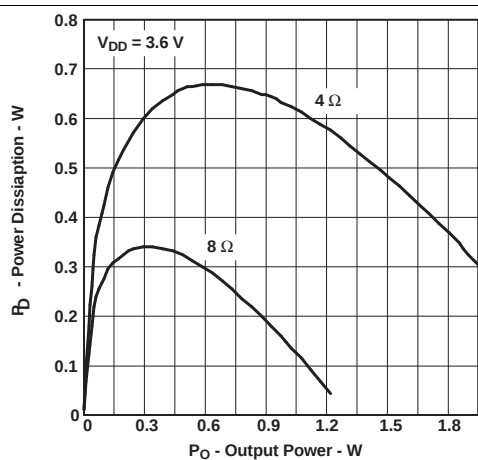


Figure 3. Power Dissipation vs Output Power

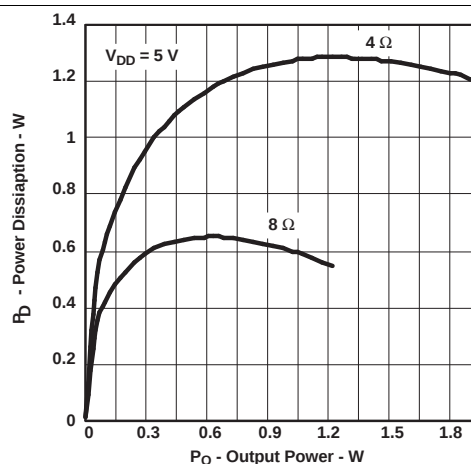


Figure 4. Power Dissipation vs Output Power

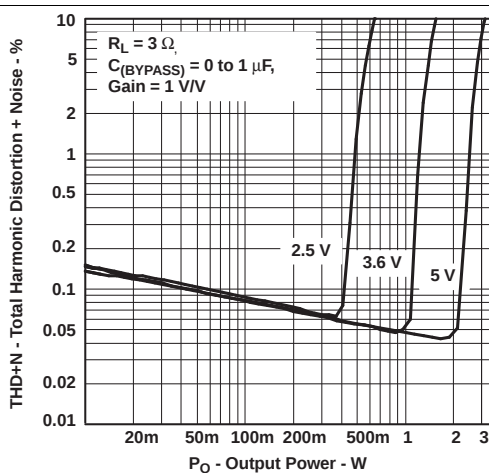


Figure 5. Total Harmonic Distortion + Noise vs Output Power

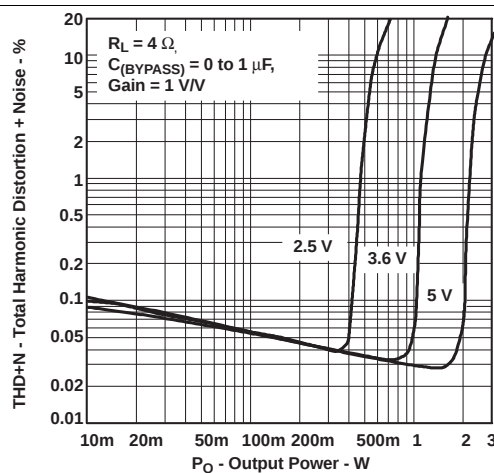


Figure 6. Total Harmonic Distortion + Noise vs Output Power

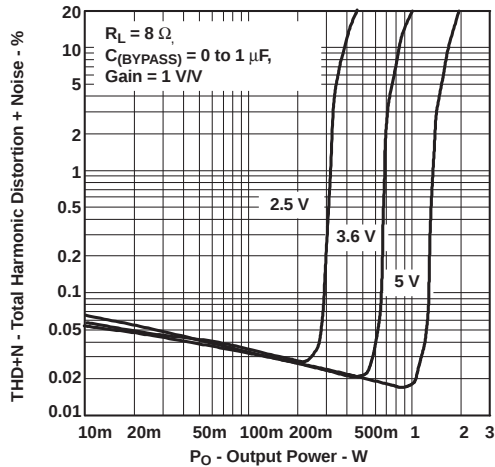


Figure 7. Total Harmonic Distortion + Noise vs Output Power

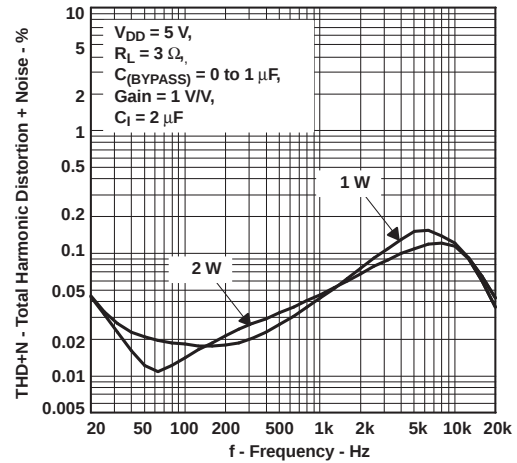


Figure 8. Total Harmonic Distortion + Noise vs Frequency

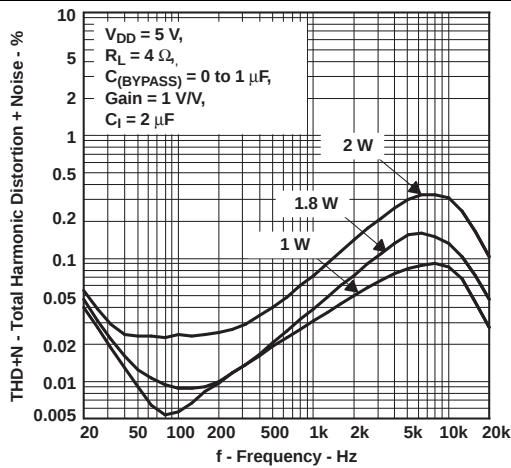


Figure 9. Total Harmonic Distortion + Noise vs Frequency

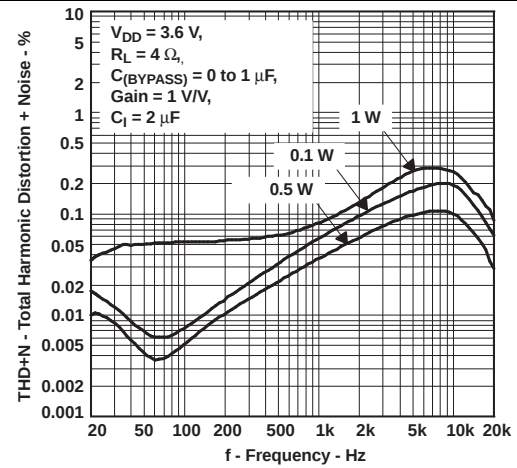


Figure 10. Total Harmonic Distortion + Noise vs Frequency

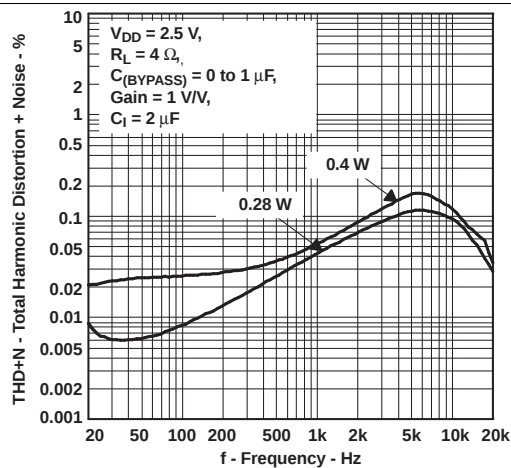


Figure 11. Total Harmonic Distortion + Noise vs Frequency

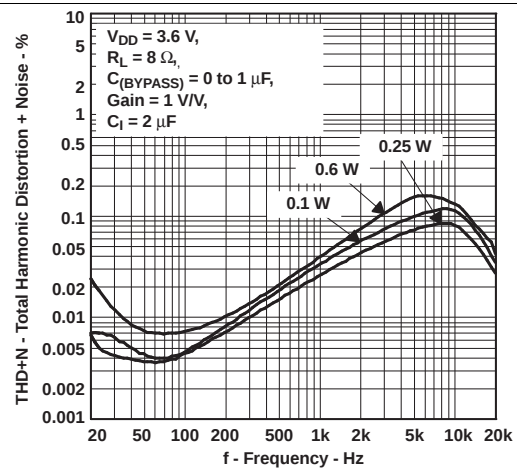


Figure 12. Total Harmonic Distortion + Noise vs Frequency

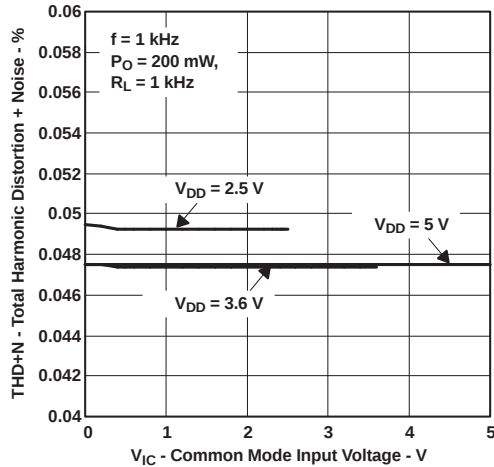


Figure 13. Total Harmonic Distortion + Noise vs Common Mode Input Voltage

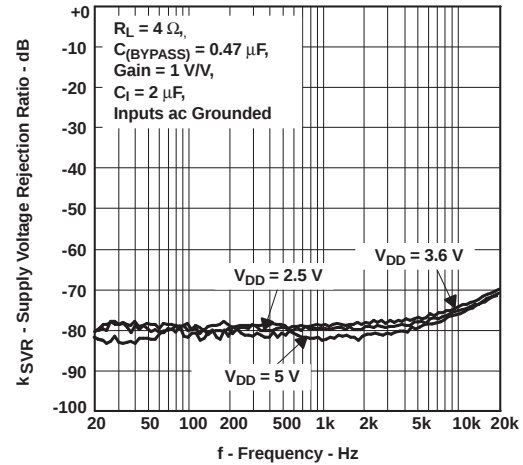


Figure 14. Supply Voltage Rejection Ratio vs Frequency

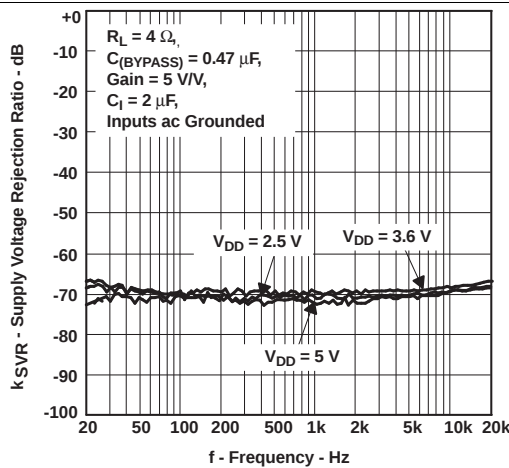


Figure 15. Supply Voltage Rejection Ratio vs Frequency

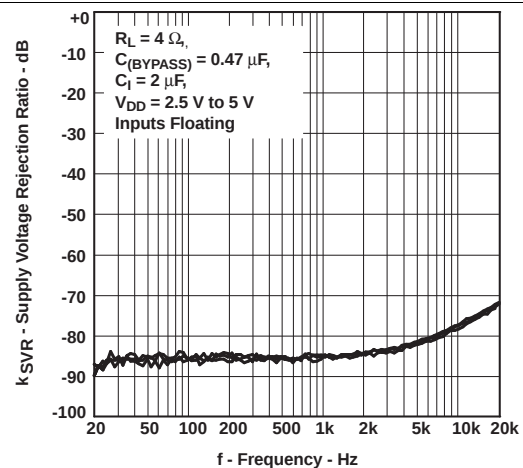


Figure 16. Supply Voltage Rejection Ratio vs Frequency

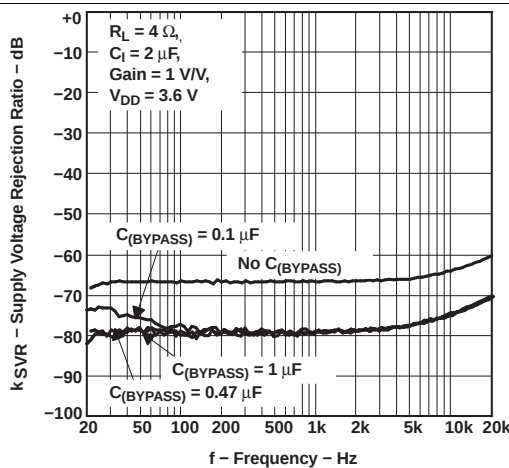


Figure 17. Supply Voltage Rejection Ratio vs Frequency

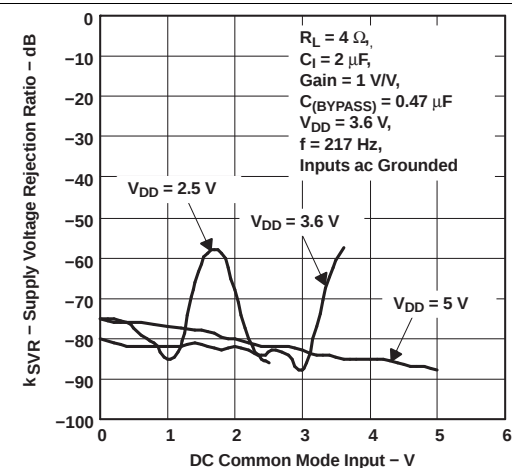
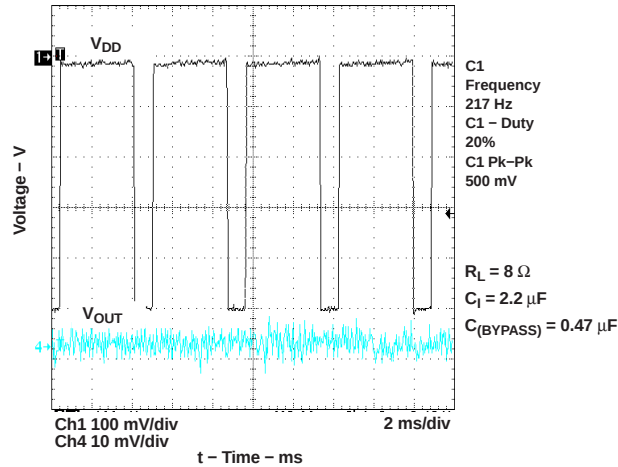
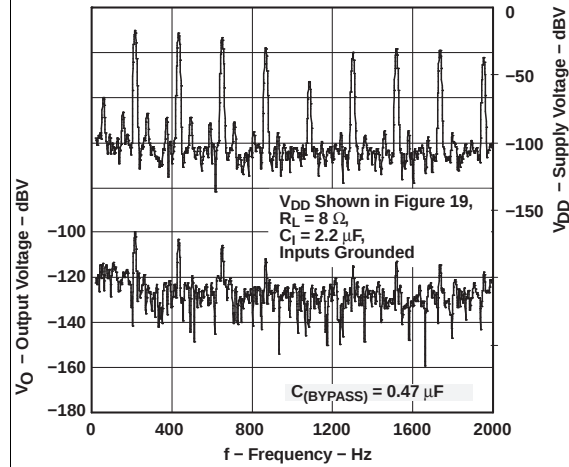
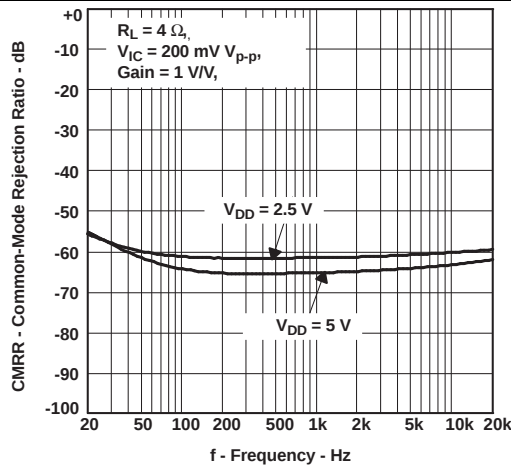
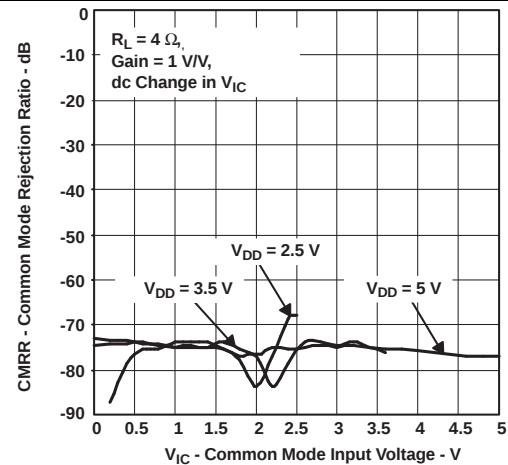
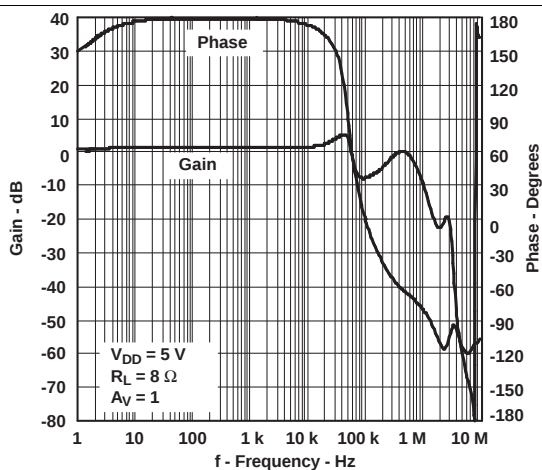
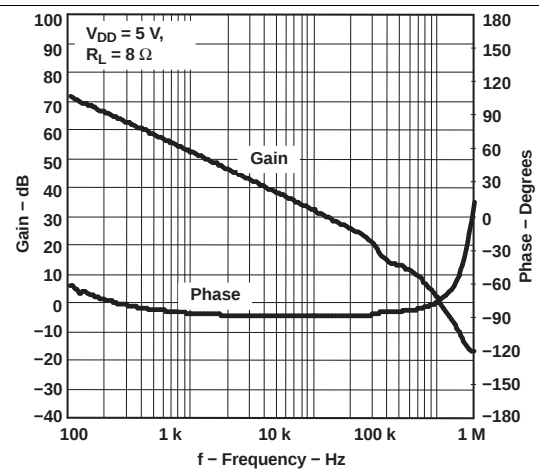


Figure 18. Supply Voltage Rejection Ratio vs DC Common Mode Input

TPA6211A1

SLOS367E –AUGUST 2003–REVISED NOVEMBER 2015

www.ti.com

Figure 19. GSM Power Supply Rejection vs Time

Figure 20. GSM Power Supply Rejection vs Frequency

Figure 21. Common Mode Rejection Ratio vs Frequency

Figure 22. Common-Mode Rejection Ratio vs Common-Mode Input Voltage

Figure 23. Closed Loop Gain/Phase vs Frequency

Figure 24. Open Loop Gain/Phase vs Frequency

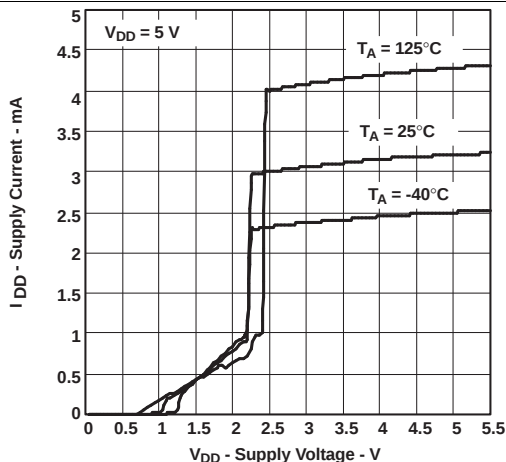


Figure 25. Supply Current vs Supply Voltage

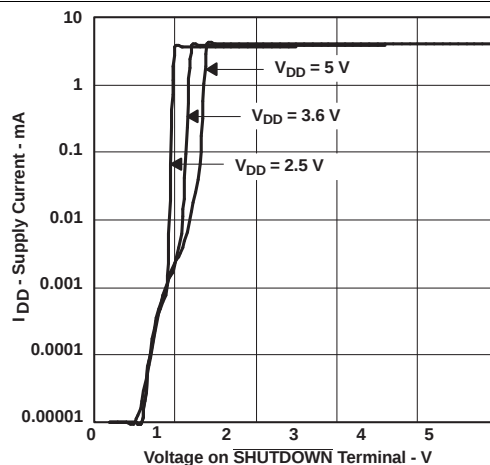


Figure 26. Supply Current vs Shutdown Voltage

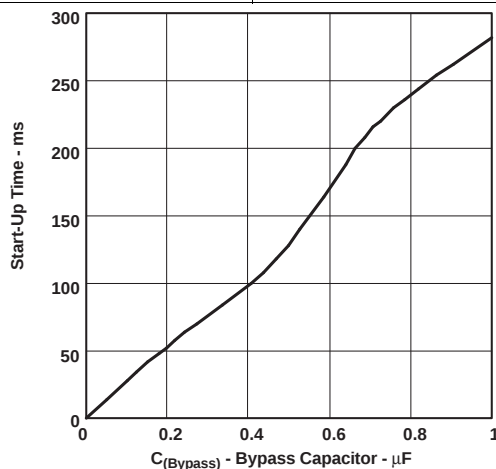


Figure 27. Start-Up Time vs Bypass Capacitor

8 Parameter Measurement Information

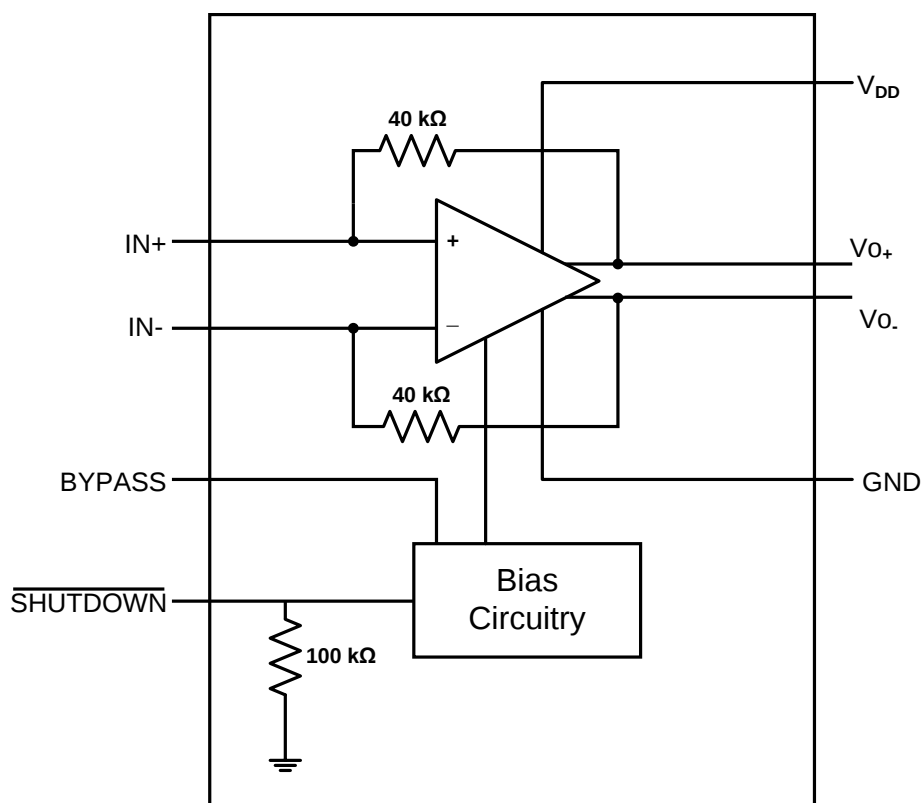
All parameters are measured according to the conditions described in [Specifications](#) section.

9 Detailed Description

9.1 Overview

The TPA6211A1 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around $V_{DD}/2$ regardless of the common-mode voltage at the input.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Fully Differential Amplifier Efficiency and Thermal Information

Class-AB amplifiers are inefficient, primarily because of voltage drop across the output-stage transistors. The two components of this internal voltage drop are the headroom or dc voltage drop that varies inversely to output power, and the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD} . The internal voltage drop multiplied by the average value of the supply current, $I_{DD}(avg)$, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see [Figure 28](#)).

Feature Description (continued)

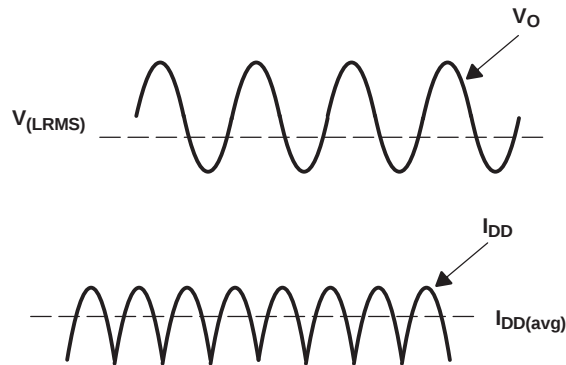


Figure 28. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

These definitions are true for the following equations:

- η_{BTL} = Efficiency of a BTL amplifier
- P_L = Power delivered to load
- P_{SUP} = Power drawn from power supply
- V_{LRMS} = RMS voltage on BTL load
- V_P = Peak voltage on BTL load
- V_{DD} = Power supply voltage
- I_{DDavg} = Average current drawn from the power supply

Use [Equation 1](#) to calculate the efficiency of a BTL amplifier.

$$\eta_{\text{BTL}} = \frac{P_L}{P_{\text{SUP}}}$$

where

$$\begin{aligned} & \bullet \quad P_L = \frac{V_{\text{LRMS}}^2}{R_L} \\ & \quad \text{where} \\ & \quad V_{\text{LRMS}} = \frac{V_P}{\sqrt{2}} \\ & \quad \text{therefore} \\ & \quad P_L = \frac{V_P^2}{2R_L} \\ & \bullet \quad P_{\text{SUP}} = V_{\text{DD}} I_{\text{DDavg}} \\ & \quad \text{where} \\ & \quad I_{\text{DDavg}} = \frac{1}{\pi} \int_0^\pi \frac{V_P}{R_L} \sin(t) dt = -\frac{1}{\pi} \times \frac{V_P}{R_L} [\cos(t)]_0^\pi = \frac{2V_P}{\pi R_L} \\ & \quad \text{therefore} \\ & \quad P_{\text{SUP}} = \frac{2V_{\text{DD}} V_P}{\pi R_L} \end{aligned} \tag{1}$$

Feature Description (continued)

Using these values, substitute P_L and P_{SUP} from Equation 1 as shown in Equation 2.

$$\eta_{BTL} = \frac{\frac{V_P^2}{2R_L}}{\frac{2V_{DD}V_P}{\pi R_L}} = \frac{\pi V_P}{4V_{DD}}$$

where

$$V_P = \sqrt{2P_L R_L} \quad (2)$$

Therefore, η_{BTL} can be calculated using Equation 3.

$$\eta_{BTL} = \frac{\pi \sqrt{2P_L R_L}}{4V_{DD}} \quad (3)$$

Table 2. Efficiency and Maximum Ambient Temperature vs Output Power

OUTPUT POWER (W)	EFFICIENCY (%)	INTERNAL DISSIPATION (W)	POWER FROM SUPPLY (W)	MAX AMBIENT TEMPERATURE ⁽¹⁾ (°C)
5-V, 3-Ω Systems				
0.5	27.2	1.34	1.84	85 ⁽²⁾
1	38.4	1.6	2.6	76
2.45	60.2	1.62	4.07	75
3.1	67.7	1.48	4.58	82
5-V, 4-Ω BTL Systems				
0.5	31.4	1.09	1.59	85 ⁽²⁾
1	44.4	1.25	2.25	85 ⁽²⁾
2	62.8	1.18	3.18	85 ⁽²⁾
2.8	74.3	0.97	3.77	85 ⁽²⁾
5-V, 8-Ω Systems				
0.5	44.4	0.625	1.13	85 ⁽²⁾
1	62.8	0.592	1.6	85 ⁽²⁾
1.36	73.3	0.496	1.86	85 ⁽²⁾
1.7	81.9	0.375	2.08	85 ⁽²⁾

(1) DRB package

(2) Package limited to 85°C ambient

Table 2 uses Equation 3 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a 2.8-W audio system with 4-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.8 W.

A final point to remember about Class-AB amplifiers is how to manipulate the terms in the efficiency equation to the utmost advantage when possible. Note that in Equation 3, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

Use Equation 4 as a simple formula for calculating the maximum power dissipated, P_{Dmax} , for a differential output application.

$$P_{Dmax} = \frac{2V_{DD}^2}{\pi^2 R_L}$$

where

- P_{Dmax} for a 5-V, 4- Ω system is 1.27 W. (4)

The maximum ambient temperature depends on the heat sinking ability of the PCB system. The derating factor for the 3 mm × 3 mm DRB package is shown in the dissipation rating table. Converting this to θ_{JA} :

$$\theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.0218} = 45.9^{\circ}\text{C} / \text{W} \quad (5)$$

Given θ_{JA} , the maximum allowable junction temperature, and the maximum internal dissipation, the maximum ambient temperature can be calculated with Equation 6. The maximum recommended junction temperature for the TPA6211A1 is 150°C.

$$T_{A\text{ Max}} = T_{J\text{ Max}} - \theta_{JA} P_{Dmax} = 150 - 45.9(1.27) = 91.7^{\circ}\text{C} \quad (6)$$

Equation 6 shows that the maximum ambient temperature is 91.7°C (package limited to 85°C ambient) at maximum power dissipation with a 5-V supply.

Table 2 shows that for most applications no airflow is required to keep junction temperatures in the specified range. The TPA6211A1 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. In addition, using speakers with an impedance higher than 4- Ω dramatically increases the thermal performance by reducing the output current.

9.3.1.1 Advantages of Fully Differential Amplifiers

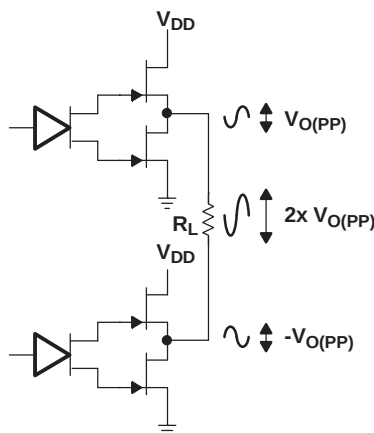
- **Input coupling capacitors not required:** A fully differential amplifier with good CMRR, like the TPA6211A1, allows the inputs to be biased at voltage other than mid-supply. For example, if a DAC has a lower mid-supply voltage than that of the TPA6211A1, the common-mode feedback circuit compensates, and the outputs are still biased at the mid-supply point of the TPA6211A1. The inputs of the TPA6211A1 can be biased from 0.5 V to $V_{DD} - 0.8$ V. If the inputs are biased outside of that range, input coupling capacitors are required.
- **Mid-supply bypass capacitor, $C_{(BYPASS)}$, not required:** The fully differential amplifier does not require a bypass capacitor. Any shift in the mid-supply voltage affects both positive and negative channels equally, thus canceling at the differential output. Removing the bypass capacitor slightly worsens power supply rejection ratio (k_{SVR}), but a slight decrease of k_{SVR} may be acceptable when an additional component can be eliminated (See Figure 17).
- **Better RF-immunity:** GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217 Hz. The transmitted signal is picked-up on input and output traces. The fully differential amplifier cancels the signal much better than the typical audio amplifier.
- Figure 31 through Figure 38 show application schematics for differential and single-ended inputs.

9.3.1.2 Differential Output Versus Single-Ended Output

Figure 29 shows a Class-AB audio power amplifier (APA) in a fully differential configuration. The TPA6211A1 amplifier has differential outputs driving both ends of the load. One of several potential benefits to this configuration is power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground-referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance Equation 7.

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

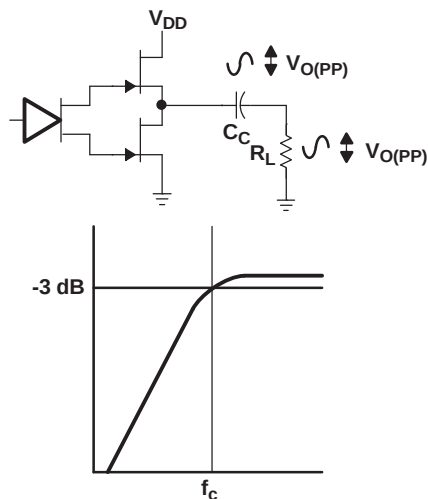
$$\text{Power} = \frac{V_{(rms)}^2}{R_L} \quad (7)$$


Figure 29. Differential Output Configuration

In a typical wireless handset operating at 3.6 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 200 mW to 800 mW. This is a 6-dB improvement in sound power—loudness that can be heard. In addition to increased power, there are frequency-response concerns. Consider the single-supply SE configuration shown in [Figure 30](#). A coupling capacitor (C_C) is required to block the dc-offset voltage from the load. This capacitor can be quite large (approximately 33 μF to 1000 μF) so it tends to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance. This frequency-limiting effect is due to the high-pass filter network created with the speaker impedance and the coupling capacitance. This is calculated with [Equation 8](#).

$$f_c = \frac{1}{2\pi R_L C_C} \quad (8)$$

For example, a 68-μF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.


Figure 30. Single-Ended Output and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration.

9.4 Device Functional Modes

9.4.1 Shutdown Mode

The TPA6211A1 device can be put in shutdown mode when asserting SHUTDOWN pin to a logic LOW. While in shutdown mode, the device output stage is turned off and set into high impedance, making the current consumption very low. The device exits shutdown mode when a HIGH logic level is applied to SHUTDOWN pin.

10 Application and Implementation

NOTE

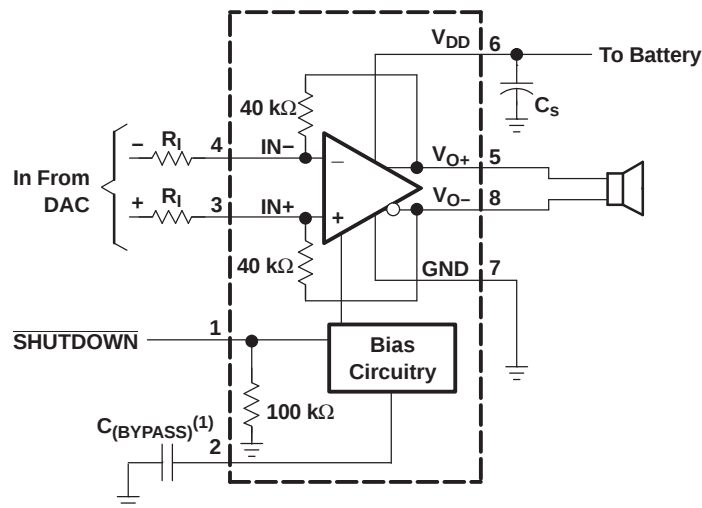
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPA6211A1 is a fully-differential amplifier designed to drive a speaker with at least 3- Ω impedance while consuming only 20 mm² total printed circuit board (PCB) area in most applications.

10.2 Typical Application

Figure 31 shows a typical application circuit for the TPA6211A1 with a speaker, input resistors and supporting power supply decoupling capacitors.



(1) C_(BYPASS) is optional

Figure 31. Typical Differential Input Application Schematic

Typical values are shown in Table 3.

Table 3. Typical Component Values

COMPONENT	VALUE
R _I	40 k Ω
C _(BYPASS) ⁽¹⁾	0.22 μ F
C _S	1 μ F
C _I	0.22 μ F

(1) C_(BYPASS) is optional.

10.2.1 Design Requirements

For this design example, use the parameters listed in [Table 4](#).

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Power supply	2.5 V to 5.5 V
Current	4 mA to 5 mA
Shutdown	High > 1.55 V
	Low < 0.5 V
Speaker	3 Ω, 4 Ω, or 8 Ω

10.2.2 Detailed Design Procedure

10.2.2.1 Selecting Components

10.2.2.1.1 Resistors (R_I)

The input resistor (R_I) can be selected to set the gain of the amplifier according to [Equation 9](#).

$$\text{Gain} = \frac{R_F}{R_I} \quad (9)$$

The internal feedback resistors (R_F) are trimmed to 40 kΩ.

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and the cancellation of the second harmonic distortion diminishes if resistor mismatch occurs. Therefore, 1%-tolerance resistors or better are recommended to optimize performance.

10.2.2.1.2 Bypass Capacitor (C_{BYPASS}) and Start-Up Time

The internal voltage divider at the BYPASS pin of this device sets a mid-supply voltage for internal references and sets the output common mode voltage to $V_{\text{DD}}/2$. Adding a capacitor filters any noise into this pin, increasing k_{SVR} . C_{BYPASS} also determines the rise time of $V_{\text{O+}}$ and $V_{\text{O-}}$ when the device exits shutdown. The larger the capacitor, the slower the rise time.

10.2.2.1.3 Input Capacitor (C_I)

The TPA6211A1 does not require input coupling capacitors when driven by a differential input source biased from 0.5 V to $V_{\text{DD}} - 0.8$ V. Use 1% tolerance or better gain-setting resistors if not using input coupling capacitors.

In the single-ended input application, an input capacitor, C_I , is required to allow the amplifier to bias the input signal to the proper dc level. In this case, C_I and R_I form a high-pass filter with the corner frequency defined in [Equation 10](#).

$$f_c = \frac{1}{2\pi R_I C_I} \quad (10)$$

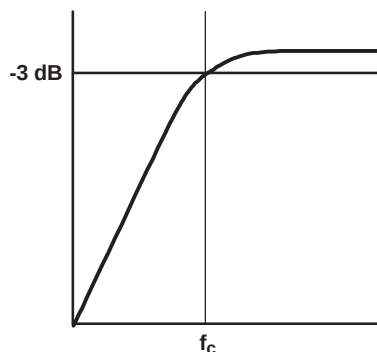


Figure 32. Input Filter Cutoff Frequency

The value of C_1 is an important consideration. It directly affects the bass (low frequency) performance of the circuit. Consider the example where R_1 is 10 k Ω and the specification calls for a flat bass response down to 100 Hz. Equation 10 is reconfigured as Equation 11.

$$C_1 = \frac{1}{2\pi R_1 f_c} \quad (11)$$

In this example, C_1 is 0.16 μ F, so the likely choice ranges from 0.22 μ F to 0.47 μ F. Ceramic capacitors are preferred because they are the best choice in preventing leakage current. When polarized capacitors are used, the positive side of the capacitor faces the amplifier input in most applications. The input dc level is held at $V_{DD}/2$, typically higher than the source dc level. It is important to confirm the capacitor polarity in the application.

10.2.2.1.4 Band-Pass Filter (R_a , C_a , and C_b)

It may be desirable to have signal filtering beyond the one-pole high-pass filter formed by the combination of C_1 and R_1 . A low-pass filter may be added by placing a capacitor (C_F) between the inputs and outputs, forming a band-pass filter.

An example of when this technique might be used would be in an application where the desirable pass-band range is between 100 Hz and 10 kHz, with a gain of 4 V/V. The following equations illustrate how the proper values of C_F and C_1 can be determined.

10.2.2.1.4.1 Step 1: Low-Pass Filter

$$f_{c(LPF)} = \frac{1}{2\pi R_F C_F}$$

where

- R_F is the internal 40 k Ω resistor

$$f_{c(LPF)} = \frac{1}{2\pi 40\text{k}\Omega C_F} \quad (13)$$

Therefore,

$$C_F = \frac{1}{2\pi 40\text{k}\Omega f_{c(LPF)}} \quad (14)$$

Substitute $f_{c(LPF)}$ with 10 kHz and solve for C_F : $C_F = 398$ pF

10.2.2.1.4.2 Step 2: High-Pass Filter

$$f_{c(HPF)} = \frac{1}{2\pi R_1 C_1}$$

where

- R_1 is the input resistor

Because the application in this case requires a gain of 4 V/V, R_1 must be set to 10 k Ω .

Substitute R_1 in Equation 15 with 10 k Ω as shown in Equation 16.

$$f_{c(HPF)} = \frac{1}{2\pi 10\text{k}\Omega C_1} \quad (16)$$

Therefore,

$$C_1 = \frac{1}{2\pi 10\text{k}\Omega f_{c(HPF)}} \quad (17)$$

Substitute $f_{c(HPF)}$ with 100 Hz and solve for C_1 : $C_1 = 0.16$ μ F

At this point, a first-order band-pass filter has been created with the low-frequency cutoff set to 100 Hz and the high-frequency cutoff set to 10 kHz.

The process can be taken a step further by creating a second-order high-pass filter. This is accomplished by placing a resistor (R_a) and capacitor (C_a) in the input path. It is important to note that R_a must be at least 10 times smaller than R_i ; otherwise its value has a noticeable effect on the gain, as R_a and R_i are in series.

10.2.2.1.4.3 Step 3: Additional Low-Pass Filter

R_a must be at least 10x smaller than R_i , Set $R_a = 1\text{ k}\Omega$,

$$f_{c(\text{LPF})} = \frac{1}{2\pi R_a C_a} \quad (18)$$

Therefore,

$$C_a = \frac{1}{2\pi \cdot 1\text{ k}\Omega \cdot f_{c(\text{LPF})}} \quad (19)$$

Substitute $f_{c(\text{LPF})}$ with 10 kHz and solving for C_a : $C_a = 160\text{ pF}$

Figure 33 is a bode plot for the band-pass filter in the previous example. Figure 38 shows how to configure the TPA6211A1 as a band-pass filter.

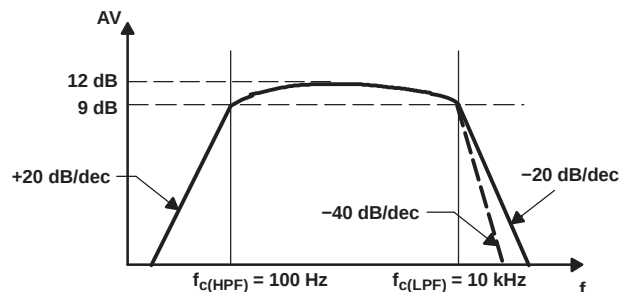


Figure 33. Bode Plot

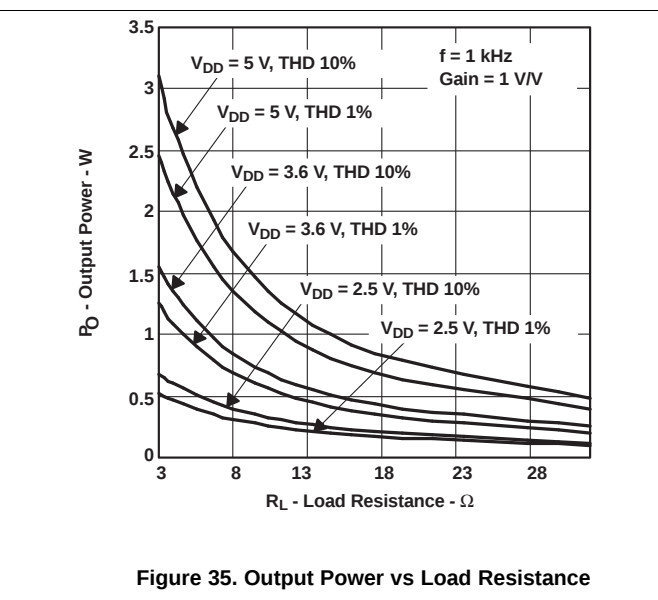
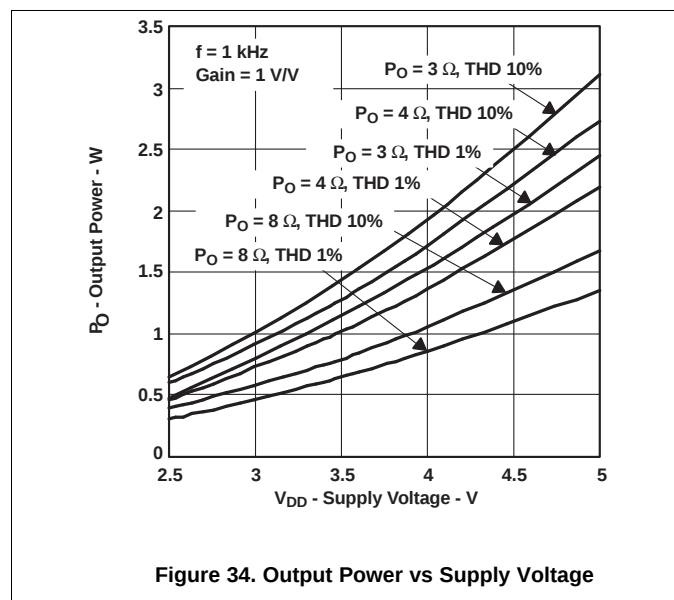
10.2.2.1.5 Decoupling Capacitor (C_S)

The TPA6211A1 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power-supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF to 1 μF , placed as close as possible to the device V_{DD} lead works best. For filtering lower frequency noise signals, a 10- μF or greater capacitor placed near the audio power amplifier also helps, but is not required in most applications because of the high PSRR of this device.

10.2.2.1.6 Using Low-ESR Capacitors

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

10.2.3 Application Curves



10.3 System Examples

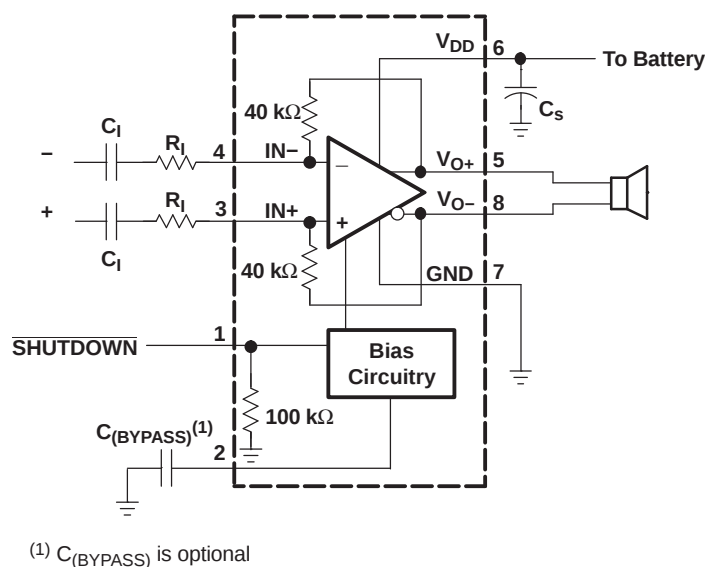
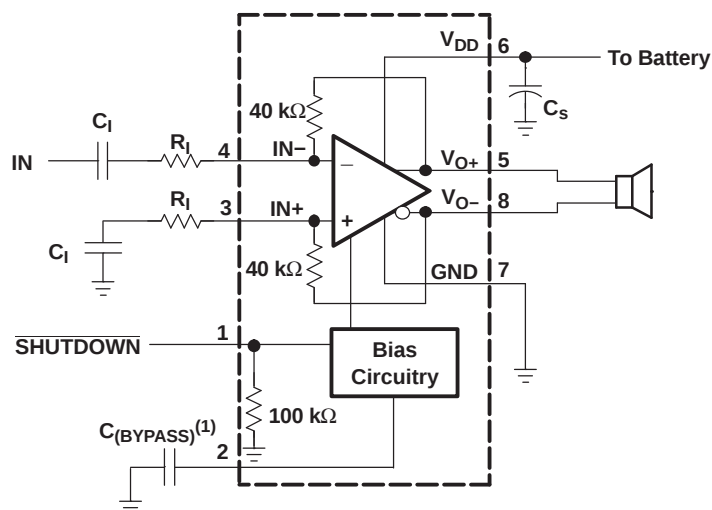


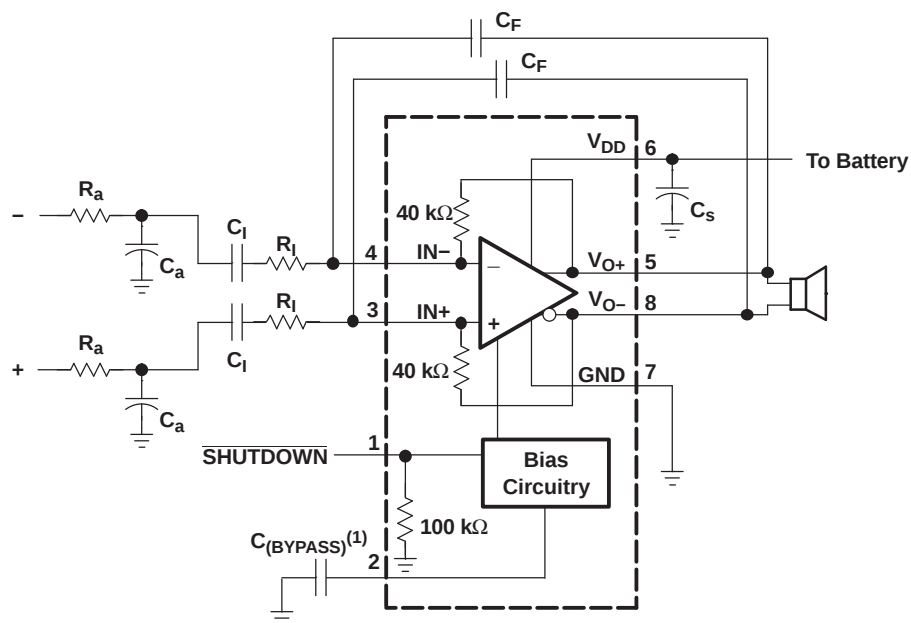
Figure 36. Differential Input Application Schematic Optimized With Input Capacitors

System Examples (continued)



(1) $C_{(BYPASS)}$ is optional

Figure 37. Single-Ended Input Application Schematic



(1) $C_{(BYPASS)}$ is optional

Figure 38. Differential Input Application Schematic With Input Bandpass Filter

11 Power Supply Recommendations

The TPA6211A1 device is designed to operate from an input voltage supply range between 2.5 V and 5.5 V. Therefore, the output voltage range of power supply must be within this range and well regulated. The current capability of upper power should not exceed the maximum current limit of the power switch.

11.1 Power Supply Decoupling Capacitor

The TPA6211A1 device requires adequate power supply decoupling to ensure a high efficiency operation with low total harmonic distortion (THD).

Place a low equivalent series resistance (ESR) ceramic capacitor, typically 0.1 μF , as close as possible of the VDD pin. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. Also is recommended to place a 2.2- μF to 10- μF capacitor on the VDD supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any droop in the supply voltage.

12 Layout

12.1 Layout Guidelines

Place all the external components close to the TPA6211A1 device. The input resistors need to be close to the device input pins so noise does not couple on the high impedance nodes between the input resistors and the input amplifier of the device. Placing the decoupling capacitors, C_S and C_{BYPASS} , close to the TPA6211A1 device is important for the efficiency of the amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

12.2 Layout Examples

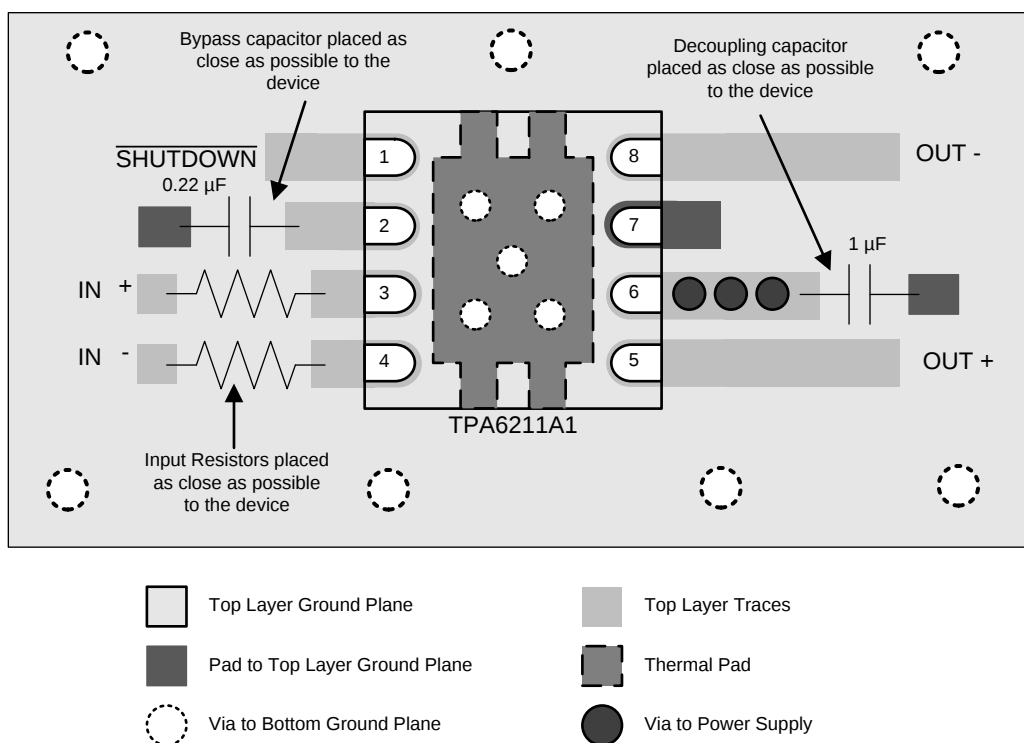


Figure 39. TPA6211A1 8-Pin SON (DRB) Board Layout

Layout Examples (continued)

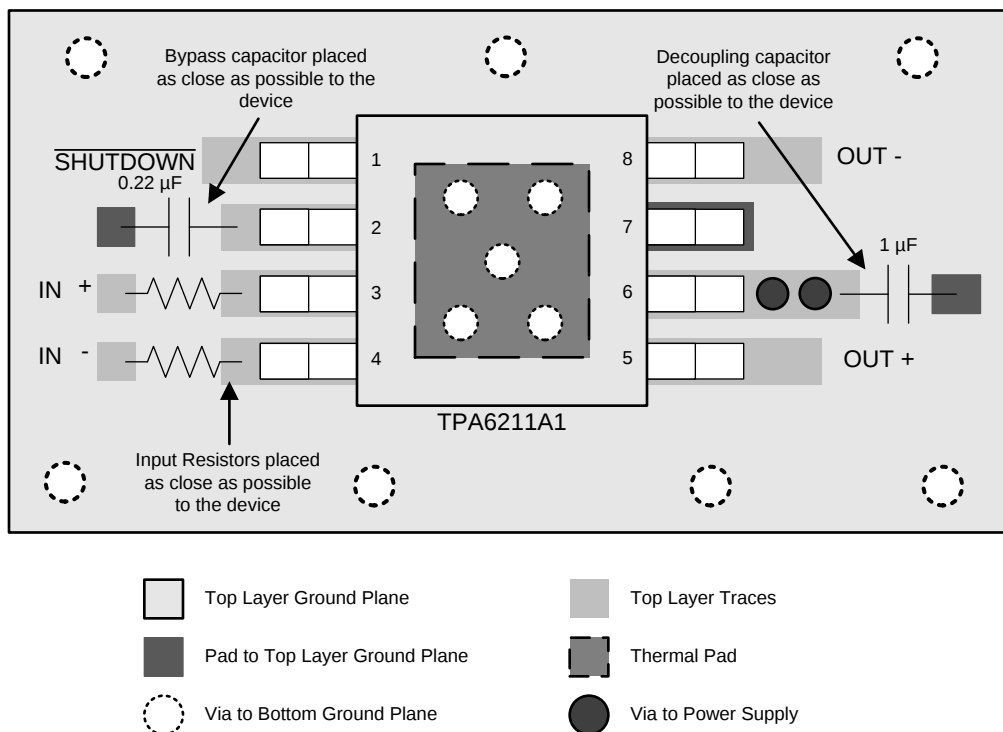


Figure 40. TPA6211A1 8-Pin MSOP-PowerPAD™ (DGN) Board Layout

13 Device and Documentation Support

13.1 Device Support

13.1.1 Development Support

For the TPA6211A1 TINA-TI Spice Model, see [SBOM819](#).

For the TPA6211A1 TINA-TI Reference Design, see [SBOM820](#).

For the TPA6211A1EVM Gerber files, see [SLOC009](#).

For the *Speaker Amplifier Class AB/Class D* Parametric Table, go to www.ti.com/lscs/ti/audio-ic/speaker-amplifier-class-ab-class-d-product.page

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation, see the following:

TPA6211A1EVM User's Guide, *TPA6211A1 Audio Power Amplifier Evaluation Module*, [SLOU162](#)

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HPA00169DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AYK	Samples
TPA6211A1DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AYK	Samples
TPA6211A1DGNG4	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AYK	Samples
TPA6211A1DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AYK	Samples
TPA6211A1DGNRG4	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AYK	Samples
TPA6211A1DRB	ACTIVE	SON	DRB	8	121	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AYN	Samples
TPA6211A1DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AYN	Samples
TPA6211A1DRBRG4	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AYN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPA6211A1 :

- Automotive: [TPA6211A1-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

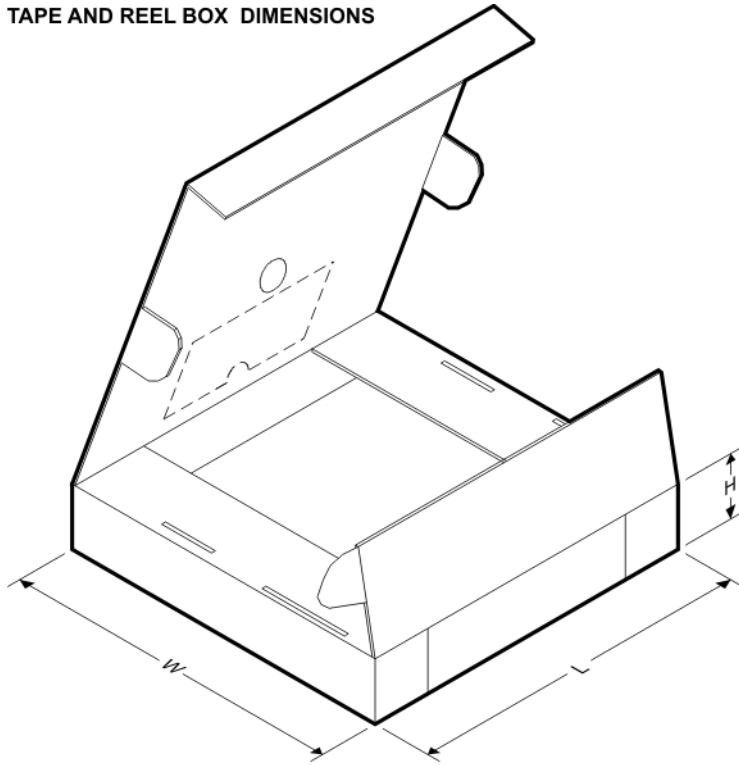
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6211A1DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPA6211A1DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPA6211A1DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPA6211A1DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

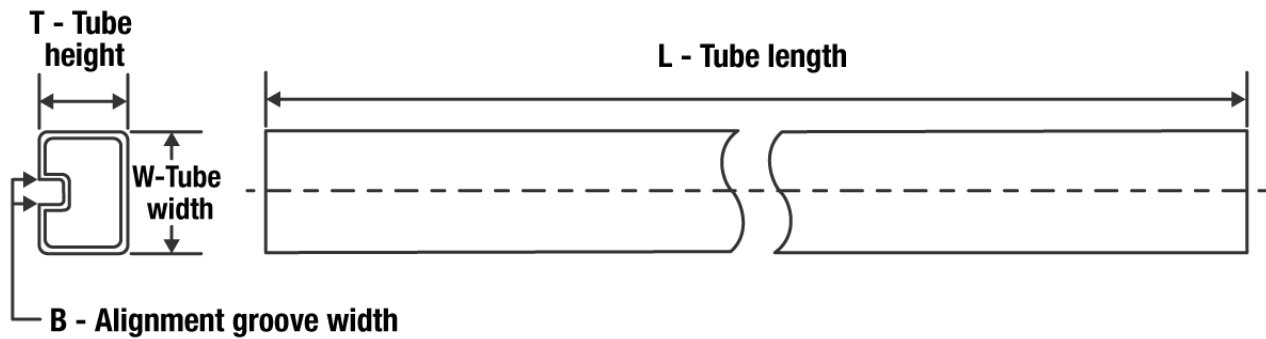
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6211A1DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
TPA6211A1DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPA6211A1DRBR	SON	DRB	8	3000	853.0	449.0	35.0
TPA6211A1DRBR	SON	DRB	8	3000	367.0	367.0	35.0

TUBE



*All dimensions are nominal

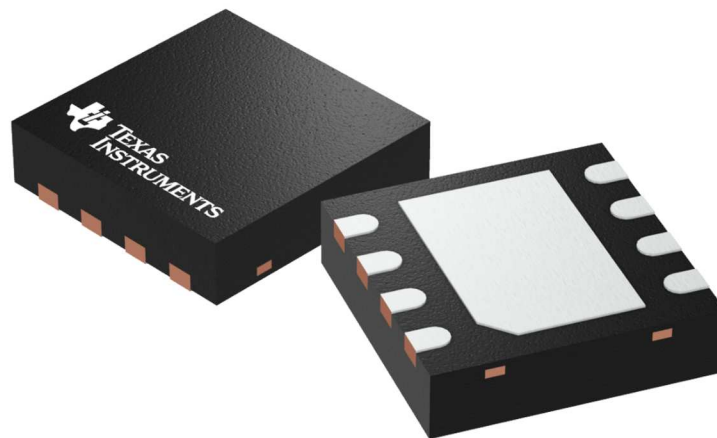
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPA6211A1DGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPA6211A1DGNG4	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPA6211A1DRB	DRB	VSON	8	121	381	4.82	2286	NA
TPA6211A1DRB	DRB	VSON	8	121	381	4.82	2286	NA
TPA6211A1DRB	DRB	VSON	8	121	381	4.83	2286	0

DRB 8

GENERIC PACKAGE VIEW

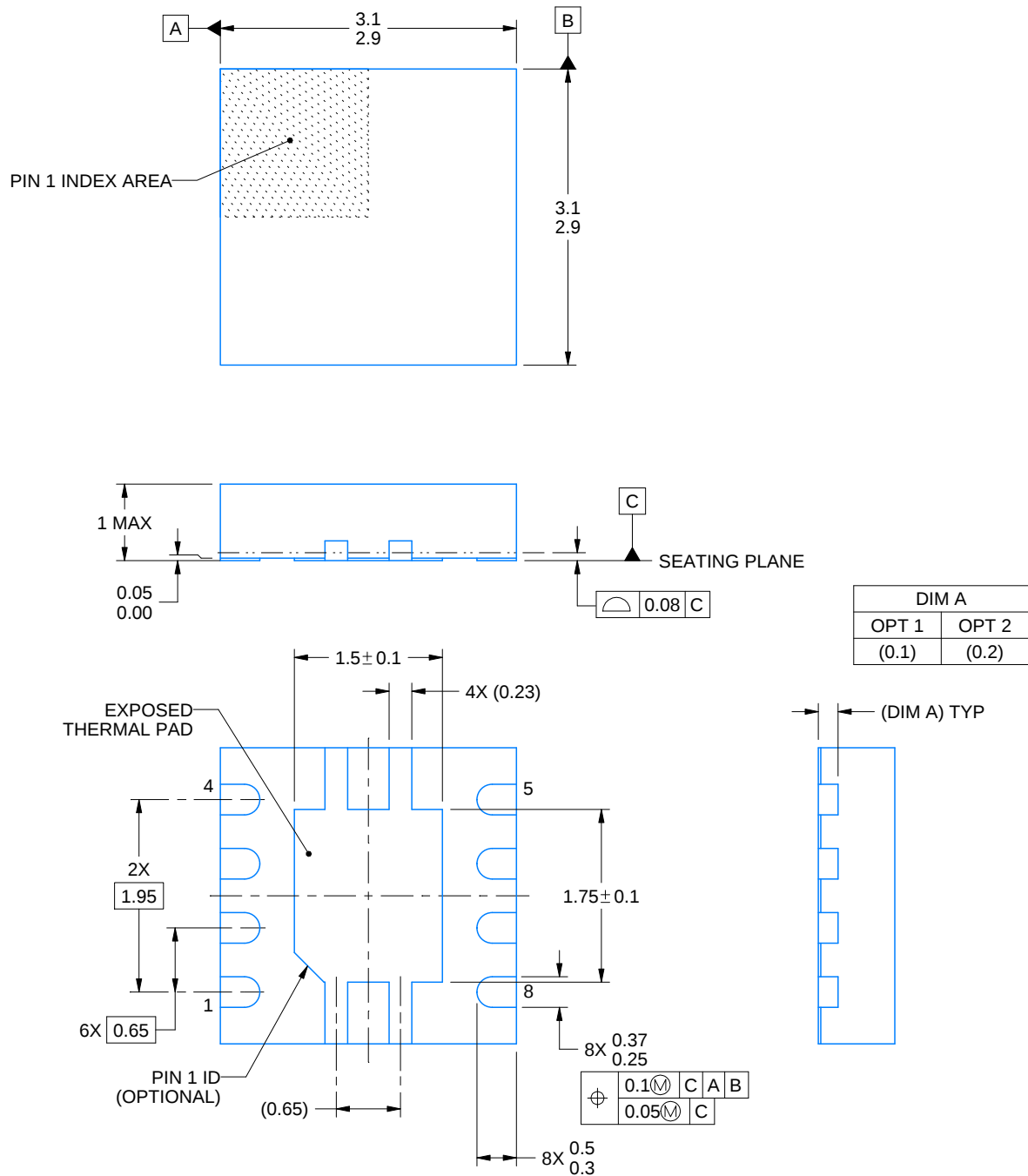
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L



4218875/A 01/2018

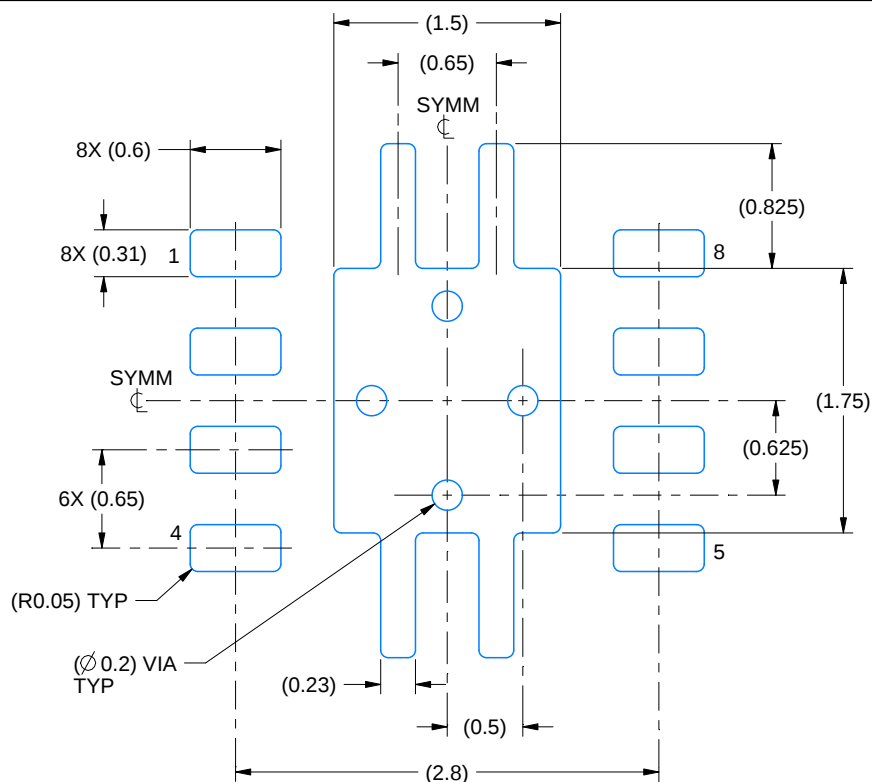
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

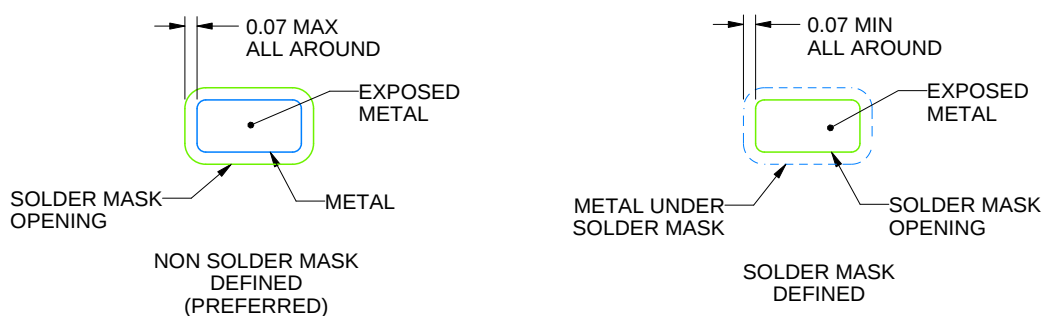
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

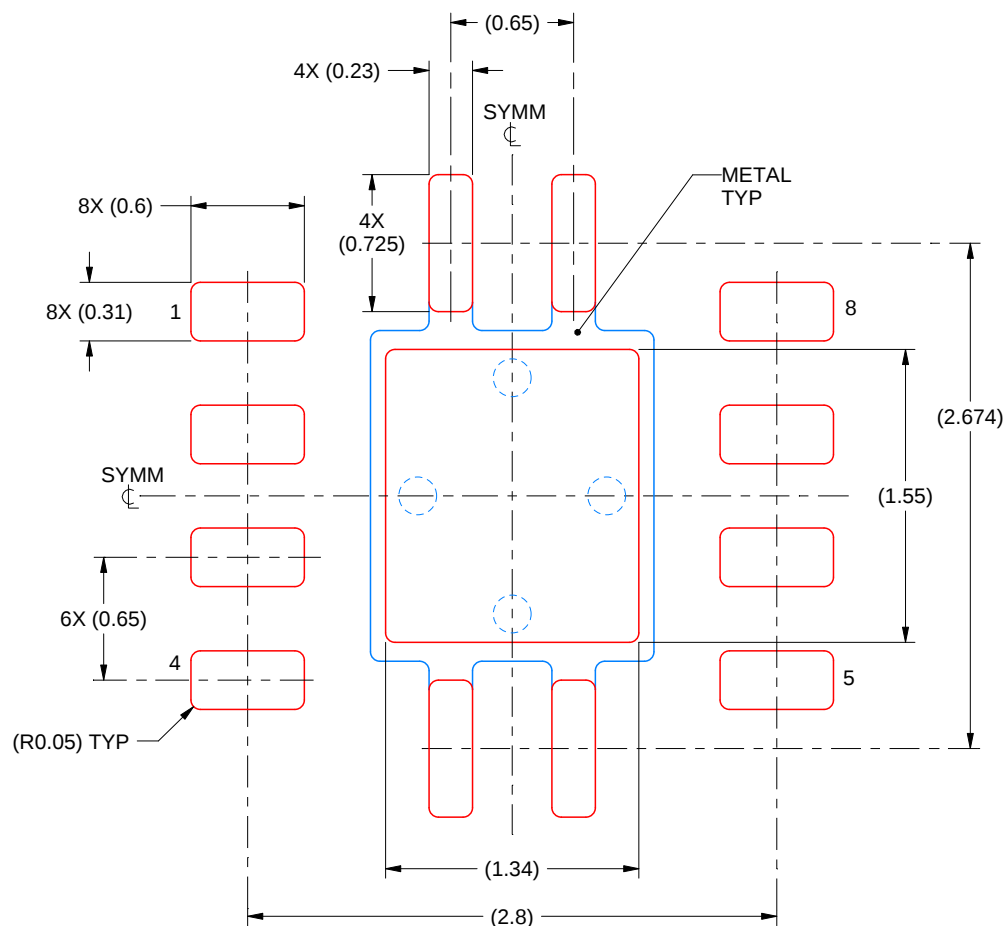
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

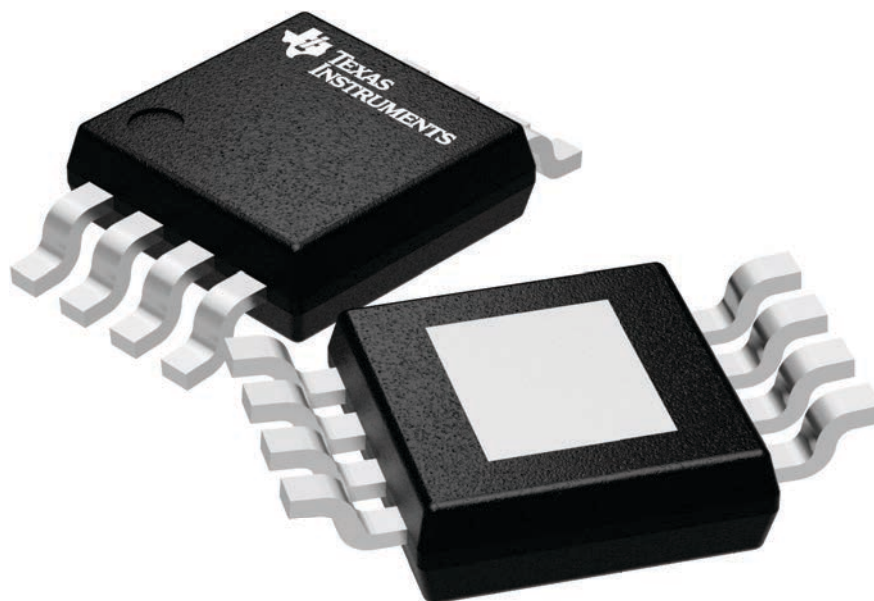
DGN 8

PowerPAD VSSOP - 1.1 mm max height

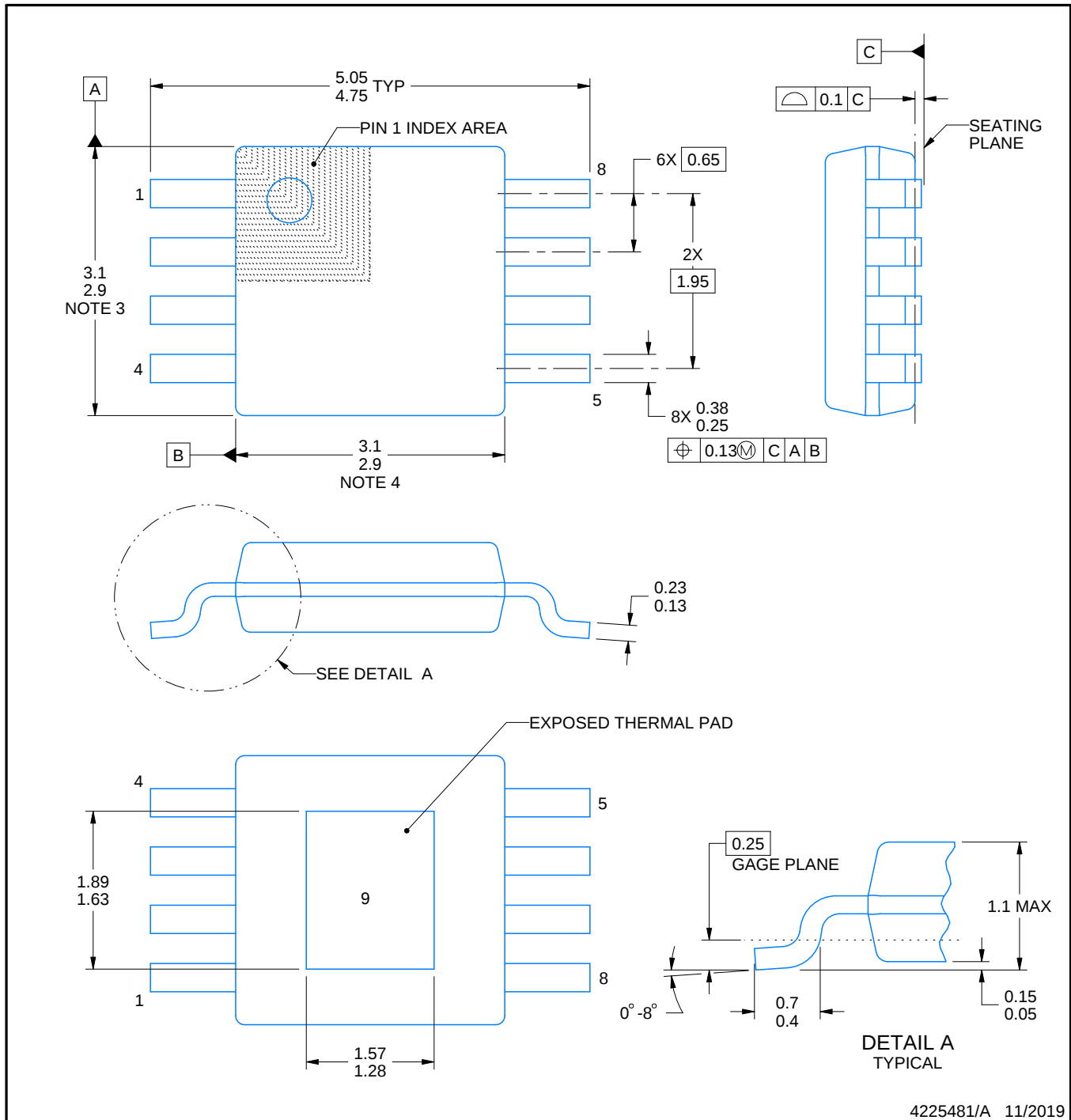
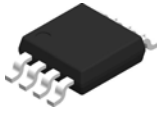
3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A



4225481/A 11/2019

NOTES:

PowerPAD is a trademark of Texas Instruments.

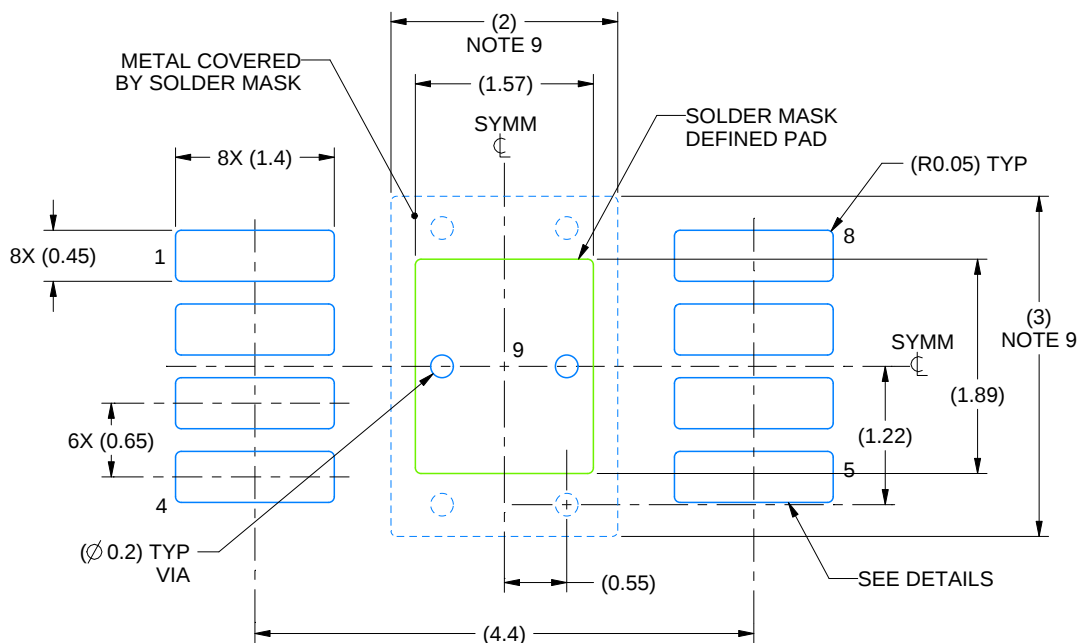
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

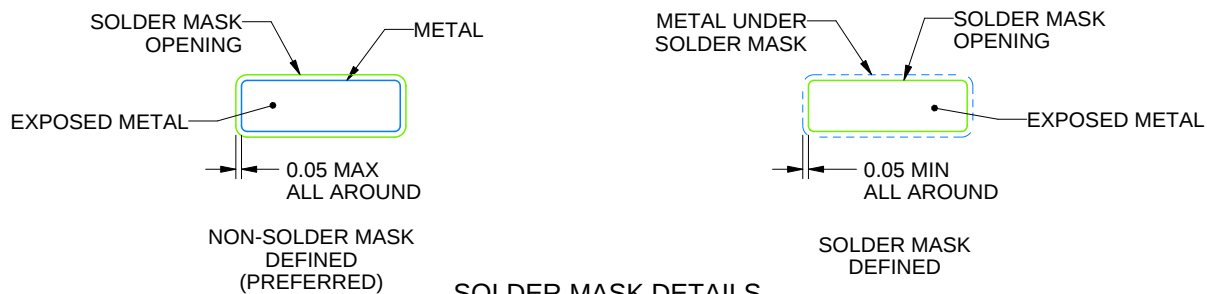
DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

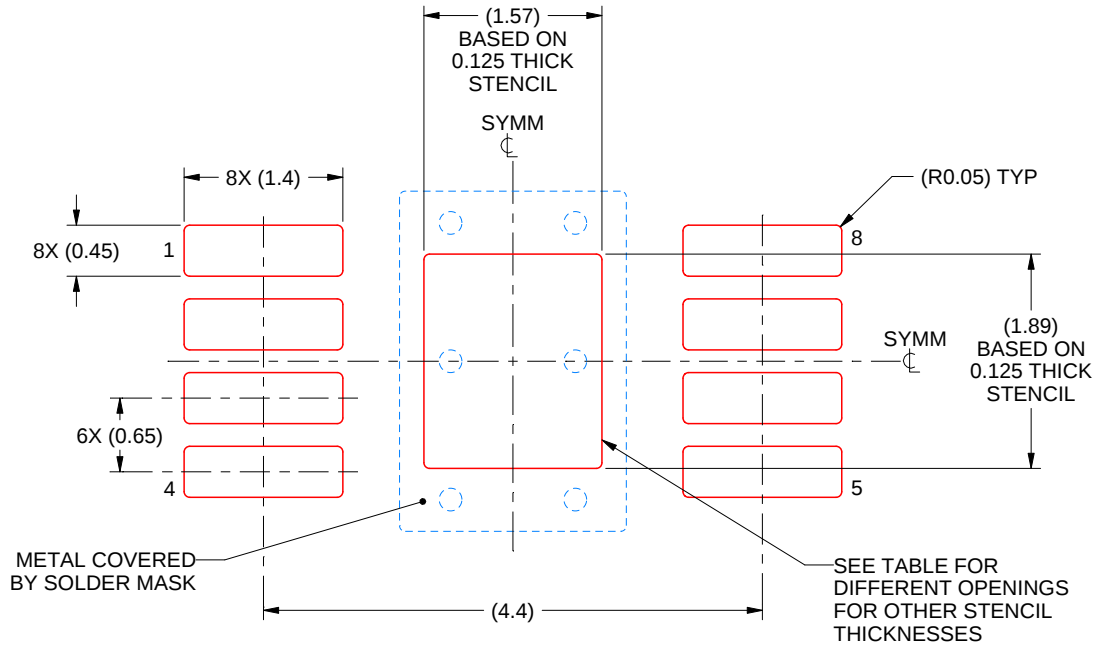
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



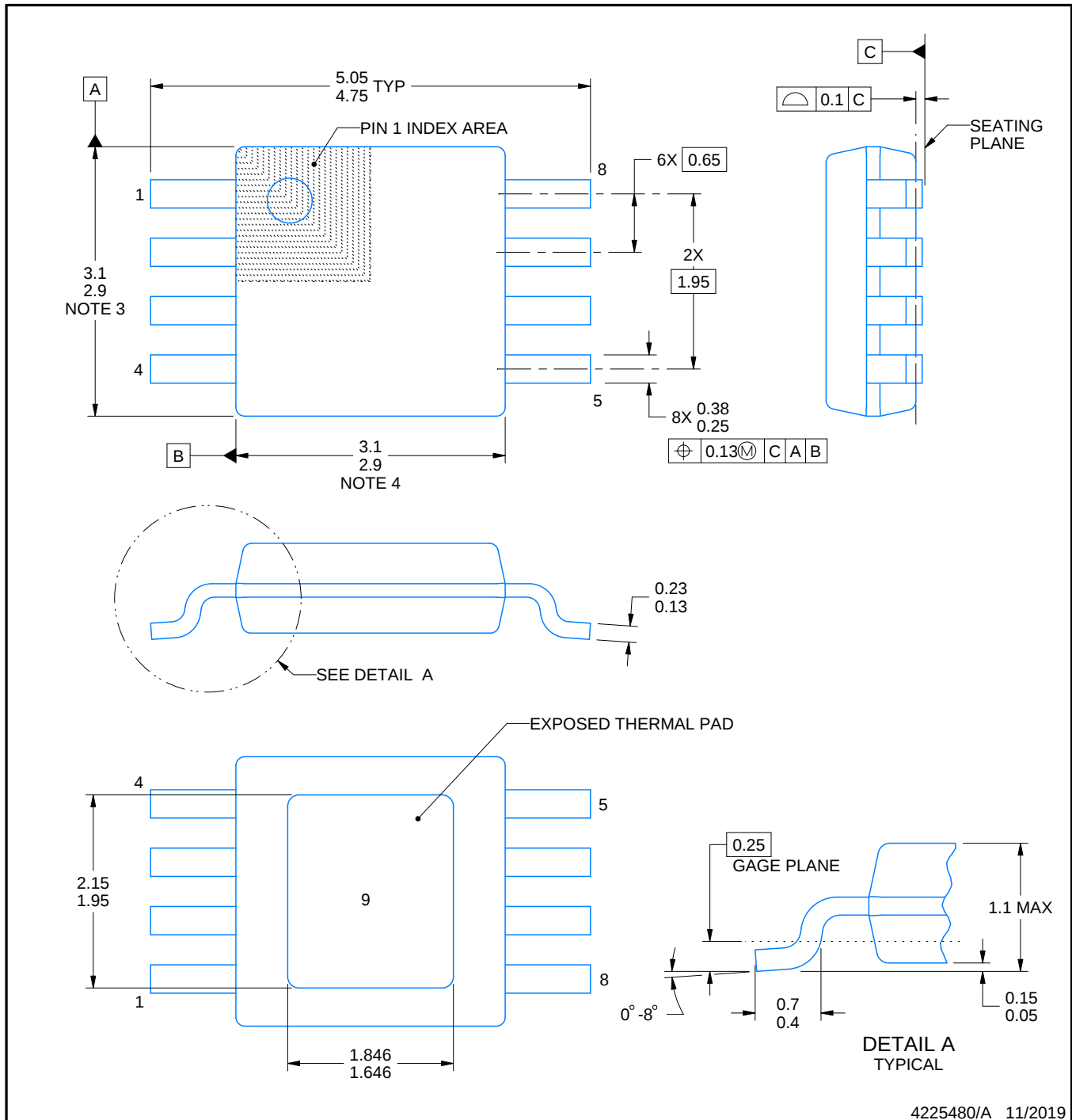
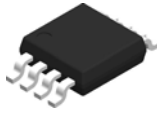
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.



NOTES:

PowerPAD is a trademark of Texas Instruments.

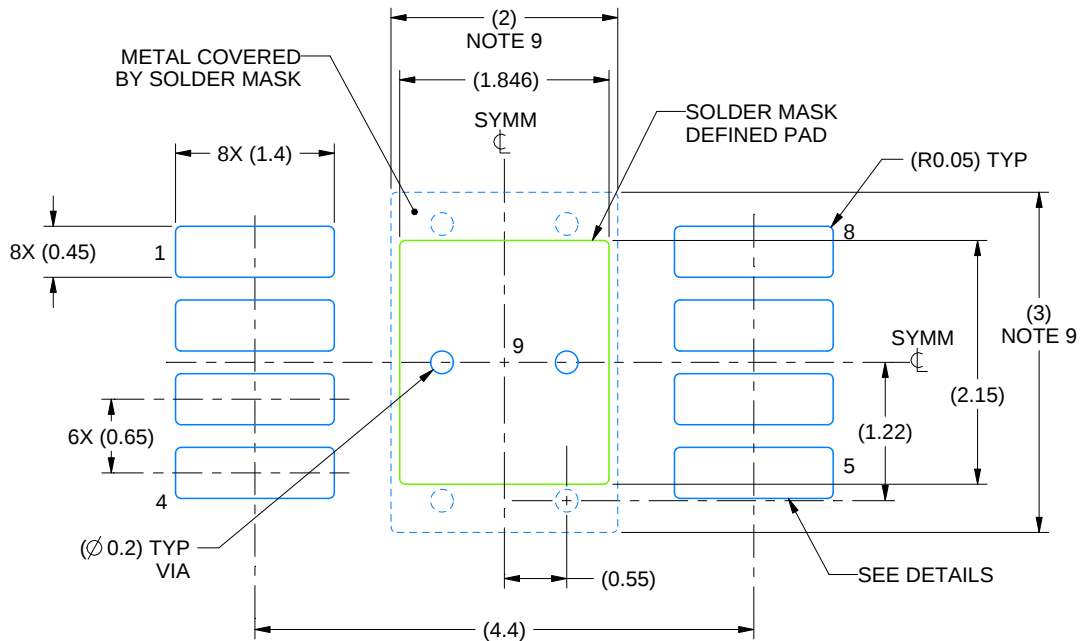
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

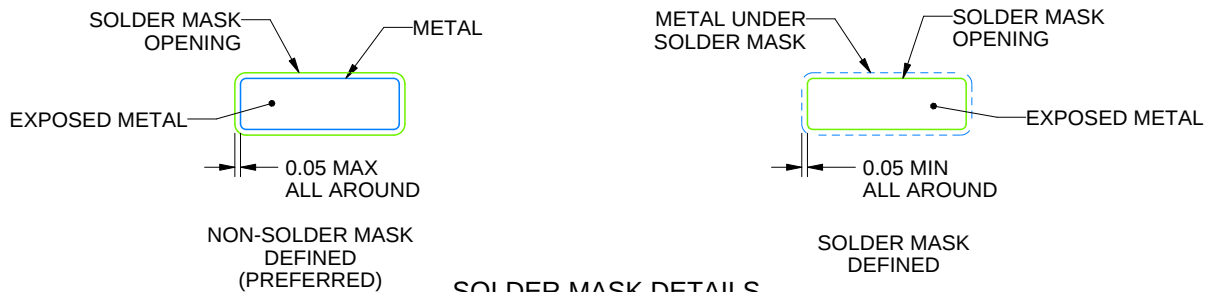
DGN0008G

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4225480/A 11/2019

NOTES: (continued)

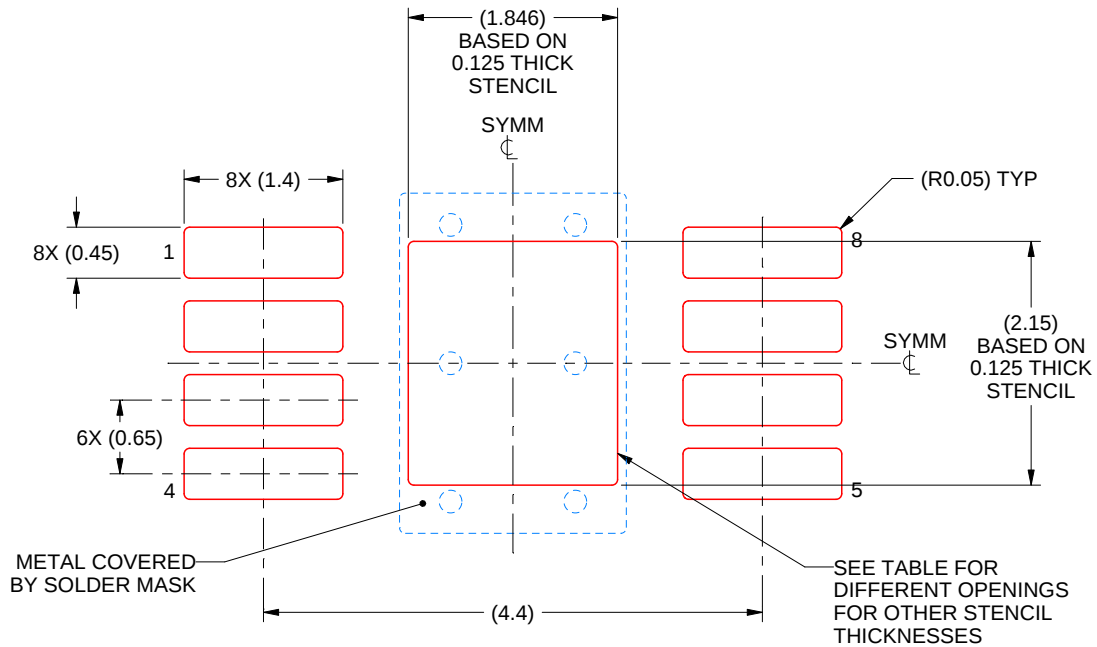
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008G

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.06 X 2.40
0.125	1.846 X 2.15 (SHOWN)
0.15	1.69 X 1.96
0.175	1.56 X 1.82

4225480/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated