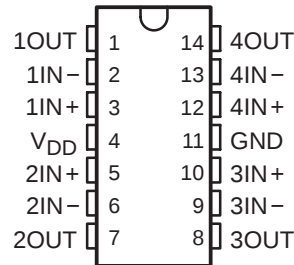


TLC274, TLC274A, TLC274B, TLC274Y, TLC279 LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

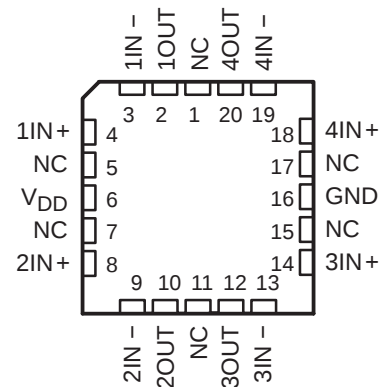
SLOS092D – SEPTEMBER 1987 – REVISED MARCH 2001

- **Trimmed Offset Voltage:**
TLC279 . . . 900 μV Max at 25°C,
 $V_{\text{DD}} = 5\text{ V}$
- **Input Offset Voltage Drift . . . Typically**
0.1 $\mu\text{V}/\text{Month}$, Including the First 30 Days
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
0°C to 70°C . . . 3 V to 16 V
–40°C to 85°C . . . 4 V to 16 V
–55°C to 125°C . . . 4 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix and I-Suffix Versions)**
- **Low Noise . . . Typically 25 nV/ $\sqrt{\text{Hz}}$ at $f = 1\text{ kHz}$**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . $10^{12}\ \Omega$ Typ**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up Immunity**

D, J, N, OR PW PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

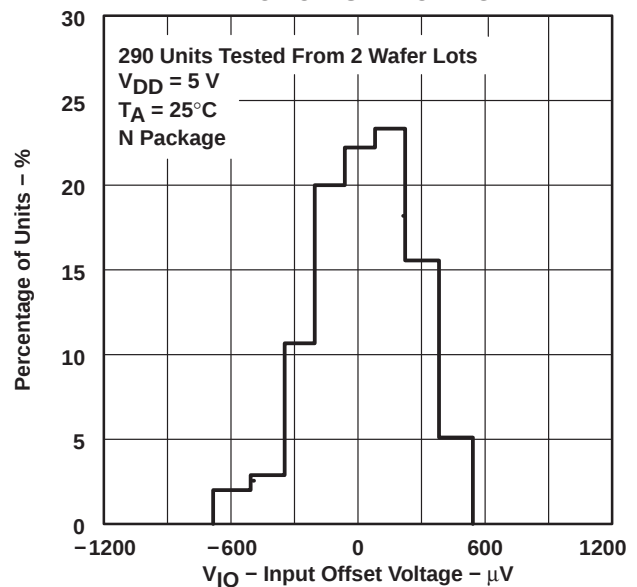
description

The TLC274 and TLC279 quad operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching that of general-purpose BiFET devices.

These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications which have previously been reserved for BiFET and NFET products. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC274 (10 mV) to the high-precision TLC279 (900 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

DISTRIBUTION OF TLC279
INPUT OFFSET VOLTAGE



LinCMOS is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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TLC274, TLC274A, TLC274B, TLC274Y, TLC279 LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

SLOS092D – SEPTEMBER 1987 – REVISED MARCH 2001

description (continued)

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC274 and TLC279. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip-carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up.

The TLC274 and TLC279 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

AVAILABLE OPTIONS

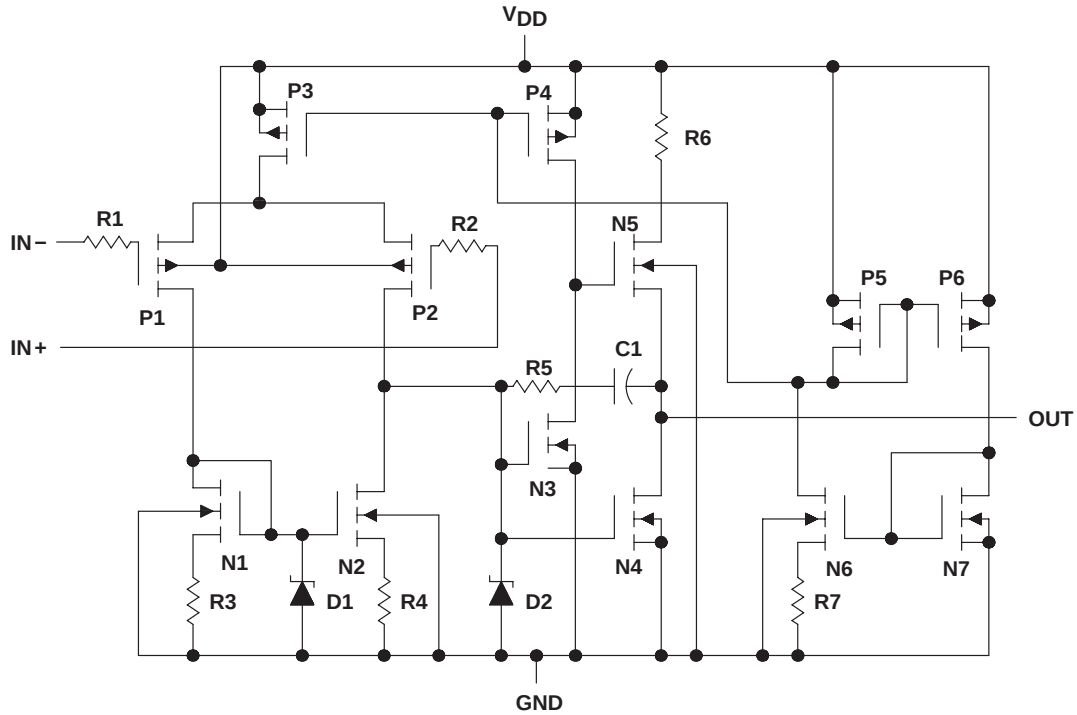
T _A	V _{IO} max AT 25°C	PACKAGED DEVICES					CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP (PW)	
0°C to 70°C	900 µV	TLC279CD	—	—	TLC279CN	—	—
	2 mV	TLC274BCD	—	—	TLC274BCN	—	—
	5 mV	TLC274ACD	—	—	TLC274ACN	—	—
	10 mV	TLC274CD	—	—	TLC274CN	TLC274CPW	TLC274Y
–40°C to 85°C	900 µV	TLC279ID	—	—	TLC279IN	—	—
	2 mV	TLC274BID	—	—	TLC274BIN	—	—
	5 mV	TLC274AID	—	—	TLC274AIN	—	—
	10 mV	TLC274ID	—	—	TLC274IN	—	—
–55°C to 125°C	900 µV	TLC279MD	TLC279MFK	TLC279MJ	TLC279MN	—	—
	10 mV	TLC274MD	TLC274MFK	TLC274MJ	TLC274MN	—	—

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC279CDR).



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equivalent schematic (each amplifier)

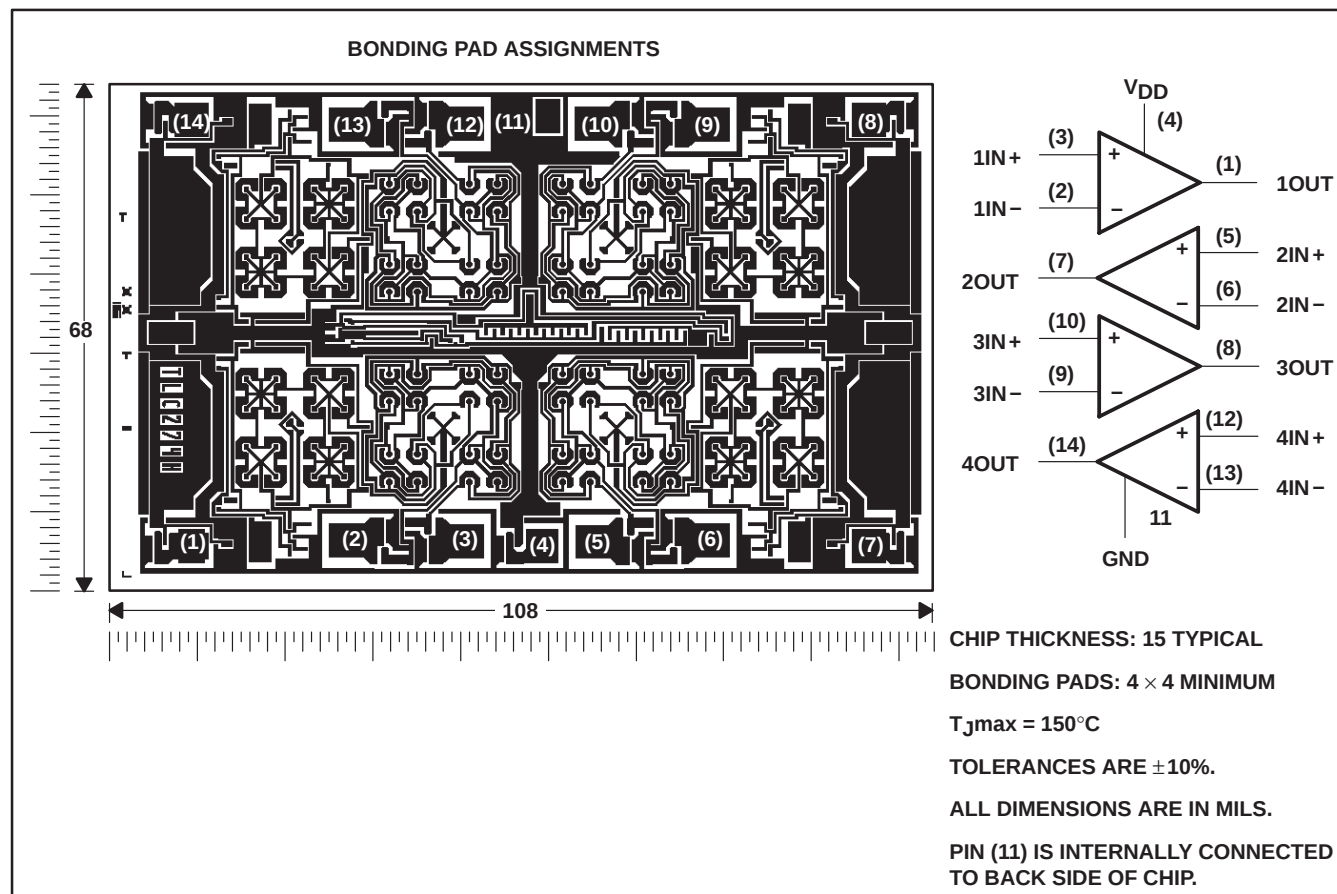


TLC274, TLC274A, TLC274B, TLC274Y, TLC279 LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

SLOS092D – SEPTEMBER 1987 – REVISED MARCH 2001

TLC274Y chip information

These chips, when properly assembled, display characteristics similar to the TLC274C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



TLC274, TLC274A, TLC274B, TLC274Y, TLC279 LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

SLOS092D – SEPTEMBER 1987 – REVISED MARCH 2001

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage, V_{ID} (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input)	-0.3 V to V_{DD}
Input current, I_I	± 5 mA
Output current, I_O (each output)	± 30 mA
Total current into V_{DD}	45 mA
Total current out of GND	45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A : C suffix	0°C to 70°C
I suffix	-40°C to 85°C
M suffix	-55°C to 125°C
Storage temperature range	-65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or PW package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	—
PW	700 mW	5.6 mW/°C	448 mW	—	—

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}		3	16	4	16	4	16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	-0.2	3.5	-0.2	3.5	0	3.5	V
	$V_{DD} = 10$ V	-0.2	8.5	-0.2	8.5	0	8.5	
Operating free-air temperature, T_A		0	70	-40	85	-55	125	°C



TLC274, TLC274A, TLC274B, TLC274Y, TLC279 LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

SLOS092D – SEPTEMBER 1987 – REVISED MARCH 2001

electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A^\dagger$	TLC274C, TLC274AC, TLC274BC, TLC279C			UNIT
					MIN	TYP	MAX	
V_{IO} Input offset voltage	TLC274C	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$,	$V_{IC} = 0$, $R_L = 10\text{ k}\Omega$	25°C		1.1	10	mV
				Full range			12	
	TLC274AC	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$,	$V_{IC} = 0$, $R_L = 10\text{ k}\Omega$	25°C		0.9	5	
				Full range			6.5	
	TLC274BC	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$,	$V_{IC} = 0$, $R_L = 10\text{ k}\Omega$	25°C		340	2000	μV
				Full range			3000	
	TLC279C	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$,	$V_{IC} = 0$, $R_L = 10\text{ k}\Omega$	25°C		320	900	
				Full range			1500	
α_{VIO} Average temperature coefficient of input offset voltage				25°C to 70°C		1.8		$\mu\text{V}/^\circ\text{C}$
I_{IO} Input offset current (see Note 4)		$V_O = 2.5\text{ V}$,	$V_{IC} = 2.5\text{ V}$	25°C		0.1	60	pA
				70°C		7	300	
I_{IB} Input bias current (see Note 4)				25°C		0.6	60	pA
				70°C		40	600	
V_{ICR} Common-mode input voltage range (see Note 5)				25°C	-0.2 to 4	-0.3 to 4.2		V
				Full range	-0.2 to 3.5			V
V_{OH} High-level output voltage		$V_{ID} = 100\text{ mV}$,	$R_L = 10\text{ k}\Omega$	25°C		3.2	3.8	V
				0°C		3	3.8	
				70°C		3	3.8	
V_{OL} Low-level output voltage		$V_{ID} = -100\text{ mV}$,	$I_{OL} = 0$	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD} Large-signal differential voltage amplification		$V_O = 0.25\text{ V to } 2\text{ V}$,	$R_L = 10\text{ k}\Omega$	25°C		5	23	V/mV
				0°C		4	27	
				70°C		4	20	
CMRR Common-mode rejection ratio		$V_{IC} = V_{ICRmin}$		25°C		65	80	dB
				0°C		60	84	
				70°C		60	85	
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		$V_{DD} = 5\text{ V to } 10\text{ V}$,	$V_O = 1.4\text{ V}$	25°C		65	95	dB
				0°C		60	94	
				70°C		60	96	
I_{DD} Supply current (four amplifiers)		$V_O = 2.5\text{ V}$, No load	$V_{IC} = 2.5\text{ V}$	25°C		2.7	6.4	mA
				0°C		3.1	7.2	
				70°C		2.3	5.2	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



TLC274, TLC274A, TLC274B, TLC274Y, TLC279 LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

SLOS092D – SEPTEMBER 1987 – REVISED MARCH 2001

electrical characteristics at specified free-air temperature, $V_{DD} = 10\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A †	TLC274C, TLC274AC, TLC274BC, TLC279C			UNIT
				MIN	TYP	MAX	
V_{IO} Input offset voltage	TLC274C	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 0$, $R_L = 10\text{ k}\Omega$	25°C		1.1	10	mV
			Full range			12	
	TLC274AC	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 0$, $R_L = 10\text{ k}\Omega$	25°C		0.9	5	
			Full range			6.5	
	TLC274BC	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 0$, $R_L = 10\text{ k}\Omega$	25°C		390	2000	μV
			Full range			3000	
	TLC279C	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 0$, $R_L = 10\text{ k}\Omega$	25°C		370	1200	
			Full range			1900	
α_{VIO} Average temperature coefficient of input offset voltage			25°C to 70°C		2		$\mu\text{V}/^\circ\text{C}$
I_{IO} Input offset current (see Note 4)		$V_O = 5\text{ V}$, $V_{IC} = 5\text{ V}$	25°C		0.1	60	pA
			70°C		7	300	
I_{IB} Input bias current (see Note 4)			25°C		0.7	60	pA
			70°C		50	600	
V_{ICR} Common-mode input voltage range (see Note 5)			25°C	-0.2 to 9	-0.3 to 9.2		V
			Full range	-0.2 to 8.5			V
V_{OH} High-level output voltage		$V_{ID} = 100\text{ mV}$, $R_L = 10\text{ k}\Omega$	25°C	8	8.5		V
			0°C	7.8	8.5		
			70°C	7.8	8.4		
V_{OL} Low-level output voltage		$V_{ID} = -100\text{ mV}$, $I_{OL} = 0$	25°C	0	50		mV
			0°C	0	50		
			70°C	0	50		
A_{VD} Large-signal differential voltage amplification		$V_O = 1\text{ V to }6\text{ V}$, $R_L = 10\text{ k}\Omega$	25°C	10	36		V/mV
			0°C	7.5	42		
			70°C	7.5	32		
CMRR Common-mode rejection ratio		$V_{IC} = V_{ICRmin}$	25°C	65	85		dB
			0°C	60	88		
			70°C	60	88		
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		$V_{DD} = 5\text{ V to }10\text{ V}$, $V_O = 1.4\text{ V}$	25°C	65	95		dB
			0°C	60	94		
			70°C	60	96		
I_{DD} Supply current (four amplifiers)		$V_O = 5\text{ V}$, No load $V_{IC} = 5\text{ V}$	25°C	3.8	8		mA
			0°C	4.5	8.8		
			70°C	3.2	6.8		

† Full range is 0°C to 70°C.

- NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.



TLC274, TLC274A, TLC274B, TLC274Y, TLC279

LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

SLOS092D – SEPTEMBER 1987 – REVISED MARCH 2001

electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	TLC274I, TLC274AI, TLC274BI, TLC279I			UNIT
				MIN	TYP	MAX	
V_{IO} Input offset voltage	TLC274I	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 0$, $R_L = 10\text{ k}\Omega$	25°C		1.1	10	mV
			Full range			13	
	TLC274AI	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 0$, $R_L = 10\text{ k}\Omega$	25°C		0.9	5	
			Full range			7	
	TLC274BI	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 0$, $R_L = 10\text{ k}\Omega$	25°C		340	2000	μV
			Full range			3500	
	TLC279I	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 0$, $R_L = 10\text{ k}\Omega$	25°C		320	900	
			Full range			2000	
α_{VIO} Average temperature coefficient of input offset voltage			25°C to 85°C		1.8		$\mu\text{V}/^\circ\text{C}$
I_{IO} Input offset current (see Note 4)		$V_O = 2.5\text{ V}$, $V_{IC} = 2.5\text{ V}$	25°C		0.1	60	pA
			85°C		24	1000	
I_{IB} Input bias current (see Note 4)			25°C		0.6	60	pA
			85°C		200	2000	
V_{ICR} Common-mode input voltage range (see Note 5)			25°C	-0.2 to 4	-0.3 to 4.2		V
			Full range	-0.2 to 3.5			V
V_{OH} High-level output voltage		$V_{ID} = 100\text{ mV}$, $R_L = 10\text{ k}\Omega$	25°C	3.2	3.8		V
			-40°C	3	3.8		
			85°C	3	3.8		
V_{OL} Low-level output voltage		$V_{ID} = -100\text{ mV}$, $I_{OL} = 0$	25°C		0	50	mV
			-40°C		0	50	
			85°C		0	50	
A_{VD} Large-signal differential voltage amplification		$V_O = 0.25\text{ V to } 2\text{ V}$, $R_L = 10\text{ k}\Omega$	25°C	5	23		V/mV
			-40°C	3.5	32		
			85°C	3.5	19		
CMRR Common-mode rejection ratio		$V_{IC} = V_{ICRmin}$	25°C	65	80		dB
			-40°C	60	81		
			85°C	60	86		
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		$V_{DD} = 5\text{ V to } 10\text{ V}$, $V_O = 1.4\text{ V}$	25°C	65	95		dB
			-40°C	60	92		
			85°C	60	96		
I_{DD} Supply current (four amplifiers)		$V_O = 2.5\text{ V}$, No load $V_{IC} = 2.5\text{ V}$	25°C		2.7	6.4	mA
			-40°C		3.8	8.8	
			85°C		2.1	4.8	

† Full range is -40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



TLC274, TLC274A, TLC274B, TLC274Y, TLC279 LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

SLOS092D – SEPTEMBER 1987 – REVISED MARCH 2001

electrical characteristics at specified free-air temperature, $V_{DD} = 10\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	TLC274I, TLC274AI, TLC274BI, TLC279I			UNIT
				MIN	TYP	MAX	
V_{IO} Input offset voltage	TLC274I	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 0$, $R_L = 10\text{ k}\Omega$	25°C		1.1	10	mV
			Full range			13	
	TLC274AI	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 0$, $R_L = 10\text{ k}\Omega$	25°C		0.9	5	
			Full range			7	
	TLC274BI	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 0$, $R_L = 10\text{ k}\Omega$	25°C		390	2000	μV
			Full range			3500	
	TLC279I	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 0$, $R_L = 10\text{ k}\Omega$	25°C		370	1200	
			Full range			2900	
α_{VIO} Average temperature coefficient of input offset voltage			25°C to 85°C		2		$\mu\text{V}/^\circ\text{C}$
I_{IO} Input offset current (see Note 4)		$V_O = 5\text{ V}$, $V_{IC} = 5\text{ V}$	25°C		0.1	60	pA
			85°C		26	1000	
I_{IB} Input bias current (see Note 4)			25°C		0.7	60	pA
			85°C		220	2000	
V_{ICR} Common-mode input voltage range (see Note 5)			25°C	-0.2 to 9	-0.3 to 9.2		V
			Full range	-0.2 to 8.5			V
V_{OH} High-level output voltage		$V_{ID} = 100\text{ mV}$, $R_L = 10\text{ k}\Omega$	25°C	8	8.5		V
			-40°C	7.8	8.5		
			85°C	7.8	8.5		
V_{OL} Low-level output voltage		$V_{ID} = -100\text{ mV}$, $I_{OL} = 0$	25°C	0	50		mV
			-40°C	0	50		
			85°C	0	50		
A_{VD} Large-signal differential voltage amplification		$V_O = 1\text{ V to }6\text{ V}$, $R_L = 10\text{ k}\Omega$	25°C	10	36		V/mV
			-40°C	7	47		
			85°C	7	31		
CMRR Common-mode rejection ratio		$V_{IC} = V_{ICRmin}$	25°C	65	85		dB
			-40°C	60	87		
			85°C	60	88		
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		$V_{DD} = 5\text{ V to }10\text{ V}$, $V_O = 1.4\text{ V}$	25°C	65	95		dB
			-40°C	60	92		
			85°C	60	96		
I_{DD} Supply current (four amplifiers)		$V_O = 5\text{ V}$, No load $V_{IC} = 5\text{ V}$	25°C	3.8	8		mA
			-40°C	5.5	10		
			85°C	2.9	6.4		

† Full range is -40°C to 85°C.

- NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.



TLC274, TLC274A, TLC274B, TLC274Y, TLC279

LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

SLOS092D – SEPTEMBER 1987 – REVISED MARCH 2001

electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	TLC274M, TLC279M			UNIT
				MIN	TYP	MAX	
V_{IO} Input offset voltage	TLC274M	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 0$, $R_L = 10\text{ k}\Omega$	25°C	1.1	10		mV
			Full range		12		
	TLC279M	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 0$, $R_L = 10\text{ k}\Omega$	25°C	320	900		μV
			Full range		3750		
α_{VIO} Average temperature coefficient of input offset voltage			25°C to 125°C	2.1			$\mu\text{V}/^\circ\text{C}$
I_{IO} Input offset current (see Note 4)		$V_O = 2.5\text{ V}$, $V_{IC} = 2.5\text{ V}$	25°C	0.1	60		pA
			125°C	1.4	15		nA
I_{IB} Input bias current (see Note 4)			25°C	0.6	60		pA
			125°C	9	35		nA
V_{ICR} Common-mode input voltage range (see Note 5)			25°C	0 to 4	-0.3 to 4.2		V
			Full range	0 to 3.5			V
V_{OH} High-level output voltage		$V_{ID} = 100\text{ mV}$, $R_L = 10\text{ k}\Omega$	25°C	3.2	3.8		V
			-55°C	3	3.8		
			125°C	3	3.8		
V_{OL} Low-level output voltage		$V_{ID} = -100\text{ mV}$, $I_{OL} = 0$	25°C	0	50		mV
			-55°C	0	50		
			125°C	0	50		
A_{VD} Large-signal differential voltage amplification		$V_O = 0.25\text{ V to } 2\text{ V}$, $R_L = 10\text{ k}\Omega$	25°C	5	23		V/mV
			-55°C	3.5	35		
			125°C	3.5	16		
CMRR Common-mode rejection ratio		$V_{IC} = V_{ICRmin}$	25°C	65	80		dB
			-55°C	60	81		
			125°C	60	84		
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		$V_{DD} = 5\text{ V to } 10\text{ V}$, $V_O = 1.4\text{ V}$	25°C	65	95		dB
			-55°C	60	90		
			125°C	60	97		
I_{DD} Supply current (four amplifiers)		$V_O = 2.5\text{ V}$, No load $V_{IC} = 2.5\text{ V}$	25°C	2.7	6.4		mA
			-55°C	4	10		
			125°C	1.9	4.4		

† Full range is -55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



TLC274, TLC274A, TLC274B, TLC274Y, TLC279 LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

SLOS092D – SEPTEMBER 1987 – REVISED MARCH 2001

electrical characteristics at specified free-air temperature, $V_{DD} = 10\text{ V}$ (unless) otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	TLC274M, TLC279M			UNIT
				MIN	TYP	MAX	
V_{IO} Input offset voltage	TLC274M	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 0$, $R_L = 10\text{ k}\Omega$	25°C		1.1	10	mV
			Full range			12	
	TLC279M	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 0$, $R_L = 10\text{ k}\Omega$	25°C		370	1200	μV
			Full range			4300	
α_{VIO} Average temperature coefficient of input offset voltage			25°C to 125°C		2.2		$\mu\text{V}/^\circ\text{C}$
I_{IO} Input offset current (see Note 4)		$V_O = 5\text{ V}$, $V_{IC} = 5\text{ V}$	25°C		0.1	60	pA
			125°C		1.8	15	nA
I_{IB} Input bias current (see Note 4)			25°C		0.7	60	pA
			125°C		10	35	nA
V_{ICR} Common-mode input voltage range (see Note 5)			25°C	0 to 9	-0.3 to 9.2		V
			Full range	0 to 8.5			V
V_{OH} High-level output voltage		$V_{ID} = 100\text{ mV}$, $R_L = 10\text{ k}\Omega$	25°C	8	8.5		V
			-55°C	7.8	8.5		
			125°C	7.8	8.4		
V_{OL} Low-level output voltage		$V_{ID} = -100\text{ mV}$, $I_{OL} = 0$	25°C		0	50	mV
			-55°C		0	50	
			125°C		0	50	
A_{VD} Large-signal differential voltage amplification		$V_O = 1\text{ V to }6\text{ V}$, $R_L = 10\text{ k}\Omega$	25°C	10	36		V/mV
			-55°C	7	50		
			125°C	7	27		
CMRR Common-mode rejection ratio		$V_{IC} = V_{ICRmin}$	25°C	65	85		dB
			-55°C	60	87		
			125°C	60	86		
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		$V_{DD} = 5\text{ V to }10\text{ V}$, $V_O = 1.4\text{ V}$	25°C	65	95		dB
			-55°C	60	90		
			125°C	60	97		
I_{DD} Supply current (four amplifiers)		$V_O = 5\text{ V}$, No load $V_{IC} = 5\text{ V}$	25°C		3.8	8	mA
			-55°C		6.0	12	
			125°C		2.5	5.6	

† Full range is -55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.



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TLC274, TLC274A, TLC274B, TLC274Y, TLC279

LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

SLOS092D – SEPTEMBER 1987 – REVISED MARCH 2001

operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS		T_A	TLC274C, TLC274AC, TLC274AC, TLC274BC, TLC279C			UNIT
				MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 10\ \Omega$, $C_L = 20\text{ pF}$, See Figure 1	$V_{I\text{PP}} = 1\text{ V}$	25°C		3.6		V/ μs
			0°C		4		
			70°C		3		
		$V_{I\text{PP}} = 2.5\text{ V}$	25°C		2.9		
			0°C		3.1		
			70°C		2.5		
V_n Equivalent input noise voltage	$f = 1\text{ kHz}$, See Figure 2	$R_S = 20\ \Omega$,	25°C		25		nV/ $\sqrt{\text{Hz}}$
B_{OM} Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 10\text{ k}\Omega$,	$C_L = 20\text{ pF}$, See Figure 1	25°C		320		kHz
			0°C		340		
			70°C		260		
B_1 Unity-gain bandwidth	$V_I = 10\text{ mV}$, See Figure 3	$C_L = 20\text{ pF}$,	25°C		1.7		MHz
			0°C		2		
			70°C		1.3		
ϕ_m Phase margin	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$,	$f = B_1$,	25°C		46°		
			0°C		47°		
			70°C		44°		

operating characteristics at specified free-air temperature, $V_{DD} = 10\text{ V}$

PARAMETER	TEST CONDITIONS		T_A	TLC274C, TLC274AC, TLC274AC, TLC274BC, TLC279C			UNIT
				MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 10\ \Omega$, $C_L = 20\text{ pF}$, See Figure 1	$V_{I\text{PP}} = 1\text{ V}$	25°C		5.3		V/ μs
			0°C		5.9		
			70°C		4.3		
		$V_{I\text{PP}} = 5.5\text{ V}$	25°C		4.6		
			0°C		5.1		
			70°C		3.8		
V_n Equivalent input noise voltage	$f = 1\text{ kHz}$, See Figure 2	$R_S = 20\ \Omega$,	25°C		25		nV/ $\sqrt{\text{Hz}}$
B_{OM} Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 10\text{ k}\Omega$,	$C_L = 20\text{ pF}$, See Figure 1	25°C		200		kHz
			0°C		220		
			70°C		140		
B_1 Unity-gain bandwidth	$V_I = 10\text{ mV}$, See Figure 3	$C_L = 20\text{ pF}$,	25°C		2.2		MHz
			0°C		2.5		
			70°C		1.8		
ϕ_m Phase margin	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$,	$f = B_1$, See Figure 3	25°C		49°		
			0°C		50°		
			70°C		46°		



TLC274, TLC274A, TLC274B, TLC274Y, TLC279 LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

SLOS092D – SEPTEMBER 1987 – REVISED MARCH 2001

operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS		T_A	TLC274I, TLC274AI, TLC274BI, TLC279I			UNIT
				MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 10\text{ k}\Omega$, $C_L = 20\text{ pF}$, See Figure 1	$V_{I\text{PP}} = 1\text{ V}$	25°C		3.6		$\text{V}/\mu\text{s}$
			–40°C		4.5		
			85°C		2.8		
		$V_{I\text{PP}} = 2.5\text{ V}$	25°C		2.9		
			–40°C		3.5		
			85°C		2.3		
V_n Equivalent input noise voltage	$f = 1\text{ kHz}$, See Figure 2	$R_S = 20\text{ }\Omega$,	25°C		25		$\text{nV}/\sqrt{\text{Hz}}$
B_{OM} Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 10\text{ k}\Omega$,	$C_L = 20\text{ pF}$, See Figure 1	25°C		320		kHz
			–40°C		380		
			85°C		250		
B_1 Unity-gain bandwidth	$V_I = 10\text{ mV}$, See Figure 3	$C_L = 20\text{ pF}$,	25°C		1.7		MHz
			–40°C		2.6		
			85°C		1.2		
ϕ_m Phase margin	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$,	$f = B_1$, See Figure 3	25°C		46°		
			–40°C		49°		
			85°C		43°		

operating characteristics at specified free-air temperature, $V_{DD} = 10\text{ V}$

PARAMETER	TEST CONDITIONS		T_A	TLC274I, TLC274AI, TLC274BI, TLC279I			UNIT
				MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 10\text{ }\Omega$, $C_L = 20\text{ pF}$, See Figure 1	$V_{I\text{PP}} = 1\text{ V}$	25°C		5.3		$\text{V}/\mu\text{s}$
			–40°C		6.7		
			85°C		4		
		$V_{I\text{PP}} = 5.5\text{ V}$	25°C		4.6		
			–40°C		5.8		
			85°C		3.5		
V_n Equivalent input noise voltage	$f = 1\text{ kHz}$, See Figure 2	$R_S = 20\text{ }\Omega$,	25°C		25		$\text{nV}/\sqrt{\text{Hz}}$
B_{OM} Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 10\text{ k}\Omega$,	$C_L = 20\text{ pF}$, See Figure 1	25°C		200		kHz
			–40°C		260		
			85°C		130		
B_1 Unity-gain bandwidth	$V_I = 10\text{ mV}$, See Figure 3	$C_L = 20\text{ pF}$,	25°C		2.2		MHz
			–40°C		3.1		
			85°C		1.7		
ϕ_m Phase margin	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$,	$f = B_1$, See Figure 3	25°C		49°		
			–40°C		52°		
			85°C		46°		



TLC274, TLC274A, TLC274B, TLC274Y, TLC279

LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

SLOS092D – SEPTEMBER 1987 – REVISED MARCH 2001

operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS		T_A	TLC274M, TLC279M			UNIT
				MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 10\text{ k}\Omega$, $C_L = 20\text{ pF}$, See Figure 1	$V_{I\text{PP}} = 1\text{ V}$	25°C		3.6		V/ μs
			–55°C		4.7		
			125°C		2.3		
		$V_{I\text{PP}} = 2.5\text{ V}$	25°C		2.9		
			–55°C		3.7		
			125°C		2		
V_n Equivalent input noise voltage	$f = 1\text{ kHz}$, See Figure 2	$R_S = 20\text{ }\Omega$	25°C		25		nV/ $\sqrt{\text{Hz}}$
B_{OM} Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 10\text{ k}\Omega$	$C_L = 20\text{ pF}$, See Figure 1	25°C		320		kHz
			–55°C		400		
			125°C		230		
B_1 Unity-gain bandwidth	$V_I = 10\text{ mV}$, See Figure 3	$C_L = 20\text{ pF}$	25°C		1.7		MHz
			–55°C		2.9		
			125°C		1.1		
ϕ_m Phase margin	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$	$f = B_1$, See Figure 3	25°C		46°		
			–55°C		49°		
			125°C		41°		

operating characteristics at specified free-air temperature, $V_{DD} = 10\text{ V}$

PARAMETER	TEST CONDITIONS		T_A	TLC274M, TLC279M			UNIT
				MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 10\text{ }\Omega$, $C_L = 20\text{ pF}$, See Figure 1	$V_{I\text{PP}} = 1\text{ V}$	25°C		5.3		V/ μs
			–55°C		7.1		
			125°C		3.1		
		$V_{I\text{PP}} = 5.5\text{ V}$	25°C		4.6		
			–55°C		6.1		
			125°C		2.7		
V_n Equivalent input noise voltage	$f = 1\text{ kHz}$, See Figure 2	$R_S = 20\text{ }\Omega$	25°C		25		nV/ $\sqrt{\text{Hz}}$
B_{OM} Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 10\text{ k}\Omega$	$C_L = 20\text{ pF}$, See Figure 1	25°C		200		kHz
			–55°C		280		
			125°C		110		
B_1 Unity-gain bandwidth	$V_I = 10\text{ mV}$, See Figure 3	$C_L = 20\text{ pF}$	25°C		2.2		MHz
			–55°C		3.4		
			125°C		1.6		
ϕ_m Phase margin	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$	$f = B_1$, See Figure 3	25°C		49°		
			–55°C		52°		
			125°C		44°		



TLC274, TLC274A, TLC274B, TLC274Y, TLC279 LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

SLOS092D – SEPTEMBER 1987 – REVISED MARCH 2001

electrical characteristics, $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TLC274Y			UNIT
		MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 0$, $R_L = 10\text{ k}\Omega$		1.1	10	mV
I_{IO} Input offset current (see Note 4)	$V_O = 2.5\text{ V}$, $V_{IC} = 2.5\text{ V}$	0.1			pA
I_{IB} Input bias current (see Note 4)		0.6			pA
V_{ICR} Common-mode input voltage range (see Note 5)		-0.2 to 4	-0.3 to 4.2		V
V_{OH} High-level output voltage	$V_{ID} = 100\text{ mV}$, $R_L = 10\text{ k}\Omega$	3.2	3.8		V
V_{OL} Low-level output voltage	$V_{ID} = -100\text{ mV}$, $I_{OL} = 0$	0	50		mV
A_{VD} Large-signal differential voltage amplification	$V_O = 0.25\text{ V to } 2\text{ V}$, $R_L = 10\text{ k}\Omega$	5	23		V/mV
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$	65	80		dB
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 5\text{ V to } 10\text{ V}$, $V_O = 1.4\text{ V}$	65	95		dB
I_{DD} Supply current (four amplifiers)	$V_O = 2.5\text{ V}$, No load $V_{IC} = 2.5\text{ V}$	2.7	6.4		mA

electrical characteristics, $V_{DD} = 10\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TLC274Y			UNIT
		MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 0$, $R_L = 10\text{ k}\Omega$		1.1	10	mV
I_{IO} Input offset current (see Note 4)	$V_O = 5\text{ V}$, $V_{IC} = 5\text{ V}$	0.1			pA
I_{IB} Input bias current (see Note 4)		0.7			pA
V_{ICR} Common-mode input voltage range (see Note 5)		-0.2 to 9	-0.3 to 9.2		V
V_{OH} High-level output voltage	$V_{ID} = 100\text{ mV}$, $R_L = 10\text{ k}\Omega$	8	8.5		V
V_{OL} Low-level output voltage	$V_{ID} = -100\text{ mV}$, $I_{OL} = 0$	0	50		mV
A_{VD} Large-signal differential voltage amplification	$V_O = 1\text{ V to } 6\text{ V}$, $R_L = 10\text{ k}\Omega$	10	36		V/mV
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$	65	85		dB
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 5\text{ V to } 10\text{ V}$, $V_O = 1.4\text{ V}$	65	95		dB
I_{DD} Supply current (four amplifiers)	$V_O = 5\text{ V}$, No load $V_{IC} = 5\text{ V}$	3.8	8		mA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.



TLC274, TLC274A, TLC274B, TLC274Y, TLC279

LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

SLOS092D – SEPTEMBER 1987 – REVISED MARCH 2001

operating characteristics, $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TLC274Y			UNIT
		MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 10\text{ k}\Omega$, $C_L = 20\text{ pF}$, See Figure 1	$V_{IPP} = 1\text{ V}$ $V_{IPP} = 2.5\text{ V}$			$\text{V}/\mu\text{s}$
V_n Equivalent input noise voltage	$f = 1\text{ kHz}$, $R_S = 20\text{ }\Omega$, See Figure 2	25			$\text{nV}/\sqrt{\text{Hz}}$
B_{OM} Maximum output-swing bandwidth	$V_O = V_{OH}$, $C_L = 20\text{ pF}$, See Figure 1	320			kHz
B_1 Unity-gain bandwidth	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$, See Figure 3	1.7			MHz
ϕ_m Phase margin	$V_I = 10\text{ mV}$, $f = B_1$, See Figure 3	46°			

operating characteristics, $V_{DD} = 10\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TLC274Y			UNIT
		MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 10\text{ k}\Omega$, $C_L = 20\text{ pF}$, See Figure 1	$V_{IPP} = 1\text{ V}$ $V_{IPP} = 5.5\text{ V}$			$\text{V}/\mu\text{s}$
V_n Equivalent input noise voltage	$f = 1\text{ kHz}$, $R_S = 20\text{ }\Omega$, See Figure 2	25			$\text{nV}/\sqrt{\text{Hz}}$
B_{OM} Maximum output-swing bandwidth	$V_O = V_{OH}$, $C_L = 20\text{ pF}$, See Figure 1	200			kHz
B_1 Unity-gain bandwidth	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$, See Figure 3	2.2			MHz
ϕ_m Phase margin	$V_I = 10\text{ mV}$, $f = B_1$, See Figure 3	49°			

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC274 and TLC279 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.

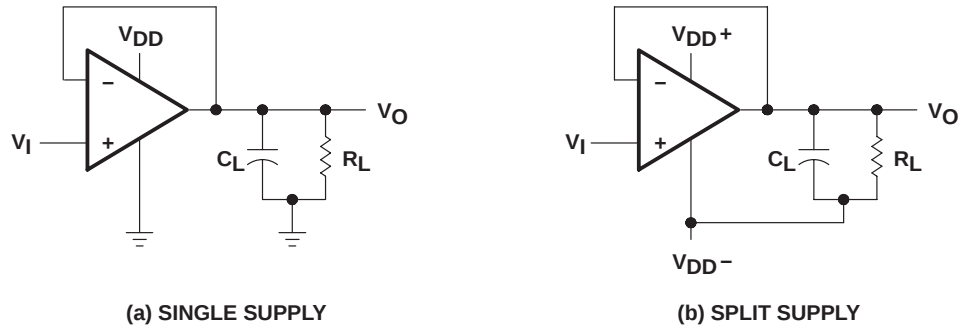


Figure 1. Unity-Gain Amplifier

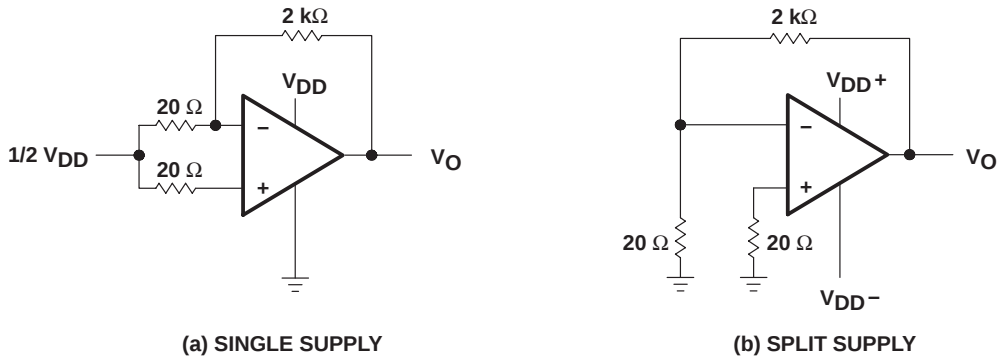


Figure 2. Noise-Test Circuit

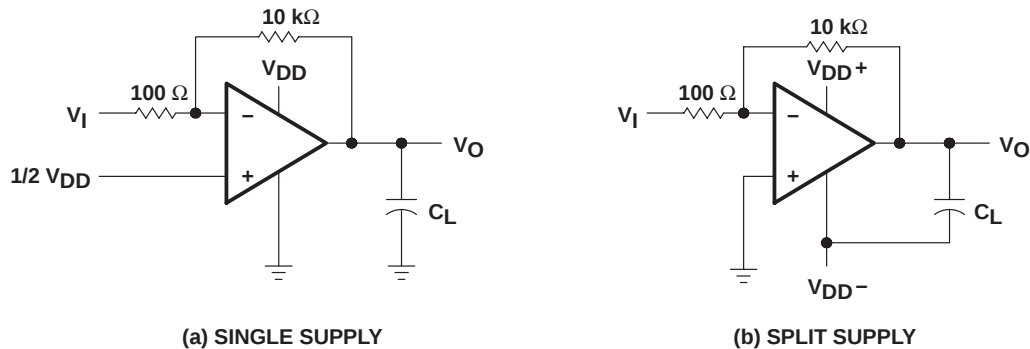


Figure 3. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC274 and TLC279 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs are shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution: many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

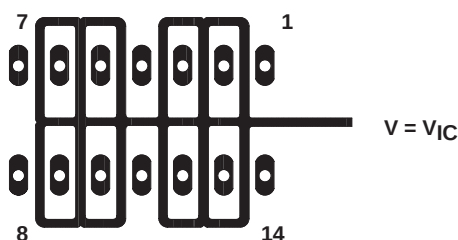


Figure 4. Isolation Metal Around Device Inputs (J and N packages)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

PARAMETER MEASUREMENT INFORMATION

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

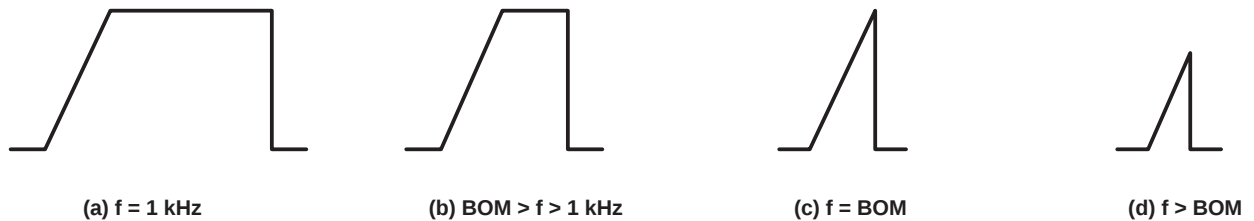


Figure 5. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TLC274, TLC274A, TLC274B, TLC274Y, TLC279

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SLOS092D – SEPTEMBER 1987 – REVISED MARCH 2001

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6, 7
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	8, 9
V_{OH}	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	10, 11 12 13
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	14, 15 16 17 18, 19
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	20 21 32, 33
I_{IB}	Input bias current	vs Free-air temperature	22
I_{IO}	Input offset current	vs Free-air temperature	22
V_{IC}	Common-mode input voltage	vs Supply voltage	23
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	24 25
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27
	Normalized slew rate	vs Free-air temperature	28
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	29
B_1	Unity-gain bandwidth	vs Free-air temperature vs Supply voltage	30 31
ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature vs Load capacitance	34 35 36
V_n	Equivalent input noise voltage	vs Frequency	37
	Phase shift	vs Frequency	32, 33



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TYPICAL CHARACTERISTICS

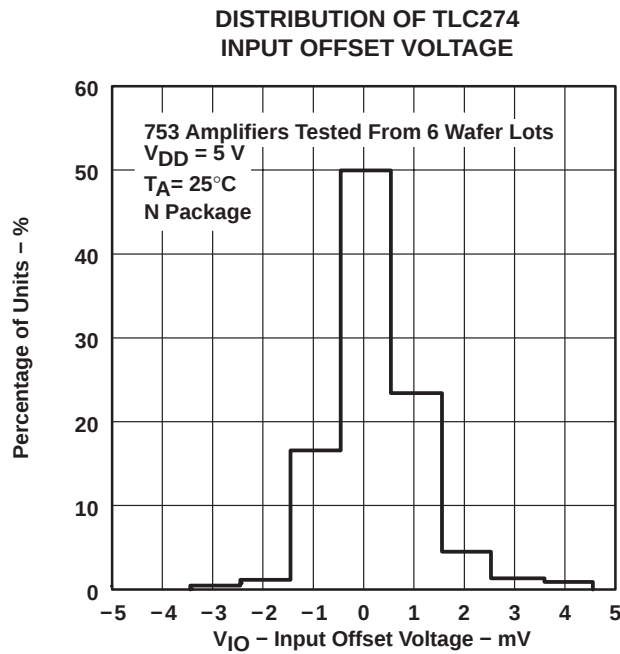


Figure 6

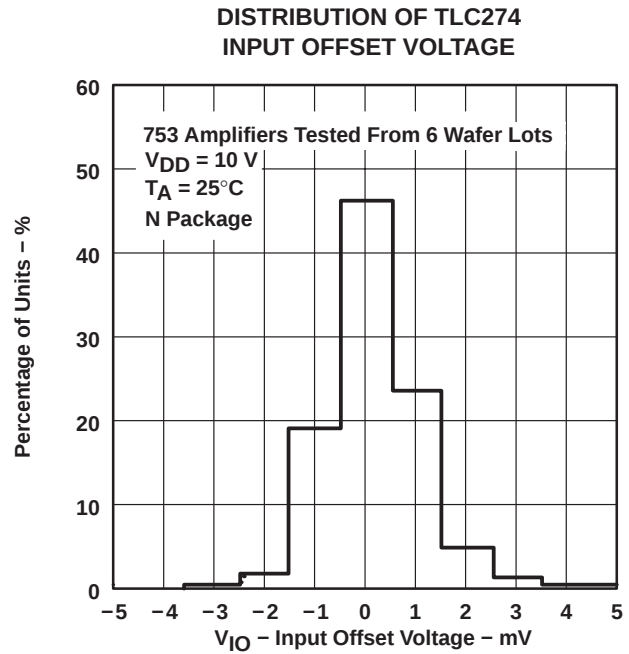


Figure 7

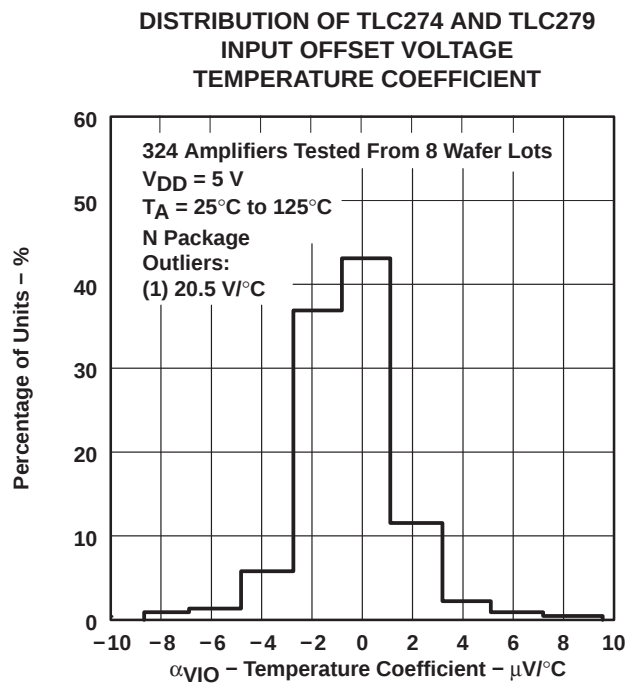


Figure 8

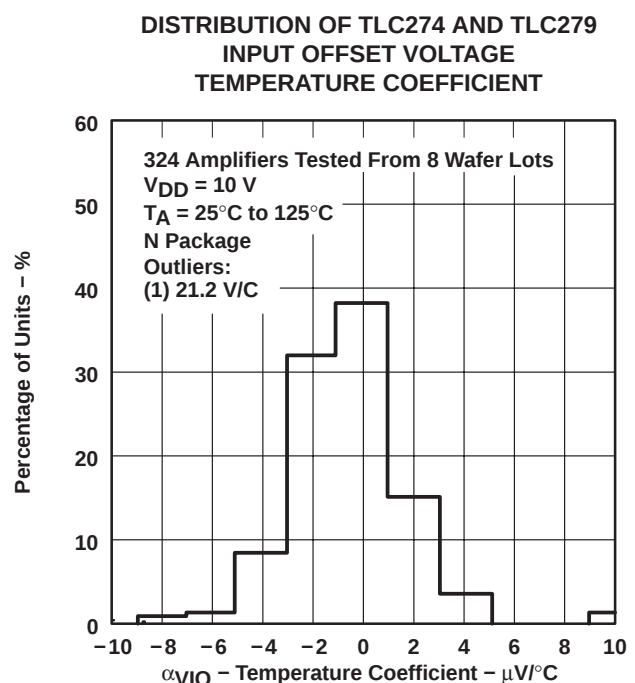


Figure 9

TLC274, TLC274A, TLC274B, TLC274Y, TLC279

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SLOS092D – SEPTEMBER 1987 – REVISED MARCH 2001

TYPICAL CHARACTERISTICS†

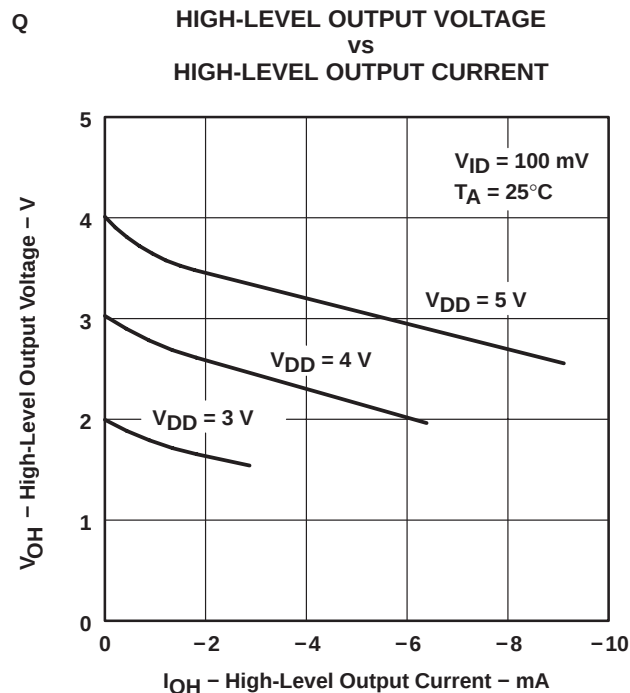


Figure 10

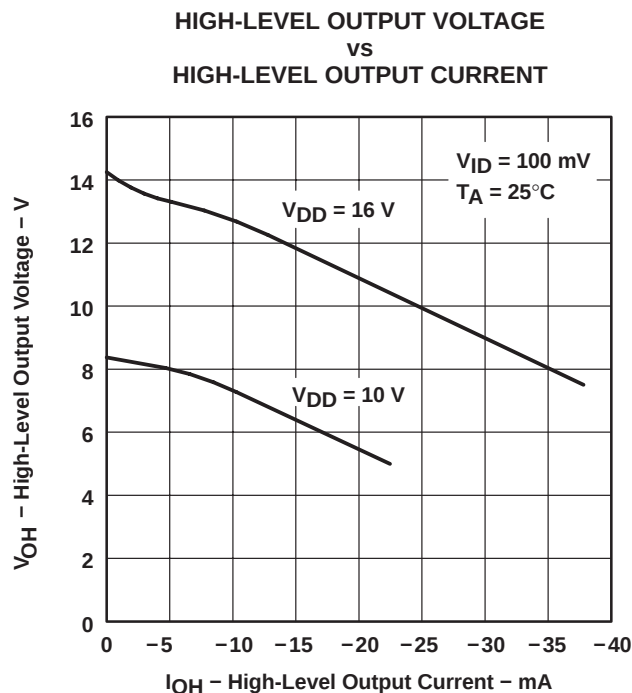


Figure 11

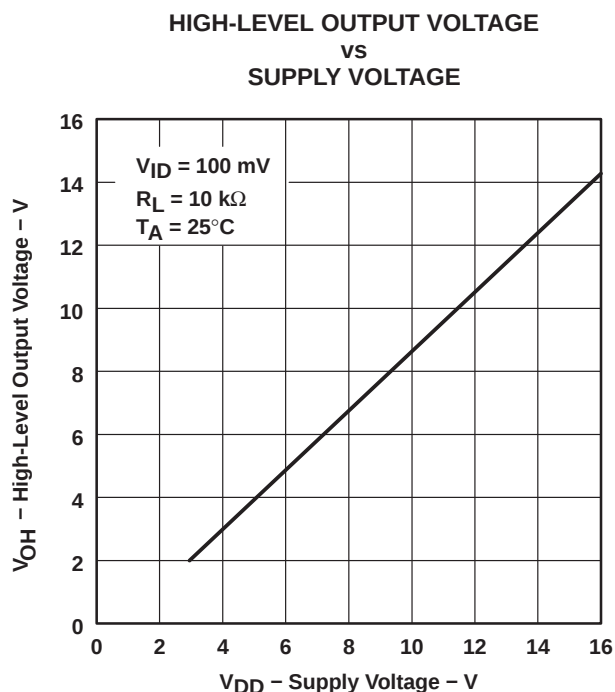


Figure 12

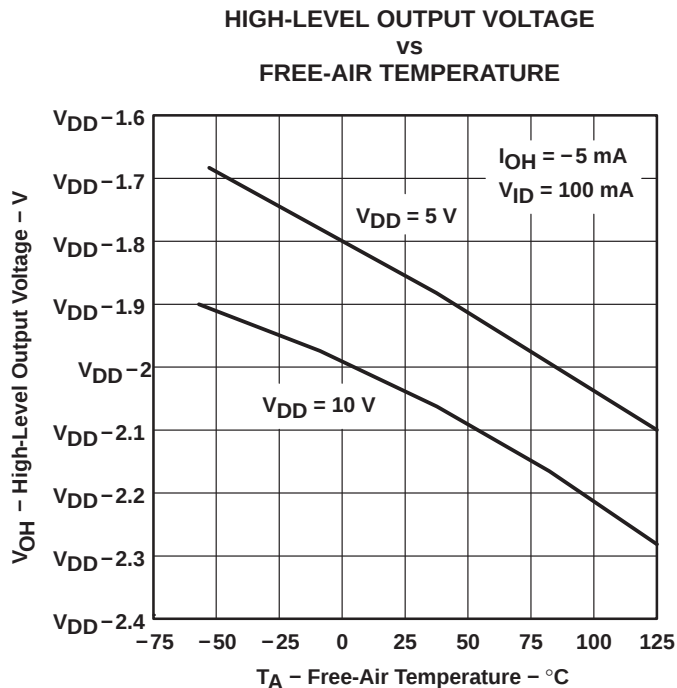


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

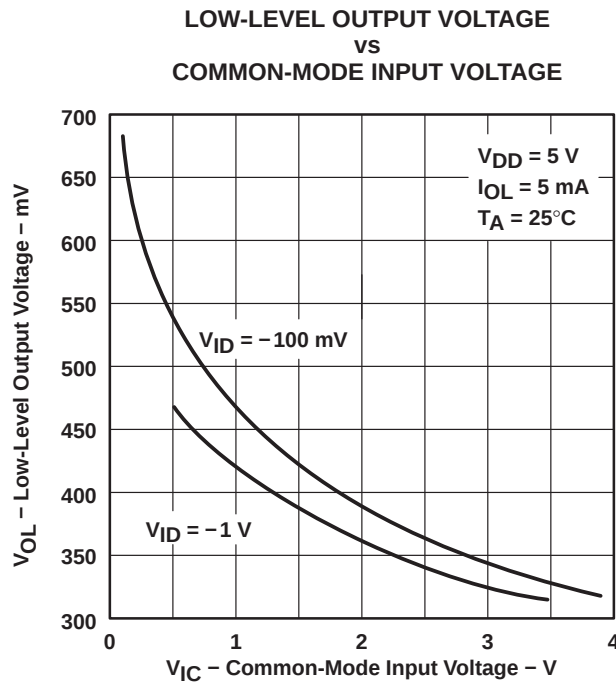


Figure 14

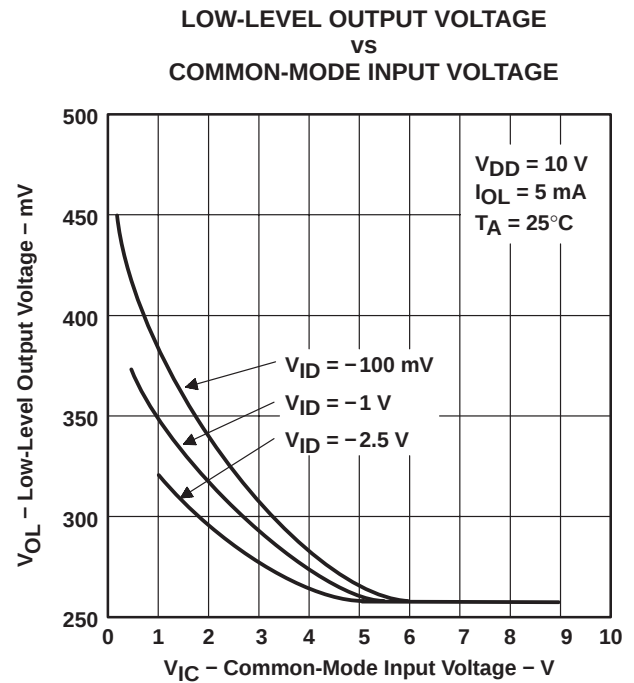


Figure 15

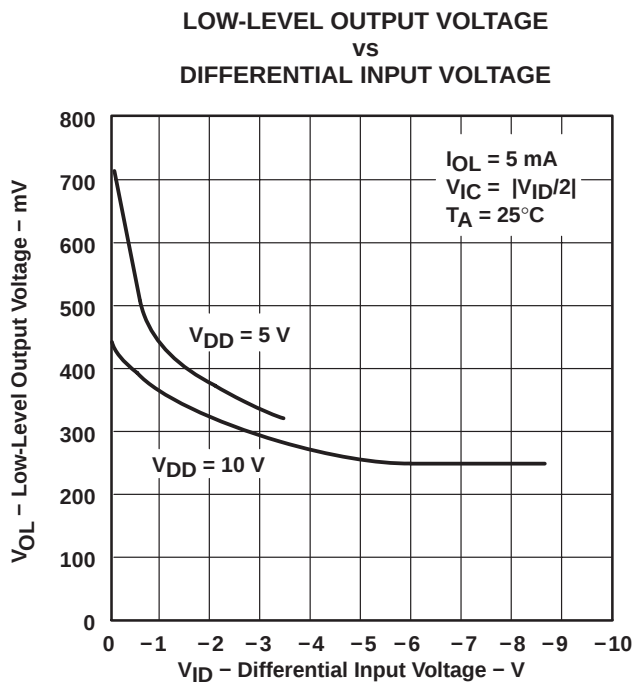


Figure 16

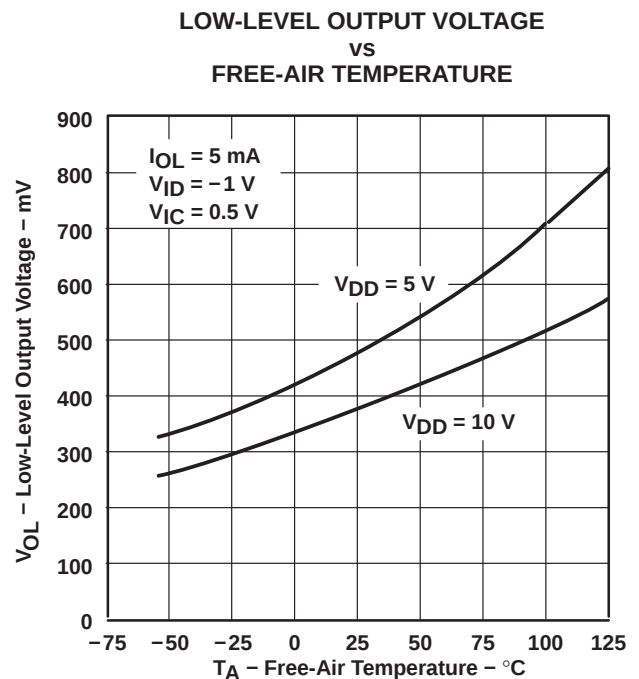


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TLC274, TLC274A, TLC274B, TLC274Y, TLC279

LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

SLOS092D – SEPTEMBER 1987 – REVISED MARCH 2001

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

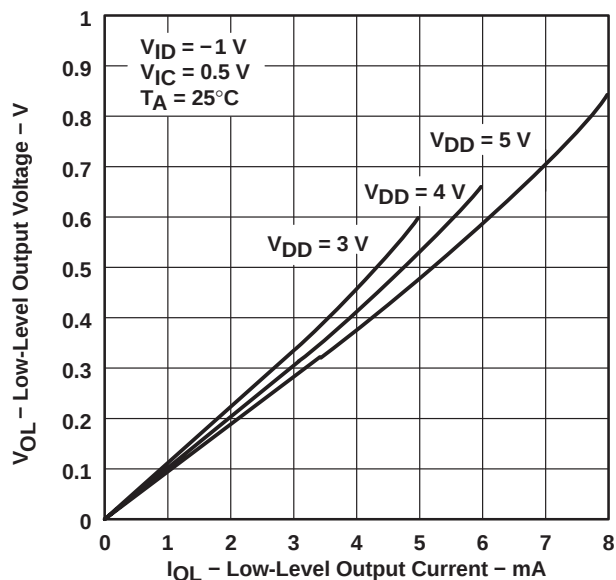


Figure 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

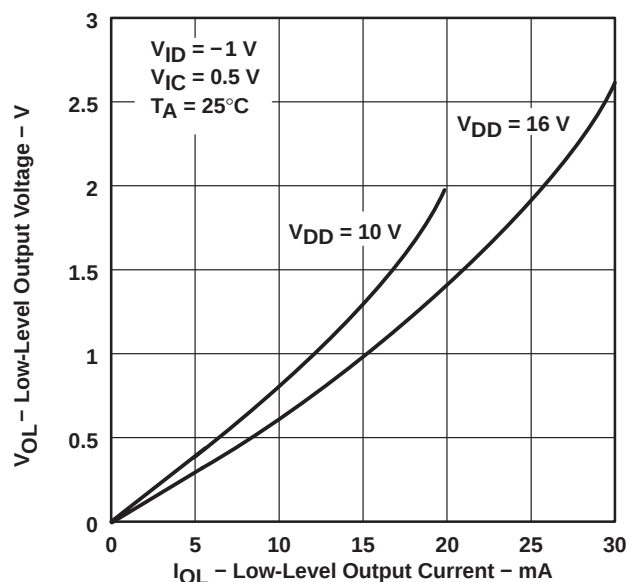


Figure 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

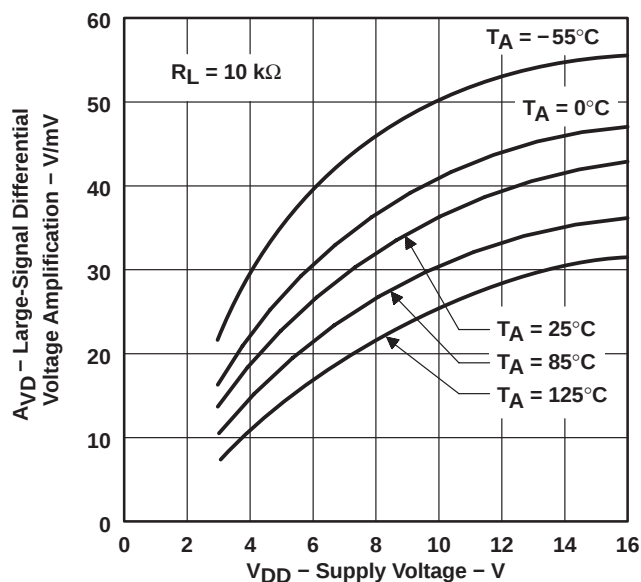


Figure 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

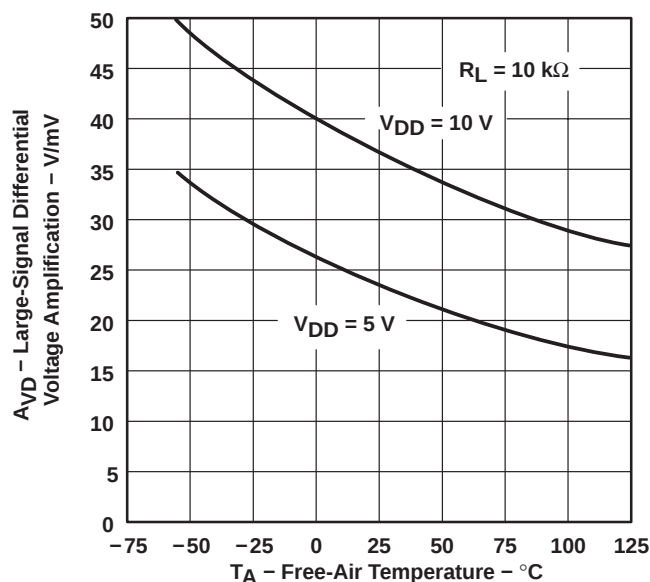
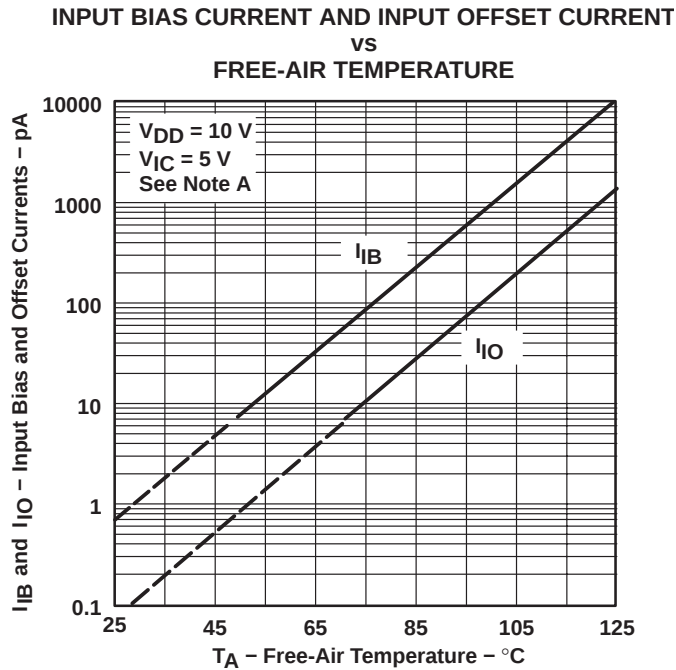


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 22

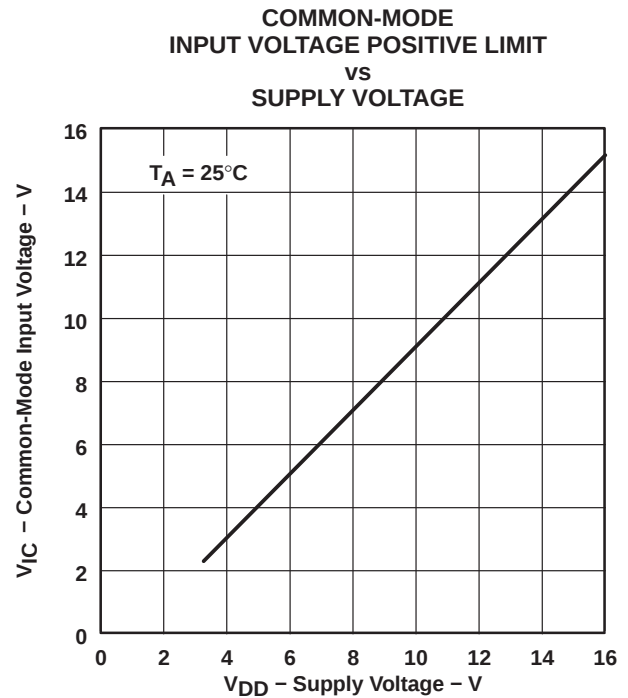


Figure 23

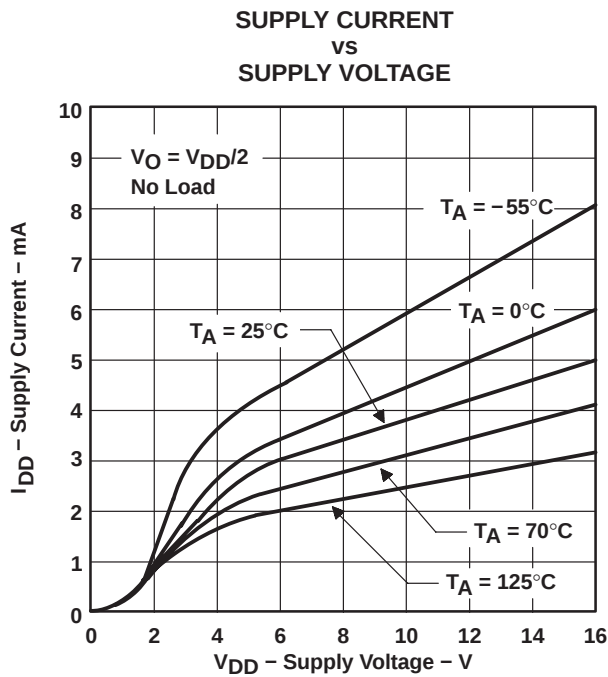


Figure 24

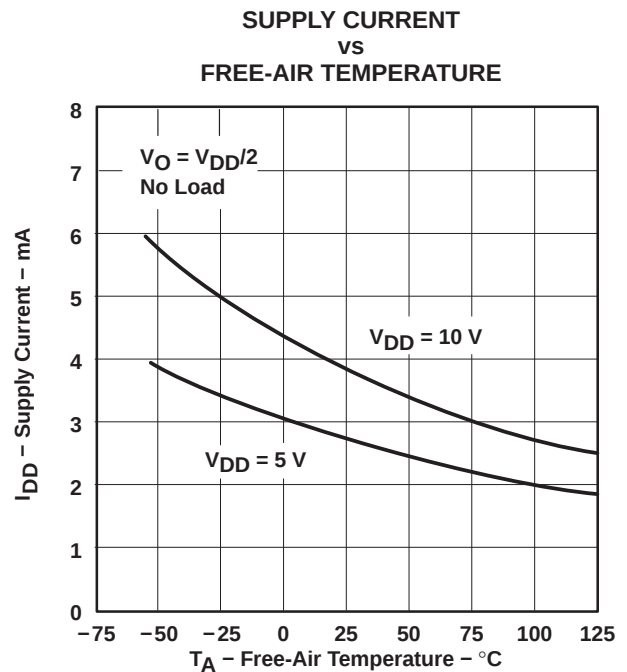


Figure 25

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TLC274, TLC274A, TLC274B, TLC274Y, TLC279

LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

SLOS092D – SEPTEMBER 1987 – REVISED MARCH 2001

TYPICAL CHARACTERISTICS†

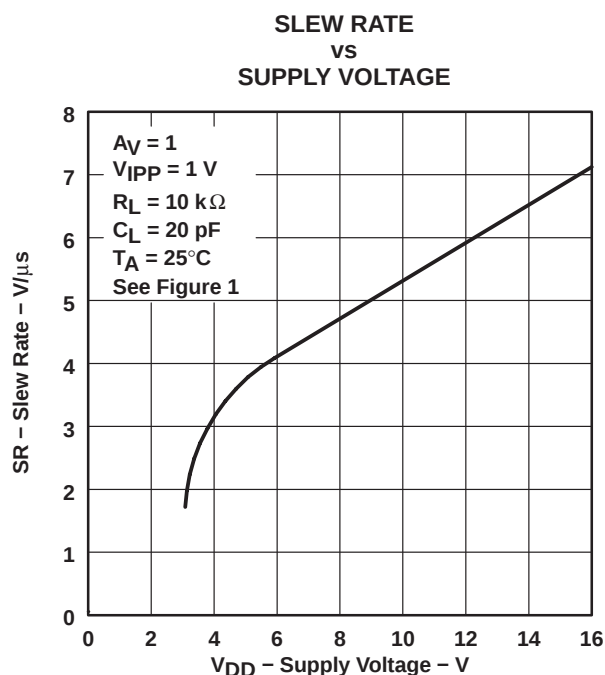


Figure 26

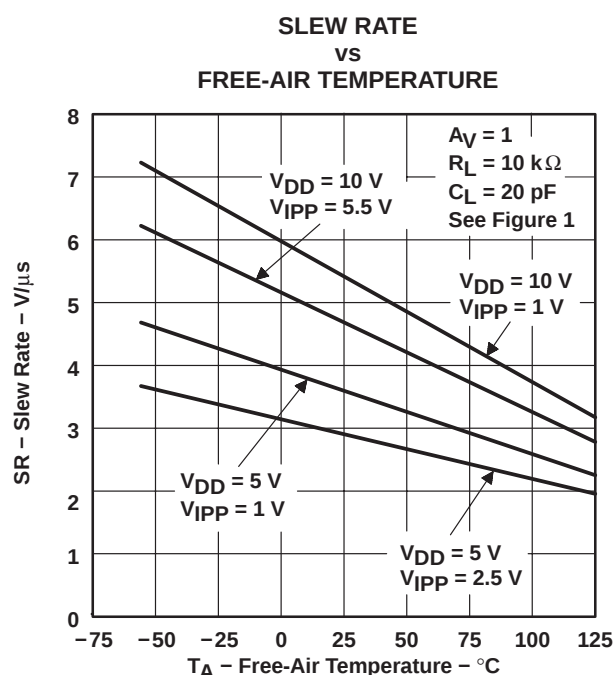


Figure 27

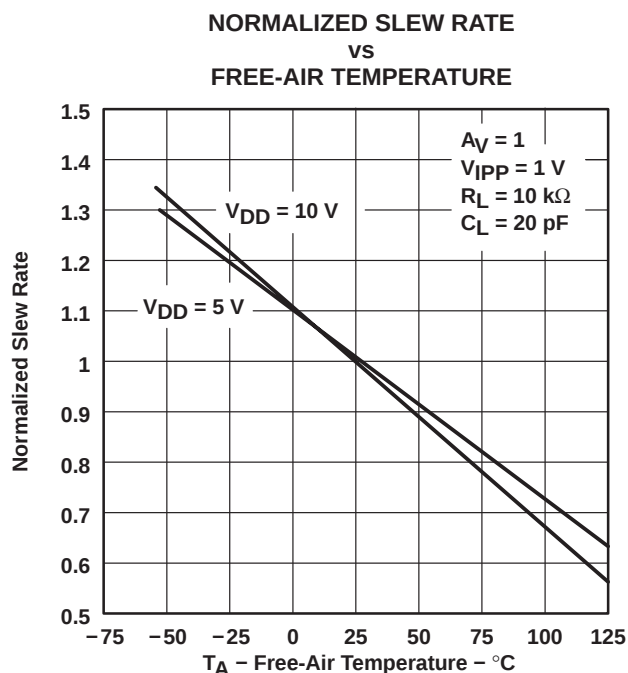


Figure 28

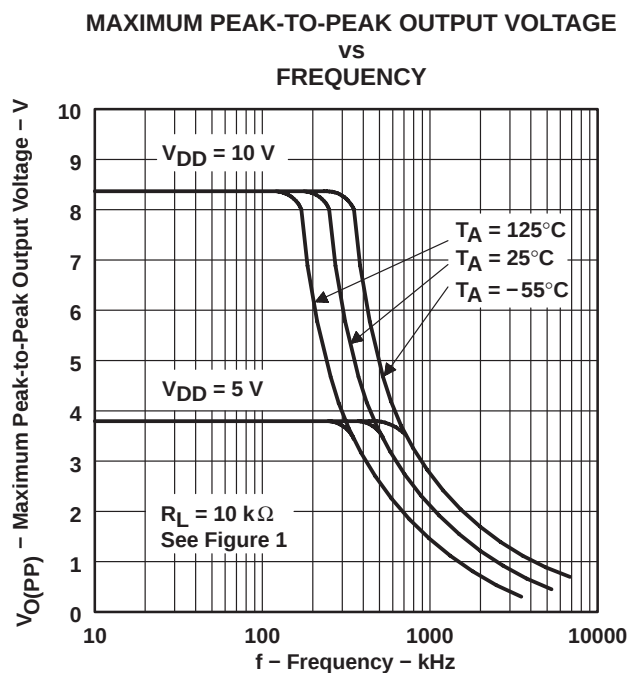


Figure 29

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

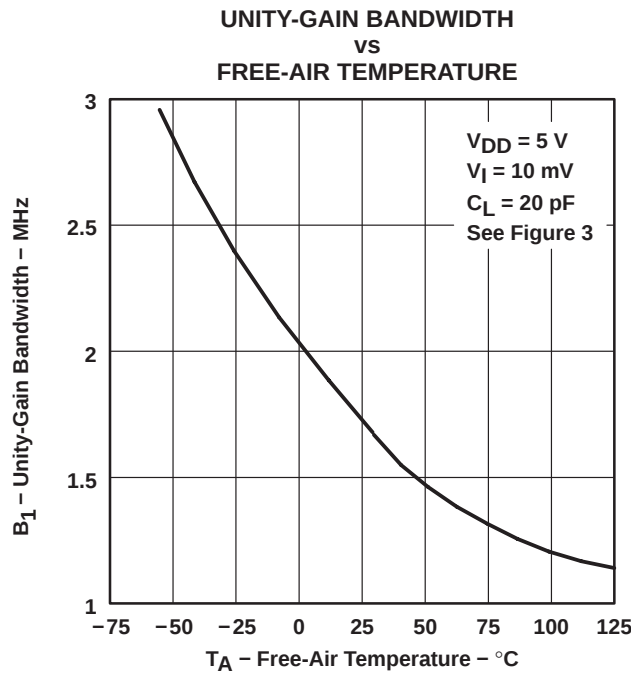


Figure 30

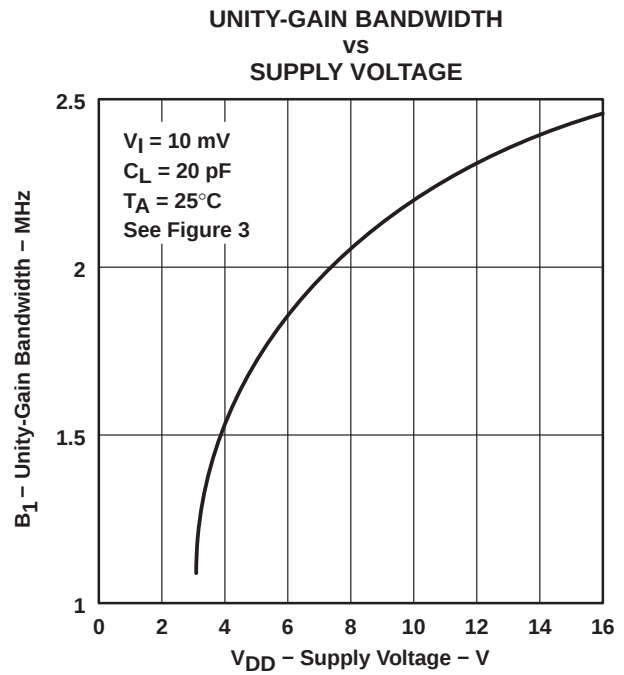


Figure 31

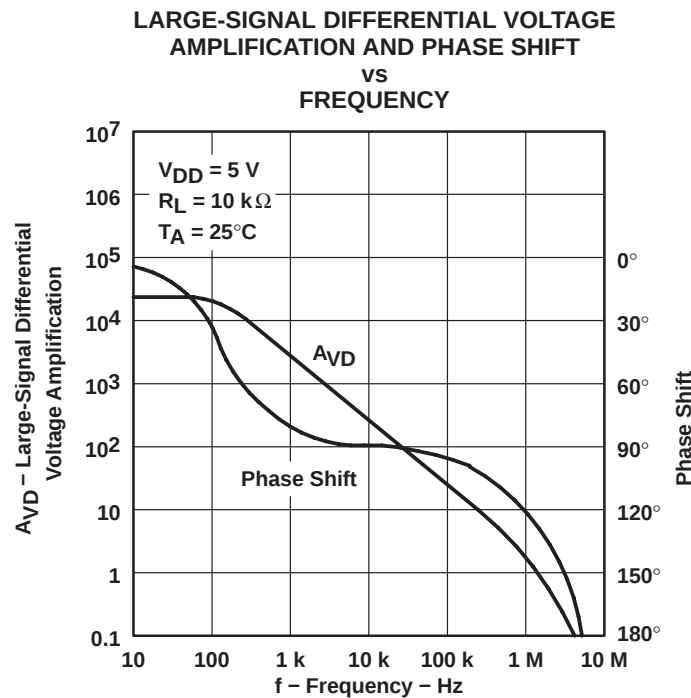


Figure 32

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TLC274, TLC274A, TLC274B, TLC274Y, TLC279
LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS†

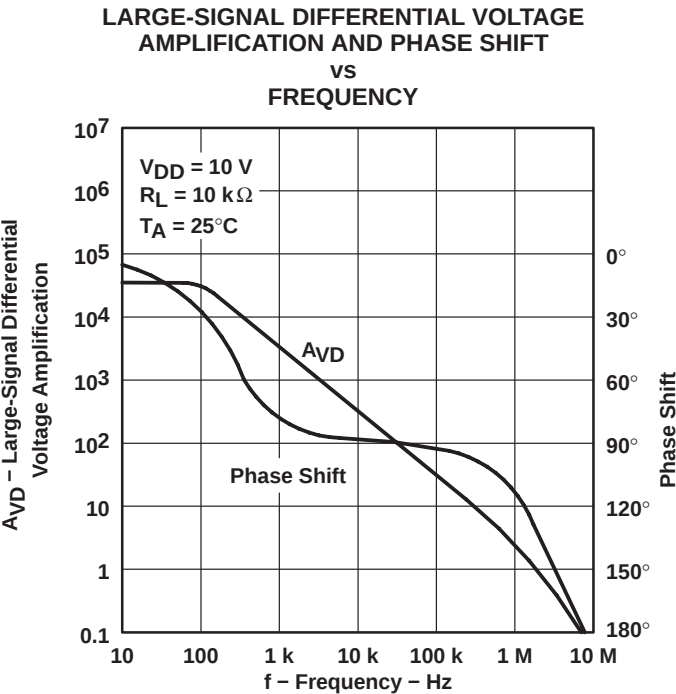


Figure 33

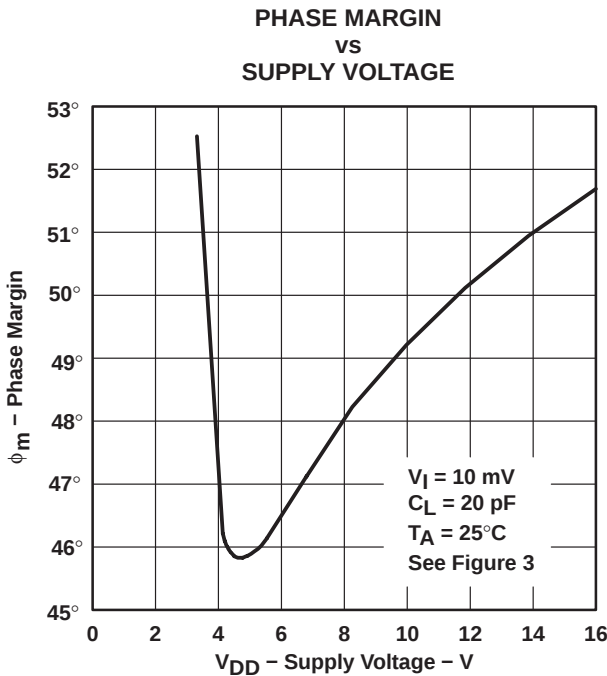


Figure 34

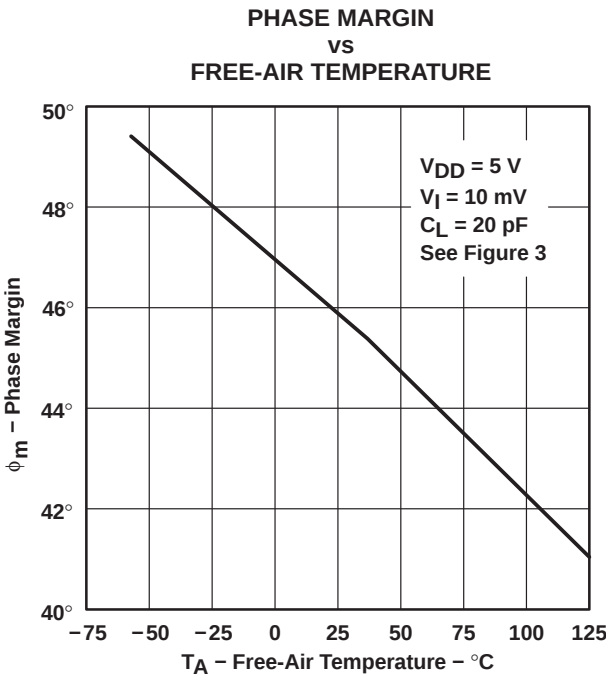


Figure 35

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

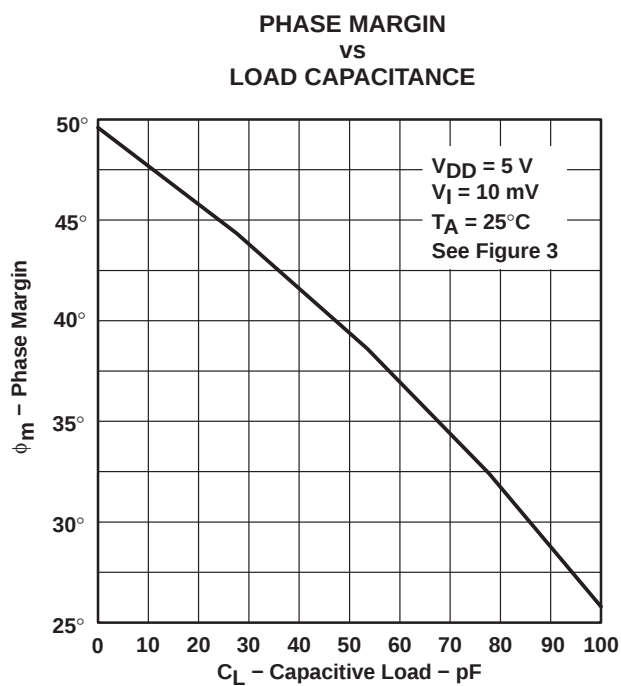


Figure 36

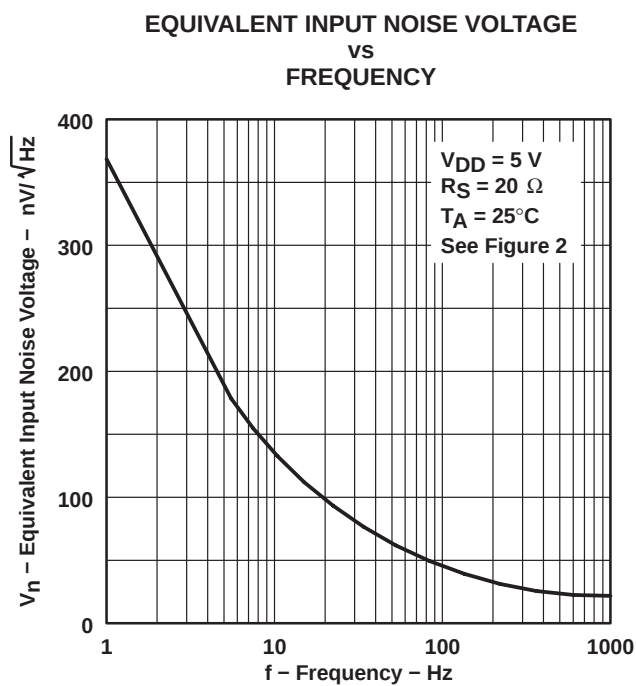


Figure 37

APPLICATION INFORMATION

single-supply operation

While the TLC274 and TLC279 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC274 and TLC279 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC274 and TLC279 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require R_C decoupling.

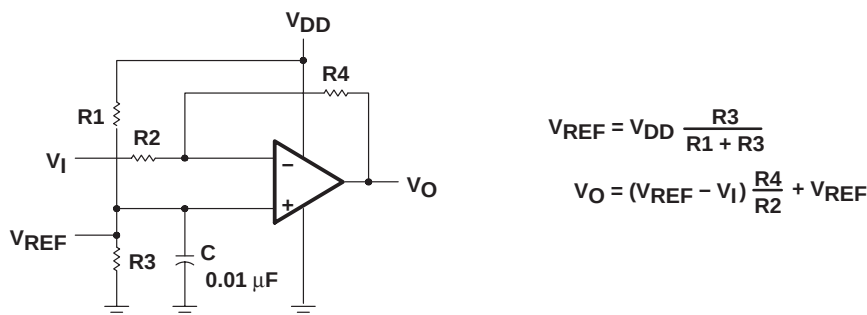


Figure 38. Inverting Amplifier With Voltage Reference

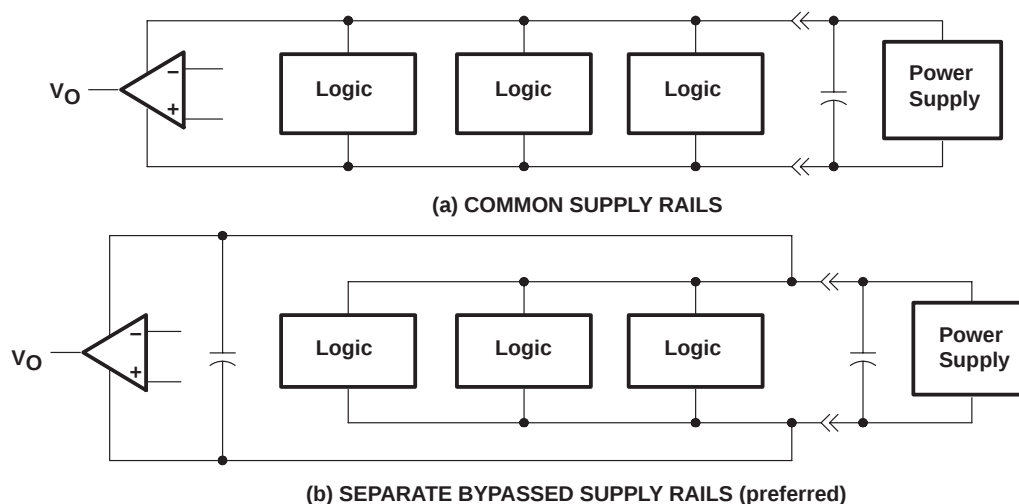


Figure 39. Common Versus Separate Supply Rails

APPLICATION INFORMATION

input characteristics

The TLC274 and TLC279 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1\text{ V}$ at $T_A = 25^\circ\text{C}$ and at $V_{DD} - 1.5\text{ V}$ at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLC274 and TLC279 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically $0.1\text{ }\mu\text{V/month}$, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC274 and TLC279 are well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

Unused amplifiers should be connected as grounded unity-gain followers to avoid possible oscillation.

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC274 and TLC279 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than $50\text{ k}\Omega$, since bipolar devices exhibit greater noise currents.

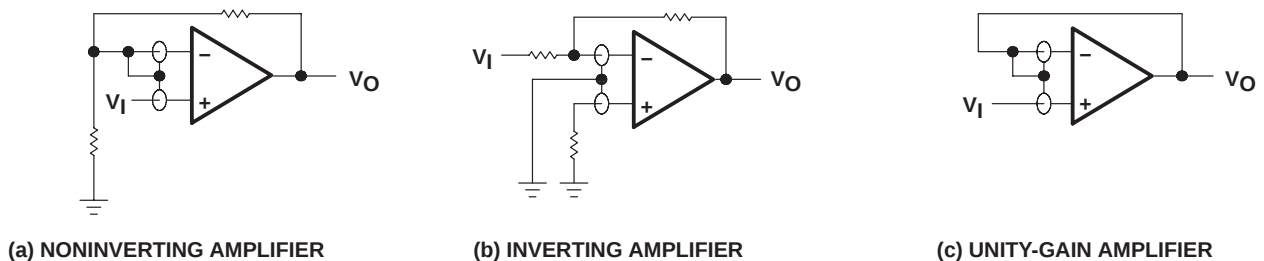


Figure 40. Guard-Ring Schemes

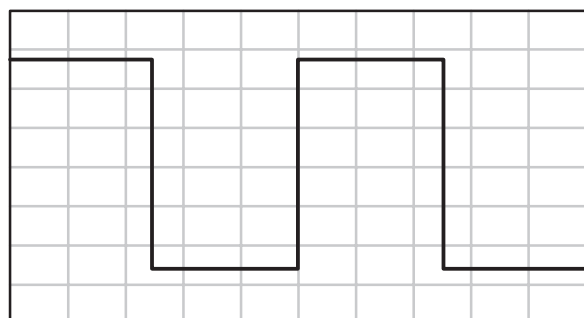
output characteristics

The output stage of the TLC274 and TLC279 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

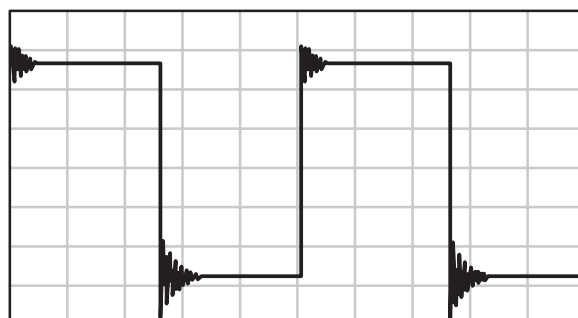
All operating characteristics of the TLC274 and TLC279 were measured using a 20-pF load. The devices drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance alleviates the problem.

APPLICATION INFORMATION

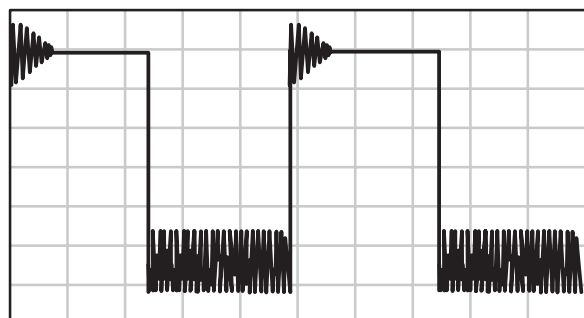
output characteristics (continued)



(a) $C_L = 20 \text{ pF}$, $R_L = \text{NO LOAD}$



(b) $C_L = 130 \text{ pF}$, $R_L = \text{NO LOAD}$



(c) $C_L = 150 \text{ pF}$, $R_L = \text{NO LOAD}$

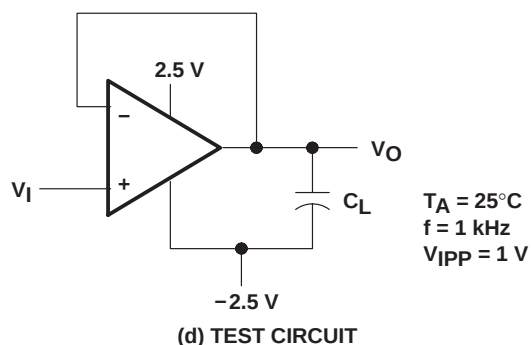
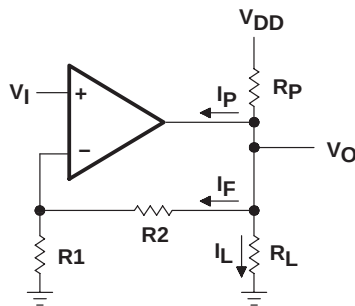


Figure 41. Effect of Capacitive Loads and Test Circuit

Although the TLC274 and TLC279 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60Ω and 180Ω , depending on how hard the op amp input is driven. With very low values of R_P , a voltage offset from 0 V at the output occurs. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

APPLICATION INFORMATION

output characteristics (continued)



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required
by the operational amplifier
(typically 500 μ A)

Figure 42. Resistive Pullup to Increase V_{OH}

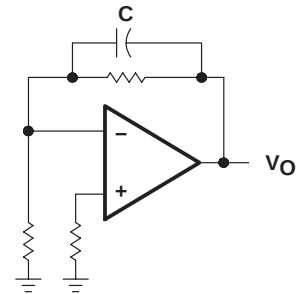


Figure 43. Compensation for
Input Capacitance

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

The TLC274 and TLC279 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature-dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC274 and TLC279 inputs and outputs were designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μ F typical) located across the supply rails as close to the device as possible.

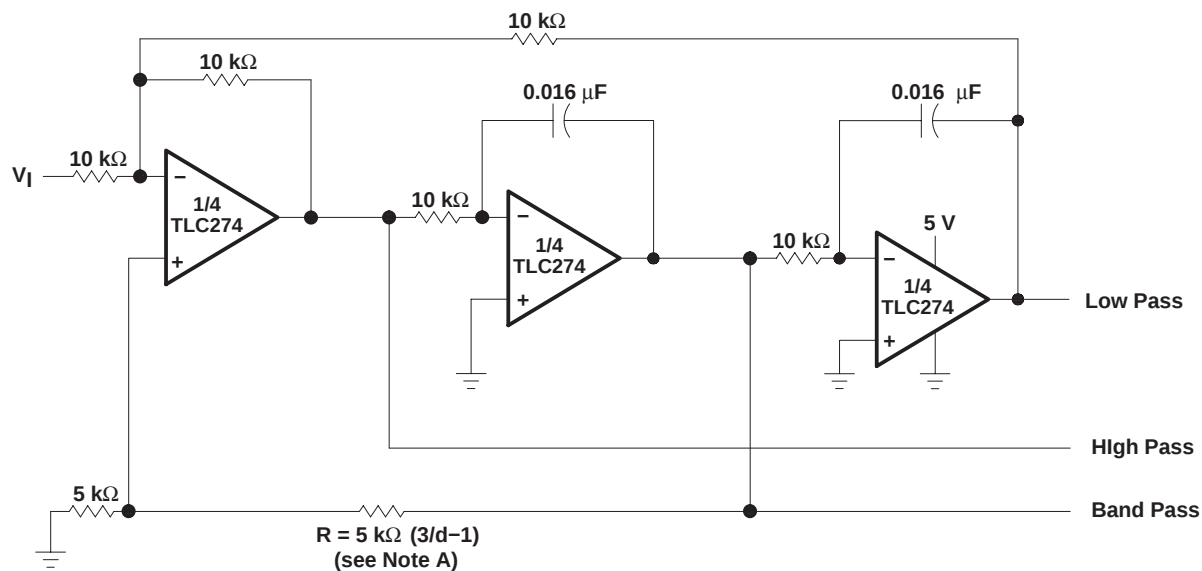
The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

TLC274, TLC274A, TLC274B, TLC274Y, TLC279

LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

SLOS092D – SEPTEMBER 1987 – REVISED MARCH 2001

APPLICATION INFORMATION



NOTE A: d = damping factor, $1/Q$

Figure 44. State-Variable Filter

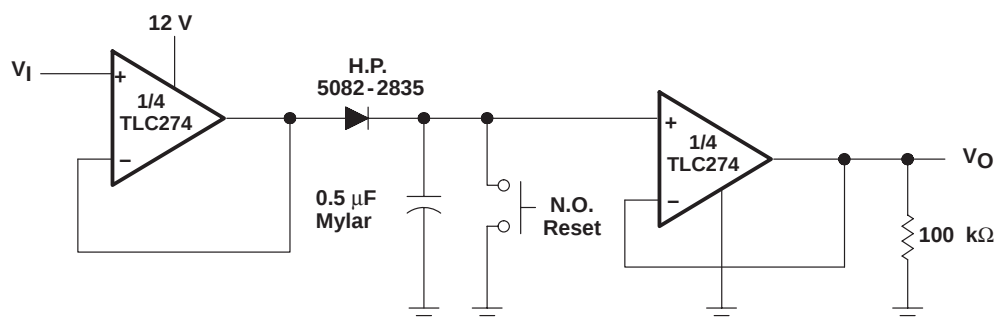
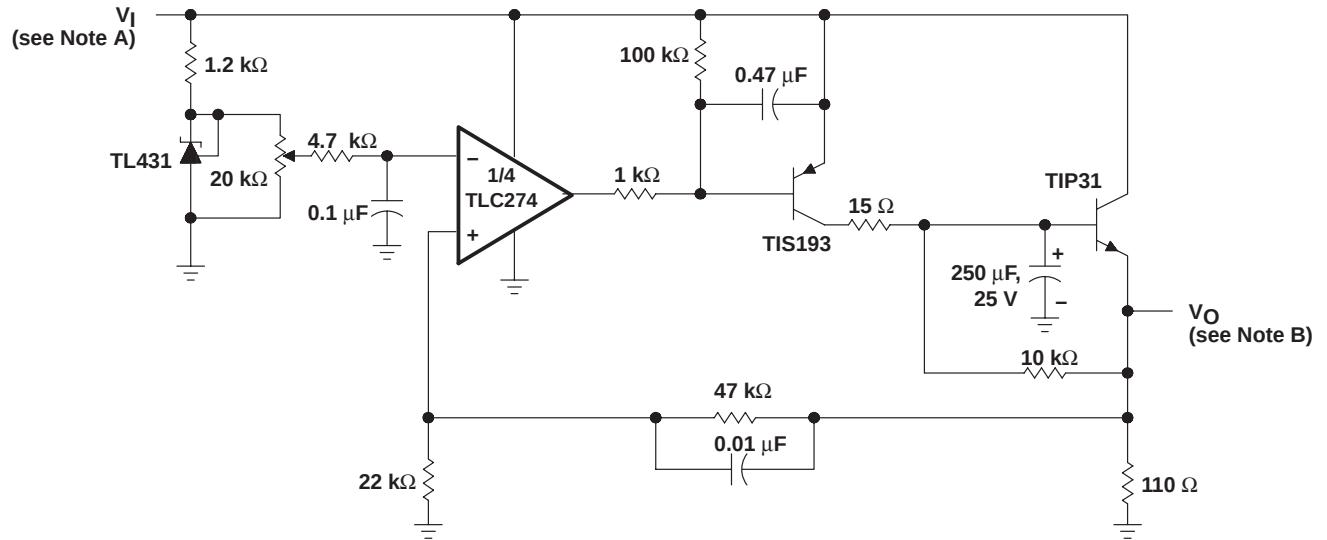


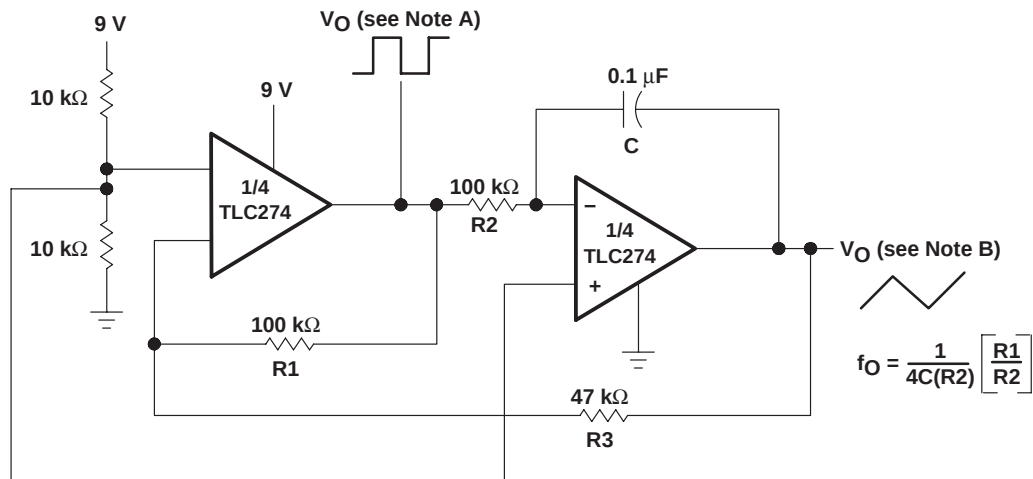
Figure 45. Positive-Peak Detector

APPLICATION INFORMATION



NOTES: B. $V_I = 3.5 \text{ V to } 15 \text{ V}$
C. $V_O = 2 \text{ V, } 0 \text{ to } 1 \text{ A}$

Figure 46. Logic-Array Power Supply



NOTES: A. $V_{O(PP)} = 8 \text{ V}$
B. $V_{O(PP)} = 4 \text{ V}$

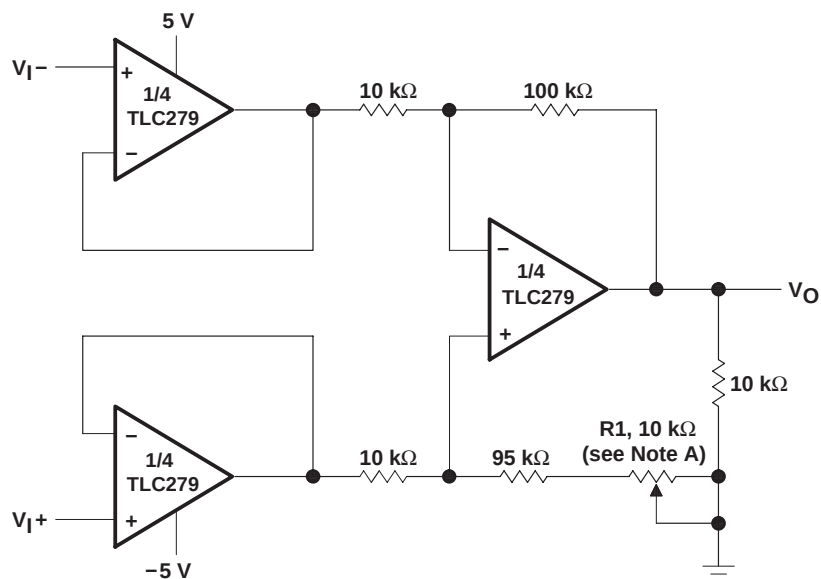
Figure 47. Single-Supply Function Generator

TLC274, TLC274A, TLC274B, TLC274Y, TLC279

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SLOS092D – SEPTEMBER 1987 – REVISED MARCH 2001

APPLICATION INFORMATION



NOTE C: CMRR adjustment must be noninductive.

Figure 48. Low-Power Instrumentation Amplifier

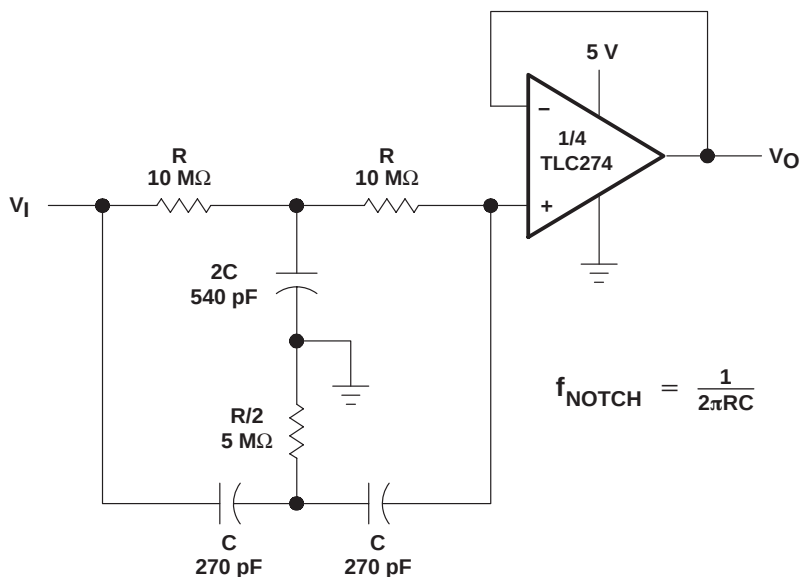


Figure 49. Single-Supply Twin-T Notch Filter

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC274ACD	ACTIVE	SOIC	D	14	50	RoHS & Green	Call TI NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC274AC	Samples
TLC274ACDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC274AC	Samples
TLC274ACN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC274ACN	Samples
TLC274ACNE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC274ACN	Samples
TLC274AID	ACTIVE	SOIC	D	14	50	RoHS & Green	Call TI NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC274AI	Samples
TLC274AIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC274AI	Samples
TLC274AIN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLC274AIN	Samples
TLC274BCD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC274BC	Samples
TLC274BCDG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC274BC	Samples
TLC274BCDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC274BC	Samples
TLC274BCN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC274BCN	Samples
TLC274BCNE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC274BCN	Samples
TLC274BCNS	ACTIVE	SO	NS	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC274B	Samples
TLC274BID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC274BI	Samples
TLC274BIDG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC274BI	Samples
TLC274BIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC274BI	Samples
TLC274BIDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC274BI	Samples
TLC274BIN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLC274BIN	Samples
TLC274CD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC274C	Samples
TLC274CDB	ACTIVE	SSOP	DB	14	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P274	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC274CDBG4	ACTIVE	SSOP	DB	14	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P274	Samples
TLC274CDBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P274	Samples
TLC274CDG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC274C	Samples
TLC274CDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC274C	Samples
TLC274CDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC274C	Samples
TLC274CN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC274CN	Samples
TLC274CNE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC274CN	Samples
TLC274CNS	ACTIVE	SO	NS	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC274	Samples
TLC274CNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC274	Samples
TLC274CPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P274	Samples
TLC274CPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P274	Samples
TLC274CPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P274	Samples
TLC274ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC274I	Samples
TLC274IDG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC274I	Samples
TLC274IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC274I	Samples
TLC274IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLC274IN	Samples
TLC274INE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLC274IN	Samples
TLC274IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	P274	Samples
TLC274IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y274	Samples
TLC274IPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y274	Samples
TLC274MD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLC274M	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC274MDG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLC274M	Samples
TLC274MDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLC274M	Samples
TLC279CD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC279C	Samples
TLC279CDG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC279C	Samples
TLC279CDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC279C	Samples
TLC279CN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC279CN	Samples
TLC279ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC279I	Samples
TLC279IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC279I	Samples
TLC279IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLC279IN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

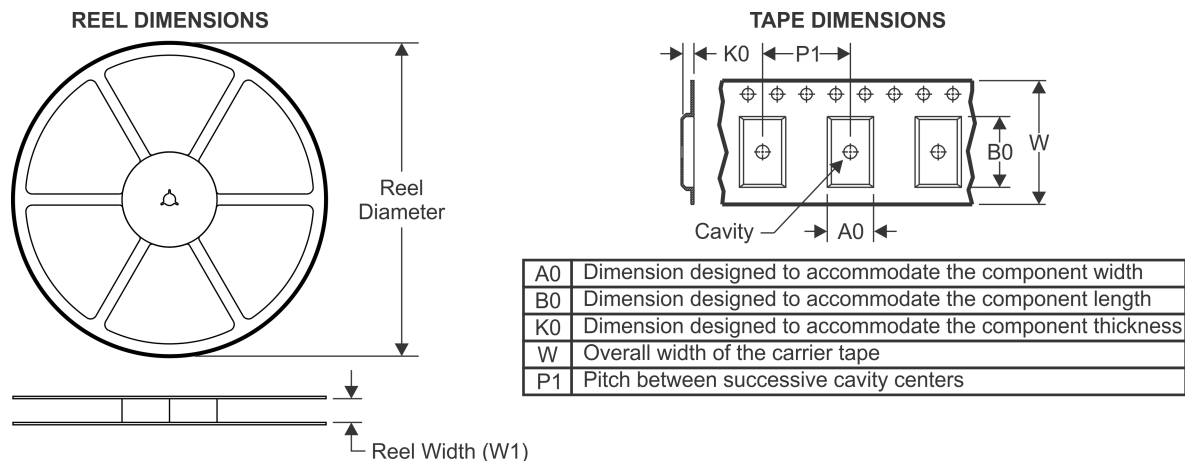
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

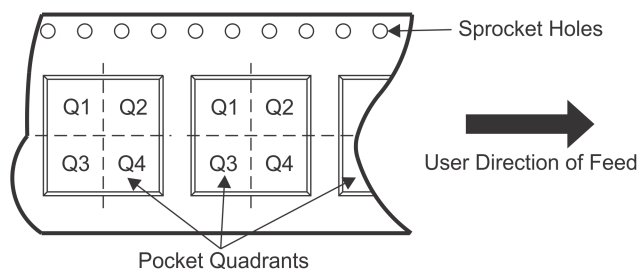
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TAPE AND REEL INFORMATION



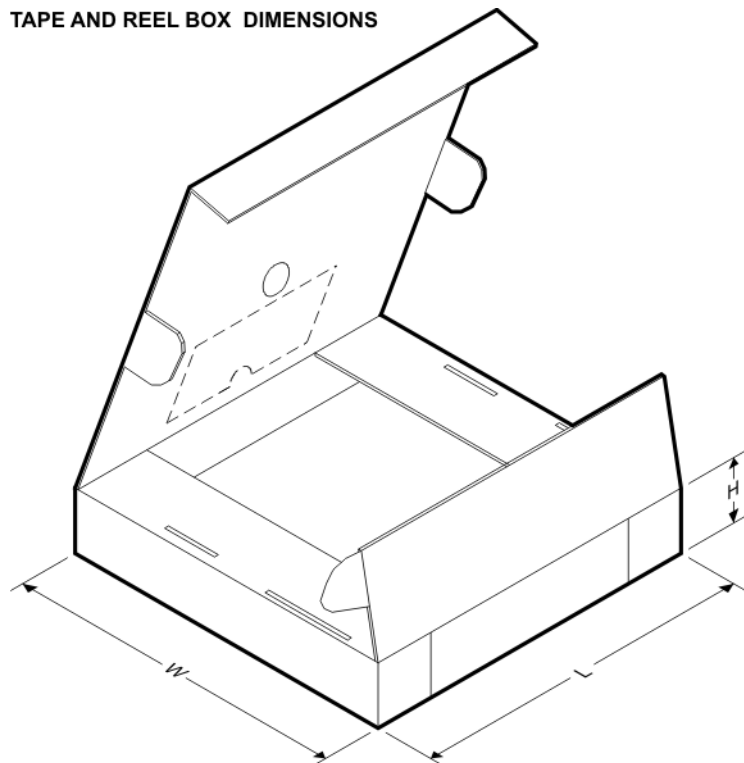
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

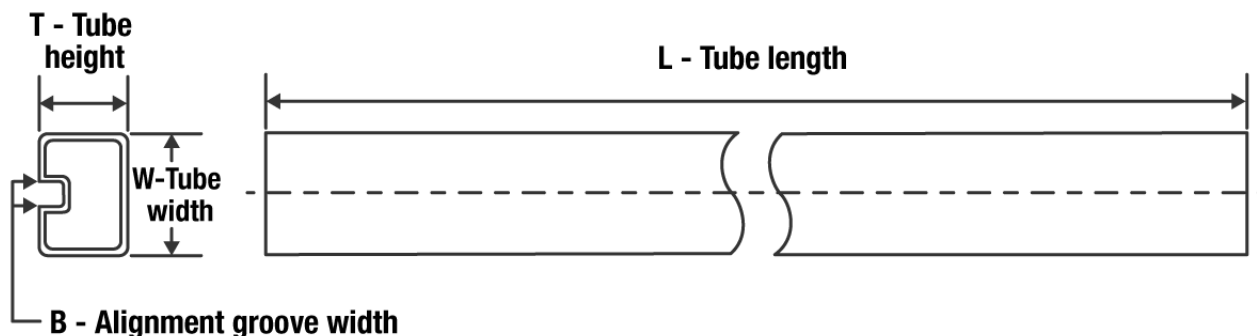
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC274ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC274ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC274AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC274AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC274BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC274BIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC274CDBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.5	12.0	16.0	Q1
TLC274CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC274CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC274CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC274CNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TLC274CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC274IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC274IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC274MDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC279CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC279IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC274ACDR	SOIC	D	14	2500	367.0	367.0	38.0
TLC274ACDR	SOIC	D	14	2500	350.0	350.0	43.0
TLC274AIDR	SOIC	D	14	2500	853.0	449.0	35.0
TLC274AIDR	SOIC	D	14	2500	350.0	350.0	43.0
TLC274BCDR	SOIC	D	14	2500	367.0	367.0	38.0
TLC274BIDR	SOIC	D	14	2500	853.0	449.0	35.0
TLC274CDBR	SSOP	DB	14	2000	853.0	449.0	35.0
TLC274CDR	SOIC	D	14	2500	350.0	350.0	43.0
TLC274CDR	SOIC	D	14	2500	853.0	449.0	35.0
TLC274CDR	SOIC	D	14	2500	340.5	336.1	32.0
TLC274CNSR	SO	NS	14	2000	853.0	449.0	35.0
TLC274CPWR	TSSOP	PW	14	2000	853.0	449.0	35.0
TLC274IDR	SOIC	D	14	2500	853.0	449.0	35.0
TLC274IPWR	TSSOP	PW	14	2000	853.0	449.0	35.0
TLC274MDRG4	SOIC	D	14	2500	350.0	350.0	43.0
TLC279CDR	SOIC	D	14	2500	350.0	350.0	43.0
TLC279IDR	SOIC	D	14	2500	350.0	350.0	43.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLC274ACD	D	SOIC	14	50	506.6	8	3940	4.32
TLC274ACD	D	SOIC	14	50	505.46	6.76	3810	4
TLC274ACN	N	PDIP	14	25	506	13.97	11230	4.32
TLC274ACNE4	N	PDIP	14	25	506	13.97	11230	4.32
TLC274AID	D	SOIC	14	50	505.46	6.76	3810	4
TLC274AID	D	SOIC	14	50	506.6	8	3940	4.32
TLC274AIN	N	PDIP	14	25	506	13.97	11230	4.32
TLC274BCD	D	SOIC	14	50	506.6	8	3940	4.32
TLC274BCD	D	SOIC	14	50	505.46	6.76	3810	4
TLC274BCDG4	D	SOIC	14	50	505.46	6.76	3810	4
TLC274BCDG4	D	SOIC	14	50	506.6	8	3940	4.32
TLC274BCN	N	PDIP	14	25	506	13.97	11230	4.32
TLC274BCNE4	N	PDIP	14	25	506	13.97	11230	4.32
TLC274BCNS	NS	SOP	14	50	530	10.5	4000	4.1
TLC274BID	D	SOIC	14	50	506.6	8	3940	4.32
TLC274BID	D	SOIC	14	50	505.46	6.76	3810	4
TLC274BIDG4	D	SOIC	14	50	506.6	8	3940	4.32
TLC274BIDG4	D	SOIC	14	50	505.46	6.76	3810	4
TLC274BIN	N	PDIP	14	25	506	13.97	11230	4.32
TLC274CD	D	SOIC	14	50	507	8	3940	4.32
TLC274CD	D	SOIC	14	50	506.6	8	3940	4.32
TLC274CD	D	SOIC	14	50	505.46	6.76	3810	4
TLC274CDB	DB	SSOP	14	80	530	10.5	4000	4.1
TLC274CDBG4	DB	SSOP	14	80	530	10.5	4000	4.1
TLC274CDG4	D	SOIC	14	50	506.6	8	3940	4.32
TLC274CDG4	D	SOIC	14	50	505.46	6.76	3810	4
TLC274CDG4	D	SOIC	14	50	507	8	3940	4.32
TLC274CN	N	PDIP	14	25	506	13.97	11230	4.32

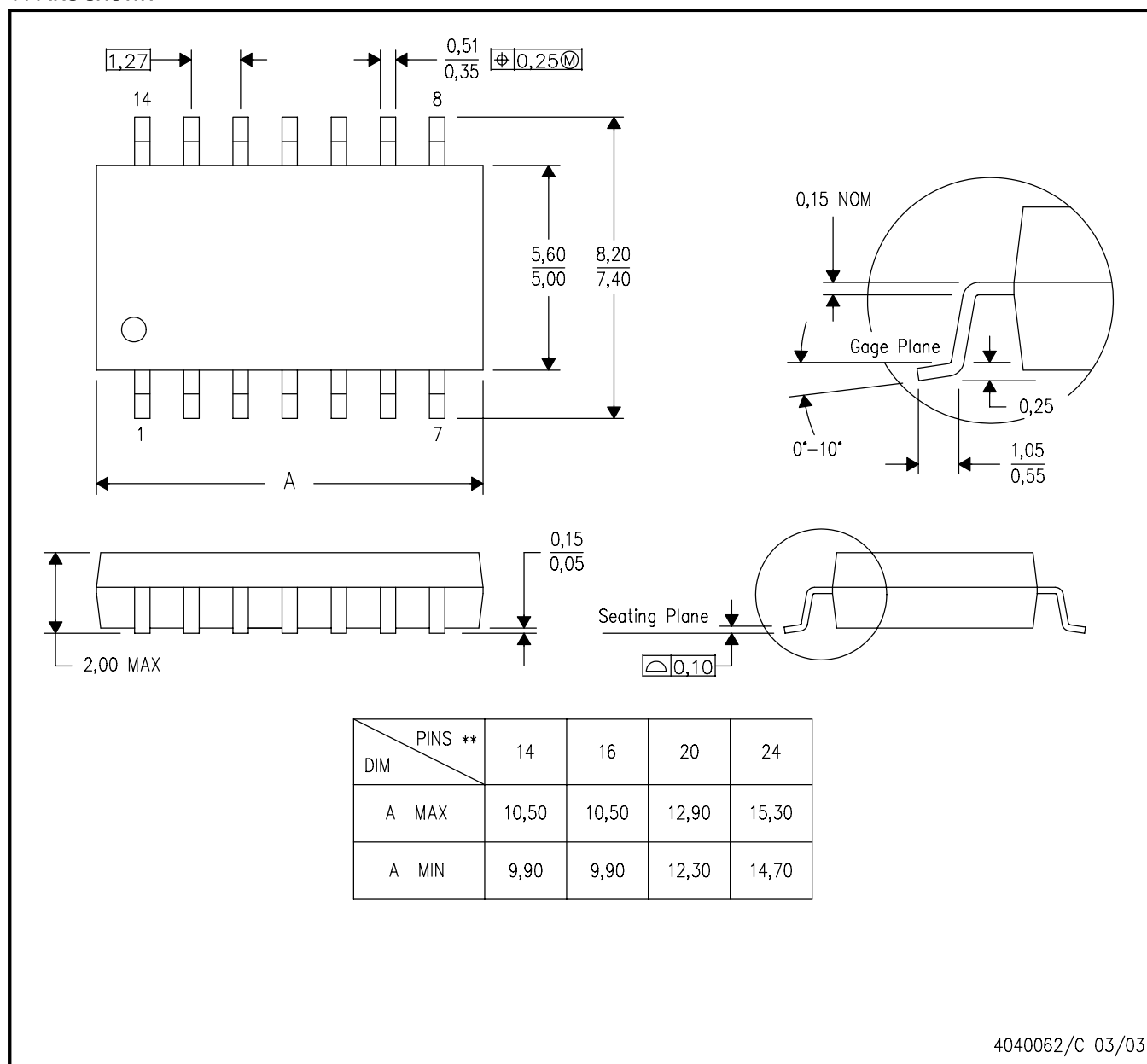
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLC274CNE4	N	PDIP	14	25	506	13.97	11230	4.32
TLC274CNS	NS	SOP	14	50	530	10.5	4000	4.1
TLC274CPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TLC274ID	D	SOIC	14	50	505.46	6.76	3810	4
TLC274ID	D	SOIC	14	50	506.6	8	3940	4.32
TLC274IDG4	D	SOIC	14	50	506.6	8	3940	4.32
TLC274IDG4	D	SOIC	14	50	505.46	6.76	3810	4
TLC274IN	N	PDIP	14	25	506	13.97	11230	4.32
TLC274INE4	N	PDIP	14	25	506	13.97	11230	4.32
TLC274IPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TLC274MD	D	SOIC	14	50	505.46	6.76	3810	4
TLC274MDG4	D	SOIC	14	50	505.46	6.76	3810	4
TLC279CD	D	SOIC	14	50	505.46	6.76	3810	4
TLC279CDG4	D	SOIC	14	50	505.46	6.76	3810	4
TLC279CN	N	PDIP	14	25	506	13.97	11230	4.32
TLC279ID	D	SOIC	14	50	505.46	6.76	3810	4
TLC279IN	N	PDIP	14	25	506	13.97	11230	4.32

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

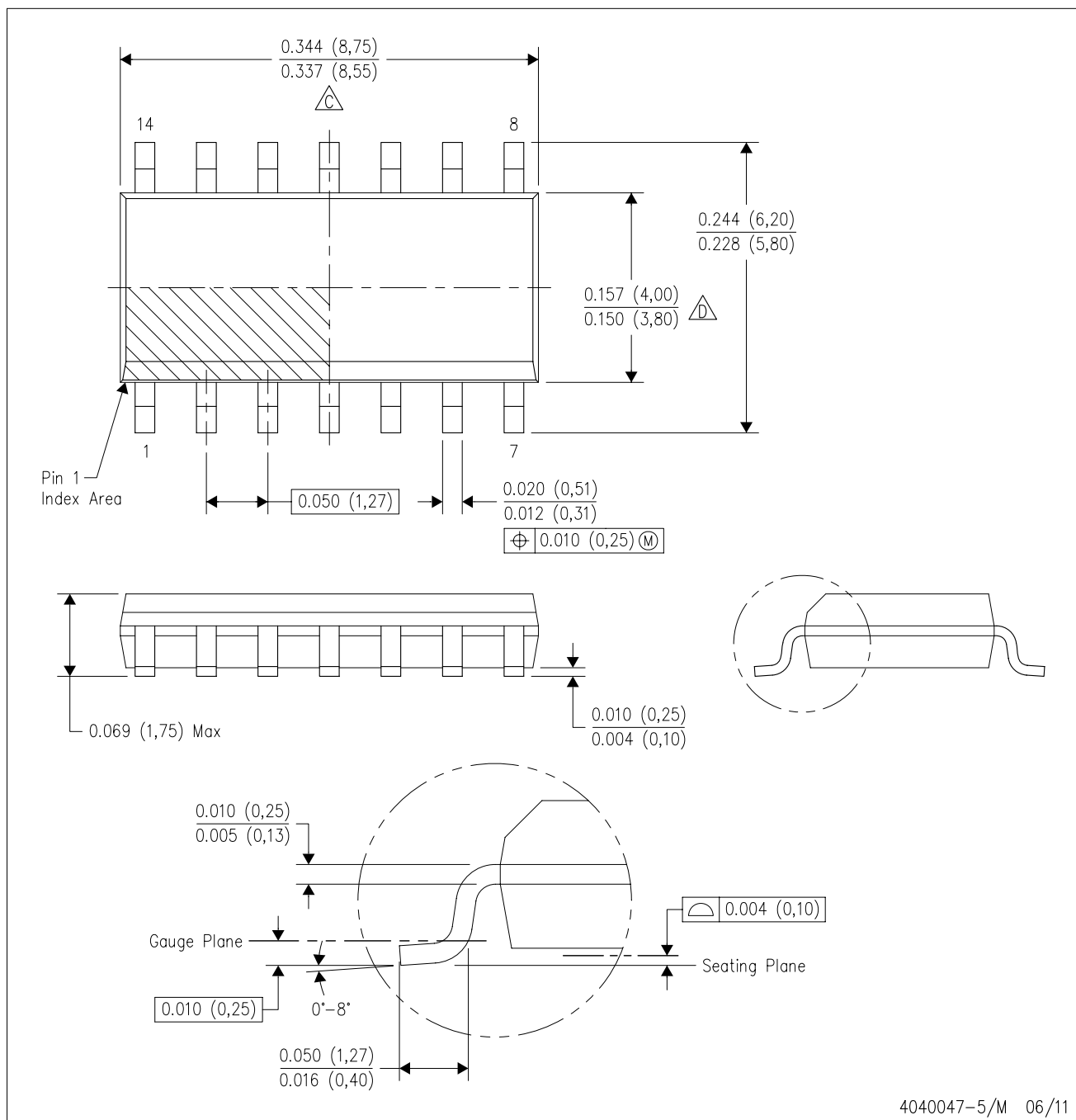
14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

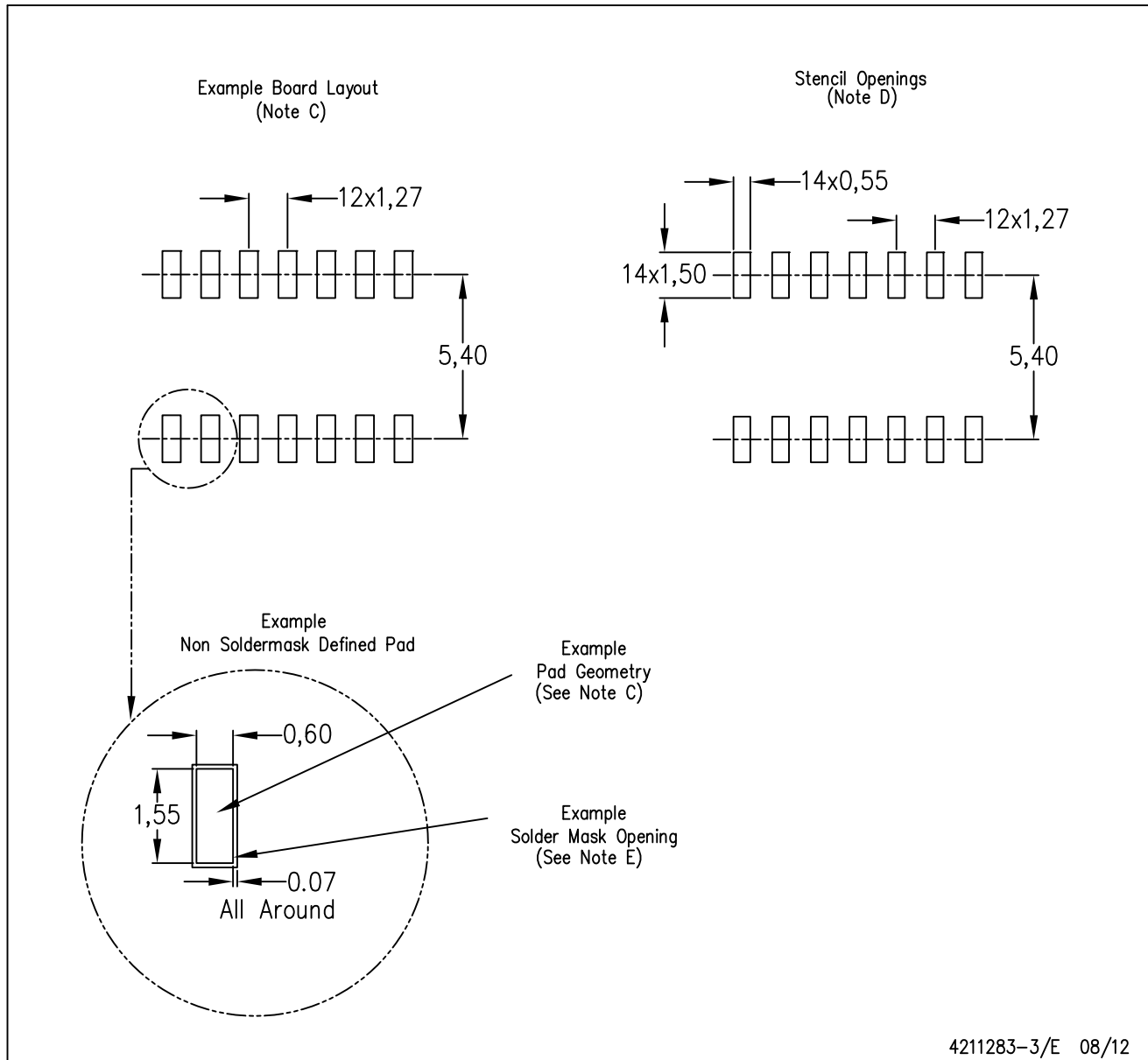


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

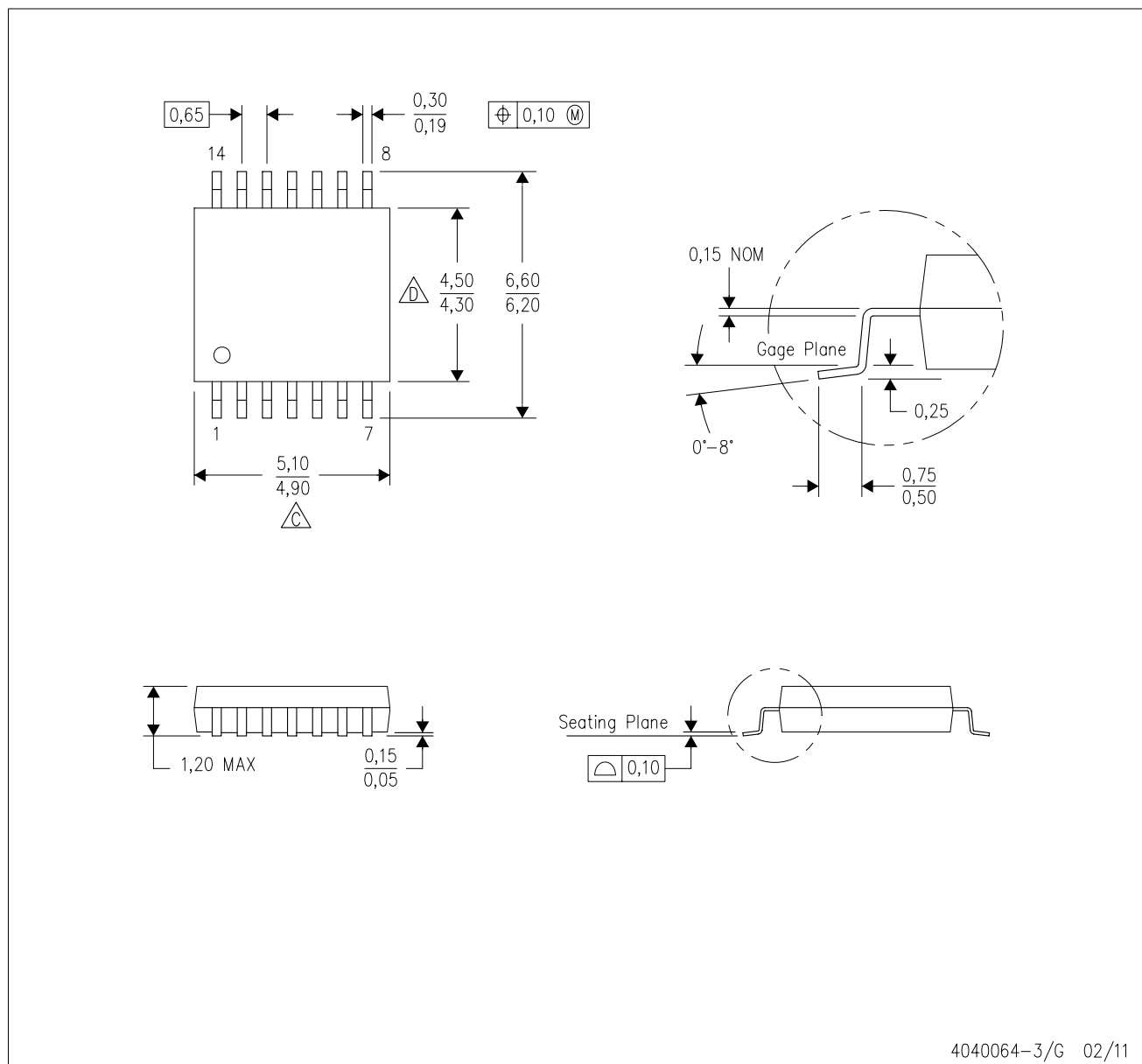
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



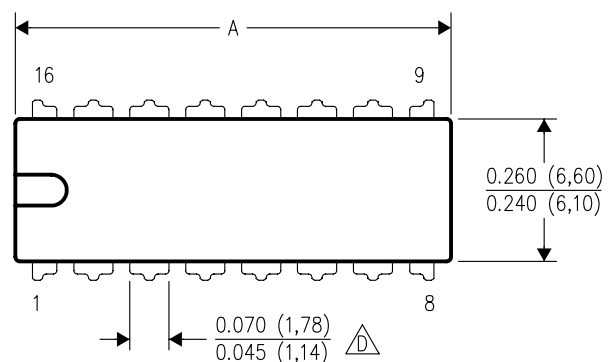
4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

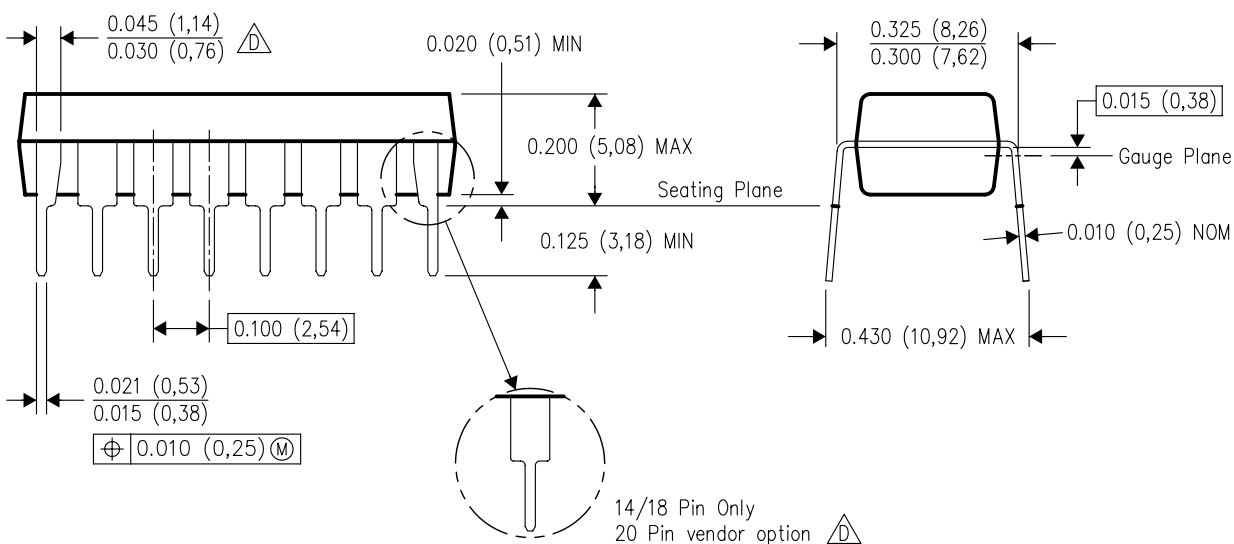
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

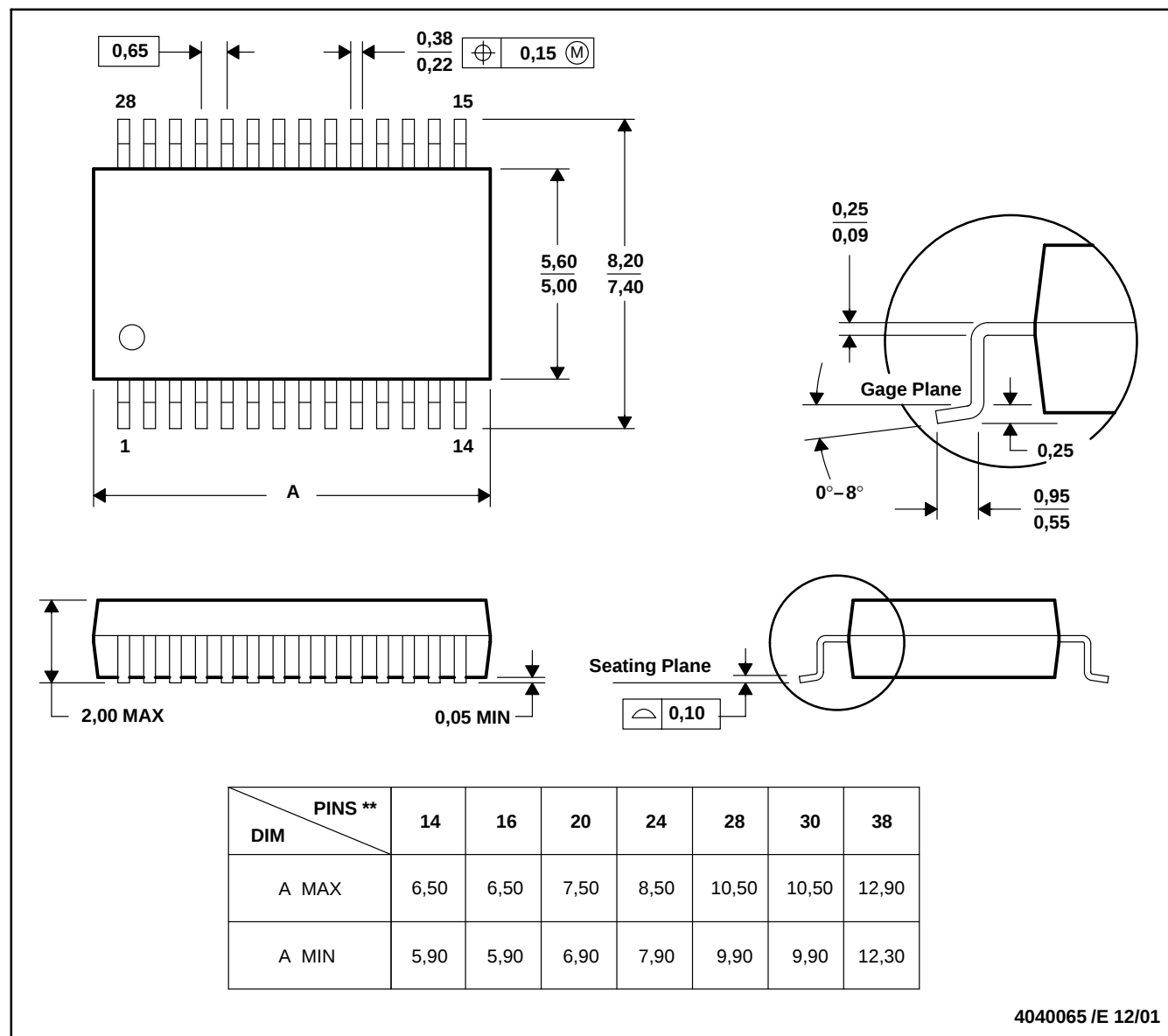
NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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