具有集成式看门狗计时器的 TPS3852-Q1 高精度电压监控器

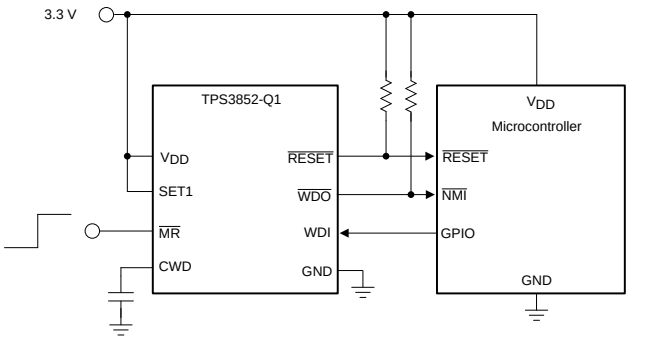
1 特性

- 具有符合 AEC-Q100 的下列结果：
  - 器件温度 1 级：-40°C 至 125°C 的环境运行温度范围
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 2
  - 器件组件充电模式 (CDM) ESD 分类等级 C4B
- V_{DD} 输入电压范围：1.6V 至 6.5V
- 0.8% 电压阈值精度
- 低电源电流：I_{DD} = 10µA（典型值）
- 用户可编程看门狗超时
- 经过出厂编程的高精度看门狗和复位定时器：
  - ±15% 精确 WDT 和 RST 延迟
- 漏极开路输出
- 手动复位输入 ($\overline{MR}$)
- 高精度电压监控：
  - 支持 1.8V 到 5.0V 常见电压轨
  - 支持 4% 和 7% 阈值
  - 0.5% 迟滞
- 看门狗禁用功能
- 采用 3mm x 3mm、8 引脚超薄小外形尺寸无引线 (VSON) 封装

2 应用

- 安全型 应用范围
- 汽车视觉系统
- 汽车高级驾驶员辅助系统 (ADAS)
- 远程信息处理控制单元
- 现场可编程门阵列 (FPGA) 和专用集成电路 (ASIC)
- 微控制器和数字信号处理器 (DSP)

典型应用电路



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3 说明

TPS3852-Q1 是一款具有集成式窗口看门狗计时器的高精度电压监控器。TPS3852-Q1 包含一个高精度欠压监控器，其在 –40°C 至 +125°C 的指定温度范围内的欠压阈值 (V_{ITN}) 精度达 0.8%。此外，TPS3852-Q1 还包含精确磁滞，是小容差系统的理想之选。监控器 $\overline{RESET}$ 延迟 具有 一个精度为 15% 的高精度延迟定时器。

TPS3852-Q1 包含可编程窗口看门狗计时器，广泛适用于各种 应用。专用的看门狗输出 ($\overline{WDO}$) 可提高分辨率，从而帮助确定出现故障情况的原因。看门狗超时可通过外部电容器或通过出厂时编制的默认延迟设置进行编程。在开发过程中，可以将看门狗禁用，从而避免出现不必要的看门狗超时。

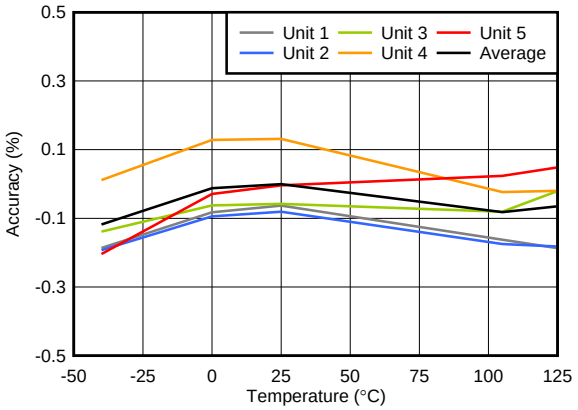
TPS3852-Q1 可提供小型 3.00mm × 3.00mm、8 引脚 VSON 封装。TPS3852-Q1 包含 可湿性侧面，可轻松进行光学检查。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS3852-Q1	VSON (8)	3.00mm x 3.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

欠压阈值 (V_{ITN}) 精度与温度间的关系



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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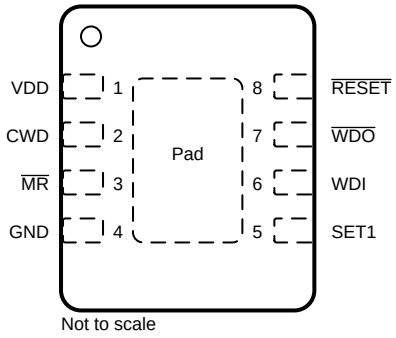
4 修订历史记录

日期	修订版本	注释
2017 年2 月	*	最初发布。

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5 Pin Configuration and Functions

DRB Package
8-Pin VSON
Top View



Not to scale

Pin Functions

NAME	NO.	I/O	DESCRIPTION
CWD	2	—	Programmable watchdog timeout input. Watchdog timeout is set by connecting a capacitor between this pin and ground. Furthermore, this pin can also be connected by a 10-kΩ resistor to VDD, or leaving unconnected (NC) further enables the selection of the preset watchdog timeouts; see the *Timing Requirements* table. When using a capacitor, the TPS3852-Q1 determines the window watchdog upper boundary with 公式 1. See 表 4 and the *CWD Functionality* section for additional information.
GND	4	—	Ground pin
$\overline{MR}$	3	I	Manual reset pin. A logical low on this pin issues a $\overline{RESET}$. This pin is internally pulled up to V_{DD}. $\overline{RESET}$ remains low for a fixed reset delay (t_{RST}) time after $\overline{MR}$ is deasserted (high).
$\overline{RESET}$	8	O	Reset output. Connect $\overline{RESET}$ using a 1-kΩ to 100-kΩ resistor to the desired pullup voltage rail (V_{PU}). $\overline{RESET}$ goes low when V_{DD} goes below the undervoltage threshold (V_{ITN}). When V_{DD} is within the normal operating range, the $\overline{RESET}$ timeout counter starts. At completion, $\overline{RESET}$ goes high. During startup, the state of $\overline{RESET}$ is undefined below the specified power-on-reset (POR) voltage (V_{POR}). Above POR, $\overline{RESET}$ goes low and remains low until the monitored voltage is within the correct operating range (above $V_{ITN} + V_{HYST}$) and the $\overline{RESET}$ timeout is complete.
SET1	5	I	Logic input. Grounding the SET1 pin disables the watchdog timer.
VDD	1	I	Supply voltage pin. For noisy systems, connecting a 0.1-µF bypass capacitor is recommended.
WDI	6	I	Watchdog input. A falling transition (edge) must occur at this pin between the lower ($t_{WDL(max)}$) and upper ($t_{WDU(min)}$) window boundaries in order for $\overline{WDO}$ to not assert. When the watchdog is not in use, the SET1 pin can be used to disable the watchdog. The input at WDI is ignored when $\overline{RESET}$ or $\overline{WDO}$ are low (asserted) and also when the watchdog is disabled. If the watchdog is disabled, then WDI cannot be left unconnected and must be driven to either VDD or GND.
$\overline{WDO}$	7	O	Watchdog output. Connect $\overline{WDO}$ with a 1-kΩ to 100-kΩ resistor to the desired pullup voltage rail (V_{PU}). $\overline{WDO}$ goes low (asserts) when a watchdog timeout occurs. $\overline{WDO}$ only asserts when $\overline{RESET}$ is high. When a watchdog timeout occurs, $\overline{WDO}$ goes low (asserts) for the set $\overline{RESET}$ timeout delay (t_{RST}). When $\overline{RESET}$ goes low, $\overline{WDO}$ is in a high-impedance state.
Thermal pad		—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range	VDD	–0.3	7	V
Output voltage range	$\overline{\text{RESET}}$, $\overline{\text{WDO}}$	–0.3	7	V
Voltage ranges	SET1, WDI, $\overline{\text{MR}}$	–0.3	7	V
	CWD, CRST	–0.3	V_{DD} + 0.3(2)	
Output pin current			±20	mA
Input current (all pins)			±20	mA
Continuous total power dissipation		See *Thermal Information*		
Temperature	Operating junction, T_J(3)	–40	150	°C
	Operating free-air, T_A(3)	–40	150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{DD} + 0.3 V or 7.0 V, whichever is smaller.
(3) Assume that $T_J = T_A$ as a result of the low dissipated power in this device.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply pin voltage	1.6		6.5	V
V_{SET1}	SET1 pin voltage	0		6.5	V
$V_{\overline{MR}}$	MR pin voltage	0		6.5	V
C_{CWD}	Watchdog timing capacitor	0.1(1)		1000(1)	nF
CWD	Pullup resistor to VDD	9	10	11	kΩ
R_{PU}	Pullup resistor, $\overline{\text{RESET}}$ and $\overline{\text{WDO}}$	1	10	100	kΩ
$I_{\overline{RESET}}$	$\overline{\text{RESET}}$ pin current			10	mA
$I_{\overline{WDO}}$	Watchdog output current			10	mA
T_J	Junction temperature	–40		125	°C

(1) Using a C_{CWD} capacitor of 0.1 nF or 1000 nF gives a $t_{WDU(typ)}$ of 62.74 ms or 77.45 seconds, respectively.

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6.4 Thermal Information

THERMAL METRIC[1]		TPS3852-Q1 DRB (VSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at $V_{ITN} + V_{HYST} \le V_{DD} \le 6.5$ V over the operating temperature range of $-40°C \le T_A, T_J \le +125°C$ (unless otherwise noted); the open-drain pullup resistors are 10 kΩ for each output; typical values are at $T_J = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL CHARACTERISTICS						
V_{DD}[1]	Supply voltage		1.6		6.5	V
I_{DD}	Supply current			10	19	µA
RESET FUNCTION						
V_{POR}[2]	Power-on-reset voltage	$I_{\overline{RESET}}$ = 15 µA, $V_{OL(MAX)}$ = 0.25 V			0.8	V
V_{UVLO}[3]	Undervoltage lockout voltage			1.35		V
V_{ITN}	Undervoltage threshold accuracy, entering $\overline{RESET}$	V_{DD} falling	V_{ITN} – 0.8%		V_{ITN} + 0.8%	
V_{HYST}	Hysteresis voltage	V_{DD} rising	0.2%	0.5%	0.8%	
$I_{\overline{MR}}$	$\overline{MR}$ pin internal pullup current	$V_{\overline{MR}}$ = 0 V	500	620	700	nA
WINDOW WATCHDOG FUNCTION						
I_{CWD}	CWD pin charge current	CWD = 0.5 V	337	375	413	nA
V_{CWD}	CWD pin threshold voltage		1.192	1.21	1.228	V
V_{OL}	$\overline{RESET}$, $\overline{WDO}$ output low	VDD = 5 V, $I_{\overline{RESET}} = I_{\overline{WDO}}$ = 3 mA			0.4	V
I_D	$\overline{RESET}$, $\overline{WDO}$ output leakage current, open-drain	VDD = $V_{ITN} + V_{HYST}$, $V_{\overline{RESET}} = V_{\overline{WDO}}$ = 6.5 V			1	µA
V_{IL}	Low-level input voltage ($\overline{MR}$, SET1)				0.25	V
V_{IH}	High-level input voltage ($\overline{MR}$, SET1)		0.8			V
$V_{IL(WDI)}$	Low-level input voltage (WDI)				0.3 × V_{DD}	V
$V_{IH(WDI)}$	High-level input voltage (WDI)		0.8 × V_{DD}			V

(1) During power on, V_{DD} must be a minimum of 1.6 V for at least 300 µs before $\overline{RESET}$ correlates with V_{DD}.
(2) When V_{DD} falls below V_{POR}, $\overline{RESET}$ and $\overline{WDO}$ are undefined.
(3) When V_{DD} falls below UVLO, $\overline{RESET}$ is driven low.

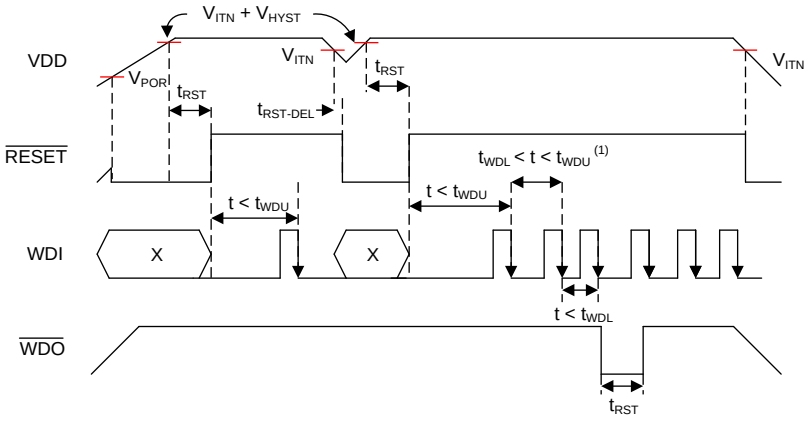
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6.6 Timing Requirements

at $V_{ITN} + V_{HYST} \le V_{DD} \le 6.5$ V over the operating temperature range of –40°C ≤ T_A, T_J ≤ +125°C (unless otherwise noted); the open-drain pullup resistors are 10 kΩ for each output; typical values are at T_J = 25°C

			MIN	TYP	MAX	UNIT
GENERAL						
t_{INIT}	CWD pin evaluation period			381		µs
	Minimum $\overline{MR}$, SET1 pin pulse duration			1		µs
	Startup delay			300		µs
RESET FUNCTION						
t_{RST}	Reset timeout period		170	200	230	ms
$t_{RST-DEL}$	V_{DD} to $\overline{RESET}$ delay	$V_{DD} = V_{ITN} + V_{HYST} + 2.5\%$		35		µs
		$V_{DD} = V_{ITN} - 2.5\%$		17		
t_{MR-DEL}	$\overline{MR}$ to $\overline{RESET}$ delay			200		ns
Watchdog Function						
t_{WDL}	Window watchdog lower boundary	CWD = NC, SET1 = 0 (1)	Watchdog disabled			
		CWD = NC, SET1 = 1 (1)	680	800	920	ms
		CWD = 10 kΩ to VDD, SET1 = 0 (1)	Watchdog disabled			
		CWD = 10 kΩ to VDD, SET1 = 1 (1)	1.48	1.85	2.22	ms
t_{WDU}	Window watchdog upper boundary	CWD = NC, SET1 = 0 (1)	Watchdog disabled			
		CWD = NC, SET1 = 1 (1)	1360	1600	1840	ms
		CWD = 10 kΩ to VDD, SET1 = 0 (1)	Watchdog disabled			
		CWD = 10 kΩ to VDD, SET1 = 1 (1)	9.35	11.0	12.65	ms
$t_{WD-setup}$	Setup time required for device to respond to changes on WDI after being enabled			150		µs
	Minimum WDI pulse duration			50		ns
t_{WD-DEL}	WDI to $\overline{WDO}$ delay			50		ns

(1) SET1 = 0 means $V_{SET1} < V_{IL}$, SET1 = 1 means $V_{SET1} > V_{IH}$.



(1) See 图 2 for WDI timing requirements.

图 1. Timing Diagram

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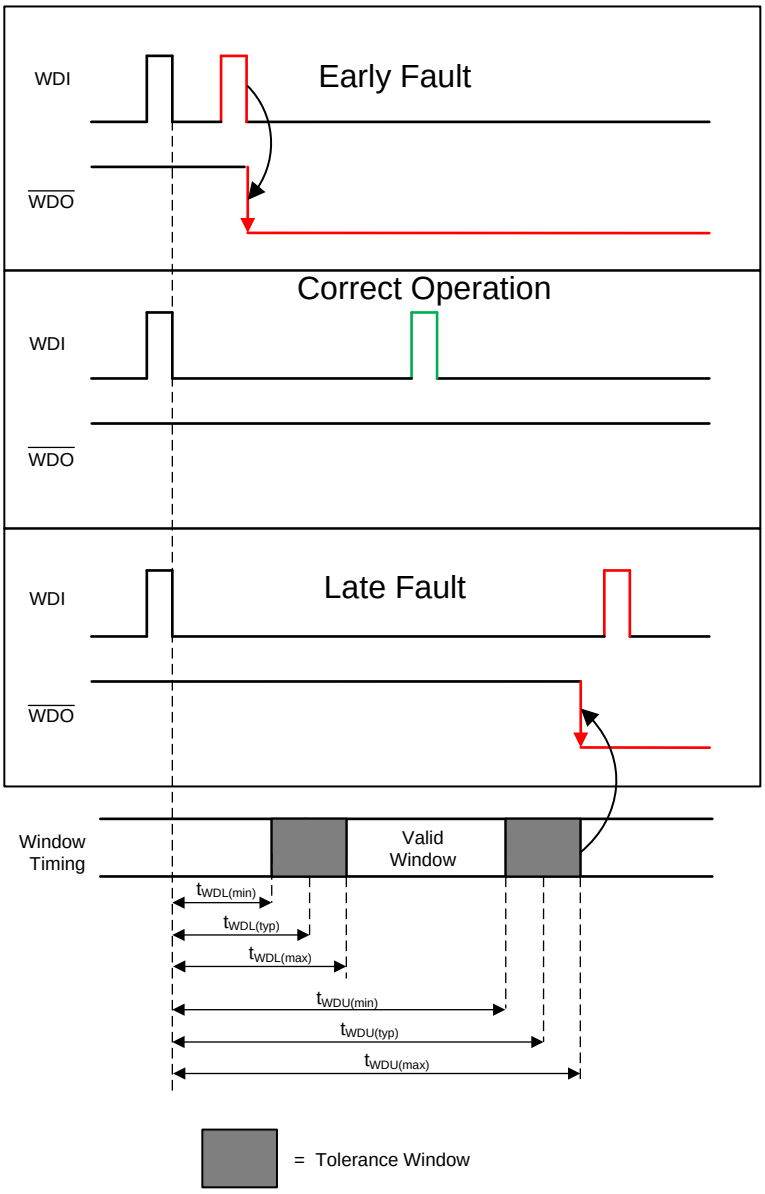


图 2. TPS3852-Q1 Window Watchdog Timing

6.7 Typical Characteristics

all curves are taken at 25°C with 1.6 V ≤ VDD ≤ 6.5 V (unless otherwise noted)

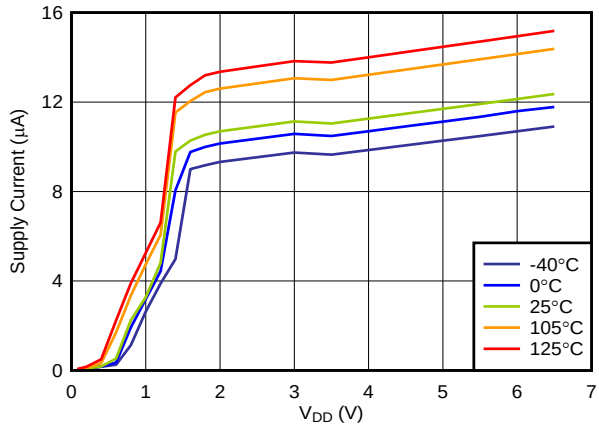
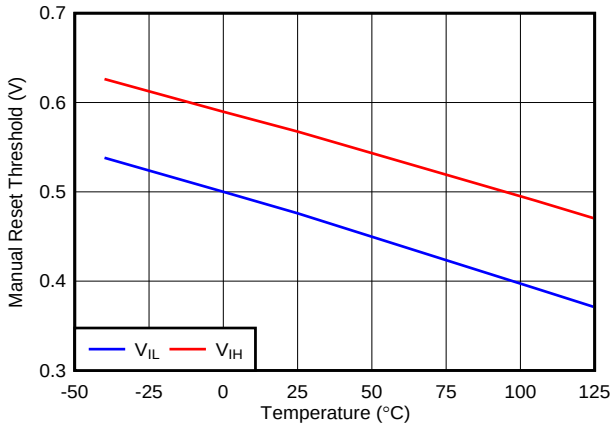


图 3. Supply Current vs V_{DD}



VDD = 1.6 V

图 4. $\overline{MR}$ Threshold vs Temperature

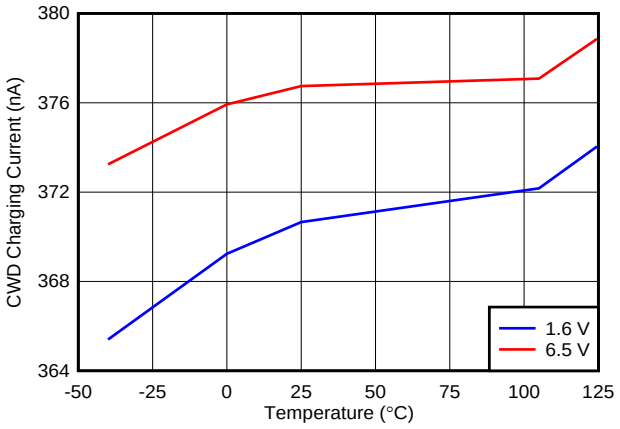
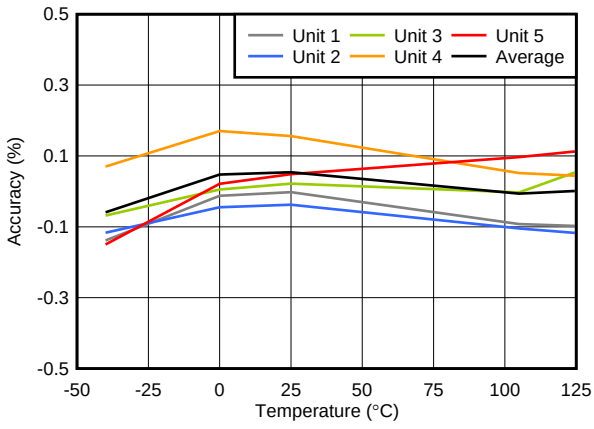
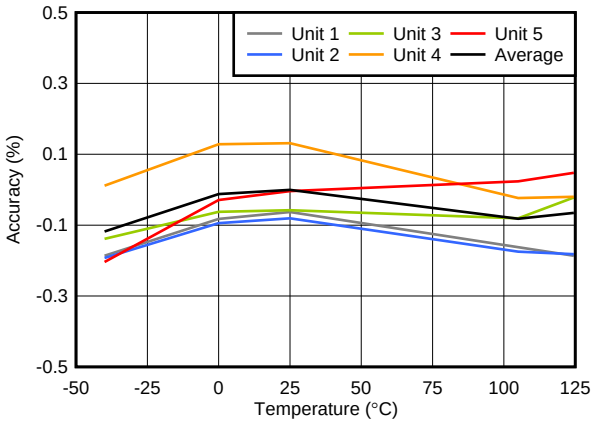


图 5. CWD Charging Current vs Temperature



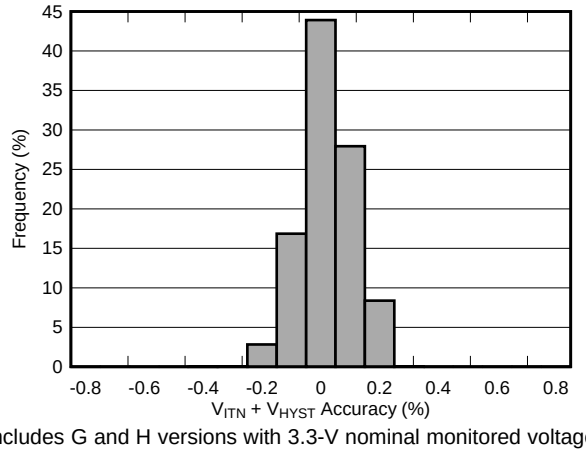
TPS3852G33-Q1

图 6. V_{ITN} + V_{HYST} Accuracy vs Temperature



TPS3852G33-Q1

图 7. V_{ITN} Accuracy vs Temperature



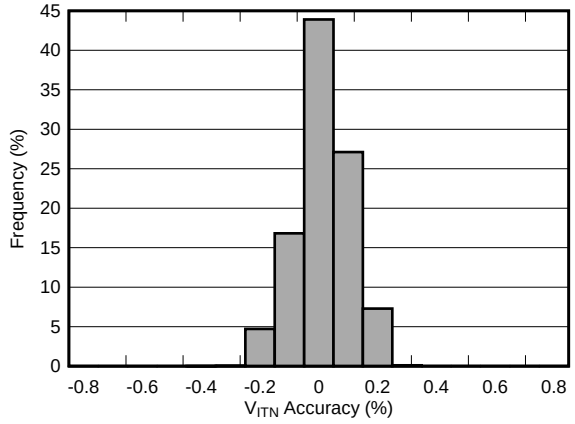
Includes G and H versions with 3.3-V nominal monitored voltage, total units = 15,536

图 8. V_{ITN} + V_{HYST} Accuracy Histogram

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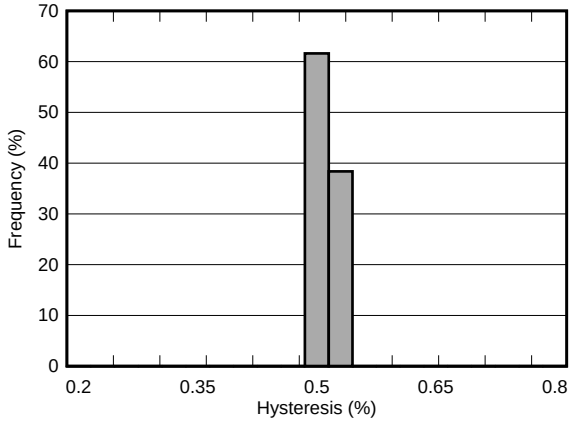
Typical Characteristics (接下页)

all curves are taken at 25°C with 1.6 V ≤ VDD ≤ 6.5 V (unless otherwise noted)



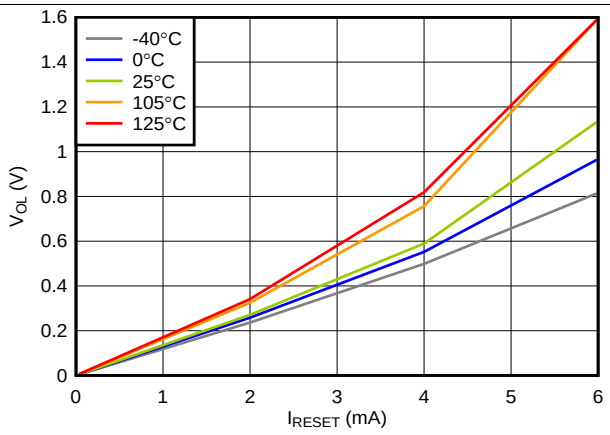
Includes G and H versions with 3.3-V nominal monitored voltage, total units = 15,536

图 9. V_{ITN} Accuracy Histogram



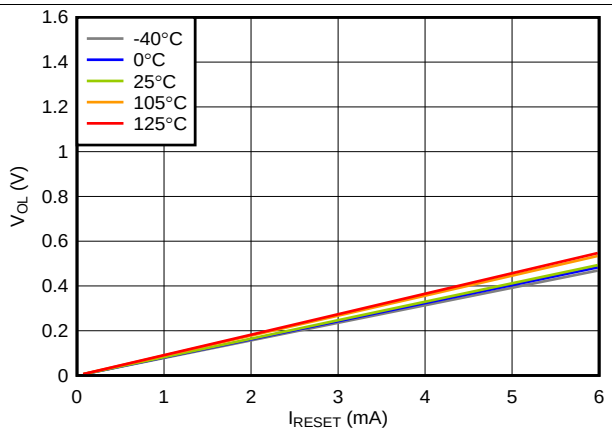
Includes G and H versions with 3.3-V nominal monitored voltage, total units = 15,536

图 10. Hysteresis Histogram



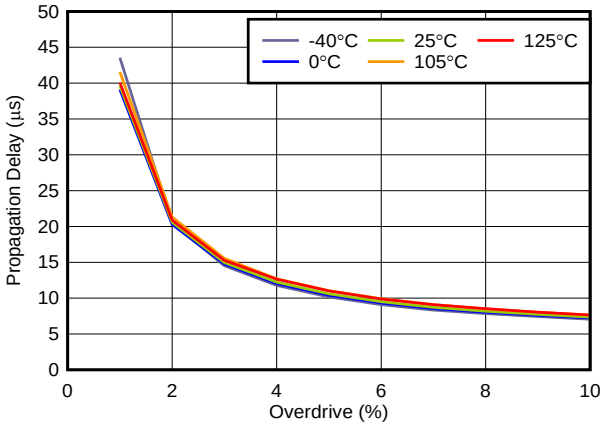
VDD = 1.6 V

图 11. Low-Level $\overline{\text{RESET}}$ Voltage vs $\overline{\text{RESET}}$ Current



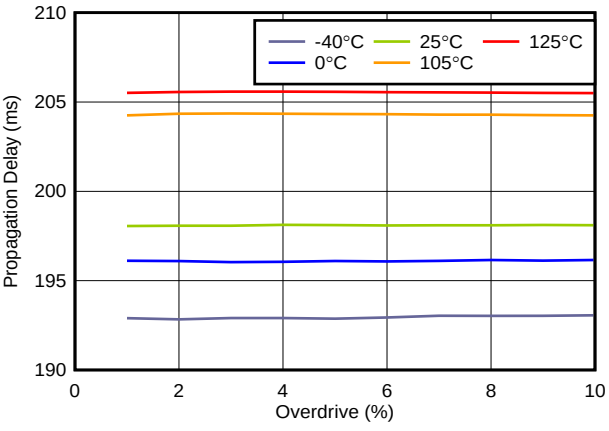
VDD = 6.5 V

图 12. Low-Level $\overline{\text{RESET}}$ Voltage vs $\overline{\text{RESET}}$ Current



TPS3852G33-Q1 entering undervoltage

图 13. Propagation Delay vs Overdrive



TPS3852G33-Q1 exiting undervoltage

图 14. Propagation Delay (t_{RST}) vs Overdrive

Typical Characteristics (接下页)

all curves are taken at 25°C with 1.6 V ≤ VDD ≤ 6.5 V (unless otherwise noted)

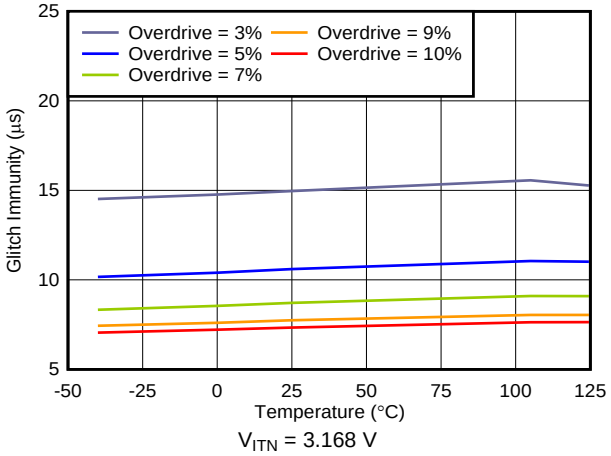


图 15. High-to-Low Glitch Immunity vs Temperature

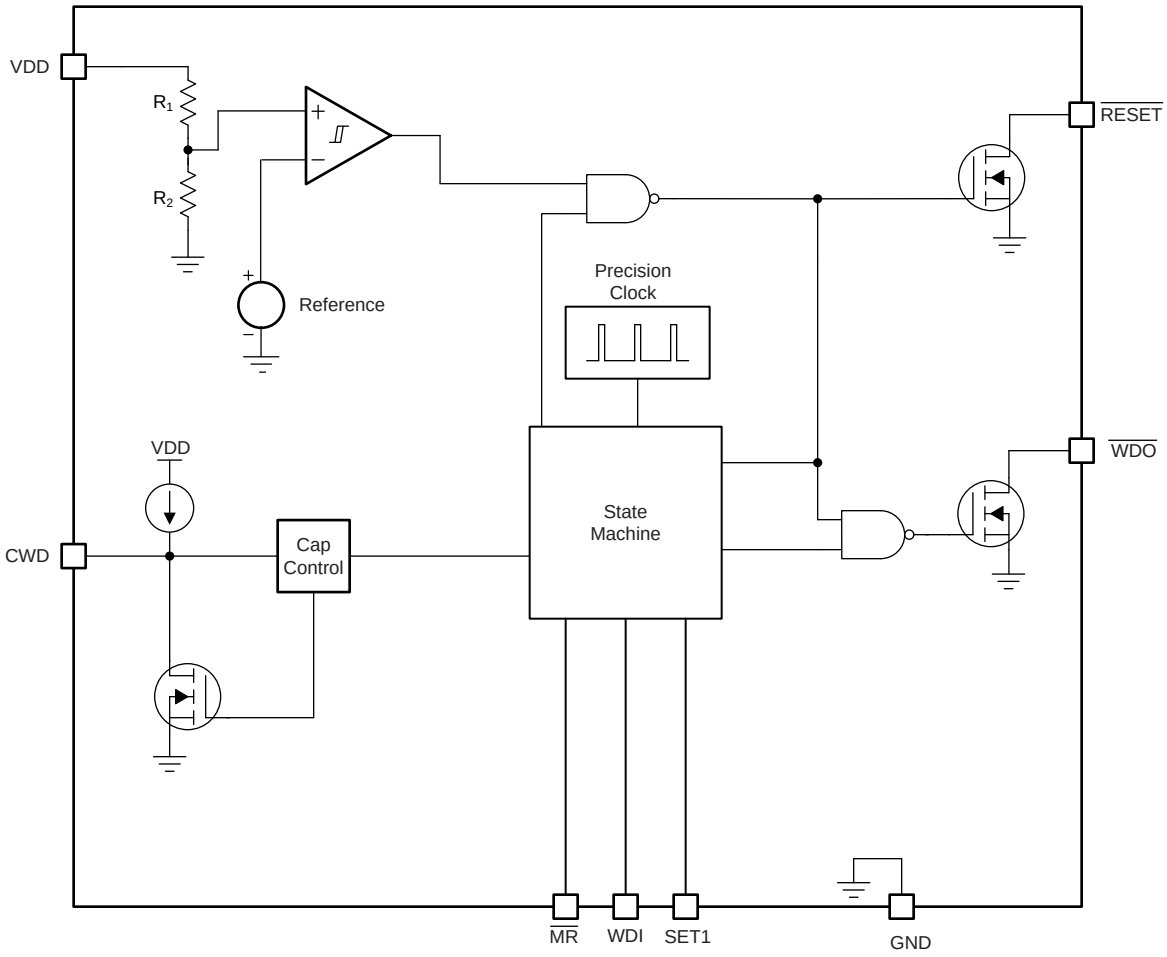
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7 Detailed Description

7.1 Overview

The TPS3852-Q1 is a high-accuracy voltage supervisor with an integrated window watchdog timer. This device includes a precision undervoltage supervisor with a threshold that achieves 0.8% accuracy over the specified temperature range of –40°C to +125°C. In addition, the TPS3852-Q1 includes accurate hysteresis on the threshold, making the device ideal for use with tight tolerance systems where voltage supervisors must ensure a $\overline{\text{RESET}}$ before the minimum supply tolerance of the microprocessor or system-on-a-chip (SoC) is reached.

7.2 Functional Block Diagram



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NOTE: $R_1 + R_2 = 4.5\ M\Omega$.

7.3 Feature Description

7.3.1 $\overline{\text{RESET}}$

Connect $\overline{\text{RESET}}$ to V_{PU} through a 1-kΩ to 100-kΩ pullup resistor. $\overline{\text{RESET}}$ remains high (deasserted) when V_{DD} is greater than the negative threshold voltage (V_{ITN}). If V_{DD} falls below the negative threshold (V_{ITN}), then $\overline{\text{RESET}}$ is asserted, driving the $\overline{\text{RESET}}$ pin to low impedance. When V_{DD} rises above V_{ITN} + V_{HYST}, a delay circuit is enabled that holds $\overline{\text{RESET}}$ low for a specified reset delay period (t_{RST}). When the reset delay has elapsed, the $\overline{\text{RESET}}$ pin goes to a high-impedance state and uses a pullup resistor to hold $\overline{\text{RESET}}$ high. The pullup resistor must be connected to the desired voltage rail to allow other devices to be connected at the correct interface voltage. To ensure proper voltage levels, give some consideration when choosing the pullup resistor values. The pullup resistor value is determined by output logic low voltage (V_{OL}), leakage current (I_D), and the current through the $\overline{\text{RESET}}$ pin $I_{\overline{\text{RESET}}}$.

7.3.2 Manual Reset ($\overline{\text{MR}}$)

The manual reset ($\overline{\text{MR}}$) input allows a processor or other logic circuits to initiate a reset. A logic low on $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to assert. After $\overline{\text{MR}}$ returns to a logic high and V_{DD} is above V_{ITN} + V_{HYST}, $\overline{\text{RESET}}$ is deasserted after the reset delay time (t_{RST}). If $\overline{\text{MR}}$ is not controlled externally, then $\overline{\text{MR}}$ can either be connected to V_{DD} or left floating because the $\overline{\text{MR}}$ pin is internally pulled up. When $\overline{\text{MR}}$ is asserted, the watchdog is disabled and all signals input to WDI are ignored.

7.3.3 Undervoltage Fault Detection

The TPS3852-Q1 features undervoltage detection for common rails between 1.8 V and 5 V. The voltage is monitored on the input rail of the device. If V_{DD} drops below V_{ITN}, then $\overline{\text{RESET}}$ is asserted (driven low). When V_{DD} is above V_{ITN} + V_{HYST}, $\overline{\text{RESET}}$ deasserts after t_{RST}, as shown in 图 16. The internal comparator has built-in hysteresis that provides some noise immunity and ensures stable operation. Although not required in most cases, for noisy applications, good analog design practice is to place a 1-nF to 100-nF bypass capacitor close to the VDD pin to reduce sensitivity to transient voltages on the monitored signal.

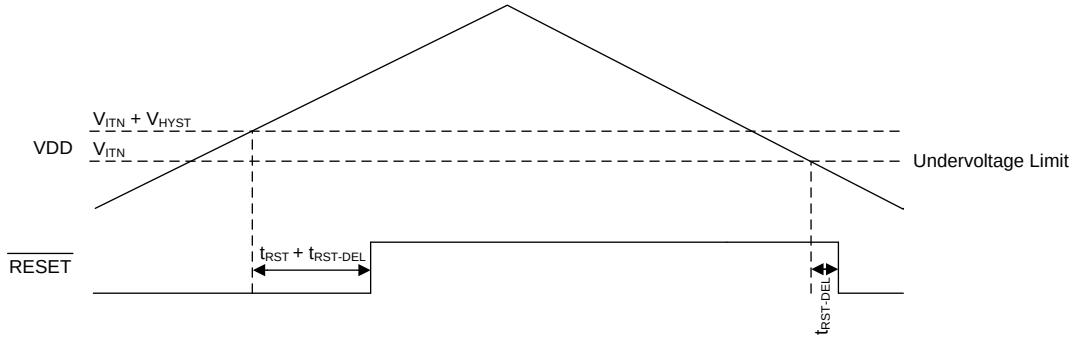


图 16. Undervoltage Detection

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Feature Description (接下页)

7.3.4 Watchdog Mode

This section provides information for the watchdog mode of operation.

7.3.4.1 SET1

The SET1 pin can enable and disable the watchdog timer. If SET1 is set to GND, the watchdog timer is disabled and WDI is ignored. When the watchdog is disabled, $\overline{WDO}$ is in a high-impedance state. If the watchdog timer is disabled, drive the WDI pin to either GND or VDD to ensure that there is no increase in I_{DD}. When SET1 is logic high, the watchdog operates normally. The SET1 pin can be changed dynamically; however, if the watchdog is going from disabled to enabled there is a setup time $t_{WD\text{-}setup}$ where the watchdog does not respond to changes on WDI, as shown in 图 17.

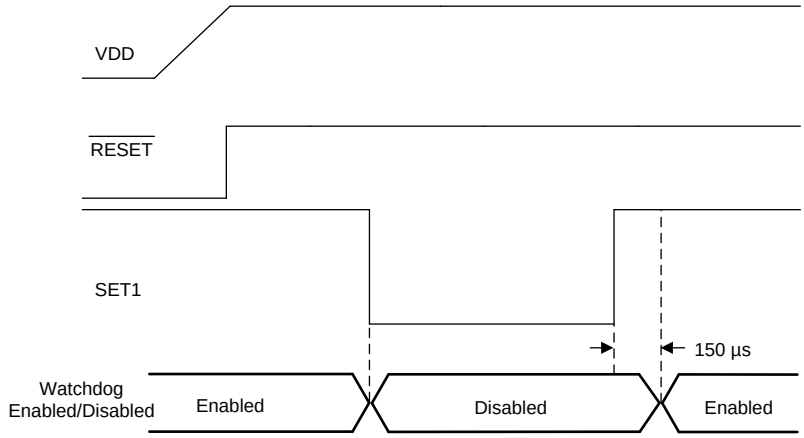


图 17. Enabling and Disabling the Watchdog

7.3.4.2 Window Watchdog Timer

This section provides information for the window watchdog mode of operation. A window watchdog is typically employed in safety-critical applications where a traditional watchdog timer is inadequate. In a traditional watchdog there is a maximum time in which a pulse must be issued to prevent the reset from occurring. In a window watchdog, the pulse must be issued between a maximum lower window time ($t_{WDL(max)}$) and the minimum upper window time ($t_{WDU(min)}$) set by the CWD pin.

7.3.4.3 Watchdog Input (WDI)

WDI is the watchdog timer input that controls the $\overline{WDO}$ output. The WDI input is triggered by the falling edge of the input signal. For the first pulse, the watchdog acts as a traditional watchdog timer; thus, the first pulse must be issued before $t_{WDU(min)}$. After the first pulse, to ensure proper functionality of the watchdog timer, always issue the WDI pulse within the window of $t_{WDL(max)}$ and $t_{WDU(min)}$. If the pulse is issued in this region, then $\overline{WDO}$ remains unasserted. Otherwise the device asserts $\overline{WDO}$, putting the $\overline{WDO}$ pin into a low-impedance state.

The watchdog input (WDI) is a digital pin. In order to ensure there is no increase in I_{DD}, drive the WDI pin to either VDD or GND at all times. Putting the pin to an intermediate voltage can cause an increase in supply current (I_{DD}) because of the architecture of the digital logic gates. When $\overline{RESET}$ is asserted, the watchdog is disabled and all signals input to WDI are ignored. When $\overline{RESET}$ is no longer asserted, the device resumes normal operation and no longer ignores the signal on WDI. If the watchdog is disabled, drive the WDI pin to either VDD or GND.

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Feature Description (接下页)

7.3.4.4 CWD

The CWD pin provides the functionality of both high-precision, factory-programmed window watchdog timing options and user-programmable window watchdog timing. The CWD pin can be either pulled up to V_{DD} through a resistor, have an external capacitor to ground, or be left floating. Every time that the device issues a reset event and the supply voltage is above V_{ITN}, the device tries to determine which of these three options is connected to the pin. There is an internal state machine that the device goes through to determine which option is connected to the CWD pin. The state machine can take up to 381 μs to determine if the CWD pin is left floating, pulled-up through a resistor, or connected to a capacitor.

If the CWD pin is being pulled up to V_{DD} using a pullup resistor, then use a 10-kΩ resistor.

7.3.4.5 Watchdog Output ($\overline{WDO}$)

The TPS3852-Q1 features a window watchdog with an independent watchdog output ($\overline{WDO}$). The independent watchdog output gives the flexibility to flag when there is a fault in the watchdog timing without performing an entire system reset. For legacy applications, $\overline{WDO}$ can be tied to $\overline{RESET}$. When the $\overline{RESET}$ output is not asserted, the $\overline{WDO}$ signal maintains normal operation. However, when the $\overline{RESET}$ signal is asserted, the $\overline{WDO}$ pin goes to a high-impedance state. This is due to using the standard $\overline{RESET}$ timing options when a fault occurs on $\overline{WDO}$. When $\overline{RESET}$ is unasserted, the window watchdog timer resumes normal operation.

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7.4 Device Functional Modes

表 1 summarises the functional modes of the TPS3852-Q1.

表 1. Device Functional Modes

V_{DD}	WDI	$\overline{WDO}$	$\overline{RESET}$
$V_{DD} < V_{POR}$	—	—	Undefined
$V_{POR} \le V_{DD} < V_{DD(min)}$	Ignored	High	Low
$V_{DD(min)} \le V_{DD} \le V_{ITN} + V_{HYST}$ (1)	Ignored	High	Low
$V_{DD} > V_{ITN}$ (2)	$t_{WDL(max)} < t_{PULSE} < t_{WDU(min)}$ (3)	High	High
	$t_{PULSE} > t_{WDU(min)}$ (3)	Low	High
	$t_{PULSE} < t_{WDL(max)}$ (3)	Low	High

(1) Only valid before V_{DD} goes above $V_{ITN} + V_{HYST}$.
(2) Only valid after V_{DD} goes above $V_{ITN} + V_{HYST}$.
(3) Where t_{PULSE} is the time between the falling edges on WDI.

7.4.1 V_{DD} is Below V_{POR} ($V_{DD} < V_{POR}$)

When V_{DD} is less than V_{POR}, $\overline{RESET}$ is undefined and can be either high or low. The state of $\overline{RESET}$ largely depends on the load that the $\overline{RESET}$ pin is experiencing.

7.4.2 Above Power-On-Reset, But Less Than $V_{DD(min)}$ ($V_{POR} \le V_{DD} < V_{DD(min)}$)

When the voltage on V_{DD} is less than $V_{DD(min)}$ and greater than or equal to V_{POR}, the $\overline{RESET}$ signal is asserted (logic low). When $\overline{RESET}$ is asserted, the watchdog output $\overline{WDO}$ is in a high-impedance state regardless of the WDI signal that is input to the device.

7.4.3 Normal Operation ($V_{DD} \ge V_{DD(min)}$)

When V_{DD} is greater than or equal to $V_{DD(min)}$, the $\overline{RESET}$ signal is determined by V_{DD}. When $\overline{RESET}$ is asserted, $\overline{WDO}$ goes to a high-impedance state. $\overline{WDO}$ is then pulled high through the pullup resistor.

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8 Application and Implementation

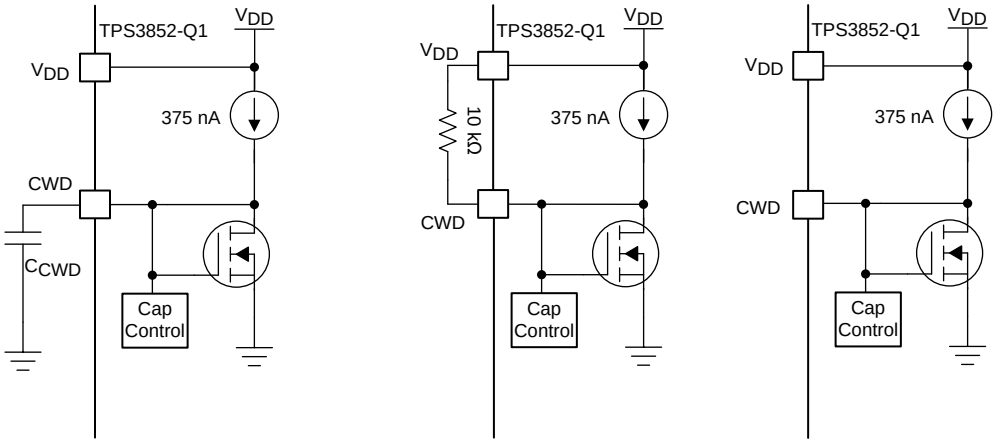
注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 CWD Functionality

The TPS3852-Q1 features three options for setting the watchdog window: connecting a capacitor to the CWD pin, connecting a pullup resistor to VDD, and leaving the CWD pin unconnected. 图 18 shows a schematic drawing of all three options. If this pin is connected to VDD through a 10-kΩ pullup resistor or left unconnected (high impedance), then the factory-programmed watchdog timeouts are enabled; see the *Timing Requirements* table. Otherwise, the watchdog timeout can be adjusted by placing a capacitor from the CWD pin to ground.



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图 18. CWD Charging Circuit

8.1.1.1 Factory-Programmed Timing Options

If using the factory-programmed timing options (listed in 表 2), the CWD pin must either be unconnected or pulled up to VDD through a 10-kΩ pullup resistor. Using these options enables high-precision watchdog timing.

表 2. Factory-Programmed Watchdog Timing

INPUT		WATCHDOG LOWER BOUNDARY (t_{WDL})			WATCHDOG UPPER BOUNDARY (t_{WDU})			UNIT
CWD	SET1	MIN	TYP	MAX	MIN	TYP	MAX	
NC	0	Watchdog disabled			Watchdog disabled			
	1	680	800	920	1360	1600	1840	ms
10 kΩ to VDD	0	Watchdog disabled			Watchdog disabled			
	1	1.48	1.85	2.22	9.35	11.0	12.65	ms

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8.1.1.2 Adjustable Capacitor Timing

Adjustable capacitor timing is achievable by connecting a capacitor to the CWD pin. If a capacitor is connected to CWD, then a 375-nA current source charges C_{CWD} until V_{CWD} = 1.21 V. The TPS3852-Q1 determines the window watchdog upper boundary with the formula given in 公式 1, where C_{CWD} is in microfarads (µF) and t_{WDU} is in seconds.

$$t_{WDU(typ)}(s) = 77.4 \times C_{CWD}(\mu F) + 0.055\ (s) \quad (1)$$

The TPS3852-Q1 is limited to using C_{CWD} capacitors between 100 pF and 1 µF. Note that 公式 1 is for ideal capacitors; capacitor tolerances cause the actual device timing to vary. For the most accurate timing, use ceramic capacitors with COG dielectric material. As shown in 表 3, when using the minimum capacitance of 100 pF, the watchdog upper boundary is 62.74 ms; whereas with a 1-µF capacitance, the watchdog upper boundary is 77.455 seconds. If a C_{CWD} capacitor is used, 公式 1 can be used to set the window watchdog upper boundary (t_{WDU}). 表 4 shows how t_{WDU} can be used to calculate t_{WDL}.

表 3. t_{WDU} Values for Common Ideal Capacitor Values

C_{CWD}	WATCHDOG UPPER BOUNDARY (t_{WDU})			UNIT
	MIN(1)	TYP	MAX(1)	
100 pF	53.32	62.74	72.15	ms
1 nF	112.5	132.4	152.2	ms
10 nF	704	829	953	ms
100 nF	6625	7795	8964	ms
1 µF	65836	77455	89073	ms

(1) Minimum and maximum values are calculated using ideal capacitors.

表 4. Programmable CWD Timing

INPUT		WATCHDOG LOWER BOUNDARY (t_{WDL})			WATCHDOG UPPER BOUNDARY (t_{WDU})			UNIT
CWD	SET1	MIN	TYP	MAX	MIN	TYP	MAX	
C_{CWD}	0	Watchdog disabled			Watchdog disabled			
	1	$t_{WDU(min)}$ x 0.5	t_{WDU} x 0.5	$t_{WDU(max)}$ x 0.5	0.85 x $t_{WDU(typ)}$	$t_{WDU(typ)}$(1)	1.15 x $t_{WDU(typ)}$	s

(1) Calculated from 公式 1 using ideal capacitors.

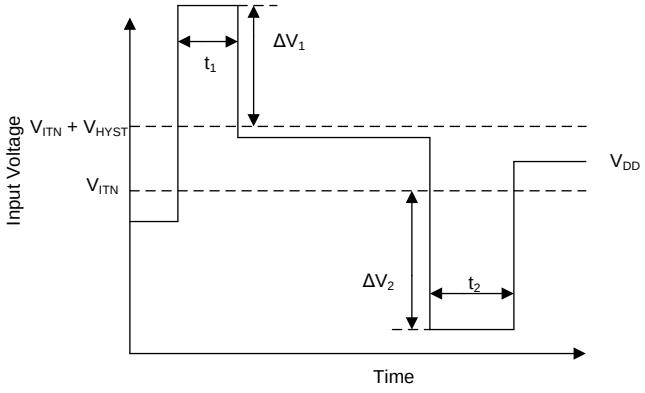
8.1.2 Overdrive Voltage

Forcing a $\overline{\text{RESET}}$ is dependent on two conditions: the amplitude V_{DD} is beyond the trip point (ΔV_1 and ΔV_2), and the length of time that the voltage is beyond the trip point (t_1 and t_2). If the voltage is just under the trip point for a long period of time, $\overline{\text{RESET}}$ asserts and the output is pulled low. However, if V_{DD} is just under the trip point for a few nanoseconds, $\overline{\text{RESET}}$ does not assert and the output remains high. The length of time required for $\overline{\text{RESET}}$ to assert can be changed by increasing the amount V_{DD} goes under the trip point. If V_{DD} is under the trip point by 10%, the amount of time required for the comparator to respond is much faster and causes $\overline{\text{RESET}}$ to assert much quicker than when barely under the trip point voltage. 公式 2 shows how to calculate the percentage overdrive.

$$\text{Overdrive} = |(V_{DD} / V_{ITX} - 1) \times 100\% | \quad (2)$$

In 公式 2, V_{ITX} corresponds to the threshold trip point. If V_{DD} is exceeding the positive threshold, $V_{ITN} + V_{HYST}$ is used. V_{ITN} is used when V_{DD} is falling below the negative threshold. In 图 19, t_1 and t_2 correspond to the amount of time that V_{DD} is over the threshold; the propagation delay versus overdrive for V_{ITN} and $V_{ITN} + V_{HYST}$ is illustrated in 图 13 and 图 14, respectively.

The TPS3852-Q1 is relatively immune to short positive and negative transients on VDD because of the overdrive voltage.



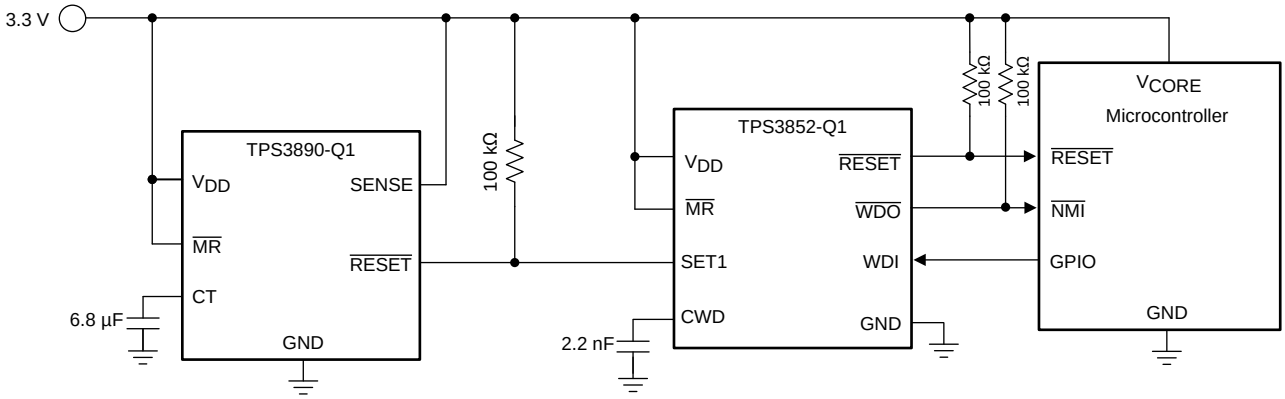
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图 19. Overdrive Voltage

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8.2 Typical Application

A typical application for the TPS3852-Q1 is shown in 图 20. The TPS3852G33-Q1 is used to monitor the 3.3-V, V_{CORE} rail powering the microcontroller.



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图 20. Monitoring Supply Voltage and Watchdog Supervision of a Microcontroller

8.2.1 Design Requirements

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Watchdog disable for initialization period	Watchdog must remain disabled for 7 seconds until logic enables the watchdog timer	7.21 seconds (typ)
Output logic voltage	3.3-V CMOS	3.3-V CMOS
Monitored rail	3.3 V with a 5% threshold	Worst-case V_{ITN} = 3.142 V (–4.7% threshold)
Watchdog window	250 ms, maximum	$t_{WDL(max)}$ = 135 ms, $t_{WDU(min)}$ = 181 ms
Maximum device current consumption	50 µA	52 µA (worst-case) when $\overline{RESET}$ or $\overline{WDO}$ is asserted(1)

(1) Only includes the TPS3852G33-Q1 current consumption.

8.2.2 Detailed Design Procedure

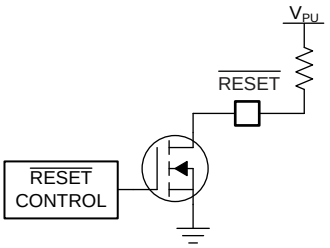
8.2.2.1 Monitoring the 3.3-V Rail

This application calls for very tight monitoring of the rail with only 5% of variation allowed on the rail. To ensure this requirement is met, the TPS3852G33-Q1 was chosen for its –4% threshold. To calculate the worst-case for V_{ITN}, the accuracy must also be taken into account. The worst-case for V_{ITN} can be calculated by 公式 3:

$$V_{ITN(Worst\text{-}Case)} = V_{ITN(typ)} \times 0.992 = 3.3 \times 0.96 \times 0.992 = 3.142\ V \quad (3)$$

8.2.2.2 Calculating $\overline{\text{RESET}}$ and the $\overline{\text{WDO}}$ Pullup Resistor

The TPS3852-Q1 uses an open-drain configuration for the $\overline{\text{RESET}}$ circuit, as shown in 图 21. When the FET is off, the resistor pulls the drain of the transistor to VDD and when the FET is turned on, the FET attempts to pull the drain to ground, thus creating an effective resistor divider. The resistors in this divider must be chosen to ensure that V_{OL} is below the maximum value. To choose the proper pullup resistor, there are three key specifications to keep in mind: the pullup voltage (V_{PU}), the recommended maximum $\overline{\text{RESET}}$ pin current ($I_{\overline{\text{RESET}}}$), and V_{OL}. The maximum V_{OL} is 0.4 V, meaning that the effective resistor divider created must be able to bring the voltage on the reset pin below 0.4 V with $I_{\overline{\text{RESET}}}$ kept below 10 mA. For this example, with a V_{PU} of 3.3 V, a resistor must be chosen to keep $I_{\overline{\text{RESET}}}$ below 50 μA because this value is the maximum consumption current allowed. To ensure this specification is met, a pullup resistor value of 100 kΩ was selected, which sinks a maximum of 33 μA when $\overline{\text{RESET}}$ or $\overline{\text{WDO}}$ is asserted. As illustrated in 图 11, when the $\overline{\text{RESET}}$ current is at 33 μA the low-level output voltage is approximately zero.



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图 21. $\overline{\text{RESET}}$ Open-Drain Configuration

8.2.2.3 Setting the Window Watchdog

As illustrated in 图 18, there are three options for setting the window watchdog. The design specifications in this application require the programmable timing option (external capacitor connected to CWD). When a capacitor is connected to the CWD pin, the window is governed by 公式 4. 公式 4 is only valid for ideal capacitors, any temperature or voltage derating must be accounted for separately.

$$C_{CWD}\left(\mu F\right) = \frac{t_{WDU} - 0.055}{77.4} = \frac{0.25 - 0.055}{77.4} = 0.0025\ \mu F \tag{4}$$

The nearest standard capacitor value to 2.5 nF is 2.2 nF. Selecting 2.2 nF for the C_{CWD} capacitor gives the following minimum and maximum timing parameters:

$$t_{WDU(MIN)} = 0.85 \times t_{WDU(TYP)} = 0.85 \times \left(77.4 \times 2.2 \times 10^{-3} + 0.055\right) = 191\ ms \tag{5}$$

$$t_{WDL(MAX)} = 0.5 \times t_{WDU(MAX)} = 0.5 \times \left[1.15 \times \left(77.4 \times 2.2 \times 10^{-3} + 0.055\right)\right] = 129\ ms \tag{6}$$

Capacitor tolerance also influence $t_{WDU(MIN)}$ and $t_{WDL(MAX)}$. Select a ceramic COG dielectric capacitor for high accuracy. For 2.2 nF, COG capacitors are readily available with a 5% tolerance, which results in a 5% decrease in $t_{WDU(MIN)}$ and a 5% increase in $t_{WDL(MAX)}$, giving 181 ms and 135 ms, respectively. A falling edge must be issued within this window.

8.2.2.4 Watchdog Disabled During Initialization Period

The watchdog is often needed to be disabled during startup to allow for an initialization period. When the initialization period is over, the watchdog timer is turned back on to allow the microcontroller to be monitored by the TPS3852-Q1. To achieve this setup, SET1 must start at GND. In this design, SET1 is controlled by a TPS3890-Q1 supervisor. In this application, the TPS3890-Q1 was chosen to monitor V_{DD} as well, meaning that $\overline{\text{RESET}}$ on the TPS3890-Q1 stays low until V_{DD} rises above V_{ITN}. When V_{DD} comes up, the delay time can be adjusted through the CT capacitor on the TPS3890-Q1. With this approach, the $\overline{\text{RESET}}$ delay can be adjusted from a minimum of 25 μs to a maximum of 30 seconds. For this design, a minimum delay of 7 seconds is needed until the watchdog timer is enabled. The CT capacitor calculation (see the TPS3890-Q1 data sheet) yields an ideal capacitance of 6.59 μF, giving a closest standard ceramic capacitor value of 6.8 μF. When connecting a 6.8-μF capacitor from CT to GND, the typical delay time is 7.21 seconds. 图 22 illustrates the typical startup waveform for this circuit when the watchdog input is off. 图 22 illustrates that when the watchdog is disabled, the $\overline{\text{WDO}}$ output remains high. See the TPS3890-Q1 data sheet for detailed information on the TPS3890-Q1.

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8.2.3 Glitch Immunity

图 25 shows the high-to-low glitch immunity for the TPS3852G33-Q1 with a 7% overdrive with V_{DD} starting at 3.3 V. This curve shows that V_{DD} can go below the threshold for 5.2 µs without $\overline{\text{RESET}}$ asserting.

8.2.4 Application Curves

Unless otherwise stated, application curves were taken at T_A = 25°C.

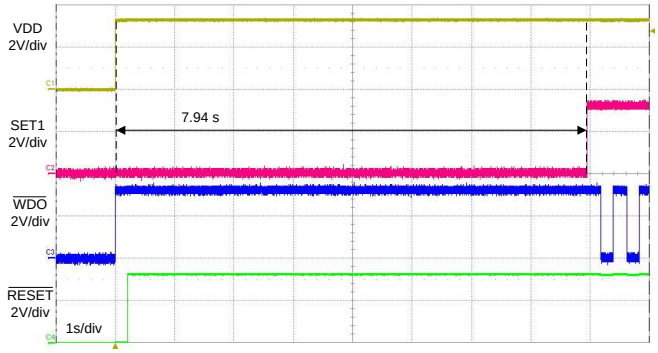


图 22. Startup Without a WDI Signal

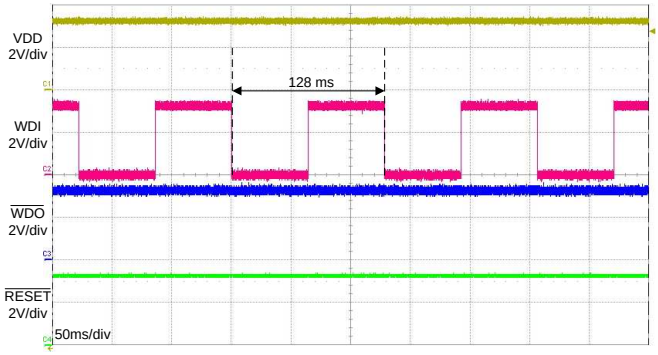


图 23. Typical WDI Signal

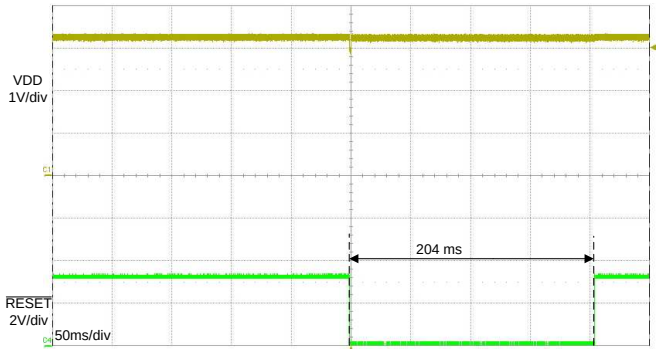


图 24. Typical $\overline{\text{RESET}}$ Delay

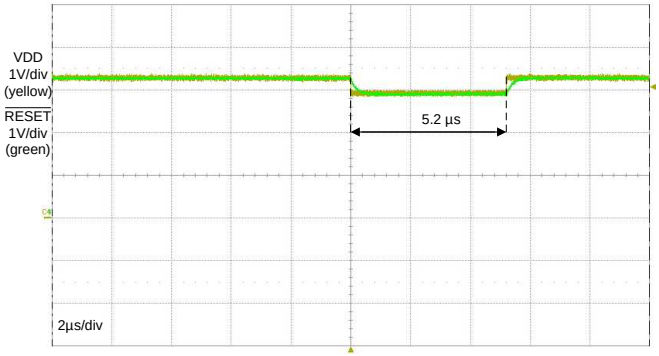


图 25. High-to-Low Glitch Immunity

9 Power Supply Recommendations

This device is designed to operate from an input supply with a voltage range between 1.6 V and 6.5 V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1-µF capacitor between the VDD pin and the GND pin.

10 Layout

10.1 Layout Guidelines

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1-µF ceramic capacitor as near as possible to the VDD pin.
- If a C_{CWD} capacitor or pull-up resistor is used, place these components as close as possible to the CWD pin. If the CWD pin is left unconnected, make sure to minimize the amount of parasitic capacitance on the pin.
- Place the pullup resistors on $\overline{\text{RESET}}$ and $\overline{\text{WDO}}$ as close to the pin as possible.

10.2 Layout Example

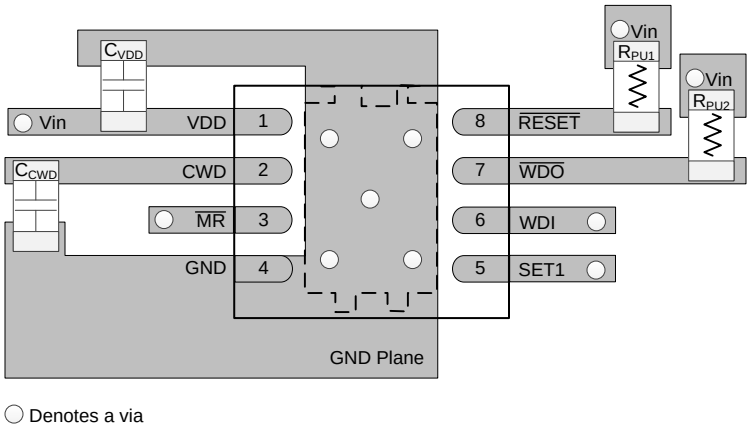


图 26. Typical Layout for the TPS3852-Q1

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11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 评估模块

*TPS3851EVM-780 评估模块*可用于评估此部件。使用此评估模块时，必须将 EVM 上的器件更换为 TPS3852-Q1。

11.1.2 器件命名规则

表 **5.** 器件命名规则

说明	命名规则	值
TPS3852 （具有窗口看门狗的高精度监控器）	—	—
X （标称阈值，受监视电压标称值的百分比）	G	V_{ITN} = –4%
	H	V_{ITN} = -7%
yy(y)(1) （受监视电压标称值选项）	18	1.8V
	33	3.3V

(1) 例如，TPS3852G33QDRBQ1 对应的受监视电压标称值为 3.3V，标称阈值为 -4%。

11.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

11.3 社区资源

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TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

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11.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3852G18QDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	852DB	Samples
TPS3852G33QDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	852GB	Samples
TPS3852H18QDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	852LB	Samples
TPS3852H33QDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	852PB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

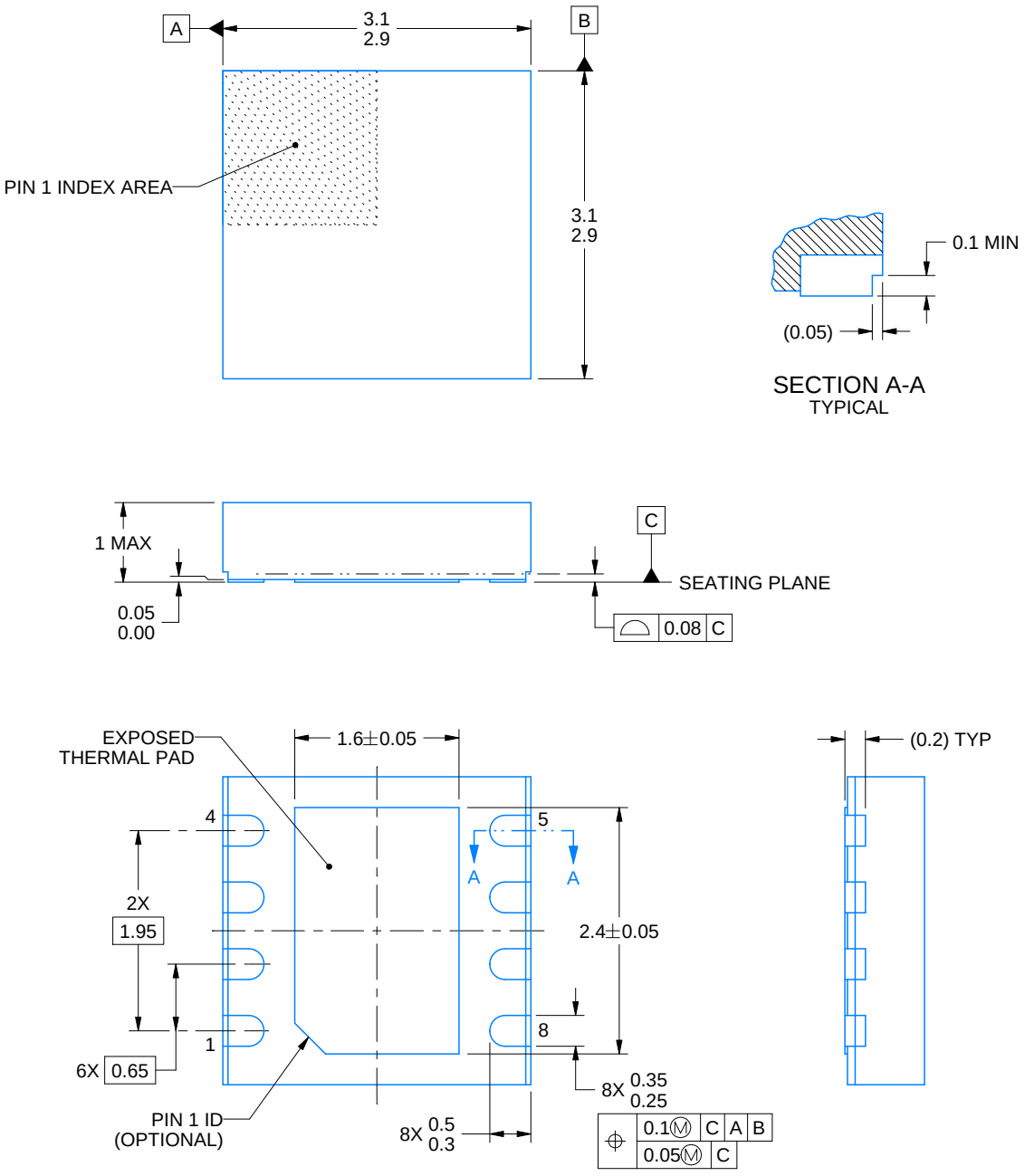
4203482/L

DRB0008F

PACKAGE OUTLINE

VSON - 1 mm max height

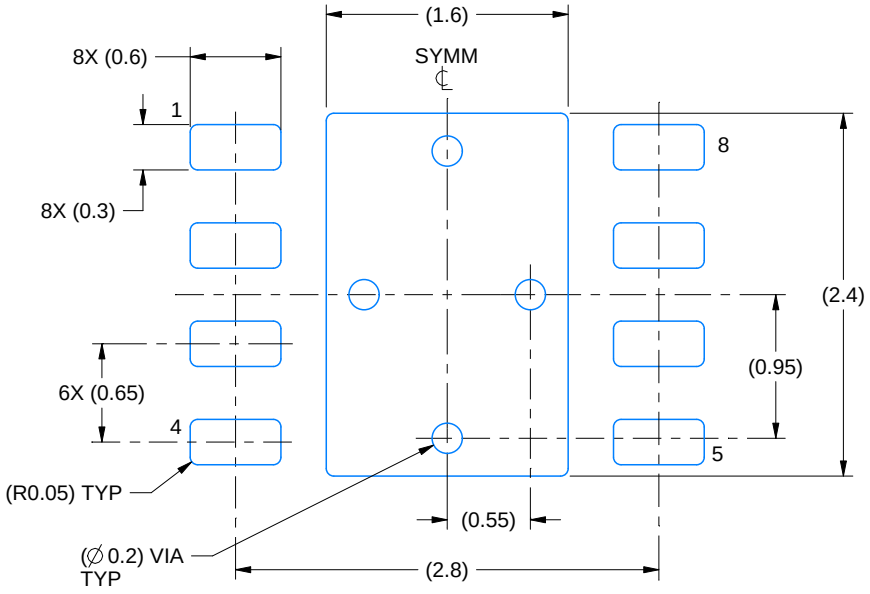
PLASTIC SMALL OUTLINE - NO LEAD



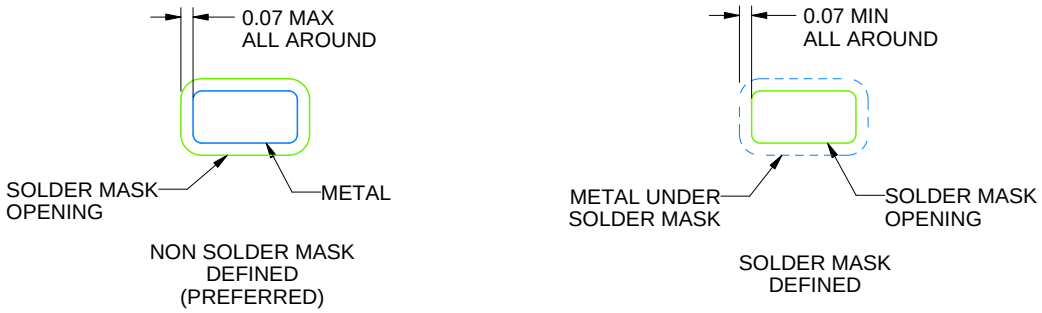
4222121/C 10/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

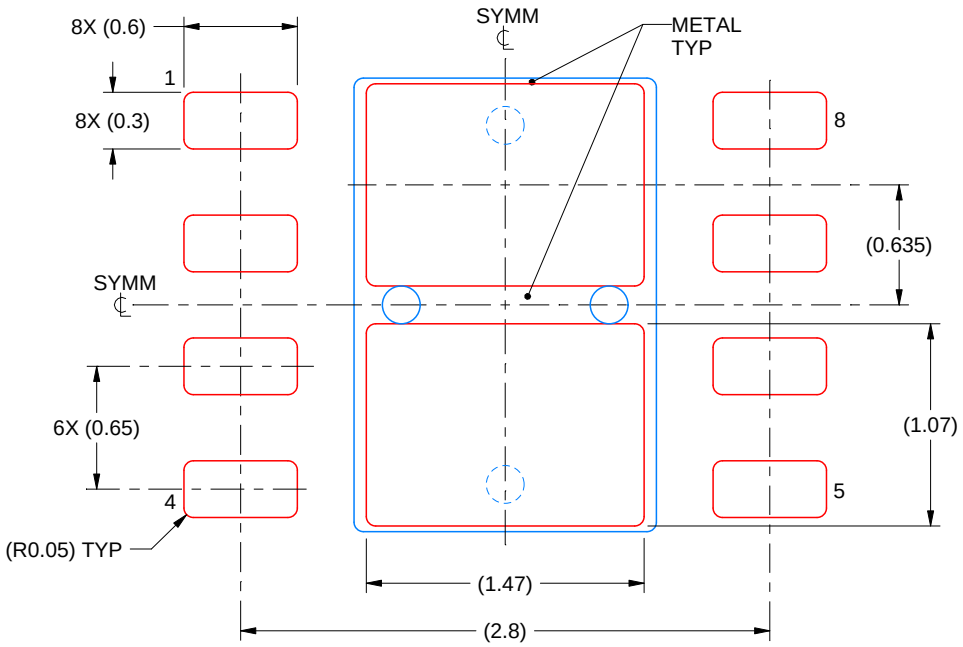


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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