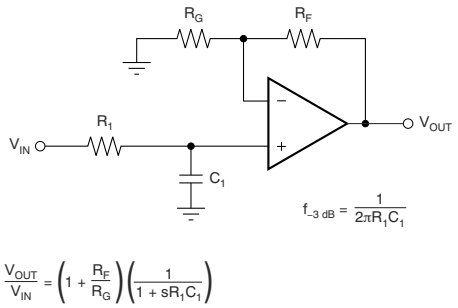
TLV910x 16V、1MHz、轨到轨输入/输出、低功耗运算放大器

1 特性

- 轨至轨输入和输出
- 高带宽：1.1MHz GBW
- 低静态电流：每个放大器 120μA
- 低失调电压：±300μV
- 低失调电压漂移：±0.6μV/°C
- 低噪声：10 kHz 时为 28nV/ √Hz
- 高共模抑制：110dB
- 低偏置电流：±10pA
- 高压摆率：4.5V/μs
- 宽电源电压：±1.35V 至 ±8V，2.7V 至 16V
- 强大的 EMIRR 性能：1.8GHz 时为 77dB

2 应用

- 光学模块
- 便携式测试和测量
- 宏远程无线电单元 (RRU)
- 基带单元 (BBU)
- 电器



TLV910x 应用于单极低通滤波器

3 说明

TLV910x 系列（TLV9101、TLV9102 和 TLV9104）是 16V 通用运算放大器系列。该系列具有出色的直流精度和交流性能，包括轨到轨输入/输出、低失调电压（±300μV，典型值）、低温漂（±0.6μV/°C，典型值）和 1.1MHz 带宽。

TLV910x 具有宽差分和共模输入电压范围、高输出电流（±80mA，典型值）、高压摆率（4.5V/μs，典型值）、低功耗运行（115μA，典型值）和关断功能，因而是一款稳定的低功耗、高性能运算放大器，适用于各种工业应用。

TLV910x 系列运算放大器采用*微型*尺寸封装以及标准封装，额定工作温度范围为 -40°C 至 125°C。

器件信息

器件型号 (1)	封装	封装尺寸（标称值）
TLV9101	SOT-23 (5)	2.90mm × 1.60mm
	SOT-23 (6)	2.90mm × 1.60mm
	SC70 (5)	2.00mm × 1.25mm
	SOT-553 (5)(2)	1.60mm × 1.20mm
TLV9102	SOIC (8)	4.90mm × 3.90mm
	SOT-23 (8)	2.90mm × 1.60mm
	TSSOP (8)	3.00mm × 4.40mm
	VSSOP (8)	3.00mm × 3.00mm
	VSSOP (10)	3.00mm × 3.00mm
	WSON (8)	2.00mm × 2.00mm
	X2QFN (10)	1.50mm × 1.50mm
TLV9104	SOIC (14)	8.65mm × 3.90mm
	TSSOP (14)	5.00mm × 4.40mm
	WQFN (16)	3.00mm × 3.00mm
	X2QFN (14)	2.00mm × 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 此封装为仅预发布状态。

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。
English Data Sheet: SBOS943

Table of Contents

1 特性 1
2 应用 1
3 说明 1
4 Revision History 2
5 Pin Configuration and Functions 5
6 Specifications 11
6.1 Absolute Maximum Ratings 11
6.2 ESD Ratings 11
6.3 Recommended Operating Conditions 11
6.4 Thermal Information for Single Channel 12
6.5 Thermal Information for Dual Channel 12
6.6 Thermal Information for Quad Channel 12
6.7 Electrical Characteristics 13
6.8 Typical Characteristics 16
7 Detailed Description 24
7.1 Overview 24
7.2 Functional Block Diagram 24
7.3 Feature Description 25
7.4 Device Functional Modes 32
8 Application and Implementation 33
8.1 Application Information 33
8.2 Typical Applications 33
9 Power Supply Recommendations 35
10 Layout 35
10.1 Layout Guidelines 35
10.2 Layout Example 35
11 Device and Documentation Support 38
11.1 Device Support 38
11.2 Documentation Support 38
11.3 接收文档更新通知 38
11.4 支持资源 38
11.5 Trademarks 38
11.6 Electrostatic Discharge Caution 38
11.7 术语表 38
12 Mechanical, Packaging, and Orderable Information 39

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (June 2021) to Revision E (August 2021) — **Page**

- 从*器件信息*表中删除了 TLV9102 VSSOP (8) 封装的预发布符号 1
- Removed preview notation from TLV9102 VSSOP-8 (DGK) package in the *Pin Configuration and Functions* section 5
- Removed preview note and added thermal data for VSSOP-8 (DGK) package in *Thermal Information for Dual Channel*. 12
- Added clarifying statement regarding logic low signal for SHDN pin in the *Shutdown* section 31
- Corrected statement on shutdown enable and disable times in the *Shutdown* section from 30 μs and 3 μs to 11 μs and 2.5 μs, respectively, to match the *Electrical Characteristics* section 31

Copyright © 2021 Texas Instruments Incorporated

Changes from Revision C (May 2020) to Revision D (June 2021) **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式 1
- 从*器件信息* 表中删除了 TLV9104 SOIC (14) 封装的预发布符号 1
- 从*器件信息* 表中删除了 TLV9104 TSSOP (14) 封装的预发布符号 1
- 从*器件信息* 表中删除了 TLV9102 SOT-23 (8) 封装的预发布符号 1
- 从*器件信息* 表中删除了 TLV9104 WQFN (16) 封装的预发布符号 1
- Removed preview notation from TLV9101 DBV package (SOT-23) in the *Pin Configuration and Functions* section 5
- Adjusted DRL pinout in the *Pin Configuration and Functions* section 5
- Removed preview notation from TLV9101 DCK package (SC70) in the *Pin Configuration and Functions* section 5
- Removed preview notation from TLV9101S DBV package (SOT-23) in the *Pin Configuration and Functions* section 5
- Clarified shutdown notation in the *Pin Configuration and Functions* section 5
- Removed preview notation from TLV9102 DDF package (SOT-23-8) in the *Pin Configuration and Functions* section 5
- Removed preview notation from TLV9104 SOIC (D) and TSSOP (PW) packages in the *Pin Configuration and Functions* section 5
- Removed preview notation from TLV9104 X2QFN (RUC) package in the *Pin Configuration and Functions* section 5
- Removed preview notation from TLV9104 WQFN (RTE) package in the *Pin Configuration and Functions* section 5
- Removed preview notation from TLV9104S WQFN (RTE) package in the *Pin Configuration and Functions* section 5
- Removed Table of Graphs from the *Specifications* section 11
- Removed preview note from WQFN (RTE) package in thermal information for quad channel 12
- Removed *Related Links* section from the *Device and Documentation Support* section 38

Changes from Revision B (May 2020) to Revision C (May 2020) **Page**

- 从*器件信息* 表中删除了 TLV9102 VSSOP (10) 封装的预发布符号 1
- 从*器件信息* 表中删除了 TLV9102 X2QFN (10) 封装的预发布符号 1
- Removed preview notation from TLV9102 DGS package (VSSOP) in the *Pin Configuration and Functions* section 5
- Removed preview notation from TLV9102 RUG package (X2QFN) in the *Pin Configuration and Functions* section 5

Changes from Revision A (April 2019) to Revision B (May 2020) **Page**

- 将 TLV9101 和 TLV9104 器件状态从*预告信息* 更改为*量产数据* 1
- 从*器件信息* 表中删除了 TLV9101 SOT-23 (5) 封装的预发布符号 1
- 从*器件信息* 表中删除了 TLV9101 SOT-23 (6) 封装的预发布符号 1
- 从*器件信息* 表中删除了 TLV9101 SC70 (5) 封装的预发布符号 1
- 从*器件信息* 表中删除了 TLV9102 TSSOP (8) 封装的预发布符号 1
- 从*器件信息* 表中删除了 TLV9102 WSON (8) 封装的预发布符号 1
- Removed preview notation from TLV9102 DSG package (WSON) in the *Pin Configuration and Functions* section 5
- Added SHUTDOWN to *Electrical Characteristics* 13
- Added *Packages With an Exposed Thermal Pad* to the *Feature Description* 31

Changes from Revision * (February 2019) to Revision A (April 2019) **Page**

- 将 TLV9102 器件状态从*预告信息*更改为*量产数据* 1
- 从*器件信息*表中删除了 TLV9102 SOIC (8) 封装的预发布符号.....1

Copyright © 2021 Texas Instruments Incorporated

5 Pin Configuration and Functions

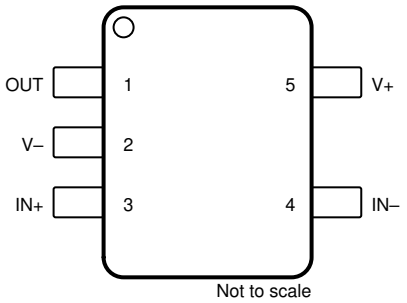
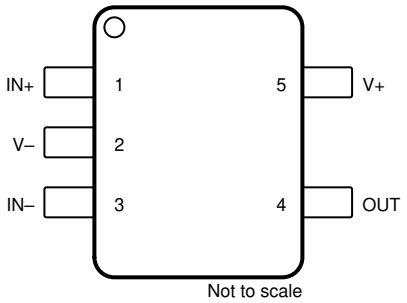


图 5-1. TLV9101 DBV Package 5-Pin SOT-23 Top View



A. Package is preview only.

图 5-2. TLV9101 DCK and DRL Package(A) 5-Pin SC70 and SOT-553 Top View

表 5-1. Pin Functions: TLV9101

PIN			I/O	DESCRIPTION
NAME	DBV	DCK and DRL		
+IN	3	1	I	Noninverting input
– IN	4	3	I	Inverting input
OUT	1	4	O	Output
V+	5	5	—	Positive (highest) power supply
V –	2	2	—	Negative (lowest) power supply

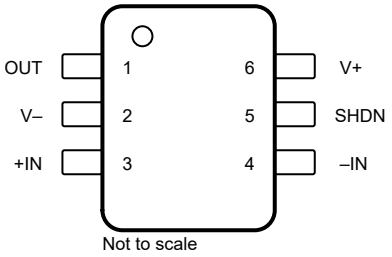


图 5-3. TLV9101S DBV Package 6-Pin SOT-23 Top View

表 5-2. Pin Functions: TLV9101S

PIN		I/O	DESCRIPTION
NAME	NO.		
IN+	3	I	Noninverting input
IN –	4	I	Inverting input
OUT	1	O	Output
SHDN	5	I	Shutdown: low = amplifier enabled, high = amplifier disabled. See 节 7.3.10 for more information.
V+	6	—	Positive (highest) power supply
V –	2	—	Negative (lowest) power supply

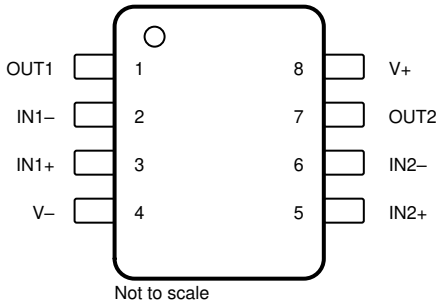
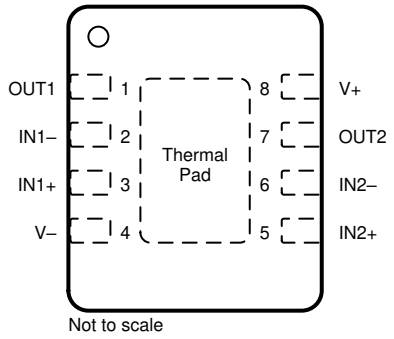


图 5-4. TLV9102 D, DDF, DGK, and PW Package 8-Pin SOIC, SOT-23, TSSOP, and VSSOP Top View



A. Connect thermal pad to V–. See 节 7.3.9 for more information.

图 5-5. TLV9102 DSG Package(A) 8-Pin WSON With Exposed Thermal Pad Top View

表 5-3. Pin Functions: TLV9102

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN1–	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2–	6	I	Inverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

Copyright © 2021 Texas Instruments Incorporated

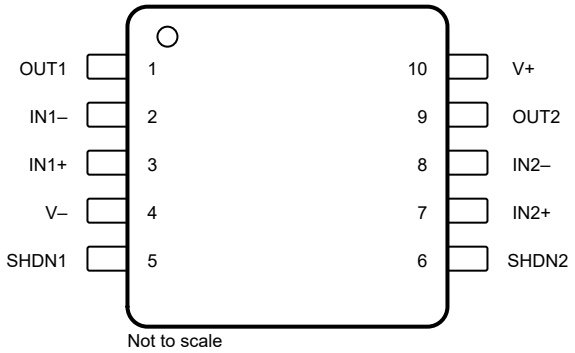


图 5-6. TLV9102S DGS Package 10-Pin VSSOP Top View

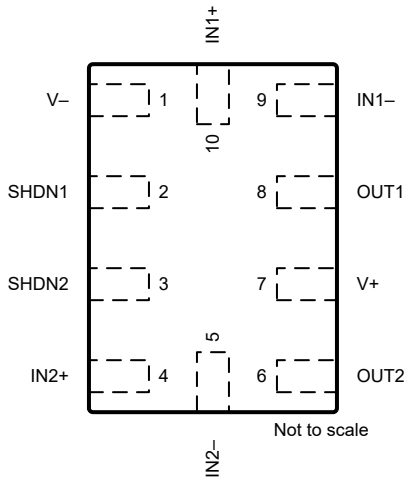


图 5-7. TLV9102S RUG Package 10-Pin X2QFN Top View

表 5-4. Pin Functions: TLV9102S

PIN			I/O	DESCRIPTION
NAME	VSSOP	X2QFN		
IN1+	3	10	I	Noninverting input, channel 1
IN1 –	2	9	I	Inverting input, channel 1
IN2+	7	4	I	Noninverting input, channel 2
IN2 –	8	5	I	Inverting input, channel 2
OUT1	1	8	O	Output, channel 1
OUT2	9	6	O	Output, channel 2
SHDN1	5	2	I	Shutdown, channel 1: low = amplifier enabled, high = amplifier disabled. See 节 7.3.10 for more information.
SHDN2	6	3	I	Shutdown, channel 2: low = amplifier enabled, high = amplifier disabled. See 节 7.3.10 for more information.
V+	10	7	—	Positive (highest) power supply
V –	4	1	—	Negative (lowest) power supply

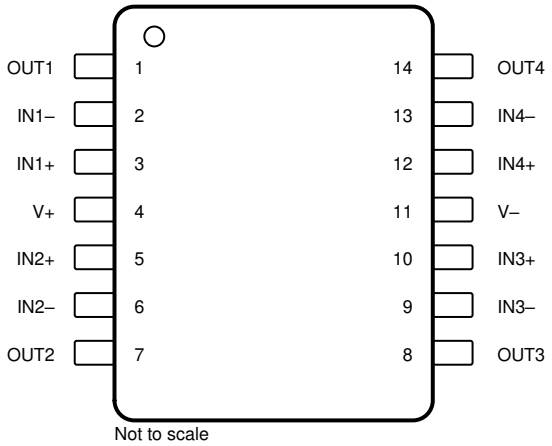
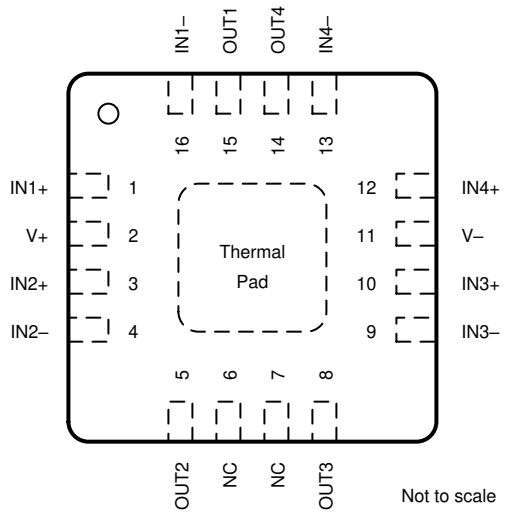


图 5-8. TLV9104 D and PW Package 14-Pin SOIC and TSSOP Top View



A. Connect thermal pad to V–. See 节 7.3.9 for more information.

图 5-9. TLV9104 RTE Package(A) 16-Pin WQFN With Exposed Thermal Pad Top View

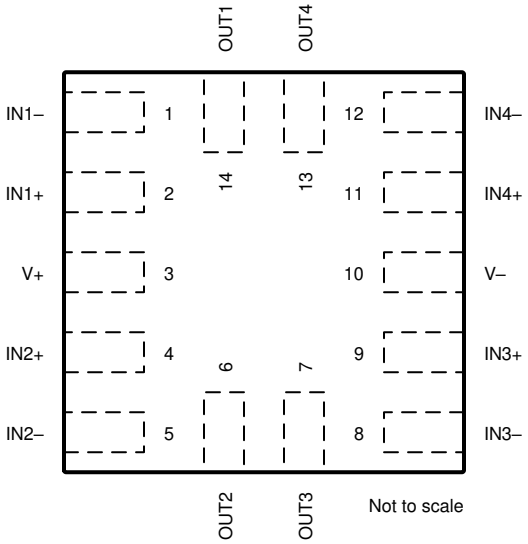


图 5-10. TLV9104 RUC Package 14-Pin WQFN With Exposed Thermal Pad Top View

表 5-5. Pin Functions: TLV9104

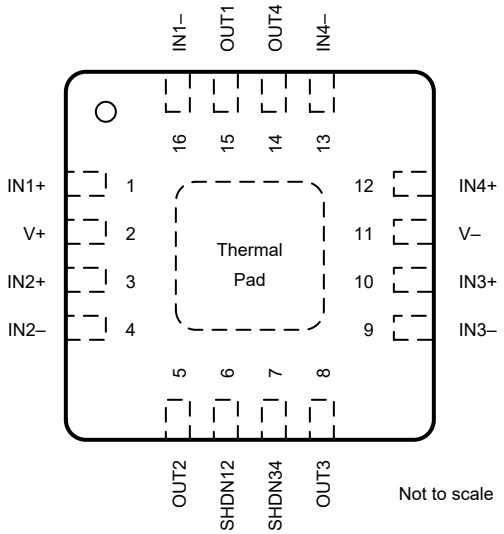
PIN				I/O	DESCRIPTION
NAME	SOIC and TSSOP	WQFN	X2QFN		
IN1+	3	1	2	I	Noninverting input, channel 1
IN1–	2	16	1	I	Inverting input, channel 1
IN2+	5	3	4	I	Noninverting input, channel 2
IN2–	6	4	5	I	Inverting input, channel 2

Copyright © 2021 Texas Instruments Incorporated

表 5-5. Pin Functions: TLV9104 (continued)

PIN				I/O	DESCRIPTION
NAME	SOIC and TSSOP	WQFN	X2QFN		
IN3+	10	10	9	I	Noninverting input, channel 3
IN3 –	9	9	8	I	Inverting input, channel 3
IN4+	12	12	11	I	Noninverting input, channel 4
IN4 –	13	13	12	I	Inverting input, channel 4
NC	—	6, 7	—	—	Do not connect
OUT1	1	15	14	O	Output, channel 1
OUT2	7	5	6	O	Output, channel 2
OUT3	8	8	7	O	Output, channel 3
OUT4	14	14	13	O	Output, channel 4
V+	4	2	3	—	Positive (highest) power supply
V –	11	11	10	—	Negative (lowest) power supply

Copyright © 2021 Texas Instruments Incorporated



A. Connect thermal pad to V – . See 节 7.3.9 for more information.

图 5-11. TLV9104S RTE Package(A)
16-Pin WQFN With Exposed Thermal Pad
Top View

表 5-6. Pin Functions: TLV9104S

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	1	I	Noninverting input, channel 1
IN1 –	16	I	Inverting input, channel 1
IN2+	3	I	Noninverting input, channel 2
IN2 –	4	I	Inverting input, channel 2
IN3+	10	I	Noninverting input, channel 3
IN3 –	9	I	Inverting input, channel 3
IN4+	12	I	Noninverting input, channel 4
IN4 –	13	I	Inverting input, channel 4
OUT1	15	O	Output, channel 1
OUT2	5	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
SHDN12	6	I	Shutdown, channels 1 and 2: low = amplifiers enabled, high = amplifiers disabled. See 节 7.3.10 for more information.
SHDN34	7	I	Shutdown, channels 3 and 4: low = amplifiers enabled, high = amplifiers disabled. See 节 7.3.10 for more information.
V+	2	—	Positive (highest) power supply
V –	11	—	Negative (lowest) power supply

Copyright © 2021 Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	20	V
Signal input pins	Common-mode voltage[3]	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage[3]		V_S + 0.2	V
	Current[3]	–10	10	mA
Shutdown pin voltage		V–	V+	V
Output short-circuit[2]		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	2.7	16	V
V_I	Input voltage range	(V–) – 0.2	(V+) + 0.2	V
V_{IH}	High level input voltage at shutdown pin (amplifier disabled)	(V–) + 1.1	V+	V
V_{IL}	Low level input voltage at shutdown pin (amplifier enabled)	V–	(V–) + 0.2	V
T_A	Specified temperature	–40	125	°C

6.4 Thermal Information for Single Channel

THERMAL METRIC[1]		TLV9101, TLV9101S				UNIT
		DBV (SOT-23)		DCK (SC70)	DRL[2] (SOT-553)	
		5 PINS	6 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	192.2	174.6	204.7	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	113.7	113.5	116.6	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.6	55.9	51.9	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	37.4	39.7	24.9	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	60.4	55.7	51.6	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) This package option is preview for TLV9101.

6.5 Thermal Information for Dual Channel

THERMAL METRIC[1]		TLV9102, TLV9102S							UNIT
		D (SOIC)	DDF (SOT-23-8)	DGK (VSSOP)	DGS (VSSOP)	DSG (WSON)	PW (TSSOP)	RUG (X2QFN)	
		8 PINS	8 PINS	8 PINS	10 PINS	8 PINS	8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138.7	150.4	189.3	152.2	81.6	188.4	149.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.7	85.6	75.8	67.3	101.6	77.1	58.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	82.2	70.0	111.0	95.5	48.3	119.1	77.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.8	8.1	15.4	67.9	6.0	14.2	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	81.4	69.6	109.3	94.3	48.3	117.4	77.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	22.8	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Thermal Information for Quad Channel

THERMAL METRIC[1]		TLV9104, TLV9104S				UNIT
		D (SOIC)	PW (TSSOP)	RTE (WQFN)	RUC (WQFN)	
		14 PINS	14 PINS	16 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.2	134.7	53.5	143.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.2	55.0	58.3	46.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.1	79.0	28.6	81.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	21.4	9.2	2.1	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	60.7	78.1	28.6	81.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	12.6	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Copyright © 2021 Texas Instruments Incorporated

6.7 Electrical Characteristics

For V_S = (V+) – (V–) = 2.7 V to 16 V (±1.35 V to ±8 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = V–			±0.3	±1.5	mV
			T_A = –40°C to 125°C			±1.75	
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to 125°C		±0.6		μV/℃
PSRR	Input offset voltage versus power supply	V_{CM} = V–	T_A = –40°C to 125°C		±0.1	±0.7	μV/V
	Channel separation	f = 0 Hz			5		μV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±10		pA
I_{OS}	Input offset current				±5		pA
NOISE							
E_N	Input voltage noise	f = 0.1 Hz to 10 Hz			6		$μV_{PP}$
					1		$μV_{RMS}$
e_N	Input voltage noise density	f = 1 kHz			30		nV/√Hz
		f = 10 kHz			28		
i_N	Input current noise	f = 1 kHz			2		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	V_S = 16 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V (Main input pair)	T_A = –40°C to 125°C	90	110		dB
		V_S = 4 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V (Main input pair)		75	95		
		V_S = 2.7 – 16 V, (V+) – 1 V < V_{CM} < (V+) + 0.1 V (Aux input pair)			80		
		(V+) – 2 V < V_{CM} < (V+) – 1 V		See Offset Voltage (Transition Region) in the *Typical Characteristics* section			
INPUT CAPACITANCE							
Z_{ID}	Differential				100 ‖ 3		MΩ ‖ pF
Z_{ICM}	Common-mode				6 ‖ 1		TΩ ‖ pF

6.7 Electrical Characteristics (continued)

For V_S = (V+) – (V–) = 2.7 V to 16 V (±1.35 V to ±8 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 16 V, V_{CM} = V– (V–) + 0.1 V < V_O < (V+) – 0.1 V	T_A = –40°C to 125°C	115	135		dB
		V_S = 4 V, V_{CM} = V– (V–) + 0.1 V < V_O < (V+) – 0.1 V		104	125		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				1.1		MHz
SR	Slew rate	V_S = 16 V, G = +1, C_L = 20 pF			4.5		V/µs
t_S	Settling time	To 0.1%, V_S = 16 V, V_{STEP} = 10 V, G = +1, CL = 20 pF			4		µs
		To 0.1%, V_S = 16 V, V_{STEP} = 2 V, G = +1, CL = 20 pF			2		
		To 0.01%, V_S = 16 V, V_{STEP} = 10 V, G = +1, CL = 20 pF			5		
		To 0.01%, V_S = 16 V, V_{STEP} = 2 V, G = +1, CL = 20 pF			3		
	Phase margin	G = +1, R_L = 10 kΩ, C_L = 20 pF			60		°
	Overload recovery time	V_{IN} × gain > V_S			600		ns
THD+N	Total harmonic distortion + noise	V_S = 16 V, V_O = 1 V_{RMS}, G = -1, f = 1 kHz			0.0028%		
OUTPUT							
	Voltage output swing from rail	Positive and negative rail headroom	V_S = 16 V, R_L = no load		3		mV
			V_S = 16 V, R_L = 10 kΩ		45	60	
			V_S = 16 V, R_L = 2 kΩ		200	300	
			V_S = 2.7 V, R_L = no load		1		
			V_S = 2.7 V, R_L = 10 kΩ		5	20	
			V_S = 2.7 V, R_L = 2 kΩ		25	50	
I_{SC}	Short-circuit current				±80		mA
C_{LOAD}	Capacitive load drive			See Small-Signal Overshoot vs Capacitive Load in the *Typical Characteristics* section			
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A			600		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			115	150	µA
			T_A = –40°C to 125°C			160	

Copyright © 2021 Texas Instruments Incorporated

6.7 Electrical Characteristics (continued)

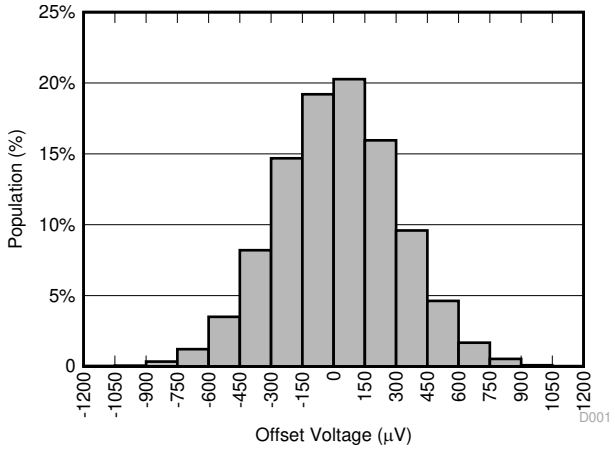
For V_S = (V+) – (V–) = 2.7 V to 16 V (±1.35 V to ±8 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SHUTDOWN						
I_{QSD}	Quiescent current per amplifier	V_S = 2.7 V to 16 V, all amplifiers disabled, SHDN = V+		20	30	µA
Z_{SHDN}	Output impedance during shutdown	V_S = 2.7 V to 16 V, amplifier disabled, SHDN = V+		10 || 12		GΩ || pF
V_{IH}	Logic high threshold voltage (amplifier disabled)	For valid input high, the SHDN pin voltage should be greater than the maximum threshold but less than or equal to V+		(V–) + 0.8	(V–) + 1.1	V
V_{IL}	Logic low threshold voltage (amplifier enabled)	For valid input low, the SHDN pin voltage should be less than the minimum threshold but greater than or equal to V–	(V–) + 0.2	(V–) + 0.8		V
t_{ON}	Amplifier enable time (1)	G = +1, V_{CM} = V–, V_O = 0.1 × V_S / 2		11		µs
t_{OFF}	Amplifier disable time (1)	V_{CM} = V–, V_O = V_S / 2		2.5		µs
	SHDN pin input bias current (per pin)	V_S = 2.7 V to 16 V, (V–) + 20 V ≥ SHDN ≥ (V–) + 0.9 V		500		nA
		V_S = 2.7 V to 16 V, (V–) ≤ SHDN ≤ (V–) + 0.7 V		150		

(1) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the SHDN pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.

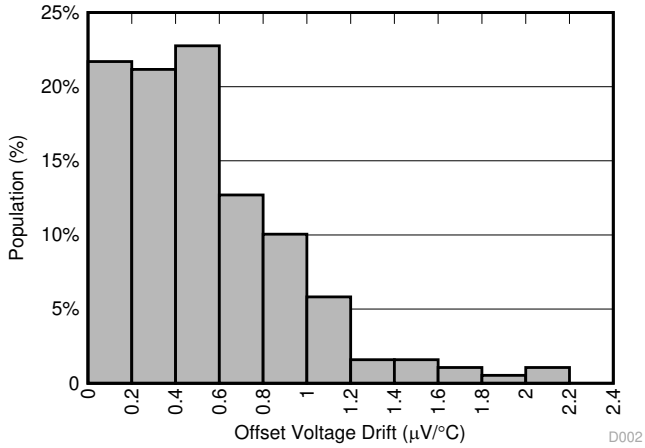
6.8 Typical Characteristics

at T_A = 25°C, V_S = ±8 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



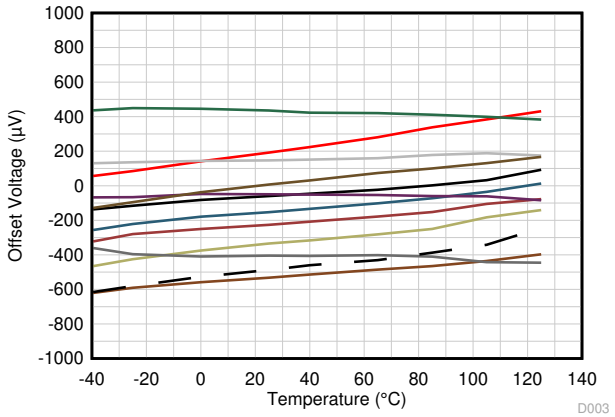
Distribution from 13, 481 amplifiers; T_A = 25°C

图 6-1. Offset Voltage Production Distribution



Distribution from 175 amplifiers

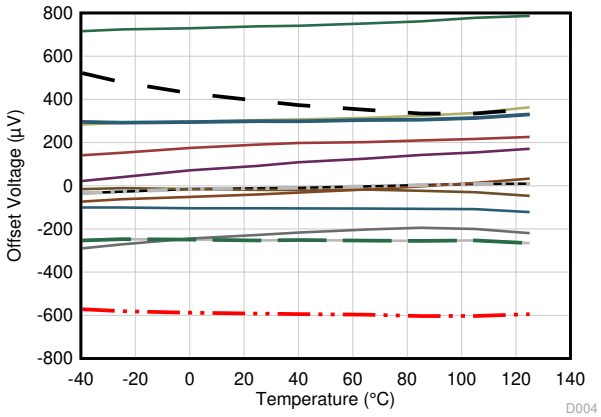
图 6-2. Offset Voltage Drift Distribution



V_{CM} = V+

Each color represents one sample device.

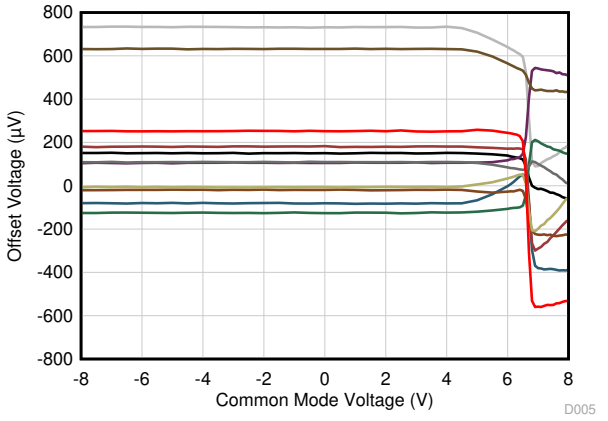
图 6-3. Offset Voltage vs Temperature



V_{CM} = V –

Each color represents one sample device.

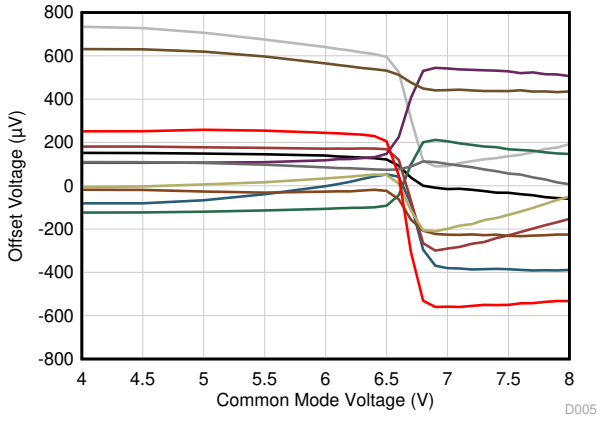
图 6-4. Offset Voltage vs Temperature



T_A = 25°C

Each color represents one sample device.

图 6-5. Offset Voltage vs Common-Mode Voltage



T_A = 25°C

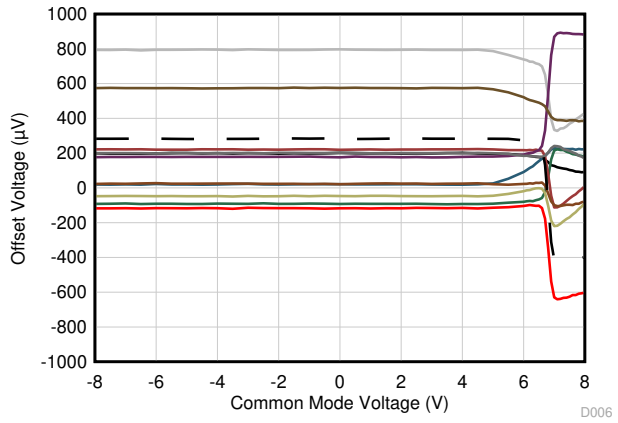
Each color represents one sample device.

图 6-6. Offset Voltage vs Common-Mode Voltage (Transition Region)

Copyright © 2021 Texas Instruments Incorporated

6.8 Typical Characteristics (continued)

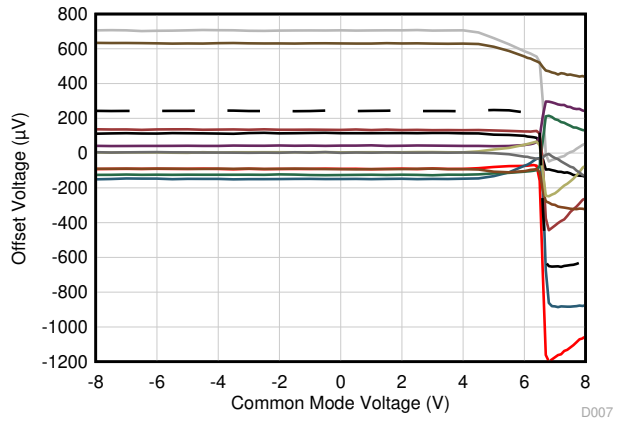
at T_A = 25°C, V_S = ±8 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



T_A = 125°C

Each color represents one sample device.

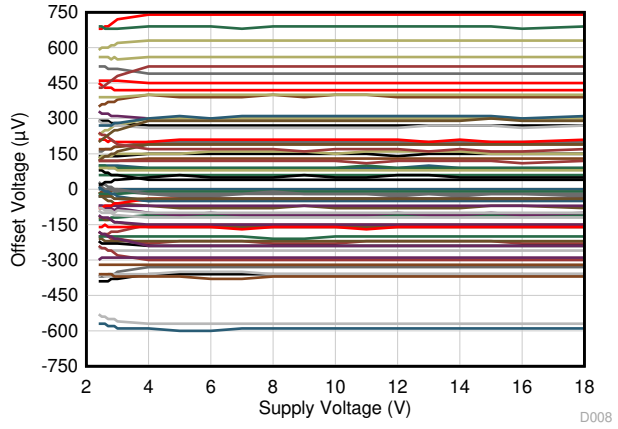
图 6-7. Offset Voltage vs Common-Mode Voltage



T_A = –40°C

Each color represents one sample device.

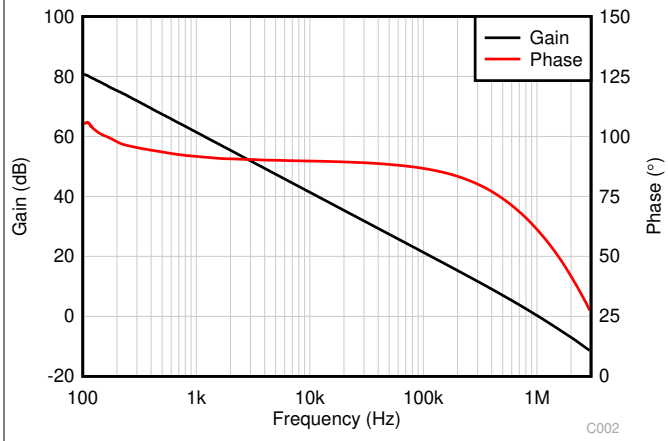
图 6-8. Offset Voltage vs Common-Mode Voltage



V_{CM} = V –

Each color represents one sample device.

图 6-9. Offset Voltage vs Power Supply



C_{LOAD} = 15 pF

图 6-10. Open-Loop Gain and Phase vs Frequency

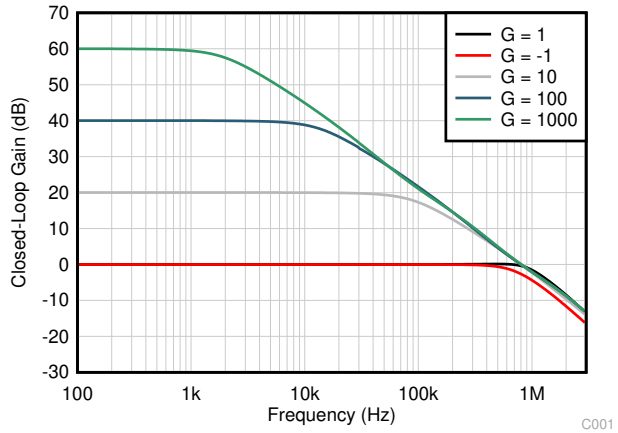


图 6-11. Closed-Loop Gain and Phase vs Frequency

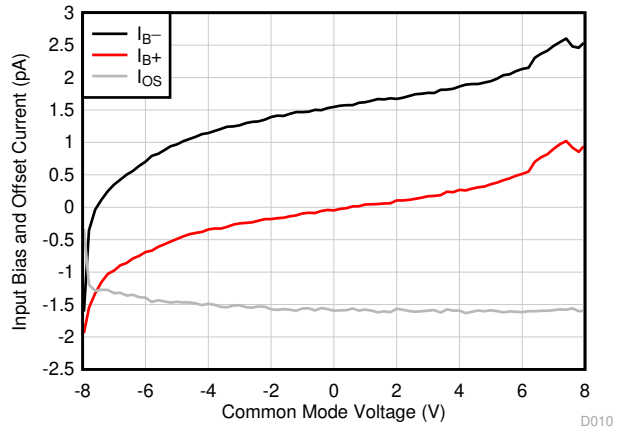


图 6-12. Input Bias Current vs Common-Mode Voltage

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±8 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

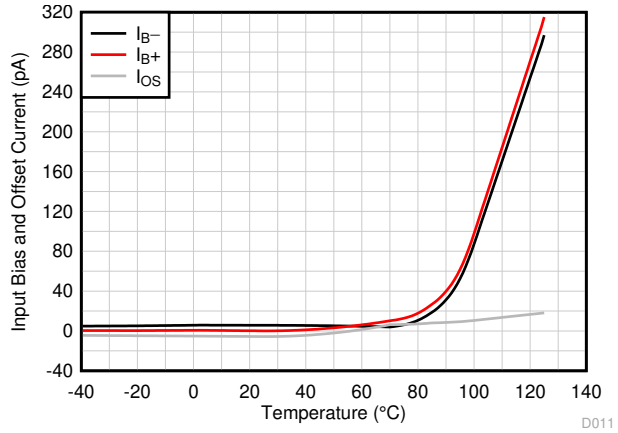


图 6-13. Input Bias Current vs Temperature

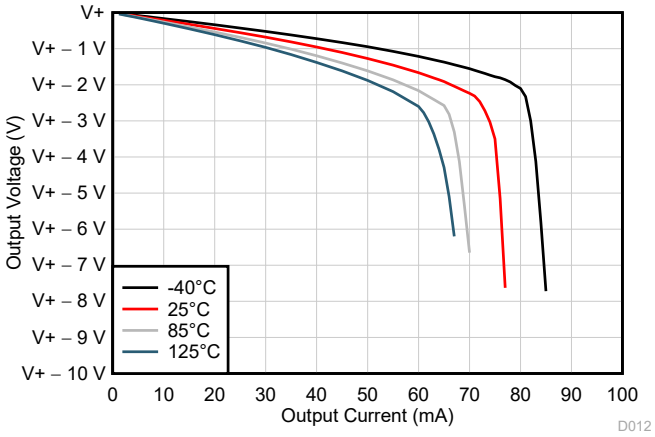


图 6-14. Output Voltage Swing vs Output Current (Sourcing)

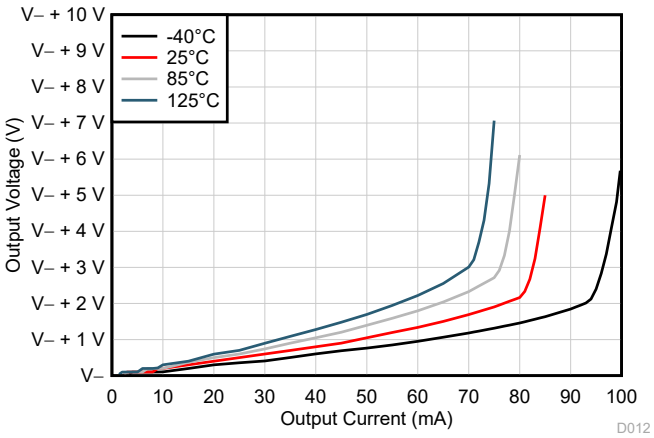
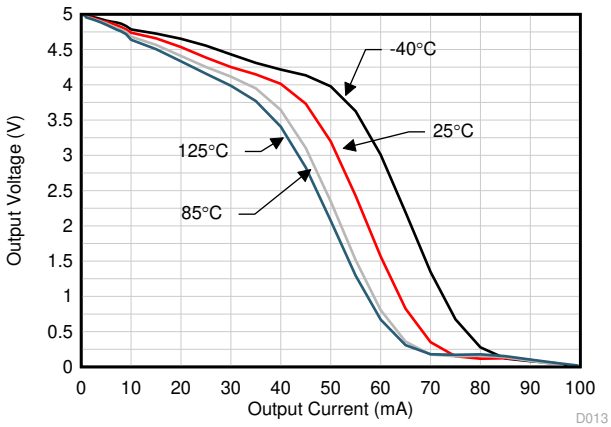
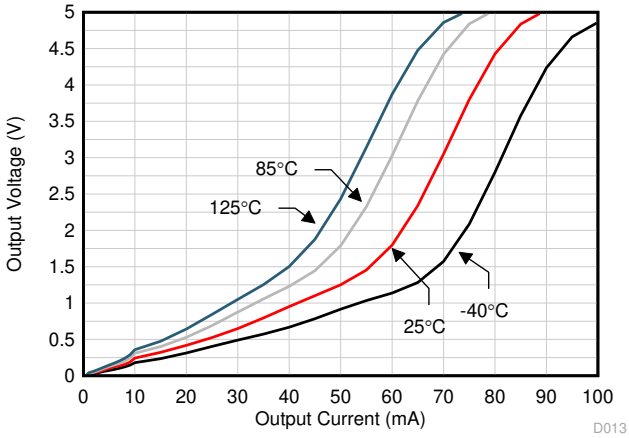


图 6-15. Output Voltage Swing vs Output Current (Sinking)



V_S = 5 V, R_L connected to V –

图 6-16. Output Voltage Swing vs Output Current (Sourcing)



V_S = 5 V, R_L connected to V+

图 6-17. Output Voltage Swing vs Output Current (Sinking)

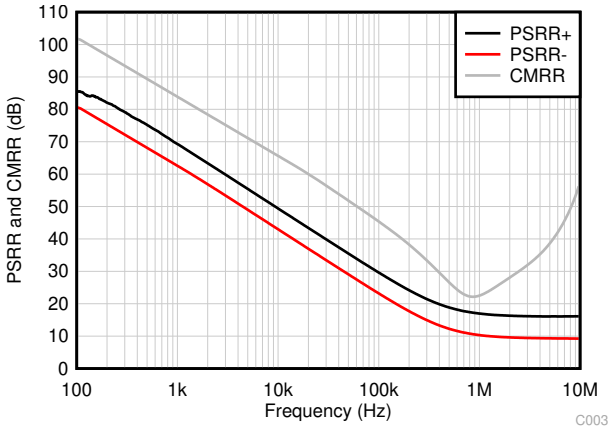
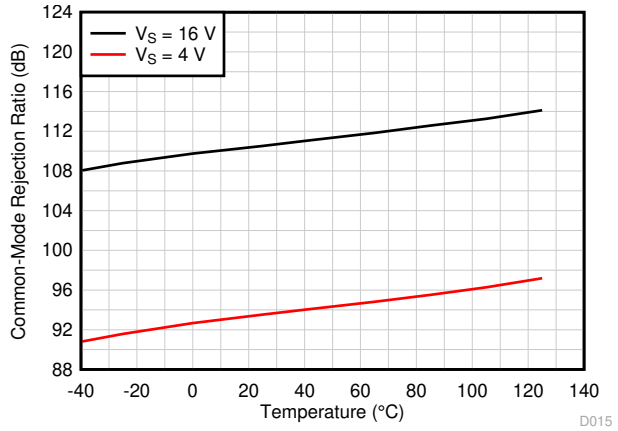


图 6-18. CMRR and PSRR vs Frequency

Copyright © 2021 Texas Instruments Incorporated

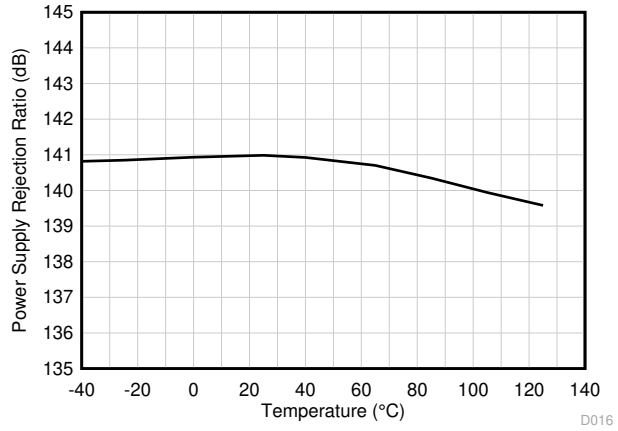
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±8 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



f = 0 Hz

图 6-19. CMRR vs Temperature (dB)



f = 0 Hz

图 6-20. PSRR vs Temperature (dB)

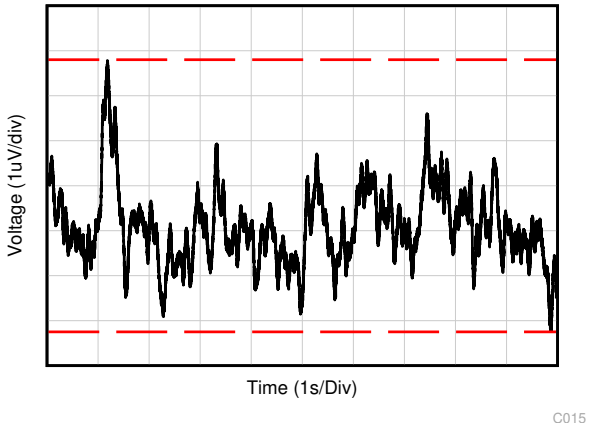


图 6-21. 0.1-Hz to 10-Hz Noise

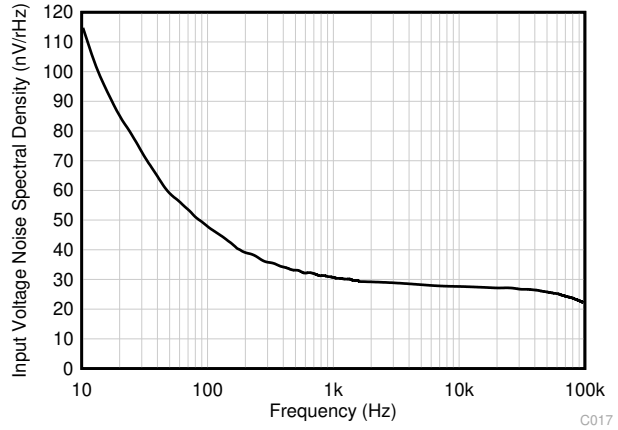
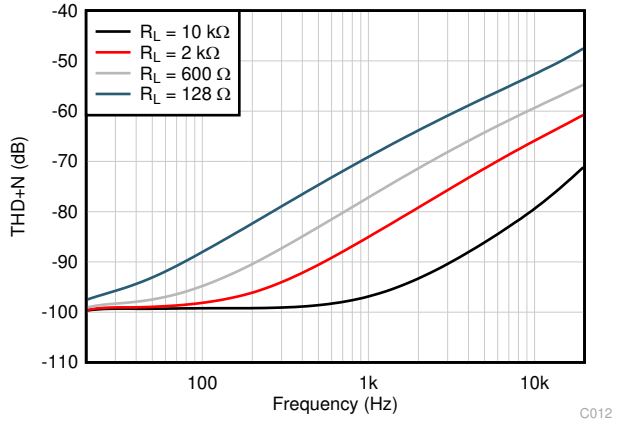
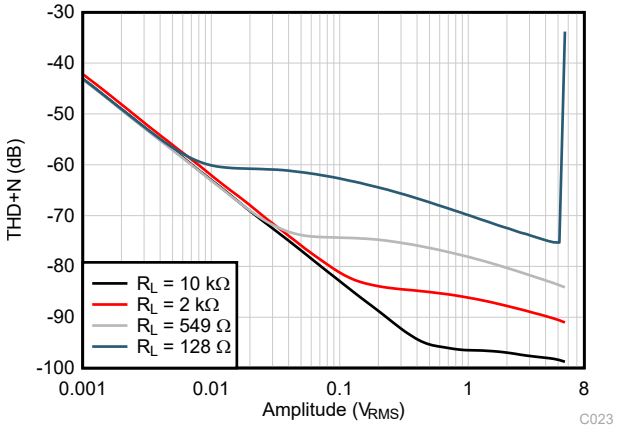


图 6-22. Input Voltage Noise Spectral Density vs Frequency



BW = 80 kHz, V_{OUT} = 3.5 V_{RMS}

图 6-23. THD+N Ratio vs Frequency



BW = 80 kHz, f = 1 kHz

图 6-24. THD+N vs Output Amplitude

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±8 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

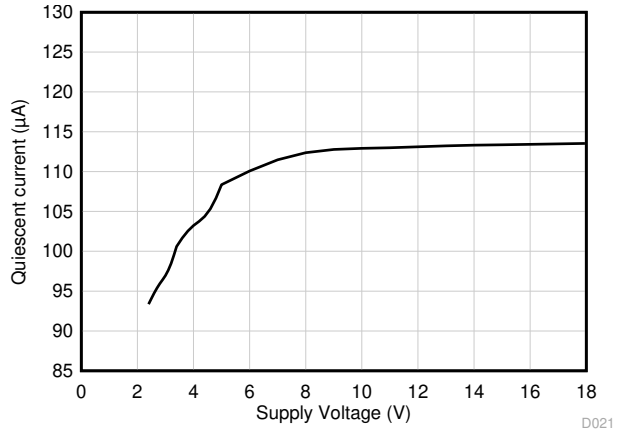


图 6-25. Quiescent Current per Channel vs Supply Voltage

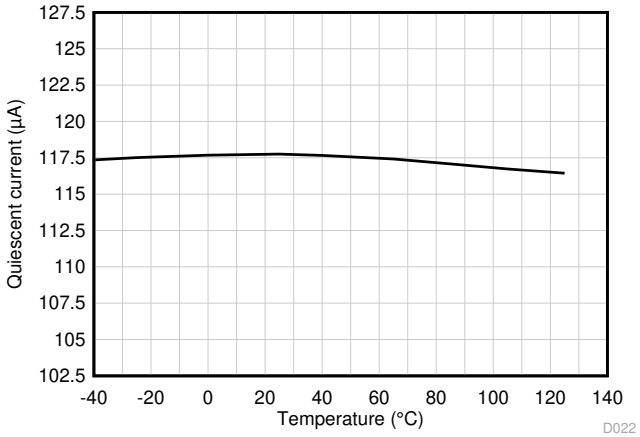


图 6-26. Quiescent Current per Channel vs Temperature

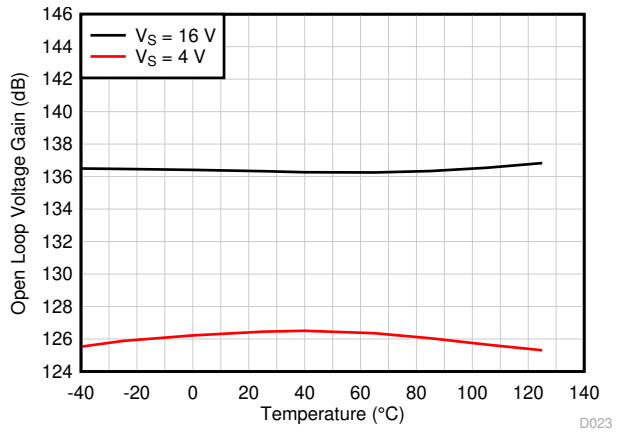


图 6-27. Open-Loop Voltage Gain vs Temperature (dB)

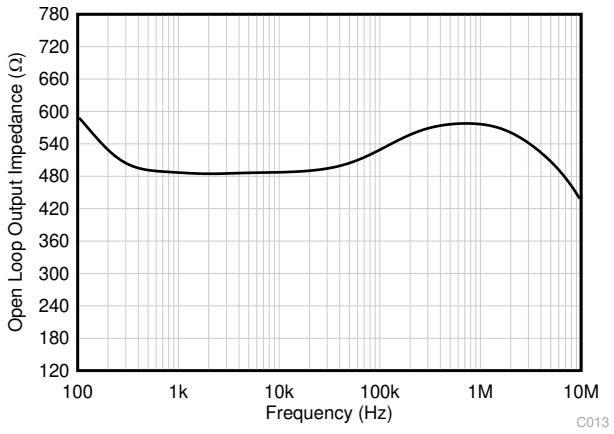
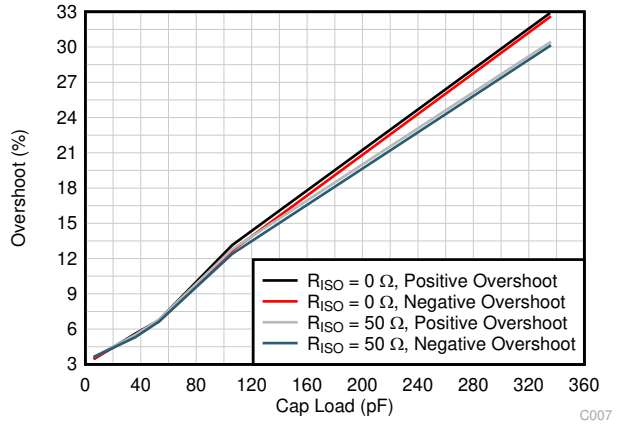
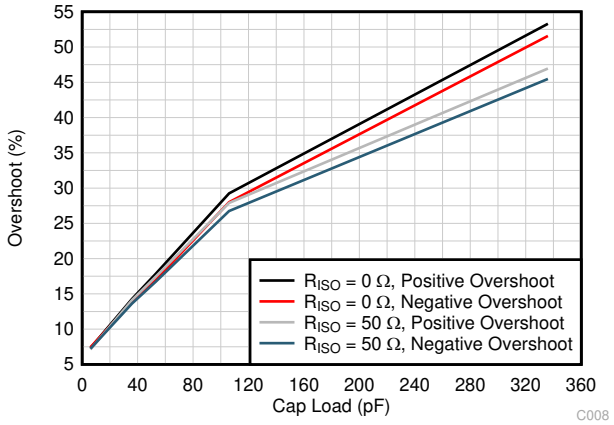


图 6-28. Open-Loop Output Impedance vs Frequency



G = –1, 100-mV output step

图 6-29. Small-Signal Overshoot vs Capacitive Load



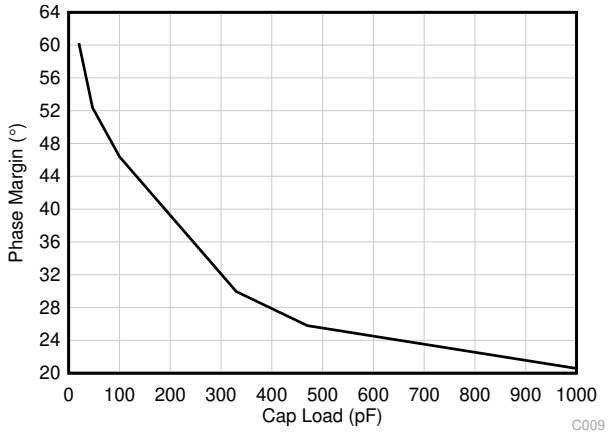
G = 1, 100-mV output step

图 6-30. Small-Signal Overshoot vs Capacitive Load

Copyright © 2021 Texas Instruments Incorporated

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±8 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



G = –1, 100-mV output step

图 6-31. Small-Signal Overshoot vs Capacitive Load

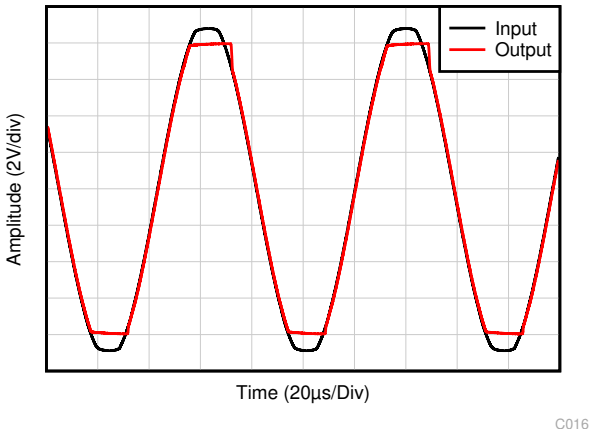
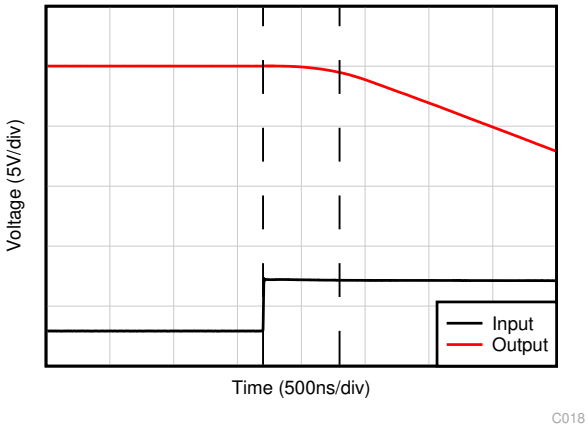
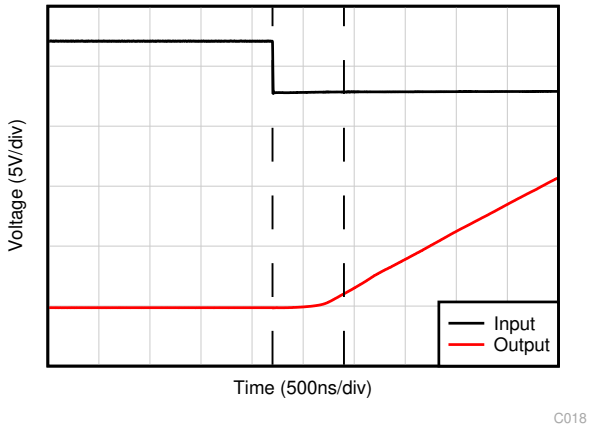


图 6-32. No Phase Reversal



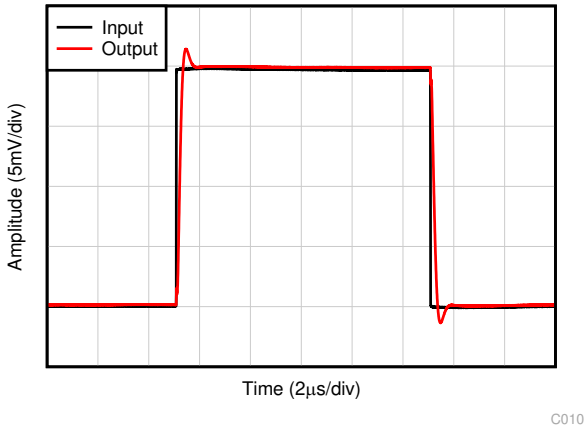
G = –10

图 6-33. Positive Overload Recovery



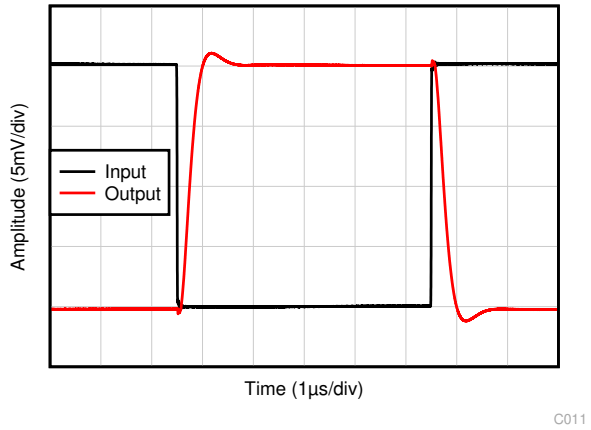
G = –10

图 6-34. Negative Overload Recovery



C_L = 20 pF, G = 1, 20-mV step response

图 6-35. Small-Signal Step Response

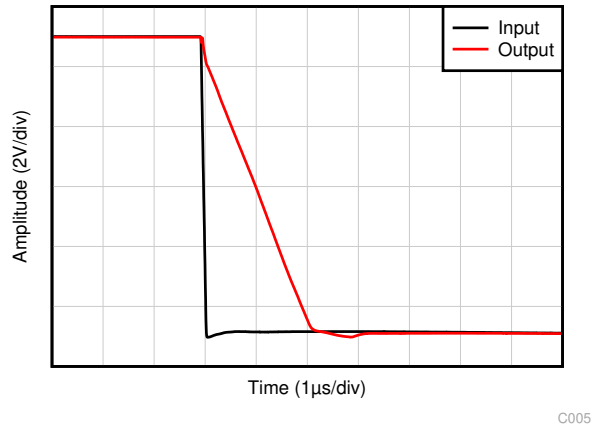


R_L = 1 kΩ, C_L = 20 pF, G = –1, 10-mV step response

图 6-36. Small-Signal Step Response

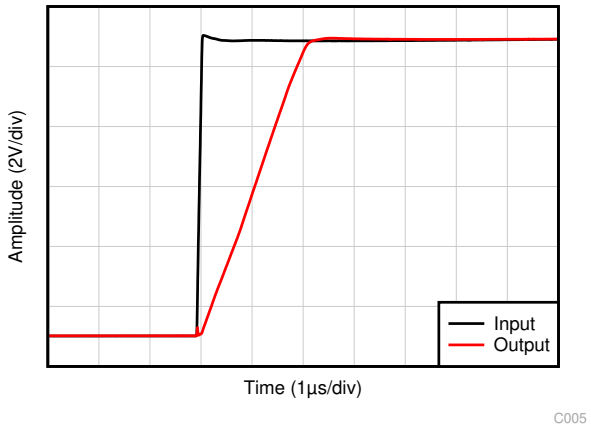
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±8 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



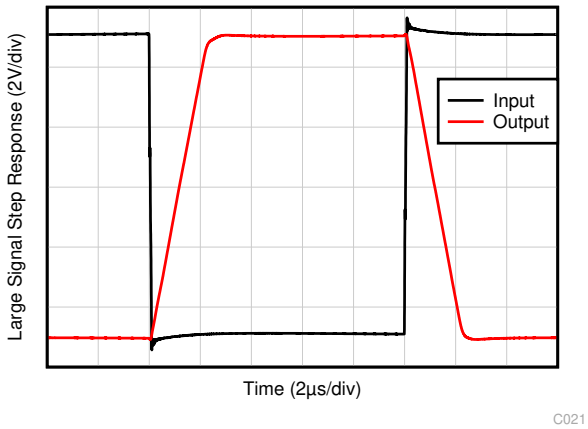
C_L = 20 pF, G = 1

图 6-37. Large-Signal Step Response (Falling)



C_L = 20 pF, G = 1

图 6-38. Large-Signal Step Response (Rising)



C_L = 10 pF, G = –1

图 6-39. Large-Signal Step Response

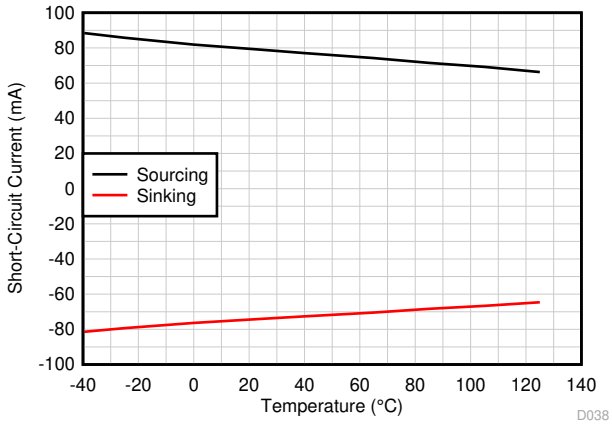


图 6-40. Short-Circuit Current vs Temperature

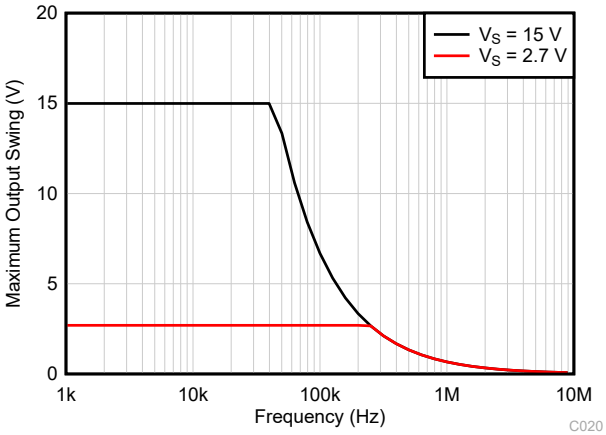


图 6-41. Maximum Output Voltage vs Frequency

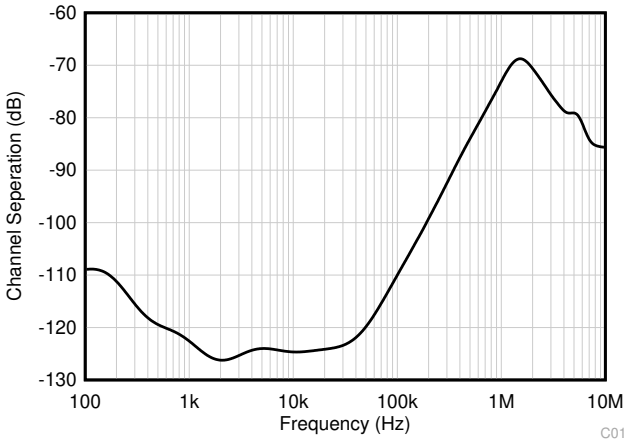


图 6-42. Channel Separation vs Frequency

Copyright © 2021 Texas Instruments Incorporated

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±8 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

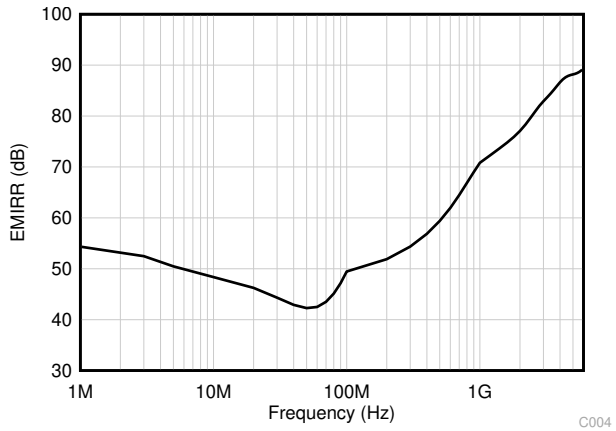


图 6-43. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

7 Detailed Description

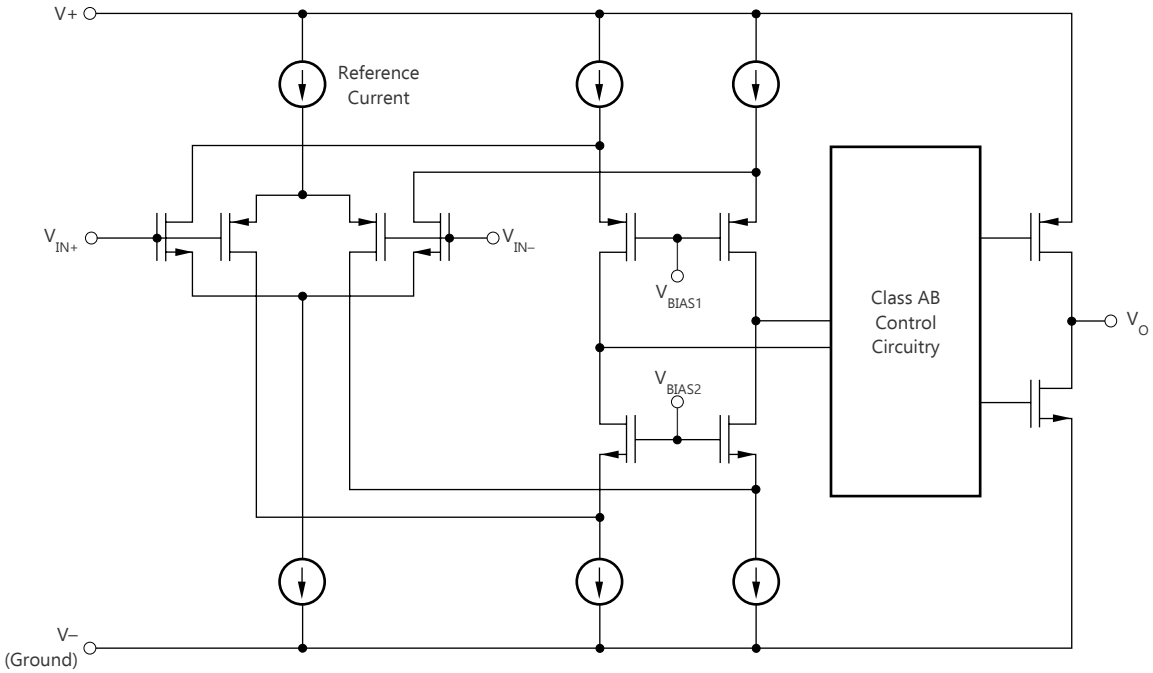
7.1 Overview

The TLV910x family (TLV9101, TLV9102, and TLV9104) is a family of 16-V general purpose operational amplifiers.

These devices offer excellent DC precision and AC performance, including rail-to-rail input/output, low offset (±300 µV, typ), low offset drift (±0.6 µV/°C, typ), and 1.1-MHz bandwidth.

Wide differential and common-mode input-voltage range, high output current (±80 mA), high slew rate (4.5 V/µs), low power operation (120 µA, typ), and shutdown functionality make the TLV910x a robust, low-power, high-performance operational amplifier for industrial applications.

7.2 Functional Block Diagram



Copyright © 2021 Texas Instruments Incorporated

7.3 Feature Description

7.3.1 EMI Rejection

The TLV910x uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV910x benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 图 7-1 shows the results of this testing on the TLV910x. 表 7-1 shows the EMIRR IN+ values for the TLV910x at particular frequencies commonly encountered in real-world applications. 表 7-1 lists applications that can be centered on or operated near the particular frequency shown. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

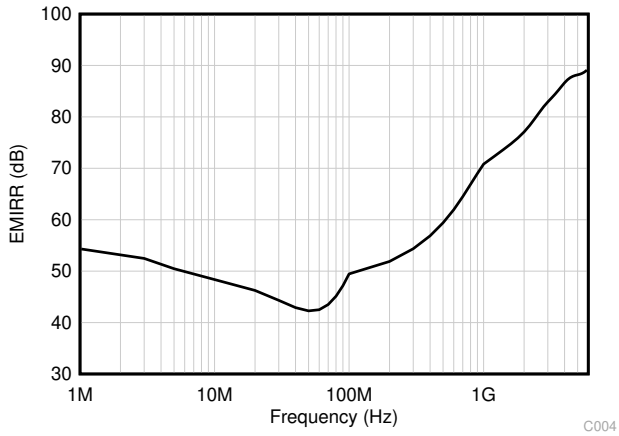


图 7-1. TLV910x EMIRR Testing

表 7-1. TLV910x EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	59.5 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	68.9 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	77.8 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	78.0 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88.8 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	87.6 dB

7.3.2 Phase Reversal Protection

The TLV910x family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The TLV910x is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in 图 7-2.

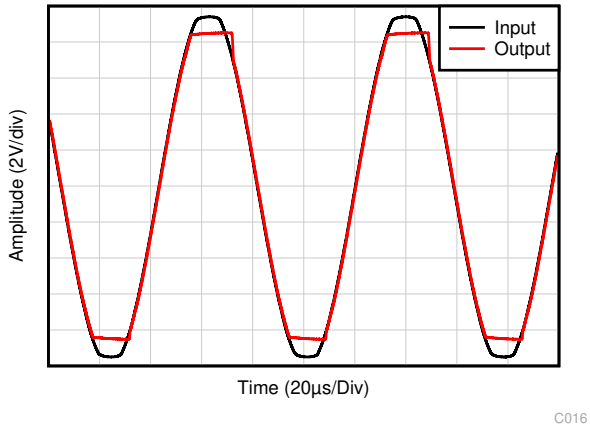


图 7-2. No Phase Reversal

7.3.3 Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the TLV910x is 150°C. Exceeding this temperature causes damage to the device. The TLV910x has a thermal protection feature that prevents damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 140°C. 图 7-3 shows an application example for the TLV9101 that has significant self heating (154°C) because of its power dissipation (0.39 W). Thermal calculations indicate that for an ambient temperature of 100°C, the device junction temperature must reach 154°C. The actual device, however, turns off the output drive to maintain a safe junction temperature. 图 7-3 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3 V. When self heating causes the device junction temperature to increase above 140°C, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor RL.

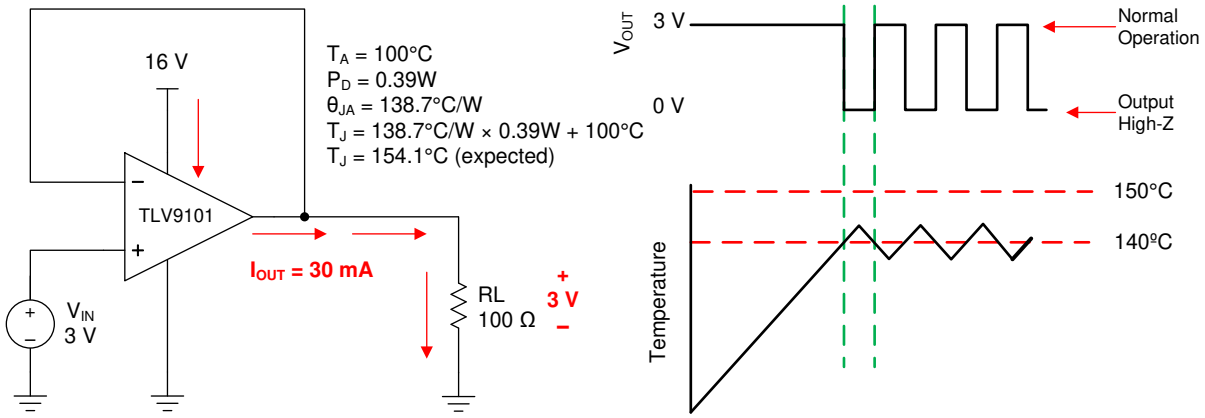


图 7-3. Thermal Protection

Copyright © 2021 Texas Instruments Incorporated

7.3.4 Capacitive Load and Stability

The TLV910x features a resistive output stage capable of driving moderate capacitive loads, and by leveraging an isolation resistor, the device can easily be configured to drive large capacitive loads. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see 图 7-4 and 图 7-5. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation.

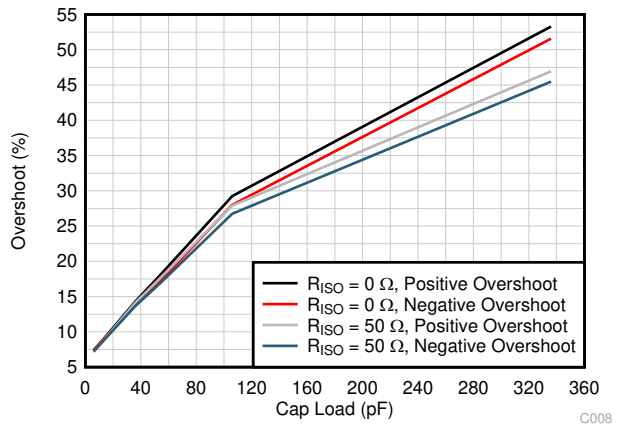


图 7-4. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step, G = 1)

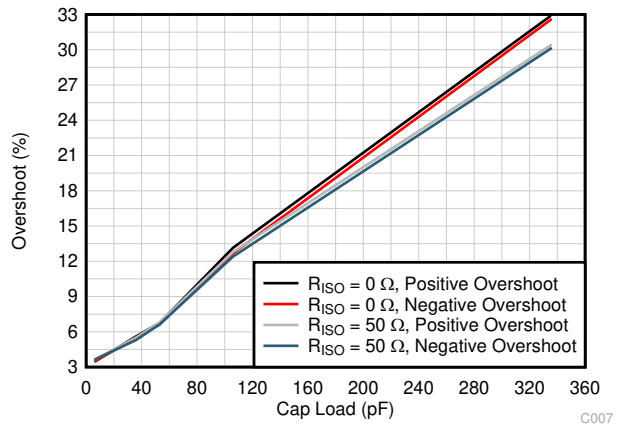


图 7-5. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step, G = –1)

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small (10 Ω to 20 Ω) resistor, R_{ISO}, in series with the output, as shown in 图 7-6. This resistor significantly reduces ringing and maintains DC performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. A high capacitive load drive makes the TLV910x well suited for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in 图 7-6 uses an isolation resistor, R_{ISO}, to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin.

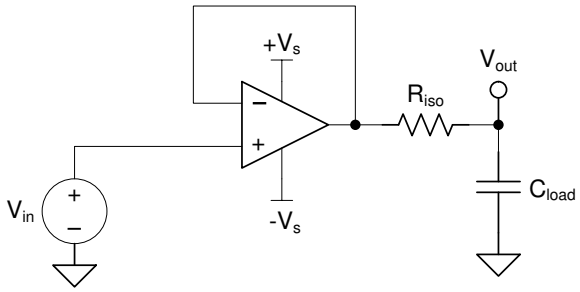


图 7-6. Extending Capacitive Load Drive With the TLV9101

7.3.5 Common-Mode Voltage Range

The TLV910x is a 16-V, true rail-to-rail input operational amplifier with an input common-mode range that extends 100 mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in 图 7-7. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1 V to 100 mV above the positive supply. The P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 2 V. There is a small transition region, typically (V+) –2 V to (V+) – 1 V in which both input pairs are on. This transition region can vary modestly with process variation, and within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance can be degraded compared to operation outside this region. To achieve best performance with the TLV910x family, avoid this transition region when possible.

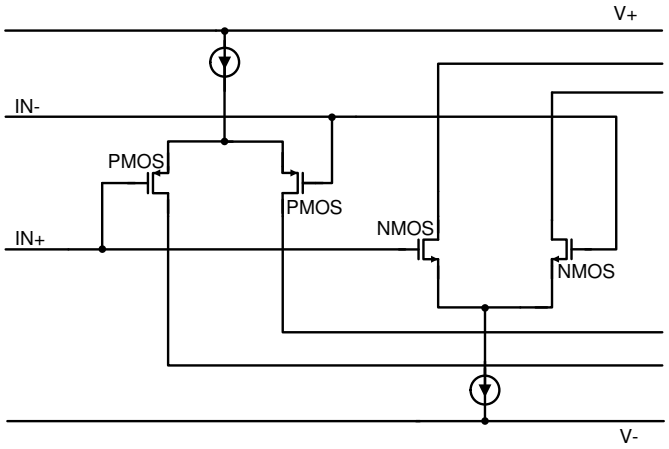


图 7-7. Rail-to-Rail Input Stage

Copyright © 2021 Texas Instruments Incorporated

7.3.6 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. 图 7-8 shows an illustration of the ESD circuits contained in the TLV910x (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

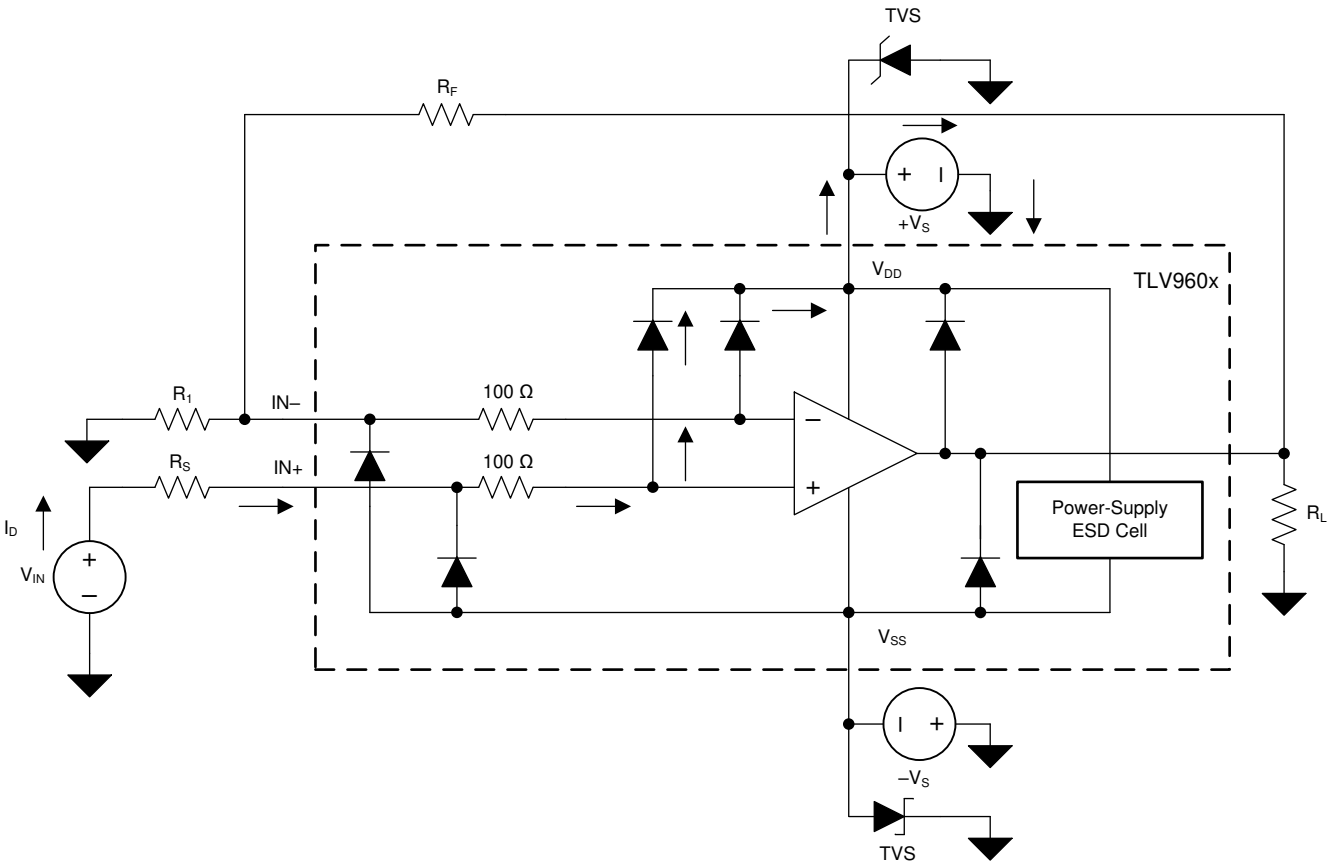


图 7-8. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example, 1 kV, 100 ns), whereas an EOS event is long duration and lower voltage (for example, 50 V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

7.3.7 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV910x is approximately 1 µs.

7.3.8 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier in order to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier will exhibit some amount of deviation from the ideal value, like the input offset voltage of an amplifier. These deviations often follow *Gaussian* ("bell curve"), or *normal* distributions, and circuit designers can leverage this information to guardband their system, even when there is not a minimum or maximum specification in 节 6.7.

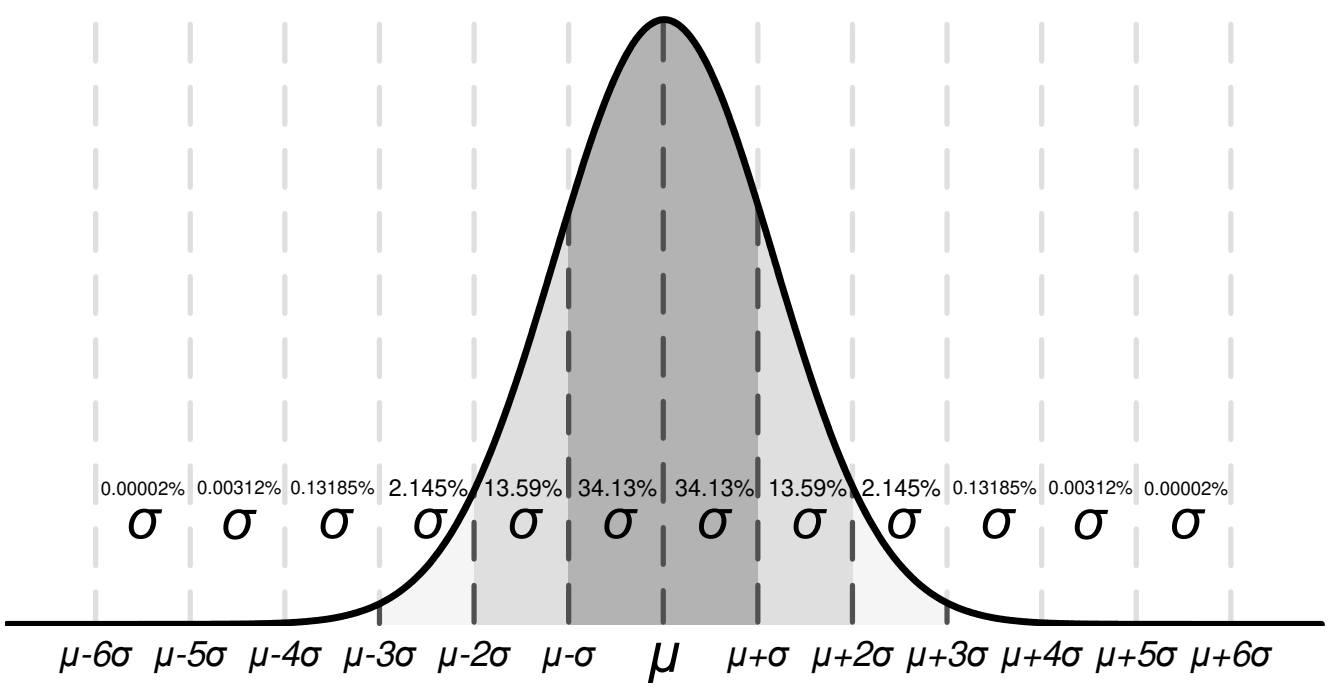


图 7-9. Ideal Gaussian Distribution

图 7-9 shows an example distribution, where *μ*, or *mu*, is the mean of the distribution, and where σ, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-

Copyright © 2021 Texas Instruments Incorporated

thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from $\mu - \sigma$ to $\mu + \sigma$).

Depending on the specification, values listed in the *typical* column of 节 6.7 are represented in different ways. As a general rule of thumb, if a specification naturally has a nonzero mean (for example, gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation (μ + σ) in order to most accurately represent the typical value.

You can use this chart to calculate approximate probability of a specification in a unit; for example, for TLV910x, the typical input voltage offset is 300 μV, so 68.2% of all TLV910x devices are expected to have an offset from –300 μV to +300 μV. At 4 σ (±1200 μV), 99.9937% of the distribution has an offset voltage less than ±1200 μV, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are assured by TI, and units outside these limits will be removed from production material. For example, the TLV910x family has a maximum offset voltage of 1.5 mV at 25°C, and even though this corresponds to 5 σ (≈1 in 1.7 million units), which is extremely unlikely, TI assures that any unit with larger offset than 1.5 mV will be removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for your application, and design worst-case conditions using this value. For example, the 6-σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance and can be an option as a wide guardband to design a system around. In this case, the TLV910x family does not have a maximum or minimum for offset voltage drift, but based on 图 6-2 and the typical value of 0.6 μV/°C in 节 6.7, it can be calculated that the 6-σ value for offset voltage drift is about 3.6 μV/°C. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot assure the performance of a device. This information should be used only to estimate the performance of a device.

7.3.9 Packages With an Exposed Thermal Pad

The TLV910x family is available in packages such as the WSON-8 (DSG) and WQFN-16 (RTE), which feature an exposed thermal pad. Inside the package, the die is attached to this thermal pad using an electrically conductive compound. For this reason, when using a package with an exposed thermal pad, the thermal pad must either be connected to V– or left floating. Attaching the thermal pad to a potential other than V– is not allowed, and performance of the device is not assured when doing so.

7.3.10 Shutdown

The TLV910xS devices feature one or more shutdown pins (SHDN) that disable the op amp, placing it into a low-power standby mode. In this mode, the op amp typically consumes about 20 μA. The SHDN pins are active high, meaning that shutdown mode is enabled when the input to the SHDN pin is a valid logic high. The amplifier is enabled when the input to the SHDN pin is a valid logic low.

The SHDN pins are referenced to the negative supply rail of the op amp. The threshold of the shutdown feature lies around 800 mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to ensure smooth switching characteristics. To ensure optimal shutdown behavior, the SHDN pins should be driven with valid logic signals. A valid logic low is defined as a voltage between V– and V– + 0.2 V. A valid logic high is defined as a voltage between V– + 1.1 V and V+. The shutdown pin circuitry includes a pulldown resistor, which will inherently pull the voltage of the pin to the negative supply rail if not driven. Thus, to enable the amplifier, the SHDN pins should either be left floating or driven to a valid logic low. To disable the amplifier, the SHDN pins must be driven to a valid logic high. The maximum voltage allowed at the SHDN pins is V+ or V– + 20 V, whichever is lower. Exceeding this voltage level will damage the device.

The SHDN pins are high-impedance CMOS inputs. Channels of single and dual op amp packages are independently controlled, and channels of quad op amp packages are controlled in pairs. For battery-operated

applications, this feature can be used to greatly reduce the average current and extend battery life. The typical enable time out of shutdown is 11 µs; disable time is 2.5 µs. When disabled, the output assumes a high-impedance state. This architecture allows the TLV910xS family to operate as a gated amplifier, multiplexer, or programmable-gain amplifier. Shutdown time (t_{OFF}) depends on loading conditions and increases as load resistance increases. To ensure shutdown (disable) within a specific shutdown time, the specified 10-kΩ load to midsupply (VS / 2) is required. If using the TLV910xS without a load, the resulting turnoff time significantly increases.

7.4 Device Functional Modes

The TLV910x has a single functional mode and is operational when the power-supply voltage is greater than 2.7 V (±1.35 V). The maximum power supply voltage for the TLV910x is 16 V (±8 V).

Copyright © 2021 Texas Instruments Incorporated

8 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TLV910x family offers excellent DC precision and DC performance. These devices operate up to 16-V supply rails and offer true rail-to-rail input/output, low offset voltage and offset voltage drift, as well as 1.1-MHz bandwidth and high output drive. These features make the TLV910x a robust, high-performance operational amplifier for high-voltage industrial applications.

8.2 Typical Applications

8.2.1 High Voltage Precision Comparator

Many different systems require controlled voltages across numerous system nodes to ensure robust operation. A comparator can be used to monitor and control voltages by comparing a reference threshold voltage with an input voltage and providing an output when the input crosses this threshold.

The TLV910x family of op amps make excellent high voltage, precision comparators due to their robust input stage, low typical offset, and high slew rate. Previous generation high-voltage op amps often use back-to-back diodes across the inputs to prevent damage to the op amp which greatly limits these op amps to be used as comparators, but the patented input stage of the TLV910x allows the device to have a wide differential voltage between the inputs.

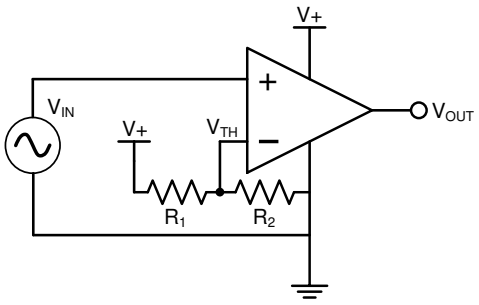


图 8-1. Typical Comparator Application

8.2.1.1 Design Requirements

The primary objective is to design a 15-V precision comparator.

- System supply voltage (V+): 15 V
- Resistor 1 value: 100 kΩ
- Resistor 2 value: 100 kΩ
- Reference threshold voltage (V_{TH}): 7.5 V
- Input voltage range (V_{IN}): 2.5 V – 12.5 V
- Output voltage range (V_{OUT}): 0 V – 15 V

8.2.1.2 Detailed Design Procedure

This noninverting comparator circuit applies the input voltage (V_{IN}) to the noninverting terminal of the op amp. Two resistors (R_1 and R_2) divide the supply voltage (V+) to create a mid-supply threshold voltage (V_{TH}) as calculated in 方程式 1. The circuit is shown in 图 8-1. When V_{IN} is less then V_{TH}, the output voltage transitions to the negative supply and equals the low-level output voltage. When V_{IN} is greater than V_{TH}, the output voltage transitions to the positive supply and equals the high-level output voltage.

In this example, resistor 1 and 2 have been selected to be 100 kΩ, which sets the reference threshold at 7.5 V. However, resistor 1 and 2 can be adjusted to modify the threshold using 方程式 1. The values of resistor 1 and 2 have also been selected to reduce power consumption, but these values can be further increased to reduce power consumption, or reduced to improve noise performance.

$$V_{TH} = \frac{R_2}{R_1 + R_2} \times V_+ \tag{1}$$

8.2.1.3 Application Curve

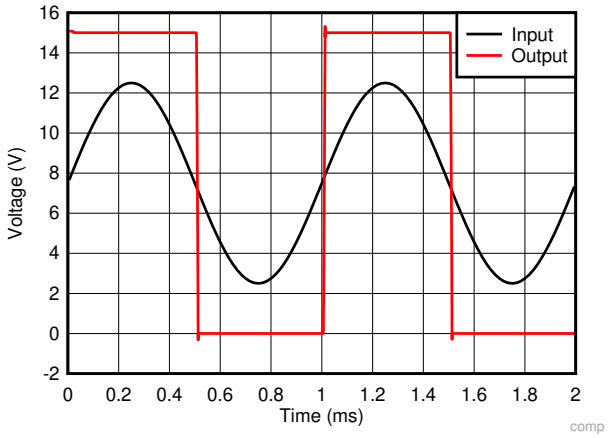


图 8-2. Comparator Output Response to Input Voltage

Copyright © 2021 Texas Instruments Incorporated

9 Power Supply Recommendations

The TLV910x is specified for operation from 2.7 V to 16 V (±1.35 V to ±8 V); many specifications apply from –40°C to 125°C.

CAUTION

Supply voltages larger than 20 V can permanently damage the device; see 节 6.1.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to 节 10.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in 图 10-2, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

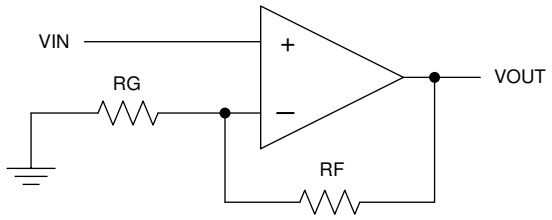


图 10-1. Schematic Representation

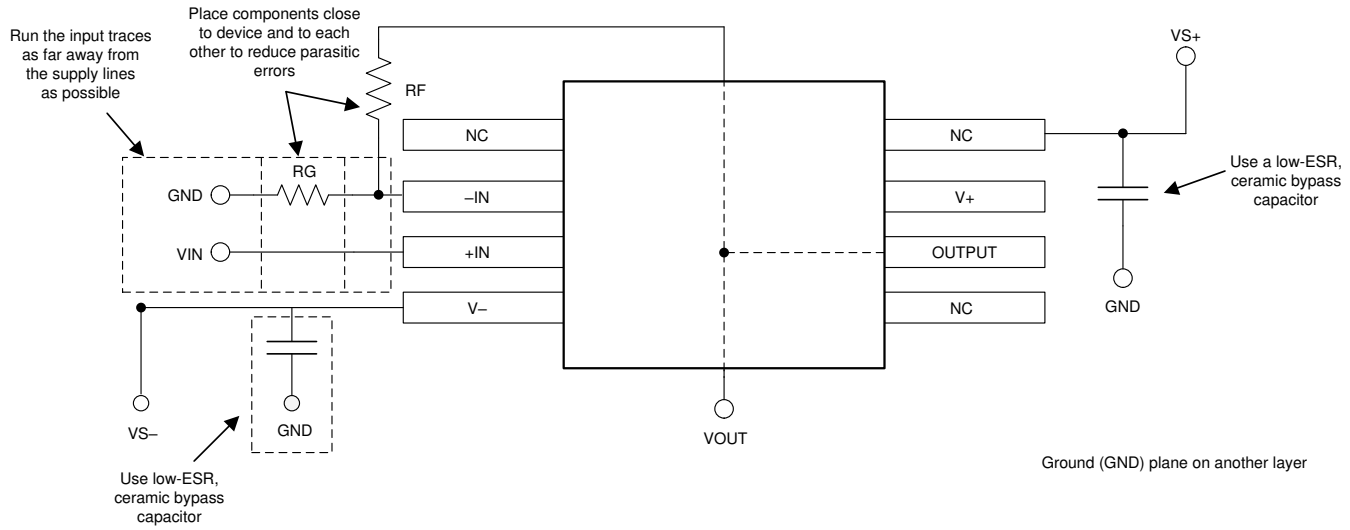


图 10-2. Operational Amplifier Board Layout for Noninverting Configuration

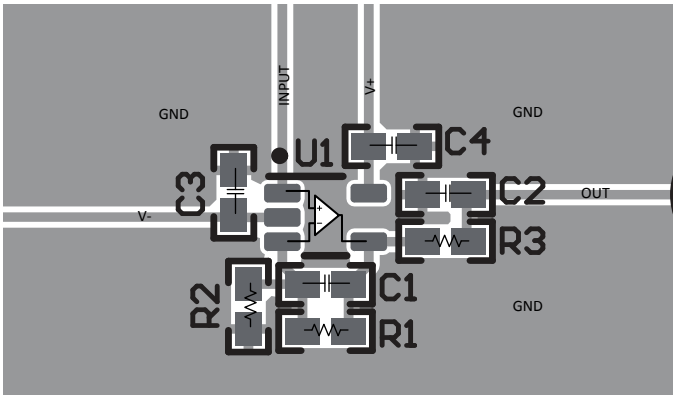


图 10-3. Example Layout for SC70 (DCK) Package

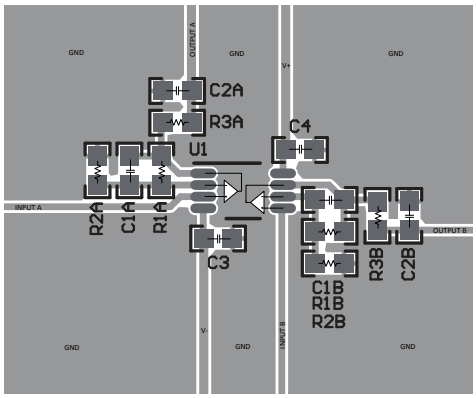


图 10-4. Example Layout for VSSOP-8 (DGK) Package

Copyright © 2021 Texas Instruments Incorporated

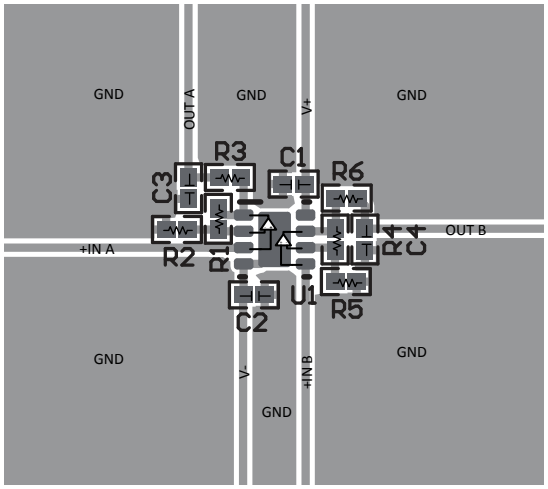


图 10-5. Example Layout for WSON-8 (DSG) Package

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional DC, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.2 Documentation Support

11.2.1 Related Documentation

Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.5 Trademarks

TINA-TI™ are trademarks of Texas Instruments, Inc and DesignSoft, Inc.
TINA™ and DesignSoft™ are trademarks of DesignSoft, Inc.
TI E2E™ is a trademark of Texas Instruments.
Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
所有商标均为其各自所有者的财产。

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

Copyright © 2021 Texas Instruments Incorporated

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (https:www.ti.com/legal/termsofsale.html) 或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021，德州仪器 (TI) 公司

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV9101IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T91V	Samples
TLV9101IDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1FO	Samples
TLV9101SIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T91S	Samples
TLV9102IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T91F	Samples
TLV9102IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2HBT	Samples
TLV9102IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T9102D	Samples
TLV9102IDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T912	Samples
TLV9102IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T9102P	Samples
TLV9102SIDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T910	Samples
TLV9102SIRUGR	ACTIVE	X2QFN	RUG	10	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	HBF	Samples
TLV9104IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV9104D	Samples
TLV9104IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	(PTL91PW, TLV91PW)	Samples
TLV9104IRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		T91RT	Samples
TLV9104IRUCR	ACTIVE	QFN	RUC	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	FOF	Samples
TLV9104SIRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T9104S	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

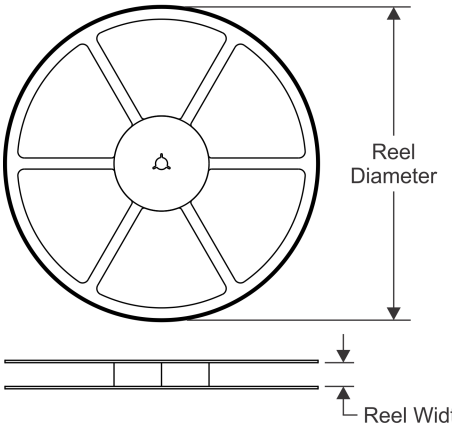
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

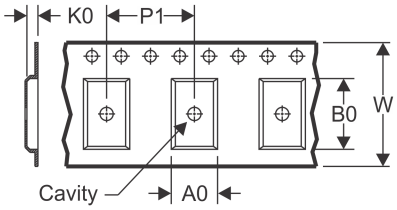
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

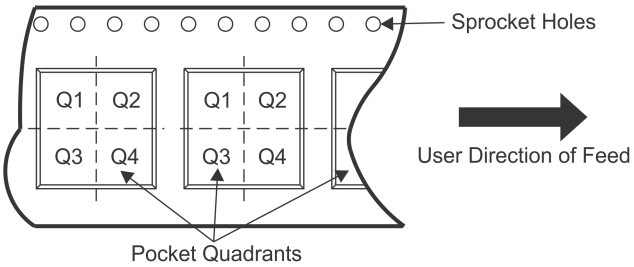


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

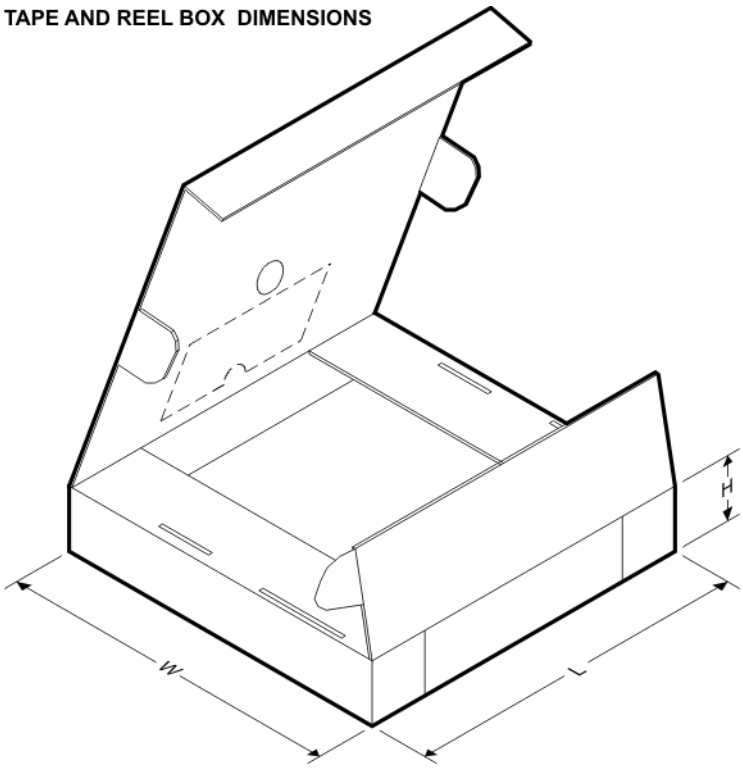
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9101IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9101IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV9101SIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9102IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9102IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9102IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9102IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV9102IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV9102SIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9102SIRUGR	X2QFN	RUG	10	3000	178.0	8.4	1.75	2.25	0.56	4.0	8.0	Q1
TLV9104IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV9104IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV9104IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV9104IRUCR	QFN	RUC	14	3000	180.0	9.5	2.16	2.16	0.5	4.0	8.0	Q2
TLV9104SIRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

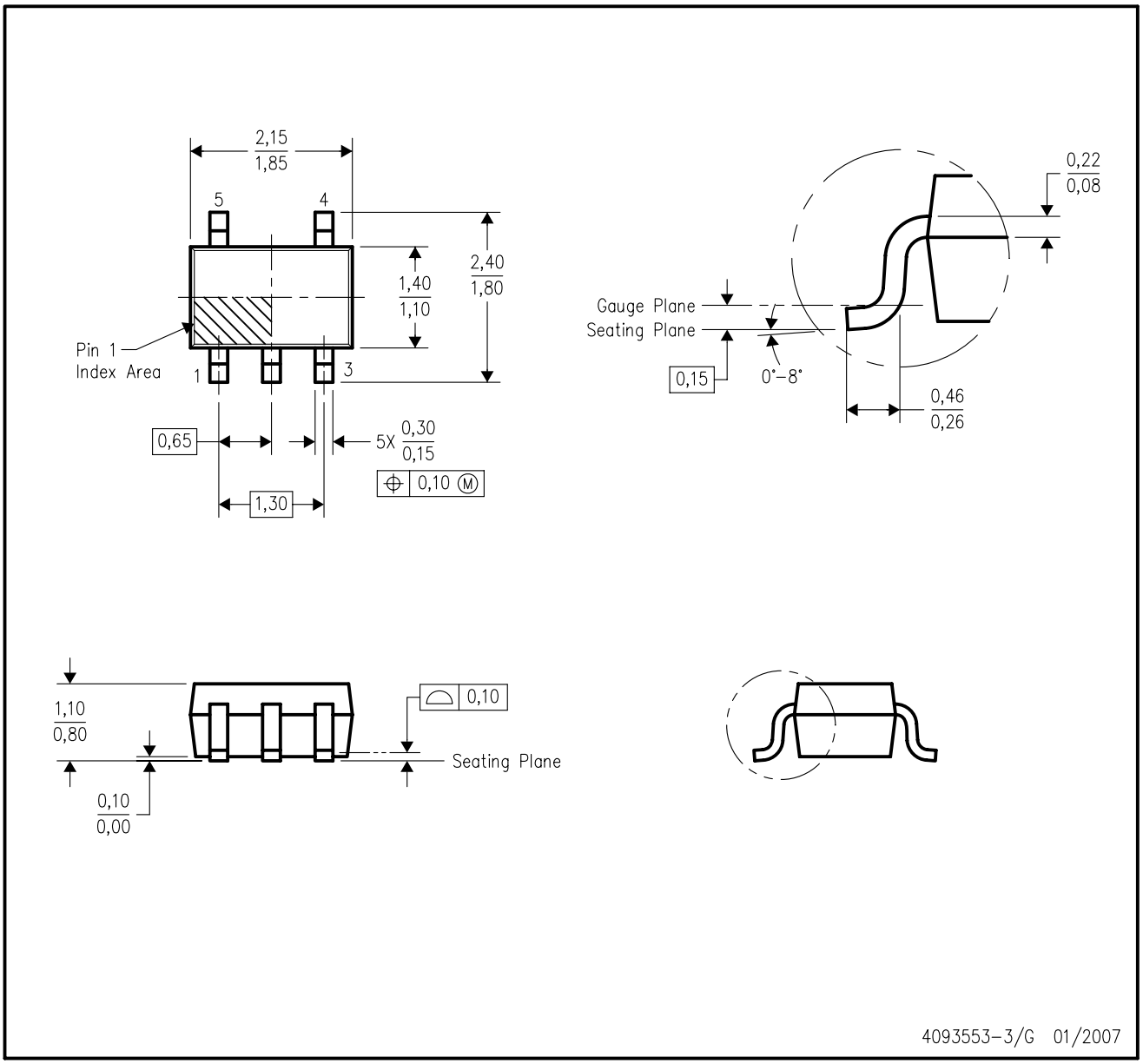
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

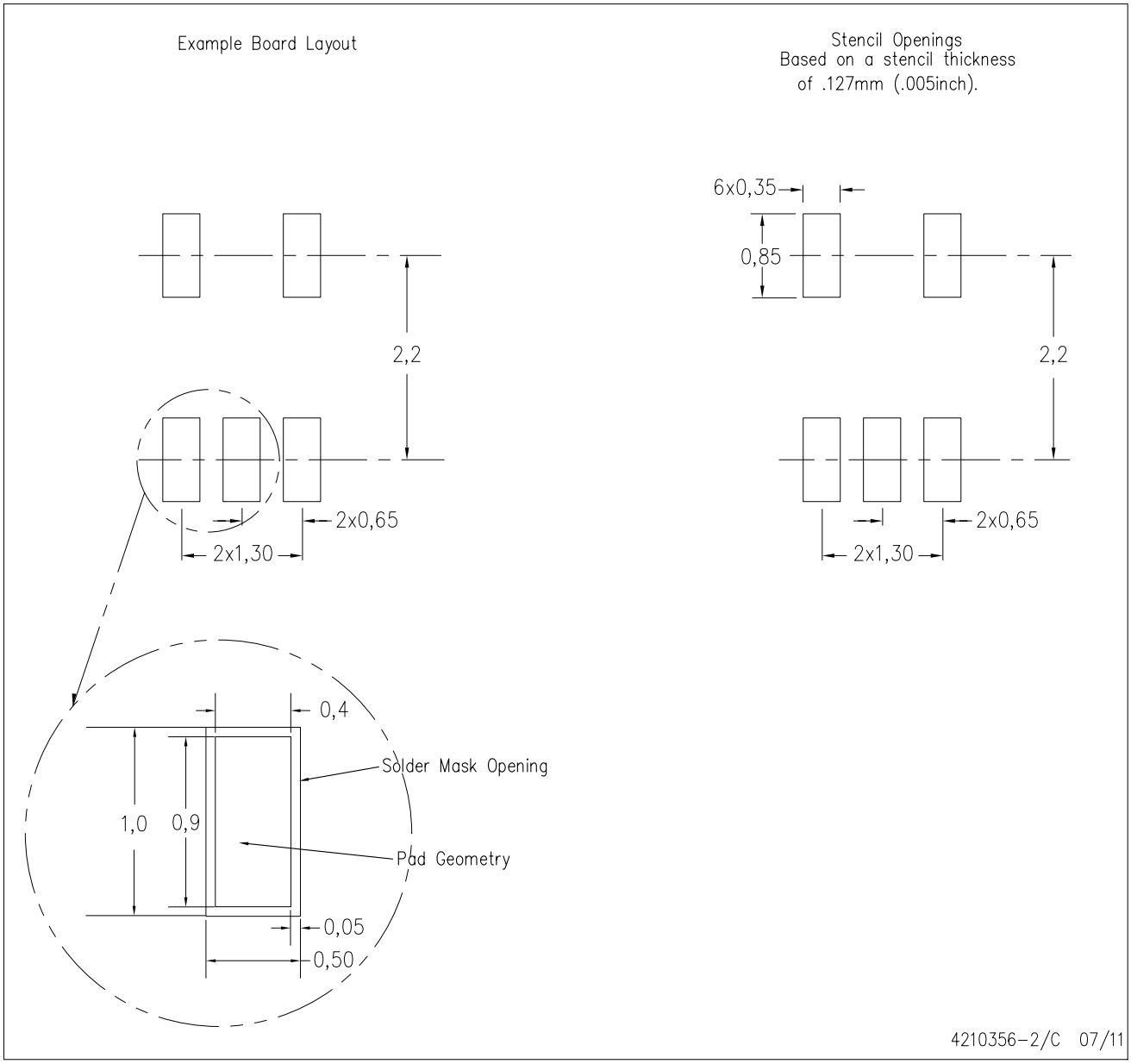
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9101IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9101IDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TLV9101SIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV9102IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV9102IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV9102IDR	SOIC	D	8	2500	853.0	449.0	35.0
TLV9102IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TLV9102IPWR	TSSOP	PW	8	2000	853.0	449.0	35.0
TLV9102SIDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TLV9102SIRUGR	X2QFN	RUG	10	3000	205.0	200.0	33.0
TLV9104IDR	SOIC	D	14	2500	853.0	449.0	35.0
TLV9104IPWR	TSSOP	PW	14	2000	366.0	364.0	50.0
TLV9104IRTER	WQFN	RTE	16	3000	360.0	360.0	36.0
TLV9104IRUCR	QFN	RUC	14	3000	205.0	200.0	30.0
TLV9104SIRTER	WQFN	RTE	16	3000	360.0	360.0	36.0

DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE

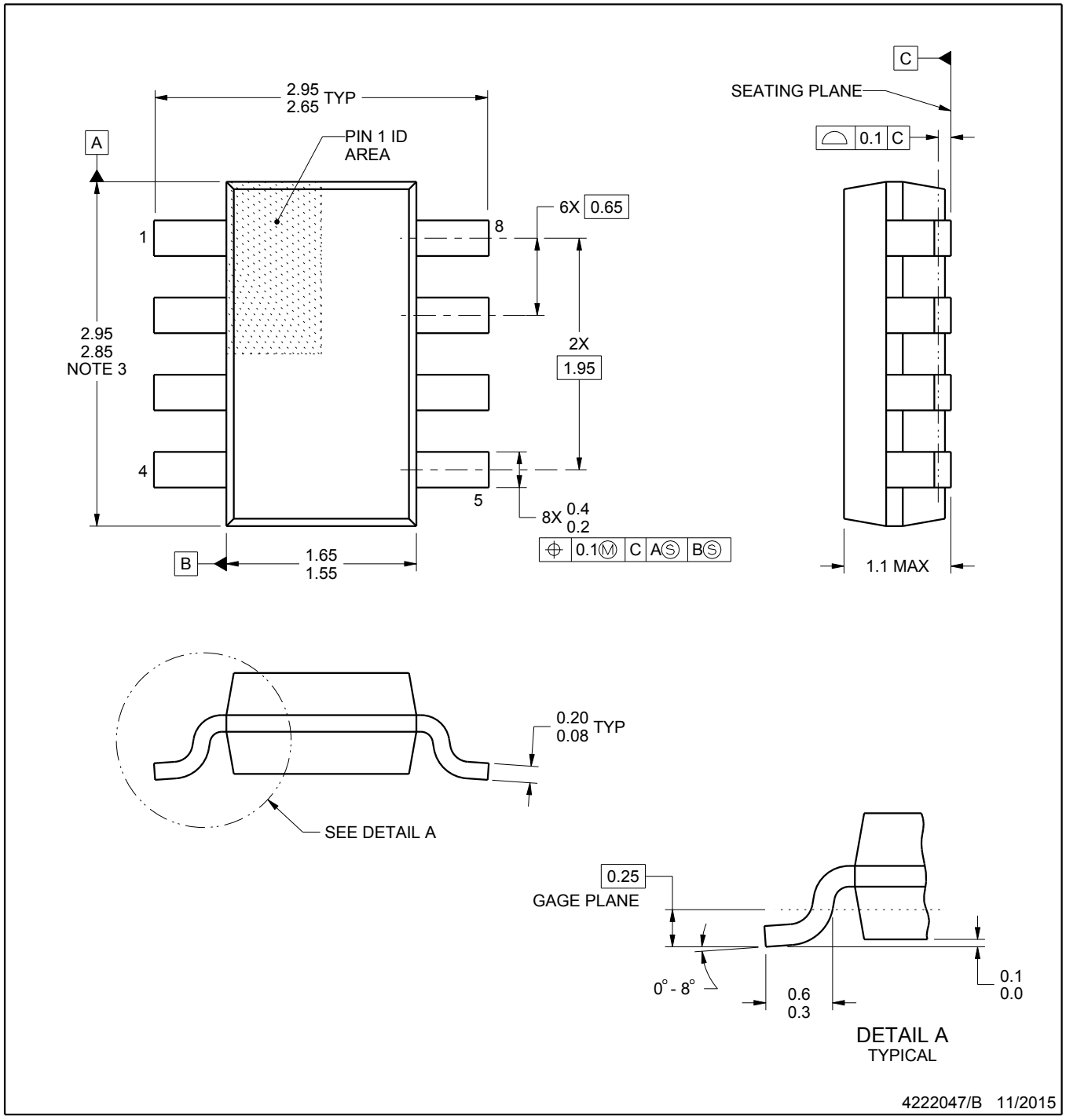


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R-PDSO-G5) PLASTIC SMALL OUTLINE

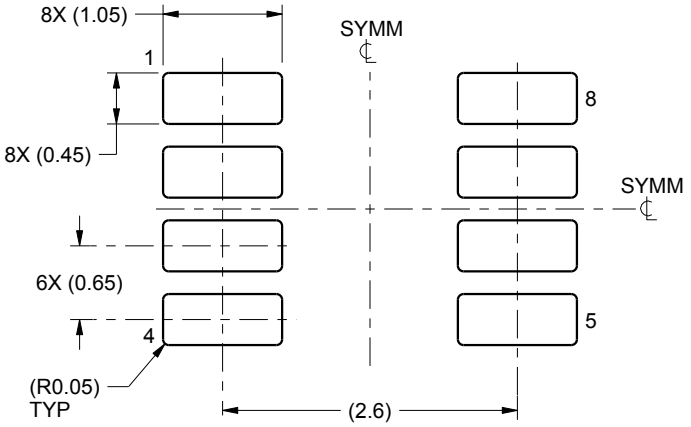


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

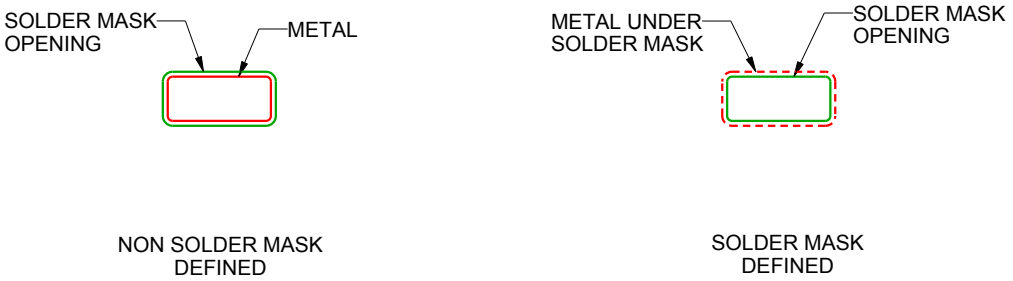


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X

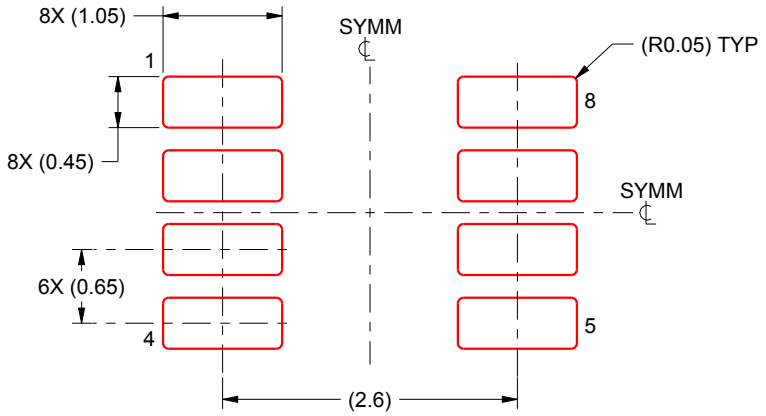


SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

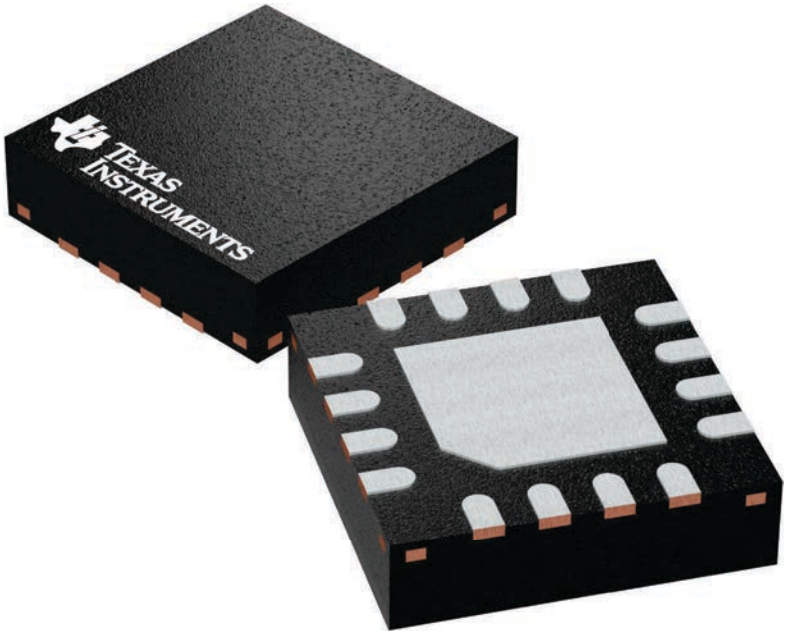
RTE 16

WQFN - 0.8 mm max height

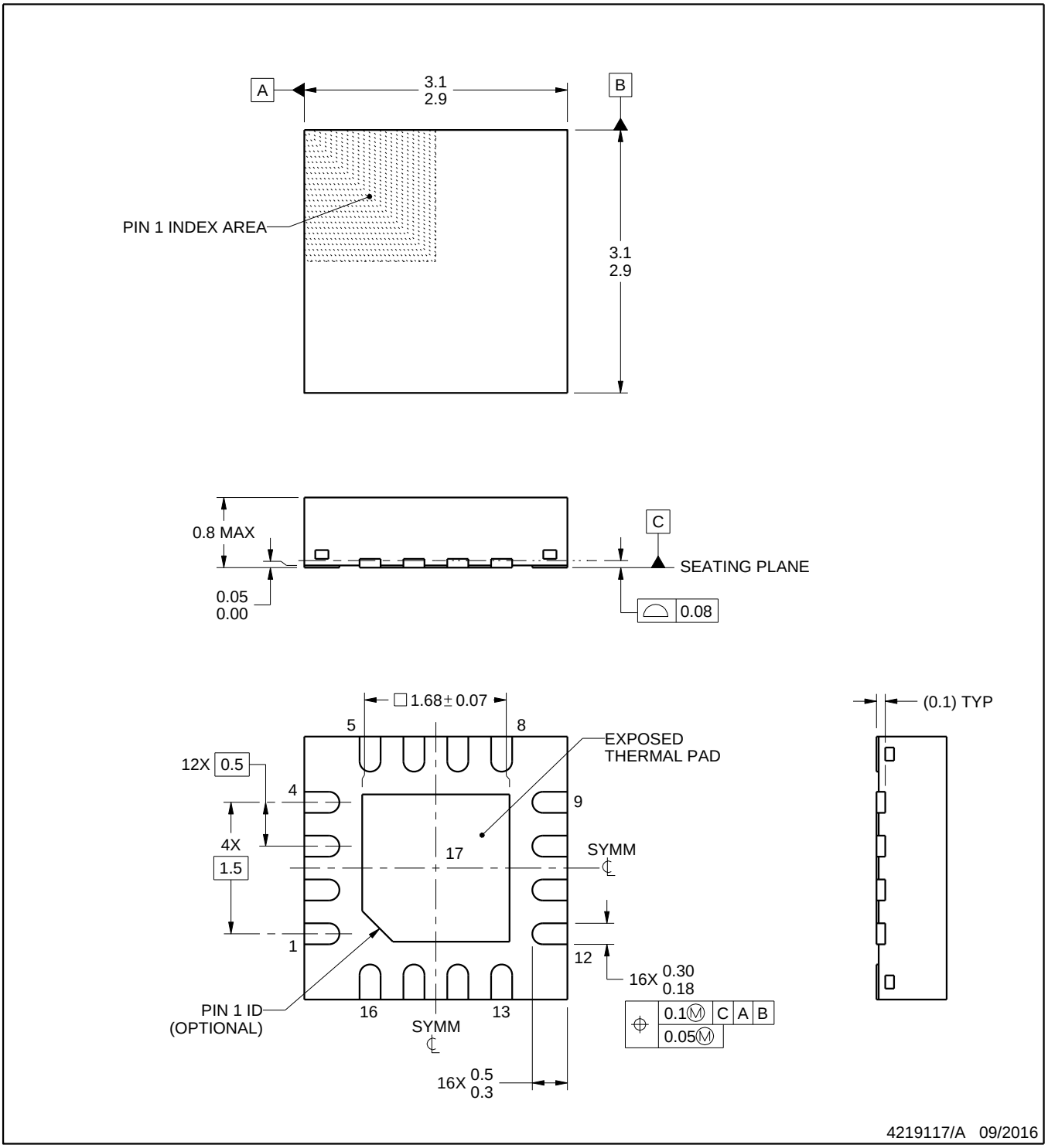
3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

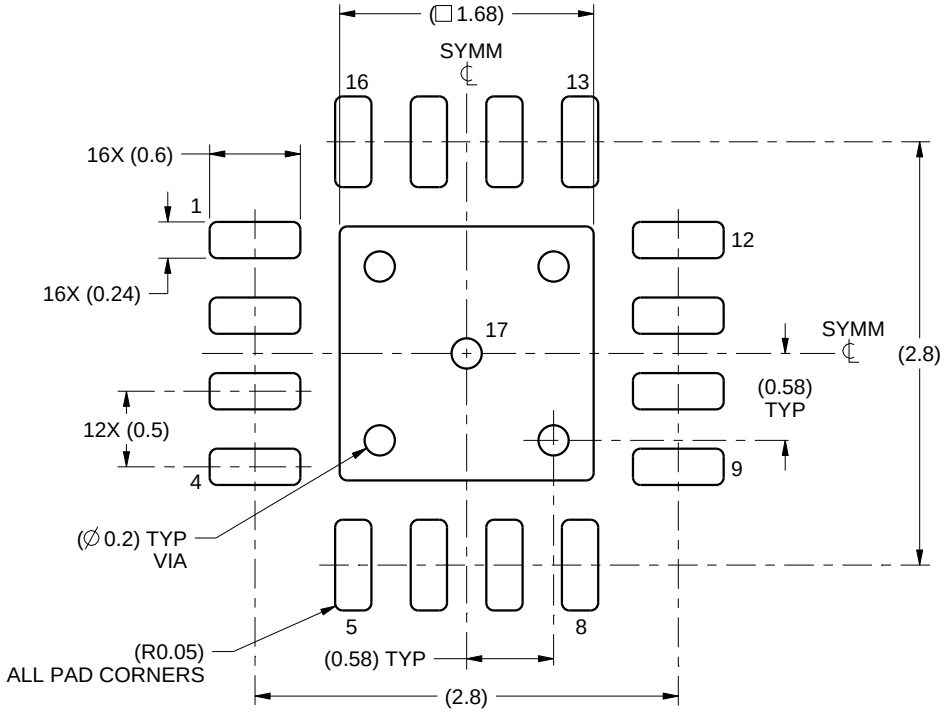


4225944/A

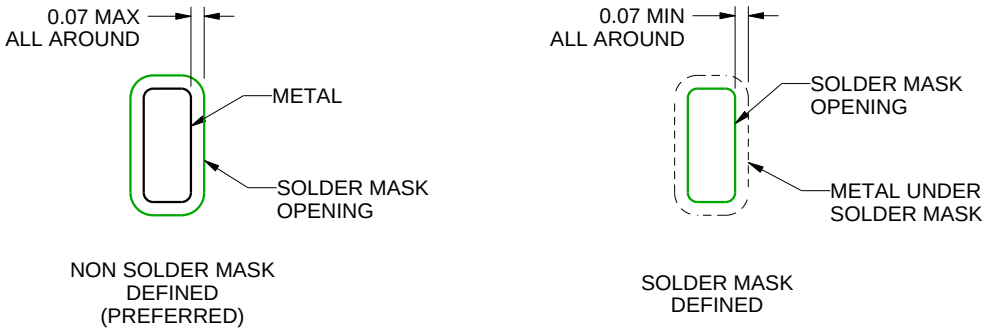


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

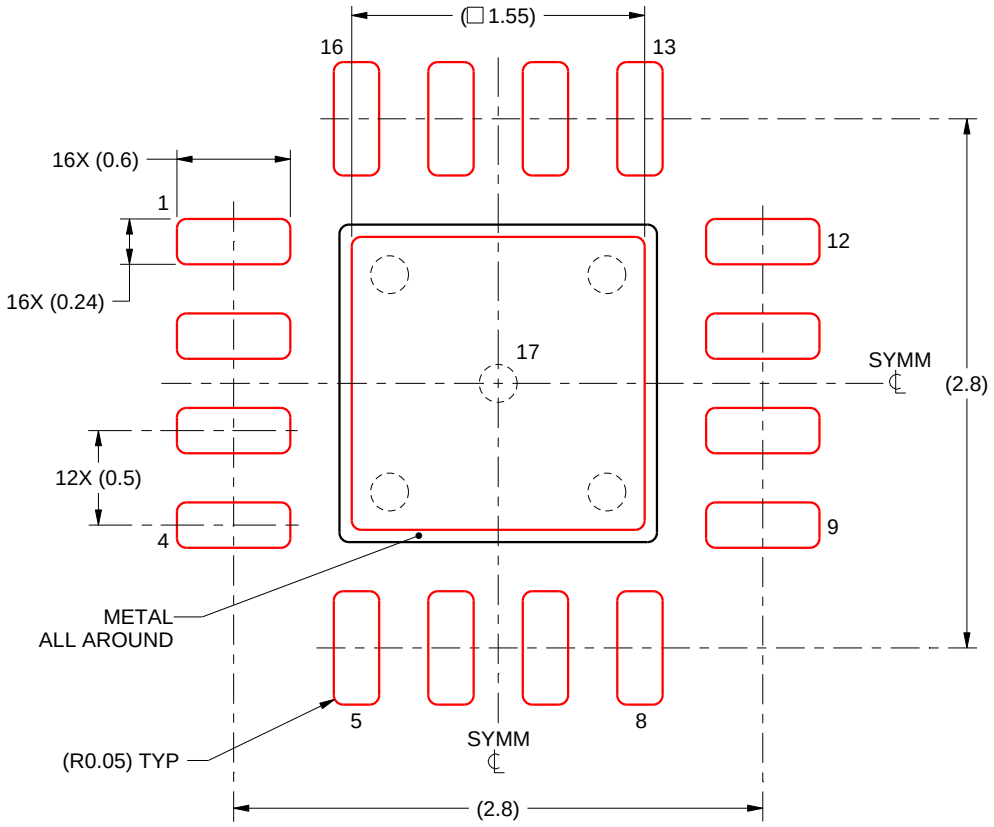


SOLDER MASK DETAILS

4219117/A 09/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



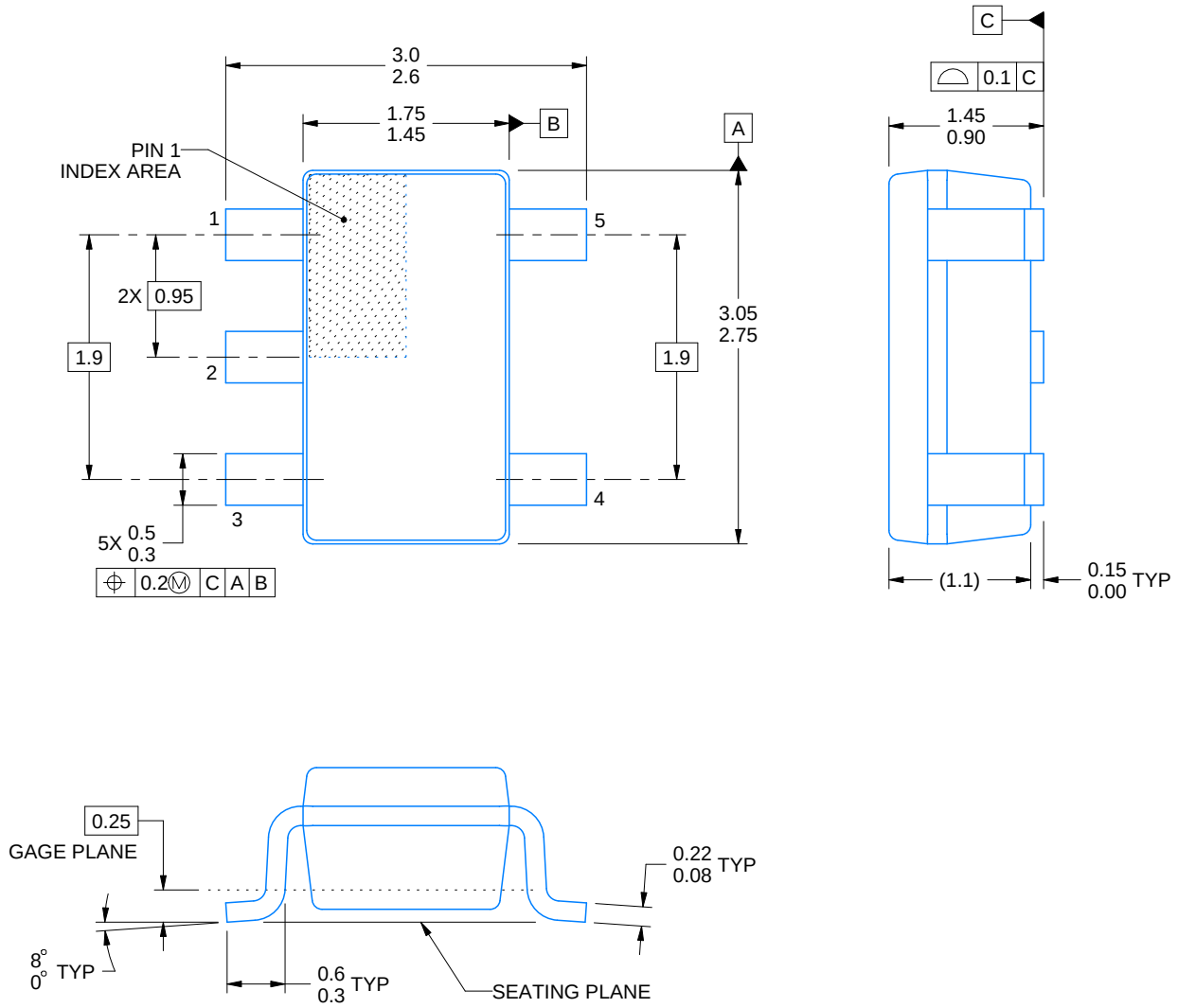
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/A 09/2016

NOTES: (continued)

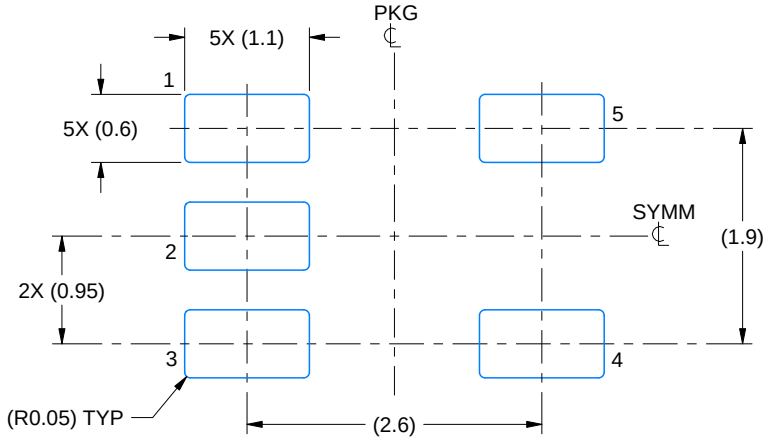
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



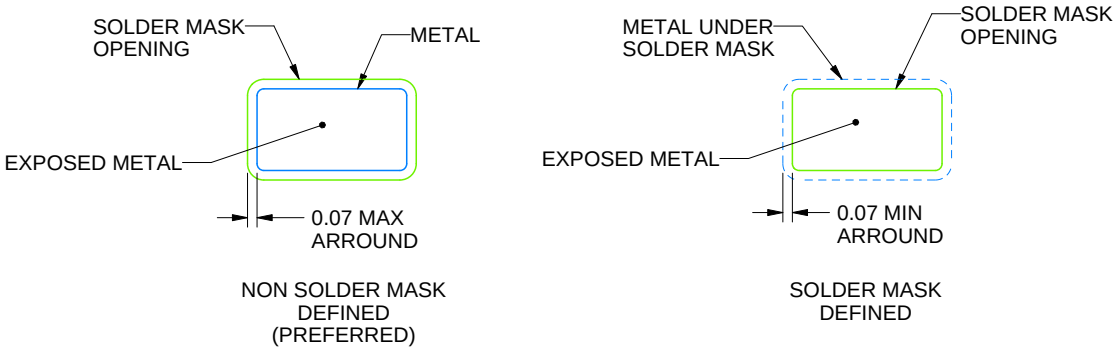
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

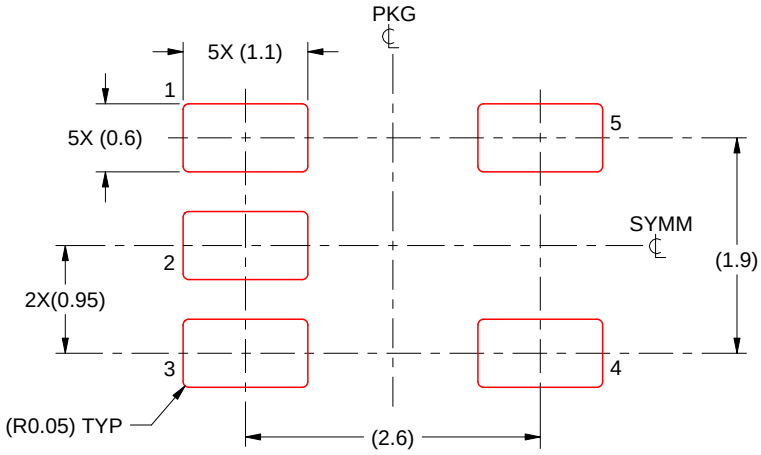


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

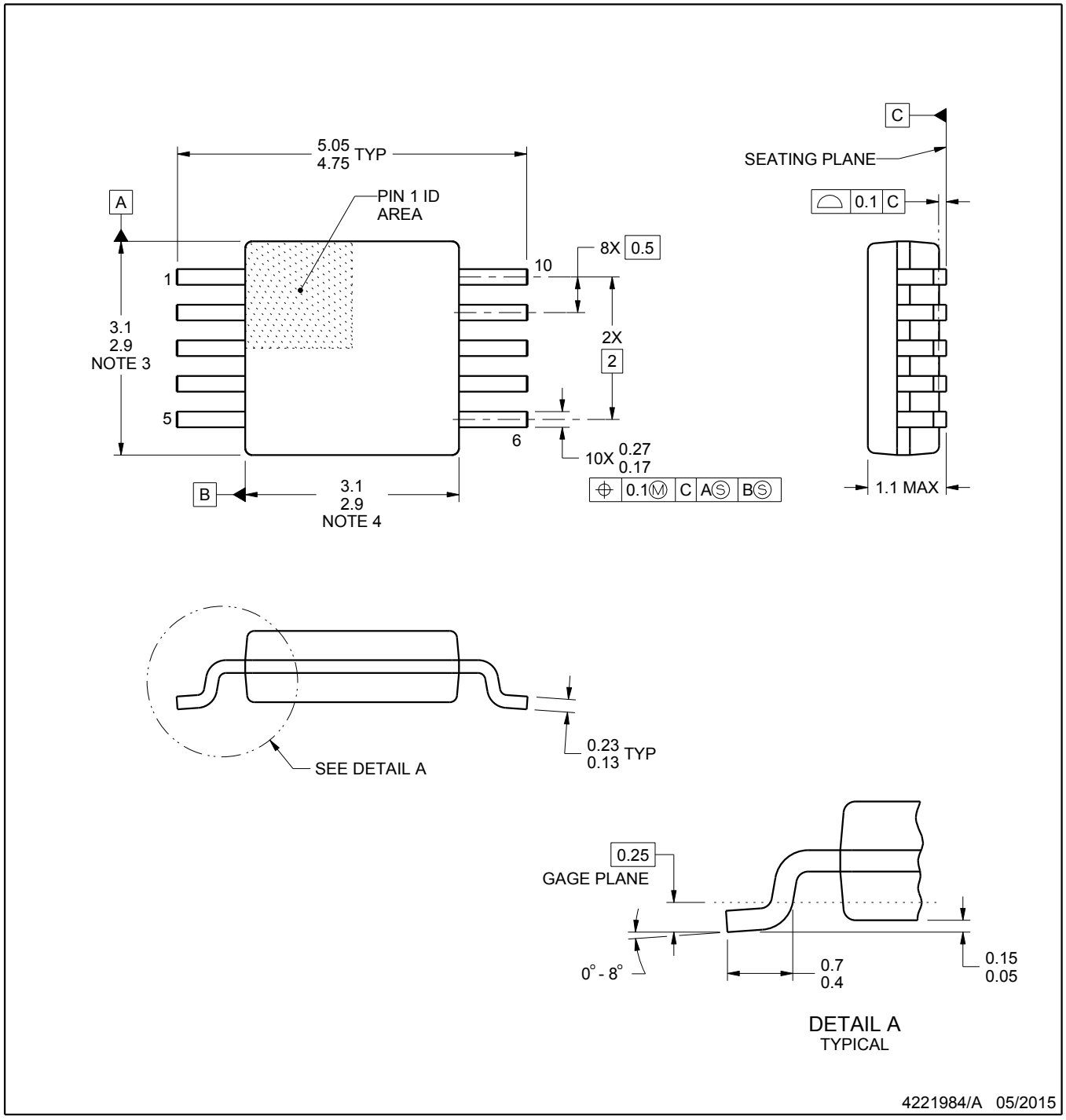


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

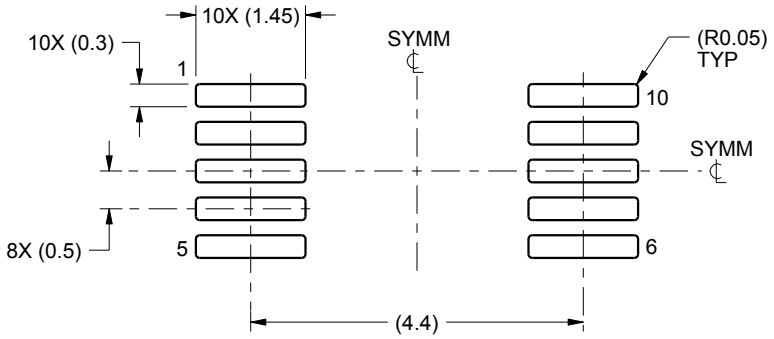
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

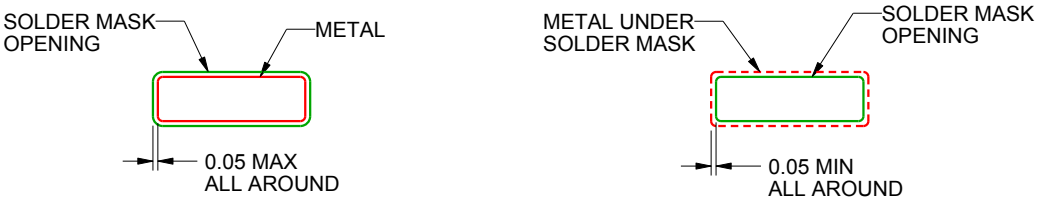


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK
DEFINED

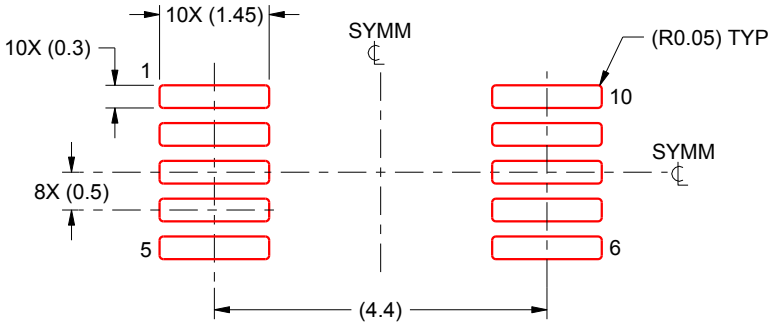
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



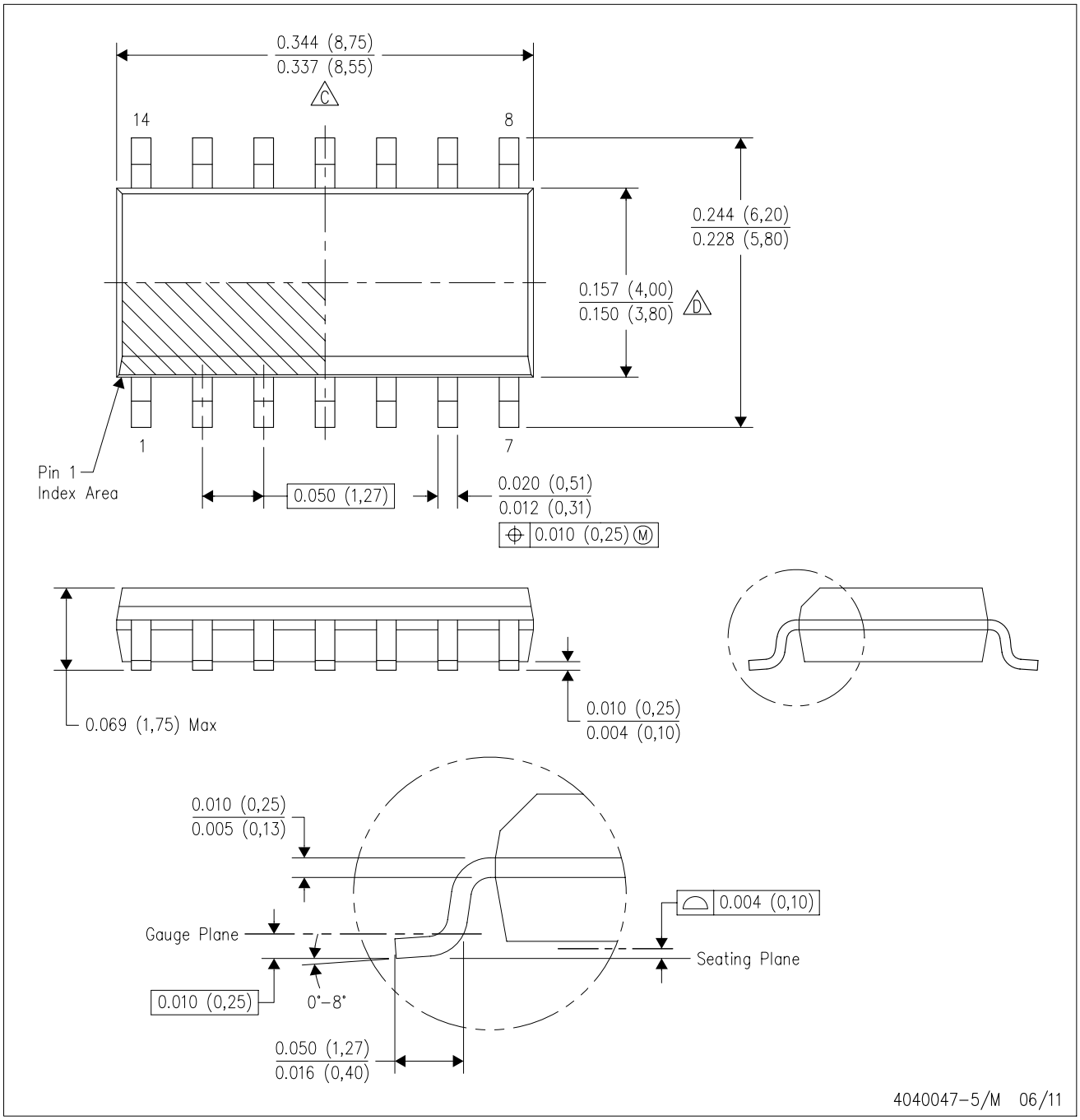
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

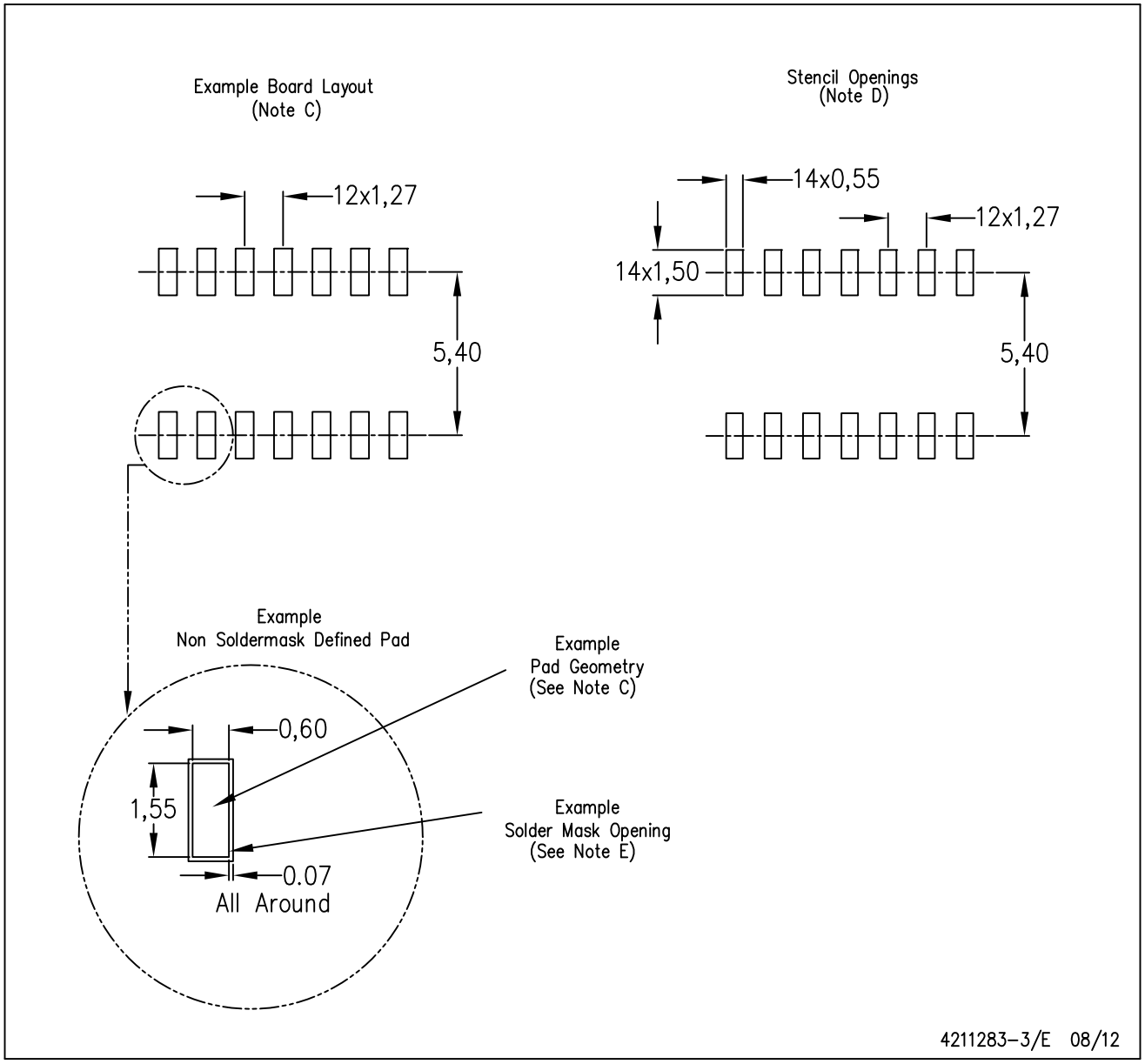
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



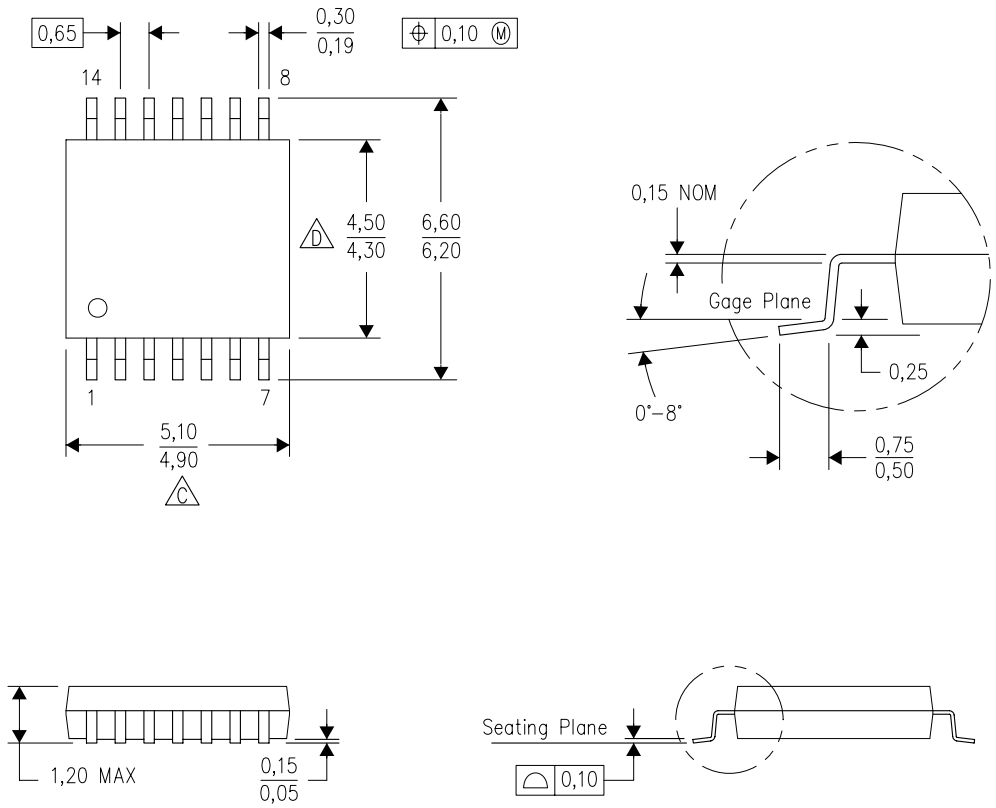
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



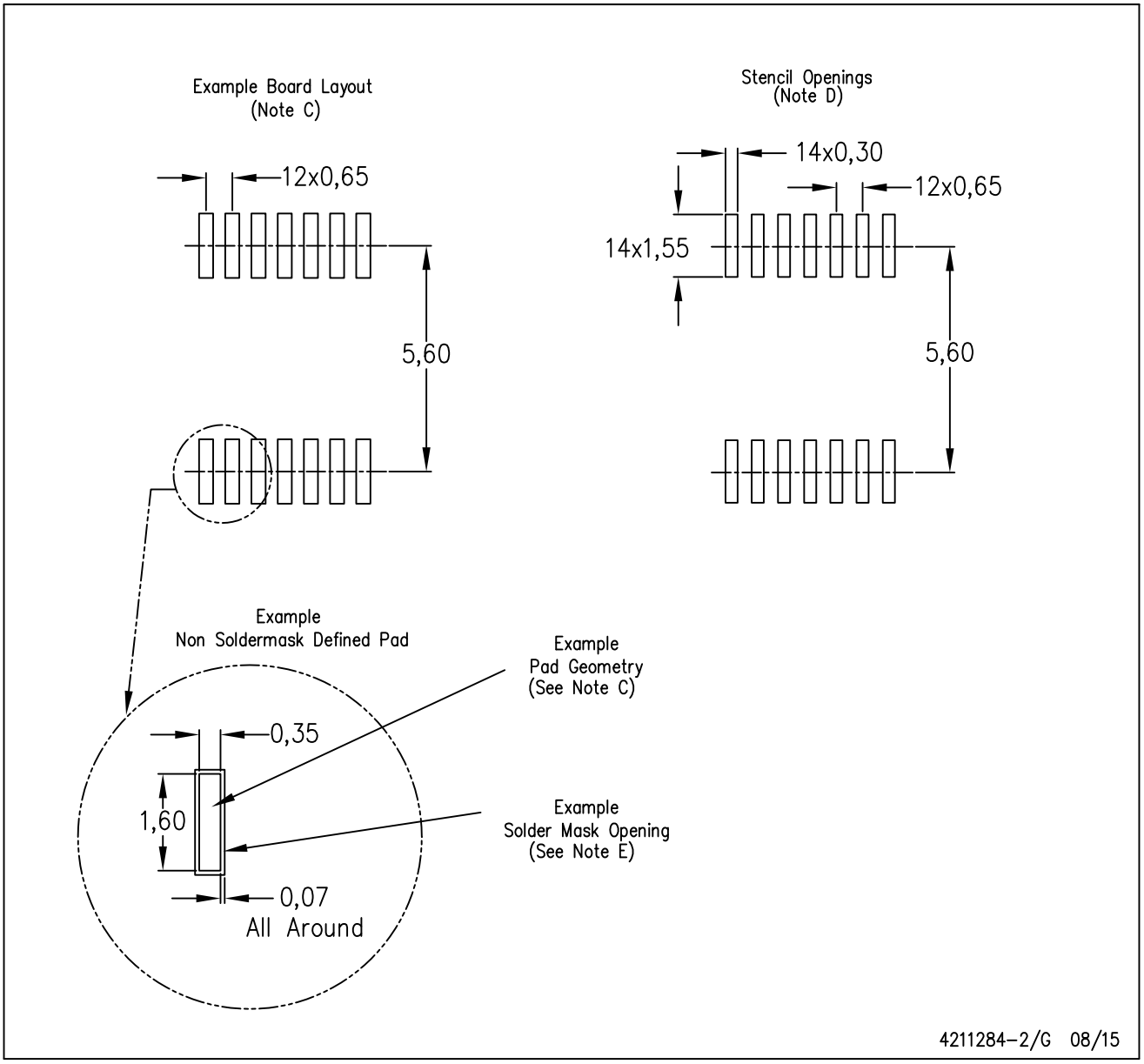
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



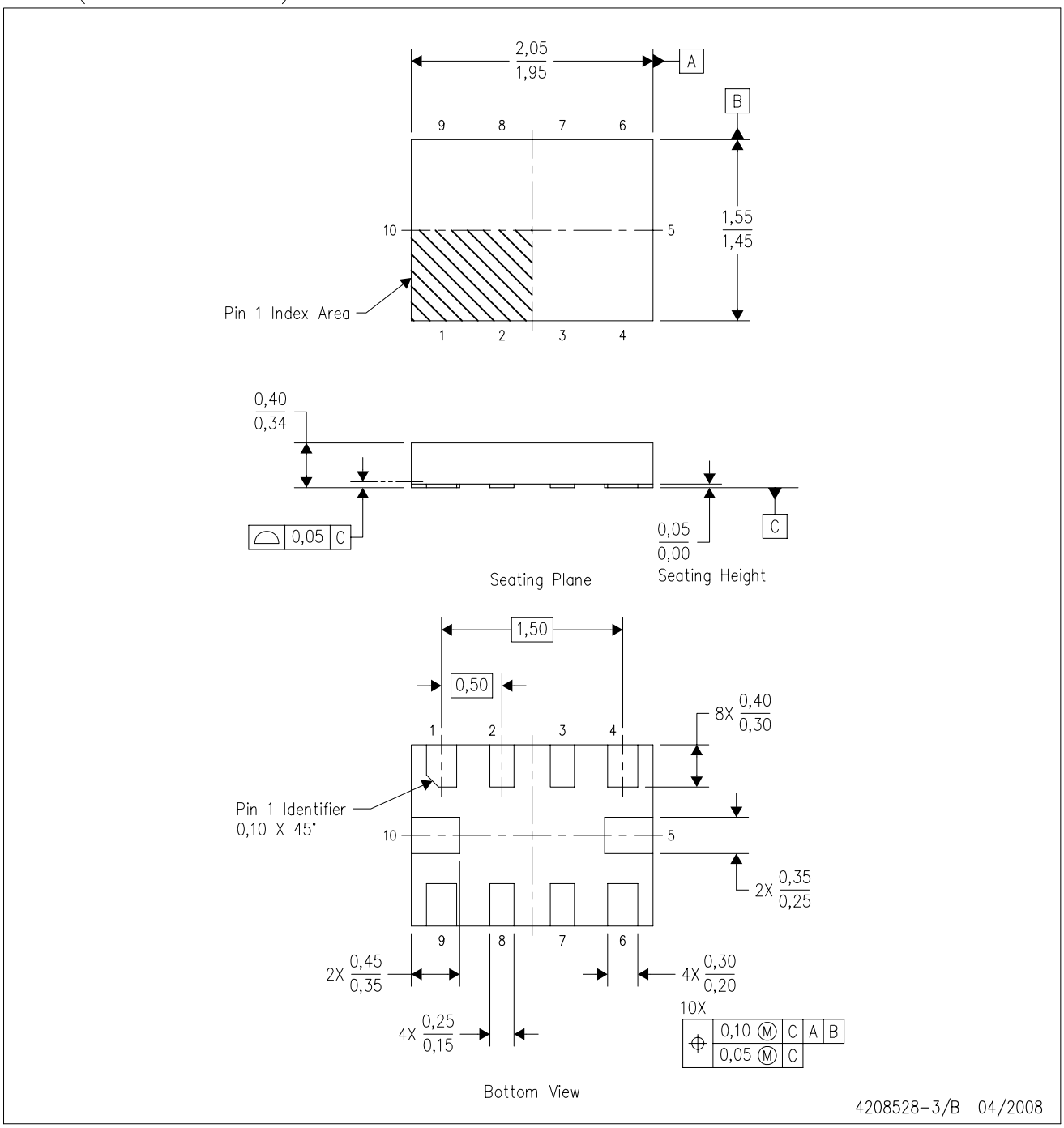
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



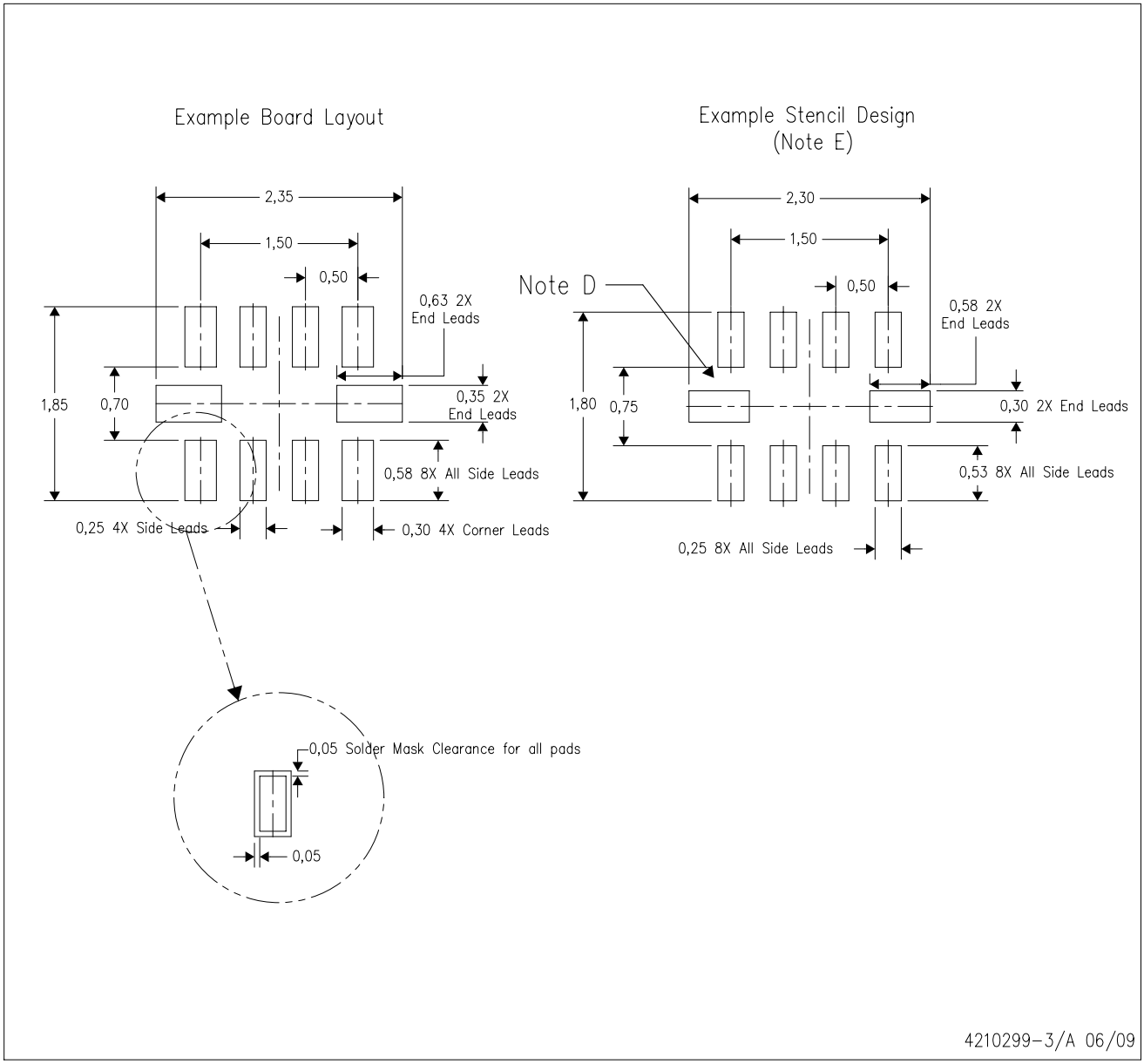
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RUG (R–PQFP–N10) PLASTIC QUAD FLATPACK

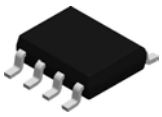


NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2EFD.

RUG (R–PQFP–N10)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

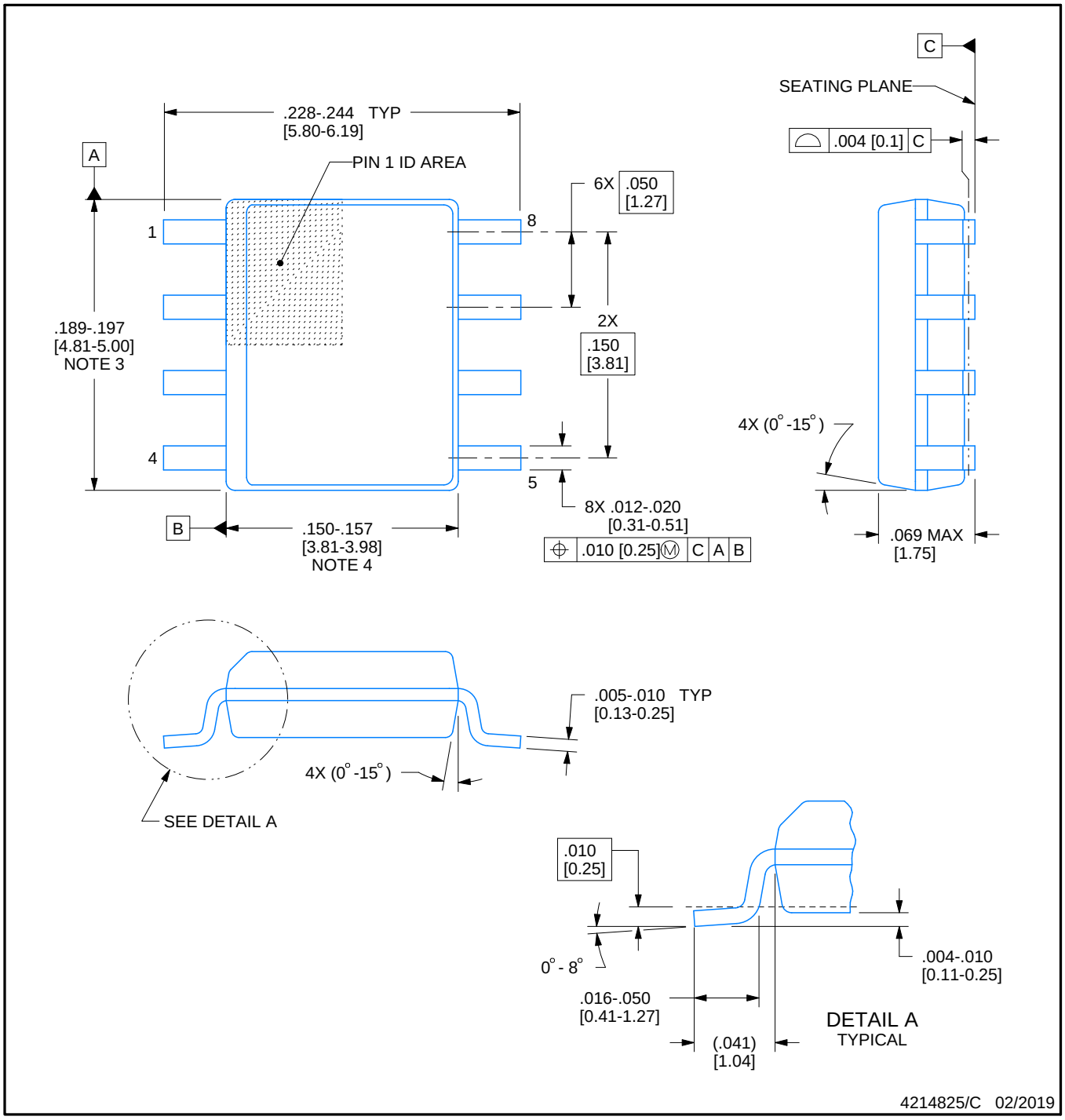


PACKAGE OUTLINE

D0008A

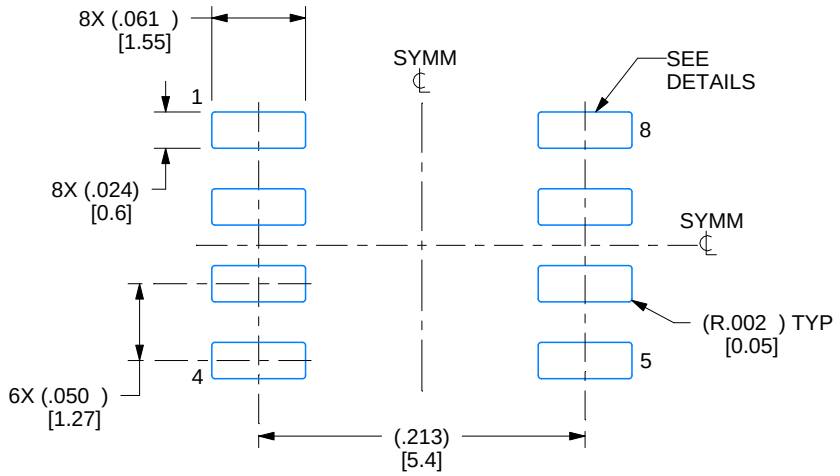
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

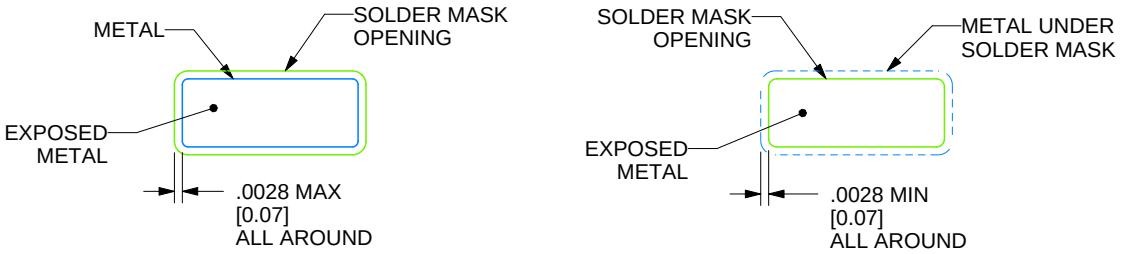


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

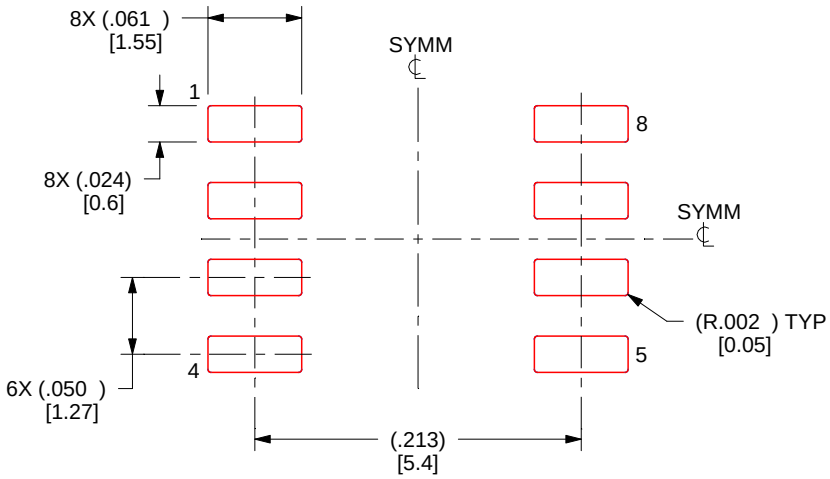


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

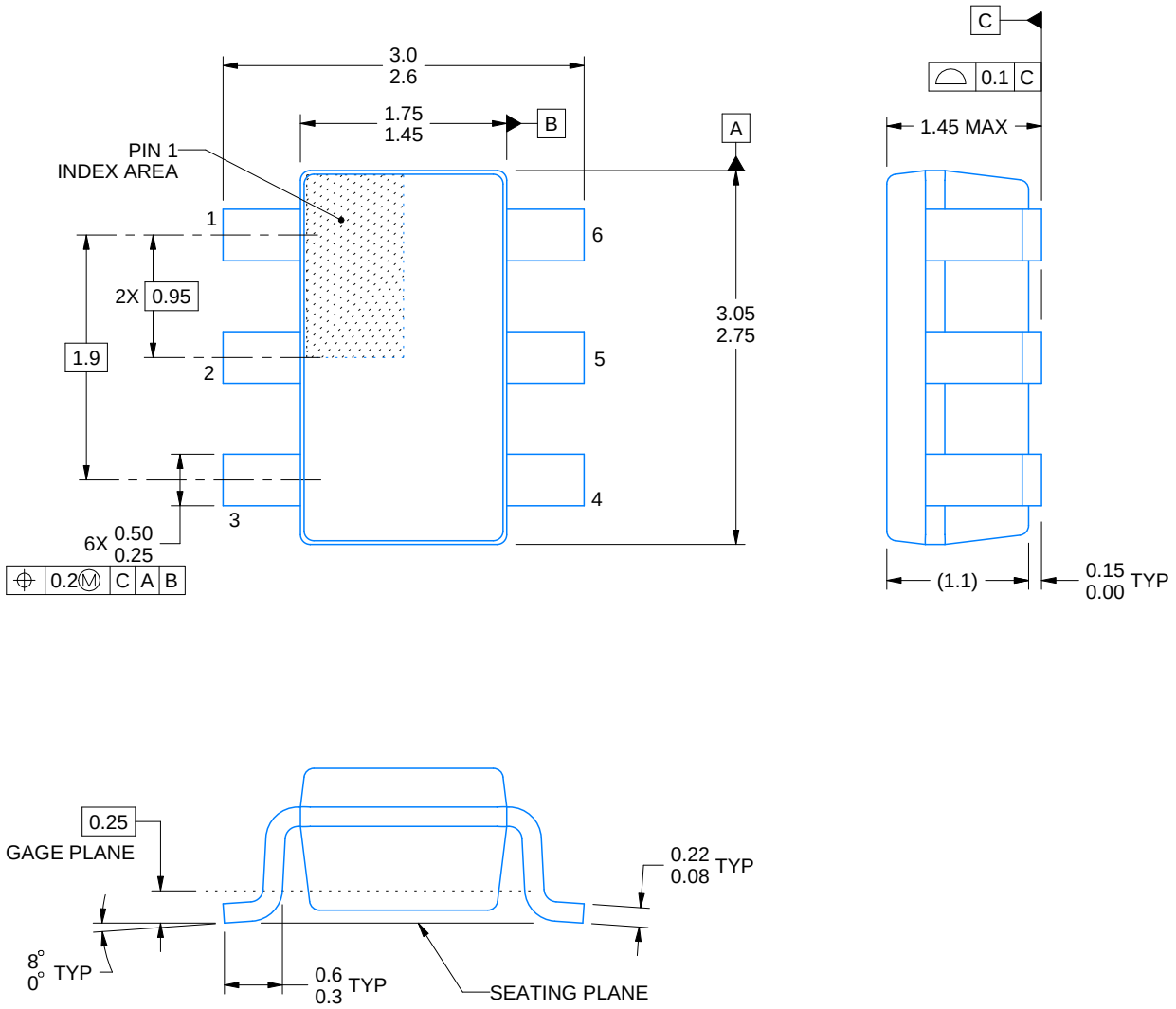


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

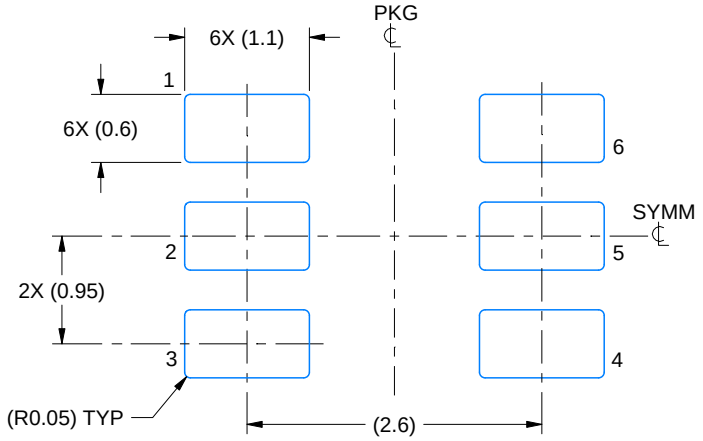
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



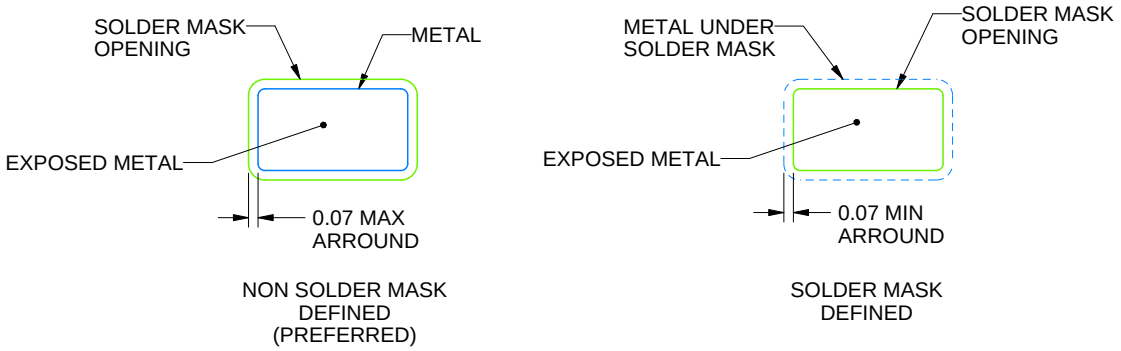
4214840/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

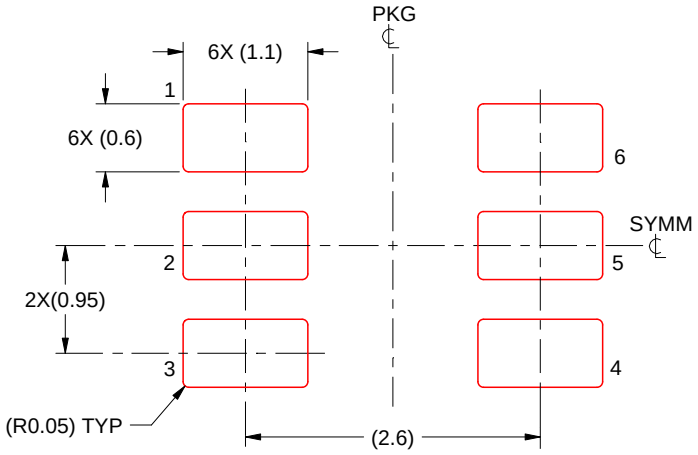


SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



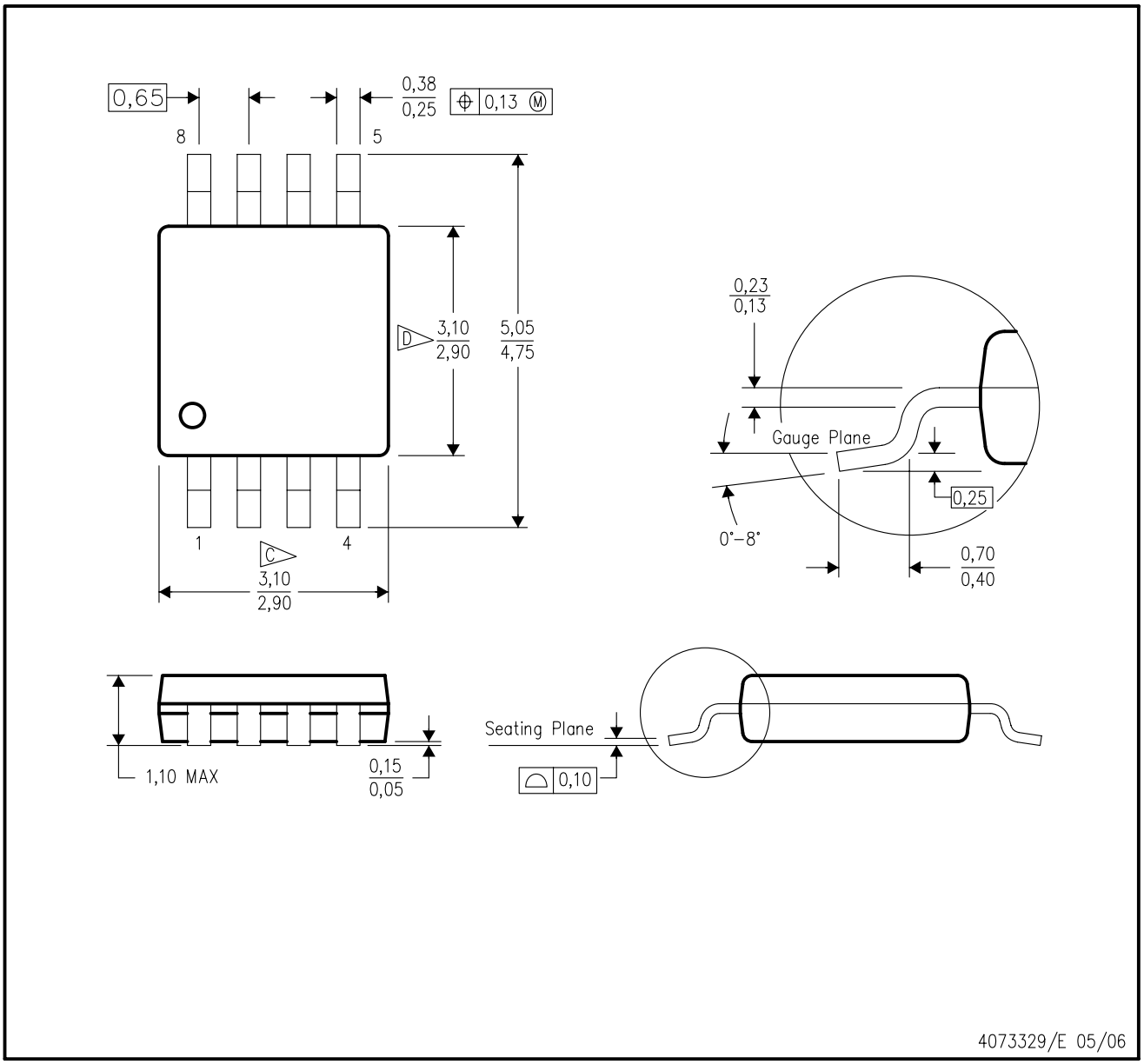
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

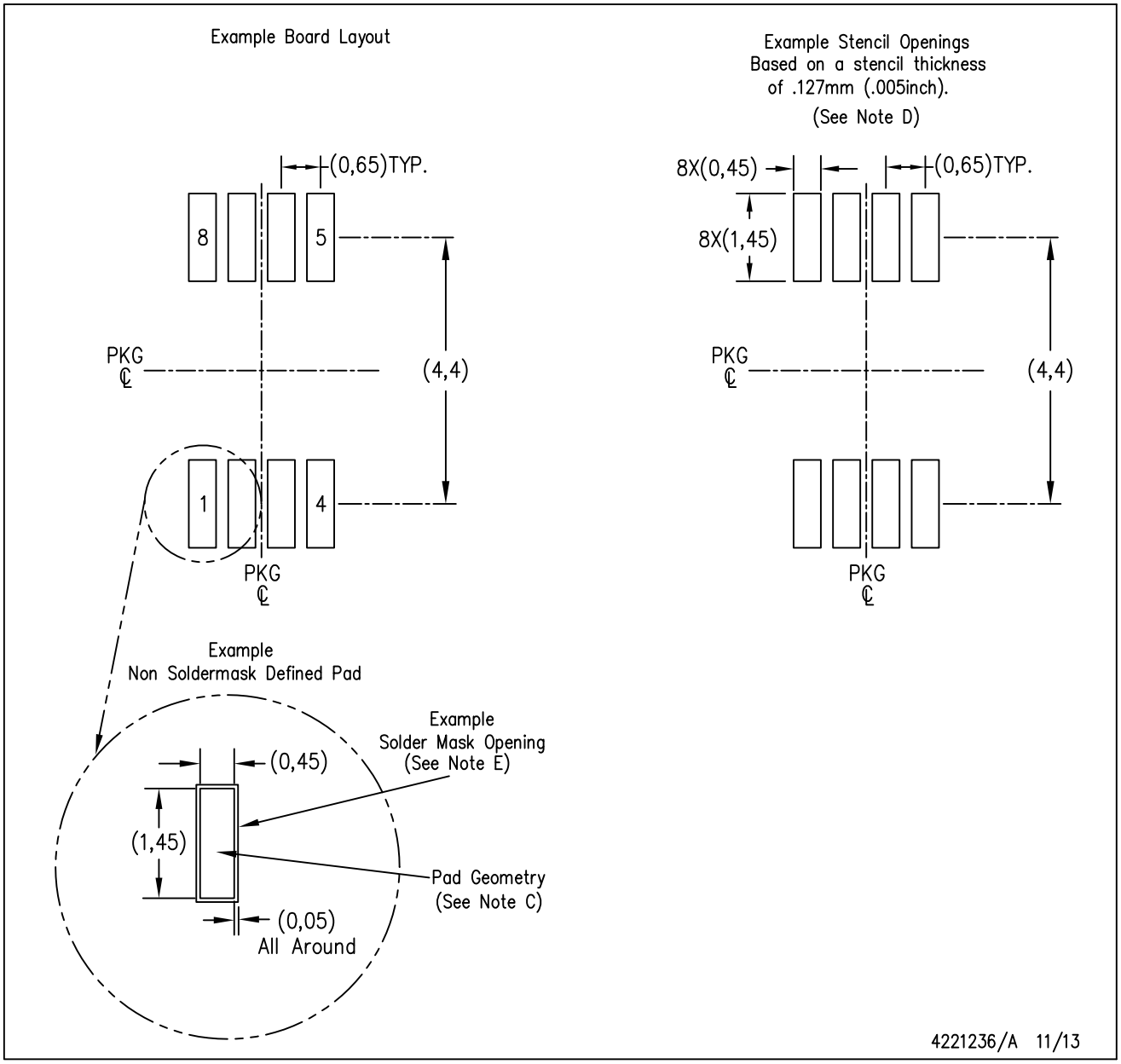
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

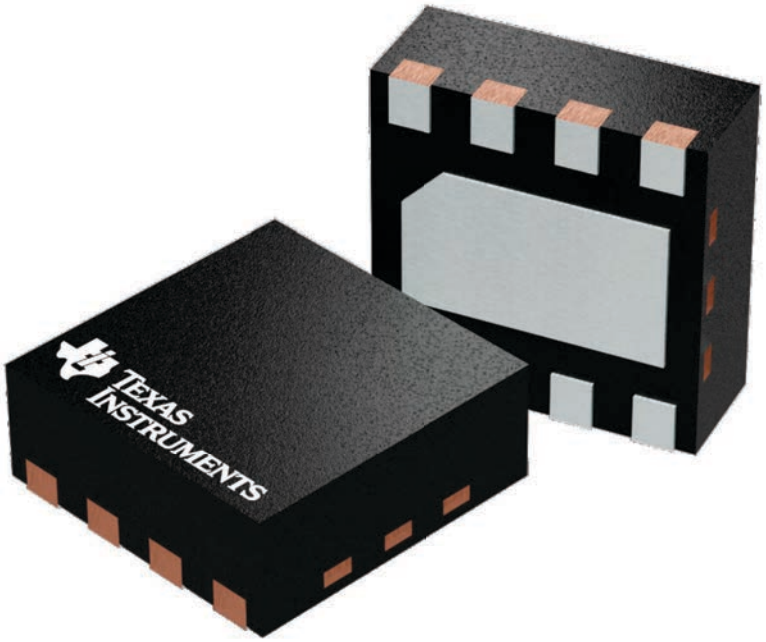
DSG 8

WSON - 0.8 mm max height

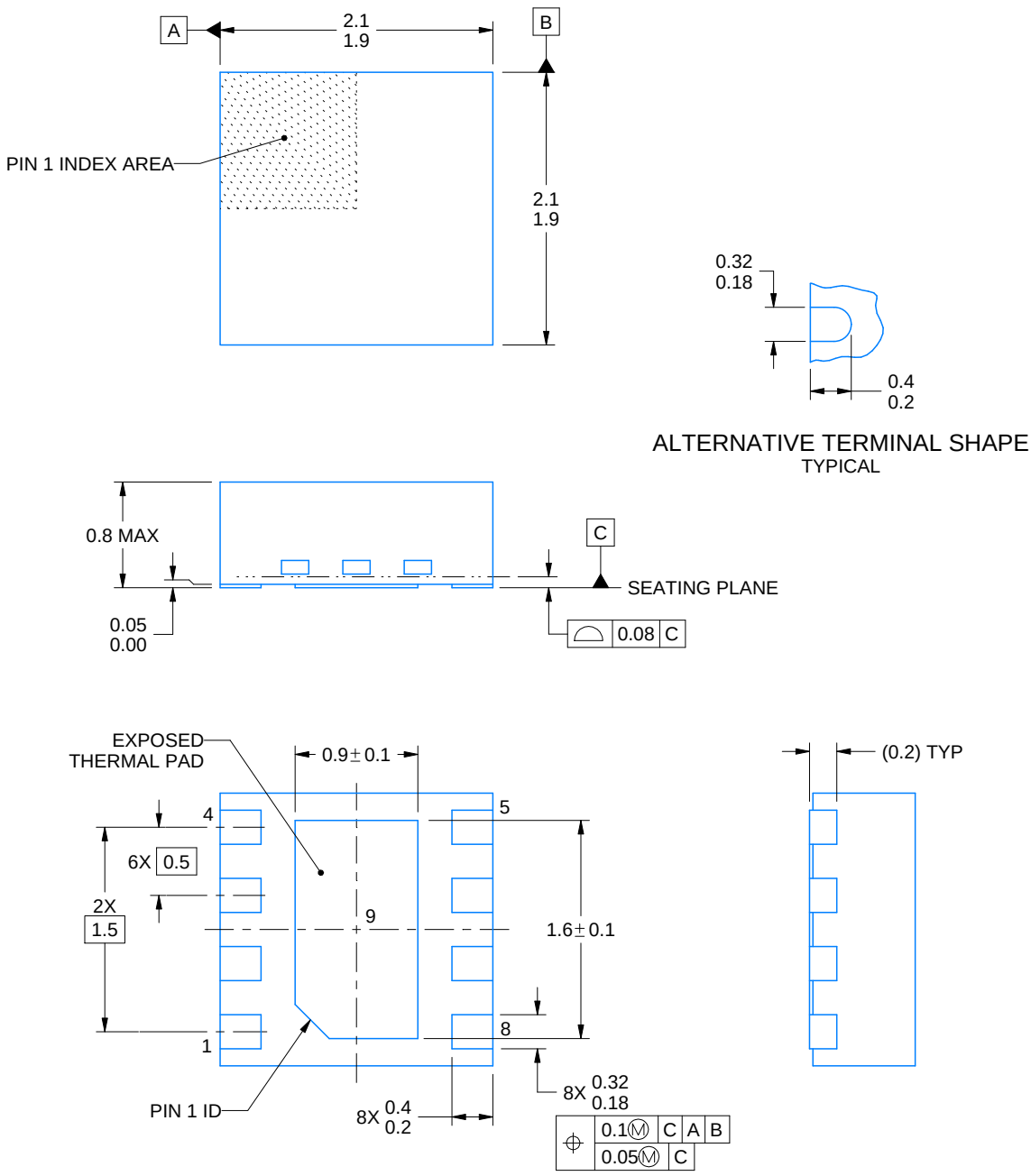
2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

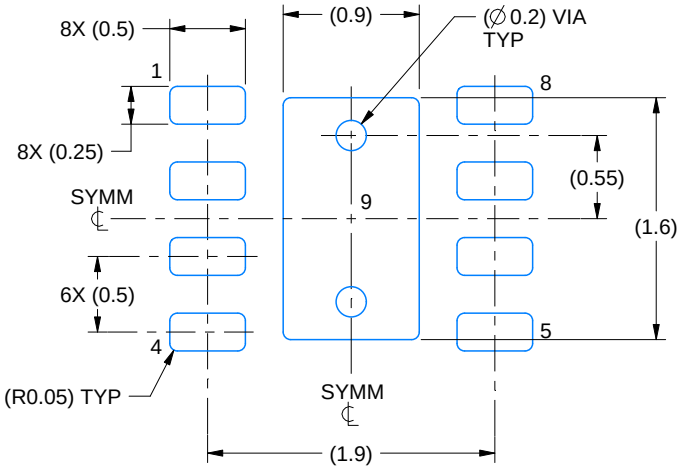


4224783/A

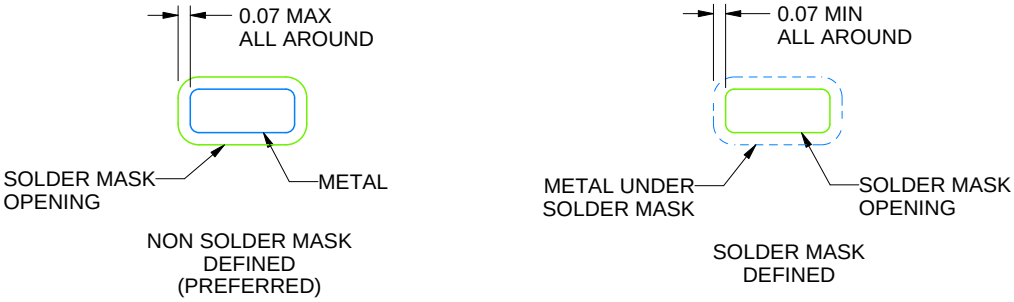


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

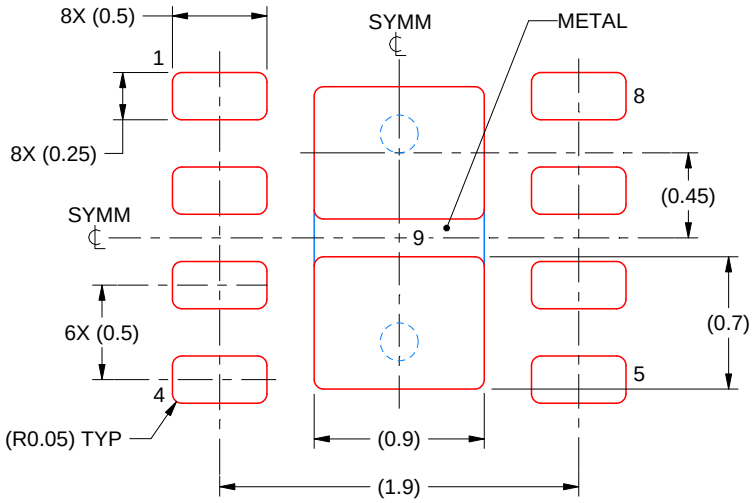


SOLDER MASK DETAILS

4218900/D 04/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



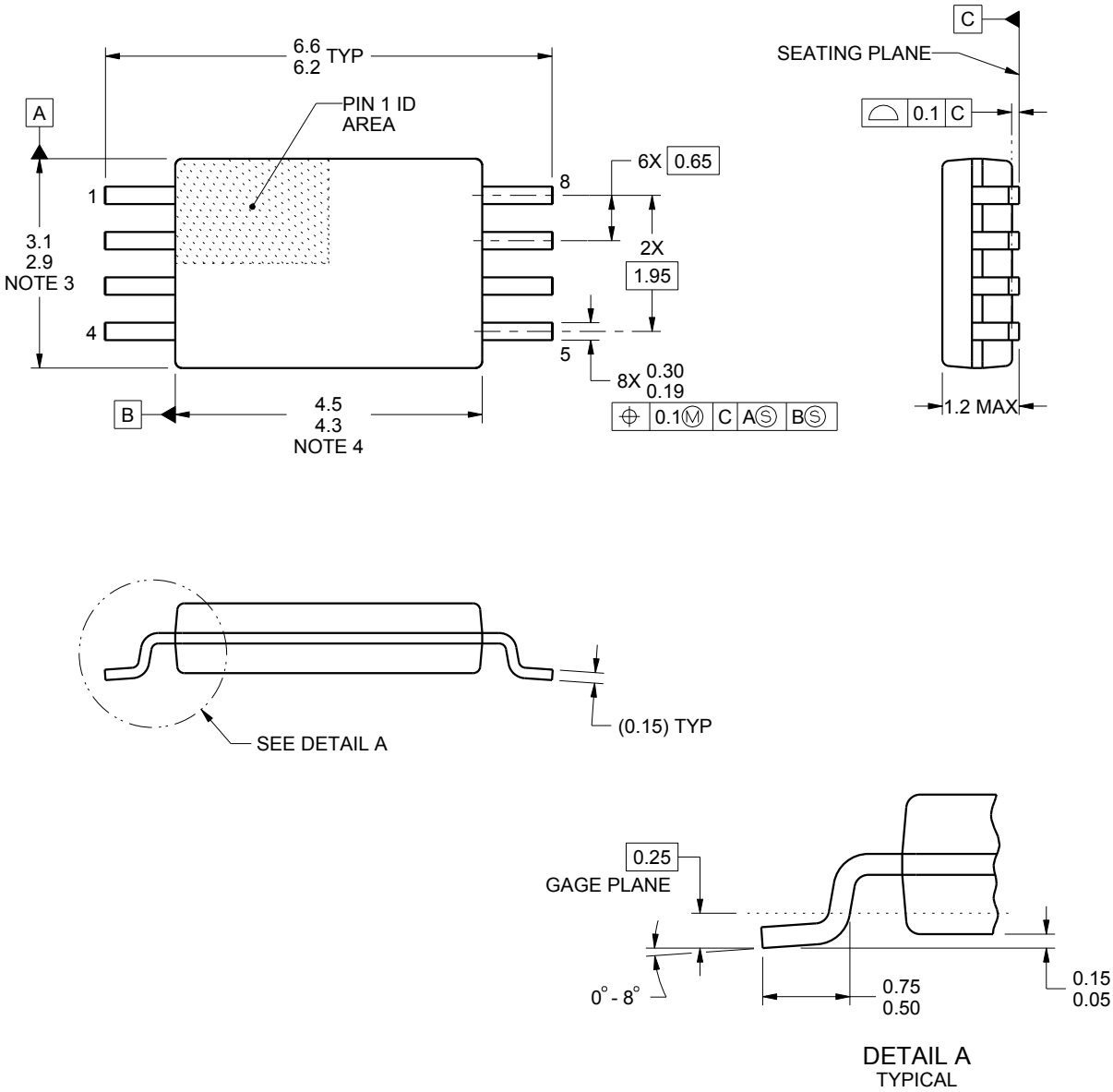
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/D 04/2020

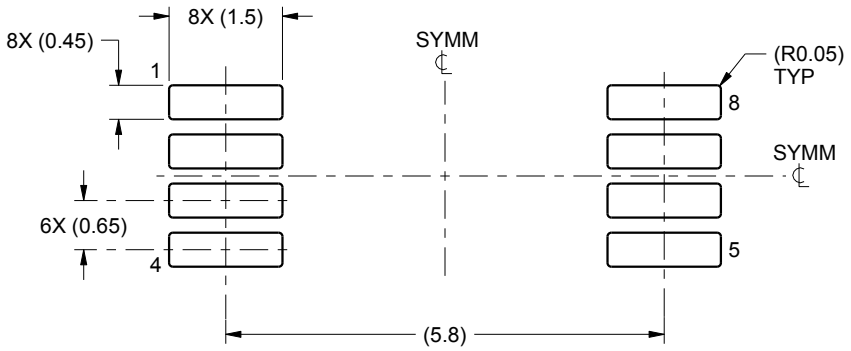
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

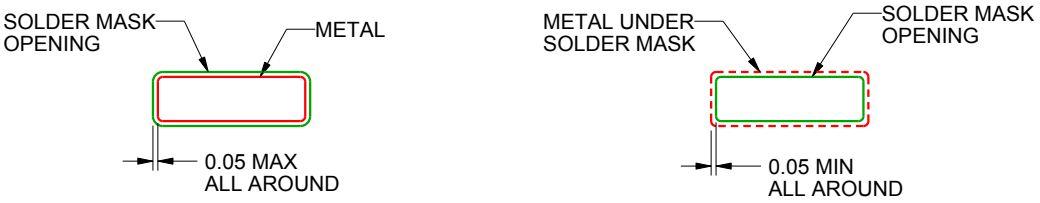


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK
DEFINED

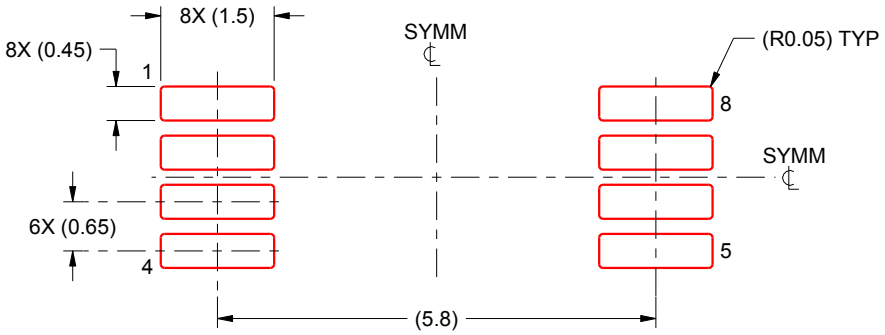
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

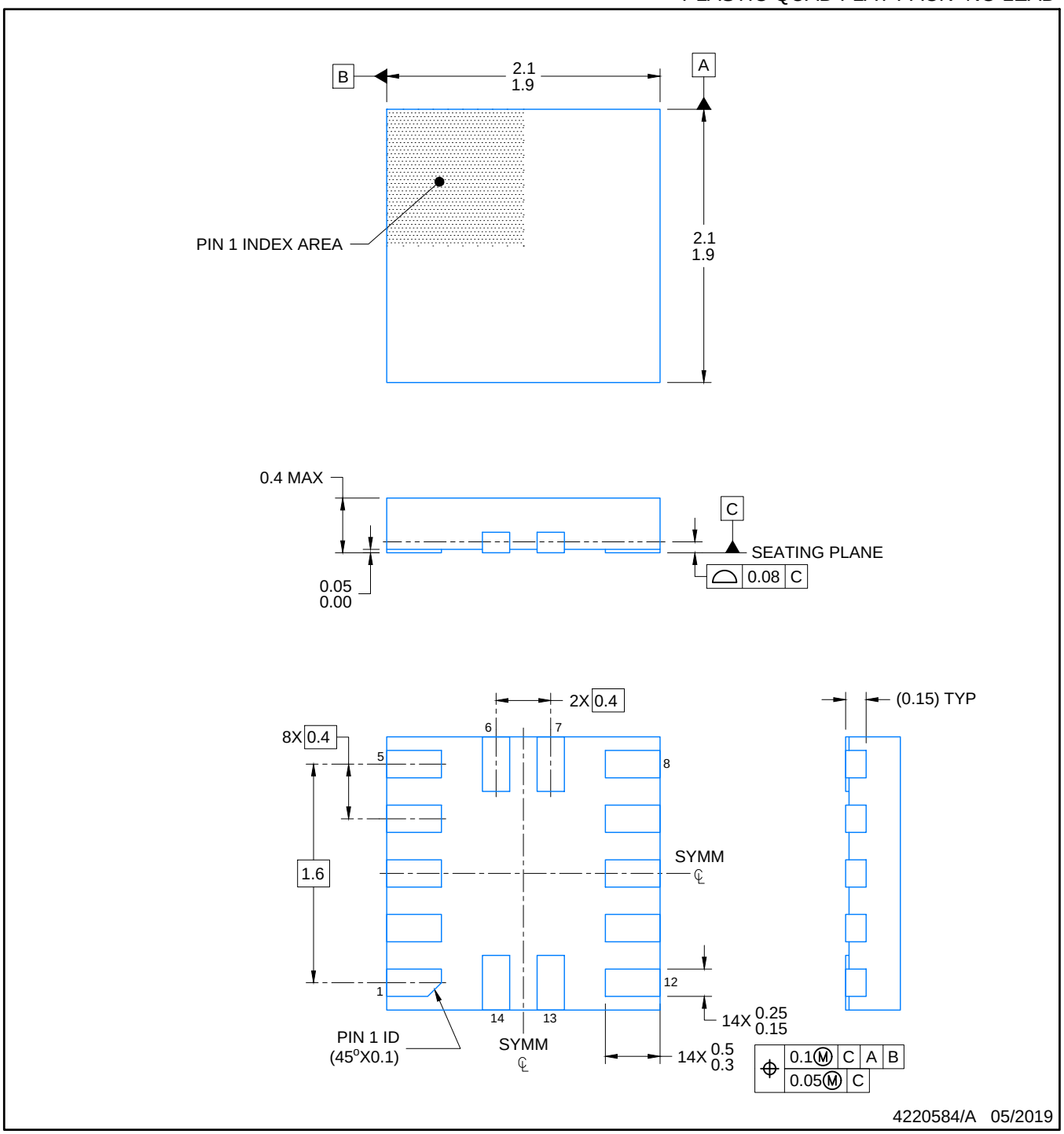


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

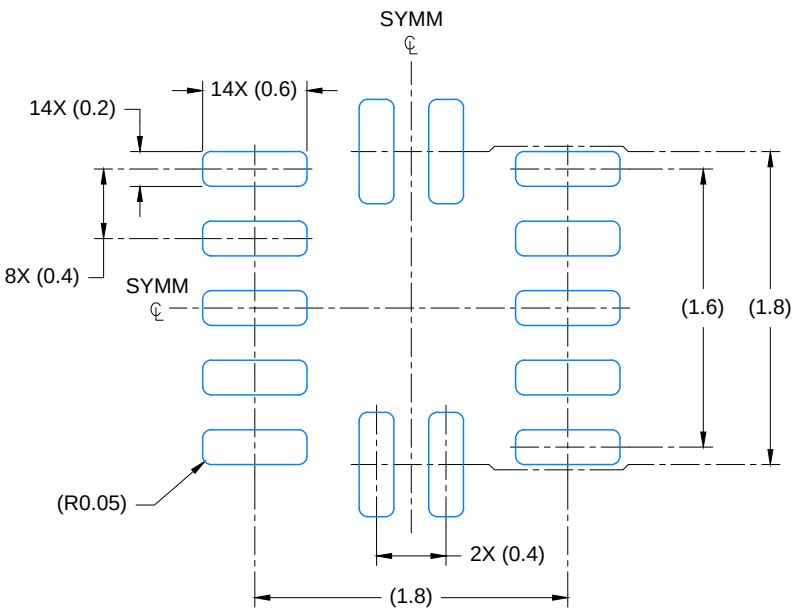
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

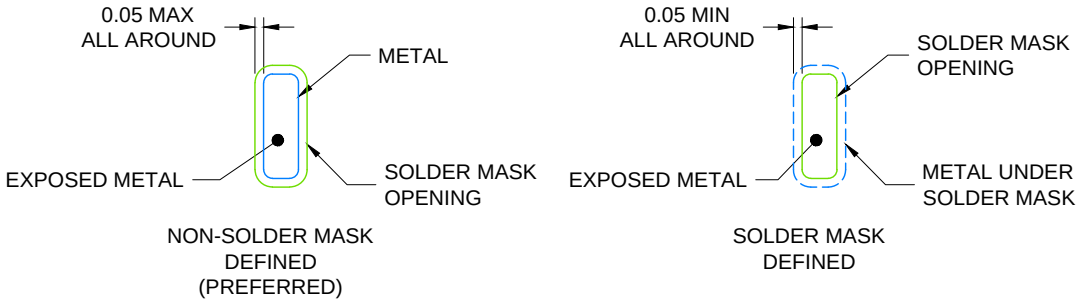


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 23X

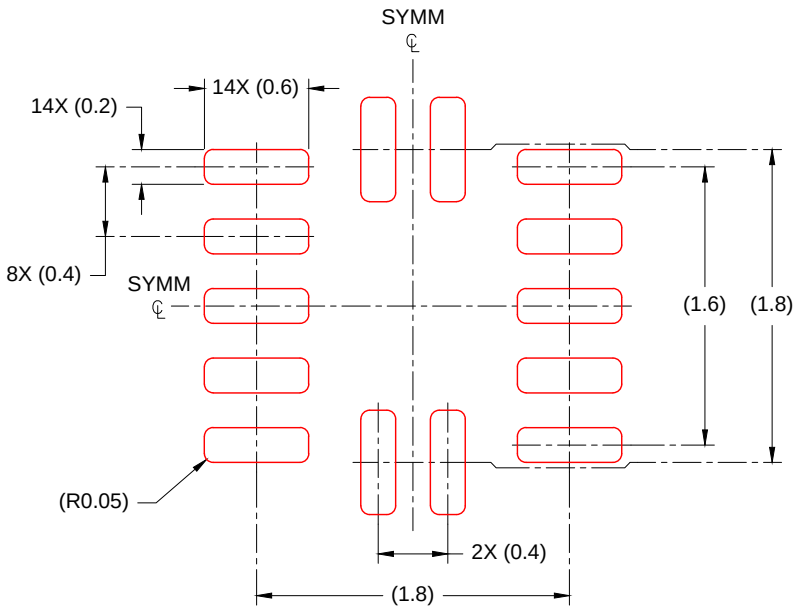


SOLDER MASK DETAILS

4220584/A 05/2019

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.100mm THICK STENCIL
SCALE: 23X

4220584/A 05/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022，德州仪器 (TI) 公司