



ISO733x 耐用 EMC 低功耗三通道数字隔离器

1 特性

- 信号传输速率: 25Mbps
- 输入时使用集成噪声滤波器
- 默认输出“高”和“低”选项
- 低功耗: 每通道的 I_{CC} 典型值 (1Mbps 时):
 - ISO7330: 1mA (5V 电源供电时), 0.8mA (3.3V 电源供电时)
 - ISO7331: 1.4mA (5V 电源供电时), 1mA (3.3V 电源供电时)
- 低传播延迟: 典型值 32ns (5V 电源供电时)
- 可由 3.3V 和 5V 电源供电
- 3.3V 和 5V 电平转换
- 宽温度范围: -40°C 至 125°C
- 70KV/ μ s 瞬态抗扰度, 典型值 (5V 电源供电时)
- 优异的电磁兼容性 (EMC)
 - 系统级静电放电 (ESD)、瞬态放电 (EFT) 以及抗浪涌保护
 - 低辐射
- 宽体小外形尺寸集成电路 (SOIC)-16 封装
- 隔离栅寿命: > 25 年
- 安全及管理批准:
 - 符合 DIN V VDE V 0884-10 和 DIN EN 61010-14242 标准的 V_{PK} 隔离部分)
 - 符合 UL 1577 标准且长达 1 分钟的 3000V_{RMS} 隔离
 - CSA 组件接受通知 5A, IEC 60950-1 和 IEC 61010-1 终端设备标准
 - 通过 GB4943.1-2011 CQC 认证

2 应用

- 在下列应用中的光电耦合器替代产品:
 - 工业用 FieldBus
 - ProfiBus
 - ModBus
 - DeviceNet™ 数据总线
 - 伺服控制接口
 - 电机控制
 - 电源
 - 电池组

3 说明

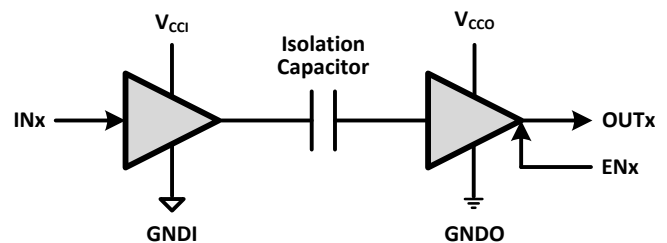
ISO733x 可提供符合 UL 标准的长达 1 分钟且高达 3000V_{RMS} 的电流隔离, 以及符合 VDE 标准的 4242V_{PK} 隔离。这些器件具有三个隔离通道, 其逻辑输入和输出缓冲器由二氧化硅 (SiO₂) 绝缘栅分离开来。ISO7330 有三个同向通道, ISO7331 有两个正向通道和一个反向通道。如果出现输入功率或信号损失, 则后缀为“F”的器件默认输出“低”电平, 后缀没有“F”的器件则默认输出“高”电平。更多详细信息与隔离式电源一起使用时, 这些器件可防止数据总线或者其它电路上的噪声电流进入本地接地并且干扰或损坏敏感电路。ISO733x 已针对恶劣环境集成了噪声滤波器, 在此类环境下, 器件的输入引脚上可能会出现短噪音脉冲。ISO733x 具有晶体管晶体管逻辑电路 (TTL) 输入阈值, 工作电压范围为 3V 到 5.5V。凭借创新的芯片设计和布线技术, ISO733x 的电磁兼容性得到了显著增强, 从而可确保提供系统级 ESD、EFT 和浪涌保护并符合辐射标准。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
ISO7330C	SOIC (16)	10.3mm x 7.5mm
ISO7330FC		
ISO7331C		
ISO7331FC		

(1) 如需了解所有可用封装, 请见数据表末尾的可订购产品附录。

简化电路原理图



(1) V_{CCI} 和 $GNDI$ 分别是输入通道的电源和接地连接。

(2) V_{CCO} 和 $GNDO$ 分别是输出的电源和接地连接。



目录

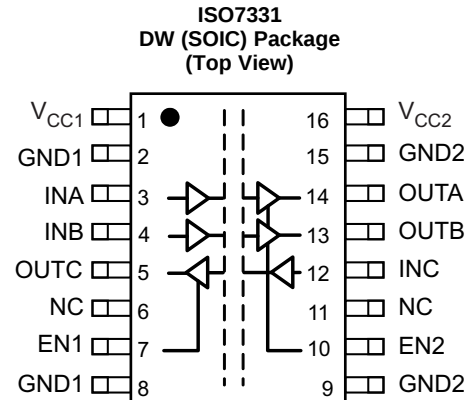
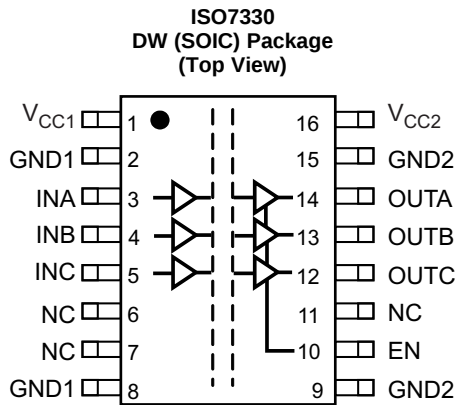
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4 修订历史记录

Changes from Revision A (April 2015) to Revision B	Page
• 已将 4242 V_{PK} 部分的“(VDE V 0884-10):2006-12”更改为“和 DIN EN 61010-1”（ 特性 ）	1
• Changed From: V_{CCI} To: V_{CC} in Figure 12	10
• Deleted IEC from the section title: Package Insulation Specifications	13
• Changed the CTI Test Conditions in Package Insulation Specifications	13
• Changed V_{ISO} Test Condition in the Insulation Characteristics table	14
• Deleted the V_{ISO} Specification 3600 in the Insulation Characteristics table	14

Changes from Original (January 2015) to Revision A	Page
• 将器件状态从产品预览更改为量产数据	1
• 已更改 特性 ，从 ISO7330: TBD mA 改为 1mA	1
• 已更改 特性 ，从 ISO731: TBD mA（3.3V 电源供电时）改为 0.8mA	1
• 已更改 特性 ，从 ISO731: TBD mA（5V 电源供电时）改为 1.4mA	1
• 从 特性 65KV/ μ s 瞬态抗扰度改为 70KV/ μ s 瞬态抗扰度	1
• 已更改安全及管理批准 特性	1
• 更改了简化电路原理图并增加了注释 1 和注释 2	1

5 Pin Configuration and Functions



Pin Functions

NAME	PIN		I/O	DESCRIPTION
	ISO7330	ISO7331		
V _{CC1}	1	1	–	Power supply, V _{CC1}
V _{CC2}	16	16	–	Power supply, V _{CC2}
GND1	2, 8	2, 8	–	Ground connection for V _{CC1}
GND2	9, 15	9, 15	–	Ground connection for V _{CC2}
INA	3	3	I	Input, channel A
INB	4	4	I	Input, channel B
INC	5	12	I	Input, channel C
NC	6, 7, 11	6, 11	–	No Connect. These pins have no internal connection.
OUTA	14	14	O	Output, channel A
OUTB	13	13	O	Output, channel B
OUTC	12	5	O	Output, channel C
EN	10	–	I	Output enable. OUTA, OUTB, and OUTC are enabled when EN is high or disconnected and disabled when EN is low.
EN1	–	7	I	Output enable 1. OUTC is enabled when EN1 is high or disconnected and disabled when EN1 is low.
EN2	–	10	I	Output enable 2. OUTA and OUTB are enabled when EN2 is high or disconnected and disabled when EN2 is low.

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

		MIN	MAX	UNIT
Supply voltage ⁽²⁾	V_{CC1}, V_{CC2}	–0.5	6	V
Voltage ⁽²⁾	INx, OUTx, ENx	–0.5	$V_{CC}+0.5^{(3)}$	V
Output current, I_O			±15	mA
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal and are peak voltage values.
- (3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

		VALUE	UNIT
V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage	3		5.5	V
I_{OH}	High-level output current	–4			mA
I_{OL}	Low-level output current			4	mA
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage	0		0.8	V
t_{ui}	Input pulse duration	40			ns
$1 / t_{ui}$	Signaling rate	0		25	Mbps
T_J ⁽¹⁾	Junction temperature			136	°C
T_A	Ambient temperature	–40	25	125	°C

- (1) To maintain the recommended operating conditions for T_J , see the [Thermal Information](#) table.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DW PACKAGE	UNIT
		(16) PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78.3	°C/W
$R_{\theta JCTop}$	Junction-to-case (top) thermal resistance	40.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	42.9	
Ψ_{JT}	Junction-to-top characterization parameter	15.3	
Ψ_{JB}	Junction-to-board characterization parameter	42.4	
$R_{\theta JCBot}$	Junction-to-case (bottom) thermal resistance	N/A	
P_D (ISO7330)	Maximum Power Dissipation by ISO7330	70	mW
P_{D1} (ISO7330)	Maximum Power Dissipation by Side-1 of ISO7330	20	
P_{D2} (ISO7330)	Maximum Power Dissipation by Side-2 of ISO7330	50	
P_D (ISO7331)	Maximum Power Dissipation by ISO7331	84	mW
P_{D1} (ISO7331)	Maximum Power Dissipation by Side-1 of ISO7331	35	
P_{D2} (ISO7331)	Maximum Power Dissipation by Side-2 of ISO7331	49	

- (1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, [SPRA953](#).

6.5 Electrical Characteristics

V_{CC1} and V_{CC2} at 5 V $\pm$ 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = −4 mA; see Figure 11		V _{CCO} ⁽¹⁾ − 0.5	4.7		V
		I _{OH} = −20 μA; see Figure 11		V _{CCO} ⁽¹⁾ − 0.1	5		
V _{OL}	Low-level output voltage	I _{OL} = 4 mA; see Figure 11			0.2	0.4	V
		I _{OL} = 20 μA; see Figure 11			0	0.1	
V _{I(HYS)}	Input threshold voltage hysteresis				480		mV
I _{IH}	High-level input current	I _N = V _{CC}				10	μA
I _{IL}	Low-level input current	I _N = 0 V			−10		μA
CMTI	Common-mode transient immunity	V _I = V _{CC} or 0 V; see Figure 14 .			25	70	kV/μs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I _{CC} measurement)							
ISO7330							
I _{CC1}	Supply current for V _{CC1} and V _{CC2}	Disable	V _I = V _{CC} or 0 V, EN = 0 V		0.5	1.1	mA
I _{CC2}					0.4	0.9	
I _{CC1}		DC to 1 Mbps	DC Input: V _I = V _{CC} or 0 V, AC Input: C _L = 15pF		0.5	1.1	
I _{CC2}					2.6	4.2	
I _{CC1}		10 Mbps	C _L = 15pF		1.1	1.9	
I _{CC2}					4.3	6	
I _{CC1}		25 Mbps	C _L = 15pF		2.1	3.3	
I _{CC2}					7	9.3	
ISO7331							
I _{CC1}	Supply current for V _{CC1} and V _{CC2}	Disable	V _I = V _{CC} or 0 V, EN1 = EN2 = 0 V		0.7	1.6	mA
I _{CC2}					0.7	1.3	
I _{CC1}		DC to 1 Mbps	DC Input: V _I = V _{CC} or 0 V, AC Input: C _L = 15pF		1.8	3	
I _{CC2}					2.4	3.6	
I _{CC1}		10 Mbps	C _L = 15pF		2.8	4.1	
I _{CC2}					3.8	5.1	
I _{CC1}		25 Mbps	C _L = 15pF		4.3	6.2	
I _{CC2}					5.8	7.8	

(1) V_{CCO} is supply voltage, V_{CC1} or V_{CC2} , for the output channel being measured.

6.6 Electrical Characteristics

V_{CC1} and V_{CC2} at 3.3 V $\pm$ 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = −4 mA; see Figure 11		V _{CCO} ⁽¹⁾ − 0.5	3		V
		I _{OH} = −20 μA; see Figure 11		V _{CCO} ⁽¹⁾ − 0.1	3.3		
V _{OL}	Low-level output voltage	I _{OL} = 4 mA; see Figure 11			0.2	0.4	V
		I _{OL} = 20 μA; see Figure 11			0	0.1	
V _{I(HYS)}	Input threshold voltage hysteresis				425		mV
I _{IH}	High-level input current	I _N = V _{CC}				10	μA
I _{IL}	Low-level input curree	I _N = 0 V		−10			μA
CMTI	Common-mode transient immunity	V _I = V _{CC} or 0 V; see Figure 14		25	50		kV/μs
SUPPLY CURRENT(All inputs switching with square wave clock signal for dynamic I _{CC} measurement)							
ISO7330							
I _{CC1}	Supply current for V _{CC1} and V _{CC2}	Disable	V _I = V _{CC} or 0 V, EN = 0 V		0.3	0.6	mA
I _{CC2}					0.3	0.6	
I _{CC1}		DC to 1 Mbps	DC Input: V _I = V _{CC} or 0 V, AC Input: C _L = 15pF		0.3	0.6	
I _{CC2}					2	3.1	
I _{CC1}		10 Mbps	C _L = 15pF		0.7	1.1	
I _{CC2}					3.1	4.3	
I _{CC1}		25 Mbps	C _L = 15pF		1.2	2	
I _{CC2}					4.8	6.3	
ISO7331							
I _{CC1}	Supply current for V _{CC1} and V _{CC2}	Disable	V _I = V _{CC} or 0 V, EN = 0 V		0.5	0.9	mA
I _{CC2}					0.5	0.8	
I _{CC1}		DC to 1 Mbps	DC Input: V _I = V _{CC} or 0 V, AC Input: C _L = 15pF		1.3	2.1	
I _{CC2}					1.7	2.6	
I _{CC1}		10 Mbps	C _L = 15pF		1.9	2.7	
I _{CC2}					2.6	3.5	
I _{CC1}		25 Mbps	C _L = 15pF		2.9	4.2	
I _{CC2}					3.9	5.2	

(1) V_{CCO} is supply voltage, V_{CC1} or V_{CC2} , for the output channel being measured.

6.7 Switching Characteristics

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} , t _{PHL}	Propagation delay time		See Figure 11	20	32	58	ns
PWD ⁽¹⁾	Pulse width distortion t _{PHL} – t _{PLH}					4	ns
t _{sk(o)} ⁽²⁾	Channel-to-channel output skew time		Same direction channels			2.5	ns
			Opposite direction channels			17	
t _{sk(pp)} ⁽³⁾	Part-to-part skew time					23	ns
t _r	Output signal rise time		See Figure 11		3		ns
t _f	Output signal fall time				2		ns
t _{PHZ}	Disable propagation delay, high-to-high impedance output		See Figure 12		7	12	ns
t _{PLZ}	Disable propagation delay, low-to-high impedance output				7	12	
t _{PZH}	Enable propagation delay, high impedance-to-high output	ISO733xC			7	12	
		ISO733xFC			11000	23000 ⁽⁴⁾	
t _{PZL}	Enable propagation delay, high impedance-to-low output	ISO733xC			11000	23000 ⁽⁴⁾	
		ISO733xFC			7	12	
t _{IS}	Fail-safe output delay time from input power loss		See Figure 13		7		μs

(1) Also known as pulse skew.

(2) t_{sk(o)} is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3) t_{sk(pp)} is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

(4) The enable signal rate should be ≤ 43 Kbps

6.8 Switching Characteristics

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} , t _{PHL}	Propagation delay time		See Figure 11	22	36	66	ns
PWD ⁽¹⁾	Pulse width distortion t _{PHL} – t _{PLH}					2.5	ns
t _{sk(o)} ⁽²⁾	Channel-to-channel output skew time		Same direction channels			3	ns
			Opposite direction channels			16	
t _{sk(pp)} ⁽³⁾	Part-to-part skew time					27	ns
t _r	Output signal rise time		See Figure 11		3		ns
t _f	Output signal fall time				2		ns
t _{PHZ}	Disable propagation delay, high-to-high impedance output		See Figure 12		9	18	ns
t _{PLZ}	Disable propagation delay, low-to-high impedance output				9	18	
t _{PZH}	Enable propagation delay, high impedance-to-high output	ISO733xC			9	18	
		ISO733xFC			13000	24000 ⁽⁴⁾	
t _{PZL}	Enable propagation delay, high impedance-to-low output	ISO733xC			13000	24000 ⁽⁴⁾	
		ISO733xFC			9	18	
t _{fs}	Fail-safe output delay time from input power loss		See Figure 13		7		μs

(1) Also known as pulse skew.

(2) t_{sk(o)} is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3) t_{sk(pp)} is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

(4) The enable signal rate should be ≤ 41 Kbps

6.9 Typical Characteristics

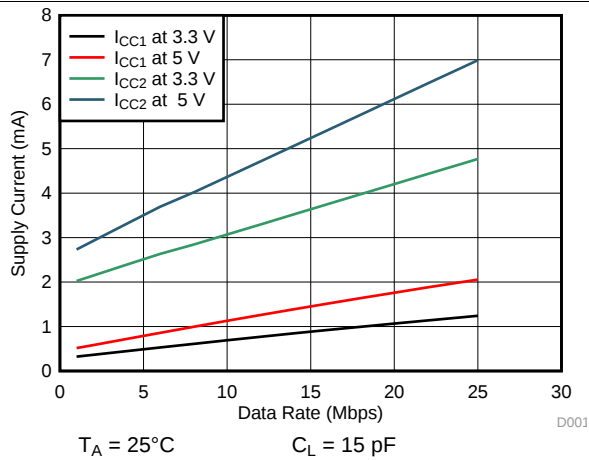


Figure 1. ISO7330 Supply Current vs Data Rate (with 15 pF Load)

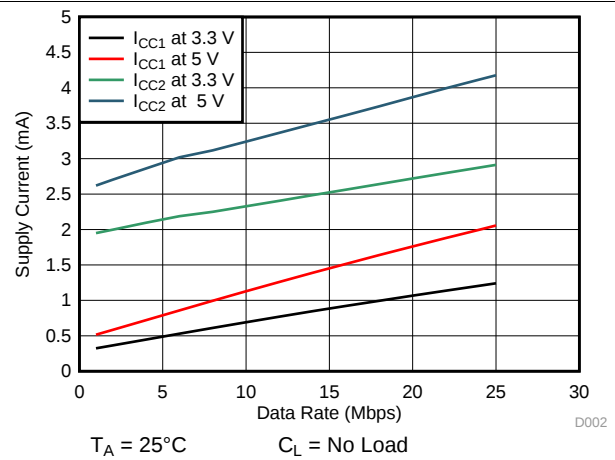


Figure 2. ISO7330 Supply Current vs Data Rate (with No Load)

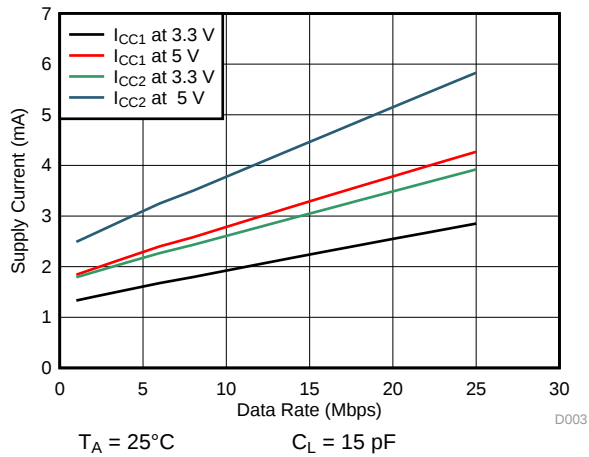


Figure 3. ISO7331 Supply Current vs Data Rate (with 15 pF Load)

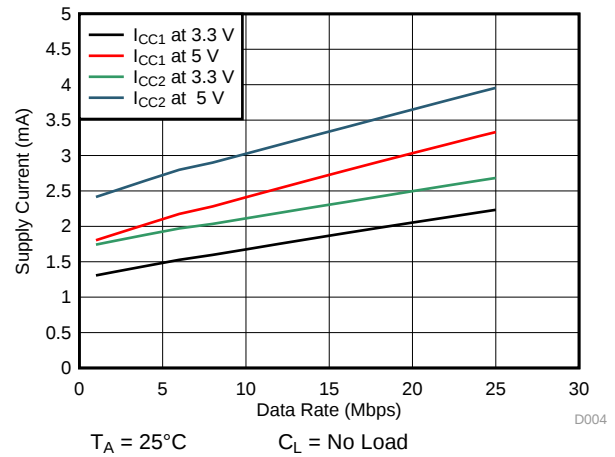


Figure 4. ISO7331 Supply Current vs Data Rate (with No Load)

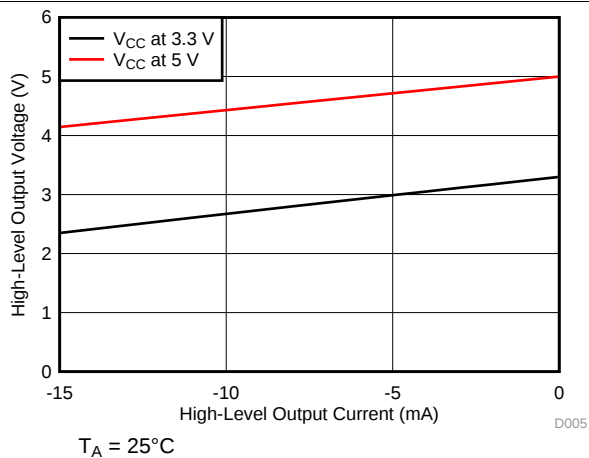


Figure 5. High-Level Output Voltage vs High-level Output Current

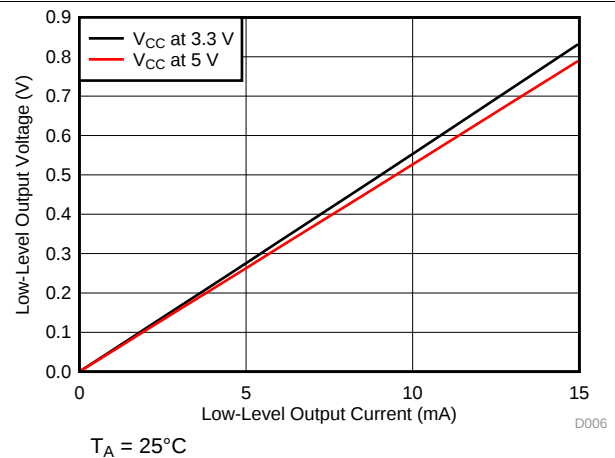


Figure 6. Low-Level Output Voltage vs Low-Level Output Current

Typical Characteristics (continued)

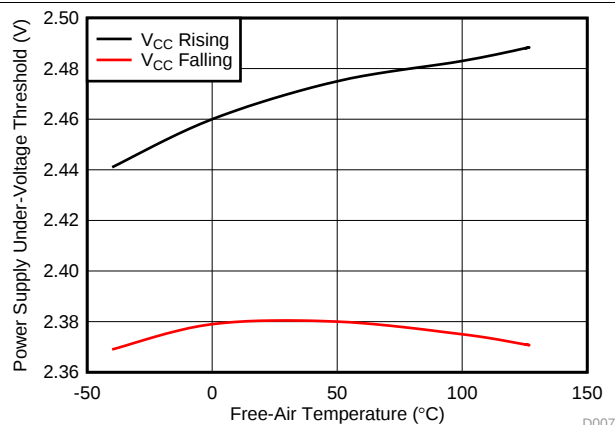


Figure 7. Power Supply Undervoltage Threshold vs Free-Air Temperature

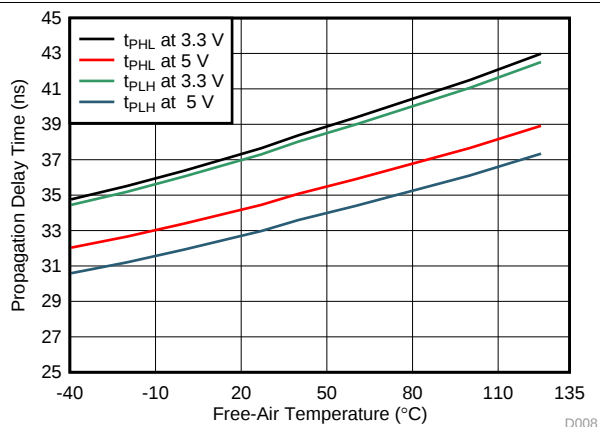


Figure 8. Propagation Delay Time vs Free-Air Temperature

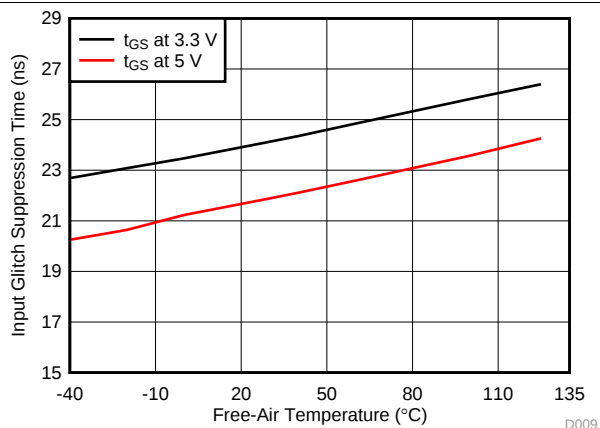


Figure 9. Input Glitch Suppression Time vs Free-Air Temperature

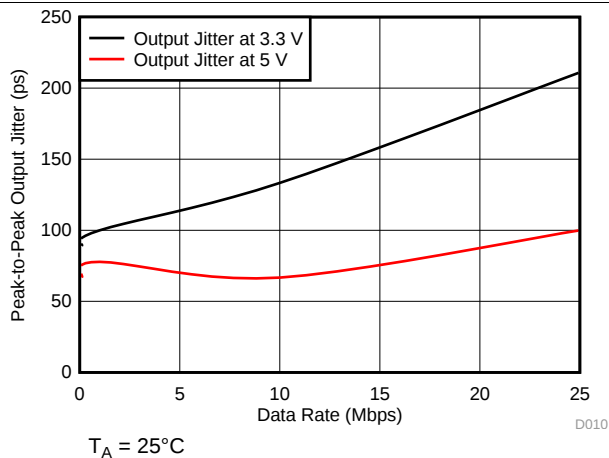
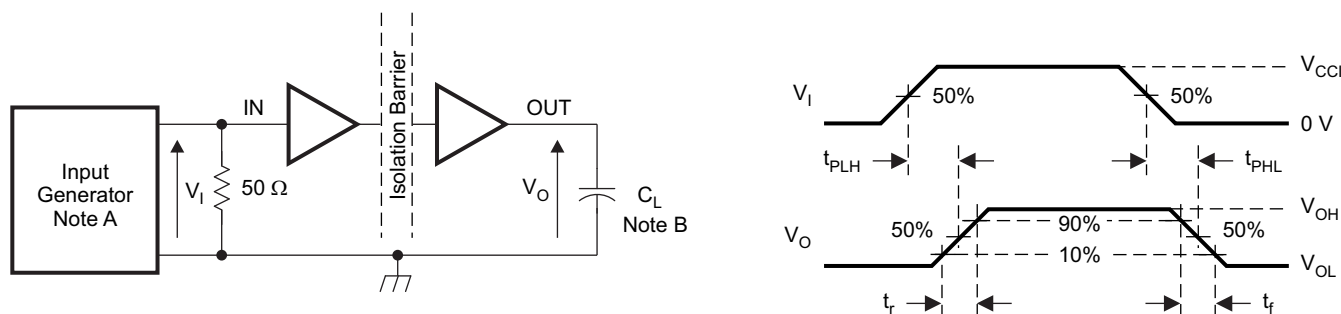


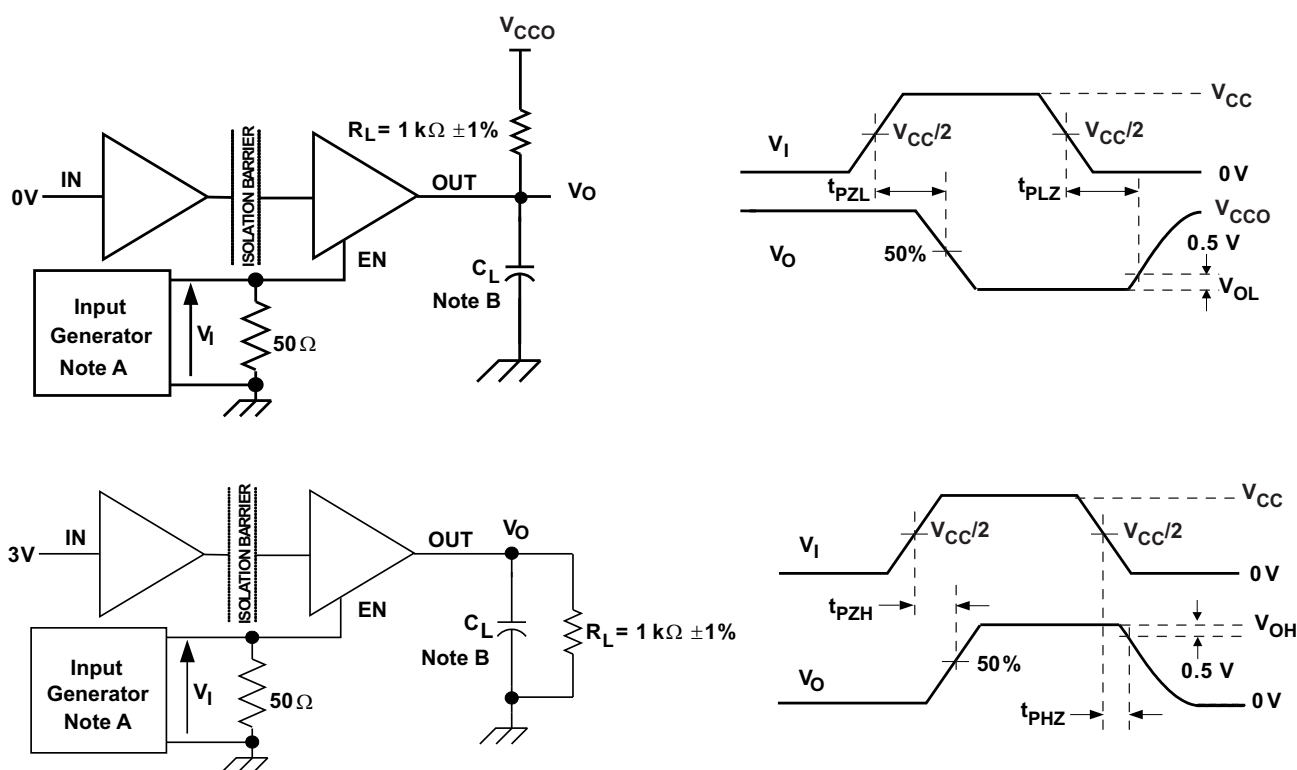
Figure 10. Output Jitter vs Data Rate

7 Parameter Measurement Information



- The input pulse is supplied by a generator having the following characteristics: $PRR \leq 50$ kHz, 50% duty cycle, $t_r \leq 3$ ns, $t_f \leq 3$ ns, $Z_O = 50 \Omega$. At the input, a 50- Ω resistor is required to terminate the Input Generator signal. It is not needed in actual application.
- $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

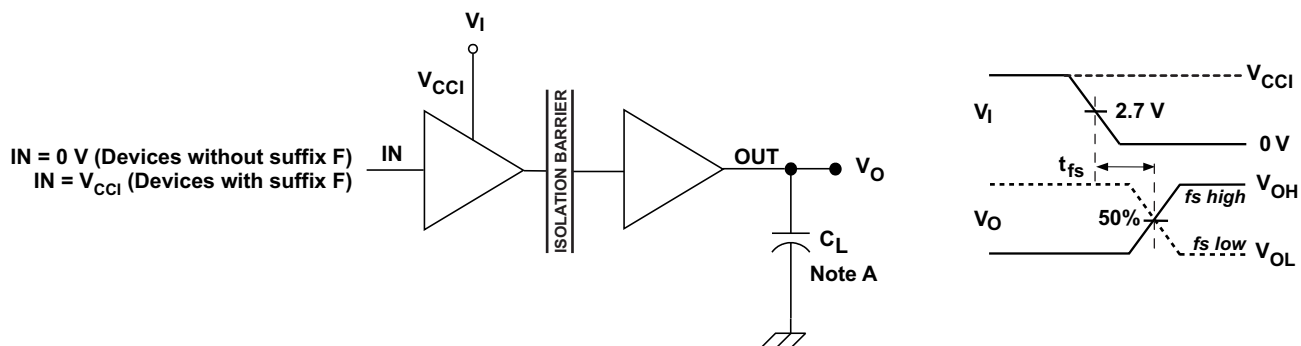
Figure 11. Switching Characteristic Test Circuit and Voltage Waveforms



- The input pulse is supplied by a generator having the following characteristics: $PRR \leq 10$ kHz, 50% duty cycle, $t_r \leq 3$ ns, $t_f \leq 3$ ns, $Z_O = 50 \Omega$.
- $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

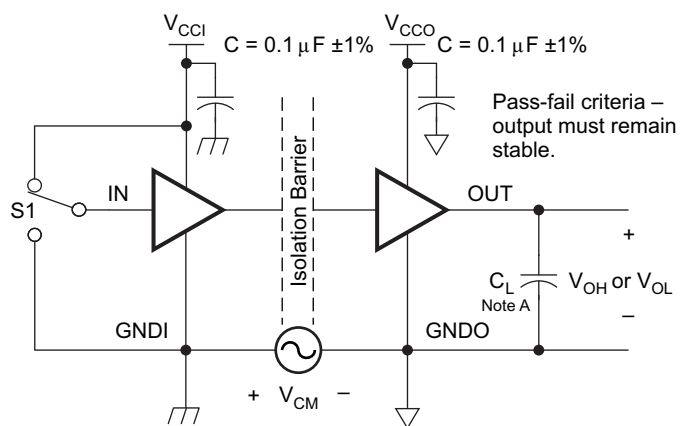
Figure 12. Enable/Disable Propagation Delay Time Test Circuit and Waveform

Parameter Measurement Information (continued)



A. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 13. Fail-Safe Output Delay-Time Test Circuit and Voltage Waveforms



A. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 14. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The isolator in Figure 15 is based on a capacitive isolation barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency (HF) channel with a bandwidth from 100 kbps up to 25 Mbps, and a low-frequency (LF) channel covering the range from 100 kbps down to DC.

In principle, a single-ended input signal entering the HF channel is split into a differential signal via the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transient pulses, which then are converted into CMOS levels by a comparator. The transient pulses at the input of the comparator can be either above or below the common mode voltage V_{REF} depending on whether the input bit transitioned from 0 to 1 or 1 to 0. The comparator threshold is adjusted based on the expected bit transition. A decision logic (DCL) at the output of the HF channel comparator measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high-frequency to the low-frequency channel.

8.2 Functional Block Diagram

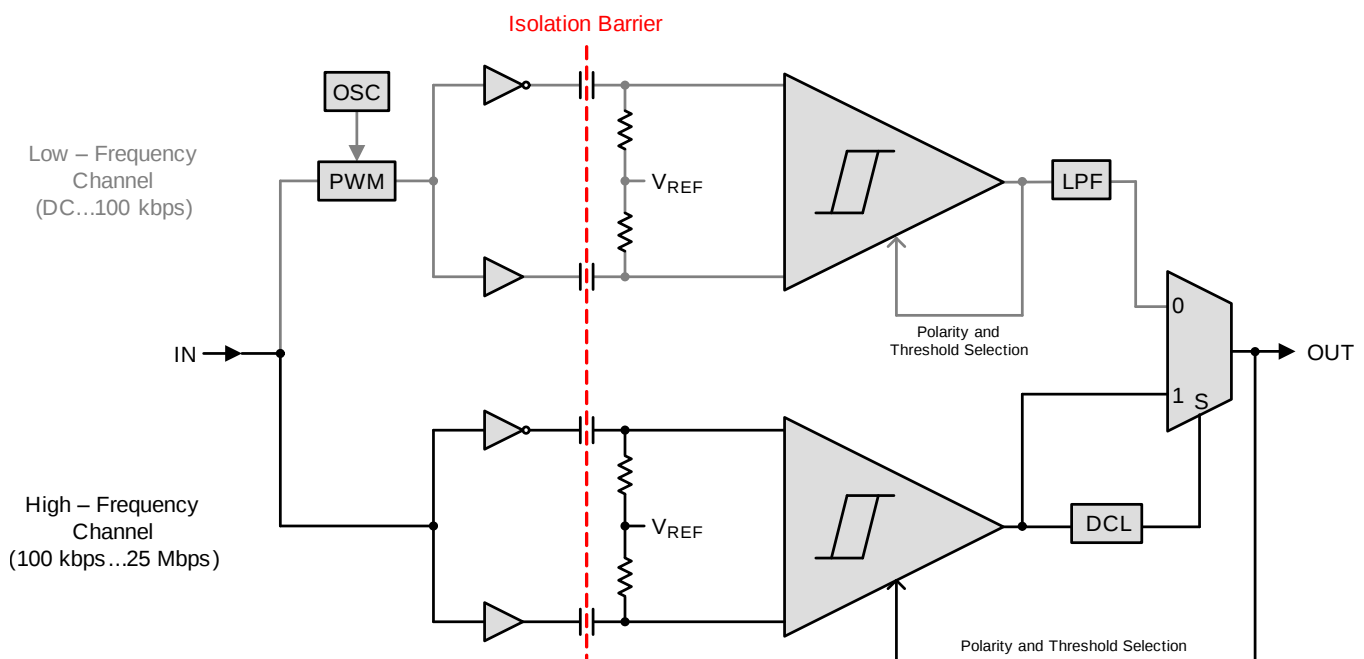


Figure 15. Conceptual Block Diagram of a Digital Capacitive Isolator

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

8.3 Feature Description

PRODUCT	CHANNEL DIRECTION	RATED ISOLATION	MAX DATA RATE	DEFAULT OUTPUT
ISO7330C	3 Forward, 0 Reverse	3000 V _{RMS} / 4242 V _{PK} ⁽¹⁾	25 Mbps	High
ISO7330FC				Low
ISO7331C	2 Forward, 1 Reverse			High
ISO7331FC				Low

(1) See the [Regulatory Information](#) section for detailed Isolation Ratings

8.3.1 High Voltage Feature Description

8.3.1.1 Package Insulation Specifications

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal-to-terminal distance through air	8			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal-to-terminal distance across the package surface	8			mm
CTI	Tracking resistance (comparative tracking index)	DIN EN 60112 (VDE 0303-11); IEC 60112	>400			V
DTI	Minimum internal gap (internal clearance)	Distance through the insulation	13			μm
R _{IO}	Isolation resistance, input to output ⁽¹⁾	V _{IO} = 500 V, T _A = 25°C		>10 ¹²		Ω
		V _{IO} = 500 V, 100°C ≤ T _A ≤ max		>10 ¹¹		Ω
C _{IO}	Isolation capacitance, input to output ⁽¹⁾	V _{IO} = 0.4 sin (2πft), f = 1 MHz		2		pF
C _I	Input capacitance ⁽²⁾	V _I = V _{CC} /2 + 0.4 sin (2πft), f = 1 MHz, V _{CC} = 5 V		2		pF

(1) All pins on each side of the barrier tied together creating a two-terminal device.

(2) Measured from input pin to ground.

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

8.3.1.2 Insulation Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER ⁽¹⁾		TEST CONDITIONS	SPECIFICATION	UNIT
V _{IOWM}	Maximum isolation working voltage		1000	V _{RMS}
V _{IORM}	Maximum repetitive peak voltage per DIN V VDE V 0884-10		1414	V _{PK}
V _{PR}	Input-to-output test voltage per DIN V VDE V 0884-10	After Input/Output safety test subgroup 2/3, V _{PR} = V _{IORM} × 1.2, t = 10 s, Partial discharge < 5 pC	1697	V _{PK}
		Method a, After environmental tests subgroup 1, V _{PR} = V _{IORM} × 1.6, t = 10 s, Partial Discharge < 5 pC	2262	
		Method b1, V _{PR} = V _{IORM} × 1.875, t = 1 s (100% Production test) Partial discharge < 5 pC	2651	
V _{IOTM}	Maximum transient overvoltage per DIN V VDE V 0884-10	V _{TEST} = V _{IOTM} t = 60 sec (qualification) t = 1 sec (100% production)	4242	V _{PK}
V _{IOSM}	Maximum surge isolation voltage per DIN V VDE V 0884-10	Test method per IEC 60065, 1.2/50 μs waveform, V _{TEST} = 1.3 × V _{IOSM} = 7800 V _{PK} (qualification)	6000	V _{PK}
V _{ISO}	Withstand isolation voltage per UL 1577	V _{TEST} = V _{ISO} = 3000 V _{RMS} , t = 60 sec (qualification) V _{TEST} = 1.2 × V _{ISO} = 3600 V _{RMS} , t = 1 sec (100% production)	3000	V _{RMS}
R _S	Insulation resistance	V _{IO} = 500 V at T _S	>10 ⁹	Ω
Pollution degree			2	

(1) Climatic Classification 40/125/21

Table 1. IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤ 300 V _{RMS}	I–IV
	Rated mains voltage ≤ 600 V _{RMS}	I–III
	Rated mains voltage ≤ 1000 V _{RMS}	I–II

8.3.1.3 Regulatory Information

VDE	CSA	UL	CQC
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1 (VDE 0411-1):2011-07	Approved under CSA Component Acceptance Notice 5A, IEC 60950-1, and IEC 61010-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB4943.1-2011
Basic Insulation Maximum Transient Overvoltage, 4242 V _{PK} ; Maximum Surge Isolation Voltage, 6000 V _{PK} ; Maximum Repetitive Peak Isolation Voltage, 1414 V _{PK}	800 V _{RMS} Basic Insulation and 400 V _{RMS} Reinforced Insulation working voltage per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed.+A1+A2; 300 V _{RMS} Basic Insulation working voltage per CSA 61010-1-12 and IEC 61010-1 3rd Ed.	Single protection, 3000 V _{RMS} ⁽¹⁾	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V _{RMS} maximum working voltage
Certificate number: 40016131	Master contract number: 220991	File number: E181974	Certificate number: CQC15001121716

 (1) Production tested ≥ 3600 V_{RMS} for 1 second in accordance with UL 1577.

8.3.1.4 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S Safety input, output, or supply current	$R_{\theta JA} = 78.3\text{ }^{\circ}\text{C/W}$, $V_I = 5.5\text{ V}$, $T_J = 150^{\circ}\text{C}$, $T_A = 25^{\circ}\text{C}$			290	mA
	$R_{\theta JA} = 78.3\text{ }^{\circ}\text{C/W}$, $V_I = 3.6\text{ V}$, $T_J = 150^{\circ}\text{C}$, $T_A = 25^{\circ}\text{C}$			443	
T_S Maximum case temperature				150	$^{\circ}\text{C}$

The safety-limiting constraint is the absolute-maximum junction temperature specified in the [Absolut Maximun Ratings](#) table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the [Thermal Information](#) table is that of a device installed on a High-K Test Board for Leaded Surface-Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

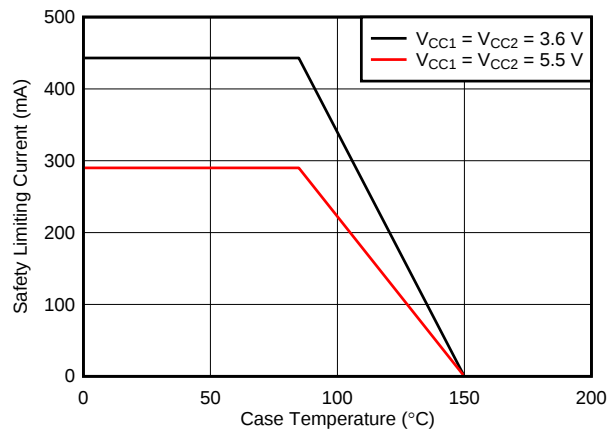


Figure 16. θ_{JC} Thermal Derating Curve per DIN V VDE V 0884-10

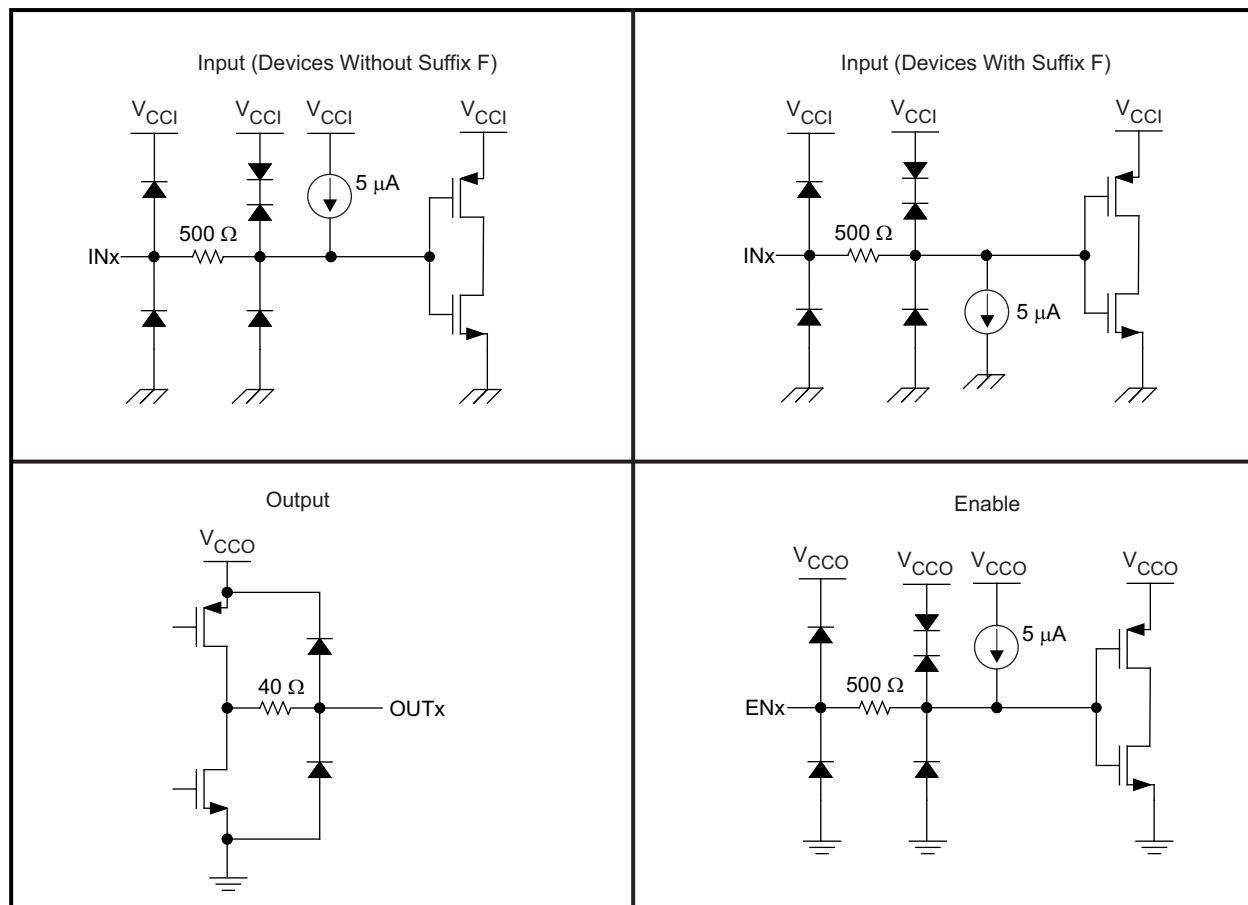
8.4 Device Functional Modes

Table 2. Function Table⁽¹⁾

V_{CCI}	V_{CCO}	INPUT (INx)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)	
				ISO733xC	ISO733xFC
PU	PU	H	H or Open	H	H
		L	H or Open	L	L
		X	L	Z	Z
		Open	H or Open	H ⁽²⁾	L ⁽³⁾
PD	PU	X	H or Open	H ⁽²⁾	L ⁽³⁾
X	PU	X	L	Z	Z
X	PD	X	X	Undetermined	Undetermined

- (1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} ; PU = Powered up ($V_{CC} \geq 3$ V); PD = Powered down ($V_{CC} \leq 2.1$ V); X = Irrelevant; H = High level; L = Low level; Open = Not connected
- (2) In fail-safe condition, output defaults to high level
- (3) In fail-safe condition, output defaults to low level

8.4.1 Device I/O Schematics


Figure 17. Device I/O Schematics

Typical Application (continued)

9.2.1 Design Requirements

9.2.1.1 Typical Supply Current Equations

ISO7330:

At $V_{CC1} = V_{CC2} = 5\text{ V}$

- $I_{CC1} = 0.46544 + (0.006455 \times f)$
- $I_{CC2} = 2.28021 + (0.08242 \times f) + (0.006237 \times f \times C_L)$

At $V_{CC1} = V_{CC2} = 3.3\text{ V}$

- $I_{CC1} = 0.29211 + (0.03588 \times f)$
- $I_{CC2} = 1.8414 + (0.02886 \times f) + (0.00548 \times f \times C_L)$

ISO7331:

At $V_{CC1} = V_{CC2} = 5\text{ V}$

- $I_{CC1} = 1.661 + (0.07916 \times f) + (0.00169 \times f \times C_L)$
- $I_{CC2} = 2.04 + (0.0778 \times f) + (0.00422 \times f \times C_L)$

At $V_{CC1} = V_{CC2} = 3.3\text{ V}$

- $I_{CC1} = 1.2402 + (0.03127 \times f) + (0.001954 \times f \times C_L)$
- $I_{CC2} = 1.53839 + (0.02933 \times f) + (0.0037285 \times f \times C_L)$

I_{CC1} and I_{CC2} are typical supply currents measured in mA, f is data rate measured in Mbps, C_L is the capacitive load measured in pF.

9.2.2 Detailed Design Procedure

9.2.2.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO733x incorporate many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

Typical Application (continued)

9.2.3 Application Performance Curves

Typical eye diagrams of ISO733x below indicate low jitter and wide open eye at the maximum data rate of 25 Mbps.

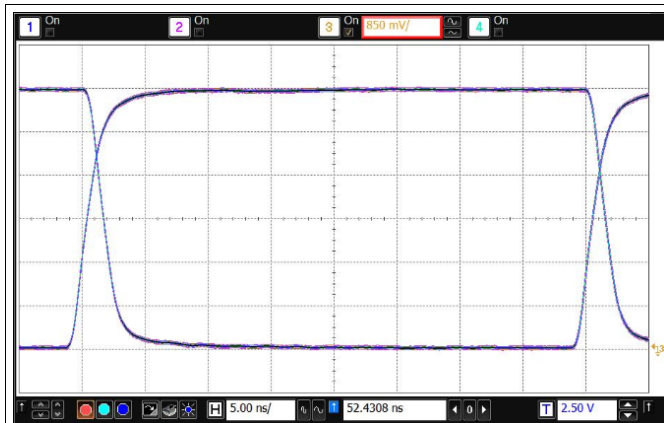


Figure 19. Eye Diagram at 25 Mbps, 5 V and 25°C

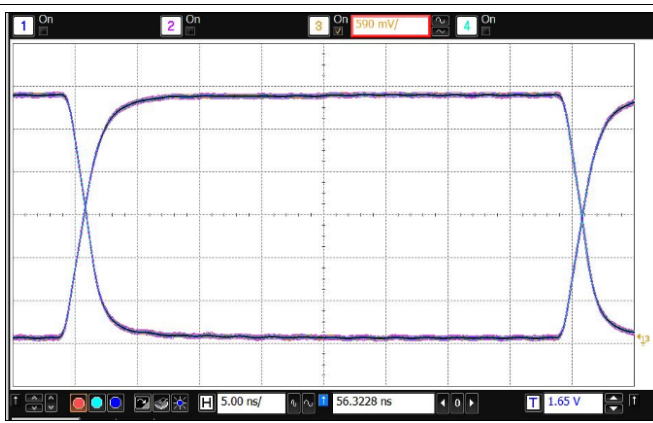


Figure 20. Eye Diagram at 25 Mbps, 3.3 V and 25°C

9.2.4 Systems Examples

Unlike Optocouplers, which need external components to improve performance, provide bias, or limit current, ISO733x only needs two external bypass capacitors to operate.

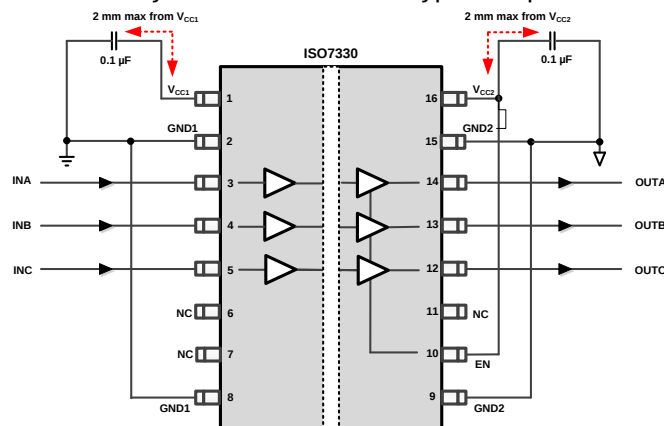


Figure 21. Typical ISO7330 Circuit Hook-up

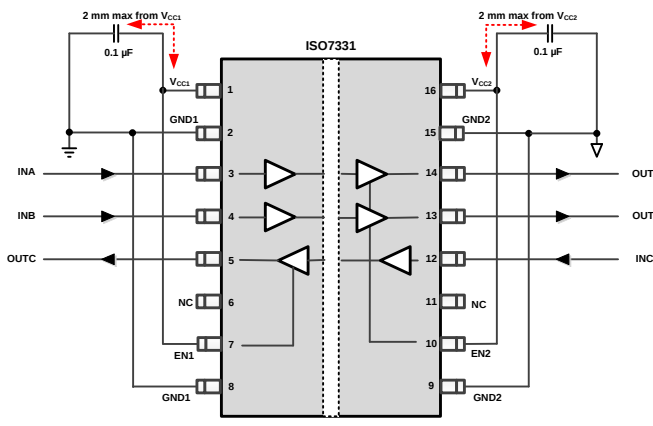


Figure 22. Typical ISO7331 Circuit Hook-up

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1 µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' [SN6501](#). For such applications, detailed power supply design and transformer selection recommendations are available in [SN6501](#) datasheet ([SLLSEA0](#)).

11 Layout

11.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and its self-extinguishing flammability-characteristics.

11.2 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see [Figure 23](#)). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/in².
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power / ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see Application Note [SLLA284](#), *Digital Isolator Design Guide*.

11.3 Layout Example

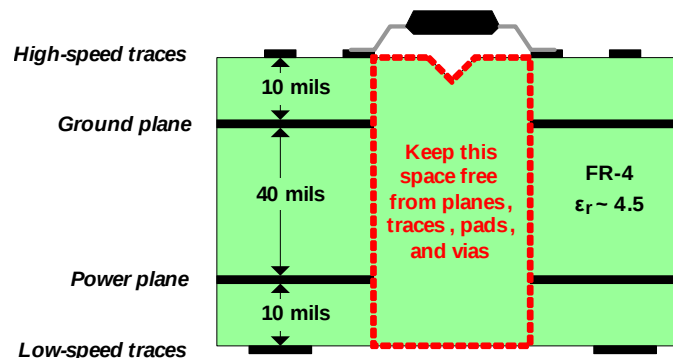


Figure 23. Recommended Layer Stack

12 器件和文档支持

12.1 相关链接

以下表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 3. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
ISO7330C	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ISO7330FC	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ISO7331C	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ISO7331FC	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.2 商标

DeviceNet is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.4 术语表

[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

[SLLA353](#), 《隔离相关术语》

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7330CDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7330C	Samples
ISO7330CDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7330C	Samples
ISO7330FCDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7330FC	Samples
ISO7330FCDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7330FC	Samples
ISO7331CDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7331C	Samples
ISO7331CDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7331C	Samples
ISO7331FCDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7331FC	Samples
ISO7331FCDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7331FC	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7330CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7330FCDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7331CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7331FCDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

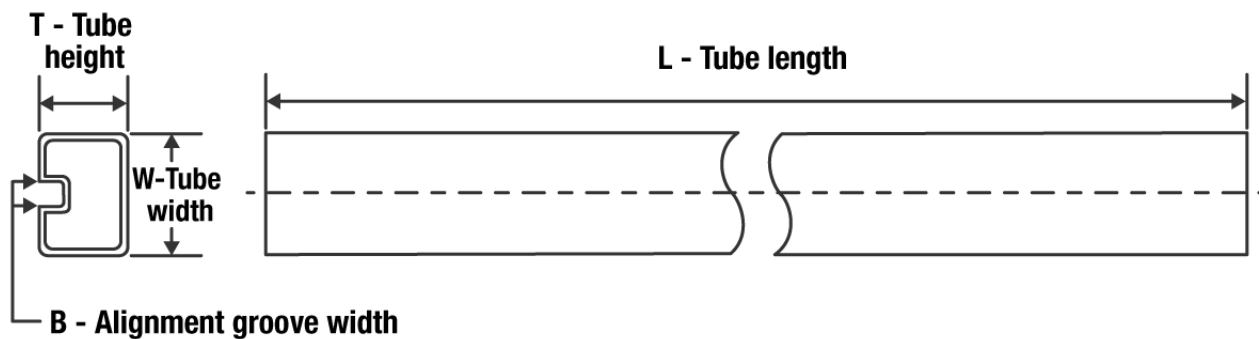
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7330CDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7330FCDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7331CDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7331FCDWR	SOIC	DW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
ISO7330CDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7330FCDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7331CDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7331FCDW	DW	SOIC	16	40	506.98	12.7	4826	6.6

重要声明和免责声明

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