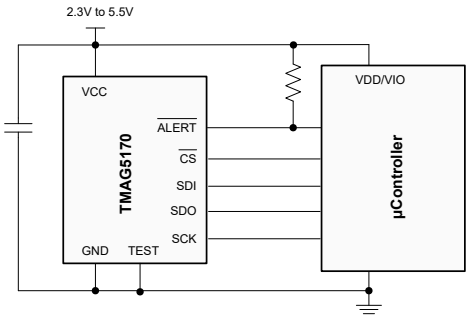
TMAG5170-Q1 具有 SPI 接口的高精度 3D 线性霍尔效应传感器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 0：–40°C 至 150°C
- 高精度线性 3D 霍尔效应传感器，可优化位置检测速度和精度：
  - 线性测量总误差：±2.6%（25°C 时为最大值）
  - 灵敏度温漂：±2.8%（最大值）
  - 单轴转换率为 20kSPS
- 符合功能安全标准：
  - 专为功能安全应用开发
  - 可帮助进行 ISO 26262 系统设计的文档
  - 系统设计符合 ASIL D
  - 硬件完整性高达 ASIL B 级
- 10MHz 串行外设接口 (SPI)，该接口具有循环冗余校验 (CRC)
- 误差 < ±3°C 的内置温度传感器
- 独立可选 X、Y 和 Z 范围：
  - TMAG5170A1-Q1：±25，±50，±100mT
  - TMAG5170A2-Q1：±75，±150，±300mT
- 仅消耗 1.5µA、可实现阈值检测的自主唤醒和睡眠模式
- $\overline{\text{ALERT}}$ 功能，用以启动传感器转换或指示转换完成
- 多种磁体类型的集成温度补偿
- 具有增益和偏轴调节的集成角 CORDIC 计算
- 2.3V 至 5.5V 电源电压范围

2 应用

- 转向柱控制
- 方向盘控制
- 换挡系统
- 电动自行车
- 雨刮器模块
- 传动器



应用方框图

3 说明

TMAG5170-Q1 是高精度线性 3D 霍尔效应传感器，适用于各种汽车类和工业应用。高集成度可在各种位置检测系统中提供灵活性和准确性。此器件在 X、Y 和 Z 轴具有 3 个独立的霍尔传感器。

精密信号链和集成 12 位 ADC 可实现高精度和低漂移磁场测量，同时支持高达 20kSPS 的采样率。片上温度传感器数据可用于系统级漂移补偿。

集成角度计算引擎 (CORDIC) 为同轴和离轴角度测量拓扑提供完整的 360° 角度位置信息。使用用户选择的两个磁轴执行角度计算。该器件具有磁增益和偏轴校正功能，可减轻系统机械误差源的影响。

可以通过 SPI 配置 TMAG5170-Q1，以实现磁轴和温度测量的任意组合。多个传感器转换方案和 SPI 读取帧有助于优化吞吐量和准确性。专用的 $\overline{\text{ALERT}}$ 引脚可以在低功耗唤醒和睡眠模式期间充当系统中断，也可以被微控制器用来触发新的传感器转换。

TMAG5170-Q1 提供多种诊断功能来检测和报告系统和器件级故障。SPI 通信具有用户启用的循环冗余校验，以增强数据完整性。

该器件具有两个不同的可订购产品，以支持从 ±25mT 到 ±300mT 的宽磁场范围。

该器件在 –40°C 至 +150°C 的宽环境温度范围内能够保持稳定一致的优异性能。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TMAG5170-Q1	VSSOP (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

Changes from Revision * (June 2020) to Revision A (December 2021)	Page
• 将数据表状态从“预告信息”更改为：量产数据	1

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5 Pin Configuration and Functions

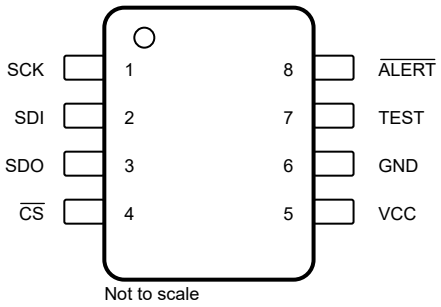

图 5-1. DGK Package 8-Pin VSSOP Top View

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	SCK	I	Serial clock
2	SDI	I	Serial data in
3	SDO	O	Serial data out
4	$\overline{CS}$	I	Chip select
5	VCC	P	Main power supply. Handles 2.3-V to 5.5-V power supply input
6	GND	G	Ground reference
7	TEST	P	TI test pin. Should be grounded in application
8	$\overline{ALERT}$	I/O	Status output/trigger

(1) I = input, O = output, I/O = input and output, G = ground, P = power

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{VCC}	Main supply voltage	–0.3	7	V
I_{OUT}	Output current, SDO, $\overline{ALERT}$	–10	10	mA
V_{OUT}	Output voltage, SDO, $\overline{ALERT}$	–0.3	7	V
V_{IN}	Input voltage, SDI, $\overline{CS}$, SCK	–0.3	V_{VCC}+ 0.3	V
B_{MAX}	Magnetic flux density		Unlimited	T
T_J	Junction temperature	–40	170	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD classification level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C4B	Corner pins (1, 4, 5, and 8)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Thermal Information

THERMAL METRIC(1)		TMAG5170-Q1 DGK (8-MSOP) PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	170.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	90.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VCC}	Main supply voltage	2.3		5.5	V
I_{OUT}	Output current, SDO	–2		2	mA
I_{OUT}	Output current, $\overline{ALERT}$	0		2	mA
V_{IH}	Input HIGH voltage, SDI, $\overline{CS}$, SCK	0.75			V_{VCC}
V_{IL}	Input LOW voltage, SDI, $\overline{CS}$, SCK			0.25	V_{VCC}
$t_{w_trigger}$	Pulse width for conversion trigger input signal	1		25	µs

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over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Operating free air temperature	-40		150	C

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDO, $\overline{\text{ALERT}}$						
V_{OH}	Output HIGH voltage, SDO pin	I_{OUT} = – 2mA	V_{CC} – 0.4		V_{CC}	V
V_{OL}	Output LOW voltage, SDO pin	I_{OUT} = 2mA	0		0.4	V
V_{OL}	Output LOW voltage, $\overline{\text{ALERT}}$ pin	I_{OUT} = 2mA	0		0.4	V
$t_{FALL_\overline{ALERT}}$	$\overline{\text{ALERT}}$ output fall time	R_{PU} =10KΩ, C_L =20pF, V_{CC} =2.3V to 5.5V		50		ns
$t_{\overline{ALERT}}$	$\overline{\text{ALERT}}$ output pulse width with conversion complete or threshold cross interrupt event	ALERT_MODE =0b, Interrupt & Trigger Mode		5		µs
$t_{\overline{ALERT}}$	$\overline{\text{ALERT}}$ output pulse width with other interrupt events	ALERT_MODE =0b, Interrupt & Trigger Mode		31		µs
I_{OZ}	Output Leakage current, $\overline{\text{ALERT}}$ pin	ALERT pin disabled, V_{OZ} = 5.5V		30		nA
DC Power						
V_{VCC_UV}	Under voltage threshold at VCC			2.1		V
V_{VCC_OV}	Over voltage threshold at VCC			5.9		V
I_{ACT}	Active mode current from VCC	$\overline{\text{CS}}$ high, VCC = 5.5V		3.4		mA
I_{STDBY}	Stand-by mode current from VCC	$\overline{\text{CS}}$ high, VCC = 5.5V		840		µA
I_{CFG}	Configuration mode current from VCC	$\overline{\text{CS}}$ high, VCC = 5.5V		60		µA
I_{SLP}	Sleep mode current from V_{CC}	$\overline{\text{CS}}$ high, VCC = 5.5V		1.5		µA
I_{DEEP_SLP}	Deep sleep mode current from VCC	$\overline{\text{CS}}$ high, VCC = 5.5V		5		nA

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Average Power						
I_{VCC_DCM}	Duty-cycle mode current consumption, one channel enabled, CONV_AVG = 000	Data active rate 1000Hz, V_{VCC} = 5V		245		µA
		Data active rate 100Hz, V_{VCC} = 5V		32		µA
		Data active rate 10Hz, V_{VCC} = 5V		4.5		µA
		Data active rate 1Hz, V_{VCC} = 5V		1.5		µA
	Duty-cycle mode current consumption, two channels enabled, CONV_AVG = 000	Data active rate 1000Hz, V_{VCC} = 5V		292		µA
		Data active rate 100Hz, V_{VCC} = 5V		39		µA
		Data active rate 10Hz, V_{VCC} = 5V		5		µA
		Data active rate 1Hz, V_{VCC} = 5V		1.6		µA
Operating Speed						
$t_{measure}$	Conversion time (1)	CONV_AVG = 000, OPERATING_MODE =010, only one channel enabled (2)		50		µs
		CONV_AVG = 101, OPERATING_MODE =010, only one channel enabled (3)		825		µs
f_{HFOSC}	Internal high-frequency oscillator speed		3	3.2	3.5	MHz
f_{LFOSC}	Internal low-frequency oscillator speed		13.5	16	19.5	KHz
Temperature Sensing						
T_{SENS_RANGE}	Temperature sensing range		-40		170	℃
T_{SENS_T0}	Reference temperature for $TADC_{T0}$		23	25	27	℃
$TADC_{T0}$	TEMP_RESULT decimal value @ T_{SENS_T0}			17522		
$TADC_{RES}$	Temp sensing resolution		58.2	60.0	61.8	LSB/℃
NRMS (T)	RMS (1 Sigma) temperature noise	CONV_AVG = 101		0.06		℃
NRMS (T)	RMS (1 Sigma) temperature noise	CONV_AVG = 000		0.35		℃

(1) To calculate the time between conversion request and the availability of the conversion result, add the initialization time to the $t_{measure}$ as explained in Comparing Operating Modes Table. For continuous conversion, the initialization time is applicable only for the first conversion.
(2) Add 25 µs for each additional channel enabled for conversion with CONV_AVG =000.
(3) For conversion with CONV_AVG =101, each axis data is collected 32 times. If an additional channel is enabled with CONV_AVG =101, add 32×25µs = 800µs to the $t_{measure}$ to calculate the conversion time for two axes.

6.6 Magnetic Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TMAG5170A1						
B_{IN_A1}	Linear magnetic range	x_RANGE(2) = 00b		±50		mT
		x_RANGE(2) = 01b		±25		mT
		x_RANGE(2) = 10b		±100		mT
$SENS_{50_A1}$	Sensitivity; X, Y, or Z axis	x_RANGE(2) = 00b		654		LSB/mT
$SENS_{25_A1}$		x_RANGE(2) = 01b		1308		LSB/mT
$SENS_{100_A1}$		x_RANGE(2) = 10b		326		LSB/mT
$SENS_{ER_25C_A1}$	Sensitivity error; X, Y, or Z axis, 25mT, 50mT range	T_A = 25℃		±0.5%	±2.5%	
$SENS_{ER_25C_A1}$	Sensitivity error; X, Y, or Z axis; 100mT range	T_A = 25℃		±0.5%	±3.5%	

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$SENS_{DR_A1}$ (1)	Sensitivity Drift from 25℃ value; X, Y, or Z axis; 25mT, 50mT range	MAG_TEMPCO = 00b, T_A = 25℃ to 125℃		±0.9%	±2.8%	
$SENS_{DR_A1}$ (1)	Sensitivity Drift from 25℃ value; X, Y, or Z axis; 25mT, 50mT range	MAG_TEMPCO = 00b, T_A = 25℃ to –40℃		±1.2%	±4.3%	
$SENS_{DR_A1}$ (1)	Sensitivity Drift from 25℃ value; X, Y, or Z axis; 25mT, 50mT range	MAG_TEMPCO = 01b, 10b, 11b; T_A = –40℃ to 125℃		±1.2%	±3.8%	
$SENS_{DR_A1}$ (1)	Sensitivity Drift from 25℃ value; X, Y, or Z axis; 100mT range	T_A = 25℃ to 125℃		±1.0%	±4.0%	
$SENS_{DR_A1}$ (1)	Sensitivity Drift from 25℃ value; X, Y, or Z axis; 100mT range	T_A = 25℃ to -40℃		±1.2%	±4.6%	
$SENS_{LDR_A1}$	Sensitivity Lifetime drift, X, Y, Z axis			±0.5%		
$SENS_{LER_XY_A1}$	Sensitivity Linearity Error, X, Y-axis	T_A = 25℃		±0.1%		
$SENS_{LER_Z_A1}$	Sensitivity Linearity Error, Z axis			±0.05%		
$SENS_{MS_XY_A1}$	Sensitivity mismatch among X-Y axes	T_A = 25℃		±0.02%	±3.5%	
$SENS_{MS_YZ_A1}$	Sensitivity mismatch among Y-Z axes	T_A = 25℃		±0.17%	±4.5%	
$SENS_{MS_XZ_A1}$	Sensitivity mismatch among X-Z axes	T_A = 25℃		±0.15%	±4.0%	
$SENS_{MS_DR_XY_A1}$ (1)	Sensitivity mismatch drift from 25℃ value; X-Y axes	T_A = 25℃ to 125℃		±0.8%	±4.0%	
$SENS_{MS_DR_XY_A1}$	Sensitivity mismatch drift from 25℃ value; X-Y axes	T_A = 25℃ to –40℃		±0.5%	±3.4%	
$SENS_{MS_DR_YZ_A1}$ (1)	Sensitivity mismatch drift from 25℃ value; Y-Z axes	T_A = 25℃ to 125℃		±0.7%	±3.5%	
$SENS_{MS_DR_YZ_A1}$	Sensitivity mismatch drift from 25℃ value; Y-Z axes	T_A = 25℃ to –40℃		±0.5%	±3.6%	
$SENS_{MS_DR_XZ_A1}$ (1)	Sensitivity mismatch drift from 25℃ value; X-Z axes	T_A = 25℃ to 125℃		±1.4%	±4.2%	
$SENS_{MS_DR_XZ_A1}$ (1)	Sensitivity mismatch drift from 25℃ value; X-Z axes	T_A = 25℃ to –40℃		±0.1%	±3.5%	
B_{off_A1}	Offset; X, Y, or Z axis; 25mT, 50mT range	T_A = 25℃		–10	±200	µT
B_{off_A1}	Offset, X, Y, or Z axis; 100mT range	T_A = 25℃		–150	±350	µT
$B_{off_DR_A1}$ (1)	Offset drift from 25℃ value; X or Y axis	T_A = 25℃ to 125℃		0	±5.0	µT/°C
$B_{off_DR_A1}$ (1)	Offset drift from 25℃ value; Z axis	T_A = 25℃ to 125℃		0	±1.5	µT/°C
$B_{off_DR_A1}$ (1)	Offset drift from 25℃ value; X or Y axis	T_A = 25℃ to –40℃	–6.5	–1.5	2.5	µT/°C
$B_{off_DR_A1}$ (1)	Offset drift from 25℃ value; Z axis	T_A = 25℃ to –40℃	-3.0	-1.0	1.0	µT/°C
$B_{off_DR_A1}$	Offset Lifetime drift			±50		µT
$N_{RMS_XY_FAST_A1}$	RMS (1 Sigma) magnetic noise (X or Y-axis)	x_RANGE(2) = 00b; CONV_AVG = 000b, T_A = 25℃		140	191	µT
$N_{RMS_XY_FAST_A1}$	RMS (1 Sigma) magnetic noise (X or Y-axis)	x_RANGE(2) = 00b; CONV_AVG = 000b, T_A = 125℃		170	228	µT
$N_{RMS_XY_SLOW_A1}$	RMS (1 Sigma) magnetic noise (X or Y-axis)	x_RANGE(2) = 00b; CONV_AVG = 101b, T_A = 25℃		24	34	µT
$N_{RMS_XY_SLOW_A1}$	RMS (1 Sigma) magnetic noise (X or Y-axis)	x_RANGE(2) = 00b; CONV_AVG = 101b, T_A = 125℃		30	41	µT
$N_{RMS_Z_FAST_A1}$	RMS (1 Sigma) magnetic noise (Z axis)	Z_RANGE = 00b; CONV_AVG = 000b, T_A = 25℃		61	76	µT
$N_{RMS_Z_FAST_A1}$	RMS (1 Sigma) magnetic noise (Z axis)	Z_RANGE = 00b; CONV_AVG = 000b, T_A = 125℃		70	84	µT

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$N_{RMS_Z_SLOW_A1}$	RMS (1 Sigma) magnetic noise (Z axis)	Z_RANGE = 00b; CONV_AVG = 101b, T_A = 25℃		11	14.2	µT
$N_{RMS_Z_SLOW_A1}$	RMS (1 Sigma) magnetic noise (Z axis)	Z_RANGE = 00b; CONV_AVG = 101b, T_A = 125℃		13	15.2	µT
$A_{ERR_Y_Z_00_101_A1}$ (3)	Y-Z Angle error in full 360 degree rotation, 25℃	x_RANGE(2) = 00b, CONV_AVG = 101b		±0.5		Degree
$A_{ERR_X_Z_00_101_A1}$ (3)	X-Z Angle error in full 360 degree rotation, 25℃	x_RANGE(2) = 00b, CONV_AVG = 101b		±0.5		Degree
$A_{ERR_X_Y_00_101_A1}$ (3)	X-Y Angle error in full 360 degree rotation, 25℃	x_RANGE(2) = 00b, CONV_AVG = 101b		±0.4		Degree
TMAG5170A2						
B_{IN_A2}	Linear magnetic range	x_RANGE(2) = 00b		±150		mT
		x_RANGE(2) = 01b		±75		mT
		x_RANGE(2) = 10b		±300		mT
$SENS_{150_A2}$	Sensitivity, X, Y, or Z axis	x_RANGE(2) = 00b		218		LSB/mT
$SENS_{75_A2}$		x_RANGE(2) = 01b		436		LSB/mT
$SENS_{300_A2}$		x_RANGE(2) = 10b		108		LSB/mT
$SENS_{ER_25C_A2}$	Sensitivity error; X, Y, or Z axis, 75mT, 150mT range	T_A = 25℃		±0.5%	±3.5%	
$SENS_{ER_25C_A2}$	Sensitivity error; X, Y, or Z axis, 300mT range	T_A = 25℃		±0.5%	±6.0%	
$SENS_{DR_A2}$ (1)	Sensitivity Drift from 25℃ value; X, Y, or Z axis; 75mT, 150mT range	T_A = –40℃ to 125℃		±0.5%	±4.5%	
$SENS_{DR_A2}$ (1)	Sensitivity Drift from 25℃ value; X, Y, or Z axis; 300mT range	T_A = 25℃ to 125℃		±0.5%	±4.0%	
$SENS_{DR_A2}$ (1)	Sensitivity Drift from 25℃ value; X, Y, or Z axis; 300mT range	T_A = 25℃ to –40℃		±1.6%	±6.2%	
$SENS_{LER_XY_A2}$	Sensitivity Linearity Error, X, Y-axis	T_A = 25℃		±0.1%		
$SENS_{LER_Z_A2}$	Sensitivity Linearity Error, Z axis	T_A = 25℃		±0.1%		
$SENS_{LDR_A2}$	Sensitivity Lifetime drift, X, Y, Z axis			±0.6%		
$SENS_{MS_XY_A2}$	Sensitivity mismatch among X-Y axes; 75mT, 150mT range	T_A = 25℃		±0.37%	±2.8%	
$SENS_{MS_XY_A2}$	Sensitivity mismatch among X-Y axes; 300mT range	T_A = 25℃		±0.42%	±5.8%	
$SENS_{MS_YZ_A2}$	Sensitivity mismatch among Y-Z axes; 75mT, 150mT range	T_A = 25℃		±0.41%	±4.3%	
$SENS_{MS_YZ_A2}$	Sensitivity mismatch among Y-Z axes; 300mT range	T_A = 25℃		±0.37%	±6.0%	
$SENS_{MS_XZ_A2}$	Sensitivity mismatch among X-Z axes; 75mT, 150mT range	T_A = 25℃		±0.38%	±3.6%	
$SENS_{MS_XZ_A2}$	Sensitivity mismatch among X-Z axes; 300mT range	T_A = 25℃		±1.2%	±7.5%	
$SENS_{MS_DR_XY_A2}$ (1)	Sensitivity mismatch drift from 25℃ value; X-Y axes; 75mT, 150mT range	T_A = –40℃ to 125℃		±0.5%	±4.0%	
$SENS_{MS_DR_XY_A2}$ (1)	Sensitivity mismatch drift from 25℃ value; X-Y axes; 300mT range	T_A = 25℃ to 125℃		±0.5%	±5.2%	
$SENS_{MS_DR_XY_A2}$ (1)	Sensitivity mismatch drift from 25℃ value; X-Y axes; 300mT range	T_A = 25℃ to -40℃		±0.9%	±7.6%	
$SENS_{MS_DR_YZ_A2}$ (1)	Sensitivity mismatch drift from 25℃ value; Y-Z axes; 75mT, 150mT range	T_A = –40℃ to 125℃		±0.4%	±4.0%	

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$SENS_{MS_DR_YZ_A2}$ (1)	Sensitivity mismatch drift from 25℃ value; Y-Z axes; 300mT range	T_A = 25℃ to 125℃		±0.2%	±5.4%	
$SENS_{MS_DR_YZ_A2}$ (1)	Sensitivity mismatch drift from 25℃ value; Y-Z axes; 300mT range	T_A = 25℃ to -40℃		±0.5%	±8.1%	
$SENS_{MS_DR_XZ_A2}$ (1)	Sensitivity mismatch drift from 25℃ value; X-Z axes; 75mT, 150mT range	T_A = –40℃ to 125℃		±0.2%	±5.5%	
$SENS_{MS_DR_XZ_A2}$ (1)	Sensitivity mismatch drift from 25℃ value; X-Z axes; 300mT range	T_A = –40℃ to 125℃		±1.1%	±6.6%	
B_{off_A2}	Offset; 75mT, 150mT range	T_A = 25℃		–50	±300	µT
B_{off_A2}	Offset; 300mT range	T_A = 25℃		–300	±900	µT
$B_{off_DR_A2}$ (1)	Offset drift from value at T_A = 25℃; X or Y axis; 75mT, 150mT range	T_A = 25℃ to 125℃		1.0	±5.5	µT/°C
$B_{off_DR_A2}$ (1)	Offset drift from value at T_A = 25℃; Z axis; 75mT, 150mT range	T_A = 25℃ to 125℃		–1.5	±3.5	µT/°C
$B_{off_DR_A2}$ (1)	Offset drift from value at T_A = 25℃; X or Y axis; 75mT, 150mT range	T_A = 25℃ to –40℃	–8.0	–3.0	2.0	µT/°C
$B_{off_DR_A2}$ (1)	Offset drift from value at T_A = 25℃; Z axis; 75mT, 150mT range	T_A = 25℃ to –40℃		–0.4	±5.0	µT/°C
$B_{off_DR_A2}$ (1)	Offset drift from value at T_A = 25℃; 300mT range	T_A = –40℃ to 125℃		±2.5	±12.0	µT/°C
$B_{off_DR_A2}$	Offset Lifetime drift			±50		µT
$N_{RMS_XY_FAST_A2}$	RMS (1 Sigma) magnetic noise (X or Y-axis)	x_RANGE(2) = 00b; CONV_AVG = 000b, T_A = 25℃		160	236	µT
$N_{RMS_XY_FAST_A2}$	RMS (1 Sigma) magnetic noise (X or Y-axis)	x_RANGE(2) = 00b; CONV_AVG = 000b, T_A =125℃		193	251	µT
$N_{RMS_XY_SLOW_A2}$	RMS (1 Sigma) magnetic noise (X or Y-axis)	x_RANGE(2) = 00b; CONV_AVG = 101b, T_A = 25℃		28	41	µT
$N_{RMS_XY_SLOW_A2}$	RMS (1 Sigma) magnetic noise (X or Y-axis)	x_RANGE(2) = 00b; CONV_AVG = 101b, T_A = 125℃		34	46	µT
$N_{RMS_Z_FAST_A2}$	RMS (1 Sigma) magnetic noise (Z axis)	Z_RANGE = 00b; CONV_AVG = 000b, T_A = 25℃		72	85	µT
$N_{RMS_Z_FAST_A2}$	RMS (1 Sigma) magnetic noise (Z axis)	Z_RANGE = 00b; CONV_AVG = 000b, T_A = 125℃		84	98	µT
$N_{RMS_Z_SLOW_A2}$	RMS (1 Sigma) magnetic noise (Z axis)	Z_RANGE = 00b; CONV_AVG = 101b, T_A = 25℃		13	16	µT
$N_{RMS_Z_SLOW_A2}$	RMS (1 Sigma) magnetic noise (Z axis)	Z_RANGE = 00b; CONV_AVG = 101b, T_A = –40℃ to 125℃		15	18	µT
$A_{ERR_Y_Z_00_101_A2}$ (3)	Y-Z Angle error in full 360 degree rotation, 25℃	x_RANGE(2) = 00b, CONV_AVG = 101b		±0.5		Degree
$A_{ERR_X_Z_00_101_A2}$ (3)	X-Z Angle error in full 360 degree rotation, 25℃	x_RANGE(2) = 00b, CONV_AVG = 101b		±0.5		Degree
$A_{ERR_X_Y_00_101_A2}$ (3)	X-Y Angle error in full 360 degree rotation, 25℃	x_RANGE(2) = 00b, CONV_AVG = 101b		±0.40		Degree

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE COMPENSATION						
TC	Temperature compensation (no compensation)	MAG_TEMPCO =00b		0		%/°C
TC	Temperature compensation (for NdBFe magnet)	MAG_TEMPCO =01b		0.12		%/°C
TC	Temperature compensation (for SmCo magnet)	MAG_TEMPCO =10b		0.03		%/°C
TC	Temperature compensation (for Ceramic magnet)	MAG_TEMPCO =11b		0.2		%/°C

(1) Drift at any temperature can be calculated from drift values at 125°C or –40°C. For example, drift at 85℃ = \((85 – 25) / (125 – 25\)) × (drift at 125℃); similarly, drift at –20℃ = \((25 – (–20\)) / (25 – (–40\))) × (drift at –40℃).
(2) x_RANGE denotes the X_RANGE, Y_RANGE, or Z_RANGE register bits
(3) Angle measurement is performed in static condition. The input sinusoidal magnetic fields have peak magnitudes equal to 80% of the magnetic full ranage. Offset and gain corrections have been performed at 25℃.

6.7 Power up Timing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} = 5.5V						
$t_{start_power_up}$	Time to start up after V_{VCC} supply voltage crossing V_{VCC_MIN}			246	350	µs
t_{start_sleep}	Time to activate from sleep mode			40	50	µs
t_{go_sleep}	Time to go into sleep mode after $\overline{CS}$ goes high			50		µs
$t_{start_deep_sleep}$	Time to start up from deep sleep mode			246	350	µs
$t_{start_deep_sleep}$	Time to go into deep sleep mode after $\overline{CS}$ goes high			75		µs
t_{stand_by}	Time to go to Stand-by mode from Configuration mode			90		µs
t_{spi_sleep}	Setup time between $\overline{CS}$ going low and SCK start during sleep mode			8	10	µs
V_{CC} =2.3V						
$t_{start_power_up}$	Time to start up after V_{CC} supply voltage crossing V_{CC_MIN}			260	500	µs
t_{start_sleep}	Time to activate from sleep mode			40	50	µs
t_{go_sleep}	Time to go into sleep mode after $\overline{CS}$ goes high			60		µs
$t_{start_deep_sleep}$	Time to start up from deep sleep mode			260	500	µs
$t_{start_deep_sleep}$	Time to go into deep sleep mode after $\overline{CS}$ goes high			75		µs
t_{stand_by}	Time to go to Stand-by mode from Configuration mode			90		µs
t_{spi_sleep}	Delay time between $\overline{CS}$ going low and SCK start during sleep mode			8	10	µs

6.8 SPI Interface Timing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI Interface						
f_{SPI}	SPI clock (SCK) frequency	LOAD = 25 pF			10	MHz
t_{whigh}	High time: SCK logic high time duration		45			ns
t_{wlow}	Low time: SCK logic low time duration		45			ns
t_{su_cs}	$\overline{CS}$ setup time: Time delay between falling edge of $\overline{CS}$ and rising edge of SCK		45			ns
t_{h_cs}	Hold time: Time between the falling edge of SCK and rising edge of $\overline{CS}$		45			ns

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd_soen}	Delay time: Time delay from falling edge of $\overline{CS}$ to data valid at SDO				45	ns
t_{pd_sodis}	Delay time: Time delay from rising edge of $\overline{CS}$ to SDO transition to tri-state				55	ns
t_{su_si}	SDI setup time: Setup time of SDI before the rising edge of SCK		25			ns
t_{h_si}	Hold time: Time between the rising edge of SCK to SDI valid		25			ns
t_{pd_so}	Propagation delay from falling edge of SCK to SDO				45	ns
t_{w_cs}	SPI transfer inactive time (time between two transfers) during which $\overline{CS}$ must remain high.	LOAD = 25 pF	100			ns
t_{spi_sleep}	Setup time between $\overline{CS}$ going low and SCK start during sleep mode			8	10	µs

6.9 Typical Characteristics

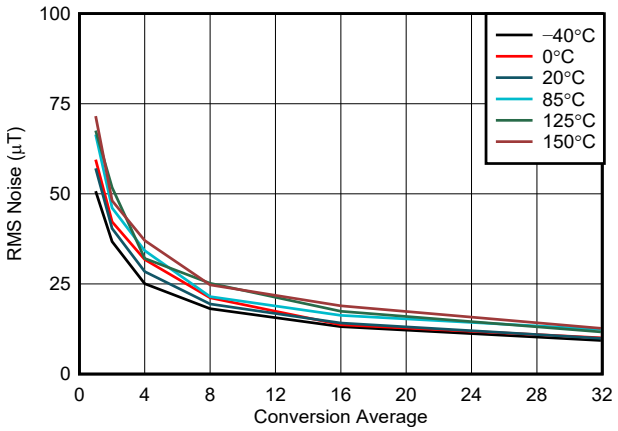

图 6-1. Z-Axis Noise vs. Conversion Average, 25-mT Range

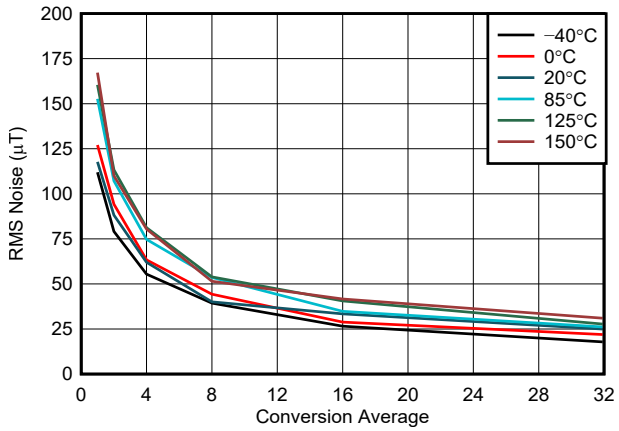

图 6-2. X, Y-Axis Noise vs. Conversion Average, 25-mT Range

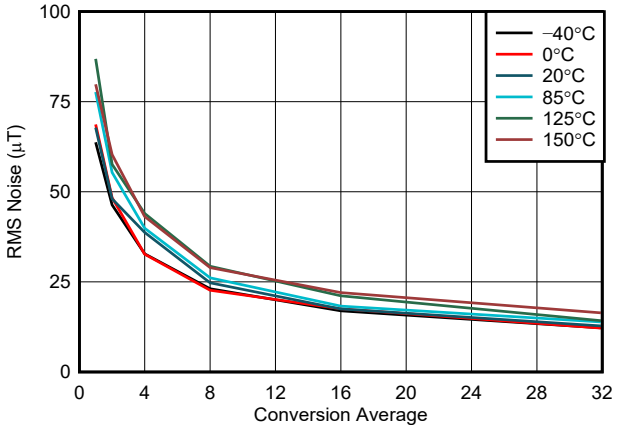

图 6-3. Z-Axis Noise vs. Conversion Average, 50-mT Range

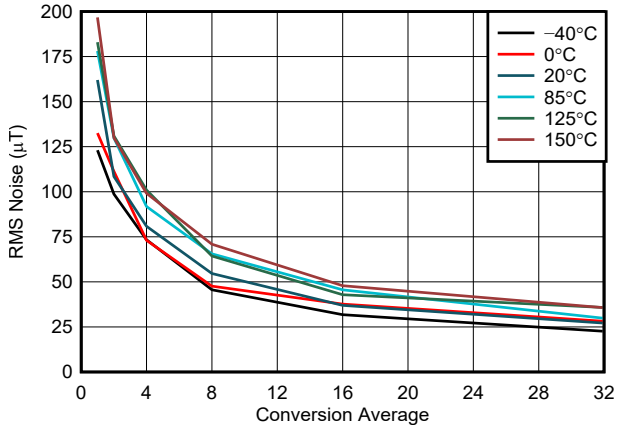

图 6-4. X, Y-Axis Noise vs. Conversion Average, 50-mT Range

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6.9 Typical Characteristics (continued)

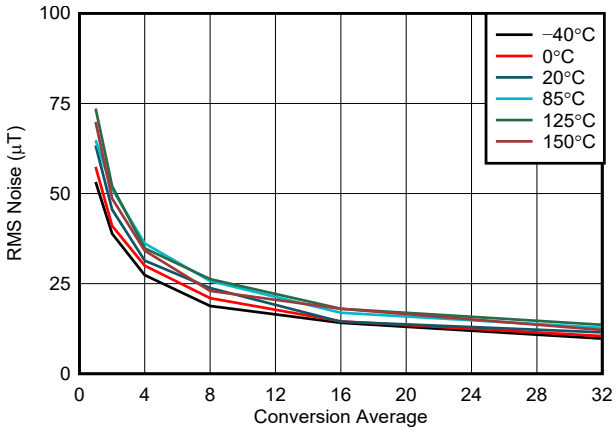

图 6-5. Z-Axis Input vs. Conversion Average, 75-mT Range

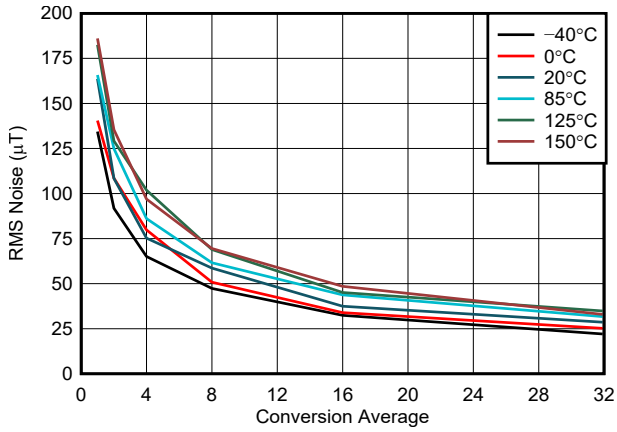

图 6-6. X, Y-Axis Noise vs. Conversion Average, 75-mT Range

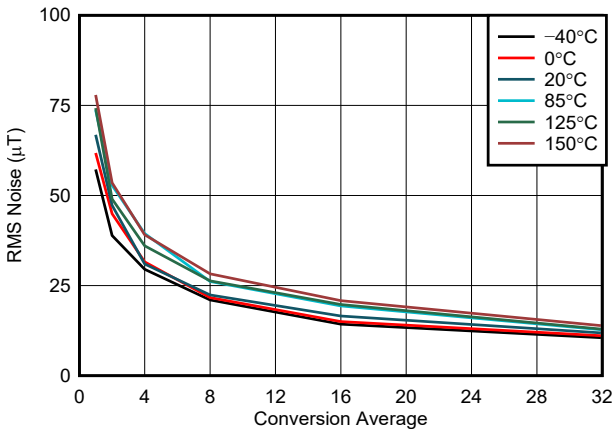

图 6-7. Z-Axis Noise vs. Conversion Average, 100-mT Range

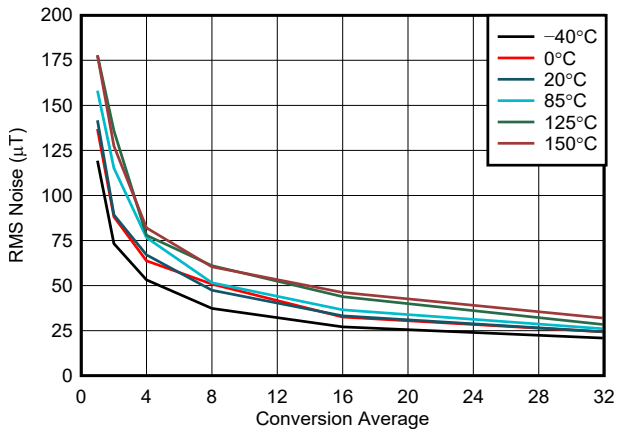

图 6-8. X, Y-Axis Noise vs. Conversion Average, 100-mT Range

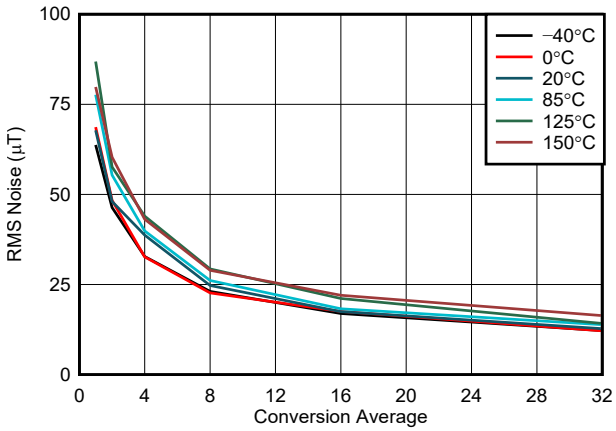

图 6-9. Z-Axis Noise vs. Conversion Average, 150-mT Range

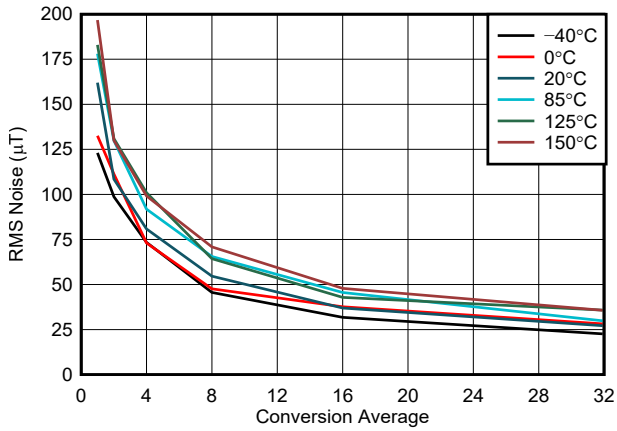

图 6-10. X, Y-Axis Noise vs. Conversion Average, 150-mT Range

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6.9 Typical Characteristics (continued)

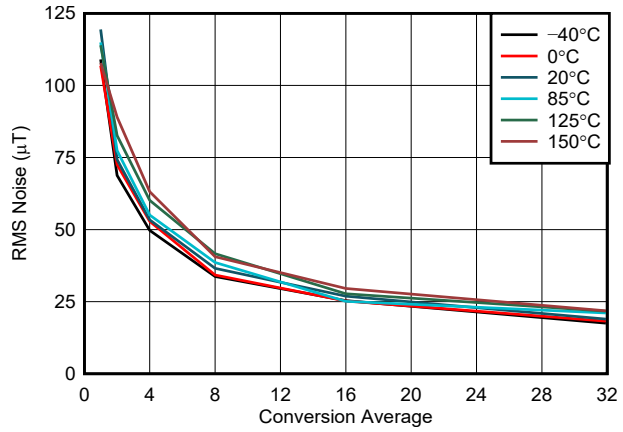

图 6-11. Z-Axis Noise vs. Conversion Average, 300-mT Range

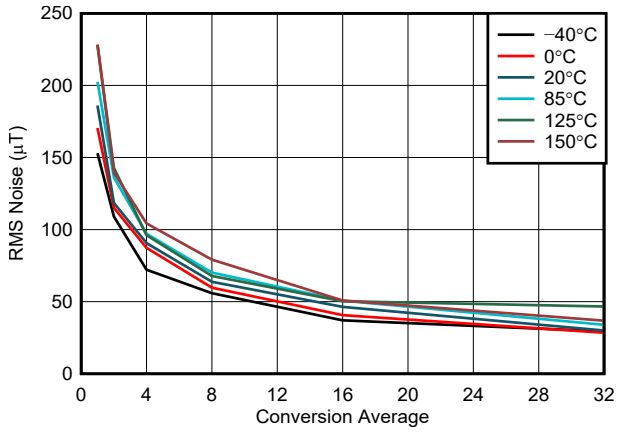

图 6-12. X, Y-Axis Noise vs. Conversion Average, 300-mT Range

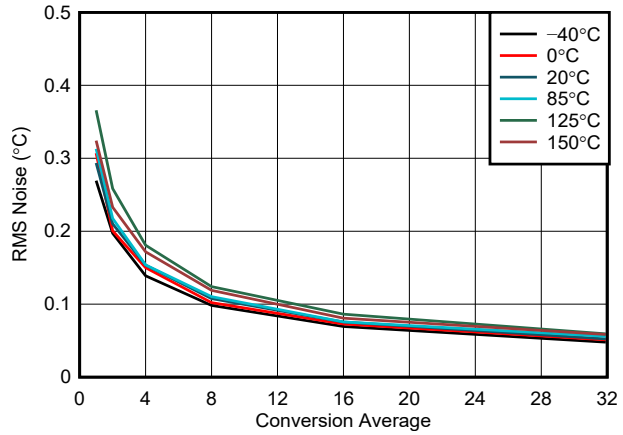

图 6-13. Temperature Sensor Noise vs. Conversion Average

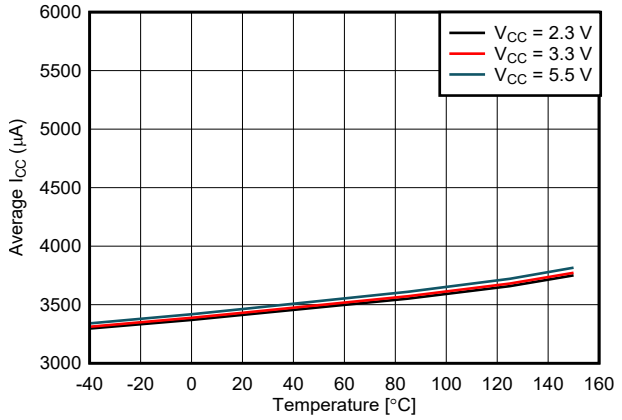

图 6-14. Active Mode Supply Current vs. Temperature

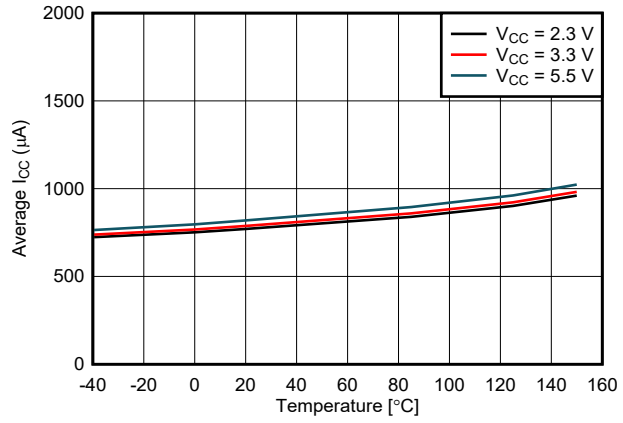

图 6-15. Standby Mode Supply Current vs. Temperature

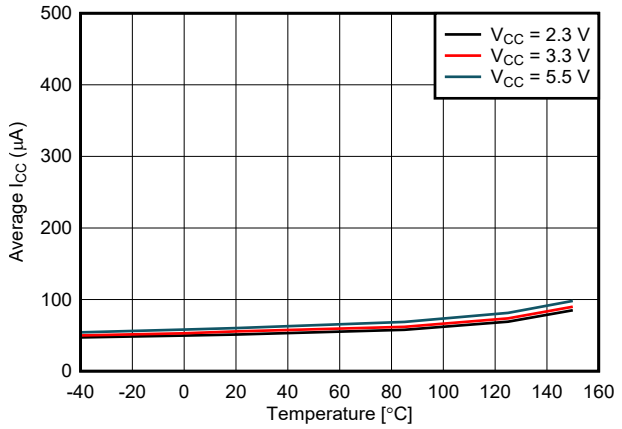

图 6-16. Configuration Mode Supply Current vs. Temperature

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6.9 Typical Characteristics (continued)

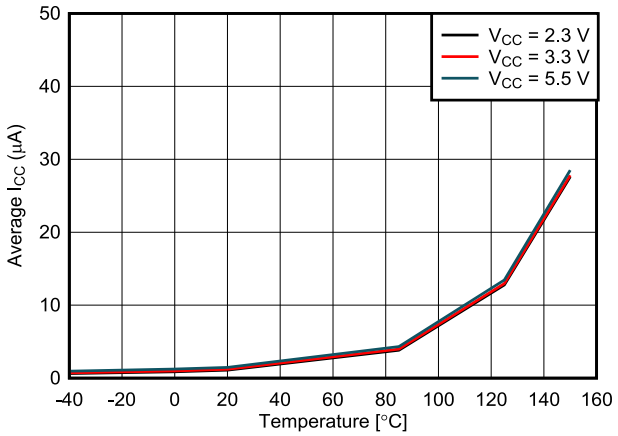

图 6-17. Sleep Mode Supply Current vs. Temperature

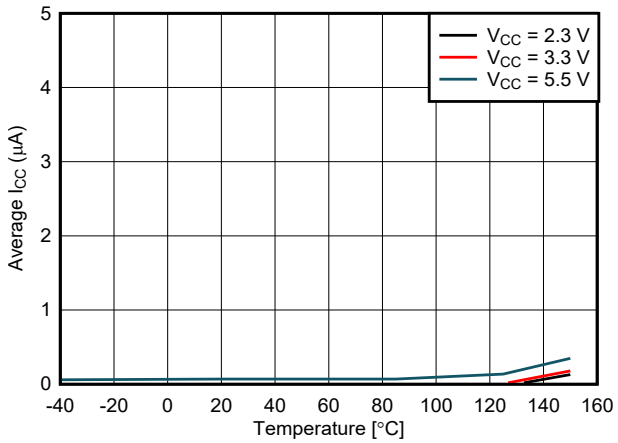

图 6-18. Deep Sleep Mode Supply Current vs. Temperature

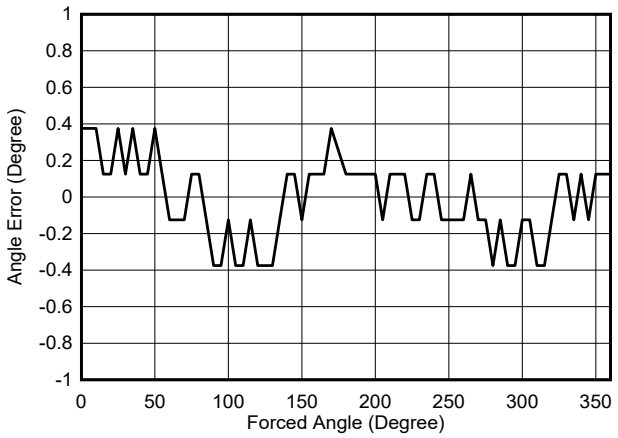

图 6-19. Angle Error at 25℃, X-Y Configuration, 50-mT Range

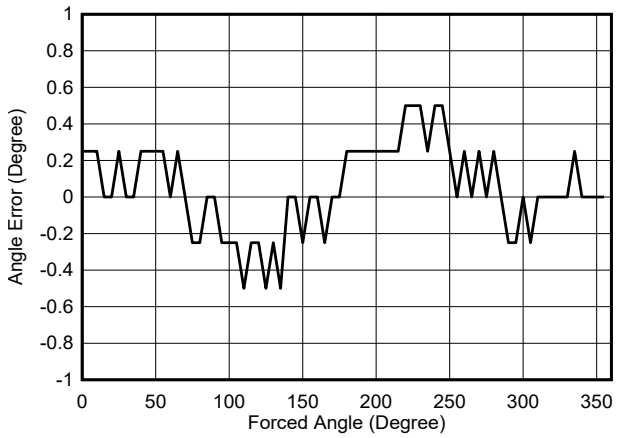

图 6-20. Angle Error at 25℃ , X-Z Configuration, 50-mT Range

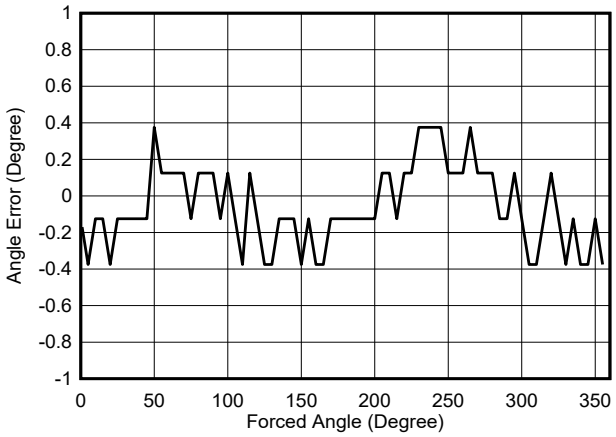

图 6-21. Angle Error at 25℃ , Y-Z Configuration, 50-mT Range

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7 Detailed Description

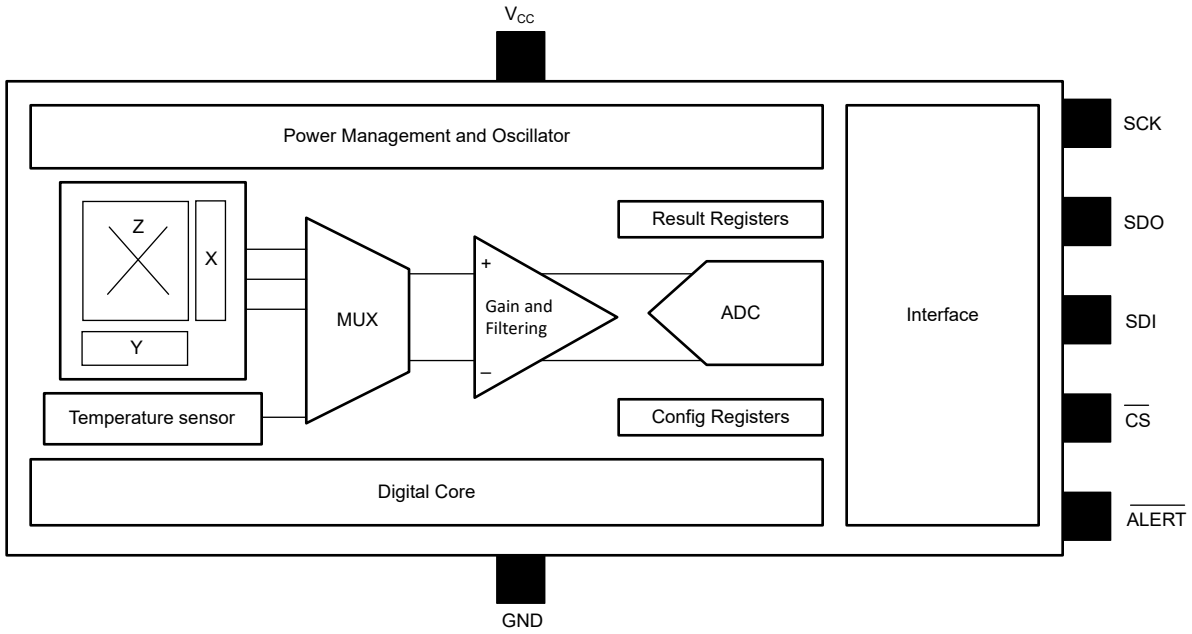
7.1 Overview

The TMAG5170-Q1 IC is based on the Hall-effect technology and precision mixed signal circuitry from Texas Instruments. The output signals (raw X, Y, Z Magnetic data and Die temperature data) is provided through the SPI. The device can be configured in multiple settings through user access registers through the SPI.

The IC consists of the following functional and building blocks:

- The Power Management & Oscillator block contains a low-power oscillator, biasing circuitry, undervoltage and overvoltage detection circuitry, and a fast oscillator.
- The sensing and temperature measurement block contains the Hall biasing, Hall sensors with multiplexers, noise filters, integrator circuit, temperature sensor, and the ADC. The Hall sensor data and temperature data are multiplexed through the same ADC.
- The Interface block contains the SPI control circuitry, ESD protection circuits, and all the I/O circuits. The TMAG5170-Q1 supports SPI along with integrated cyclic redundancy check (CRC).
- The diagnostic blocks are embedded in the circuitry to enable mandatory and user-enabled diagnostic checks.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Magnetic Flux Direction

The TMAG5170-Q1 is sensitive to the magnetic field component in X, Y, and Z directions. The X and Y fields are in plane with the package. The Z field is perpendicular to the top of the package. The device is sensitive to both magnetic north and south poles in each axis. As shown in 图 7-1, the device will generate positive ADC codes in response to a magnetic south pole in the proximity. Similarly, the device will generate negative ADC codes if magnetic north poles approach from the same directions.

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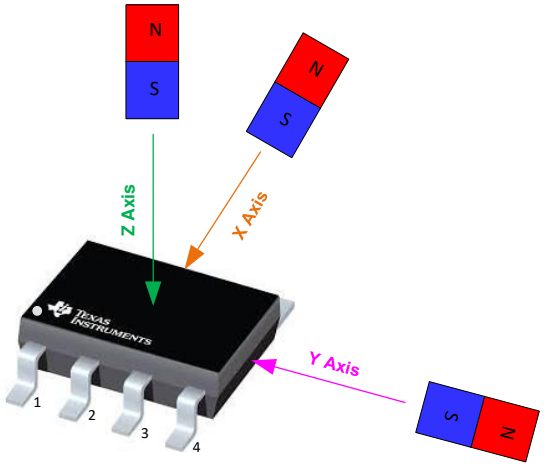

图 7-1. Direction of Applied Magnetic South Pole to Generate Positive ADC Codes

7.3.2 Sensor Location

图 7-2 shows the location of X, Y, Z Hall elements inside the TMAG5170-Q1.

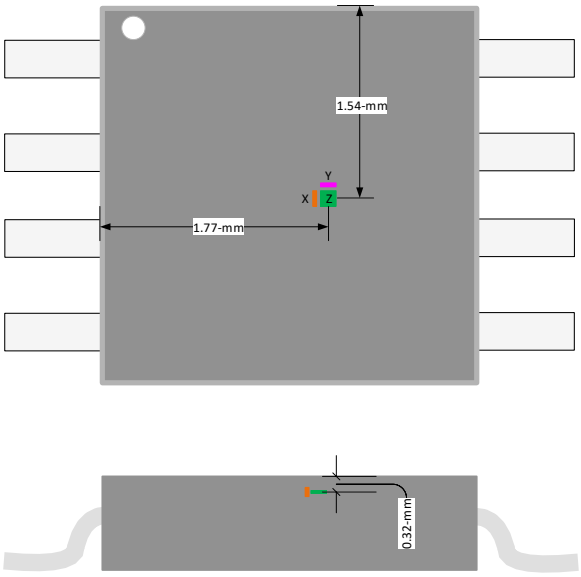

图 7-2. Location of X, Y, Z Hall Elements

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7.3.3 Magnetic Range Selection

表 7-1 shows the magnetic range selection for the TMAG5170-Q1 device. Each axis range can be independently selected irrespective of the others.

表 7-1. Magnetic Range Selection

	RANGE REGISTER SETTING	TMAG5170A1-Q1	TMAG5170A2-Q1	COMMENT
X Axis Field	X_RANGE = 00b	±50 mT	±150 mT	
	X_RANGE = 01b	±25 mT	±75 mT	Best resolution case
	X_ RANGE = 10b	±100 mT	±300 mT	Highest range, best SNR case
Y Axis Field	Y_RANGE = 00b	±50 mT	±150 mT	
	Y_RANGE = 01b	±25 mT	±75 mT	Best resolution case
	Y_RANGE = 10b	±100 mT	±300 mT	Highest range, best SNR case
Z Axis Field	Z_RANGE = 00b	±50 mT	±150 mT	
	Z_RANGE = 01b	±25 mT	±75 mT	Best resolution case
	Z_RANGE = 10b	±100 mT	±300 mT	Highest range, best SNR case

7.3.4 Update Rate Settings

The TMAG5170-Q1 offers multiple update rates for system design flexibility. 图 7-4 shows the different update rates for the TMAG5170-Q1 during continuous conversion.

表 7-2. Update Rate Settings

OPERATING MODE	REGISTER SETTING	UPDATE RATE			COMMENT
		SINGLE AXIS	TWO AXIS	THREE AXIS	
X, Y, Z Axis	CONV_AVG = 000b	20 kSPS	13.3 kSPS	10 kSPS	Fastest update rate
X, Y, Z Axis	CONV_AVG = 001b	13.3 kSPS	8.0 kSPS	5.7 kSPS	
X, Y, Z Axis	CONV_AVG = 010b	8.0 kSPS	4.4 kSPS	3.1 kSPS	
X, Y, Z Axis	CONV_AVG = 011b	4.4 kSPS	2.4 kSPS	1.6 kSPS	
X, Y, Z Axis	CONV_AVG = 100b	2.4 kSPS	1.2 kSPS	0.8 kSPS	
X, Y, Z Axis	CONV_AVG = 101b	1.2 kSPS	0.6 kSPS	0.4 kSPS	Best SNR case

7.3.5 ALERT Function

The $\overline{\text{ALERT}}$ pin of the TMAG5170-Q1 supports multiple operating modes targeting different applications.

7.3.5.1 Interrupt and Trigger Mode

With ALERT_MODE at default value of 0b, the $\overline{\text{ALERT}}$ output can be configured to generate an interrupt signal for microcontroller when a user-defined event occurs. A user-defined event can be a conversion completion or an error from diagnostic tests. The $\overline{\text{ALERT}}$ pin can also be used in this mode to trigger a conversion start using the TRIGGER_MODE register bit.

7.3.5.2 Magnetic Switch Mode

With ALERT_MODE set at 1b, the $\overline{\text{ALERT}}$ output is configured as a magnetic switch. One or multiple magnetic channels can be selected in the ALERT_CONFIG register. The magnetic switch thresholds are determined by the *_THRX_CONFIG register bits setting. If the measured magnetic field is greater than *_HI_THRESHOLD, or smaller than *_LO_THRESHOLD, the $\overline{\text{ALERT}}$ output will assert low. 图 7-3 shows the magnetic switch function using the X-axis magnetic field as an example.

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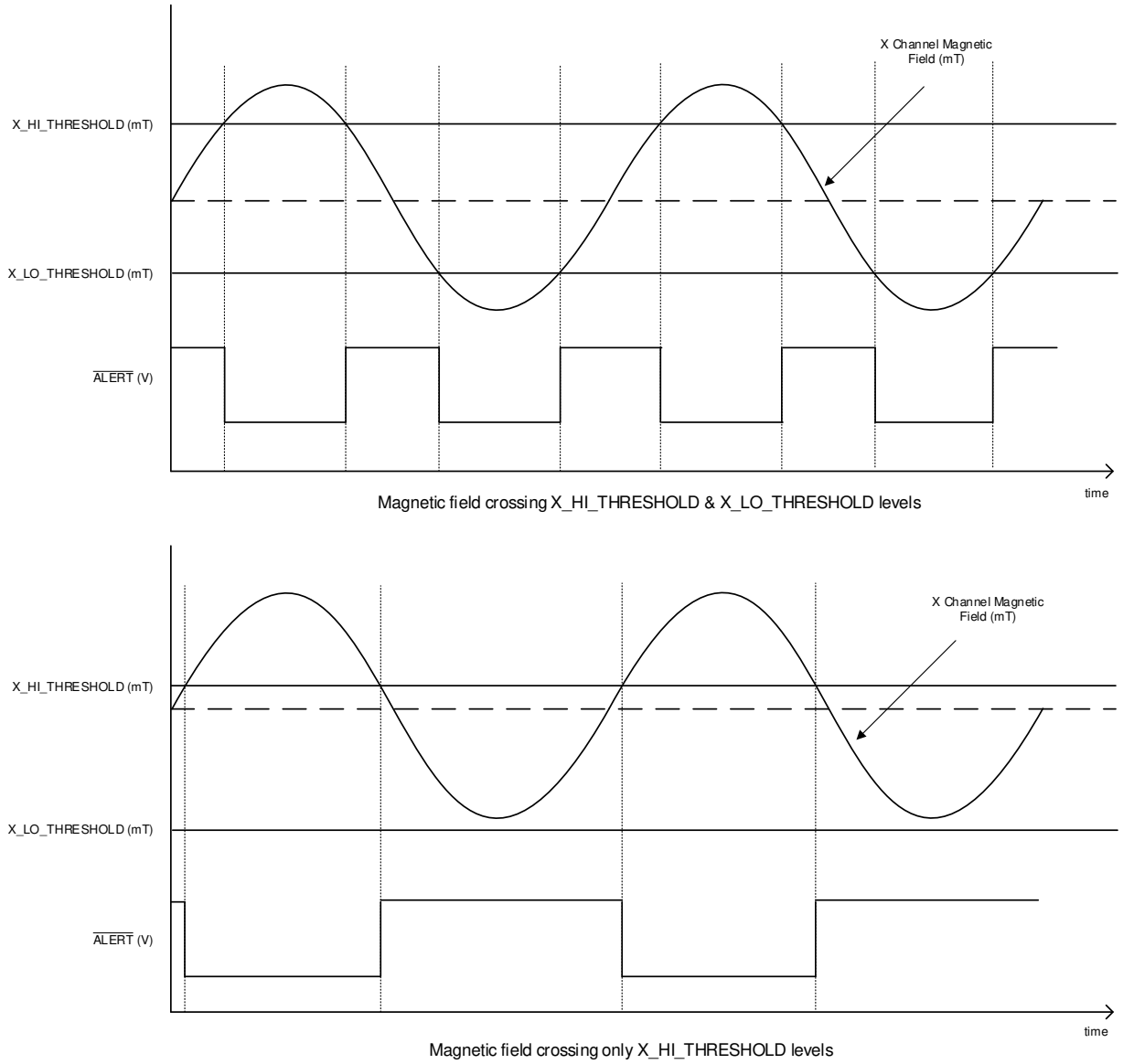

图 7-3. ALERT Pin Working as Magnetic Switch

7.3.6 Threshold Count

The THRX_COUNT bits in the ALERT_CONFIG register offer robust noise filtering and immunity against false tripping while the TMAG5170-Q1 implements the $\overline{\text{ALERT}}$ function for a specific magnetic or temperature threshold crossing. With THRX_COUNT at default 00b, only one measured value must cross the threshold to be considered a valid threshold crossing event. With THRX_COUNT at 11b, four successive measured values must cross the threshold to be considered a valid threshold crossing. An internal counter tracks and records the number of threshold crossing for a given sensor.

The counter resets if any of the below events occur:

- The device meets the threshold cross count for the specified number per the THRX_COUNT bits, the corresponding *CH_THX bit(s) are set, and the SPI read of the SYS_STATUS register has occurred
- If a measured result does not cross the threshold

When the $\overline{\text{ALERT}}$ pin is configured to work as a magnetic switch, the threshold count is active for both low-to-high and high-to-low transitions, offering noise immunity in both directions of the threshold cross.

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7.3.7 Diagnostics

The TMAG5170-Q1 supports several device and system level diagnostics features to detect, monitor, and report failures during the device operation.

In the event of a failure, the TMAG5170-Q1 reports back to the controller through the following mechanisms:

- ERROR_STAT bit during the SDO read frame
- Direct read of the status registers through the SPI
- $\overline{\text{ALERT}}$ pin response to indicate a failure, if enabled
- No response through SDO line, or CRC error during SPI communication

The TMAG5170-Q1 performs the following device and system level checks:

7.3.7.1 Memory CRC Check

This diagnostic mechanism checks the content of the internal memory by comparing a calculated CRC of the read content against a factory-programmed expected CRC value. During runtime, when the internal memory is read again for configuration for different channels, the CRC is checked again, providing detection of memory errors even during runtime.

Run Mode	Continuous
Configuration Register(s)	N/A
Fault Register Bit	TRIM_STAT
Impact if disabled	N/A. Cannot be disabled

7.3.7.2 $\overline{\text{ALERT}}$ Integrity Check

This diagnostic mechanism checks and compares the read back value of the $\overline{\text{ALERT}}$ pin to the value that is driven by the device. This will check the presence of an external short on $\overline{\text{ALERT}}$ pin to a higher voltage such as VCC which will prevent device to indicate a fault. When the controller is driving the $\overline{\text{ALERT}}$ pin to trigger a measurement, it can read the ALRT_LVL bit to check if the correct polarity of the $\overline{\text{ALERT}}$ was detected by the device, thus checking any failures on the pin.

Run Mode	Continuous
Configuration Register(s)	N/A
Fault Register Bit	ALRT_DRV and ALRT_LVL
Impact if disabled	When driven by device N/A. Cannot be disabled. When driven by controller, device may not detect a new measurement command and still report old measurement data.

7.3.7.3 VCC Check

This diagnostic mechanism continuously checks the external voltage supply on VCC pin and flags a fault if the supply is out of range.

Run Mode	Continuous
Data Sheet Parameters	V_{VCC_UV}, V_{VCC_OV}
Fault Register Bit	VCC_UV and VCC_OV
Impact if disabled	N/A. Cannot be disabled.

7.3.7.4 Internal LDO Under Voltage Check

This diagnostic mechanism continuously monitors the internal regulator that supplies the critical analog blocks and Hall sensor biasing, and flags a fault if the internal regulator falls below a threshold after which the accuracy of the magnetic field measurement cannot be guaranteed.

Run Mode	Continuous
Data Sheet Parameters	N/A
Fault Register Bit	LDO_STAT

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Impact if disabled	N/A. Cannot be disabled.

7.3.7.5 Digital Core Power-on Reset Check

This diagnostic mechanism continuously monitors the internal regulator that supplies the internal digital core, and puts the device in reset if the digital core cannot function reliably. The occurrence of the fault is detected by reading the CFG_RESET bit which can only be set at power up or if the digital core was reset.

Run Mode	Continuous
Data Sheet Parameters	N/A
Fault Register Bit	CFG_RESET
Impact if disabled	N/A. Cannot be disabled.

7.3.7.6 SDO Output Check

This diagnostic mechanism continuously compares the internally driven value by device on the SDO pin to the read-back value on SDO pin to detect any shorts to ground or power supply.

Run Mode	Continuous, every time a SPI transaction is initiated
Data Sheet Parameters	N/A
Fault Register Bit	SDO_DRV
Impact if disabled	N/A. Cannot be disabled.

7.3.7.7 Communication CRC Check

This diagnostic mechanism for every SPI transaction will compute the CRC of the received SPI frame from the controller and check the CRC against the CRC value transmitted by the controller, and flag a fault if the values do not match. The device also embeds a CRC value as part of the SPI frame in the response for the controller to check the integrity of the received data. This check detects faults with SPI communication block in digital core and the SPI I/O buffers and also controller to check for any faults on the SPI external to the device.

Another check is also run in the background that counts the number of SPI clocks in a SPI frame and flags a fault if the number of clocks sent by the controller is not same as the expected value. This can help controller detect any issues with the SPI.

Run Mode	Continuous, every time a SPI transaction is initiated
Configuration Register(s)	CRC_DIS to disable CRC in the SPI protocol
Fault Register Bit	CRC_STAT, FRAME_STAT
Impact if disabled	If CRC is disabled, then any fault with SPI communication will not be detected and incorrect value of measured field can be reported.

7.3.7.8 Oscillator Integrity Check

This diagnostic mechanism allows the controller to check any hardware fault with the internal oscillator. With this check, any drift of internal oscillators can be checked. The high-frequency oscillator is critical for precision measurement of the magnetic field and low-power oscillator is critical to control wake-up and sleep mode and other state machine control.

To run this check, external software code on the controller is required. The controller has to instate the check by setting the OSC_CNT_CTL bits to select a particular oscillator and start the internal count on the device. At the same time, the controller should also start a counter using its own timebase. After a pre-determined time, the controller should issue a stop to the oscillator count by setting OSC_CNT_CTL=0x3 and read the OSC_COUNT. The read value of the OSC_COUNT should not exceed the value based off maximum f_{HFOSC}, f_{LFPOSC} in the specification section. Variation of controller clock speed and SPI communication timing need to be considered while calculating the error margin for the OSC_COUNT.

Run Mode	On-demand as run by the external controller
Data Sheet Parameter(s)	f_{HFOSC}, f_{LFPOSC}

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Configuration Register(s)	OSC_CNT_CTL
Fault Register Bit	OSC_COUNT
Impact if disabled	If the controller decides not to run this test, then any drift of HF oscillator can impact the accuracy of the reported sensor data

7.3.7.9 Magnetic Field Threshold Check

This diagnostic mechanism allows the controller to monitor the external applied field. The controller can use this check to determine if a magnetic field is present within specified thresholds. This check, though used as check at system level, can also indicate any gross problems with the signal path if a field much outside the expected range is detected and reported.

To run this check, the controller must enable the check separately for each axis and also set the thresholds for each axis independently. The user can configure the $\overline{\text{ALERT}}$ pin to toggle if the threshold crossed, which is also reported in the user register.

Run Mode	Every time a magnetic measurement is initiated and completed
Configuration Register(s)	X_HLT_EN, Y_HLT_EN, Z_HLT_EN to enable test. X_THRX_CONFIG, Y_THRX_CONFIG, Z_THRX_CONFIG to set threshold
Fault Register Bit	XCH_THX, YCH_THX, ZCH_THX
Impact if disabled	If disabled, it does not have impact on device-level failure detection but at system level. Examples of system failure would be loss of magnet, magnet too far, or too close to the sensor.

7.3.7.10 Temperature Alert Check

This diagnostic mechanism allows the controller to monitor the junction temperature of the die, which is also an indication of the ambient temperature as the device does not generate significant self-heating. This is useful to monitor the temperature at the system level accurately and alert the controller if the temperature is exceeded. It can also be used to warn the controller if the die temperature due to some internal failure has increased beyond the expected range.

To run this check, the controller must enable the temperature check and set the threshold. The user can configure the $\overline{\text{ALERT}}$ pin to toggle if the threshold crossed, which is also reported in the user register.

Run Mode	Every time a magnetic measurement is initiated and completed
Configuration Register(s)	T_HLT_EN to enable test. T_THRX_CONFIG to set threshold
Fault Register Bit	TEMP_THX
Impact if disabled	If disabled, it does not have impact on device-level failure detection but at system level increase or decrease of temperature.

7.3.7.11 Analog Front-End (AFE) Check

This diagnostic mechanism allows the controller to check the performance of the analog signal path. In this check, the device disconnects the Hall sensor from the signal path and uses an alternate resistance bridge to create a known, predetermined signal as an input to the signal path. This mechanism then checks if the measured digital value compared to a fixed value from the factory is within a pre-programmed, factory-determined value. This mechanism can detect issues with multiplexers, offset cancellation mechanism, the gain stages, the low-pass filter, and the ADC, as well.

To run this check, the controller must enable the check and set the scheduling for the run. During this check, the AFE is not available for magnetic field conversion. The user can configure the $\overline{\text{ALERT}}$ pin to toggle if an error is detected. This error is also reported in the user register.

Run Mode	Every time a magnetic measurement is initiated and completed
Configuration Register(s)	DIAG_EN to enable test. DIAG_SEL to schedule when the test is run
Fault Register Bit	SENS_STAT
Impact if disabled	If disabled, any failures or drift with the analog front-end signal path may not be detected.

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7.3.7.12 Hall Resistance and Switch Matrix Check

This diagnostic mechanism allows the controller to check if the sensitivity of the Hall sensor is within the factory-determined limits by checking the resistance of the Hall-effect sensor. In this check, the biasing and multiplexing control of all directions of the Hall sensor (X, Y and Z) are also checked.

To run this check, the controller must enable the check and set the scheduling for the run. During this check, the Hall sensor is not available for magnetic field conversion. The user can configure the $\overline{\text{ALERT}}$ pin to toggle if an error is detected. This error is also reported in the user register.

Run Mode	Every time a magnetic measurement is initiated and completed
Configuration Register(s)	DIAG_EN to enable test. DIAG_SEL to schedule when the test is run
Fault Register Bit	ZHS_STAT, YHS_STAT and XHS_STAT
Impact if disabled	If disabled, any failures or drift in the Hall-effect sensor properties and biasing will not be detected, leading to potentially incorrect magnetic field conversion

7.3.7.13 Hall Offset Check

This diagnostic mechanism allows the controller to check if the offset of the Hall sensor is within the factory-determined limits and the offset cancellation circuitry is working properly.

To run this check, the controller must enable the check and set the scheduling for the run. During this check, the AFE is not available for magnetic field conversion. The user can configure the $\overline{\text{ALERT}}$ pin to toggle if an error is detected. This error is also reported in the user register.

Run Mode	Every time a magnetic measurement is initiated and completed
Configuration Register(s)	DIAG_EN to enable test. DIAG_SEL to schedule when the test is run
Fault Register Bit	SENS_STAT
Impact if disabled	If disabled, any failures with offset cancellation mechanism or large drift of Hall-effect sensor may not be detected, leading to potentially incorrect magnetic field conversion.

7.3.7.14 ADC Check

This diagnostic mechanism checks ADC functionality and conversion. This check is done by converting a known bandgap voltage, which is completely independent of the ADC reference, and comparing the voltage against the factory-determined tolerance limits.

To run this check, the controller must enable the check and set the scheduling for the run. During this check the AFE is not available for magnetic field conversion. The user can configure the $\overline{\text{ALERT}}$ pin to toggle if an error is detected. This error is also reported in the user register.

Run Mode	Every time a magnetic measurement is initiated and completed
Configuration Register(s)	DIAG_EN to enable test. DIAG_SEL to schedule when the test is run
Fault Register Bit	TEMP_STAT
Impact if disabled	If disabled, any failures with ADC conversion will not be detected, leading to potentially incorrect errors in the converted magnetic field values.

7.4 Device Functional Modes

7.4.1 Operating Modes

The TMAG5170-Q1 supports multiple operating modes for wide array of applications as explained in 图 7-4. The device starts powering up after the VCC supply crosses the minimum threshold as specified in the *Recommended Operating Conditions* table. Any particular operating mode can be selected by setting the corresponding OPERATING_MODE register bits.

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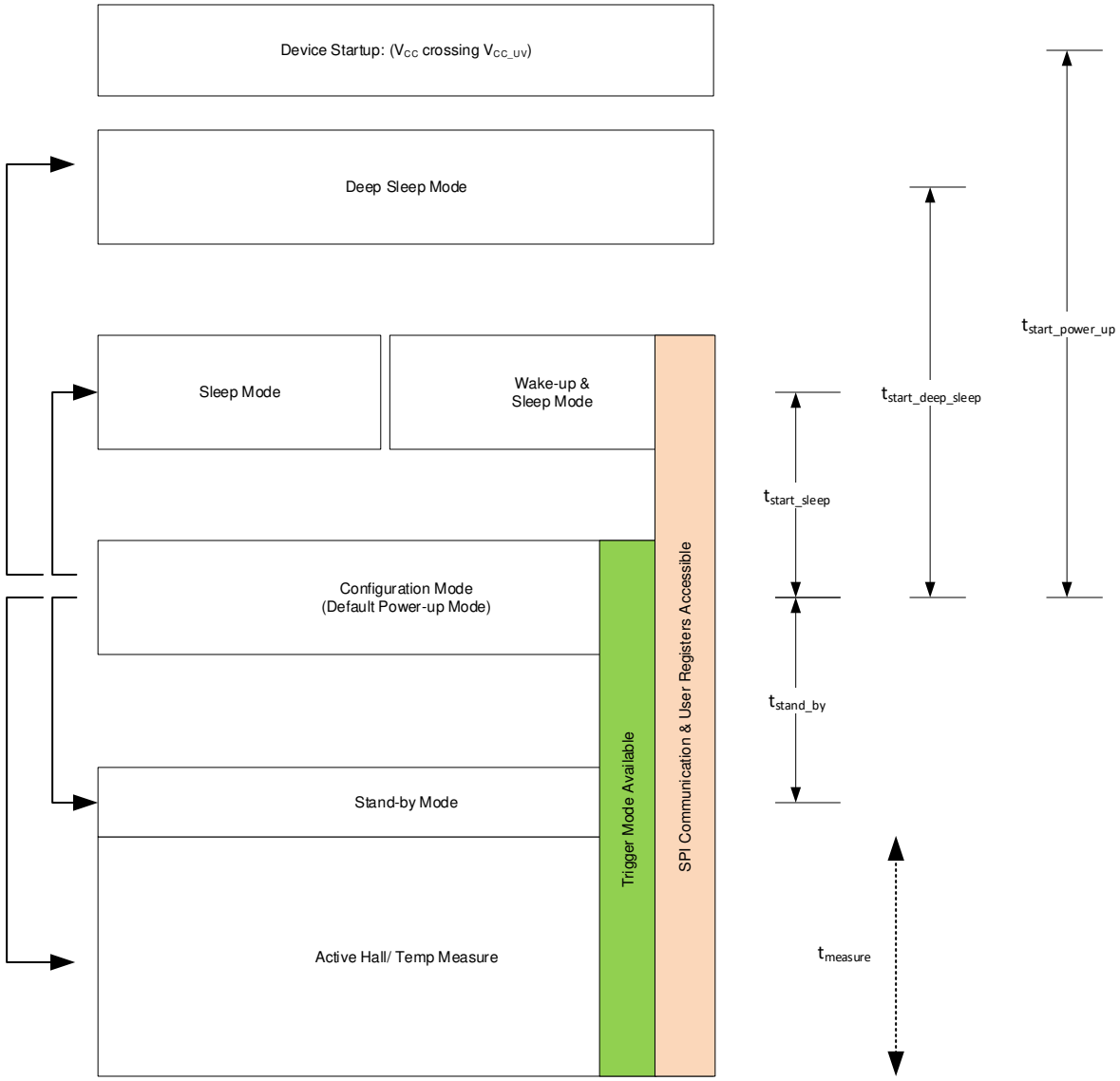

图 7-4. TMAG5170-Q1 Power-Up Sequence

表 7-3 shows different power saving modes of the TMAG5170-Q1.

表 7-3. Comparing Operating Modes

OPERATING MODE	DEVICE FUNCTION	INITIALIZATION TIME TO START CONVERSION(1)	DATA CONVERSION
Active Conversion	Continuously measuring X, Y, Z axis, or temperature data	10 µs	Supports continuous and trigger mode conversion
Standby Mode	Device is ready to accept SPI commands and start active conversion	35 µs	Supports trigger mode conversion
Configuration Mode	SPI and user configuration registers active	t_{stand_by} + 35 µs	Supports trigger mode conversion
Wake-up & Sleep Mode	Wakes up at a certain interval to measure the X, Y, Z axis, or temperature data	t_{start_sleep} + t_{stand_by} + 35 µs	1, 5, 10, 15, 20, 30, 100, 500, and 1000-ms intervals supported(1).
Sleep Mode	Device retains key configuration settings, and last measurement data	t_{start_sleep} + t_{stand_by} + 35 µs	The microcontroller can use sleep mode to implement other power saving intervals not supported by wake-up and sleep mode.

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表 7-3. Comparing Operating Modes (continued)

OPERATING MODE	DEVICE FUNCTION	INITIALIZATION TIME TO START CONVERSION(1)	DATA CONVERSION
Deep-sleep Mode	Device does not retain key configuration settings, and last measurement data	$t_{start_deep_sleep}$ + t_{stand_by} + 35 µs	No conversion start is supported during deep-sleep mode

(1) The timing numbers are typical parameters. Their value may vary depending on the internal oscillator frequency.

7.4.1.1 Active Mode

The TMAG5170-Q1 converts the magnetic sensor or temperature data during active mode. Active mode supports both continuous conversion and trigger mode conversion based off the OPERATING_MODE setting. Continuous operation at this mode is useful for applications where the fastest data conversion is required, and power budget is not stringent. In the Active trigger mode, a controller can trigger a conversion through one of several trigger mechanisms as described in the TRIGGER_MODE register bits. When the conversion started, the time it takes to finish a conversion is denoted by $t_{measure}$. The conversion time can vary widely based off the MAG_CH_EN, CONV_AVG, DIAG_SEL, and DIAG_EN register bits setting. The average current consumption during the active conversion is I_{ACT}.

7.4.1.2 Standby Mode

In the standby mode, the TMAG5170-Q1 is ready to start sensor conversion with a trigger command from a controller. Several trigger methods are supported as defined in the TRIGGER_MODE register bits. During this operating mode the relevant analog and digital support circuitry remain active to enable a faster conversion start. The average current consumption during this mode is denoted by I_{STDBY}. The time it takes for the device to go to standby mode from configuration mode is denoted by t_{stand_by}.

7.4.1.3 Configuration Mode (DEFAULT)

At power up, the TMAG5170-Q1 goes into the default configuration mode. In this mode, the SPI communication and user register access are enabled. A controller may configure the device to select the desired operating mode, sensor data conversion, enable/ disable diagnostic features, and so forth. The average current consumption during this mode is denoted by I_{CFG}. Similar to the standby mode, the configuration mode also supports sensor conversion start with a trigger. However, the configuration mode takes longer time to start the sensor conversion, and consumes approximately ten times less current compared to standby mode.

7.4.1.4 Sleep Mode

The TMAG5170-Q1 supports the sleep mode where it retains the user configuration settings and previous conversion results. A controller can wake up the device from sleep mode through either the SPI communication or the $\overline{\text{ALERT}}$ signal. The average power consumption in this mode is denoted by I_{SLP}. The time it takes for the device to go to the configuration mode from the sleep mode is denoted by t_{start_sleep}.

7.4.1.5 Wake-Up and Sleep Mode

The TMAG5170-Q1 supports the wake-up and sleep mode where the device is configured to wake up at a certain time interval, and perform the sensor conversion as defined in the SENSOR_CONFIG register setting. When the sensor conversion is complete, an $\overline{\text{ALERT}}$ signal can be generated to notify the controller that the new conversion data is ready. It is possible to generate an $\overline{\text{ALERT}}$ signal only in the event a particular magnetic or temperature threshold is exceeded. Detail setting on $\overline{\text{ALERT}}$ signal is specified in the ALERT_CONFIG register. A controller can wake up the TMAG5170-Q1 and access the conversion data at any time. The average power consumption in the wake-up and sleep mode is denoted by I_{VCC_DCM}. The time it takes for the device to go to configuration mode from wake-up and sleep mode is denoted by t_{start_sleep}.

7.4.1.6 Deep-Sleep Mode

For ultra-low power system, the TMAG5170-Q1 supports a deep-sleep mode to conserve power. In this mode, the TMAG5170-Q1 does not retain the user configuration or previous result data. The device reverts back to factory setting in this mode. The average power consumption in this mode is I_{DEEP_SLP}. The time it takes for the device to go to the configuration mode from the deep-sleep mode is denoted by t_{start_sleep}.

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7.5 Programming

7.5.1 Data Definition

7.5.1.1 Magnetic Sensor Data

The X, Y, and Z magnetic sensor data are stored in the X_CH_RESULT, Y_CH_RESULT, and Z_CH_RESULT registers, respectively. The 12-bit ADC output is stored in 16-bit result registers in 2's complement format as shown in 图 7-5. With fastest conversion (CONV_AVG = 000b), the ADC output loads the 12 MSB bits of the 16-bit result register along with 4 LSB bits as zeros. With CONV_AVG ≠ 000b, all the 16 bits are used to store the results. With DATA_TYPE = 00b, the 16-bit magnetic sensor data can be accessed through regular 32-bit SPI read. Use 方程式 1 to calculate the measured magnetic field.

$$B = \frac{-\left(D_{15} \times 2^{15}\right) + \sum_{i=0}^{14} D_i \times 2^i}{2^{16}} \times 2\left|B_R\right| \quad (1)$$

where

- B is magnetic field in mT.
- D_i is the data bit as shown in 图 7-5.
- B_R is the magnetic range in mT for the corresponding channel.

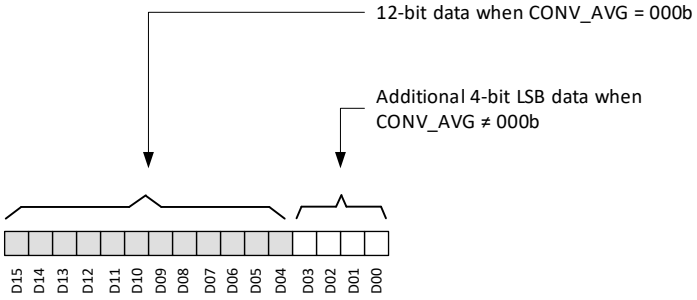

图 7-5. Magnetic Sensor Data Definition

With DATA_TYPE ≠ 00b, the 12 MSB bits (D04 to D15) from the magnetic result registers can be accessed. In this mode, use 方程式 2 to calculate the measured magnetic field.

$$B = \frac{-\left(D_{15} \times 2^{11}\right) + \sum_{i=4}^{14} D_i \times 2^{i-4}}{2^{12}} \times 2\left|B_R\right| \quad (2)$$

7.5.1.2 Temperature Sensor Data

The TMAG5170-Q1 temperature sensor will measure temperature from –40°C to 170°C. 图 7-6 shows the temperature stored in the 16-bit TEMP_RESULT register. With DATA_TYPE = 00b, the 16-bit temperature data can be accessed through regular 32-bit SPI read. Use 方程式 3 to calculate the temperature.

$$T = T_{SENS_T0} + \frac{TADC_T - TADC_{T0}}{TADC_{RES}} \quad (3)$$

where

- T is the measured temperature in degree Celsius.
- T_{SENS_T0} is the reference temperature in degree Celsius as listed in the *Electrical Characteristics* table.
- $TADC_{RES}$ is the change in ADC code per degree Celsius as listed in the *Electrical Characteristics* table.
- $TADC_{T0}$ is the TEMP_RESULT decimal value at reference temperature, T_{SENS_T0} as listed in the *Electrical Characteristics* table.
- $TADC_T$ is the measured TEMP_RESULT decimal value for temperature T.

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With DATA_TYPE ≠ 00b, the 12 MSB bits from the TEMP_RESULT register can be accessed. In this mode, use 方程式 4 to calculate the temperature.

$$T = T_{SENS_T0} + \frac{16 \times \left(TADC_T - \frac{TADC_{T0}}{16}\right)}{TADC_{RES}} \quad (4)$$

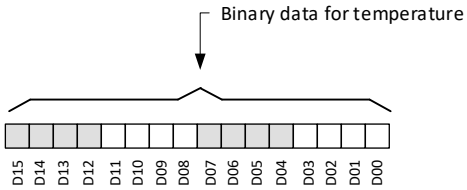

图 7-6. Temperature Sensor Data Definition

7.5.1.3 Magnetic Sensor Offset Correction

图 7-7 shows that the TMAG5170-Q1 can enable offset correction for a pair of magnetic axes. The magnetic axes and order are selected based off the ANGLE_EN register bit settings. The MAG_OFFSET_CONFIG register stores the offset values to be corrected in 2's complement data format. The selection and order of the sensors are defined in the ANGLE_EN register bits setting. The default value of these offset correction registers are set as zero.

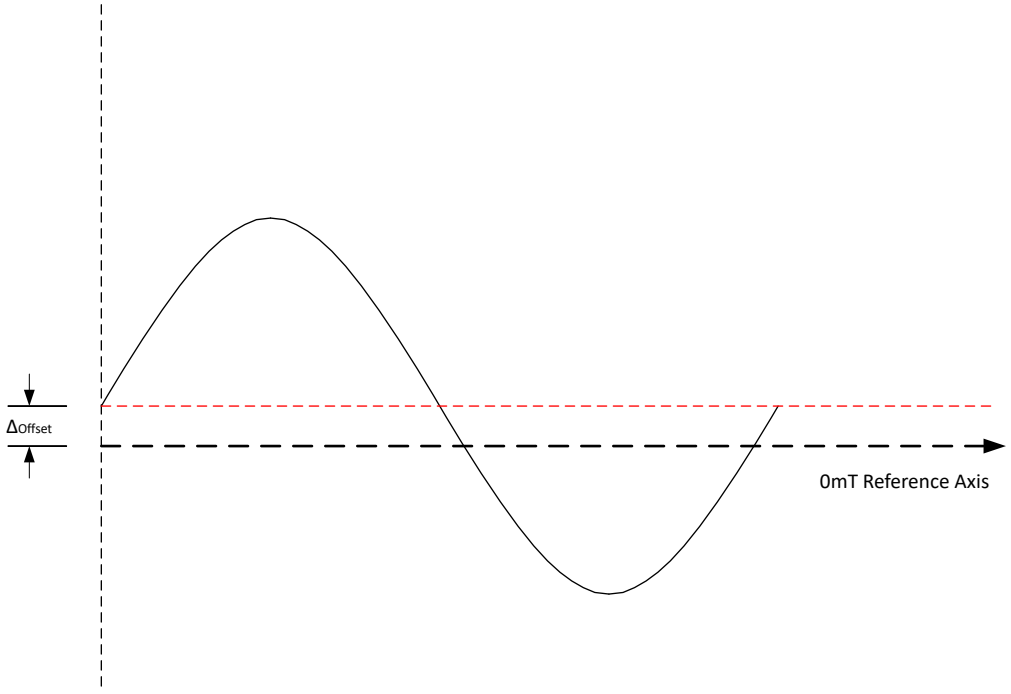

图 7-7. Magnetic Sensor Data Offset Correction

Use 方程式 5 and 方程式 6 to calculate the amount of offset for each axis. As an example, with a ±50mT magnetic range for X and Z axes, MAG_OFFSET_CONFIG set at 1110 0000 0011 0000b, ANGLE_EN set at 11b. With these conditions the offset correction for the X axis is −1.56mT and Z axis is 1.17mT. The offset values are added to the sensor conversion results before loading into the corresponding result registers.

$$\Delta_{Offset_Value1} = \frac{-\left(D_{13} \times 2^6\right) + \sum_{i=0}^{5} D_i + 7 \times 2^i}{2^{12}} \times 2|B_R| \quad (5)$$

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$$\Delta_{Offset_{Value2}} = \frac{-\left(D_6 \times 2^6\right) + \sum_{i=0}^{5} D_i \times 2^i}{2^{12}} \times 2|B_R| \quad (6)$$

where

- Δ_{Offset_Value1} is the amount of offset correction (in mT) to be applied for first axis.
- Δ_{Offset_Value2} is the amount of offset correction (in mT) to be applied for second axis.
- D_i is the data bit in the offset MAG_OFFSET_CONFIG register.
- B_R is the magnetic range in mT for the corresponding channel.

7.5.1.4 Angle and Magnitude Data Definition

The TMAG5170-Q1 calculates the angle based off the ANGLE_EN register bit settings. 图 7-8 shows that the ANGLE_RESULT register stores the angle information in the 13-LSB bits. Bits D04-D12 store angle integer value from 0 to 360 degree. Bits D00-D03 store fractional angle value with a resolution of 1/16 degree. The 3-MSB bits are always populated as b000. The TMAG5170-Q1 CORDIC offers angle resolution of 1/4 degree. An external CORDIC may be used if higher angle resolution is required. Use 方程式 7 to calculate the angle.

$$A = \sum_{i=4}^{12} D_i \times 2^{i-4} + \frac{\sum_{i=0}^{3} D_i \times 2^i}{16} \quad (7)$$

where

- A is the angle measured in degree.
- D_i is the data bit as shown in 图 7-8.

For example: a 354.50 degree is populated as 0001 0110 0010 1000b and a 17.25 degree is populated as 0000 0001 0001 0100b.

With DATA_TYPE ≠ 00b, the D01-D12 bits from the ANGLE_RESULT register can be accessed. In this mode, the angle fractional value is represented by 3 bit with resolution of 1/8 degree. Use 方程式 8 to calculate the angle in degree.

$$A = \sum_{i=4}^{12} D_i \times 2^{i-4} + \frac{\sum_{i=1}^{3} D_i \times 2^{i-1}}{8} \quad (8)$$

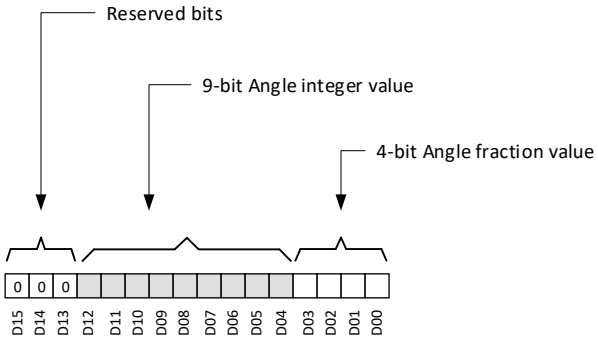

图 7-8. Angle Data Definition

During the angle calculation, use 方程式 9 to calculate the resultant vector magnitude.

$$M = \sqrt{MADC_{Ch1}{}^2 + MADC_{Ch2}{}^2} \quad (9)$$

where

- $MADC_{Ch1}$, $MADC_{Ch2}$ are the ADC codes of the two magnetic channels selected for the angle calculation.

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图 7-9 shows the magnitude value stored in the MAGNITUDE_RESULT register. This value should be constant during 360 degree angle measurements.

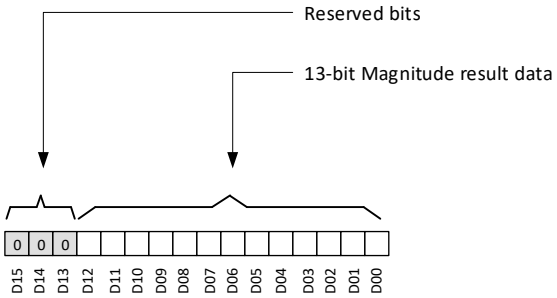

图 7-9. Magnitude Result Data Definition

The magnitude result can be accessed through SPI in 16-bit or 12-bit formats. In the 12-bit format, bit D01 to bit D12 are sent through the SPI.

7.5.2 SPI Interface

The Serial Peripheral Interface (SPI) is a synchronous serial communication interface used for short distance communication, usually between devices on a printed circuit board (PCB) assembly. The TMAG5170-Q1 supports a 4-wire SPI interface. The primary communication between the device and the external microcontroller is through the SPI bus that provides full-duplex communication. The external microcontroller works as the SPI controller that sends command requests on the SDI pin and receives device responses on the SDO pin. The TMAG5170-Q1 device works as the SPI peripheral device that receives command requests and sends responses (such as status and measured values) to the external microcontroller over the SDO line. The TMAG5170-Q1 supports a fixed 32-bit frame size to communicate with a controller device. However, the 32-bit frame can be configured through DATA_TYPE register bits to support a regular single register read data packet, or a special packet to read two-channel data simultaneously.

7.5.2.1 SCK

The Serial Clock (SCK) represents the controller clock signal. This clock determines the speed of data transfer and all receiving and sending are done synchronously to this clock. The output data on the SDO pin transitions on the falling edge of the SCK and input data on the SDI pin is latched on the rising edge of the SC.

7.5.2.2 $\overline{CS}$

The $\overline{CS}$ activates the SPI interface at the SPI. As long as the $\overline{CS}$ signal is at high level, the TMAG5170-Q1 will not accept the SCK signal or the Serial-data-in (SDI), and the Serial-data-out (SDO) is in high impedance. Hold $\overline{CS}$ low for the duration of a communication frame without toggling to ensure proper communication. The SPI is disabled each time $\overline{CS}$ is brought from low to high.

7.5.2.3 SDI

The Serial-data-in (SDI) line is used by the controller to configure the user access registers, start a new conversion, or send a read command. The SDI bits are transmitted with each SCK rising edge when the $\overline{CS}$ pin is low. 图 7-10 explains the SDI frame details. There are 4 command bits in the SDI line to select the status bit for the next frame or start a new conversion.

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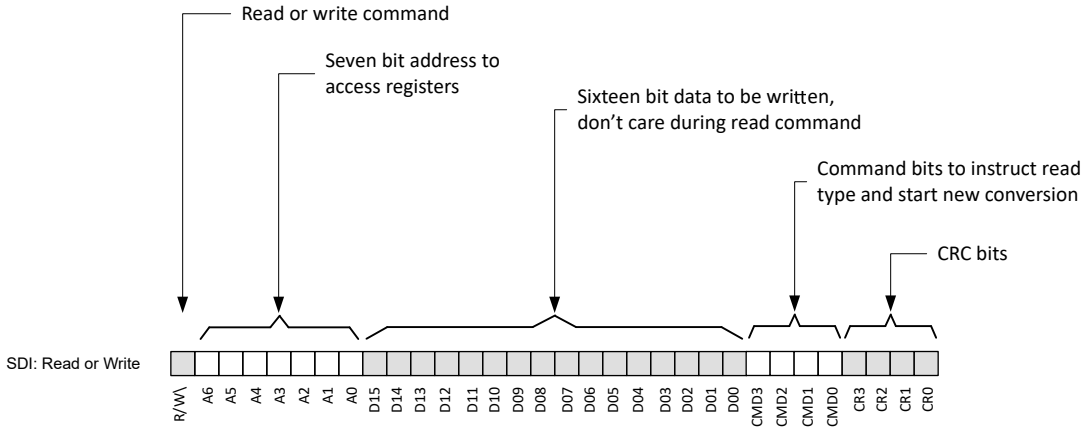


CMD0	CMD0 = 0	No conversion start through command bits
	CMD0 = 1	Start of conversion at the CS going high
CMD1	CMD1 = 0	Display SET_COUNT [2:0] in STAT [2:0] bits at SDO next frame
	CMD1 = 1	Display DATA_TYPE [2:0] in STAT [2:0] bits at SDO next frame

* CMD2 & CMD3 are reserved bits
** SET_COUNT register bits indicate the rolling count of the conversion data set. The counter is reset after 111b.
*** DATA_TYPE register bits indicate the type of data being read through the SDO line

图 7-10. 32-Bit Frame Definition of the SDI Line

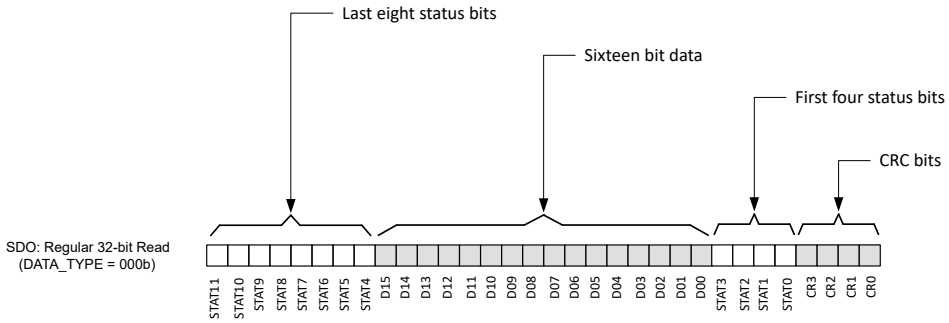
7.5.2.4 SDO

The Serial-data-out (SDO) line is used by the controller to read the data from the TMAG5170-Q1. The TMAG5170-Q1 will shift out command responses and ADC conversion data serially with each rising SCK edge when the $\overline{CS}$ pin is low. This pin assumes a high-impedance state when $\overline{CS}$ is high. Based off the DATA_TYPE bit setting, the TMAG5170-Q1 supports two different SDO frames:

- *Regular 32-Bit SDO Read*
- *Special 32-Bit SDO Read*

7.5.2.4.1 Regular 32-Bit SDO Read

With DATA_TYPE = 000b, the TMAG5170-Q1 supports a regular 16-bit register read during the 32-bit SDO frame as explained in 图 7-11. In this read mode, 12-bit status bits are displayed. All the status bits except for the ERROR_STAT bit are directly read from the status registers. The ERROR_STAT bit indicates if any error bit set in the device. 图 7-11 shows how the status bits STAT[2:0] can be changed based off CMD1 value in the previous frame.



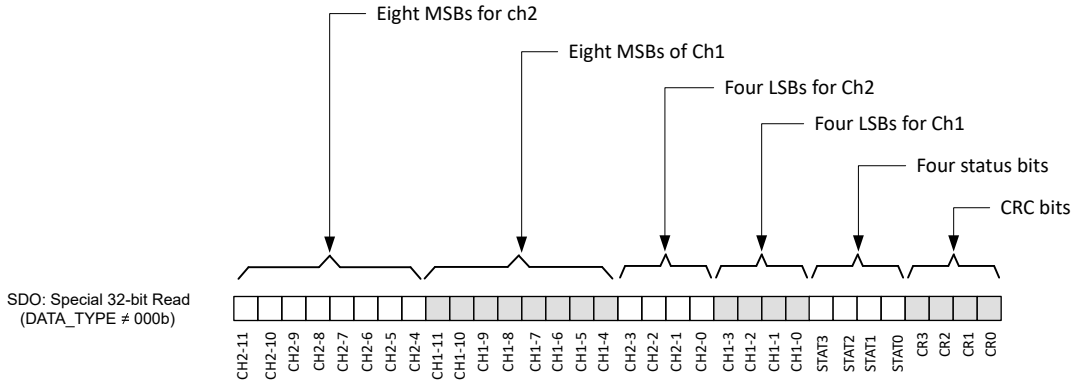
STAT11	STAT10	STAT9	STAT8	STAT7	STAT6	STAT5	STAT4	STAT3	STAT2	STAT1	STAT0
PREV_CRC_STAT	CFG_RESET	ALRT_STATUS1	ALRT_STATUS0	X	Y	Z	T	ERROR_STAT	Follows CMD1 instruction from previous frame		

* PREV_CRC_STAT indicates if there is any CRC error in the immediate past frame
** ERROR_STAT indicates if there is any error bit flipped in the part
*** STAT10 to STAT4 indicate select status bits from the CONV_STATUS and AFE_STATUS registers

图 7-11. Regular 32-Bit SDO Read

7.5.2.4.2 Special 32-Bit SDO Read

With DATA_TYPE > 000b, the TMAG5170-Q1 supports a special 32-bit SDO frame for two-channel simultaneous data read. Each channel data is limited to 12 bits. This feature is useful for systems requiring faster data throughput while performing multi-axis measurements. 图 7-12 explains the detail construction of the special 32-bit SDO frame. When the device is set to special 32-bit read, it will continue to deliver the 2-channel data set through the SDO line during consecutive read or write cycles. DATA_TYPE bits must be reset to get back to a regular read cycle. Only four status bits are transmitted in this mode. All the status bits except for the ERROR_STAT bit are directly read from the status registers. The ERROR_STAT bit indicates if any error bit set in the device. The status bits, STAT[2:0] can be changed based off CMD1 value in the previous frame.



STAT3	STAT2	STAT1	STAT0
ERROR_STAT	Follows CMD1 instruction from previous frame		

* ERROR_STAT indicates if there is any error bit set in the device

图 7-12. Special 32-Bit SDO Read

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7.5.2.5 SPI CRC

The TMAG5170-Q1 performs mandatory CRC for SPI communication. The Data integrity is maintained in both directions by a 4-bit CRC covering the content of the incoming and outgoing 32-bit messages. The four LSB bits of each 32-bit SPI frame are dedicated for the CRC. The CRC code is generated by the polynomial $x^4 + x + 1$. Initialize the CRC bits with b1111.

During the SDI write frame, the TMAG5170-Q1 reads for the CRC data before executing a write instruction. The write instruction from the controller is ignored if there is any CRC error present in the frame. During the SDI regular read frame, the TMAG5170-Q1 starts to deliver the requested data through SDO line in the same frame and notifies the controller of any error occurrence through the ERROR_STAT bit. If the device detects a CRC error in the SDI line, the device will invert the last bit of the SDO CRC in the same frame to promptly signal to a controller that the SPI communication is compromised. A controller can also determine the presence of a CRC error in the SDI frame by checking the Status11 bit in the next regular read frame.

备注

The TMAG5170-Q1 default mode at power up is CRC-enabled. With CRC enabled, the device will ignore all the SDI commands if proper CRC codes are not received. To disable the CRC at the SDI line, send the SPI SDI command x0F000407.

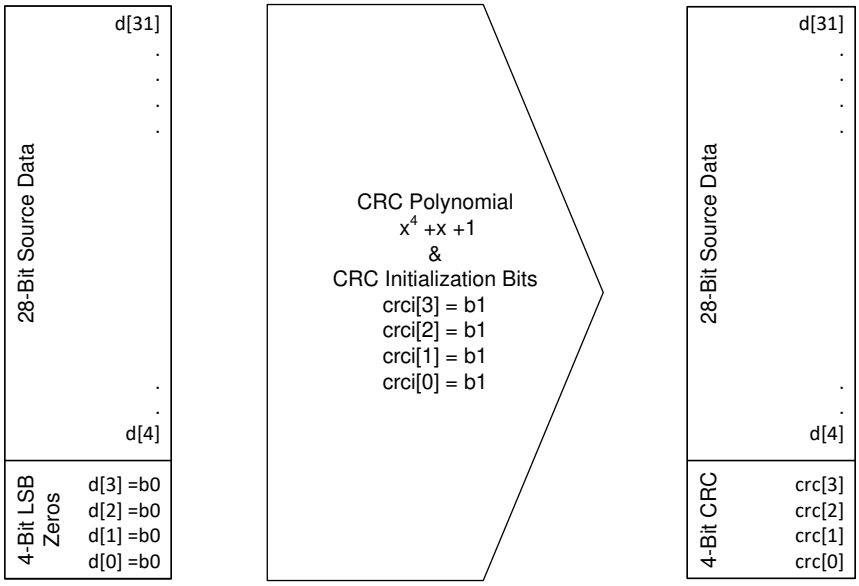

图 7-13. 4-Bit CRC Calculation

Use the following XOR function equations to calculate the 4-bit CRC. 图 7-13 describes the notations of these equations.

$$crc[0] = d[30] \wedge d[26] \wedge d[25] \wedge d[24] \wedge d[23] \wedge d[21] \wedge d[19] \wedge d[18] \wedge d[15] \wedge d[11] \wedge d[10] \wedge d[9] \wedge d[8] \wedge d[6] \wedge d[4] \wedge d[3] \wedge d[0] \wedge crci[2] \quad (10)$$

$$crc[1] = d[31] \wedge d[30] \wedge d[27] \wedge d[23] \wedge d[22] \wedge d[21] \wedge d[20] \wedge d[18] \wedge d[16] \wedge d[15] \wedge d[12] \wedge d[8] \wedge d[7] \wedge d[6] \wedge d[5] \wedge d[3] \wedge d[1] \wedge d[0] \wedge crci[2] \wedge crci[3] \quad (11)$$

$$crc[2] = d[31] \wedge d[28] \wedge d[24] \wedge d[23] \wedge d[22] \wedge d[21] \wedge d[19] \wedge d[17] \wedge d[16] \wedge d[13] \wedge d[9] \wedge d[8] \wedge d[7] \wedge d[6] \wedge d[4] \wedge d[2] \wedge d[1] \wedge crci[0] \wedge crci[3] \quad (12)$$

$$crc[3] = d[29] \wedge d[25] \wedge d[24] \wedge d[23] \wedge d[22] \wedge d[20] \wedge d[18] \wedge d[17] \wedge d[14] \wedge d[10] \wedge d[9] \wedge d[8] \wedge d[7] \wedge d[5] \wedge d[3] \wedge d[2] \wedge crci[1] \quad (13)$$

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The following shows example codes for calculating the 4-bit CRC.

```
function logic [3:0] calculate_crc4;
   input logic [27:0] frame;

   logic [31:0]       padded_frame;
   logic [3:0]           frame_crc;
   logic           inv;
   integer           i;

   padded_frame = {frame, 4'b0000};

   begin
      frame_crc = 4'hf; // initial value
      for (i=31; i >= 0; i=i-1) begin
     inv = padded_frame[i] ^ frame_crc[3];
     frame_crc[3] = frame_crc[2];
     frame_crc[2] = frame_crc[1];
     frame_crc[1] = frame_crc[0] ^ inv;
     frame_crc[0] = inv;
      end
      return frame_crc;
   end
endfunction
```

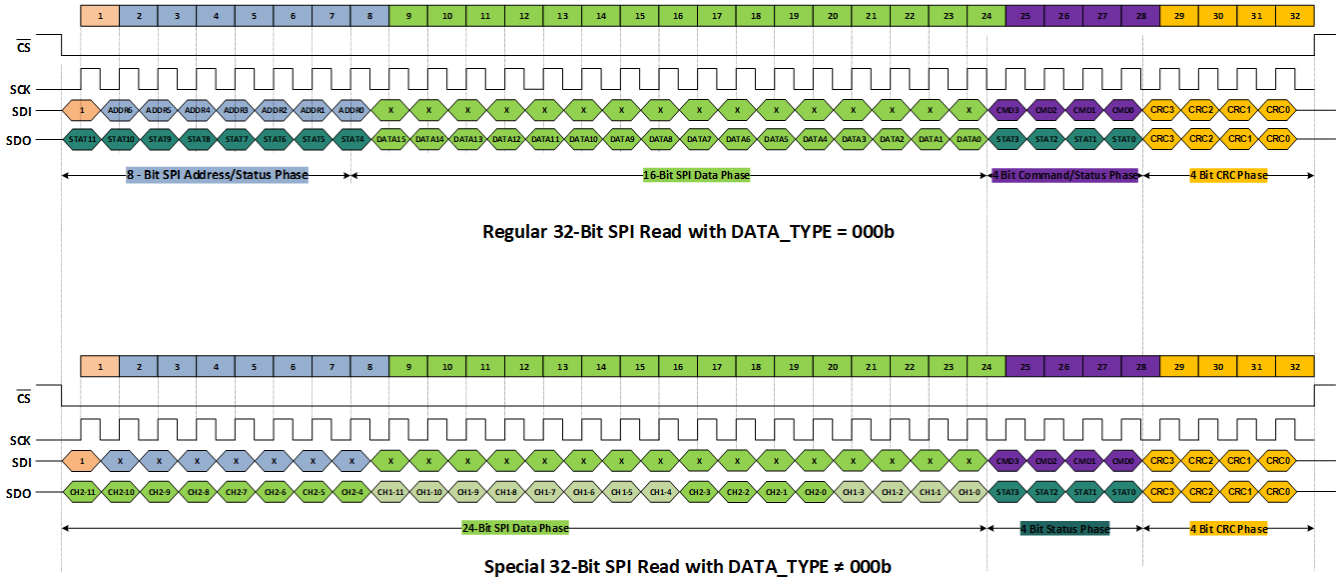
7.5.2.6 SPI Frame

With the flexible definition of the 32-bit frames, the TMAG5170-Q1 supports a wide array of application requirements catering to multiple user-specific data throughout. Two different frame examples are shown in this section to illustrate the complete SPI bus communication:

- *32-Bit Read Frame*
- *32-Bit Write Frame*

7.5.2.6.1 32-Bit Read Frame

图 7-14 shows both regular and special SDO frames during SDI read command. The TMAG5170-Q1 implements in-frame communication. When the controller sends a register read command during a regular read cycle, the corresponding 16-bit register data is sent through the SDO line in the same frame. During the special read cycle, the TMAG5170-Q1 ignores the address and data bits of the SDI line and sends the two channel data set through the SDO line as defined in the DATA_TYPE register bits.



* With DATA_TYPE = 000b, the SDO will deliver the requested 16-bit register data during the same frame
** With DATA_TYPE ≠ 000b, the SDO will continue to deliver two channel data and ignore the address and data bits of the SDI line
*** X = don't care

图 7-14. 32-Bit SPI Read

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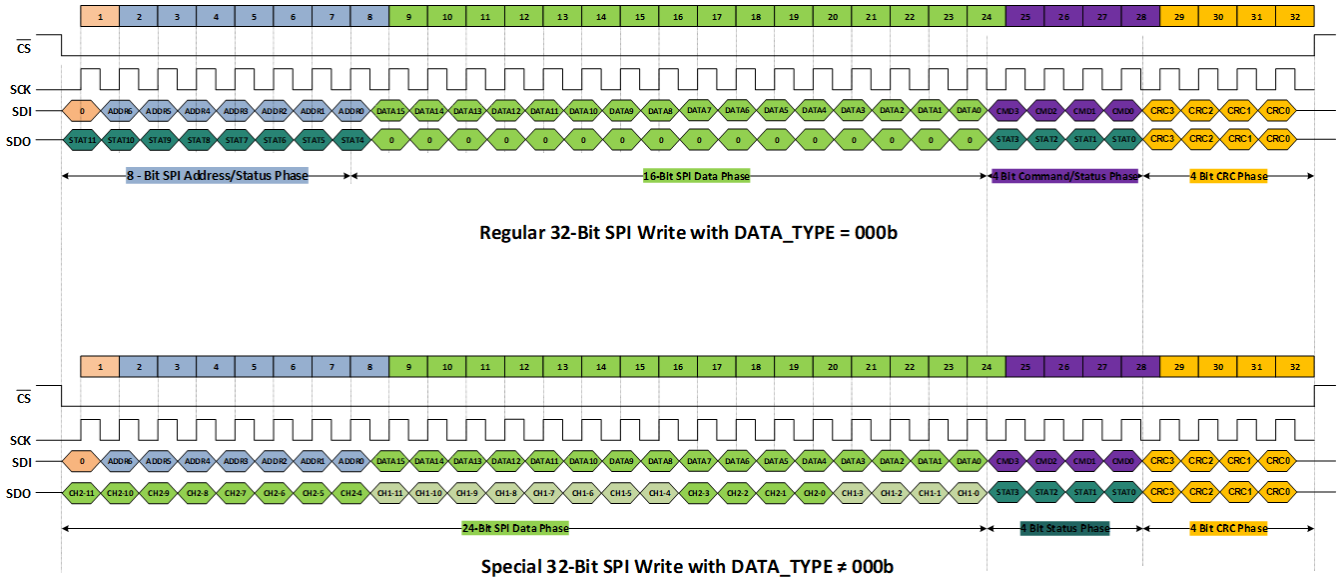
7.5.2.6.2 32-Bit Write Frame

图 7-15 shows both regular and special SDO frames during SDI write command. During a regular 32-bit frame write command through SDI, the SDO delivers '0's in place of 16-bit data placeholders. During the special frame write cycle through SDI line, the TMAG5170-Q1 will continue to send the two channel data through SDO line as defined by the DATA_TYPE register bits.



* With DATA_TYPE = 000b, the SDO will deliver '0's in the 16-bit data space during write frame
** With DATA_TYPE ≠ 000b, the SDO will continue to deliver two channel data during either read or write frames.

图 7-15. 32-BIT WRITE FRAME

7.6 Register Map

7.6.1 TMAG5170 Registers

表 7-4 lists the TMAG5170 registers. All register offset addresses not listed in 表 7-4 should be considered as reserved locations and the register contents should not be modified.

Reserved 2

表 7-4. TMAG5170 Registers

Offset	Acronym	Register Name	Section
0h	DEVICE_CONFIG	Configure Device Operation Modes	Go
1h	SENSOR_CONFIG	Configure Device Operation Modes	Go
2h	SYSTEM_CONFIG	Configure Device Operation Modes	Go
3h	ALERT_CONFIG	Configure Device Operation Modes	Go
4h	X_THRX_CONFIG	Configure Device Operation Modes	Go
5h	Y_THRX_CONFIG	Configure Device Operation Modes	Go
6h	Z_THRX_CONFIG	Configure Device Operation Modes	Go
7h	T_THRX_CONFIG	Configure Device Operation Modes	Go
8h	CONV_STATUS	Conversion Status Register	Go
9h	X_CH_RESULT	Conversion Result Register	Go
Ah	Y_CH_RESULT	Conversion Result Register	Go
Bh	Z_CH_RESULT	Conversion Result Register	Go
Ch	TEMP_RESULT	Conversion Result Register	Go
Dh	AFE_STATUS	Status Register	Go

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表 7-4. TMAG5170 Registers (continued)

Offset	Acronym	Register Name	Section
Eh	SYS_STATUS	Status Register	Go
Fh	TEST_CONFIG	Test Configuration Register	Go
10h	OSC_MONITOR	Conversion Result Register	Go
11h	MAG_GAIN_CONFIG	Configure Device Operation Modes	Go
12h	MAG_OFFSET_CONFIG	Configure Device Operation Modes	Go
13h	ANGLE_RESULT	Conversion Result Register	Go
14h	MAGNITUDE_RESULT	Conversion Result Register	Go

Complex bit access types are encoded to fit into small table cells. 表 7-5 shows the codes that are used for access types in this section.

表 7-5. TMAG5170 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
Reset or Default Value		
- *n*		Value after reset or the default value

7.6.1.1 DEVICE_CONFIG Register (Offset = 0h) [Reset = 0h]

DEVICE_CONFIG is shown in 表 7-6.

Return to the Summary Table.

表 7-6. DEVICE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-12	CONV_AVG	R/W	0h	Enables additional sampling of the sensor data to reduce the noise effect (or to increase resolution) 0h = 1x - 10.0Ksps (3-axes) or 20Ksps (1 axis) 1h = 2x - 5.7Ksps (3-axes) or 13.3Ksps (1 axis) 2h = 4x - 3.1Ksps (3-axes) or 8.0Ksps (1 axis) 3h = 8x - 1.6Ksps (3-axes) or 4.4Ksps (1 axis) 4h = 16x - 0.8Ksps (3-axes) or 2.4Ksps (1 axis) 5h = 32x - 0.4Ksps (3-axes) or 1.2Ksps (1 axis) 6h = Code not used, defaults to 000b if selected 7h = Code not used, defaults to000b if selected
11-10	RESERVED	R	0h	Reserved
9-8	MAG_TEMPCO	R/W	0h	Temperature coefficient of sense magnet 0h = 0%/ deg C (Current sensor applications) 1h = 0.12%/deg C (NdBFe) 2h = 0.03% /deg C (SmCo) 3h = 0.2%/deg C (Ceramic)
7	RESERVED	R	0h	Reserved

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表 7-6. DEVICE_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-4	OPERATING_MODE	R/W	0h	Selects operating mode 0h = Configuration mode, Default (TRIGGER_MODE active) 1h = Stand-by mode (TRIGGER_MODE active) 2h = Active measure mode (Continuous conversion) 3h = Active trigger mode (TRIGGER_MODE active) 4h = Wake-up and sleep mode (duty-cycled mode) 5h = Sleep mode 6h = Deep sleep mode (wakes up at CS signal from controller) 7h = Code not used, defaults to 000b if selected
3	T_CH_EN	R/W	0h	Enables data acquisition of the temperature channel 0h = Temp channel disabled, Default 1h = Temp channel enabled
2	T_RATE	R/W	0h	Temperature conversion rate. It is linked to the CONV_AVG field 0h = Same as other sensors per CONV_AVG, Default 1h = Once per conversion set
1	T_HLT_EN	R/W	0h	Enables temperature limit check 0h = Temperature limit check off, Default 1h = Temperature limit check on
0	RESERVED	R	0h	Reserved

7.6.1.2 SENSOR_CONFIG Register (Offset = 1h) [Reset = 0h]

SENSOR_CONFIG is shown in 表 7-7.

Return to the Summary Table.

表 7-7. SENSOR_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	ANGLE_EN	R/W	0h	Enable angle calculation using two axis data 0h = No angle calculation (default) 1h = X-Y-angle calculation enabled 2h = Y-Z-angle calculation enabled 3h = X-Z-angle calculation enabled
13-10	SLEEPTIME	R/W	0h	Selects the time spent in low power mode between conversions when OPERATING_MODE =010b 0h = 1ms 1h = 5ms 2h = 10ms 3h = 15ms 4h = 20ms 5h = 30ms 6h = 50ms 7h = 100ms 8h = 500ms 9h = 1000ms Ah = Code not used, defaults to 0000b if selected Bh = Code not used, defaults to 0000b if selected Ch = Code not used, defaults to 0000b if selected Dh = Code not used, defaults to 0000b if selected Eh = Code not used, defaults to 0000b if selected Fh = Code not used, defaults to 0000b if selected

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表 7-7. SENSOR_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-6	MAG_CH_EN	R/W	0h	Enables data acquisition of the magnetic axis channel(s) 0h = All magnetic channels of OFF, DEFAUT 1h = X channel enabled 2h = Y channel enabled 3h = X, Y channel enabled 4h = Z channel enabled 5h = Z, X channel enabled 6h = Y, Z channel enabled 7h = X, Y, Z channel enabled 8h = XYX channel enabled 9h = YXY channel enabled Ah = YZY channel enabled Bh = ZYZ channel enabled Ch = ZXZ channel enabled Dh = XZX channel enabled Eh = XYZYX channel enabled Fh = XYZZYX channel enabled
5-4	Z_RANGE	R/W	0h	Enables different magnetic ranges to support magnetic fields from ±25mT to ±300mT 0h = ±50mT (TMAG5170A1)/ ±150mT(TMAG5170A2), Default 1h = ±25mT (TMAG5170A1)/ ±75mT(TMAG5170A2) 2h = ±100mT (TMAG5170A1)/ ±300mT(TMAG5170A2) 3h = Code not used, defaults to 00b if selected
3-2	Y_RANGE	R/W	0h	Enables different magnetic ranges to support magnetic fields from ±25mT to ±300mT 0h = ±50mT (TMAG5170A1)/ ±150mT(TMAG5170A2), Default 1h = ±25mT (TMAG5170A1)/ ±75mT(TMAG5170A2) 2h = ±100mT (TMAG5170A1)/ ±300mT(TMAG5170A2) 3h = Code not used, defaults to 00b if selected
1-0	X_RANGE	R/W	0h	Enables different magnetic ranges to support magnetic fields from ±25mT to ±300mT 0h = ±50mT (TMAG5170A1)/ ±150mT(TMAG5170A2), Default 1h = ±25mT (TMAG5170A1)/ ±75mT(TMAG5170A2) 2h = ±100mT (TMAG5170A1)/ ±300mT(TMAG5170A2) 3h = Code not used, defaults to 00b if selected

7.6.1.3 SYSTEM_CONFIG Register (Offset = 2h) [Reset = 0h]

SYSTEM_CONFIG is shown in 表 7-8.

Return to the Summary Table.

表 7-8. SYSTEM_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13-12	DIAG_SEL	R/W	0h	Selects a diagnostic mode run 0h = Run all data path diagnostics all together, Default 1h = Run only enabled data path diagnostics all together 2h = Run all data path diagnostics in sequence 3h = Run only enabled data path diagnostics in sequence
11	RESERVED	R	0h	Reserved
10-9	TRIGGER_MODE	R/W	0h	Selects a condition which initiates a single conversion based off already configured registers. A running conversion completes before executing a trigger. Redundant triggers are ignored. TRIGGER_MODE is available only during the modes explicitly mentioned in OPERATING_MODE. 0h = Conversion start at SPI command, Default 1h = Conversion start at $\overline{CS}$ pulse 2h = Conversion start at $\overline{ALERT}$ pulse 3h = Code not used, defaults to 00b if selected

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表 7-8. SYSTEM_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8-6	DATA_TYPE	R/W	0h	Data Type to be accessed from results registers via SPI 0h = Default 32-bit register access 1h = 12-Bit XY data access 2h = 12-Bit XZ data access 3h = 12-Bit ZY data access 4h = 12-Bit XT data access 5h = 12-Bit YT data access 6h = 12-Bit ZT data access 7h = 12-Bit AM data access
5	DIAG_EN	R/W	0h	Enables user controlled AFE diagnostic tests 0h = Execution of AFE diagnostics is disabled, Default 1h = Execution of AFE diagnostics is enabled
4-3	RESERVED	R	0h	Reserved
2	Z_HLT_EN	R/W	0h	Enables magnetic field limit check on Z axis 0h = Z axis limit check off, Default 1h = Z axis limit check on
1	Y_HLT_EN	R/W	0h	Enables magnetic field limit check on Y axis 0h = Y axis limit check off, Default 1h = Y axis limit check on
0	X_HLT_EN	R/W	0h	Enables magnetic field limit check on X axis 0h = X axis limit check off, Default 1h = X axis limit check on

7.6.1.4 ALERT_CONFIG Register (Offset = 3h) [Reset = 0h]

ALERT_CONFIG is shown in 表 7-9.

Return to the Summary Table.

表 7-9. ALERT_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13	ALERT_LATCH	R/W	0h	Latched $\overline{\text{ALERT}}$ mode select 0h = $\overline{\text{ALERT}}$ sources are not latched. $\overline{\text{ALERT}}$ is asserted only while the source of the $\overline{\text{ALERT}}$ response is present 1h = $\overline{\text{ALERT}}$ sources are latched. $\overline{\text{ALERT}}$ response is latched when the source of the $\overline{\text{ALERT}}$ is asserted until cleared on Read of the corresponding status register (AFE_STATUS, SYS_STATUS, or result registers)
12	ALERT_MODE	R/W	0h	ALERT mode select 0h = Interrupt mode 1h = Switch mode. This mode overrides any interrupt function (ALERT trigger is also disabled), and implements Hall switch function based off the *_THRX_ALRT settings. In the switch mode the corresponding X_HLT_EN, Y_HLT_EN, Z_HLT_EN need to be set.
11	STATUS_ALRT	R/W	0h	Enable $\overline{\text{ALERT}}$ response when any flag in the AFE_STATUS or SYS_STATUS registers are set 0h = $\overline{\text{ALERT}}$ is not asserted when any of the AFE_STATUS or SYS_STATUS bit is set 1h = $\overline{\text{ALERT}}$ output is asserted when any of the AFE_STATUS or SYS_STATUS bit is set
10-9	RESERVED	R	0h	Reserved
8	RSLT_ALRT	R/W	0h	Enable $\overline{\text{ALERT}}$ response when the configured set of conversions is complete 0h = $\overline{\text{ALERT}}$ is not used to signal when the configured set of conversions are complete 1h = $\overline{\text{ALERT}}$ output is asserted when the configured set of conversions are complete

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表 7-9. ALERT_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-4	THRX_COUNT	R/W	0h	Number of conversions above the HIGH threshold or below the LOW threshold before the ALERT response is initiated 0h = 1-Conversion result 1h = 2-Conversion results 2h = 3-Conversion results 3h = 4-Conversion results
3	T_THRX_ALRT	R/W	0h	Temperature threshold ALERT enable 0h = ALERT is not used to signal when temperature thresholds are crossed 1h = ALERT output is asserted when temperature thresholds are crossed
2	Z_THRX_ALRT	R/W	0h	Z-Channel threshold ALERT enable 0h = ALERT is not used to signal when Z-Axis magnetic thresholds are crossed 1h = ALERT output is asserted when Z-Axis magnetic thresholds are crossed
1	Y_THRX_ALRT	R/W	0h	Y-Channel threshold ALERT enable 0h = ALERT is not used to signal when Y-Axis magnetic thresholds are crossed 1h = ALERT output is asserted when Y-Axis magnetic thresholds are crossed
0	X_THRX_ALRT	R/W	0h	X-Channel threshold ALERT enable 0h = ALERT is not used to signal when X-Axis magnetic thresholds are crossed 1h = ALERT output is asserted when X-Axis magnetic thresholds are crossed

7.6.1.5 X_THRX_CONFIG Register (Offset = 4h) [Reset = 7D83h]

X_THRX_CONFIG is shown in 表 7-10.

Return to the Summary Table.

表 7-10. X_THRX_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	X_HI_THRESHOLD	R/W	7Dh	X-Axis maximum magnetic field threshold. User input as 2's complement 8-bit binary number. The threshold in mT can be calculated as: (X_RANGE/128)*X_HI_THRESHOLD. Default to 98% of the full-scale
7-0	X_LO_THRESHOLD	R/W	83h	X-Axis minimum magnetic field threshold. User input as 2's complement 8-bit binary number. The threshold in mT can be calculated as: (X_RANGE/128)*X_LO_THRESHOLD. Default to -98% of the full-scale

7.6.1.6 Y_THRX_CONFIG Register (Offset = 5h) [Reset = 7D83h]

Y_THRX_CONFIG is shown in 表 7-11.

Return to the Summary Table.

表 7-11. Y_THRX_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	Y_HI_THRESHOLD	R/W	7Dh	Y-Axis maximum magnetic field threshold. User input as 2's complement 8-bit binary number. The threshold in mT can be calculated as: (Y_RANGE/128)*Y_HI_THRESHOLD. Default to 98% of the full-scale.

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表 7-11. Y_THRX_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	Y_LO_THRESHOLD	R/W	83h	Y-Axis minimum magnetic field threshold. User input as 2's complement 8-bit binary number. The threshold in mT can be calculated as: (Y_RANGE/128)*Y_LO_THRESHOLD. Default to -98% of the full-scale.

7.6.1.7 Z_THRX_CONFIG Register (Offset = 6h) [Reset = 7D83h]

Z_THRX_CONFIG is shown in 表 7-12.

Return to the Summary Table.

表 7-12. Z_THRX_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	Z_HI_THRESHOLD	R/W	7Dh	Z-Axis maximum magnetic field threshold. User input as 2's complement 8-bit binary number. The threshold in mT can be calculated as:(Z_RANGE/128)*Z_HI_THRESHOLD. Default to 98% of the full-scale
7-0	Z_LO_THRESHOLD	R/W	83h	Z-Axis minimum magnetic field threshold. User input as 2's complement 8-bit binary number. The threshold in mT can be calculated as: (Z_RANGE/128)*X_LO_THRESHOLD. Default to -98% of the full-scale

7.6.1.8 T_THRX_CONFIG Register (Offset = 7h) [Reset = 6732h]

T_THRX_CONFIG is shown in 表 7-13.

Return to the Summary Table.

表 7-13. T_THRX_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	T_HI_THRESHOLD	R/W	67h	Temperature maximum threshold. User input as 2's complement 8-bit binary number. Each LSB in this field corresponds to 4.267°C. Default value of 67h represents 172°C.
7-0	T_LO_THRESHOLD	R/W	32h	Temperature minimum threshold. User input as 2's complement 8-bit binary number. Each LSB in this field corresponds to 4.267°C. Default value of 32h represents -53°C.

7.6.1.9 CONV_STATUS Register (Offset = 8h) [Reset = 0h]

CONV_STATUS is shown in 表 7-14.

Return to the Summary Table.

表 7-14. CONV_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13	RDY	R	0h	Conversion data buffer is ready. 0h = Conversion data not valid (result registers hold previous conversion value) 1h = Conversion data valid
12	A	R	0h	Angle/Magnitude data from current conversion 0h = Data is not current 1h = Data is current
11	T	R	0h	Temperature data from current conversion 0h = Temperature data is not current 1h = Temperature data is current

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表 7-14. CONV_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	Z	R	0h	Z-Channel data from current conversion 0h = Z-Channel data is not current 1h = Z-Channel data is current
9	Y	R	0h	Y-Channel data from current conversion 0h = Y-Channel data is not current 1h = Y-Channel data is current
8	X	R	0h	X-Channel data from current conversion 0h = X-Channel data is not current 1h = X-Channel data is current
7	RESERVED	R	0h	Reserved
6-4	SET_COUNT	R	0h	Rolling count of conversion data sets
3-2	RESERVED	R	0h	Reserved
1-0	ALRT_STATUS	R	0h	State of $\overline{\text{ALERT}}$ response 0h = No $\overline{\text{ALERT}}$ conditions 1h = AFE status flag set 2h = SYS status flag set 3h = Flags set in both AFE and SYS status registers

7.6.1.10 X_CH_RESULT Register (Offset = 9h) [Reset = 0h]

X_CH_RESULT is shown in 表 7-15.

Return to the Summary Table.

表 7-15. X_CH_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	X_CH_RESULT	R	0h	X-Channel data conversion results

7.6.1.11 Y_CH_RESULT Register (Offset = Ah) [Reset = 0h]

Y_CH_RESULT is shown in 表 7-16.

Return to the Summary Table.

表 7-16. Y_CH_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Y_CH_RESULT	R	0h	Y-Channel data conversion results

7.6.1.12 Z_CH_RESULT Register (Offset = Bh) [Reset = 0h]

Z_CH_RESULT is shown in 表 7-17.

Return to the Summary Table.

表 7-17. Z_CH_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Z_CH_RESULT	R	0h	Z-Channel data conversion results

7.6.1.13 TEMP_RESULT Register (Offset = Ch) [Reset = 0h]

TEMP_RESULT is shown in 表 7-18.

Return to the Summary Table.

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表 7-18. TEMP_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TEMP_RESULT	R	0h	Temperature sensor data conversion results

7.6.1.14 AFE_STATUS Register (Offset = Dh) [Reset = 8000h]

AFE_STATUS is shown in 表 7-19.

Return to the Summary Table.

表 7-19. AFE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CFG_RESET	RC	1h	Device power up status. This bit is reset when microcontroller reads the AFE_STATUS register. 0h = Device reset has been acknowledged and cleared 1h = Device has experienced a hardware reset after a power down or brown-out
14-13	RESERVED	R	0h	Reserved
12	SENS_STAT	RC	0h	Analog front end sensor diagnostic status 0h = No error detected 1h = Analog front end sensor diagnostic test failed
11	TEMP_STAT	RC	0h	Temperature sensor diagnostic status 0h = No error detected 1h = Analog front end temperature sensor diagnostic test failed
10	ZHS_STAT	RC	0h	Z-Axis hall sensor diagnostic status 0h = No error detected 1h = Z-Axis hall sensor diagnostic test failed
9	YHS_STAT	RC	0h	Y-Axis hall sensor diagnostic status 0h = No error detected 1h = Y-Axis hall sensor diagnostic test failed
8	XHS_STAT	RC	0h	X-Axis hall sensor diagnostic status 0h = No error detected 1h = X-Axis hall sensor diagnostic test failed
7-2	RESERVED	R	0h	Reserved
1	TRIM_STAT	RC	0h	Trim data error 0h = No trim data errors were detected 1h = Trim data error was detected
0	LDO_STAT	RC	0h	LDO error 0h = No faults in the internal LDO supplied power were detected 1h = A fault in the internal LDO supplied power was detected

7.6.1.15 SYS_STATUS Register (Offset = Eh) [Reset = 0h]

SYS_STATUS is shown in 表 7-20.

Return to the Summary Table.

表 7-20. SYS_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ALRT_LVL	R	0h	Reflects the current state of the $\overline{\text{ALERT}}$ pin feed-back path 0h = The input $\overline{\text{ALERT}}$ logic level is low 1h = The input $\overline{\text{ALERT}}$ logic level is high
14	ALRT_DRV	RC	0h	Each time the open drain $\overline{\text{ALERT}}$ signal is driven, the feedback circuit checks if the $\overline{\text{ALERT}}$ output goes Low. An error flag is generated at the ALRT_DRV bit if the output doesn't go Low. 0h = No $\overline{\text{ALERT}}$ drive error detected 1h = $\overline{\text{ALERT}}$ drive error detected

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表 7-20. SYS_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	SDO_DRV	RC	0h	The Logic value driven output on SDO was not the value of the SDO Pin Feed-back path when SDO is being driven by the device 0h = No SDO drive error detected 1h = SDO drive error detected
12	CRC_STAT	RC	0h	Cyclic redundancy check error 0h = No cyclic redundancy check error was detected 1h = Cyclic redundancy check error was detected for a SPI transaction
11	FRAME_STAT	RC	0h	Incorrect number of clocks in SPI frame 0h = No frame error was detected 1h = Incorrect number of clocks detected for a SPI transaction
10-8	OPERATING_STAT	R	0h	Reports the status of operating mode 0h = Config state 1h = Standby state 2h = Active measure (Continuous Mode) state 3h = Active triggered mode state 4h = DCM active state 5h = DCM Sleep state 6h = Sleep state
7-6	RESERVED	R	0h	Reserved
5	VCC_OV	RC	0h	VCC over-voltage detection in active or stand-by mode 0h = No over-voltage detected on VCC 1h = VCC was detected to be over-voltage
4	VCC_UV	RC	0h	VCC under voltage detection in active or stand-by mode 0h = No under-voltage was detected on VCC 1h = VCC was detected to be under-voltage
3	TEMP_THX	RC	0h	Temperature threshold crossing detected 0h = No temperature threshold crossing detected 1h = Temperature threshold crossing detected
2	ZCH_THX	RC	0h	Z-Channel threshold crossing detected 0h = No Z-Axis magnetic field threshold crossing detected 1h = Z-Axis magnetic field threshold crossing detected
1	YCH_THX	RC	0h	Y-Channel threshold crossing detected 0h = No Y-Axis magnetic field threshold crossing detected 1h = Y-Axis magnetic field threshold crossing detected
0	XCH_THX	RC	0h	X-Channel threshold crossing detected 0h = No X-Axis magnetic field threshold crossing detected 1h = X-Axis magnetic field threshold crossing detected

7.6.1.16 TEST_CONFIG Register (Offset = Fh) [Reset = X]

TEST_CONFIG is shown in 表 7-21.

Return to the Summary Table.

表 7-21. TEST_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	1h	Reserved
5-4	VER	R	X	Indicates the version of the device 0h = A1 rev 1h = A2 rev 2h = reserved 3h = reserved
3	RESERVED	R	0h	Reserved
2	CRC_DIS	R/W	0h	Enable or disable CRC in SPI communication 0h = CRC enabled in SPI communication (Default) 1h = CRC disabled in SPI communication

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表 7-21. TEST_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	OSC_CNT_CTL	R/W	0h	Oscillator count control - starts, stops, and resets the counter driven by the HFOSC or LFOSC oscillator to facilitate oscillator frequency and integrity checks 0h = Reset OSC counter (default) 1h = Start OSC counter driven by HFOSC 2h = Start OSC counter driven by LFOSC 3h = Stop OSC counter

7.6.1.17 OSC_MONITOR Register (Offset = 10h) [Reset = 0h]

OSC_MONITOR is shown in 表 7-22.

Return to the Summary Table.

表 7-22. OSC_MONITOR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	OSC_COUNT	R	0h	Oscillator Counter. The number of selected oscillator clock cycles that have been counted since Oscillator Counter was started. The HFOSC and LFOSC clock roll-over the 16-bit counter once reaching the max value.

7.6.1.18 MAG_GAIN_CONFIG Register (Offset = 11h) [Reset = 0h]

MAG_GAIN_CONFIG is shown in 表 7-23.

Return to the Summary Table.

表 7-23. MAG_GAIN_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	GAIN_SELECTION	R/W	0h	Enables the selection of a particular Hall axis for amplitude correction to get accurate angle measurement 0h = No axis is selected (Default) 1h = X-axis is selected 2h = Y-axis is selected 3h = Z-axis is selected
13-11	RESERVED	R	0h	Reserved
10-0	GAIN_VALUE	R/W	0h	11-bit gain value determined by controller to adjust the a particular Hall axis value. The gain value is anywhere between 0 and 2. Gain is calculated as 'user entered value/1024'.

7.6.1.19 MAG_OFFSET_CONFIG Register (Offset = 12h) [Reset = 0h]

MAG_OFFSET_CONFIG is shown in 表 7-24.

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表 7-24. MAG_OFFSET_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	OFFSET_SELECTION	R/W	0h	Enables the selection of a particular Hall axis for offset correction to get accurate angle measurement: 00b = No axis is selected for offset correction (Default). 01b = Only OFFSET_VALUE1 is used for offset correction. Applied to X axis when ANGLE_EN = 01b or 11b, and to Y axis when ANGLE_EN =10b. No axis is selected if ANGLE_EN =00b. 10b = Only OFFSET_VALUE2 is used for offset correction. Applied to Y axis when ANGLE_EN = 01b, and to Z axis when ANGLE_EN =10b or 11b. No axis is selected if ANGLE_EN =00b. 11b = Both OFFSET_VALUE1 and OFFSET_VALUE2 are used for offset correction. OFFSET_VALUE1 applied to X axis when ANGLE_EN = 01b or 11b, and to Y axis when ANGLE_EN =10b. OFFSET_VALUE2 applied to Y axis when ANGLE_EN = 01b, and to Z axis when ANGLE_EN =10b or 11b. No axis is selected if ANGLE_EN =00b.
13-7	OFFSET_VALUE1	R/W	0h	7-bit, 2' complement offset value determined by controller to adjust a particular Hall axis value. The range of possible offset valid entries can be +/-64. The offset value is calculated from the user input as the 7 LSB bits of a 11-bit range per SENSOR_CONFIG register setting for the corresponding axis. Default offset value is 0.
6-0	OFFSET_VALUE2	R/W	0h	7-bit, 2' complement offset value determined by controller to adjust a particular Hall axis value. The range of possible offset valid entries can be +/-64. The offset value is calculated from the user input as the 7 LSB bits of a 11-bit range per SENSOR_CONFIG register setting for the corresponding axis. Default offset value is 0.

7.6.1.20 ANGLE_RESULT Register (Offset = 13h) [Reset = 0h]

ANGLE_RESULT is shown in 表 7-25.

Return to the Summary Table.

表 7-25. ANGLE_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ANGLE_RESULT	R	0h	Angle measurement result in degree. The data is displayed from 0 to 360 degree in 13 LSB bits. The 4 LSB bits allocated for fraction of an angle in the format (xxxx/16).

7.6.1.21 MAGNITUDE_RESULT Register (Offset = 14h) [Reset = 0h]

MAGNITUDE_RESULT is shown in 表 7-26.

Return to the Summary Table.

表 7-26. MAGNITUDE_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MAGNITUDE_RESULT	R	0h	Resultant vector magnitude (during angle measurement) result. This value should be constant during 360 degree measurements

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8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

8.1.1 Selecting the Sensitivity Option

Select the highest TMAG5170-Q1 sensitivity option that can measure the required range of magnetic flux density so that the ADC output range is maximized.

Larger-sized magnets and farther sensing distances can generally enable better positional accuracy than very small magnets at close distances, because magnetic flux density increases exponentially with the proximity to a magnet. TI created an online tool to help with simple magnet calculations under the TMAG5170-Q1 product folder on ti.com.

8.1.2 Temperature Compensation for Magnets

The TMAG5170-Q1 temperature compensation is designed to directly compensate the average temperature drift of several magnets as specified in the MAG_TEMPCO register bits. The residual induction (B_r) of a magnet typically reduces by 0.12%/°C for NdFeB, and 0.20%/°C for ferrite magnets as the temperature increases. Set the MAG_TEMPCO bit to default 00b if the device temperature compensation is not needed.

8.1.3 Sensor Conversion

Multiple conversion schemes can be adopted based off the MAG_CH_EN, CONV_AVG, DIAG_SEL, and DIAG_EN register bit settings.

8.1.3.1 Continuous Conversion

The TMAG5170-Q1 can be set in continuous conversion mode when OPERATING_MODE is set to 010b. 图 8-1 shows few examples of continuous conversion. The input magnetic field is processed in two steps. In the first step the device spins the hall sensor elements, and integrates the sampled data. In the second step the ADC block converts the analog signal into digital bits and stores in the corresponding result register. While the ADC starts processing the first magnetic sample, the spin block can start processing another magnetic sample. The temperature data is taken at the beginning of each new conversion. This temperature data is used to compensate for the magnetic thermal drift.

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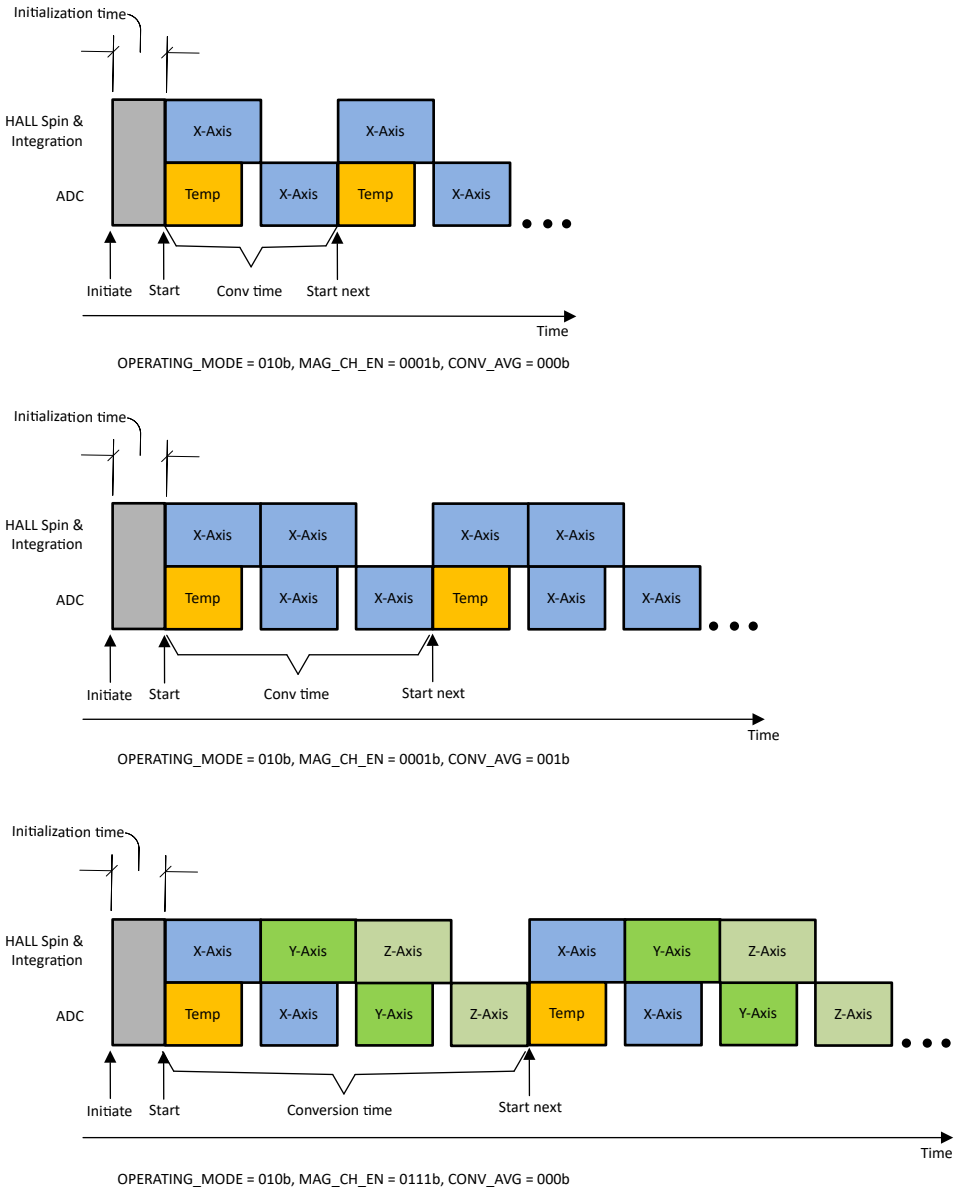

图 8-1. Continuous Conversion Examples

8.1.3.2 Trigger Conversion

The TMAG5170-Q1 supports trigger conversion with OPERATING_MODE set to 000b, 001b, or 011b. During trigger conversion, the initialization time can vary depending on the operating mode as shown in 表 7-3. The trigger event can be initiated through SPI command, $\overline{\text{ALERT}}$, or $\overline{\text{CS}}$ signal. 图 8-2 shows an example of trigger conversion with X, Y, Z, and temperature sensors activated.

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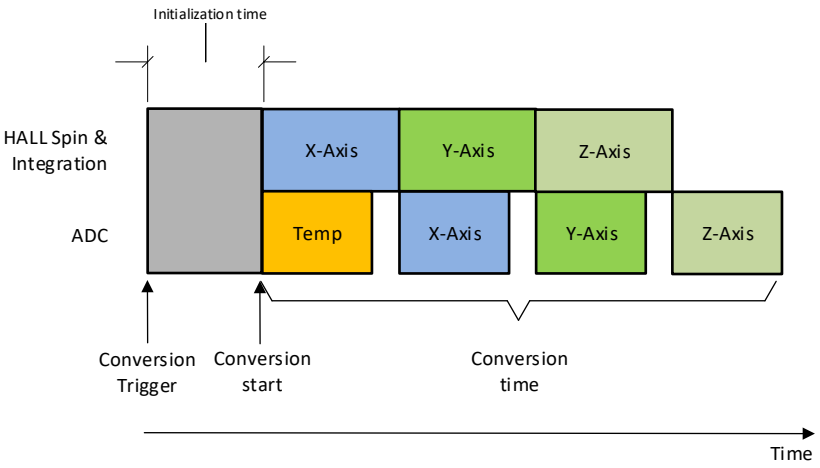

图 8-2. Trigger Conversion for X, Y, Z, and Temperature Sensors

8.1.3.3 Pseudo-Simultaneous Sampling

In absolute angle measurement, application sensor data from multiple axes are required to calculate an accurate angle. The magnetic field data collected at different times through the same signal chain introduces error in angle calculation. The TMAG5170-Q1 offers pseudo-simultaneous sampling data collection modes to eliminate this error. 图 8-3 shows an example where MAG_CH_EN is set at 1101b to collect XZX data. 方程式 14 shows that the time stamps for the X and Z sensor data are the same.

$$t_Z = \frac{t_{X1} + t_{X2}}{2} \tag{14}$$

where

- t_{X1}, t_Z, t_{X2} are time stamps for X, Z, X sensor data completion as defined in 图 8-3.

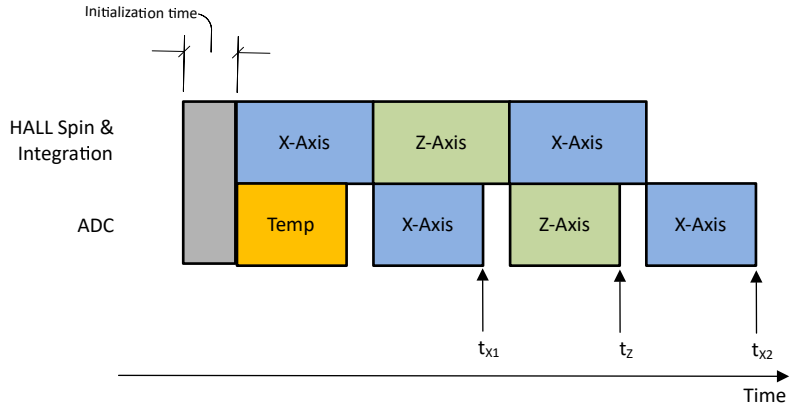

图 8-3. XZX Magnetic Field Conversion

The vertical X, Y sensors of the TMAG5170-Q1 exhibit more noise than the horizontal Z sensor. The pseudo-simultaneous sampling can be used to equalize the noise floor when two set of vertical sensor data are collected against one set of horizontal sensor data, as in examples of XZX or YZY modes.

8.1.4 Error Calculation During Linear Measurement

The TMAG5170-Q1 offers independent configurations to perform linear position measurements in X, Y, and Z axes. To calculate the expected error during linear measurement, the contributions from each of the individual error sources must be understood. The relevant error sources include sensitivity error, offset, noise, cross axis sensitivity, hysteresis, nonlinearity, drift across temperature, drift across life time, and so forth. For a 3-axis Hall

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solution like the TMAG5170-Q1, the cross-axis sensitivity and hysteresis error sources are insignificant. Use 方程式 15 to estimate the linear measurement error calculation at room temperature.

$$Error_{LM_25C} = \frac{\sqrt{(B \times SENS_{ER})^2 + B_{off}^2 + N_{RMS_25}^2}}{B} \times 100\% \quad (15)$$

where

- $Error_{LM_25C}$ is total error in % during linear measurement at 25°C.
- B is input magnetic field.
- $SENS_{ER}$ is sensitivity error at 25°C.
- B_{off} is offset error at 25°C.
- N_{RMS_25} is RMS noise at 25°C.

In many applications, system level calibration at room temperature can nullify the offset and sensitivity errors at 25°C. The noise errors can be reduced by further digital averaging the sensor data in a microcontroller. Use 方程式 15 to estimate the linear measurement error across temperature after calibration at room temperature.

$$Error_{LM_Temp} = \frac{\sqrt{(B \times SENS_{DR})^2 + B_{off_DR}^2 + N_{RMS_Temp}^2}}{B} \times 100\% \quad (16)$$

where

- $Error_{LM_Temp}$ is total error in % during linear measurement across temperature after room temperature calibration.
- B is input magnetic field.
- $SENS_{DR}$ is sensitivity drift from value at 25°C.
- B_{off_DR} is offset drift from value at 25°C.
- N_{RMS_Temp} is RMS noise across temperature.

If room temperature calibration is not performed, sensitivity and offset errors at room temperature must also account for total error calculation across temperature (see 方程式 17).

$$Error_{LM_Temp_NCal} = \frac{\sqrt{(B \times SENS_{ER})^2 + (B \times SENS_{DR})^2 + B_{off}^2 + B_{off_DR}^2 + N_{RMS_Temp}^2}}{B} \times 100\% \quad (17)$$

where

- $Error_{LM_Temp_NCal}$ is total error in % during linear measurement across temperature without room temperature calibration.

The table below summarizes linear measurement error estimate for z-axis with magnetic field range of ±50mT and CONV_AVG =101b:

表 8-1. Total Error Examples During Linear Measurement

	Input Field 50mT	Input Field 25mT
Error % for z sensor at 25°C without any calibration	2.6%	2.8%
Error % for z sensor across temperature after 25°C calibration	3.0%	3.6%
Error % for z sensor across temperature without 25°C calibration	4.0%	4.5%

备注

In this section, error sources such as system mechanical vibration, magnet temperature gradient, nonlinearity, lifetime drift, and so forth, are not considered. The user must take these additional error sources into account while calculating overall system error budgets.

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8.1.5 Error Calculation During Angular Measurement

The TMAG5170-Q1 offers on-chip CORDIC to measure angle data from any of the two magnetic axes. The linear magnetic axis data can be used to calculate the angle using an external CORDIC as well. To calculate the expected error during angular measurement, the contributions from each individual error source must be understood. The relevant error sources include sensitivity error, offset, noise, axis-axis mismatch, nonlinearity, drift across temperature, drift across life time, and so forth. Use the Angle Error Calculation Tool to estimate the total error during angular measurement.

表 8-2 offers an example angular error estimate for X-Y plane with magnetic field range of ±100mT, peak X, Y field of ±80mT, and CONV_AVG =101b. The angle error can be improved by calibrating at room and high temperature, using multi-pole magnet, implementing linearization scheme in the controller, and so forth.

表 8-2. Error Estimates During Angle Measurement

	Angle Error Calculation using Max Magnetic Specification	Expected Angle Error After Offset and Gain Calibrations
Angle error for 360° rotation at 25°C	1.5°	~0.5°
Angle error for 360° rotation across temperature	2.1°	~1.0°

备注

In this section, system level error sources such as mechanical misalignment, vibration, magnet temperature gradient, lifetime drift, and so forth, are not considered. The user must take these additional error sources into account while calculating overall system error budgets.

8.2 Typical Application

Magnetic angle sensors are very popular due to contactless and reliable measurements, especially in applications requiring long-term measurements in rugged environments. The TMAG5170-Q1 offers an on-chip angle calculator that can provide angular measurement based off any two of the magnetic axes. The two axes of interest can be selected in the ANGLE_EN register bits. The device offers an angle output in complete 360 degree scale. Take several error sources into account for angle calculation, including sensitivity error, offset error, linearity error, noise, mechanical vibration, temperature drift, and so forth.

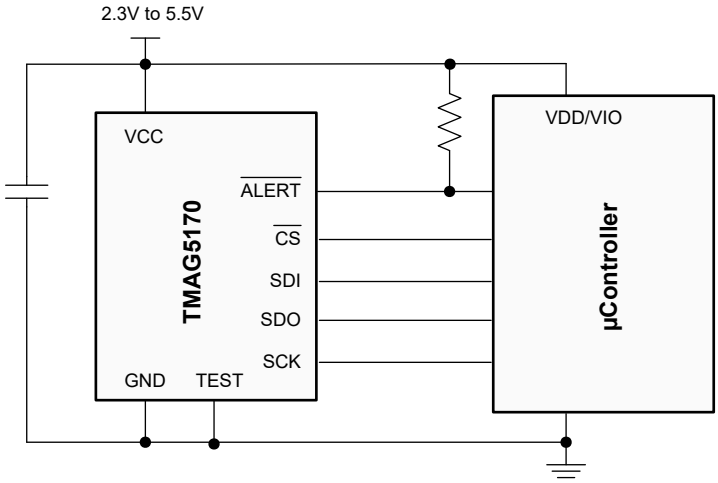

图 8-4. TMAG5170-Q1 Application Diagram

8.2.1 Design Requirements

Use the parameters listed in 表 8-3 for this design example

表 8-3. Design Parameters

DESIGN PARAMETERS	ON-AXIS MEASUREMENT	OFF-AXIS MEASUREMENT
Device	TMAG5170-A1	TMAG5170-A1
VCC	5 V	5 V
Magnet	Cylinder: 4.7625-mm diameter, 12.7-mm thick, neodymium N52, Br = 1480	Cylinder: 4.7625-mm diameter, 12.7-mm thick, neodymium N52, Br = 1480
Magnetic Range Selection	Select the same range for both axes based off the highest possible magnetic field seen by the sensor	Select the same range for both axes based off the highest possible magnetic field seen by the sensor
RPM	<600	<600
Desired Accuracy	<1° for 360° rotation	<1° for 360° rotation

8.2.1.1 Gain Adjustment for Angle Measurement

Common measurement topology include angular position measurements in on-axis or off-axis angular measurements shown in 图 8-5. Select the on-axis measurement topology whenever possible, as this offers the best optimization of magnetic field and the device measurement ranges. The TMAG5170-Q1 offers an on-chip gain adjustment option to account for mechanical position misalignments.



图 8-5. On-Axis vs. Off-Axis Angle Measurements

8.2.2 Detailed Design Procedure

For accurate angle measurement, the two axes amplitudes must be normalized by selecting the proper gain adjustment value in the MAG_GAN_CONFIG register. The gain adjustment value is a fractional decimal number between 0 and 1. The following steps must be followed to calculate this fractional value:

1. Set the device at 32x average mode and rotate the shaft a full 360 degree.
2. Record the two axes sensor ADC codes for the full 360 degree rotation.
3. Measure the maximum peak-peak ADC code delta for each axis, Ax and Ay, as shown in 图 8-6 or 图 8-7.
4. Calculate the gain adjustment value for X axis:

$$G_X = \frac{A_Y}{A_X} \tag{18}$$

5. If G_X>1, apply the gain adjustment value to Y axis:

$$G_Y = \frac{1}{G_X} \tag{19}$$

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6. Calculate the target binary gain setting at the GAIN_VALUE register bits:

$$G_X \text{ or } G_Y = GAIN_VALUE_{decimal} / 1024 \quad (20)$$

Example 1: If $A_X = A_Y = 60{,}000$, the GAIN_SELECTION resister bits can be set as 00b. The GAIN_VALUE register bits are don't care bits in this case.

Example 2: If $A_X = 60{,}000$, $A_Y = 45{,}000$, the $G_X = 45{,}000/60{,}000 = 0.75$. Select 01b for the GAIN_SELECTION register bits.

Example 3: If $A_X = 45{,}000$, $A_Y = 60{,}000$, the $G_X = (60{,}000/45{,}000) = 1.33$. Since $G_X > 1$, the gain adjustment needs to be applied to Y axis with $G_Y = 1/G_X$. Select 10b for the GAIN_SELECTION register bits.

8.2.3 Application Curves

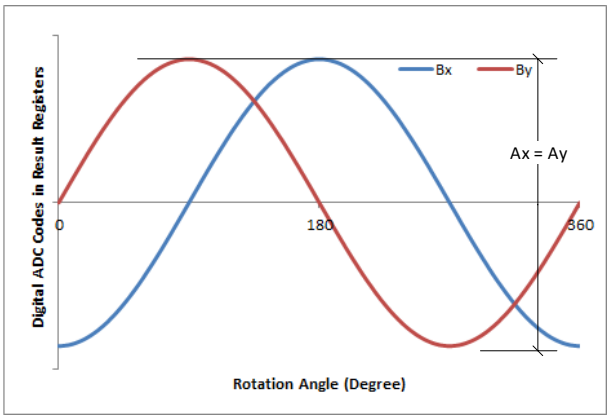

图 8-6. X and Y Sensor Data for Full 360 Degree Rotation for On-Axis Measurement

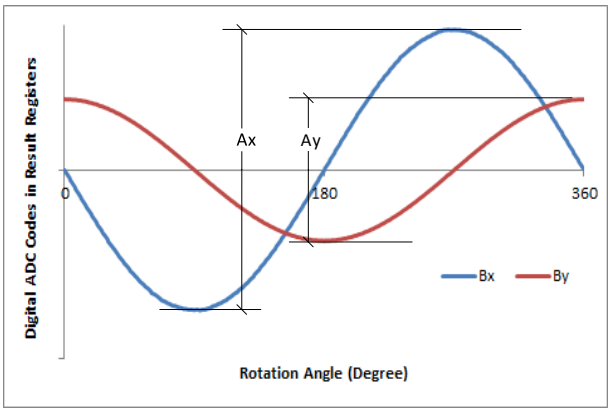

图 8-7. X and Y Sensor Data for Full 360 Degree Rotation for Off-Axis Measurement

8.3 Do's and Don'ts

The TMAG5170-Q1 updates the result registers at the end of a conversion. SPI read of the result register needs to be synchronized with the conversion update time to ensure reading the updated result data. The conversion update time, $t_{measure}$ is defined in the *Electrical Characteristics* table. 图 8-8 shows examples of correct and incorrect SPI read timings for applications with strict timing budgets. Use the $\overline{\text{ALERT}}$ signal to notify the controller when a conversion is complete.

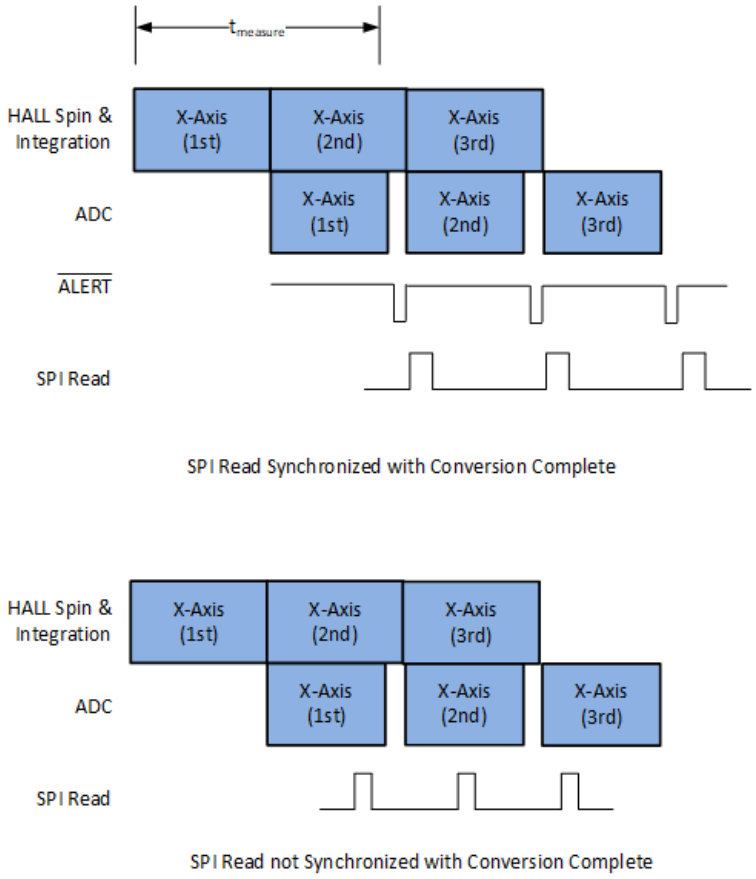

图 8-8. SPI Read During Continuous Conversion

9 Power Supply Recommendations

A decoupling capacitor close to the device must be used to provide local energy with minimal inductance. TI recommends using a ceramic capacitor with a value of at least 0.01 µF. Connect the TEST pin to ground.

10 Layout

10.1 Layout Guidelines

Magnetic fields pass through most nonferromagnetic materials with no significant disturbance. Embedding Hall-effect sensors within plastic or aluminum enclosures and sensing magnets on the outside is common practice. Magnetic fields also easily pass through most printed circuit boards (PCBs), which makes placing the magnet on the opposite side of the PCB possible.

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10.2 Layout Example

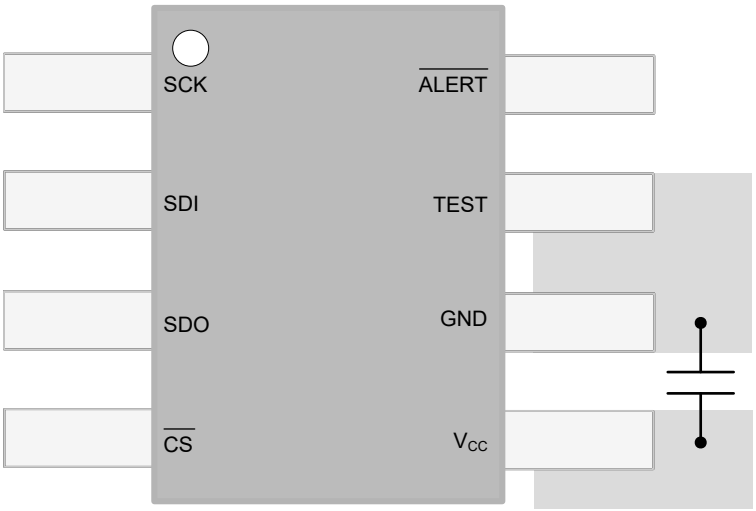

图 10-1. Layout Example With TMAG5170-Q1

11 Device and Documentation Support

11.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMAG5170A1EDGKQ1	ACTIVE	VSSOP	DGK	8	80	TBD	Call TI	Call TI	-40 to 150		Samples
TMAG5170A1EDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	70A1Q	Samples
TMAG5170A2EDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	70A2Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TMAG5170-Q1 :

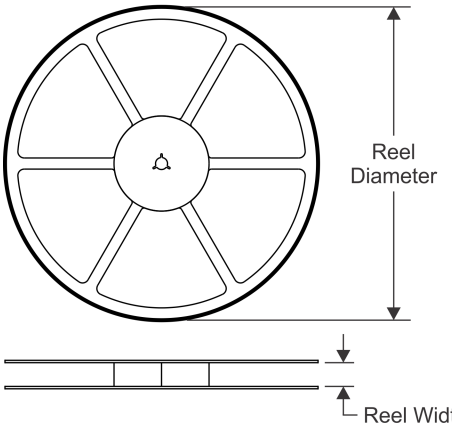
- Catalog : TMAG5170

NOTE: Qualified Version Definitions:

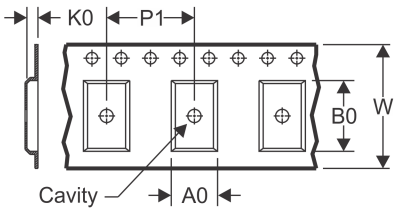
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

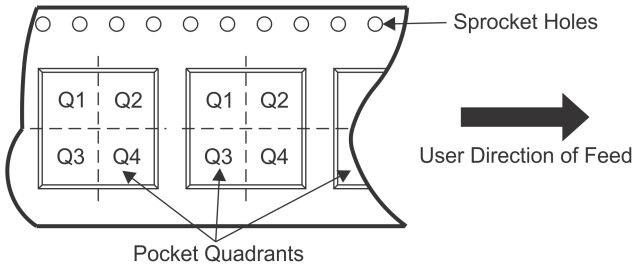


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

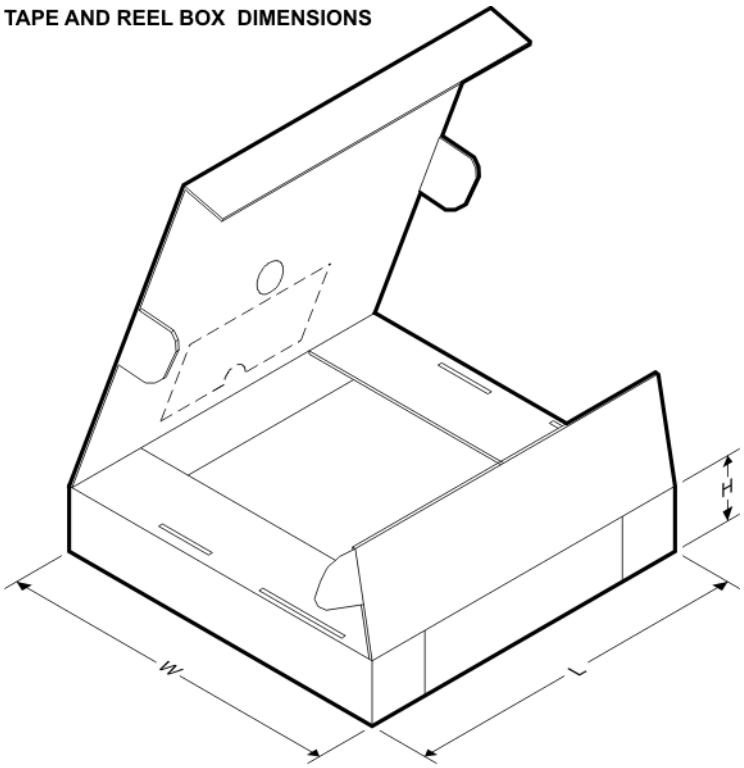
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMAG5170A1EDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMAG5170A2EDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

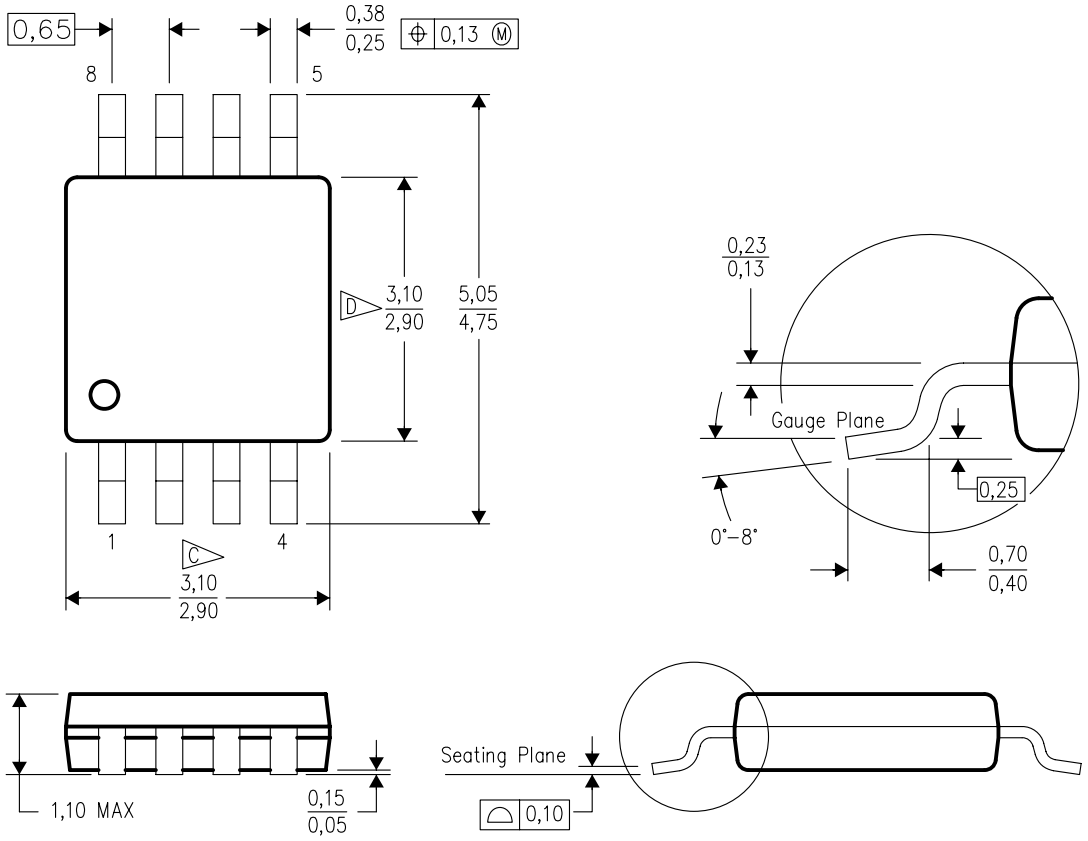
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMAG5170A1EDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMAG5170A2EDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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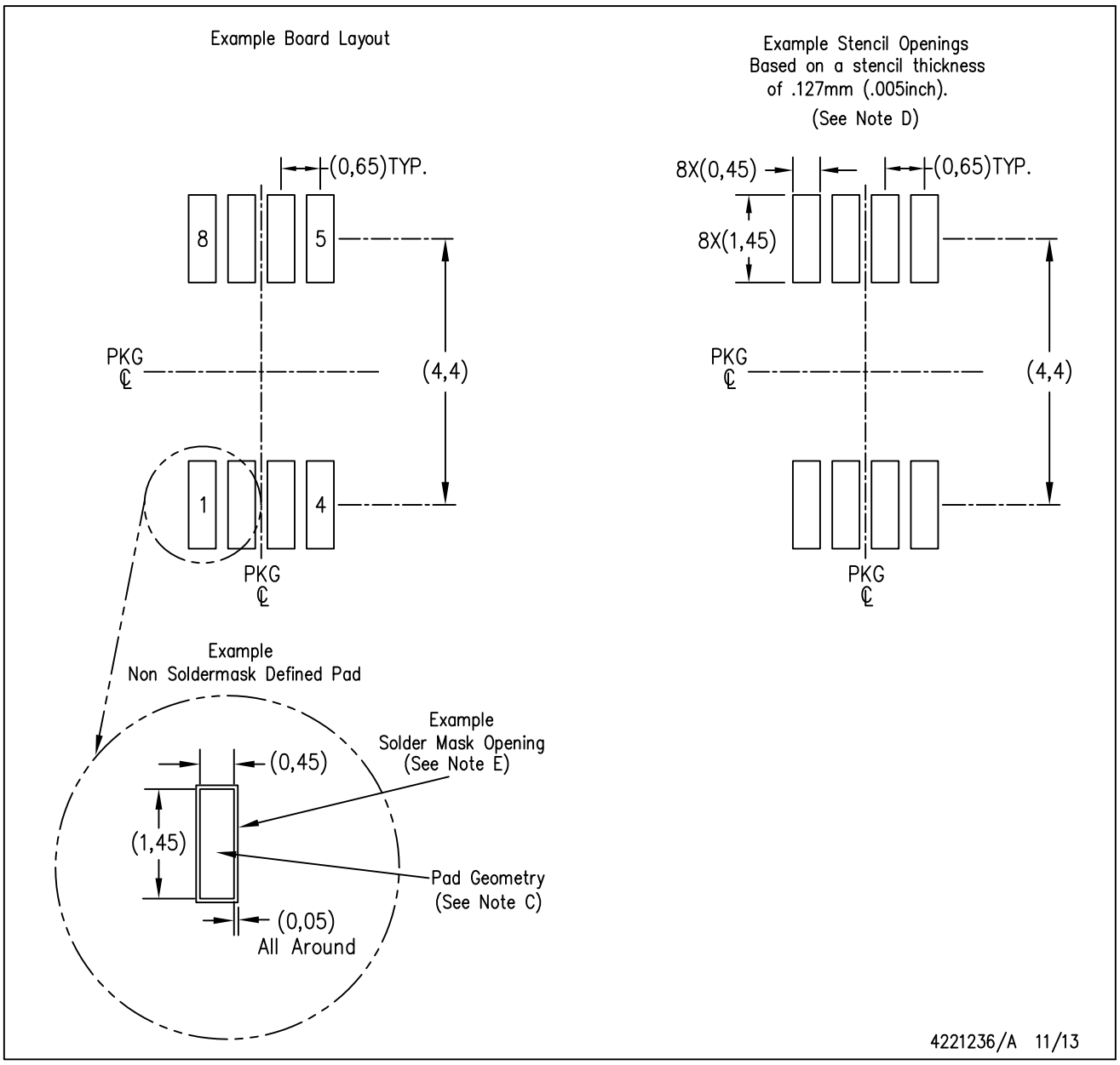
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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