CSD13383F4 12V N 沟道 FemtoFET™ MOSFET

1 特性

- 低导通电阻
- 超低 Q_g和 Q_{gd}
- 超小型封装尺寸（0402 外壳尺寸）
  - 1.0mm × 0.6mm
- 低高度
  - 高度 0.35mm
- 集成型静电放电 (ESD) 保护二极管
  - 额定值 > 2kV 人体放电模型 (HBM)
  - 额定值 > 2kV 充电器件模型 (CDM)
- 无铅且无卤素
- 符合 RoHS 标准

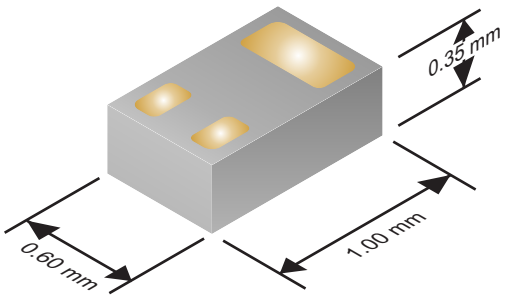
2 应用

- 针对负载开关应用进行了 优化
- 针对通用开关应用进行了 优化
- 单节电池 应用
- 手持式和移动类电感式触控不锈钢键盘参考设计 应用

3 说明

此 37mΩ 12V N 沟道 FemtoFET™MOSFET 技术经过了设计和优化，能够以最大限度减小许多手持式和移动类应用中的 封装尺寸。这项技术能够在替代标准小信号 MOSFET 的同时将封装尺寸减小 60% 以上。

典型部件尺寸



产品概要

T_A = 25°C		典型值	单位
V_{DS}	漏源电压	12	V

产品概要 (接下页)

T_A = 25°C		典型值		单位
Q_g	总栅极电荷 (4.5V)	2.0		nC
Q_{gd}	栅极电荷（栅极到漏极）	0.6		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 2.5V	53	mΩ
		V_{GS} = 4.5 V	37	
$V_{GS(th)}$	阈值电压	1.0		V

订购信息(1)

器件	数量	包装介质	封装	发货
CSD13383F4	3000	7 英寸卷带	Femto(0402) 1.0mm × 0.6mm 无引线表面贴装器件 (SMD)	卷带封装
CSD13383F4T	250			

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

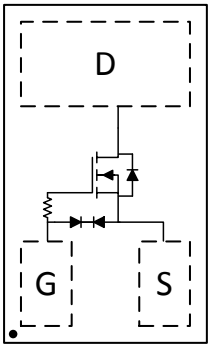
绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	12	V
V_{GS}	栅源电压	±10	V
I_D	持续漏极电流(1)	2.9	A
I_{DM}	脉冲漏极电流(1)(2)	18.5	A
I_G	持续栅极钳位电流	25	mA
	脉冲栅极钳位电流(1)(2)	250	
P_D	功率耗散	500	mW
ESD 额定值	人体放电模型 (HBM)	2	kV
	充电器件模型 (CDM)	2	kV
T_J, T_{stg}	工作结温 贮存温度	–55 至 150	°C
E_{AS}	雪崩能量，单脉冲 I_D = 6.7， L = 0.1mH，R_G = 25Ω	2.2	mJ

(1) 典型值 $R_{\theta JA}$ = 250°C/W

(2) 脉冲持续时间 ≤ 100µs，占空比 ≤ 1%.

顶视图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (January 2016) to Revision B **Page**

- 将 *绝对最大额定值* 表中的 I_{DM} 值从 27A 更改为 18.5A。 1
- Updated Figure 1. 4
- Updated Figure 10 using Typ $R_{\theta JA}$ = 250°C/W. 5
- 更新了所有机械制图，在*推荐的模版布局* 部分增加了焊盘尺寸。 8

Changes from Original (December 2014) to Revision A **Page**

- Changed the $t_{d(on)}$ value From: 39 ns To: 46 ns in the *Electrical Characteristics* table. 3
- Changed the t_r value From: 123 ns To: 122 ns in the *Electrical Characteristics* table. 3
- Changed the $t_{d(off)}$ value From: 96 ns To: 250 ns in the *Electrical Characteristics* table. 3
- Changed the t_f value From: 315 ns To: 290 ns in the *Electrical Characteristics* table. 3
- 已添加 *社区资源* 部分。 7

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = 250 μA	12			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 9.6 V			1	μA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 10 V			10	μA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	0.70	1.00	1.25	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 2.5 V, I_{DS} = 0.5 A		53	65	mΩ
		V_{GS} = 4.5 V, I_{DS} = 0.5 A		37	44	mΩ
g_{fs}	Transconductance	V_{DS} = 6 V, I_{DS} = 0.5 A		5.4		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 6 V, f = 1 MHz		224	291	pF
C_{oss}	Output capacitance			68	88	pF
C_{rss}	Reverse transfer capacitance			47	61	pF
R_G	Series gate resistance			240		Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 6 V, I_{DS} = 0.5 A		2.0	2.6	nC
Q_{gd}	Gate charge gate-to-drain			0.6		nC
Q_{gs}	Gate charge gate-to-source			0.4		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.1		nC
Q_{oss}	Output charge	V_{DS} = 6 V, V_{GS} = 0 V		0.9		nC
$t_{d(on)}$	Turn on delay time	V_{DS} = 6 V, V_{GS} = 4.5 V, I_{DS} = 0.5 A, R_G = 2 Ω		46		ns
t_r	Rise time			122		ns
$t_{d(off)}$	Turn off delay time			250		ns
t_f	Fall time			290		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 0.5 A, V_{GS} = 0 V		0.7	1.0	V

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)		90		°C/W
	Junction-to-ambient thermal resistance(2)		250		

(1) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

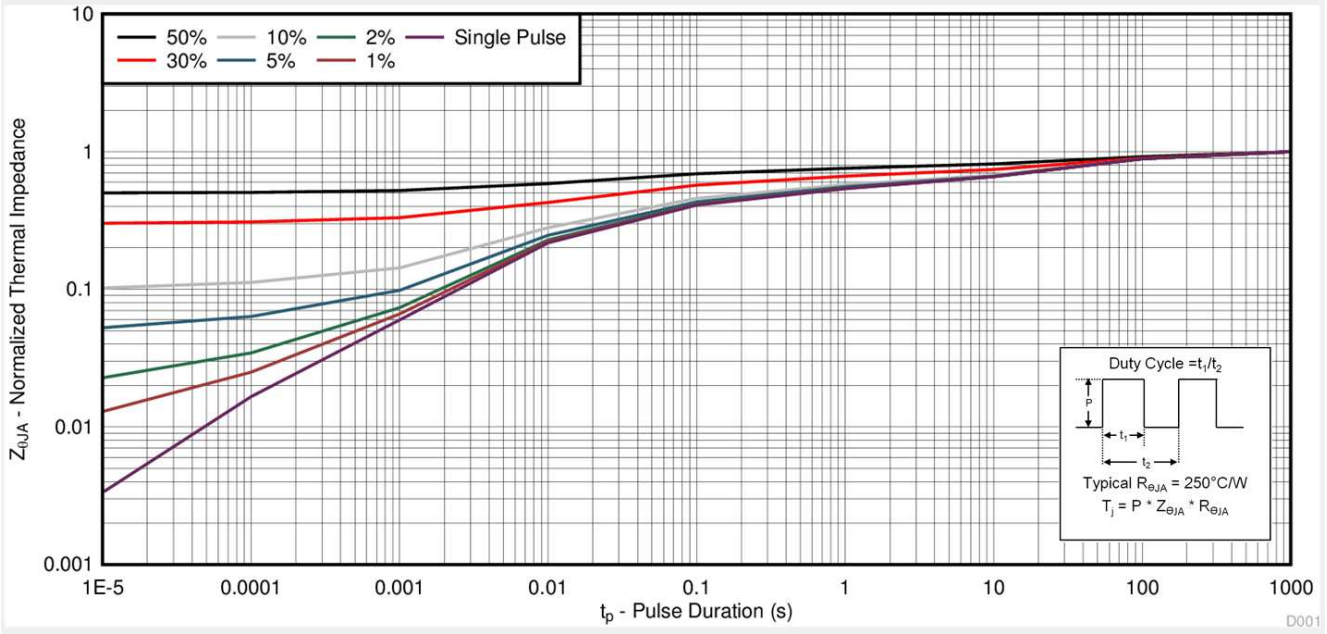


Figure 1. Transient Thermal Impedance

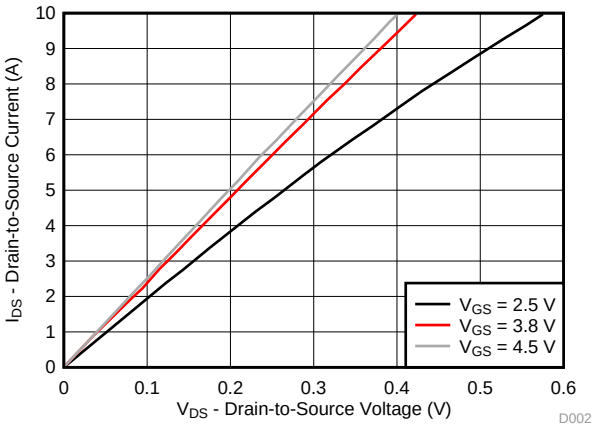


Figure 2. Saturation Characteristics

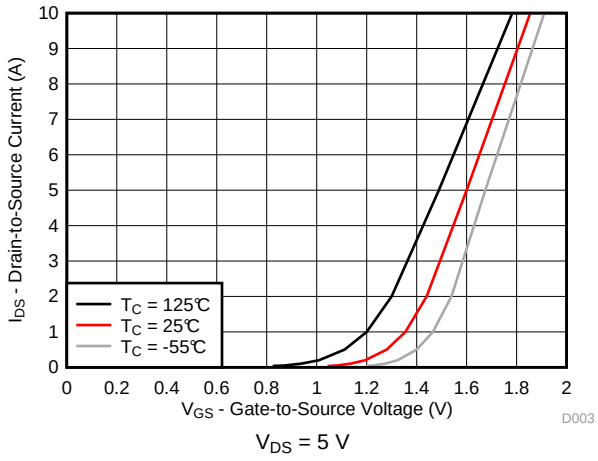


Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

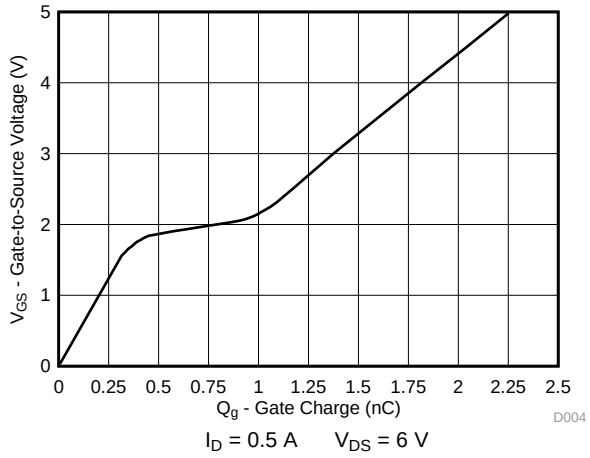


Figure 4. Gate Charge

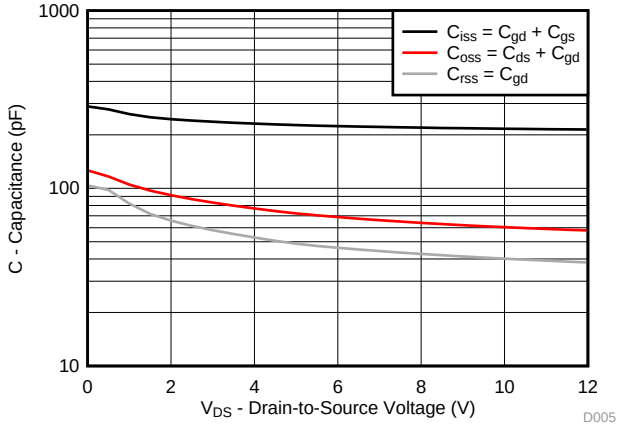


Figure 5. Capacitance

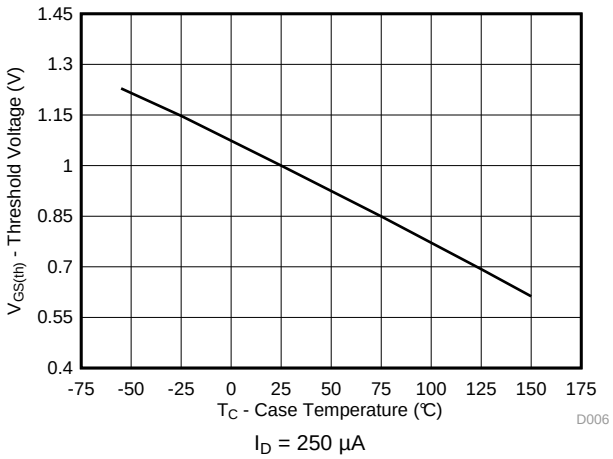


Figure 6. Threshold Voltage vs Temperature

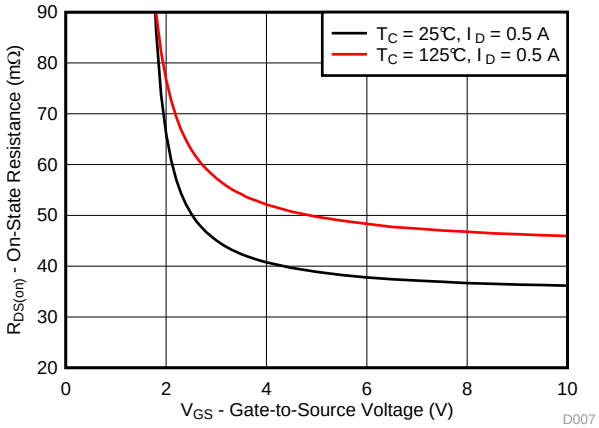


Figure 7. On-State Resistance vs Gate-to-Source Voltage

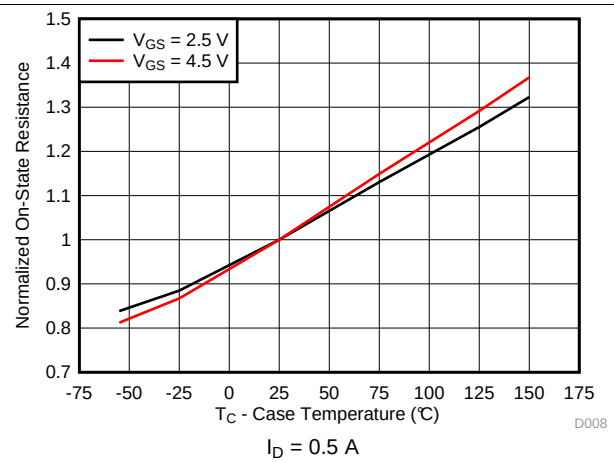


Figure 8. Normalized On-State Resistance vs Temperature

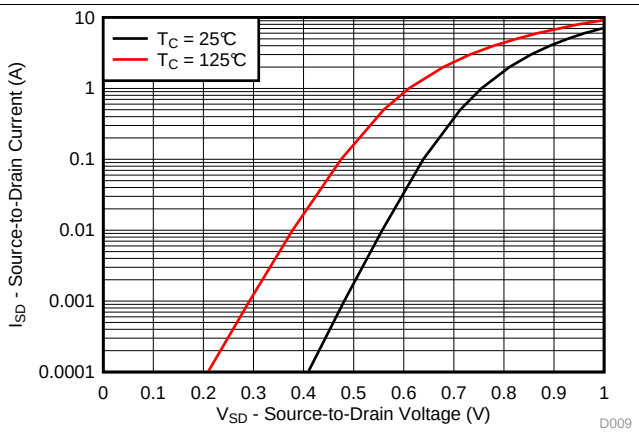


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

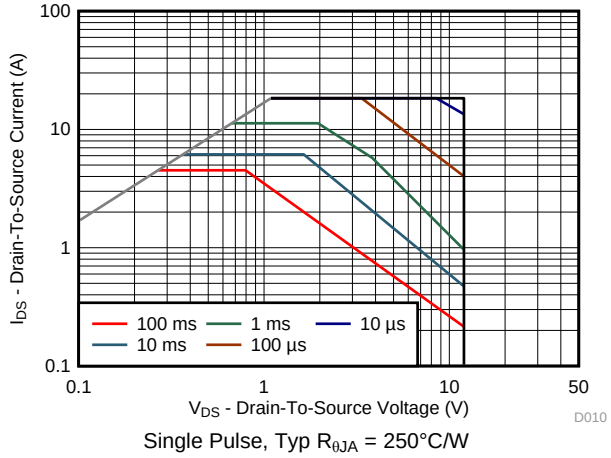


Figure 10. Maximum Safe Operating Area (SOA)

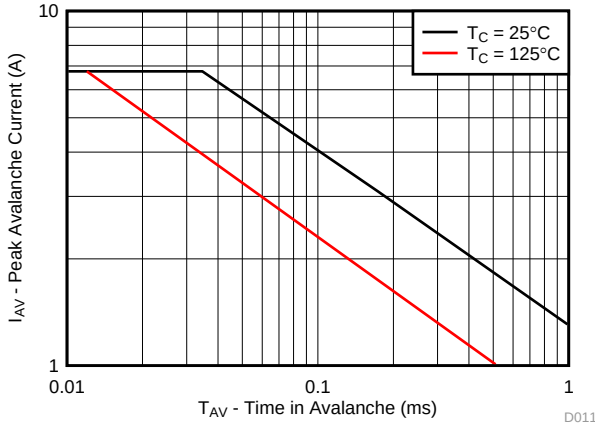


Figure 11. Single Pulse Unclamped Inductive Switching

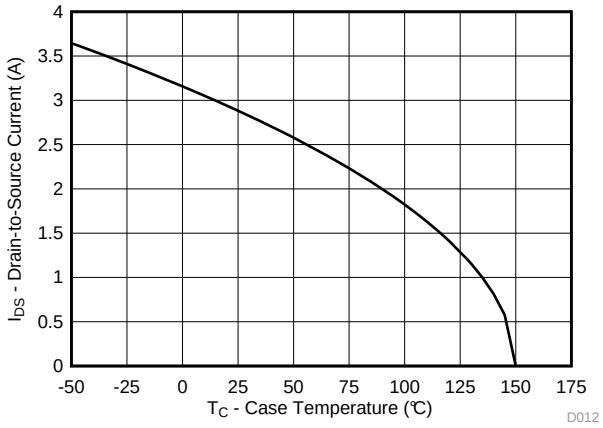


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

6.2 商标

FemtoFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.4 Glossary

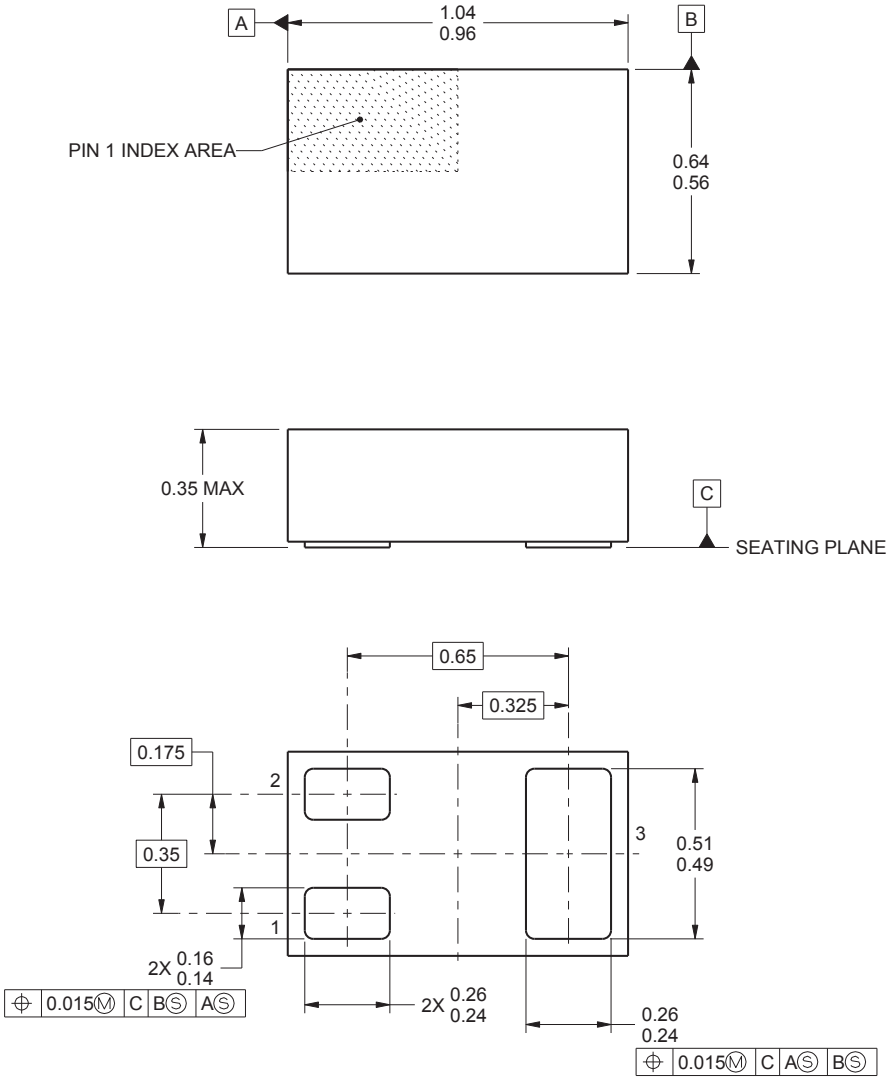
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

7.1 机械尺寸

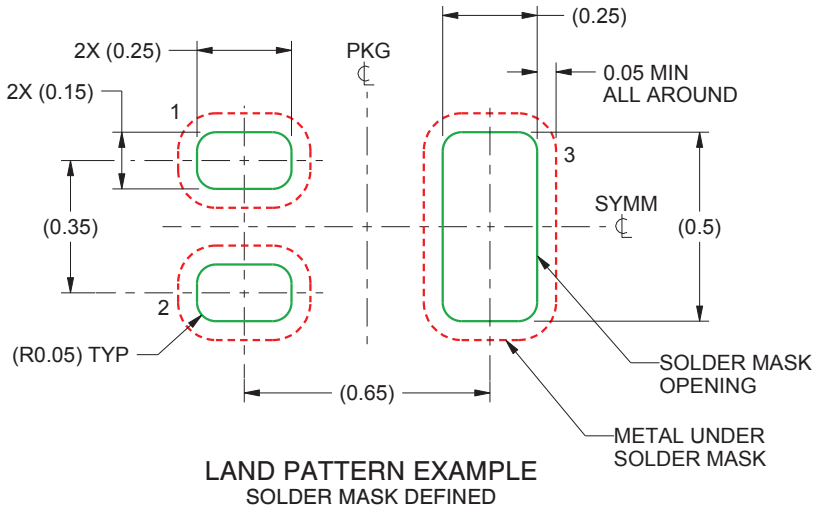


(1) 所有线性尺寸的单位均为毫米。括号中的任何尺寸仅供参考。尺寸和公差值符合 ASME Y14.5M 标准。

(2) 本图如有变更，恕不另行通知。

(3) 此封装为无铅凸点设计。凸点涂料可能有所不同。要确定确切的涂料，请参阅器件数据表或联系当地的 TI 代表。

7.2 建议的最小 PCB 布局

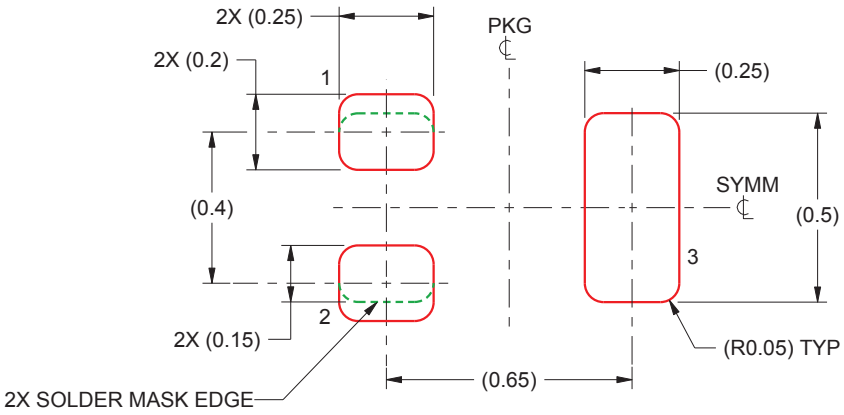


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED

(1) 所有尺寸的单位均为毫米。

(2) 有关更多信息，请参阅《*QFN/SON PCB 连接*》(SLUA271)。

7.3 推荐的模版布局



SOLDER PASTE EXAMPLE

(1) 所有尺寸的单位都是毫米。

(2) 具有漏斗形壁和圆角的激光切割孔可提供更佳的锡膏脱离。IPC-7525 可能提供替代设计建议。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD13383F4	ACTIVE	PICOSTAR	YJC	3	3000	RoHS & Green	NIAU	Level-1-260C-UNLIM		GC	Samples
CSD13383F4T	ACTIVE	PICOSTAR	YJC	3	250	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	GC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

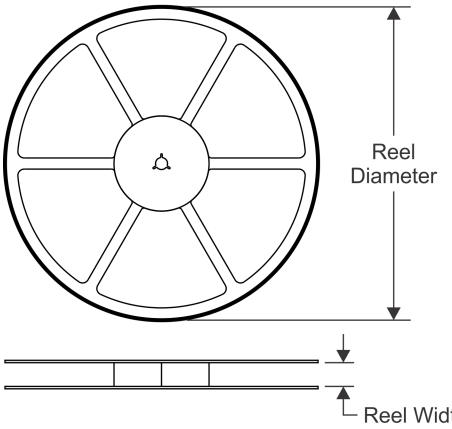
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

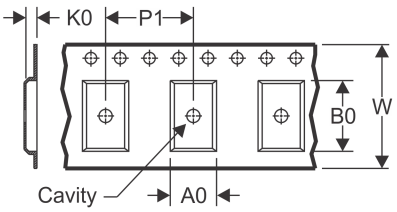
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

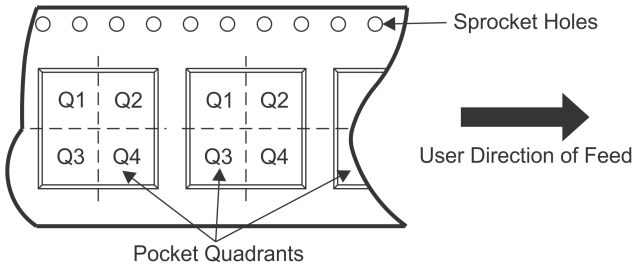


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

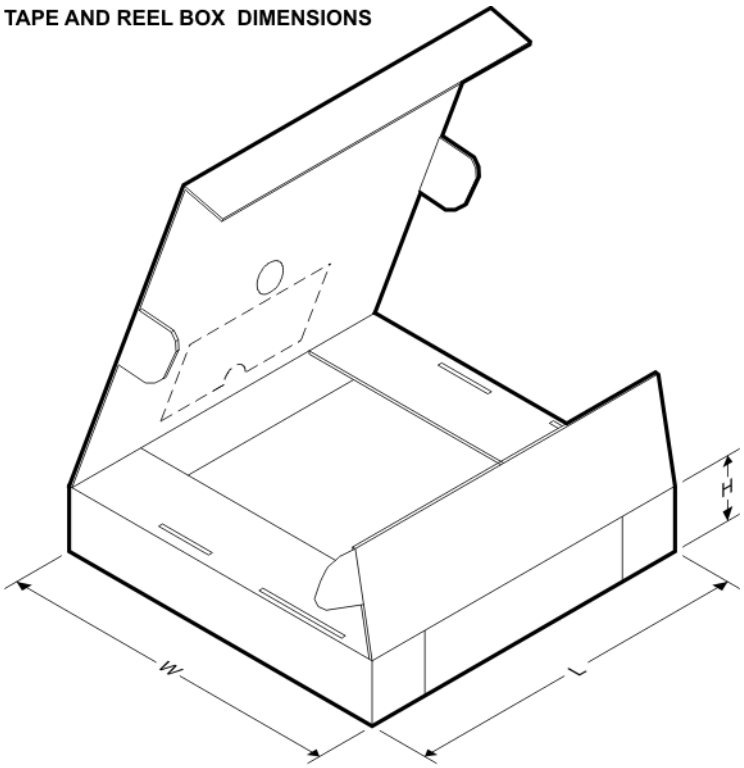
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD13383F4	PICOSTAR	YJC	3	3000	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD13383F4	PICOSTAR	YJC	3	3000	178.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD13383F4T	PICOSTAR	YJC	3	250	178.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD13383F4T	PICOSTAR	YJC	3	250	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD13383F4	PICOSTAR	YJC	3	3000	182.0	182.0	20.0
CSD13383F4	PICOSTAR	YJC	3	3000	220.0	220.0	35.0
CSD13383F4T	PICOSTAR	YJC	3	250	220.0	220.0	35.0
CSD13383F4T	PICOSTAR	YJC	3	250	182.0	182.0	20.0

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

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