SN65LVDxx High-Speed Differential Line Drivers and Receivers

1 Features

- Meets or Exceeds the ANSI TIA/EIA-644 Standard
- Designed for Signaling Rates (1) up to:
  - 630 Mbps for Drivers
  - 400 Mbps for Receivers
- Operates From a 2.4-V to 3.6-V Supply
- Available in SOT-23 and SOIC Packages
- Bus-Terminal ESD Exceeds 9 kV
- Low-Voltage Differential Signaling With Typical Output Voltages of 350 mV Into a 100-Ω Load
- Propagation Delay Times
  - 1.7-ns Typical Driver
  - 2.5-ns Typical Receiver
- Power Dissipation at 200 MHz
  - 25 mW Typical Driver
  - 60 mW Typical Receiver
- LVDT Receiver Includes Line Termination
- Low Voltage TTL (LVTTL) Level Driver Input Is 5-V Tolerant
- Driver Is Output High-Impedance with V_{CC} < 1.5 V
- Receiver Output and Inputs are High-Impedance With V_{CC} < 1.5 V
- Receiver Open-Circuit Fail Safe
- Differential Input Voltage Threshold Less Than 100 mV

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bit per second)

2 Applications

- Wireless Infrastructure
- Telecom Infrastructure
- Printer

3 Description

The SN65LVDS1, SN65LVDS2, and SN65LVDT2 devices are single, low-voltage, differential line drivers and receivers in the small-outline transistor package. The outputs comply with the TIA/EIA-644 standard and provide a minimum differential output voltage magnitude of 247 mV into a 100-Ω load at signaling rates up to 630 Mbps for drivers and 400 Mbps for receivers.

When the SN65LVDS1 device is used with an LVDS receiver (such as the SN65LVDT2) in a point-to-point connection, data or clocking signals can be transmitted over printed-circuit board traces or cables at very high rates with very low electromagnetic emissions and power consumption. The packaging, low power, low EMI, high ESD tolerance, and wide supply voltage range make the device ideal for battery-powered applications.

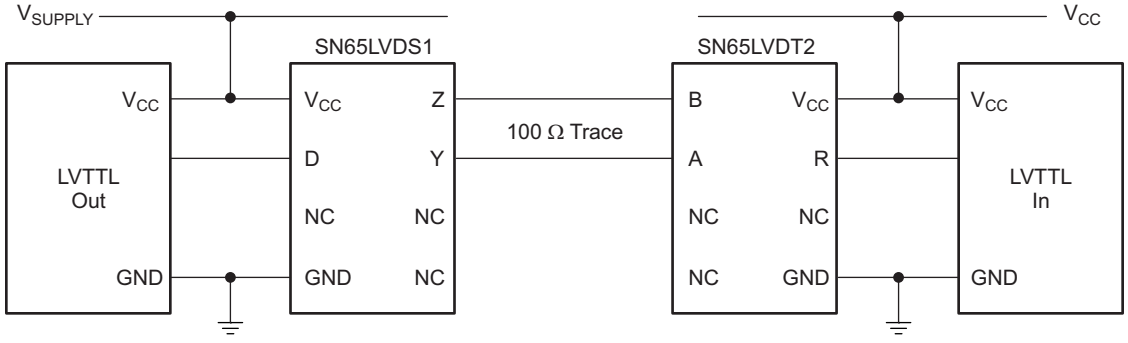
The SN65LVDS1, SN65LVDS2, and SN65LVDT2 devices are characterized for operation from –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65LVDS1	SOIC (8)	4.90 mm × 3.91 mm
	SOT (5)	2.90 mm × 1.60 mm
SN65LVDS2	SOIC (8)	4.90 mm × 3.91 mm
	SOT (5)	2.90 mm × 1.60 mm
SN65LVDT2	SOIC (8)	4.90 mm × 3.91 mm
	SOT (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision K (November 2008) to Revision L **Page**

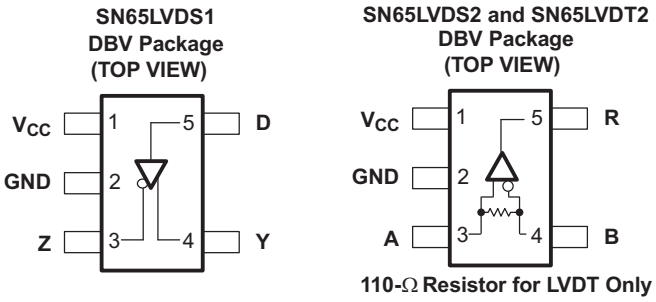
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

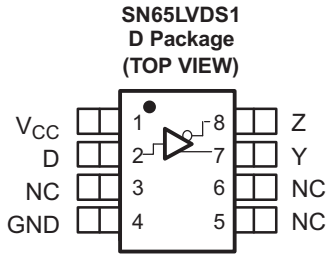
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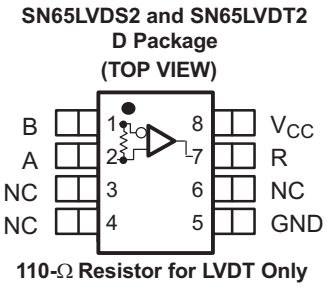
5 Device Options

PART NUMBER	INTEGRATED TERMINATION	PACKAGE
SN65LVDS1DBV		SOT-23 (5)
SN65LVDS1D		SOIC (8)
SN65LVDS2DBV		SOT-23 (5)
SN65LVDS2D		SOIC (8)
SN65LVDT2DBV	√	SOT-23 (5)
SN65LVDT2D	√	SOIC (8)

6 Pin Configuration and Functions







Pin Functions: SN65LVDS1

PIN			I/O	DESCRIPTION
NAME	DBV	D		
V_{CC}	1	1	--	Supply voltage
GND	2	4	--	Ground
D	5	2	I	LVTTL input signal
Y	4	7	O	Differential (LVDS) non-inverting output
Z	3	8	O	Differential (LVDS) inverting output
NC	--	3, 5, 6	--	No connect

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Pin Functions: SN65LVDS2, SN65LVDT2

PIN			I/O	DESCRIPTION
NAME	DBV	D		
V_{CC}	1	8	--	Supply voltage
GND	2	5	--	Ground
A	3	2	I	Differential (LVDS) non-inverting output
B	4	1	I	Differential (LVDS) inverting output
R	5	7	O	LVTTL output signal
NC	--	3, 4, 6	--	No connect

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
Supply voltage range, V_{CC} (2)		–0.5	4	V
Input voltage range, V_I	(A or B)	–0.5	4	V
	(D)	–0.5	V_{CC} + 2	V
Output voltage, V_O	(Y or Z)	–0.5	4	V
Differential input voltage magnitude, $\|V_{ID}\|$	SN65LVDT2 only		1	V
Receiver output current, I_O		–12	12	mA
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages are with respect to network ground terminal.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model electrostatic discharge, HBM ESD(1)	All pins	±4000	V
			Bus pins (A, B, Y, Z)	±9000	
		Machine-model electrostatic discharge, MM ESD(2)		±400	
		Field-induced-charge device model electrostatic discharge, FCDM ESD(3)		±1500	

(1) Test method based upon JEDEC Standard 22, Test Method A114-A. Bus pins stressed with respect to GND and V_{CC} separately.
(2) Test method based upon JEDEC Standard 22, Test Method A114-A.
(3) Test method based upon EIA-JEDEC JESD22-C101C.

7.3 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.4	3.3	3.6	V
V_{IH}	High-level input voltage	2		5	V
V_{IL}	Low-level input voltage	0		0.8	V
T_A	Operating free-air temperature	–40		85	°C
$\|V_{ID}\|$	Magnitude of differential input voltage	0.1		0.6	V
	Input voltage (any combination of input or common-mode voltage)	0		V_{CC} – 0.8	V

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7.4 Thermal Information

THERMAL METRIC(1)		SN65LVDS1, SN65LVDS2, SN65LVDT2		UNIT
		D	DBV	
		8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	172.4	322.6	°C/W
Power rating	$T_A \le 25°C$	725	385	mW
	$T_A \le 85°C$	402	200	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Driver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX	UNIT
$\lvert V_{OD}\rvert$	Differential output voltage magnitude	R_L = 100 Ω, 2.4 ≤ V_{CC} < 3 V	200	350	454	mV
		R_L = 100 Ω, 3 ≤ V_{CC} < 3.6 V	247	350	454	
$\Delta\lvert V_{OD}\rvert$	Change in differential output voltage magnitude between logic states	See Figure 10	–50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 10	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			25	100	mV
I_{CC}	Supply current	V_I = 0 V or V_{CC}, No load		2	4	mA
		V_I = 0 V or V_{CC}, R_L = 100 Ω		5.5	8	
I_{IH}	High-level input current	V_{IH} = 5 V		2	20	µA
I_{IL}	Low-level input current	V_{IL} = 0.8 V		2	10	µA
I_{OS}	Short-circuit output current	V_{OY} or V_{OZ} = 0 V		3	10	mA
		V_{OD} = 0 V			10	
$I_{O(OFF)}$	Power-off output current	V_{CC} = 1.5 V, V_O = 3.6 V	–1		1	µA
C_i	Input capacitance	V_I = 0.4sin(4E6πt) + 0.5 V		3		pF

(1) The algebraic convention, in which the least positive (most negative) limit is designated as a minimum, is used in this data sheet.
(2) All typical values are at 25°C and with a 3.3-V supply.

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7.6 Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN(1)	TYP(2)	MAX	UNIT
V_{ITH+}	Positive-going differential input voltage threshold		See Figure 11			100	mV
$V_{ITH–}$	Negative-going differential input voltage threshold			–100			
V_{OH}	High-level output voltage		I_{OH} = –8 mA, V_{CC} = 2.4 V	1.9			V
			I_{OH} = –8 mA, V_{CC} = 3 V	2.4			
V_{OL}	Low-level output voltage		I_{OL} = 8 mA		0.25	0.4	V
I_{CC}	Supply current		No load, Steady state		4	7	mA
I_I	Input current (A or B inputs)	LVDS2	V_I = 0 V, other input = 1.2 V	–20		–2	µA
			V_I = 2.2 V, other input = 1.2 V, V_{CC} = 3.0 V		–3	–1.2	
		LVDT2	V_I = 0 V, other input open	–40		-4	
			V_I = 2.2 V, other input open, V_{CC} = 3.0 V		–6	–2.4	
I_{ID}	Differential input current ($I_{IA} – I_{IB}$)	LVDS2	V_{IA} = 2.4 V, V_{IB} = 2.3 V	–2		2	µA
$I_{I(OFF)}$	Power-off input current (A or B inputs)	LVDS2	V_{CC} = 0 V, V_{IA} = V_{IB} = 2.4 V			20	µA
		LVDT2	V_{CC} = 0 V, V_{IA} = V_{IB} = 2.4 V			40	
R_T	Differential input resistance	LVDT2	V_{IA} = 2.4 V, V_{IB} = 2.2 V	90	111	132	Ω
C_I	Input capacitance		V_I = 0.4sin(4E6πt) + 0.5 V		5.8		pF
C_O	Output capacitance		V_I = 0.4sin(4E6πt) + 0.5 V		3.4		pF

(1) The algebraic convention, in which the least positive (most negative) limit is designated as a minimum, is used in this data sheet.
(2) All typical values are at 25°C and with a 2.7-V supply.

7.7 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100 Ω, C_L = 10 pF, See Figure 13		1.5	3.1	ns
t_{PHL}	Propagation delay time, high-to-low-level output			1.8	3.1	ns
t_r	Differential output signal rise time			0.6	1	ns
t_f	Differential output signal fall time			0.7	1	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)(2)			0.3		ns

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

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7.8 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 14		1.4	2.6	3.6	ns
t_{PHL}	Propagation delay time, high-to-low-level output			1.4	2.5	3.6	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL} - t_{pLH} \rvert$)(2)				0.1	0.6	ns
t_r	Output signal rise time				0.8	1.4	ns
t_f	Output signal fall time				0.8	1.4	ns
$t_{r(slew)}$	Output slew rate (rising)	C_L = 10 pF	V_{CC} = 3.0 V – 3.6 V	2.2	3	5.5	V/ns
			V_{CC} = 2.4 V – 2.7 V	1.5	1.9	2.9	V/ns
$t_{f(slew)}$	Output slew rate (falling)		V_{CC} = 3.0 V – 3.6 V	2.7	3.8	6	V/ns
			V_{CC} = 2.4 V – 2.7 V	2.1	2.3	3.9	V/ns

(1) All typical values are at 25°C and with a 2.7-V supply.
(2) $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

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7.9 Typical Characteristics

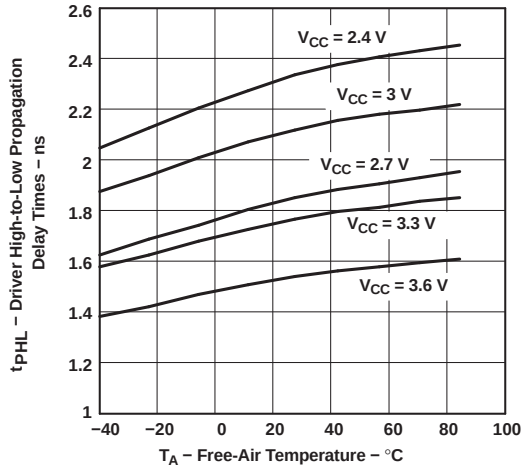


Figure 1. Driver High-to-Low Level Propagation Delay Times vs Free-Air Temperature

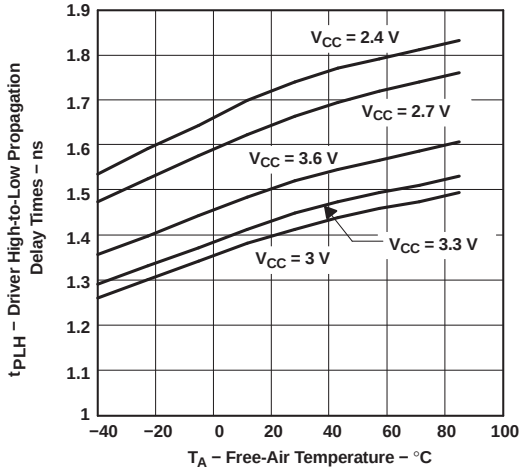


Figure 2. Driver Low-to-High Level Propagation Delay Times vs Free-Air Temperature

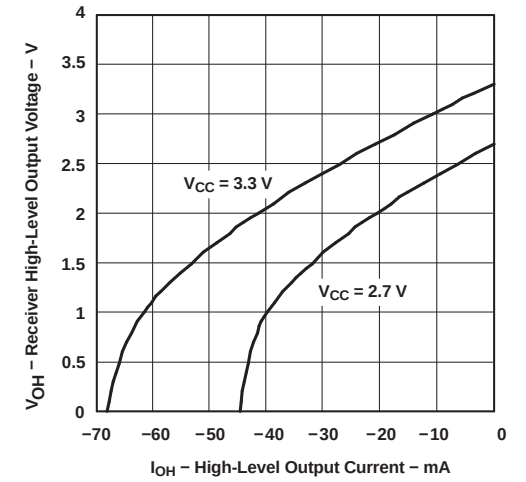


Figure 3. Receiver High-Level Output Voltage vs High-Level Output Current

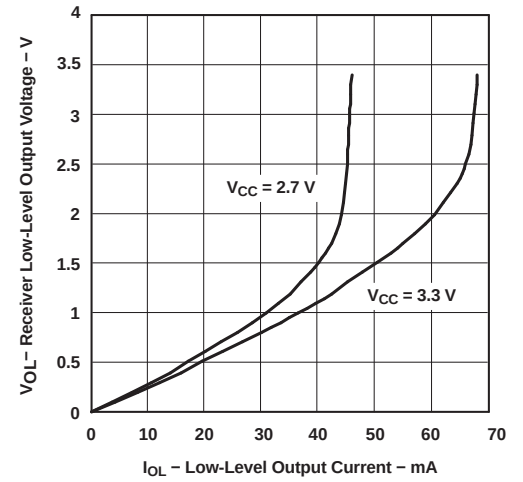


Figure 4. Receiver Low-Level Output Voltage vs Low-Level Output Current

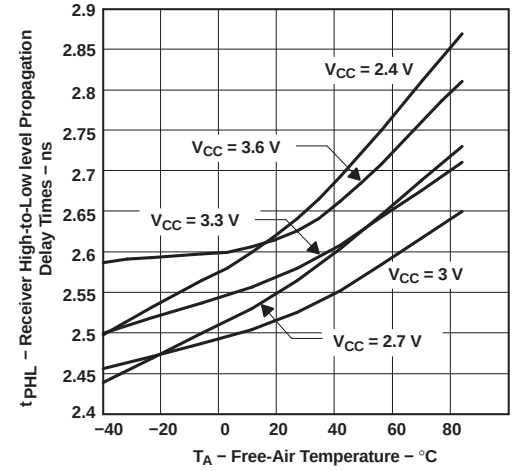


Figure 5. Receiver High-to-Low Level Propagation Delay Times vs Free-Air Temperature

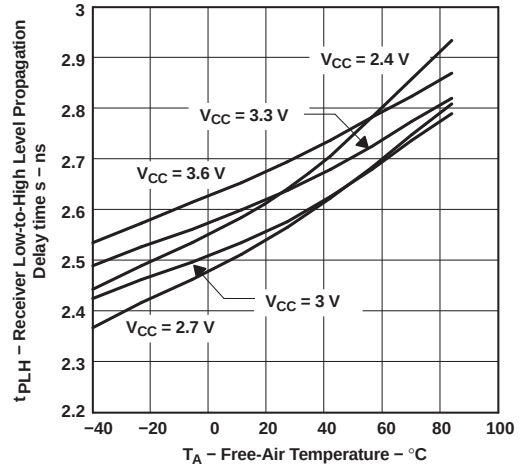


Figure 6. Receiver Low-to-High Level Propagation Delay Times vs Free-Air Temperature

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Typical Characteristics (continued)

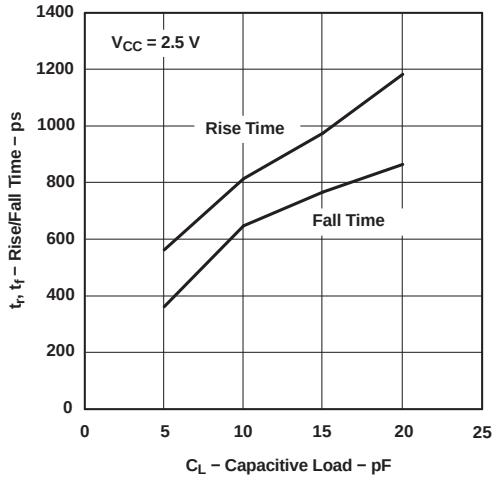


Figure 7. Rise or Fall Time vs Capacitive Load

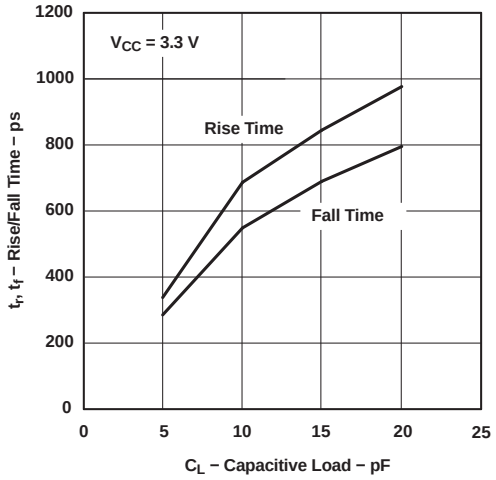


Figure 8. Rise or Fall Time vs Capacitive Load

8 Parameter Measurement Information

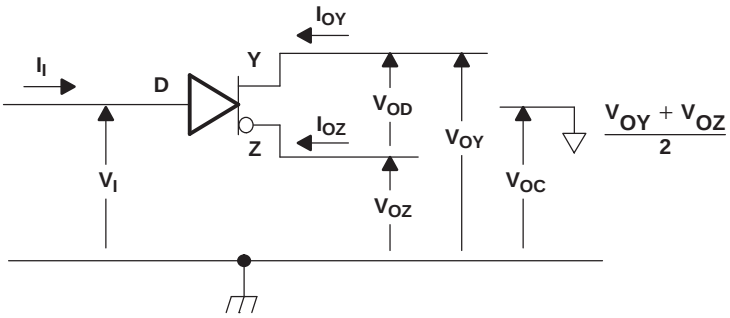
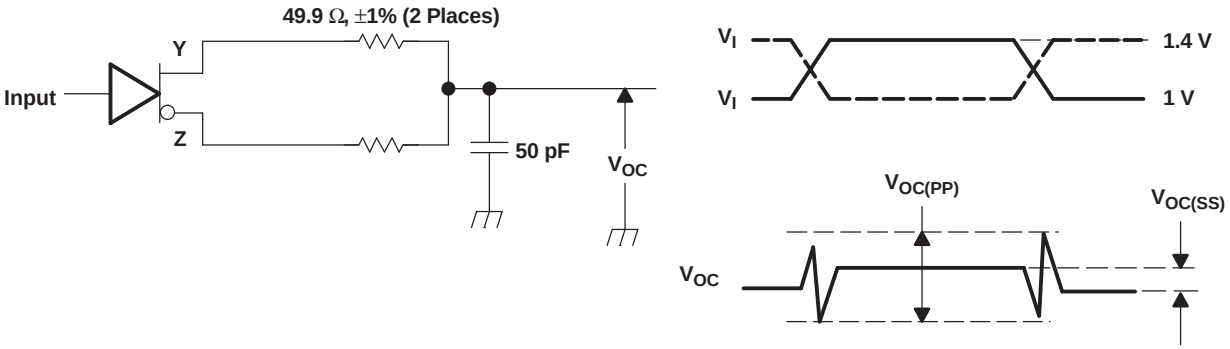


Figure 9. Driver Voltage and Current Definitions



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0.06 mm of the device under test. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3dB bandwidth of at least 300 MHz.

Figure 10. Driver Test Circuit and Definitions for the Driver Common-Mode Output Voltage

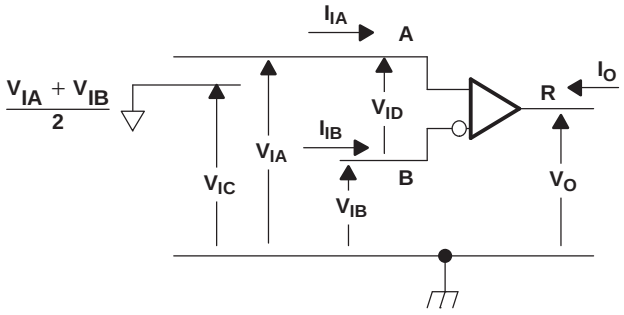
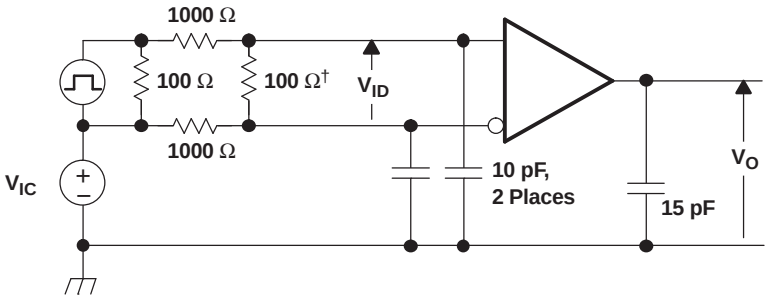


Figure 11. Receiver Voltage and Current Definitions

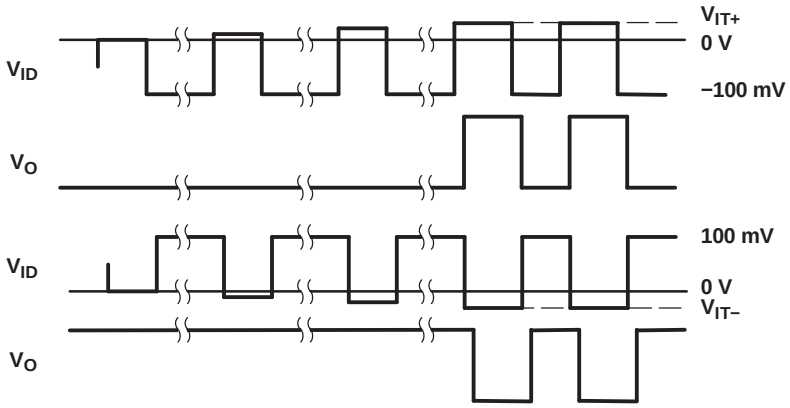
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Parameter Measurement Information (continued)



† Remove for testing LVDT device.

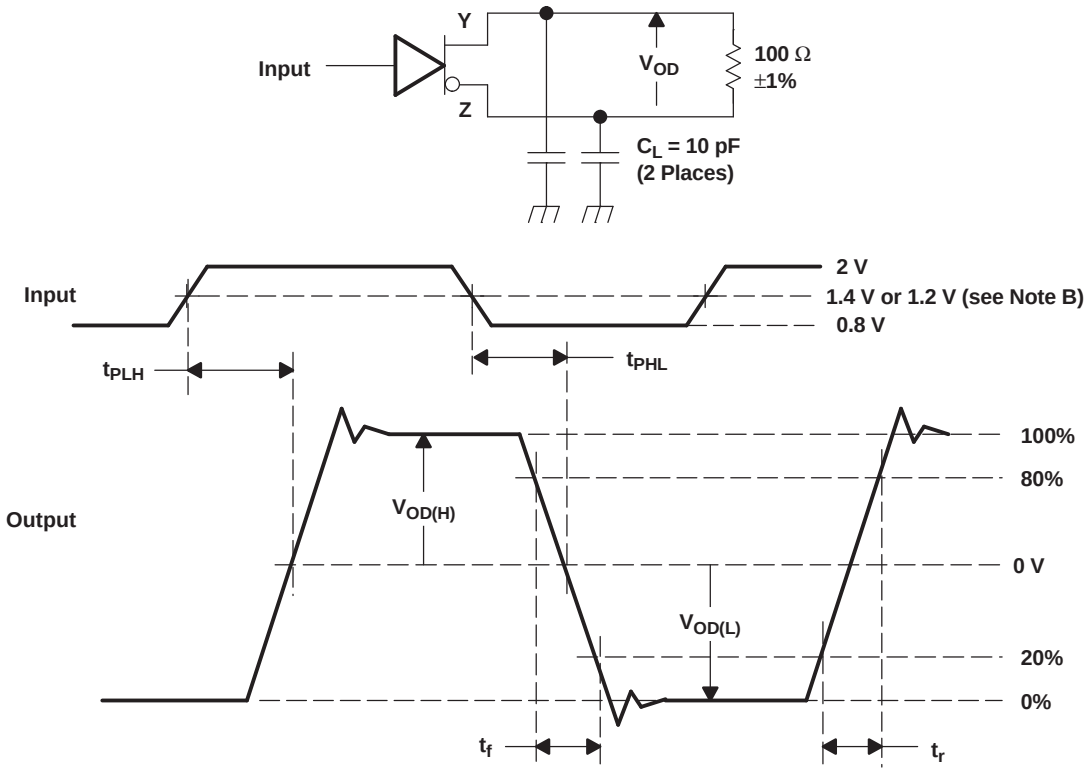
NOTE: Input signal of 3 Mpps, duration of 167 ns, and transition time of < 1 ns.



NOTE: Input signal of 3 Mpps, duration of 167 ns, and transition time of <1 ns.

Figure 12. V_{IT+} and V_{IT-} Input Voltage Threshold Test Circuit and Definitions

Parameter Measurement Information (continued)



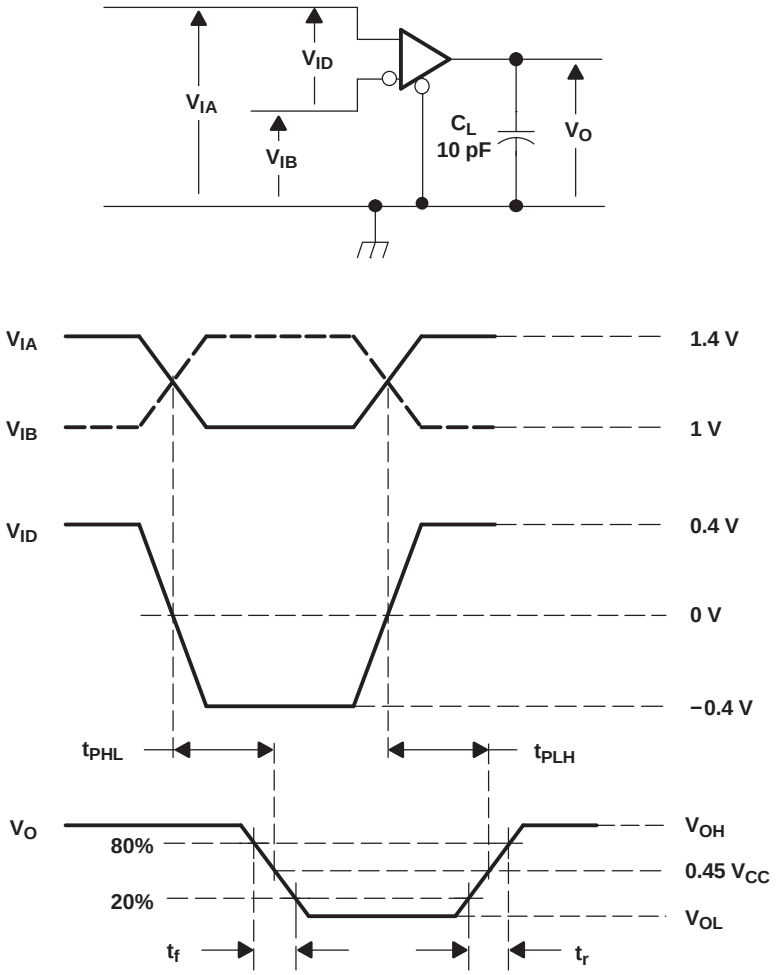
A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0.06 mm of the device under test.

B. This point is 1.4 V with V_{CC} = 3.3 V or 1.2 V with V_{CC} = 2.7 V.

Figure 13. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

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Parameter Measurement Information (continued)



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0.06 m of the device under test.

Figure 14. Receiver Timing Test Circuit and Waveforms

9 Detailed Description

9.1 Overview

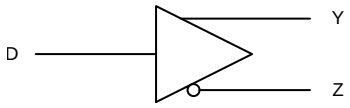
The SN65LVDS1 device is a single-channel, low-voltage differential signaling (LVDS) line driver. It operates from a single supply that is nominally 3.3 V, but can be as low as 2.4 V and as high as 3.6 V. The input signal to the SN65LVDS1 is an LVTTL signal. The output of the device is a differential signal complying with the LVDS standard (TIA/EIA-644). The differential output signal operates with a signal level of 340 mV, nominally, at a common-mode voltage of 1.2 V. This low differential output voltage results in a low emitted radiated energy, which is dependent on the signal slew rate. The differential nature of the output provides immunity to common-mode coupled signals that the driven signal may experience.

The SN65LVDS1 device is intended to drive a 100-Ω transmission line. This transmission line may be a printed-circuit board (PCB) or cabled interconnect. With transmission lines, the optimum signal quality and power delivery is reached when the transmission line is terminated with a load equal to the characteristic impedance of the interconnect. Likewise, the driven 100-Ω transmission line should be terminated with a matched resistance.

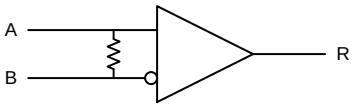
The SN65LVDS2 device is a single-channel LVDS line receiver. It also operates from a single supply that is nominally 3.3 V, but can be as low as 2.4 V and as high as 3.6 V. The input signal to the SN65LVDS2 is a differential LVDS signal. The output of the device is a LVTTL digital signal. This LVDS receiver requires ±100 mV of input signal to determine the correct state of the received signal compliant LVDS receivers can accept input signals with a common-mode range between 0.05 V and 2.35 V. As the common-mode output voltage of an LVDS driver is 1.2 V, the SN65LVDS2 correctly determines the line state when operated with a 1-V ground shift between driver and receiver.

The SN65LVDT2 device is also a single-channel LVDS receiver. This device differs from the SN65LVDS2 in that it incorporates an integrated termination resistor along with the receiver. This termination would take the place of the matched load line termination mentioned above. The SN65LVDT2 can be used in a point-to-point system or in a multidrop system when it is the last receiver on the multidrop bus. The SN65LVDT2 device should not be used at every node in a multidrop system as this would change the loaded bus impedance throughout the bus resulting in multiple reflections and signal distortion.

9.2 Functional Block Diagram



SN65LVDS1



SN65LVDS2 & SN65LVDT2
(110 Ω resistor for ‘LVDT only)

9.3 Feature Description

9.3.1 SN65LVDS1 Features

9.3.1.1 Driver Output Voltage and Power-On Reset

The SN65LVDS1 driver operates and meets all the specified performance requirements for supply voltages in the range of 2.6 V to 3.6 V. When the supply voltage drops below 1.5 V (or is turning on and has not yet reached 1.5 V), power-on reset circuitry set the driver output to a high-impedance state.

9.3.1.2 Driver Offset

An LVDS-compliant driver is required to maintain the common-mode output voltage at 1.2 V (±75 mV). The SN65LVDS1 incorporates sense circuitry and a control loop to source common-mode current and keep the output signal within specified values. Further, the device maintains the output common-mode voltage at this set point over the full 2.6-V to 3.6-V supply range.

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Feature Description (continued)

9.3.1.3 5-V Input Tolerance

5-V and 3.3-V TTL logic standards share the same input high-voltage and input low-voltage thresholds, namely 2.0 V and 0.8 V, respectively. Although the maximum supply voltage for the SN65LVDS1 is 3.6 V, the driver can operate and meet all performance requirements when the input signals are as high as 5 V. This allows operation with 3.3-V TTL as well as 5-V TTL logic. 3.3-V CMOS and 5-V CMOS inputs are also allowable, although one should ensure that the duty-cycle distortion that will result from the TTL (ground-referenced) thresholds are acceptable.

9.3.1.4 NC Pins

NC (not connected) pins are pins where the die is not physically connected to the lead frame or package. For optimum thermal performance, a good rule of thumb is to ground the NC pins at the board level.

9.3.1.5 Driver Equivalent Schematics

The SN65LVDS1 equivalent input and output schematic diagrams are shown in Figure 15. The driver input is represented by a CMOS inverter stage with a 7-V Zener diode. The input stage is high-impedance, and includes an internal pulldown to ground. If the driver input is left open, the driver input provides a low-level signal to the rest of the driver circuitry, resulting in a low-level signal at the driver output pins. The Zener diode provides ESD protection. The driver output stage is a differential pair, one half of which is shown in Figure 15. Like the input stage, the driver output includes a Zener diode for ESD protection. The schematic shows an output stage that includes a set of current sources (nominally 3.5 mA) that are connected to the output load circuit based upon the input stage signal. To the first order, the SN65LVDS2 output stage acts a constant-current source.

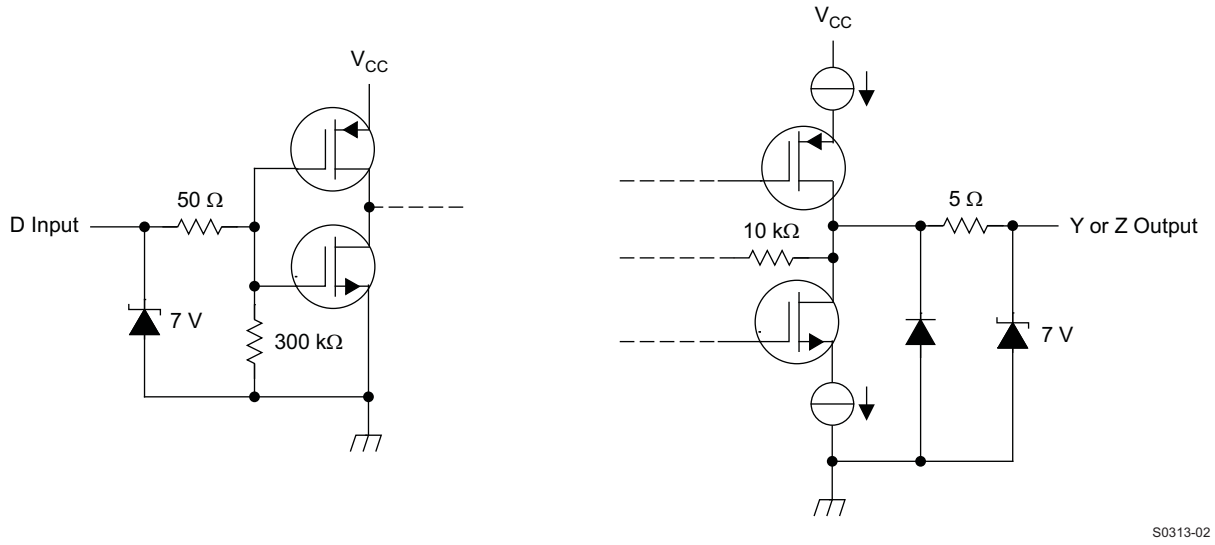


Figure 15. Driver Equivalent Input and Output Schematic Diagrams

9.3.2 SN65LVDS2 and SN65LVDT2 Features

9.3.2.1 Receiver Open Circuit Fail-Safe

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers in that its output logic state can be indeterminate when the differential input voltage is between –100 mV and 100 mV and within its recommended input common-mode voltage range. However, the TI LVDS receiver is different in how it handles the open-input circuit situation.

Open circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver pulls each line of the signal to V_{CC} through 300-kΩ resistors as shown in Figure 16. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high level.

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Feature Description (continued)

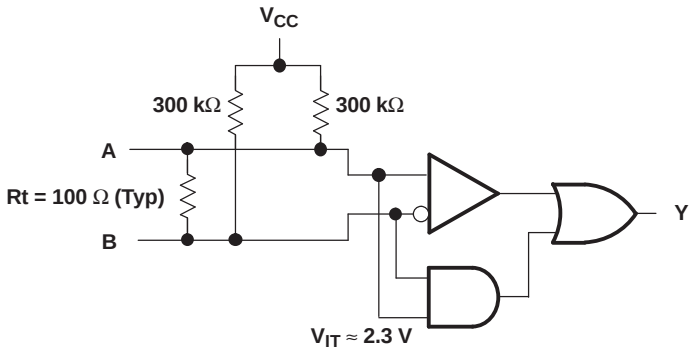


Figure 16. Open-Circuit Fail-Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver is valid with less than a 100-mV differential input voltage magnitude. The presence of the termination resistor, Rt does not affect the fail-safe function as long as it is connected as shown in Figure 16. Other termination circuits may allow a dc-current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

9.3.2.2 Receiver Output Voltage and Power-On Reset

The receiver high level outputs are a function of the device supply voltage. Both receivers support supply voltages in the range of 2.6 V to 3.6 V. The receiver high level output voltage has a minimum output voltage of 2.4 V (TTL logic compliant), when the supply voltage is above 3 V. For supply voltages in the range of 2.6 V to 3.0 V, the receiver high level has a minimum output voltage of 1.9 V. The SN65LVDS2 and the SN65LVDT2 receivers include power-on reset circuitry similar to the SN65LVDS1 circuitry. When the supply voltage drops below 1.5 V (or is turning on and has not yet reached 1.5 V), power-on reset circuitry sets the receiver input and output pins to a high-impedance state.

9.3.2.3 Common-Mode Range vs Supply Voltage

The input common-mode range over which the receivers meet all requirements is a function of the supply voltage as well. For all supply voltages, the valid input signal is from ground to 0.8 V below the supply rail. Hence, if the device is operating with a 3.3 V supply, and a minimum differential voltage of 100 mV, common-mode values in the range of 0.05 V to 2.45 V are supported. If the supply rail is set to 2.5 V, the common-mode range is limited to 0.05 V to 1.65 V.

9.3.2.4 General Purpose Comparator

While the SN65LVDS2 and SN65LVDT2 are LVDS standard-compliant receivers, their utility and applications extend to a wider range of signals. As long as the input signals are within the required differential and common-mode voltage ranges mentioned above, the receiver output will be a faithful representation of the input signal.

9.3.2.5 Receiver Equivalent Schematics

The SN65LVDS2 and SN65LVDT2 equivalent input and output schematic diagrams are shown in Figure 17. The receiver input is a high-impedance differential pair in the case of the SN65LVDS2. The SN65LVDT2 includes an internal termination resistor of 110 Ω across the input port. 7-V Zener diodes are included on each input to provide ESD protection. The receiver output structure shown is a CMOS inverter with an additional Zener diode, again for ESD protection.

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Feature Description (continued)

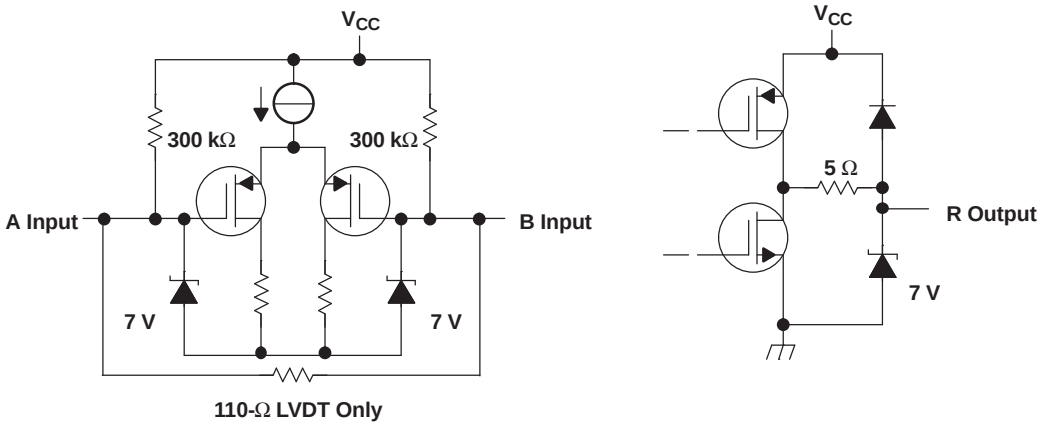


Figure 17. Receiver Equivalent Input and Output Schematic Diagrams

9.3.2.6 NC Pins

NC (not connected) pins are pins where the die is not physically connected to the lead frame or package. For optimum thermal performance, a good rule of thumb is to ground the NC pins at the board level.

9.4 Device Functional Modes

9.4.1 Operation With V_{CC} < 1.5 V

When the SN65LVDS1 is operated with its supply voltage less than 1.5 V, the driver output pins are high-impedance. When the SN65LVDS2 or the SN65LVDT2 is operated with its supply voltage less than 1.5 V, both the receiver input and the receiver output pins are high-impedance.

9.4.2 Operation With 1.5 V ≤ V_{CC} < 2.4 V

Operation with supply voltages in the range of 1.5 V ≤ V_{CC} < 2.4 V is undefined, and no specific device performance is guaranteed in this range.

9.4.3 Operation With 2.4 V ≤ V_{CC} < 3.6 V

Operation with the supply voltages greater than or equal to 2.4 and less than or equal to 3.6 V is normal operation. Some device specifications apply across the full supply range of 2.4 V ≤ V_{CC} ≤ 3.6 V, while some specifications are dependent upon the supply voltage. These dependencies are clearly described in the parametric tables above, as well as shown in the *Typical Characteristics* section.

9.4.4 SN65LVDS1 Truth Table

As can be seen from the truth table, when the driver input is left open, the differential output will be driven low.

Table 1. Driver Function(1)

INPUT	OUTPUTS	
D	Y	Z
H	H	L
L	L	H
Open	L	H

(1) H = High level, L = low level, ? = indeterminate

Table 2. Receiver Function(1)

INPUTS	OUTPUT
$V_{ID} = V_A - V_B$	R
$V_{ID} \geq 100$ mV	H
-100 mV $< V_{ID} < 100$ mV	?
$V_{ID} \leq -100$ mV	L
Open	H

(1) H = High level, L = low level, ? = indeterminate

9.4.5 SN65LVDS2 and SN65LVDT2 Truth Table

As can be seen from the truth table, when the receiver differential input signal is greater than 100 mV, the receiver output is high, and when the differential input voltage is below –100 mV, the receiver output is low. When the input voltage is between these thresholds (that is, between –100 mV and 100 mV), the receiver output is indeterminate. It may be high or low. A special case occurs when the input to the receiver is open-circuited.

Table 3. Driver Function(1)

INPUT	OUTPUTS	
D	Y	Z
H	H	L
L	L	H
Open	L	H

(1) H = High level, L = low level, ? = indeterminate

Table 4. Receiver Function(1)

INPUTS	OUTPUT
$V_{ID} = V_A - V_B$	R
$V_{ID} \geq 100$ mV	H
-100 mV $< V_{ID} < 100$ mV	?
$V_{ID} \leq -100$ mV	L
Open	H

(1) H = High level, L = low level, ? = indeterminate

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN65LVDS1, SN65LVDS2, and SN65LVDT2 devices are single-channel LVDS buffers. The functionality of these devices is simple, yet extremely flexible, leading to their use in designs ranging from wireless base stations to desktop computers. The varied class of potential applications share features and applications discussed in the paragraphs below.

10.2 Typical Applications

10.2.1 Point-to-Point Communications

The most basic application for LVDS buffers, as found in this data sheet, is for point-to-point communications of digital data, as shown in Figure 18.

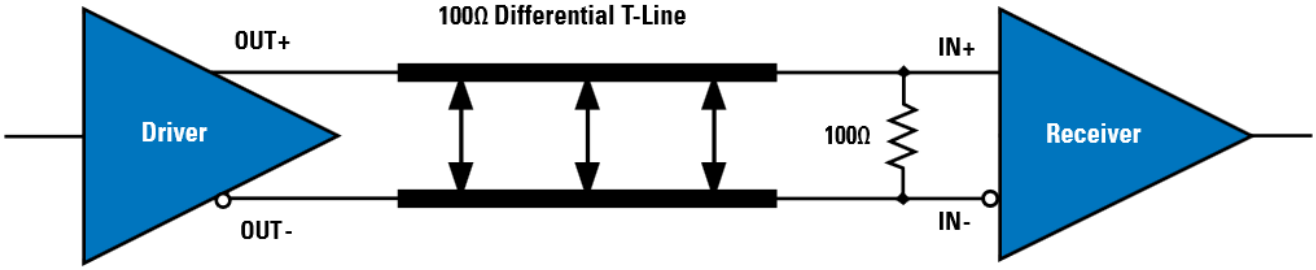


Figure 18. Point-to-Point Topology

A point-to-point communications channel has a single transmitter (driver) and a single receiver. This communications topology is often referred to as simplex. In Figure 18 the driver receives a single-ended input signal and the receiver outputs a single-ended recovered signal. The LVDS driver converts the single-ended input to a differential signal for transmission over a balanced interconnecting media of 100-Ω characteristic impedance. The conversion from a single-ended signal to an LVDS signal retains the digital data payload while translating to a signal whose features are more appropriate for communication over extended distances or in a noisy environment.

10.2.1.1 Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
Driver Supply Voltage (V_{CCD})	2.4 to 3.6 V
Driver Input Voltage	0.8 to 5.0 V
Driver Signaling Rate	DC to 400 Mbps
Interconnect Characteristic Impedance	100 Ω
Termination Resistance	100 Ω
Number of Receiver Nodes	1
Receiver Supply Voltage (V_{CCR})	2.4 to 3.6 V
Receiver Input Voltage	0 to V_{CCR} – 0.8 V
Receiver Signaling Rate	DC to 400 Mbps
Ground shift between driver and receiver	±1 V

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10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Driver Supply Voltage

The SN65LVDS1 driver is operated from a single supply. The device can support operation with a supply as low as 2.4 V and as high as 3.6 V. The driver output voltage is dependent upon the chosen supply voltage. As shown in *Driver Electrical Characteristics*, the differential output voltage is nominally 350 mV over the complete output range. The minimum output voltage stays within the specified LVDS limits (247 mV to 454 mV) for a 3.3-V supply. If the supply range is between 2.4 V and 3 V, the minimum output voltage may be as low as 200 mV. If a communication link is designed to operate with a supply within this lower range, the channel noise margin will need to be looked at carefully to ensure error-free operation.

10.2.1.2.2 Driver Bypass Capacitance

Bypass capacitors play a key role in power distribution circuitry. Specifically, they create low-impedance paths between power and ground. At low frequencies, a good digital power supply offers very low-impedance paths between its terminals. However, as higher frequency currents propagate through power traces, the source is quite often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10 µF to 1000 µF) at the board-level do a good job up into the kHz range. Due to their size and length of their leads, they tend to have large inductance values at the switching frequencies of modern digital circuitry. To solve this problem, one must resort to the use of smaller capacitors (nF to µF range) installed locally next to the integrated circuit.

Multilayer ceramic chip or surface-mount capacitors (size 0603 or 0805) minimize lead inductances of bypass capacitors in high-speed environments, because their lead inductance is about 1 nH. For comparison purposes, a typical capacitor with leads has a lead inductance around 5 nH.

The value of the bypass capacitors used locally with LVDS chips can be determined by the following formula according to Johnson, equations 8.18 to 8.21. A conservative rise time of 200 ps and a worst-case change in supply current of 1 A covers the whole range of LVDS devices offered by Texas Instruments. In this example, the maximum power supply noise tolerated is 200 mV; however, this figure varies depending on the noise budget available in your design. (1)

$$C_{chip} = \left(\frac{\Delta I_{\text{Maximum Step Change Supply Current}}}{\Delta V_{\text{Maximum Power Supply Noise}}} \right) \times T_{\text{Rise Time}} \quad (1)$$

$$C_{LVDS} = \left(\frac{1A}{0.2V} \right) \times 200\ \text{ps} = 0.001\,\mu\text{F} \quad (2)$$

The following example lowers lead inductance and covers intermediate frequencies between the board-level capacitor (>10 µF) and the value of capacitance found above (0.001 µF). You should place the smallest value of capacitance as close as possible to the chip.

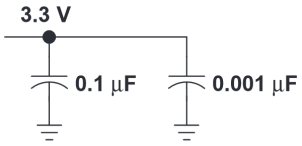


Figure 19. Recommended LVDS Bypass Capacitor Layout

(1) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.

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10.2.1.2.3 Driver Input Voltage

The SN65LVDS1 input is designed to support a wide input voltage range. The input stage can accept signals as high as 5 V, independent of the supply voltage being used on the driver. This wide input range allows operation with 3.3-V and 5-V sources. While the input stage does support this wide input range, the driver will operate with a decision threshold of ~1.4 V. For LVTTL input signals, this threshold is well-matched to the voltages representing HI and LO logic levels. For 5-V TTL input signals and CMOS input signals, this fixed threshold at 1.4 V will result in some duty-cycle distortion. The level of the distortion is easily calculated based upon the input slew rate, as well as the signaling rate of the input data. Quite often this distortion is insignificant, although the designer should consider this effect where the device is operated at higher speeds, or when duty-cycle is a critical feature.

10.2.1.2.4 Driver Output Voltage

The SN65LVDS1 driver output is a 1.2-V common-mode voltage, with a nominal differential output signal of 350 mV. This 350 mV is the absolute value of the differential swing (V_{OD} = $|V^+ – V^–|$). The peak-to-peak differential voltage is twice this value, or 700 mV. As mentioned previously, the minimum differential output voltage is 200 mV when the supply voltage is between 2.4 V and 3 V. While 200 mV does not meet the minimum specified voltage for an LVDS-compliant driver, the designer may choose to employ this driver with a lower supply voltage, as long as attention is paid to the channel noise margin.

As we will see shortly, LVDS receiver thresholds are ±100 mV. With these receiver decision thresholds, it is clear that the disadvantage of operating the driver with a lower supply will be noise margin. With fully compliant LVDS drivers and receivers, we would expect a minimum of ~150 mV of noise margin (247-mV minimum output voltage – 100-mV maximum input requirement). If we operate the SN65LVDS1 with a supply in the range of 2.4 V to 3 V, the minimum noise margin will drop to 100 mV (200 mV – 100 mV).

10.2.1.2.5 Interconnecting Media

The physical communication channel between the driver and the receiver may be any balanced paired metal conductors meeting the requirements of the LVDS standard, the key points which will be included here. This media may be a twisted pair, twinax, flat ribbon cable, or PCB traces.

The nominal characteristic impedance of the interconnect should be between 100 Ω and 120 Ω with variation no more than 10% (90 Ω to 132 Ω).

10.2.1.2.6 PCB Transmission Lines

As per SNLA187, Figure 20 depicts several transmission line structures commonly used in printed-circuit boards (PCBs). Each structure consists of a signal line and a return path with uniform cross-section along its length. A microstrip is a signal trace on the top (or bottom) layer, separated by a dielectric layer from its return path in a ground or power plane. A stripline is a signal trace in the inner layer, with a dielectric layer in between a ground plane above and below the signal trace. The dimensions of the structure along with the dielectric material properties determine the characteristic impedance of the transmission line (also called controlled-impedance transmission line).

When two signal lines are placed close by, they form a pair of coupled transmission lines. Figure 20 shows examples of edge-coupled microstrips, and edge-coupled or broad-side-coupled striplines. When excited by differential signals, the coupled transmission line is referred to as a differential pair. The characteristic impedance of each line is called odd-mode impedance. The sum of the odd-mode impedances of each line is the differential impedance of the differential pair. In addition to the trace dimensions and dielectric material properties, the spacing between the two traces determines the mutual coupling and impacts the differential impedance. When the two lines are immediately adjacent; for example, S is less than 2W, the differential pair is called a tightly-coupled differential pair. To maintain constant differential impedance along the length, it is important to keep the trace width and spacing uniform along the length, as well as maintain good symmetry between the two lines.

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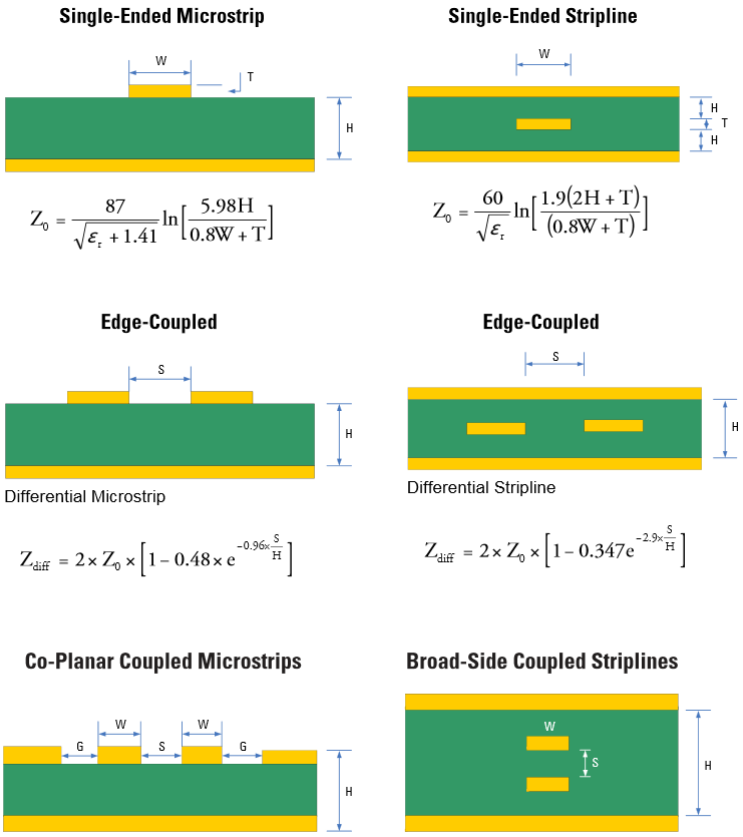


Figure 20. Controlled-Impedance Transmission Lines

10.2.1.2.7 Termination Resistor

As shown earlier, an LVDS communication channel employs a current source driving a transmission line which is terminated with a resistive load. This load serves to convert the transmitted current into a voltage at the receiver input. To ensure incident wave switching (which is necessary to operate the channel at the highest signaling rate), the termination resistance should be matched to the characteristic impedance of the transmission line. The designer should ensure that the termination resistance is within 10% of the nominal media characteristic impedance. If the transmission line is targeted for 100-Ω impedance, the termination resistance should be between 90 Ω and 110 Ω.

The line termination resistance should be located as close as possible to the receiver, thereby minimizing the stub length from the resistor to the receiver. The limiting case would be to incorporate the termination resistor into the receiver, which is exactly what is offered with the SN65LVDT2. The SN65LVDT2 provides all the functionality and performance of the SN65LVDS2 receiver, with the added feature of an integrated termination load.

While we talk in this section about point-to-point communications, a word of caution is useful when a multidrop topology is used. In such topologies, line termination resistors are to be located only at the end(s) of the transmission line. In such an environment, SN65LVDS2 receivers could be used for loads branching off the main bus, with an SN65LVDT2 used only at the bus end.

10.2.1.2.8 Driver NC Pins

NC (not connected) pins are pins where the die is not physically connected to the lead frame or package. For optimum thermal performance, a good rule of thumb is to ground the NC pins at the board level.

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10.2.1.2.9 Receiver Supply Voltage

The SN65LVDS2 and SN65LVDT2 receivers are operated from a single supply. Like the SN65LVDS1, these devices can support operation with a supply as low as 2.4 V and as high as 3.6 V. The main effects of low supply voltage for these LVDS receivers will be seen in the receiver input common-mode range and the receiver output voltage. We will address these in turn below.

10.2.1.2.10 Receiver Bypass Capacitance

Bypass capacitors recommendations have been discussed above in *Driver Bypass Capacitance*.

10.2.1.2.11 Receiver Input Common-Mode Range

The SN65LVDS2 and SN65LVDT2 support operation over an input common-mode range that is dependent upon the device supply voltage. Per the recommended conditions table, we see that operation is supported between 0 V and 0.8 V below the supply rail.

For a supply voltage of 3.3 V, operation is available when the input common-mode voltage is between GND and 2.5 V. The receivers are required to meet sensitivity requirements over the whole common-mode input range.

If we return to the transmitter discussions, we recall that the SN65LVDS1 has an output common-mode range of 1.2 V. Using one of the receivers discussed here, we see that valid operation of the communication link will occur when the ground difference between transmitter and receiver is within ~±1 V . The use of differential signaling in LVDS allows operation in an environment where the combination of ground difference and common-mode noise result in a common-mode difference between transmitter and receiver of 1 V. This 1-V potential difference hints at the intended application of LVDS circuits.

Standards such as RS-485 support potential differences of almost 10 V, allowing for communication over distances of greater than 1 km. The intended applications of LVDS devices is more moderate distances, such as those from chip to chip on a board, board to board in a rack, or from rack to nearby rack. When the 1-V potential difference is not adequate, yet the high-speed and low voltage features of LVDS are still needed, the designer can choose from either M-LVDS devices available from TI, or from LVDS devices with extended common-mode ranges, such as the SN65LVDS33.

10.2.1.2.12 Receiver Input Signal

The LVDS receivers herein comply with the LVDS standard and correctly determine the bus state when the differential input voltage is greater than 100 mV (HI output) or less than –100 mV (LO output). In addition, the receivers operate with differential input voltages of up to 600 mV.

10.2.1.2.13 Receiver Output Signal

Receiver outputs comply with LVTTL output voltage standards when the supply voltage is within the range of 3 V to 3.6 V. When the supply voltage is within the lower range of 2.4 V to 3 V, the high output voltage can be as low as 1.9 V. If a design intends to operate the receivers with a supply voltage in this lower range, care should be taken to ensure that the device being driven by these devices will be able to operate without errors with the lower output voltage.

10.2.1.2.14 Receiver NC Pins

NC (not connected) pins are pins where the die is not physically connected to the lead frame or package. For optimum thermal performance, a good rule of thumb is to ground the NC pins at the board level.

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10.2.2 Application Curve

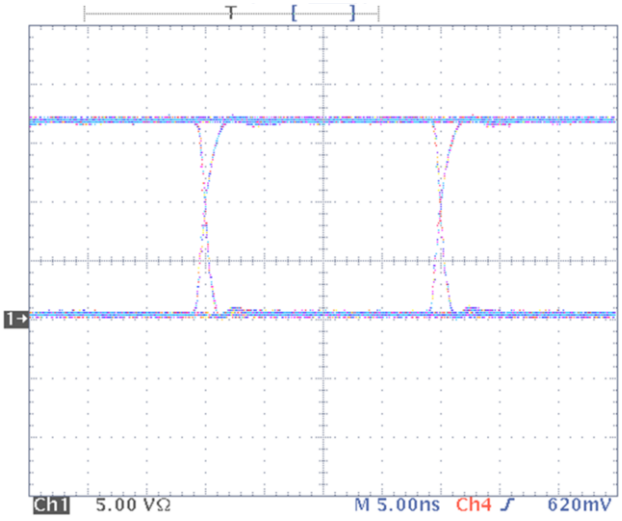


Figure 21. Typical Driver Output Eye Pattern in Point-to-Point System

10.2.3 Multidrop Communications

A second common application of LVDS buffers is a multidrop topology. In a multidrop configuration, a single driver and a shared bus are present, along with two or more receivers (with a maximum permissible number of 32 receivers). Figure 22 below shows an example of a multidrop system.

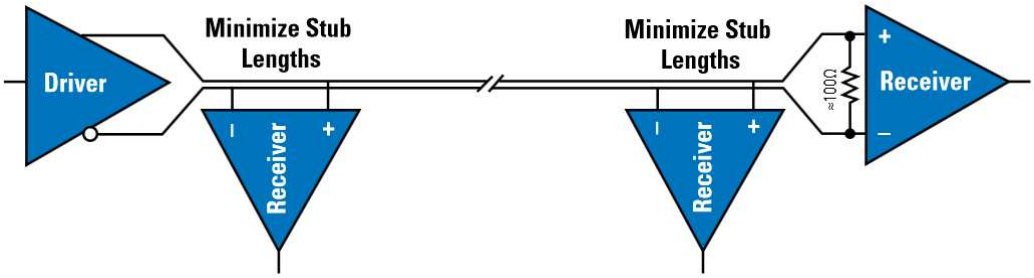


Figure 22. Multidrop Topology

10.2.3.1 Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
Driver Supply Voltage (V_{CCD})	2.4 to 3.6 V
Driver Input Voltage	0.8 to 5.0 V
Driver Signaling Rate	DC to 400 Mbps
Interconnect Characteristic Impedance	100 Ω
Termination Resistance	100 Ω
Number of Receiver Nodes	2 to 32
Receiver Supply Voltage (V_{CCR})	2.4 to 3.6 V
Receiver Input Voltage	0 to V_{CCR} – 0.8 V
Receiver Signaling Rate	DC to 400 Mbps
Ground shift between driver and receiver	±1 V

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10.2.3.2 Detailed Design Procedure

10.2.3.2.1 Interconnecting Media

The interconnect in a multidrop system differs considerably from a point-to-point system. While point-to-point interconnects are straightforward, and well understood, the bus type architecture encountered with multidrop systems requires more careful attention. We will use Figure 22 above to explore these details.

The most basic multidrop system would include a single driver, located at a bus origin, with multiple receiver nodes branching off the main line, and a final receiver at the end of the transmission line, co-located with a bus termination resistor. While this would be the most basic multidrop system, it has several considerations not yet explored.

The location of the transmitter at one bus end allows the design concerns to be simplified, but this comes at the cost of flexibility. With a transmitter located at the origin, a single bus termination at the far-end is required. The far-end termination absorbs the incident traveling wave. The flexibility lost with this arrangement is thus: if the single transmitter needed to be relocated on the bus, at any location other than the origin, we would be faced with a bus with one open-circuited end, and one properly terminated end. Locating the transmitter say in the middle of the bus may be desired to reduce (by ½) the maximum flight time from the transmitter to receiver.

Another new feature in Figure 22 is clear in that every node branching off the main line results in stubs. The stubs should be minimized in any case, but have the unintended effect of locally changing the loaded impedance of the bus.

To a good approximation, the characteristic transmission line impedance seen into any cut point in the unloaded multipoint or multidrop bus is defined by $\sqrt{L/C}$, where L is the inductance per unit length and C is the capacitance per unit length. As capacitance is added to the bus in the form of devices and interconnections, the bus characteristic impedance is lowered. This may result in signal reflections from the impedance mismatch between the unloaded and loaded segments of the bus.

If the number of loads is constant and can be distributed evenly along the line, reflections can be reduced by changing the bus termination resistors to match the loaded characteristic impedance. Normally, the number of loads are not constant or distributed evenly and the reflections resulting from any mismatching must be accounted for in the noise budget.

10.2.3.3 Application Curve

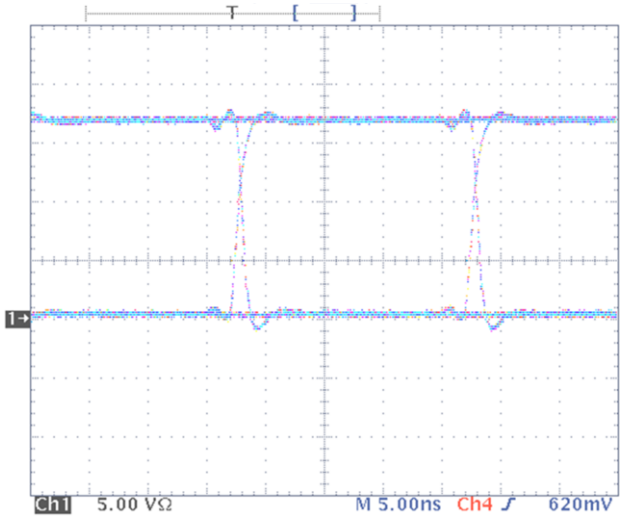


Figure 23. Typical Driver Output Eye Pattern in Multidrop System

11 Power Supply Recommendations

The LVDS driver and receivers in this data sheet are designed to operate from a single power supply. Both drivers and receivers operate with supply voltages in the range of 2.4 V to 3.6 V. In a typical application, a driver and a receiver may be on separate boards, or even separate equipment. In these cases, separate supplies would be used at each location. The expected ground potential difference between the driver power supply and the receiver power supply would be less than |±1 V|. Board level and local device level bypass capacitance should be used and are covered in *Driver Bypass Capacitance* and *Receiver Bypass Capacitance*.

12 Layout

12.1 Layout Guidelines

12.1.1 Microstrip vs. Stripline Topologies

As per SLLD009, printed-circuit boards usually offer designers two transmission line options: Microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in Figure 24.

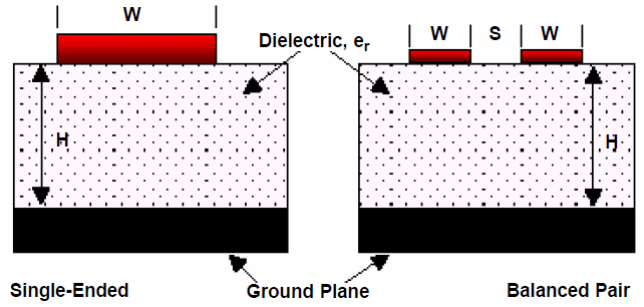


Figure 24. Microstrip Topology

On the other hand, striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems because the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing LVDS signals on microstrip transmission lines, if possible. The PCB traces allow designers to specify the necessary tolerances for Z_O based on the overall noise budget and reflection allowances. Footnotes 1, 2, and 3 provide formulas for Z_O and t_{PD} for differential and single-ended traces. (1) (2) (3)

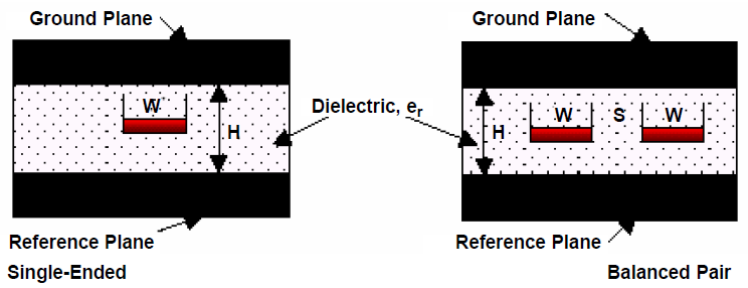


Figure 25. Stripline Topology

(1) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.
(2) Mark I. Montrose. 1996. Printed Circuit Board Design Techniques for EMC Compliance. IEEE Press. ISBN number 0780311310.
(3) Clyde F. Coombs, Jr. Ed, Printed Circuits Handbook, McGraw Hill, ISBN number 0070127549.

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Layout Guidelines (continued)

12.1.2 Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or equivalent, usually provides adequate performance for use with LVDS signals. If rise or fall times of TTL/CMOS signals are less than 500 ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13 is better suited. Once the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving LVDS devices:

- Copper weight: 15 g or 1/2 oz start, plated to 30 g or 1 oz
- All exposed circuitry should be solder-plated (60/40) to 7.62 µm or 0.0003 in (minimum).
- Copper plating should be 25.4 µm or 0.001 in (minimum) in plated-through-holes.
- Solder mask over bare copper with solder hot-air leveling

12.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, you must decide how many levels to use in the stack. To reduce the TTL/CMOS to LVDS crosstalk, it is a good practice to have at least two separate signal planes as shown in Figure 26.

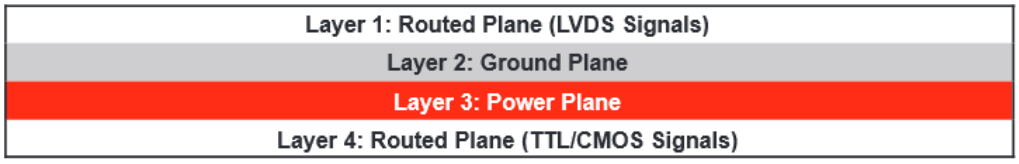


Figure 26. Four-Layer PCB Board

NOTE

The separation between layers 2 and 3 should be 127 µm (0.005 in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

One of the most common stack configurations is the six-layer board, as shown in Figure 27.

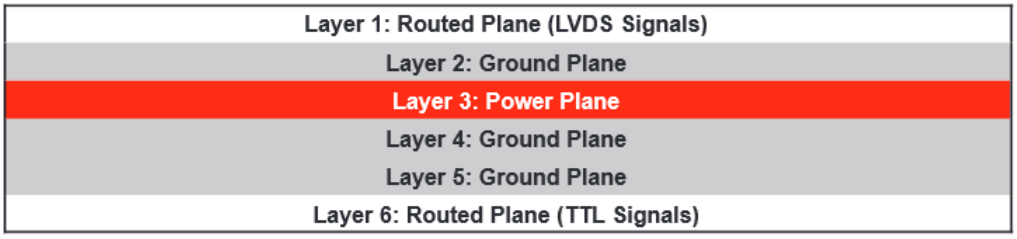


Figure 27. Six-Layer PCB Board

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity; however, fabrication is more expensive. Using the 6-layer board is preferable, because it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes, in addition to ensuring reference to a ground plane for signal layers 1 and 6.

12.1.4 Separation Between Traces

The separation between traces depends on several factors; however, the amount of coupling that can be tolerated usually dictates the actual separation. Low noise coupling requires close coupling between the differential pair of an LVDS link to benefit from the electromagnetic field cancellation. The traces should be 100-Ω differential and thus coupled in the manner that best fits this requirement. In addition, differential pairs should have the same electrical length to ensure that they are balanced, thus minimizing problems with skew and signal reflection.

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Layout Guidelines (continued)

In the case of two adjacent single-ended traces, one should use the 3-W rule, which stipulates that the distance between two traces must be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule should be applied to the separation between adjacent LVDS differential pairs, whether the traces are edge-coupled or broad-side-coupled.

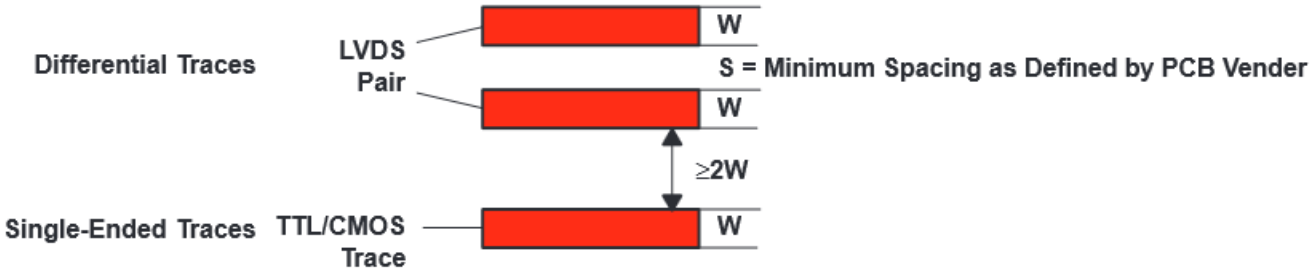


Figure 28. 3-W Rule for Single-Ended and Differential Traces (Top View)

You should exercise caution when using autorouters, because they do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

12.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high-frequency currents that is as close as possible to its originating trace. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and should be avoided.

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Layout Guidelines (continued)

12.1.6 Decoupling

Each power or ground lead of a high-speed device should be connected to the PCB through a low inductance path. For best results, one or more vias are used to connect a power or ground pin to the nearby plane. Ideally, via placement is immediately adjacent to the pin to avoid adding trace inductance. Placing a power plane closer to the top of the board reduces the effective via length and its associated inductance.

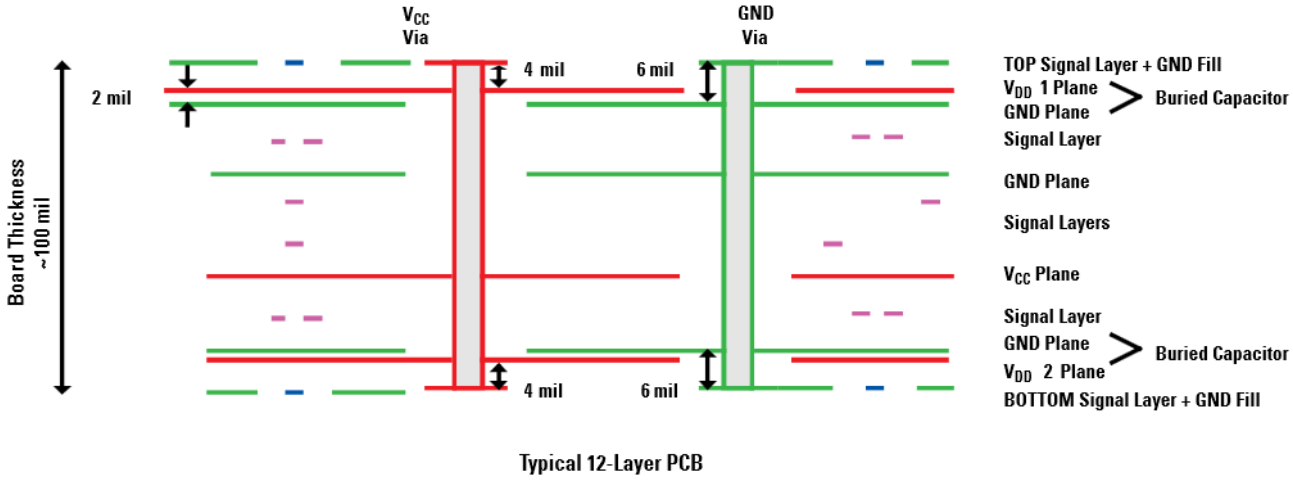


Figure 29. Low Inductance, High-Capacitance Power Connection

Bypass capacitors should be placed close to V_{DD} pins. They can be placed conveniently near the corners or underneath the package to minimize the loop area. This extends the useful frequency range of the added capacitance. Small-physical-size capacitors, such as 0402 or even 0201, or X7R surface-mount capacitors should be used to minimize body inductance of capacitors. Each bypass capacitor is connected to the power and ground plane through vias tangent to the pads of the capacitor as shown in Figure 30(a).

An X7R surface-mount capacitor of size 0402 has about 0.5 nH of body inductance. At frequencies above 30 MHz or so, X7R capacitors behave as low-impedance inductors. To extend the operating frequency range to a few hundred MHz, an array of different capacitor values like 100 pF, 1 nF, 0.03 µF, and 0.1 µF are commonly used in parallel. The most effective bypass capacitor can be built using sandwiched layers of power and ground at a separation of 2 to 3 mils. With a 2-mil FR4 dielectric, there is approximately 500 pF per square inch of PCB. Refer back to Figure 5-1 for some examples. Many high-speed devices provide a low-inductance GND connection on the backside of the package. This center dap must be connected to a ground plane through an array of vias. The via array reduces the effective inductance to ground and enhances the thermal performance of the small Surface Mount Technology (SMT) package. Placing vias around the perimeter of the dap connection ensures proper heat spreading and the lowest possible die temperature. Placing high-performance devices on opposing sides of the PCB using two GND planes (as shown in Figure 20) creates multiple paths for heat transfer. Often thermal PCB issues are the result of one device adding heat to another, resulting in a very high local temperature. Multiple paths for heat transfer minimize this possibility. In many cases the GND dap that is so important for heat dissipation makes the optimal decoupling layout impossible to achieve due to insufficient pad-to-dap spacing as shown in Figure 30(b). When this occurs, placing the decoupling capacitor on the backside of the board keeps the extra inductance to a minimum. It is important to place the V_{DD} via as close to the device pin as possible while still allowing for sufficient solder mask coverage. If the via is left open, solder may flow from the pad and into the via barrel. This will result in a poor solder connection.

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Layout Guidelines (continued)



Figure 30. Typical Decoupling Capacitor Layouts

12.2 Layout Example

At least two or three times the width of an individual trace should separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in Figure 31.

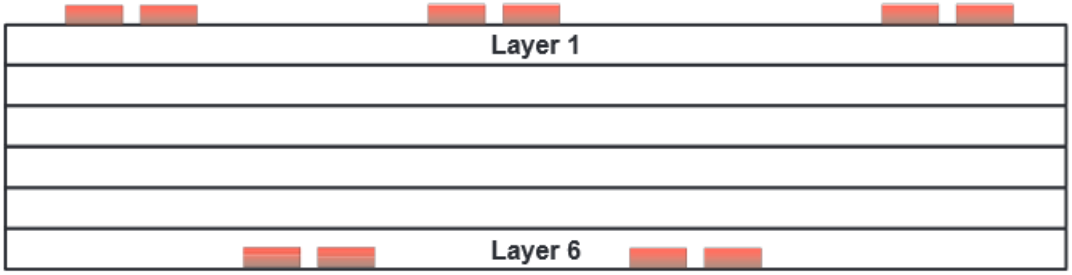


Figure 31. Staggered Trace Layout

This configuration lays out alternating signal traces on different layers; thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in Figure 32. Note that vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 1/2 pF to 1 pF in FR4.

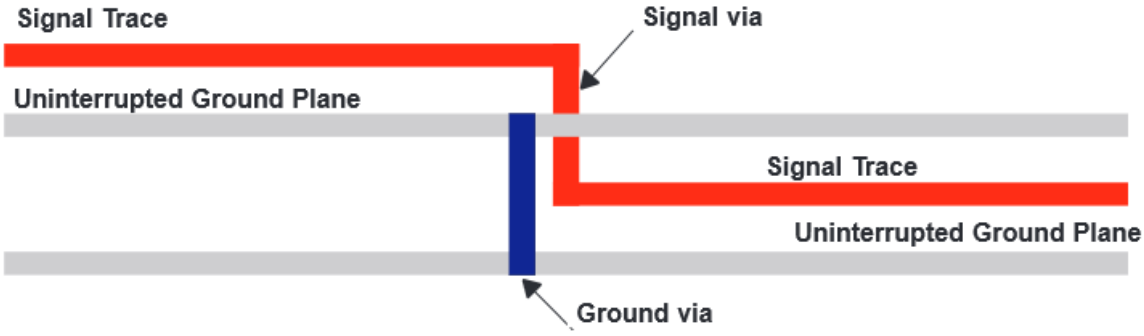


Figure 32. Ground Via Location (Side View)

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Layout Example (continued)

Short and low-impedance connection of the device ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

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13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.1.2 Other LVDS Products

For other products and application notes in the LVDS and LVDM product families visit our Web site at http://www.ti.com/sc/datatran.

13.2 Documentation Support

13.2.1 Related Information

IBIS modeling is available for this device. Contact the local TI sales office or the TI Web site at www.ti.com for more information.

For more application guidelines, see the following documents:

- *IC Package Thermal Metrics* (SPRA953)
- *Control-Impedance Transmission Lines* (SNLA187)
- *Microstrip vs Stripline Topologies* (SLLD009)

13.3 Related Links

Table 5 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65LVDS1	Click here	Click here	Click here	Click here	Click here
SN65LVDS2	Click here	Click here	Click here	Click here	Click here
SN65LVDT2	Click here	Click here	Click here	Click here	Click here

13.4 Trademarks

Rogers is a trademark of Rogers Corporation.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS1D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS1	Samples
SN65LVDS1DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SAAI	Samples
SN65LVDS1DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SAAI	Samples
SN65LVDS1DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SAAI	Samples
SN65LVDS1DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SAAI	Samples
SN65LVDS1DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS1	Samples
SN65LVDS2D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		LVDS2	Samples
SN65LVDS2DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SABI	Samples
SN65LVDS2DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SABI	Samples
SN65LVDS2DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SABI	Samples
SN65LVDS2DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SABI	Samples
SN65LVDS2DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS2	Samples
SN65LVDT2D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		LVDT2	Samples
SN65LVDT2DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SACI	Samples
SN65LVDT2DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SACI	Samples
SN65LVDT2DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SACI	Samples
SN65LVDT2DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SACI	Samples
SN65LVDT2DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		LVDT2	Samples
SN65LVDT2DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT2	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

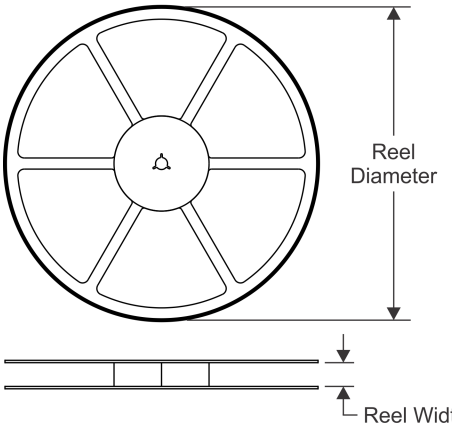
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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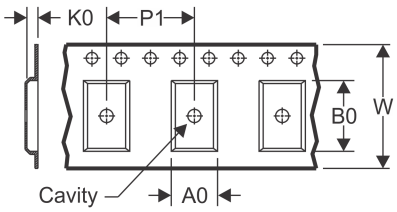
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

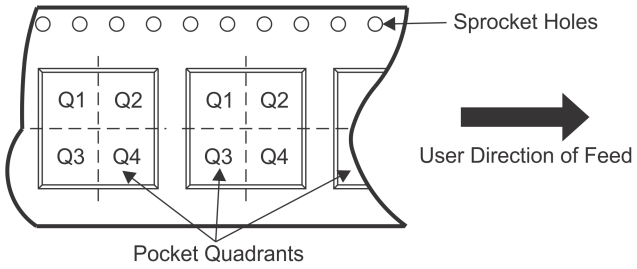


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

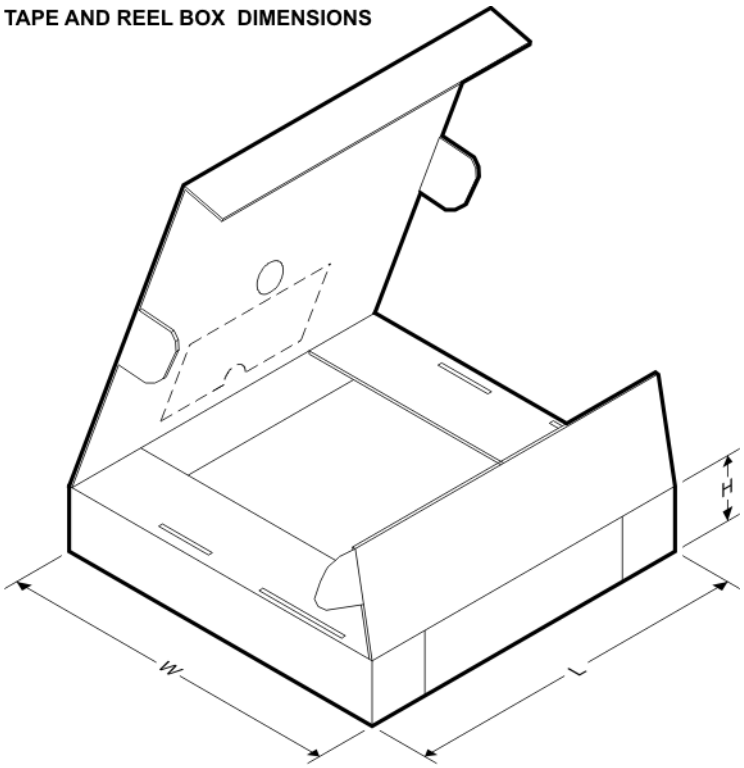
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS1DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN65LVDS1DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN65LVDS1DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LVDS2DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN65LVDS2DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN65LVDS2DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LVDT2DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
SN65LVDT2DBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
SN65LVDT2DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

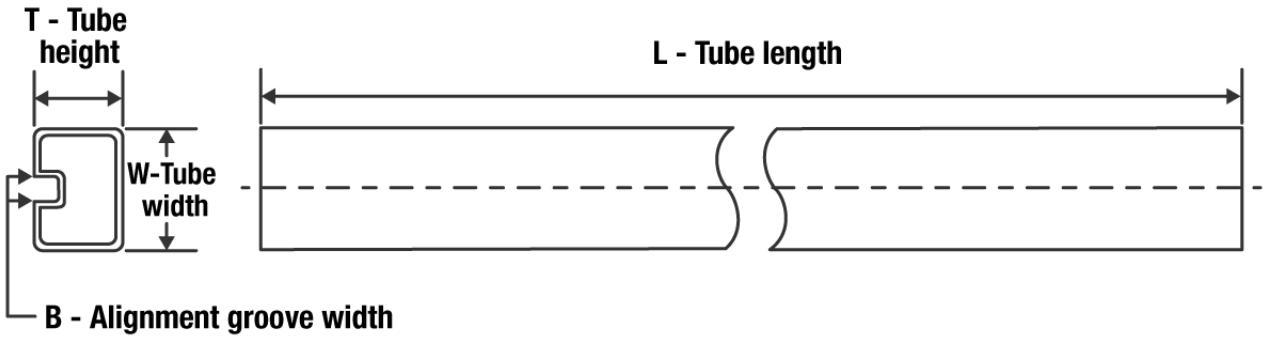
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

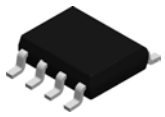
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS1DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN65LVDS1DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN65LVDS1DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65LVDS2DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN65LVDS2DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN65LVDS2DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65LVDT2DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
SN65LVDT2DBVT	SOT-23	DBV	5	250	182.0	182.0	20.0
SN65LVDT2DR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LVDS1D	D	SOIC	8	75	507	8	3940	4.32
SN65LVDS2D	D	SOIC	8	75	507	8	3940	4.32
SN65LVDT2D	D	SOIC	8	75	507	8	3940	4.32
SN65LVDT2DG4	D	SOIC	8	75	507	8	3940	4.32

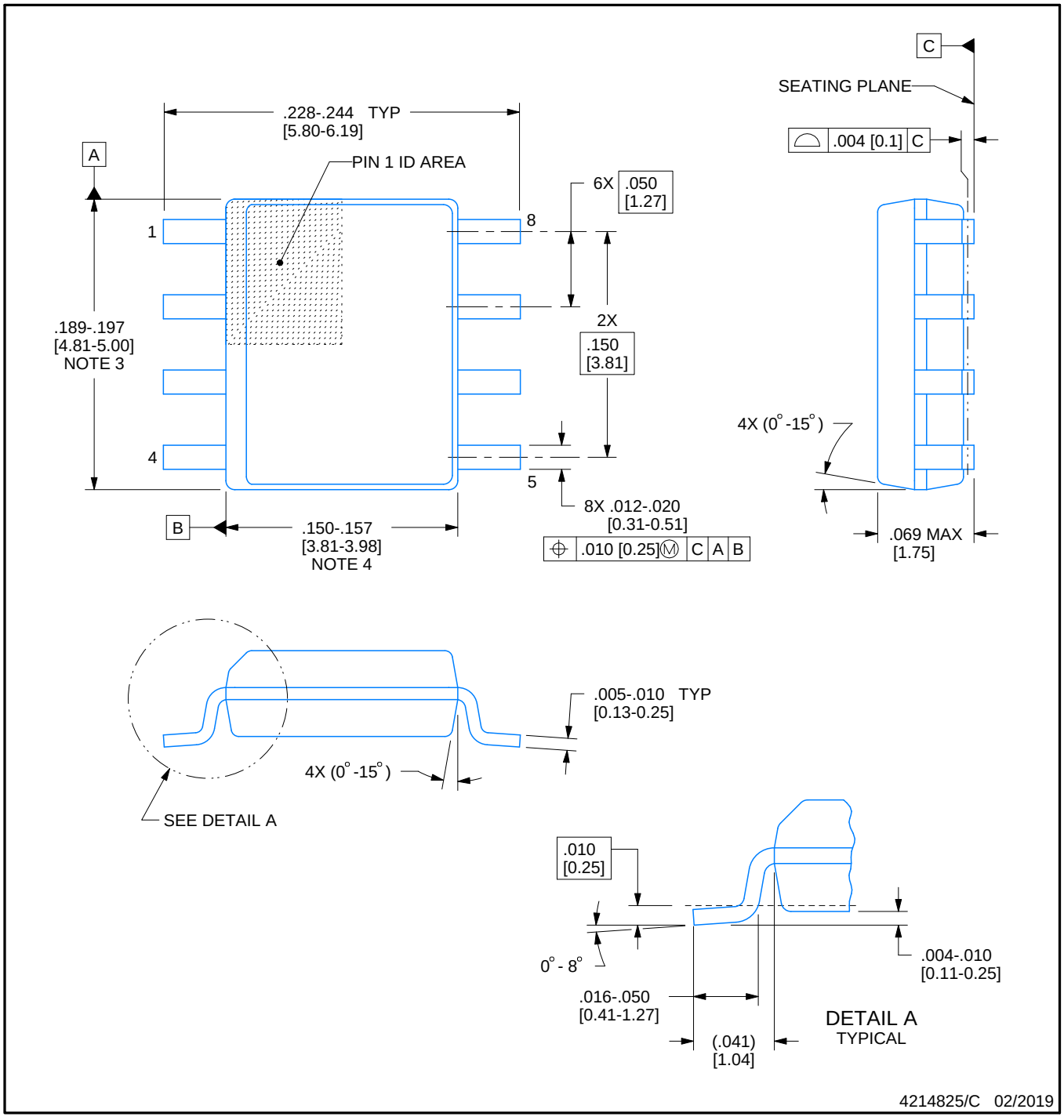


PACKAGE OUTLINE

D0008A

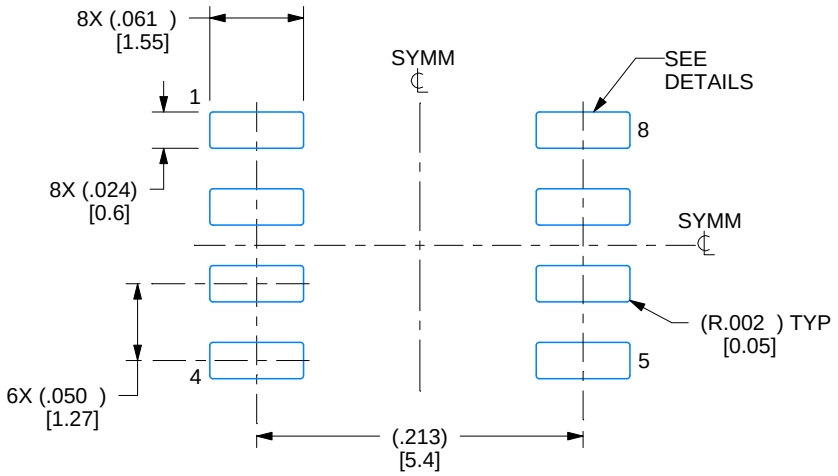
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

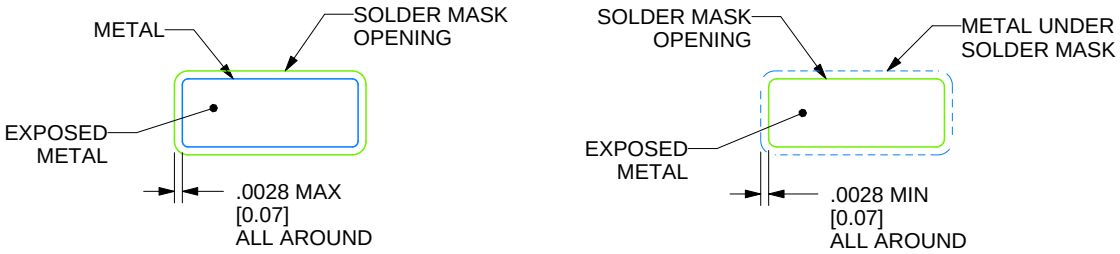


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

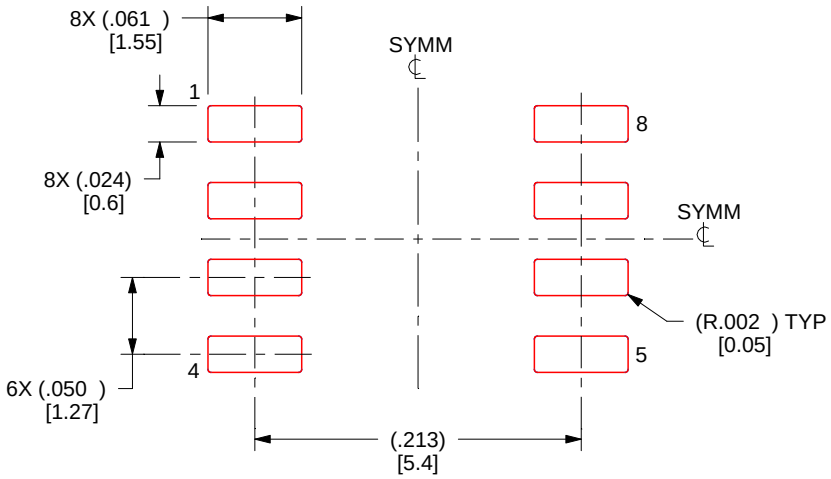
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

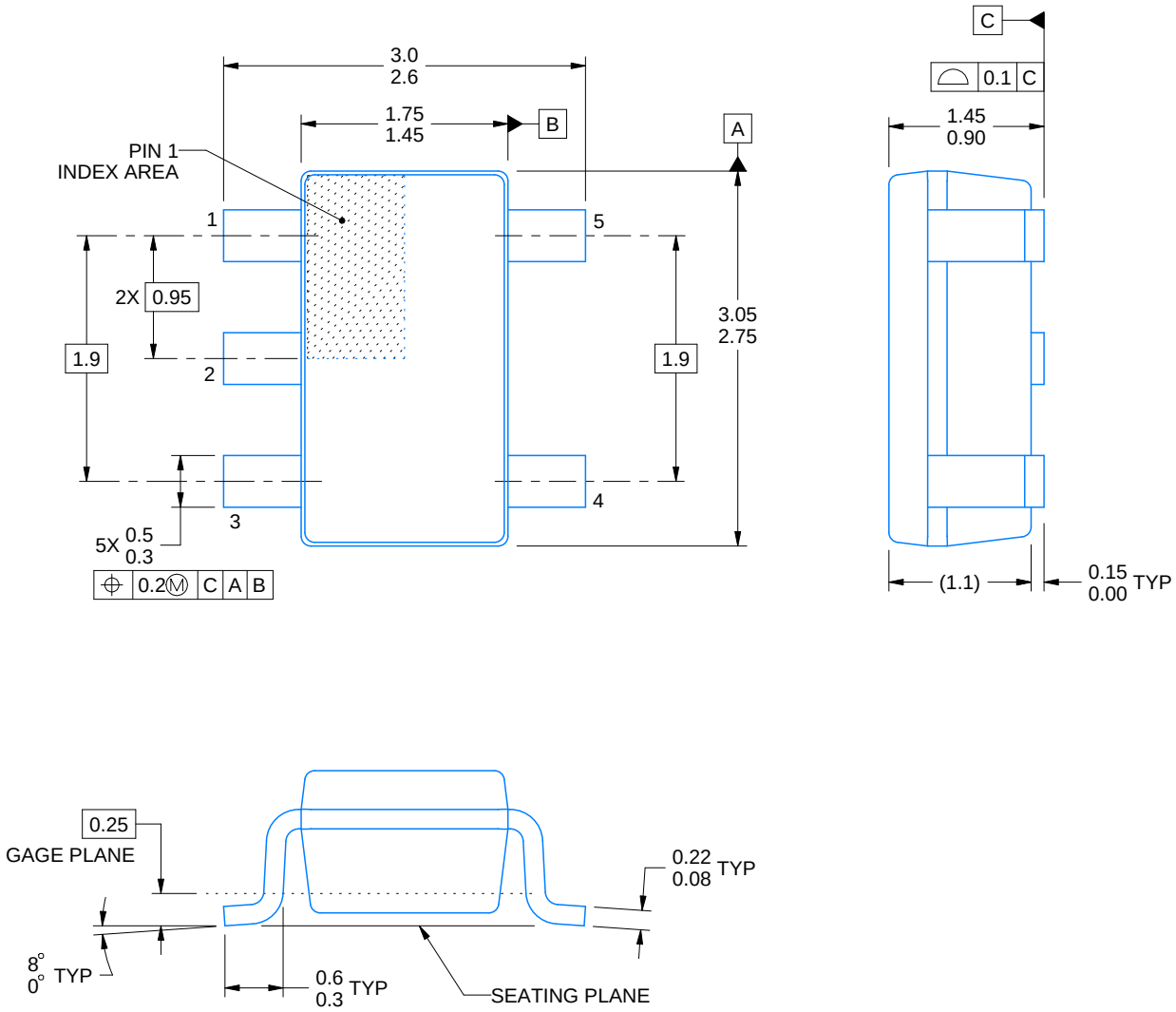
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

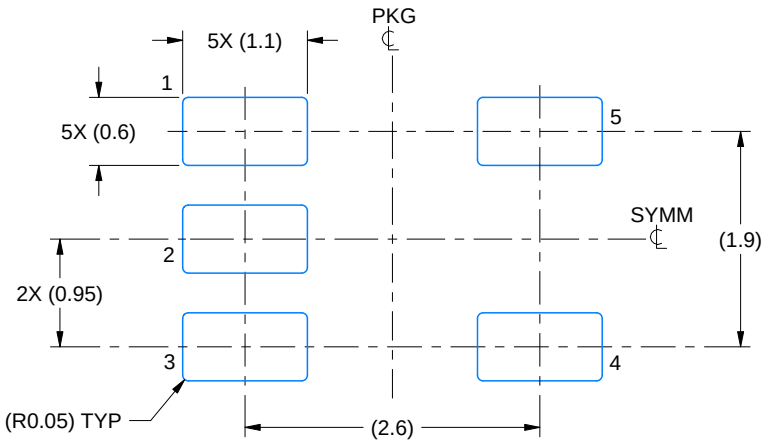
SMALL OUTLINE TRANSISTOR



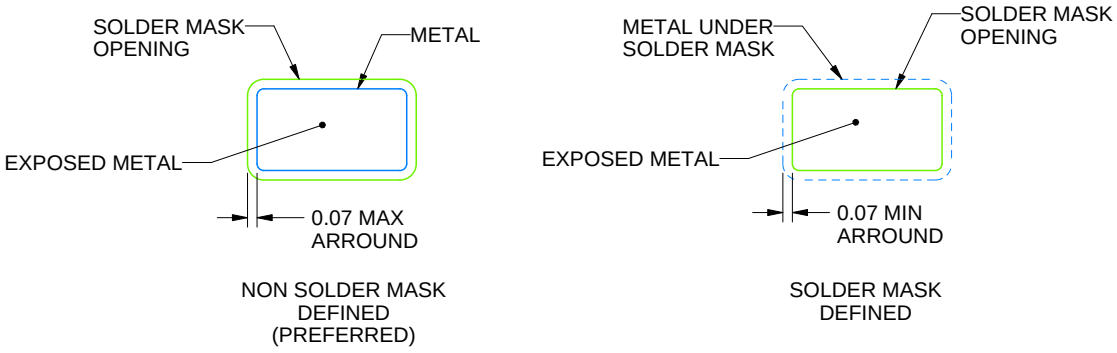
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

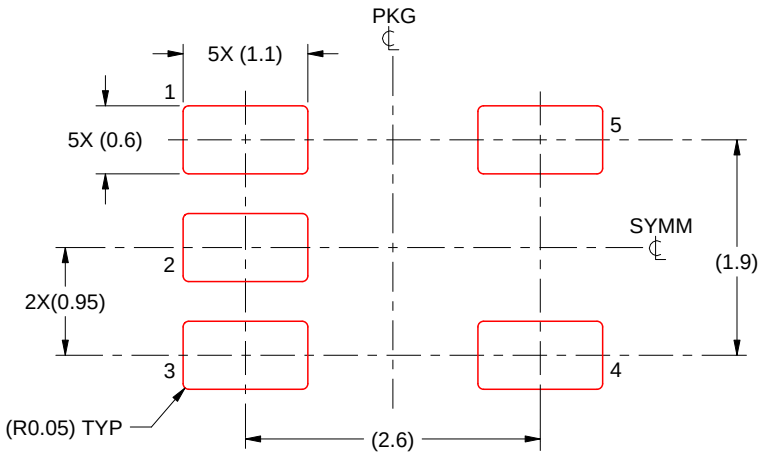


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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