TPIC2040 用于 ODD 驱动、由串行接口控制的 7 通道电机驱动器

1 特性

- 串行外设接口 (SPI)
  - 最大读写频率 35MHz
  - 3.3V 数字输入输出 (I/O)
- 执行器和电机驱动器
  - 具有 H 桥输出的脉冲宽度调制 (PWM) 控制
  - 具有 12 位数模转换器 (DAC) 控制的聚焦/跟踪/倾斜执行器驱动器
  - 具有电流模式、10 位 DAC 控制的滑动电机驱动器
  - 具有 12 位 DAC 控制的负载驱动器
  - 无需位置传感器即可检测滑动结束位置
- 主轴电机驱动器
  - 集成主轴电流感测电阻
  - 可通过设置寄存器来选择 0.20Ω 至 0.27Ω 的电流感测电阻值，从而将 SPM 电流限制在 725mA 至 980mA
  - 无传感器：通过电机反电动势 (BEMF) 感测转子位置
  - 通过串行端口编程 12 位主轴 DAC
  - 独立的感应位置感测和启动
  - 通过名为自动短制动的自动控制制动实现急停（短制动和主动制动）
  - 最大持续电流为 0.7A，不存在散热问题
  - 低速 (LS) 模式：限制在正常速度的 25%
- 实用功能
  - XRESET 信号，具有 20ms 数字延时（上电复位 (POR)）
  - 状态锁存器：执行器定时器、SIF 错误、电源监视器、热保护和过流保护 (OCP) 故障
- 开关
  - CSW：软件控制电流输出端口
- 低压降 (LDO) 前置驱动器
  - 具有外部晶体管的 3.3V 或 1.2V 电压输出的单通道 LDO 前置驱动器
- 保护
  - CSW、SPM 和执行器通道上均配有独立热保护电路
  - 两个警报级别：热保护中的*预检测*和*检测*
  - 负载驱动器中配有过流保护电路
  - CSW 输出具有可选 OCP 阈值电平
  - 硬件器件禁用引脚 XMUTE
  - 具有欠压闭锁 (UVLO) 和 过压保护 (OVP) 的电源监视器

2 应用

- DVD 播放器
- CD 播放器
- 光盘驱动器

3 说明

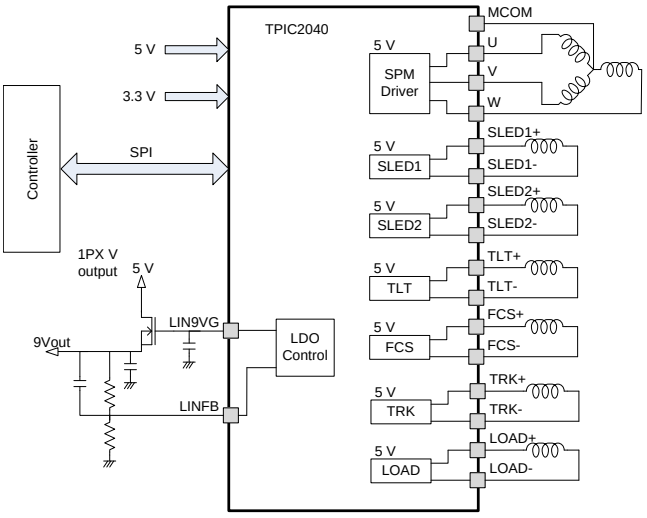
TPIC2040 是一款适用于薄型或超薄 DVD 读/写器的超低噪声电机驱动器集成电路 (IC)。该 IC 集成有电流感测电阻，能够测量 SPM 电流并降低驱动系统成本。该驱动器 IC 有 7 条通道且由串行接口控制，非常适用于驱动主轴电机、滑动电机、负载电机和聚焦/跟踪/倾斜执行器。主轴电机驱动器利用 BEMF 检测（无需传感器）来启动并控制主轴电机

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPIC2040DBT	TSSOP (38)	9.70mm x 4.40mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化框图



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4 修订历史记录

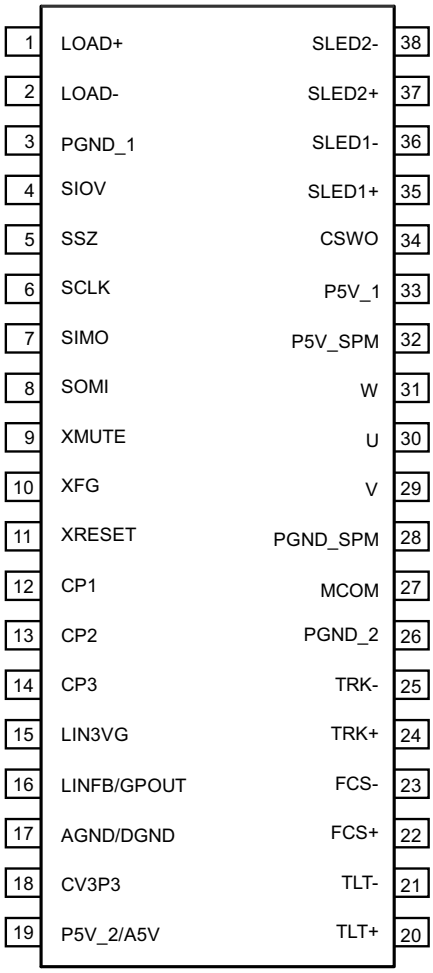
日期	修订版本	注释
2015 年 12 月	*	最初发布。

5 说明（续）

由于所有通道的输出级均在高效的 PWM 驱动下工作，因此可通过 PWM 控制实现低功率运行。可以对聚焦/跟踪/倾斜执行器驱动器进行无死区控制。此外，该器件还内置有主轴部件输出电流限制电路、热关断电路、滑动结束位置检测电路、执行器保护和电源复位电路。

6 Pin Configuration and Functions

DBT Package
38-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	LOAD+	O	Load positive output terminal
2	LOAD–	O	Load negative output terminal
3	PGND_1	PS	GND terminal
4	SIOV	PS	Power supply terminal for serial port typical 3.3 V
5	SSZ	I	SIO slave select low active input terminal
6	SCLK	I	SIO serial clock input terminal
7	SIMO	I	SIO slave input master output terminal
8	SOMI	O	SIO slave output master input terminal

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
9	XMUTE	IN	XMUTE input terminal to disable driver output
10	XFG	O	Motor speed signal output
11	XRESET	O	Power-on reset output. Internally pulled up to SIOV
12	CP1	MISC	Capacitance connection for charge pump
13	CP2	MISC	Capacitance connection for charge pump
14	CP3	MISC	Capacitance connection for charge pump
15	LIN3VG	O	3.3-V predriver output control signal for external N-channel FET
16	LINFB/GPOUT	I/O	Voltage feedback of 3.3-V predriver (be controlled to LINFB = 1.215 V)
17	AGND/DGND	PS	Ground terminal for internal logic
18	CV3P3	MISC	Capacitance terminal for internal 3.3-V regulator
19	P5V_2/A5V	PS	Power supply terminal
20	TLT+	O	Tilt positive output terminal
21	TLT–	O	Tilt negative output terminal
22	FCS+	O	Focus positive output terminal
23	FCS–	O	Focus negative output terminal
24	TRK+	O	Tracking positive output terminal
25	TRK-–	O	Tracking negative output terminal
26	PGND_2	PS	GND terminal
27	MCOM	IN	Motor center tap connection
28	PGND_SPM	PS	GND terminal for spindle driver
29	V	O	V phase output terminal for spindle motor
30	U	O	U phase output terminal for spindle motor
31	W	O	W phase output terminal for spindle motor
32	P5V_SPM	PS	Power supply terminal for spindle driver
33	P5V_1	PS	Power supply terminal
34	CSWO	O	Power switch output for 5-V OEIC in OPU
35	SLED1+	O	Sled1 positive output terminal
36	SLED1–	O	Sled1 negative output terminal
37	SLED2+	O	Sled2 positive output terminal
38	SLED2–	O	Sled2 negative output terminal

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
	+ 5 V supply voltage P5V, P5V_SPM		6	V
	Spindle output peak voltage		7	V
	Input/output voltage	–0.3	V_{CC} + 0.3 V	V
	Spindle output current		1.0	A
	Spindle output peak current (PW ≦ 2 ms, Duty ≦ 30%)		2.5	A
	Sled output peak current		0.8	A
	Focus/tilt/tracking driver output peak current		1.5	A
	Load driver output peak current		0.8	A
	Power dissipation	See *Thermal Information*		
	Operating temperature	–20	75	°C
T_{stg}	Storage temperature	–50	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
P5V	Operating supply voltage (apply for P5V)	4.5	5.0	5.5	V
V_{SIOV}	SIOV voltage	3.0	3.3	3.6	V
V_{SIFH}	XMUTE, SIMO, SSZ, SCLK pin H level input voltage range	2.2		SIOV + 0.2	V
V_{SIFL}	XMUTE, SIMO, SSZ, SCLK pin L level input voltage range	–0.2		0.8	V
I_{SPMOA}	Spindle output average current (U, V, W total)			700	mA
I_{SPMO}	Spindle output current			700	mA
I_{SLDOA}	Sled output average current			400	mA
I_{ACTOA}	Focus / tracking / tilt / loading output average current			400	mA
I_{CSWOA}	CSWO output average current			500	mA
F_{ck}	SCLK frequency	30	33.8688	35	MHz
T_O	Operating temperature	–20	25	75	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPIC2040 DBT (TSSOP) 38 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	81.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The JEDEC specification low K (1 s) board design used to derive this data.

7.5 Electrical Characteristics – Common Part

over recommended operating free-air temperature range (P5V ≈ 4.5 to 5.5 V, T_A ≈ –20℃ to 75℃, unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISTBY	Stand by supply current	LIN3P3_DIS = 1, XSLEEP = L			1.0	mA
VCV3	CV3P3 output voltage	Iload = 25 mA	2.97	3.3	3.63	V
RXM	XMUTE pulldown resistor		80	200	320	kΩ
RXRST	XRESET pullup resistor		13.2	33	52.8	kΩ
VXRSTL	XRESET low level output voltage	SIOV = 3.3 V, I_{OL} = –100 µA			0.3	V
TPOR	Power-on reset delay		15	20	25	ms
RXFG	XFG output resistor		100	200	300	Ω
VXFGH	XFG high-level output voltage	SIOV = 3.3 V, XSLEEP = 1, I_{OH} = 100 µA	SIOV – 0.3			V
VXFGL	XFG low-level output voltage	SIOV = 3.3 V, XSLEEP = 1, I_{OL} = –100 µA			0.3	V
RGPO	GPOUT output resistor		100	200	300	Ω
VGPOH	GPOUT high-level output voltage	SIOV = 3.3 V, XSLEEP = 1, GPOUT_ENA = 1,GPOUT_HL = 1, I_{OH} = 100 µA	SIOV – 0.3			V
VGPOL	GPOUT low-level output voltage	SIOV = 3.3 V, XSLEEP = 1, GPOUT_ENA = 1, GPOUT_HL = 0, I_{OH} = 100 µA			0.3	V
tTSD	Thermal protect on temperature	Design specified value	135	150	165	ºC
hytTSD	Thermal protect hysteresis temperature		5	15	25	ºC
Vonvcc	P5V reset on voltage		3.3	3.5	3.7	V
Voffvcc	P5V reset off voltage		3.5	3.7	3.9	V
Vhysvcc	P5V reset voltage hysteresis		100	200	300	mV
VonCV3	CV3P3 reset on voltage		2.4	2.5	2.6	V
VoffCV3	CV3P3 reset off voltage		2.5	2.6	2.7	V
VonSIO	SIOV reset on voltage		2.4	2.5	2.6	V
VoffSIO	SIOV reset off voltage		2.5	2.6	2.7	V
VhysSIO	SIOV reset voltage hysteresis		20	100	140	mV
VovpspmOn	OVP detection voltage (spindle) (1)		5.9	6.2	6.4	V
VovpspmOff	OVP release voltage (spindle) (1)		5.7	6.0	6.2	V
VovpSpmHys	OVP voltage hysteresis (spindle) (1)		50	200	300	mV
VovpOn	OVP detection voltage (except spindle)(1)		6.2	6.5	6.7	V
VovpOff	OVP release voltage (except spindle)(1)		6.0	6.3	6.5	V
VovpHys	OVP voltage hysteresis (except spindle)(1)		50	200	300	mV
VonLinF	LINFB reset on voltage		0.83	0.93	1.03	V
VoffLinF	LINFB reset off voltage		0.88	0.98	1.08	V
VhysLINF	LINFB reset voltage hysteresis		20	50	80	mV

(1) Those are value as protection functions only, and stress beyond those listed under *Recommended Operating Conditions* may cause permanent damage to the device.

7.6 Electrical Characteristics – Charge Pump

over recommended operating free-air temperature range (P5V ≈ 4.5 to 5.5 V, T_A ≈ –20℃ to 75℃, unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FCHGP	Frequency	XSLEEP = 1	132.6	156	179.4	kHz

Electrical Characteristics – Charge Pump (continued)

over recommended operating free-air temperature range (P5V ≈ 4.5 to 5.5 V, T_A ≈ –20℃ to 75℃, unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCHGP	Output voltage	Ccp1 = Ccp3 = 0.1 µF I_O = –1 mA	7.76	9.7	11.64	V

7.7 Electrical Characteristics – LDO Pre Driver Part

over recommended operating free-air temperature range (P5V ≈ 4.5 to 5.5 V, T_A ≈ –20℃ to 75℃, unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LINFB_Vth	LINFB threshold voltage		1.175	1.215	1.255	V

7.8 Electrical Characteristics – Spindle Motor Driver Part

over recommended operating free-air temperature range (P5V ≈ 4.5 to 5.5 V, T_A ≈ –20℃ to 75℃, unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RttlSPM	Total output resistance High side + low side(1)	I_{OUT} = 0.5 A		0.37	0.7	Ω
ResSPM	Resolution			12		bit
GnSPM	Gain	Magnification to 1.0 input	5.2	6.0	6.8	times
WidDZSPM	Spindle dead band	Forward	12h	52h	92h	
		Reverse	–92h	–52h	–12h	
WidDZSPMLS	Spindle dead band (LS mode)		–40h	0h	40h	
SPMClim	Current limit	SPM_RCOM_SEL = 00	801	890	979	mA
		SPM_RCOM_SEL = 01	882	980	1078	mA
		SPM_RCOM_SEL = 10	652	725	798	mA
		SPM_RCOM_SEL = 11	705	784	863	mA

(1) IncldRcs

7.9 Electrical Characteristics – Sled Motor Driver Part

over recommended operating free-air temperature range (P5V ≈ 4.5 to 5.5 V, T_A ≈ –20℃ to 75℃, unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RttlSLD	Total output resistance High side + low side	I_O = 0.5 A		0.9	1.3	Ω
ResSLD	Resolution			10		bit
WidDZSLD	Input dead band	Forward	2h	1Fh	60h	
		Reverse	–60h	–1Fh	–2h	
GnSLD	Sled current gain	P5V = 5 V R_L = 10 Ω, 2.2 mH VSLED = 7FFh	380	440	500	mA
VthEdetSLD	END_DET BEMF threshold voltage	SLEDENDTH<2:0> = 000	26	46	66	mV
		SLEDENDTH<2:0> = 010	42	82	122	mV
		SLEDENDTH<2:0> = 011	9	22	35	mV
		SLEDENDTH<2:0> = 100	65	125	185	mV
		SLEDENDTH<2:0> = 101	55	105	155	mV
		SLEDENDTH<2:0> = 111	70	145	220	mV

7.10 Electrical Characteristics – Focus/ Tilt/Tracking/Driver Part

over recommended operating free-air temperature range (P5V ≈ 4.5 to 5.5 V, T_A ≈ –20℃ to 75℃, unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RttlAct	Total output resistance High Side + Low Side (Focus±, Track±, Tilt±)	I_O = 0.5 A		0.9	1.3	Ω
ResACT	Resolution			12		bit
VOfstACT	Each channel output offset voltage	DAC_code = 000h	–20	0	20	mV
VOfstDACT	Output offset voltage Focus and Tilt	DIFF_TLT = 1	–50	0	50	mV
GnDAct	Difference gain Focus and Tilt	DIFF_TLT = 1	–1	0	1	db
GnAct	Gain	Magnification to 1.0 input	5.2	6	6.8	times

7.11 Electrical Characteristics – Load Driver Part

over recommended operating free-air temperature range (P5V ≈ 4.5 to 5.5 V, T_A ≈ –20℃ to 75℃, unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RttlLOD	Total output resistance High side + low side (Load±)	I_O = 0.5 A		0.9	1.3	Ω
ResLOD	Resolution			12		bit
GnLOD	Gain	Magnification to 1.0 input	5.2	6	6.8	times
WidDZLOD	Dead band	Forward		1Fh		
		Reverse		–20h		
TocpLOD	Output 100% limit time	LOAD_05CH = 0	0.64	0.8	0.96	s
IocpLOD	Overcurrent protective level	LOAD_05CH = 1 at Load_OCP_IUP = 0	120	240	400	mA
		LOAD_05CH = 1 at Load_OCP_IUP = 1	215	430	645	mA
DlyocpLOD	Overcurrent protection delay time	LOAD_05CH = 1	0.64	0.8	0.96	s

7.12 Electrical Characteristics – Current Switch Part

over recommended operating free-air temperature range (P5V ≈ 4.5 to 5.5 V, T_A ≈ –20℃ to 75℃, unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RdsCSW	Rds(on)	I_O = 0.2 A		200	500	mΩ
IlmtCSW	Current limit threshold level	CSW_OCP = 0	0.25	0.5	0.75	A
		CSW_OCP = 1	0.375	0.75	1.125	A
		CSW_OCP = 2	0.5	1.0	1.5	A
ThlCSW	Protection hold time		1.47	1.6	2.0	ms

7.13 Electrical Characteristics – Actuator Protection

over recommended operating free-air temperature range (P5V ≈ 4.5 to 5.5 V, T_A ≈ –20℃ to 75℃, unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TintACTTEMP	Update cycle		21	26	31	ms

7.14 Electrical Characteristics – Serial Port Voltage Levels

over recommended operating free-air temperature range (P5V ≈ 4.5 to 5.5 V, T_A ≈ –20℃ to 75℃, unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOMI	High-level output voltage, V_{OH}	I_{OH} = 1 mA	80 % SIOV			V
SOMI	Low-level output voltage, V_{OL}	I_{OL} = 1 mA			20% SIOV	V
SIMO	High-level input voltage, V_{IH}		70% SIOV			V
SIMO	Low level input voltage, VIL				20% SIOV	V
SIMO	Input rise/fall time	10% 90% SIOV			3.5	ns
SOMI	Output rise/fall time(1)	Cload = 30 pF, 10% 90% SIOV			10	ns
SCLK	Internal pulldown resistance		80	200	320	kΩ
SIMO			80	200	320	kΩ
SSZ	Internal pullup resistance		80	200	320	kΩ

(1) Specified by design

7.15 Serial Port I/F Write Timing Requirements

see (1)

			MIN	NOM	MAX	UNIT
F_{ck}	SCLK clock frequency	SIOV = 3.3 V			35	MHz
t_{ckl}	SCLK low time		11			ns
t_{ckh}	SCLK high time		11			ns
t_{sens}	SSZ setup time		7			ns
t_{senh}	SSZ hold time		7			ns
t_{sl}	SSZ disable high time		11			ns
t_{ds}	SIMO setup time (Write)		7			ns
t_{dh}	SIMO hold time (Write)		7			ns

(1) Specified by design

7.16 Serial I/F Read Timing Requirements

			MIN	NOM	MAX	UNIT
F_{ck}	SCLK clock frequency	SIOV = 3.3 V			35	MHz
t_{ckl}	SCLK low time		11			ns
t_{ckh}	SCLK high time		11			ns
t_{sens}	SSZ setup time		7			ns
t_{senh}	SSZ hold time		7			ns
t_{sl}	SSZ disable high time		11			ns
t_{ds}	SIMO setup time (Write)		7			ns
t_{dh}	SIMO hold time (Write)		7			ns
t_{rdly}	SOMI delay time (Read)	CLOAD = 10 pF, SIOV = 3.3 V	2		9	ns
t_{sendl}	SOMI hold time (Read)	CLOAD = 10 pF, SIOV = 3.3 V	2		9	ns
t_{rls}	SOMI release time (Read)	CLOAD = 10 pF, SIOV = 3.3 V From SSZ rise to SOMI HIZ	0		9	ns

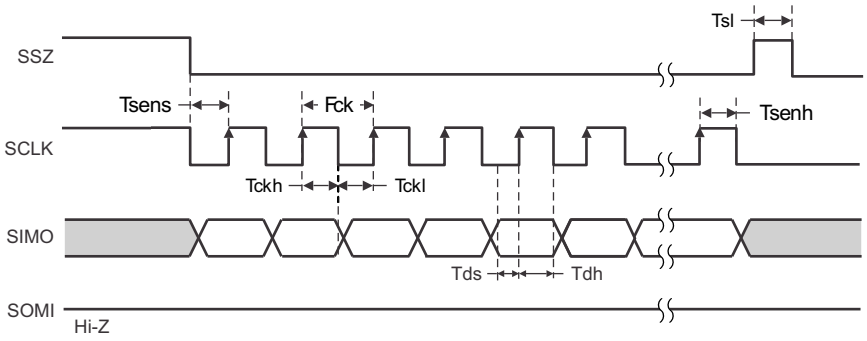


Figure 1. Serial Port Write Timing

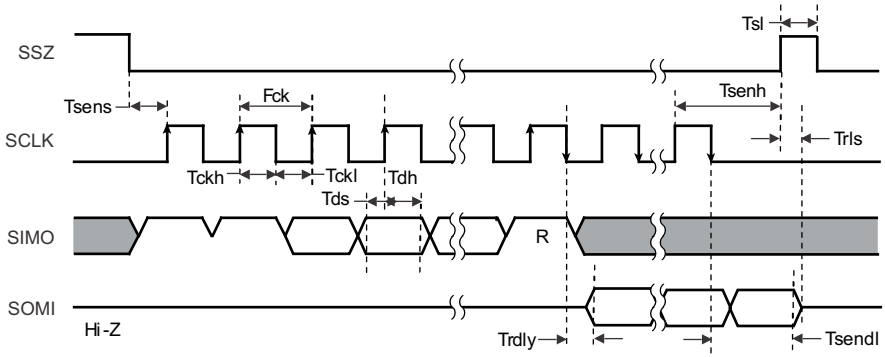


Figure 2. Serial Port Read Timings

7.17 Typical Characteristics

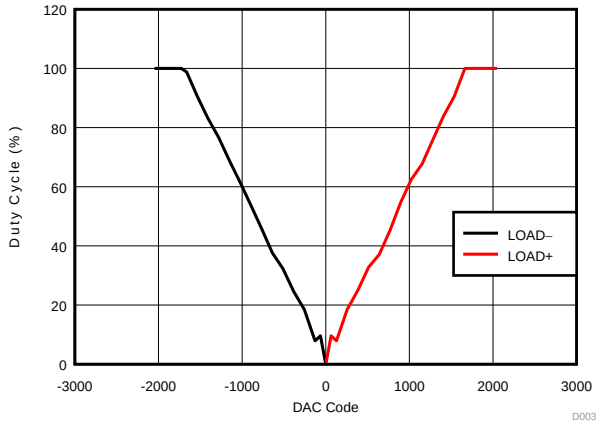


Figure 3. DAC Code vs Duty Cycle for LOAD Outputs

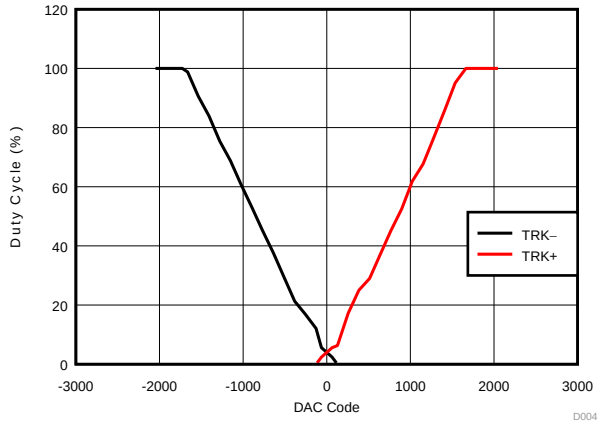


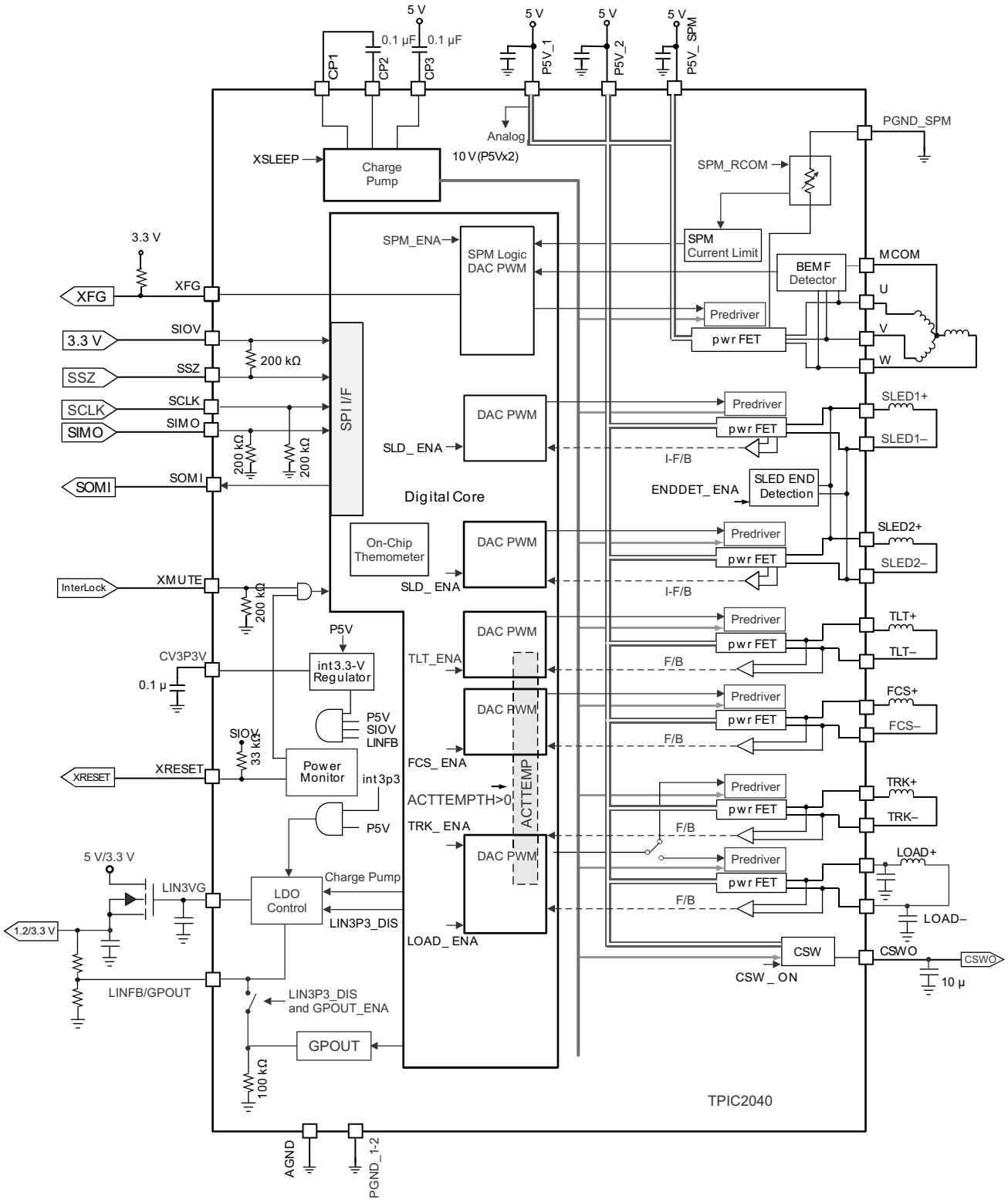
Figure 4. DAC Code vs Duty Cycle for TRK Outputs

8 Detailed Description

8.1 Overview

TPIC2040 is low noise type motor driver IC suitable for 5V optical disk drives. The 7-channel driver IC controlled by serial I/F is optimum for driving a spindle motor, a sled motor (stepping motor applicable), a load motor, and Focus / Tracking / Tilt actuators. This IC's integrated current sense resistance to measure SPM current reduces drive system cost in drastically. The spindle motor driver part uses integrated sensorless logic to attain very low-noise operation during startup and runtime. By using BEMF feedback, external sensors, such as a Hall device, are not needed to carry out self-starting by the starting circuit or perform position detection. By using the efficient PWM drivers, low-power operation can be achieved by controlling the PWM outputs. Dead zone less control is possible for a Focus / Tracking / Tilt actuator driver. In addition, the spindle part output current limiting circuit, the thermal shut down circuit, and the sled end-detection circuit offer protection for all actuators and motors.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Protect Function

TPIC2040 has five protection features, undervoltage lockout (UVLO), over voltage protection (OVP), short circuit protection (SCP), thermal protection (TSD), and actuator temperature protection (ACTTIMER) in order to protect target equipment. A protect behavior differ by generated events.

8.3.1.1 Undervoltage Lockout (UVLO)

Power Faults are reported in the UVLOMon register. Each UVLOMon bit will be initialized to zero upon a cold power up.

After a fault is detected the appropriate fault bit will be latched high. Writing to the RST_ERRFLG (REG77) will clear all UVLOMon bits. The power device faults and actions are summarized in Table 1.

Table 1. Power Fault Monitor

FAULT TYPE	LATCHED REGISTER	XRESET	CRITERIA	SPM	ACTUATOR	LDO PRE DRIVER
P5V under voltage	UVLO_P5V	Yes	<3.5 V	Hi-Z	Hi-Z	Hi-Z
internal 3.3V under voltage	UVLO_INT3P3	Yes	<2.5 V	Hi-Z	Hi-Z	Hi-Z
LINFB under voltage	UVLO_1P2V	Yes	<0.93 V	Hi-Z	Hi-Z	(13-ms timeout then 120-ms Hi-Z)
SIOV under voltage	UVLO_SIOV	Yes	<2.5 V	Hi-Z	Hi-Z	—
P5V over voltage	OVP_P5V		>6.2 V	Brake	—	—
			>6.5 V	Hi-Z	Hi-Z	—

8.3.1.2 Overvoltage Protection (OVP)

Over voltage protect function is aimed to protect the unit from the supplying hi-voltage.

When the supply voltage exceeds 6.5 V, all driver output goes Hi-Z. When the supply voltage falls below typical 6.2 V, (6.0 V for SPM) all output start to operate again. The OVP and POR (XRESET) function is not interlocking.

Moreover, when power supply exceeds 6.2 V, especially SPM enter short brake mode. This operation is offered supposing a voltage rising by motor BEMF of the high velocity revolution.

This function is for insurance, so it cannot assure that the device is safety in the condition. Because the absolute maximum ratings range of the supply voltage is 6 V. When this function works, the feedback terminals are not shorted to GND.

Figure 5 shows the behavior of over voltage protection.

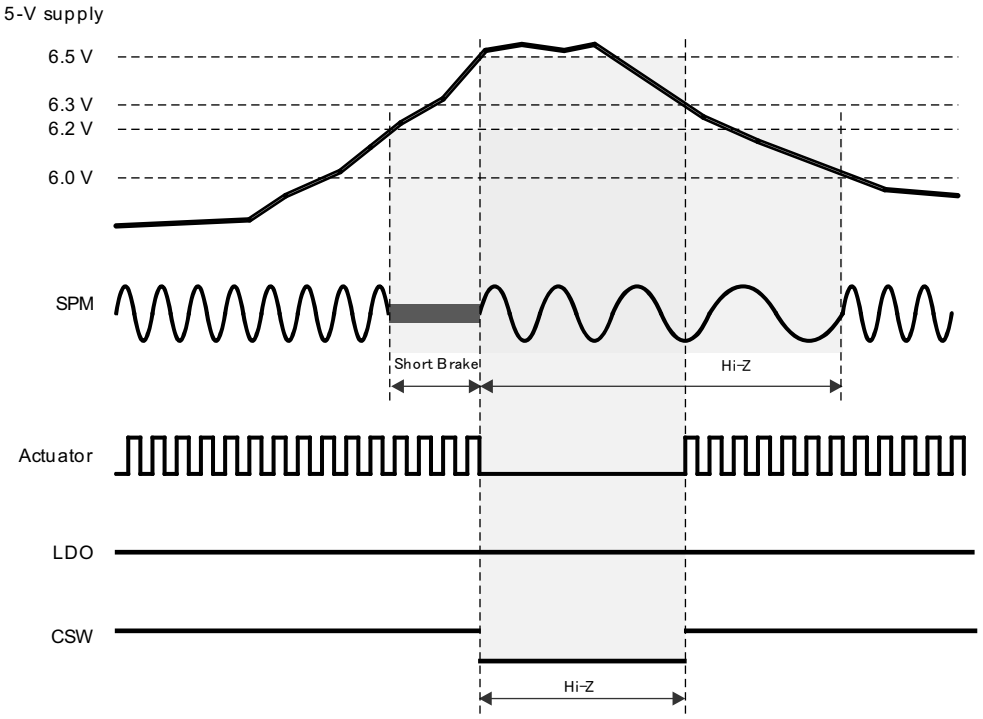


Figure 5. Overvoltage Protection

8.3.1.3 Overcurrent Protection (OCP)

The over current protect function serve to protect the device from break down by large current. The OCP is provided for four circuit blocks, and each threshold are on Table 2.

Table 2. OCP Threshold

BLOCK	DETECTION CURRENT	MONITOR TIME	PROTECTION TIME	LATCHED FLAG
Load driver 1 channel	continue 100% duty	800 ms	Forever	OCP_LOAD
Load driver 0.5 channel	240 mA/425 mA	800 ms	Forever	OCP_LOAD
CSW driver	500, 750, 1000 mA	20 µs	1.6 ms	OCP_CSW

When the large current is detected on each block, device put the output FET to Hi-Z.

The amounts of currents and time have specified the detection threshold for every circuit block.

When OCP occurs, it returns automatically after expiring set Hi-Z period.

OCPERR (REG7F) and OCP flag (REG7B) are set at OCP detection.

8.3.1.3.1 OCP for Load Driver

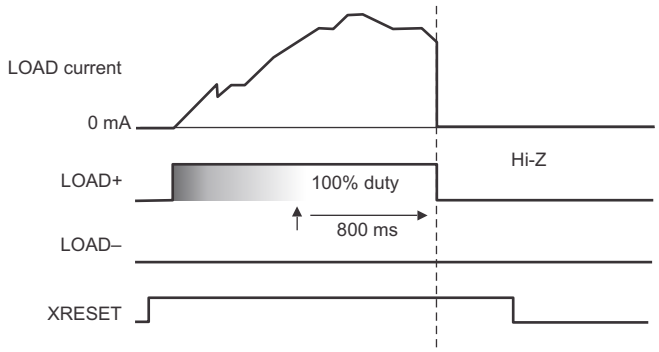


Figure 6. Overcurrent Protection Load 1 Channel

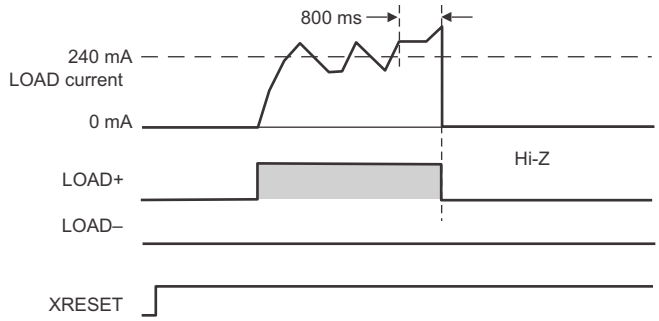


Figure 7. Overcurrent Protection Load 0.5 Channel

8.3.1.3.2 OCP for CSW

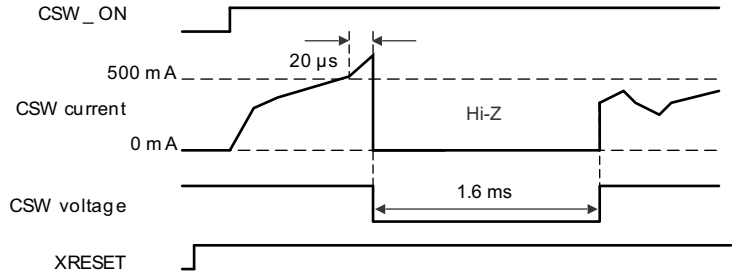


Figure 8. Overcurrent Protection Current Switch

SCP function always monitors the output voltage of high-side and low-side FET of output driver, and when the setting voltage is not outputted, it recognizes as SCP and changed output Hi-Z. It returns to the original state automatically 1.6 ms after.

Table 3. SCP Condition

BLOCK	FUNCTION	DETECTION CONDITION	DETECT TIME	HI-Z HOLD TIME
SPM driver	SCP	Monitor driver output voltage High-side FET output V = GND Low-side FET output V = Supply V	0.8 to 1.6 µs	1.6 ms
Sled driver				
Load driver				
Actuator driver				

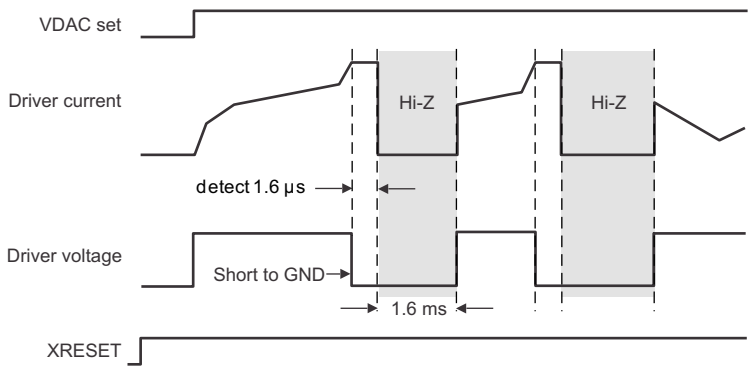


Figure 9. Example of SCP (Driver Short to GND)

8.3.1.4 Thermal Protection (TSD)

The thermal protection (TSD) is a protection function which intercepts an output and suspends an operation when the IC temperature exceed a maximum permissible on a safety. TSD makes an output Hi-Z when the temperature rises up and a threshold value is exceeded. There are two levels for threshold Alert and Trip. An alarm is given by status register TSD_FAULT_ on Alert level with 135°C. It continues rising up temperature, the register TSD_ is set at 150°C and the driver output changes HI-Z. If temperature falls and is reached 135°C, it will output again.

TPIC2040 has total 10 temperature sensors in each circuit block. Particular sensor is assigned to appropriate status flag in Table 4.

Table 4. Thermal Sensor Assignment

CIRCUIT	ALERT (°C)	TRIP (°C)	RELEASE (°C)	ALERT FLAG	TRIP FLAG
U	135	150	135	TSD_FAULT_SPM	TSD_SPM
V	135	150	135	TSD_FAULT_SPM	TSD_SPM
W	135	150	135	TSD_FAULT_SPM	TSD_SPM
TLT	135	150	135	TSD_FAULT_ACT	TSD_ACT
FCS	135	150	135	TSD_FAULT_ACT	TSD_ACT
TRK	135	150	135	TSD_FAULT_ACT	TSD_ACT
SLED1	135	150	135	TSD_FAULT_ACT	TSD_ACT
SLED2	135	150	135	TSD_FAULT_ACT	TSD_ACT
LOAD	135	150	135	TSD_FAULT_ACT	TSD_ACT
CSW	135	150	135	TSD_FAULT_ACT	TSD_ACT

8.3.1.5 Actuator Temperature Protection (ACTTIMER)

TPIC2040 has Actuator protect function named ACTTIMER. This function enables to avoid from being broken by setting actuator channel output to HIZ when actuator coil current exceeds the specific value. Up to now, be used a simple actuator protect function such like exceeding max current with continuous time. However these types were not accurate. This new protection enables to calculate heat accumulation and judge correctly. When this function operates, and load channel output will be Hi-Z, too. And spindle channel will be forced Auto short brake and disc motor will stop.

It is able to know the protection has occurred by checking Fault register ACTTIMER_FAULT (REG7F) and ACT_TIMER_PROT (REG78). ACTTIMER_FAULT has a character of advance notice, is set before detecting ACT_TIMER_PROT. Once an ACT_TIMER_PROT is set, even if temperature falls, it will not release protection automatically. It is necessary to clear the flag by setting RST_ERR_FLAG (REG77) or setting 0 to ACTTEMPTH (REG72). ACTTIMER function is able to disable by setting H to ACTPROT_OFF (REG72) or setting 0 to ACTTEMPTH (REG72).

In order to acquire the optimal value for ACTTEMPTH, you should set device into the condition of the detection level, and reading the value of ACTTEMP. Because of the present value can be read from ACTTEMP (REG78). (1)

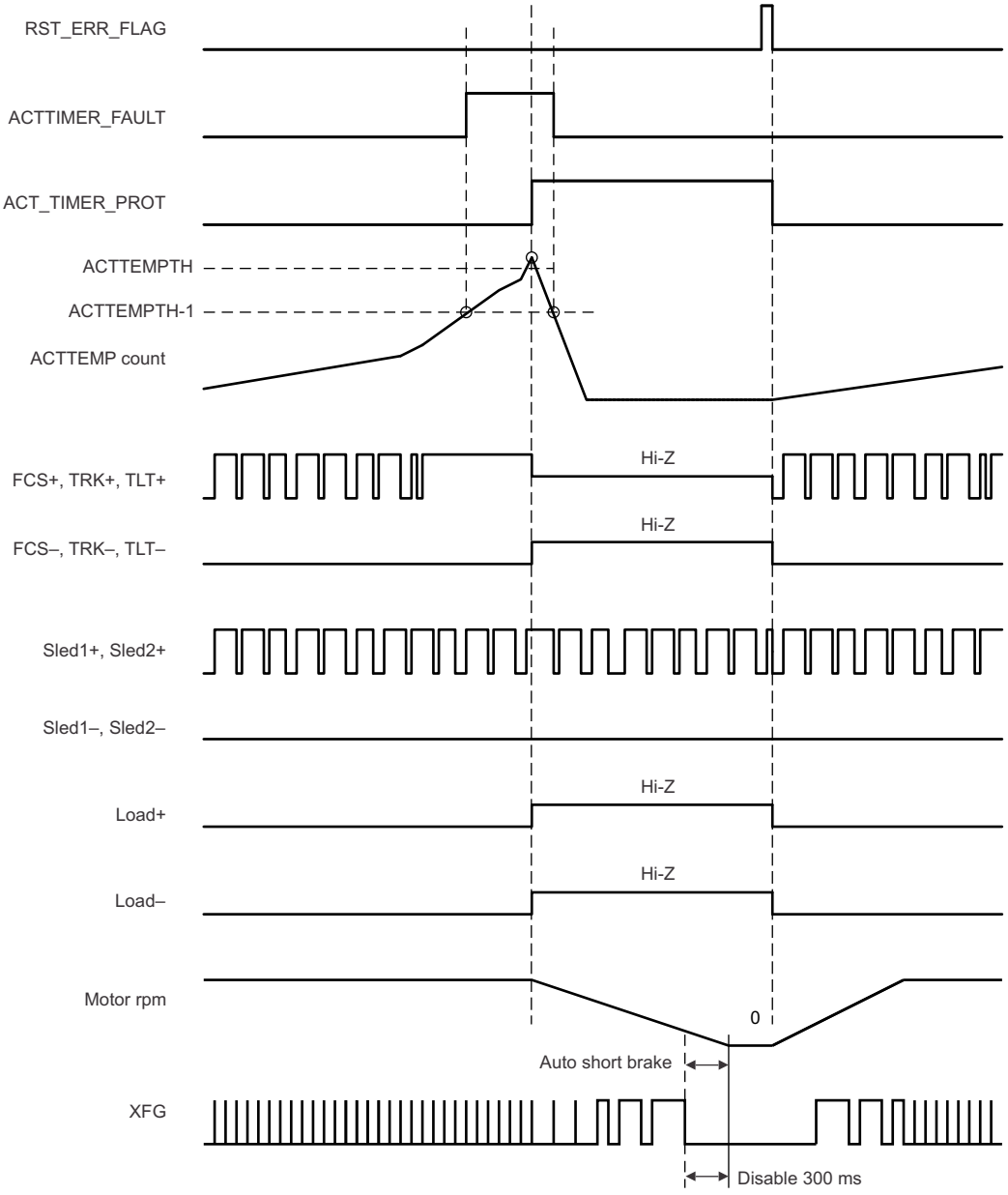


Figure 10. Actuator Temperature Protections

(1) The ACTTEMP data is updated on Register in ACTPROT_OFF = 0 and ACTTEMPTH > 0.

8.4 Device Functional Modes

8.4.1 Power-on Reset (POR)

8.4.1.1 Power-Up Sequences

In TPIC2040, the normal sequence is to wait for 5-V supply to come up to 2.2 V. After 5 V establish, the internal 3.3 V will start and wait until stabilize. Now the voltage monitors start to work and begin to look for the LDO output. When LINFB pin over 0.98 V with SIOV over 2.6 V, the power up sequence finishes and the part starts to function. Once the part finishes all of its power up tasks, it takes XRESET high to indicate that the part is no longer in reset and ready to communicate to the outside world. Figure 11 is example of power-up sequence which is set 3.3-V LDO output and output is used for SIOV supply.

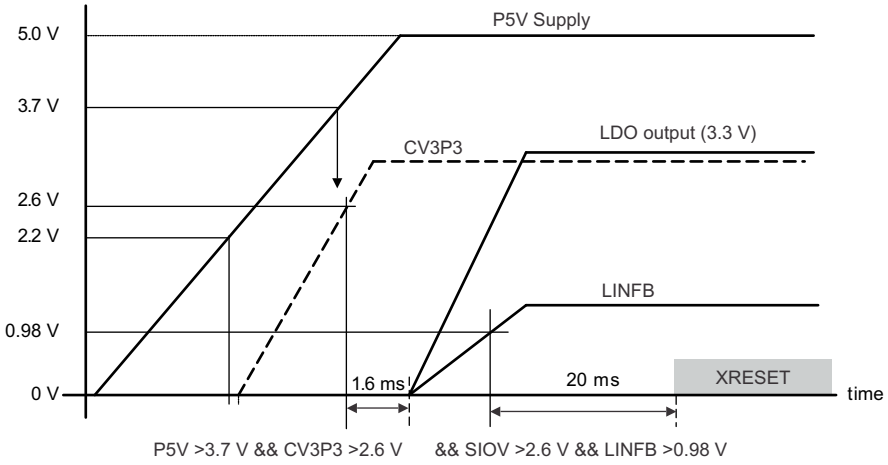


Figure 11. POR (Enable LDO)

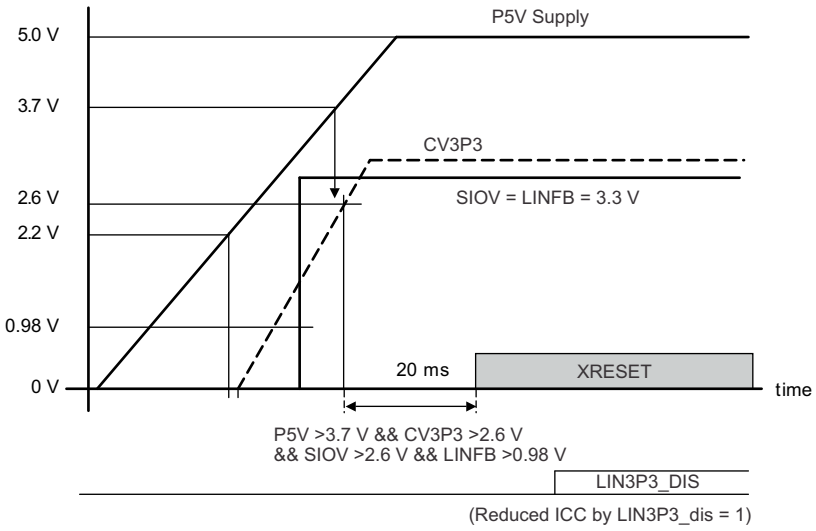


Figure 12. POR (Disable LDO)

Device Functional Modes (continued)

8.4.1.2 XRESET

TPIC2040 is preparing XRESET pin in order to notify an own status to DSP. TPIC2040 set XRESET to L when the event which has a serious effect on DSP occurs such like the power failure, the over temperature. If all the exception is removed, it will tell that XRESET pin would be set to H and it would be in the ready state. The POR (Power on reset) condition is shown in Figure 23 POR block diagram. All the behavior of XRESET is shown in Figure 14.

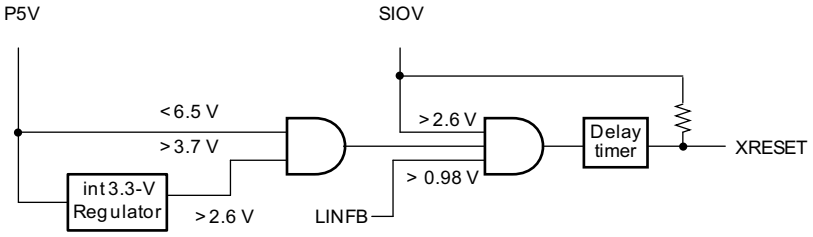


Figure 13. POR Block Diagram

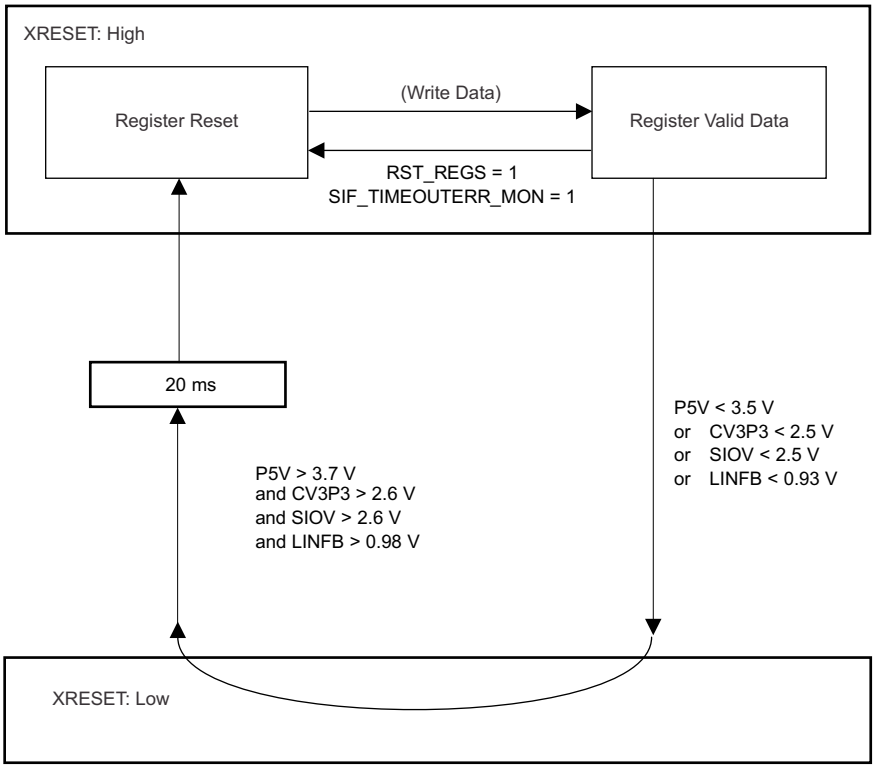


Figure 14. XRESET Behavior

8.4.2 XMUTE

This IC has XMUTE pin which had fail-safe function in preparation for unexpected operation.

If XMUTE signal is inputted during operation, all the outputs will be suspended and the danger will be avoided.

TPIC2040 will turn off all enable bits, actuator (TLT_ENA/FCS_ENA/TRK_ENA), SPM_ENA, SLD_ENA, LOAD_ENA and CSW_ON when XMUTE input change to L. LOAD_ENA bit will be disabled only when LOAD_05CH = 1. Also log this event to error latch flag XMUTE_DETECT (REG79) and PWRERR (REG7F).

On the other hand, if it is set as XMUTE_NORST (REG7F) = 1, change of XMUTE will not influence to enable bits.

8.5 Programming

8.5.1 Serial Port Functional Description

The serial communication of TPIC2040 is based on a SPI communications protocol. TPIC2040 is put on the slave side.

All 16-bit transmission data is effective in SSZ = L period.

The bit stream sent through SIMO from a master (DSP) is latched to an internal shift register by the rising edge of SCLK. All the data is transmitted in a total of 16-bit format of a command and data. A format has two types of data, 8 bits and 12 bits length. In order to access specific registers, an address and R/W flag are specified as a command part. In addition, 12-bit data do not have R/W flag in the packet because DAC register (= 12-bit data form) are Write only. A transfer packet, command and data, is transmitted sequentially from MSB to LSB. A packet is distinguished in MSB 2 bits of command. In the case of 11, it handles a packet for control register access, and the other processed as a packet for a DAC data setting.

There are the following four kinds of serial-data communication packets.

1. Write 12 bits DAC data (MSB two bit ≠ 11)
2. Write 8 bits control register (MSB two bit = 11)
3. Read 8 bits control register (MSB two bit = 11)
4. Write 12 bits Focus DAC data + Read 8 bits status register at the same time (MSB two bit ≠ 11)

8.5.2 Write Operation

For write operation, DSP transmits 16 bit (command + address + data) data a bit every in an order from MSB.

Only the 16-bit data which means 16 SCLK sent from the master during SSZ = L becomes effective. If more than 17 or less than 15 SCLK pulses are received during the time that SSZ is low, the whole packet will be ignored. For all valid write operations, the data of the shift register is latched into its designated internal register at rising edge of 16th SCLK. All internal register bits, except indicated otherwise, are reset to their default states upon power-on-reset.

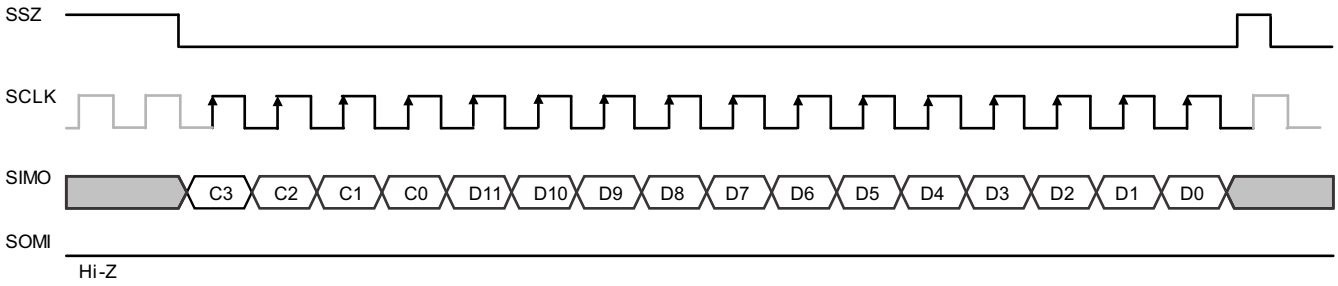


Figure 15. Write 12-Bits DAC Data

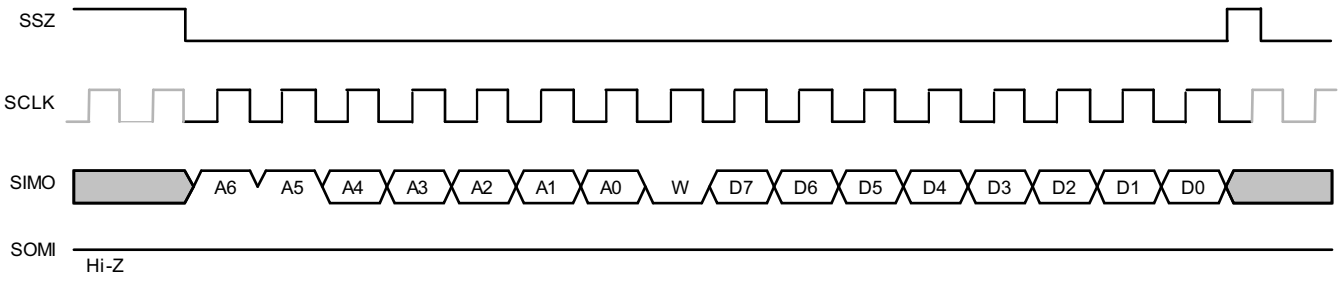


Figure 16. Write 8-Bits Control Register

Programming (continued)

8.5.3 Read Operation

DSP sends 8-bit header through SIMO, in order to perform Read operation. TPIC2040 will start to drive the SOMI line upon the eighth falling edge of SCLK and shift out eight data bits. The master DSP inputs 8bits data from SOMI after the ninth rising edge of SCLK. There is optional read mode that SOMI data is advanced a half clock cycle of SCLK. This mode becomes effective by setting ADVANCE_RD (REG74) = H.

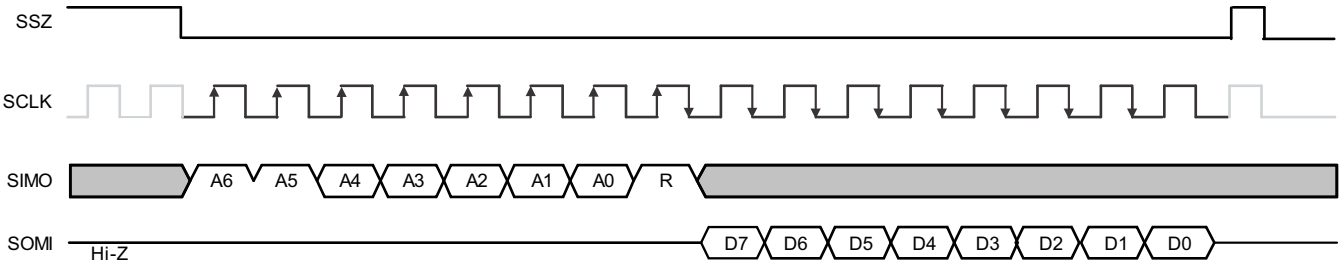


Figure 17. Read 8-Bits Control Register

8.5.4 Write and Read Operation

Optionally, the master DSP can read Status register during writing 12 bits DAC (Focus DAC) packet. It is enabled by setting bit STATUS_ON_VFCS (REG74) = H.

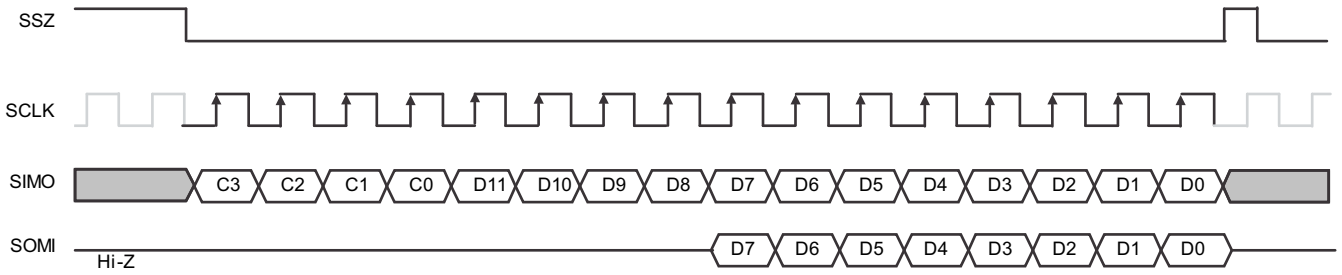


Figure 18. Write 12-Bits Focus DAC Data + Read 8-Bits Status Data

8.6 Register Maps

All registers are in WRITE-protect mode after XRESET release. WRITE_ENA bit (REG76) = H is required before writing data in register.

8.6.1 Register State Transition

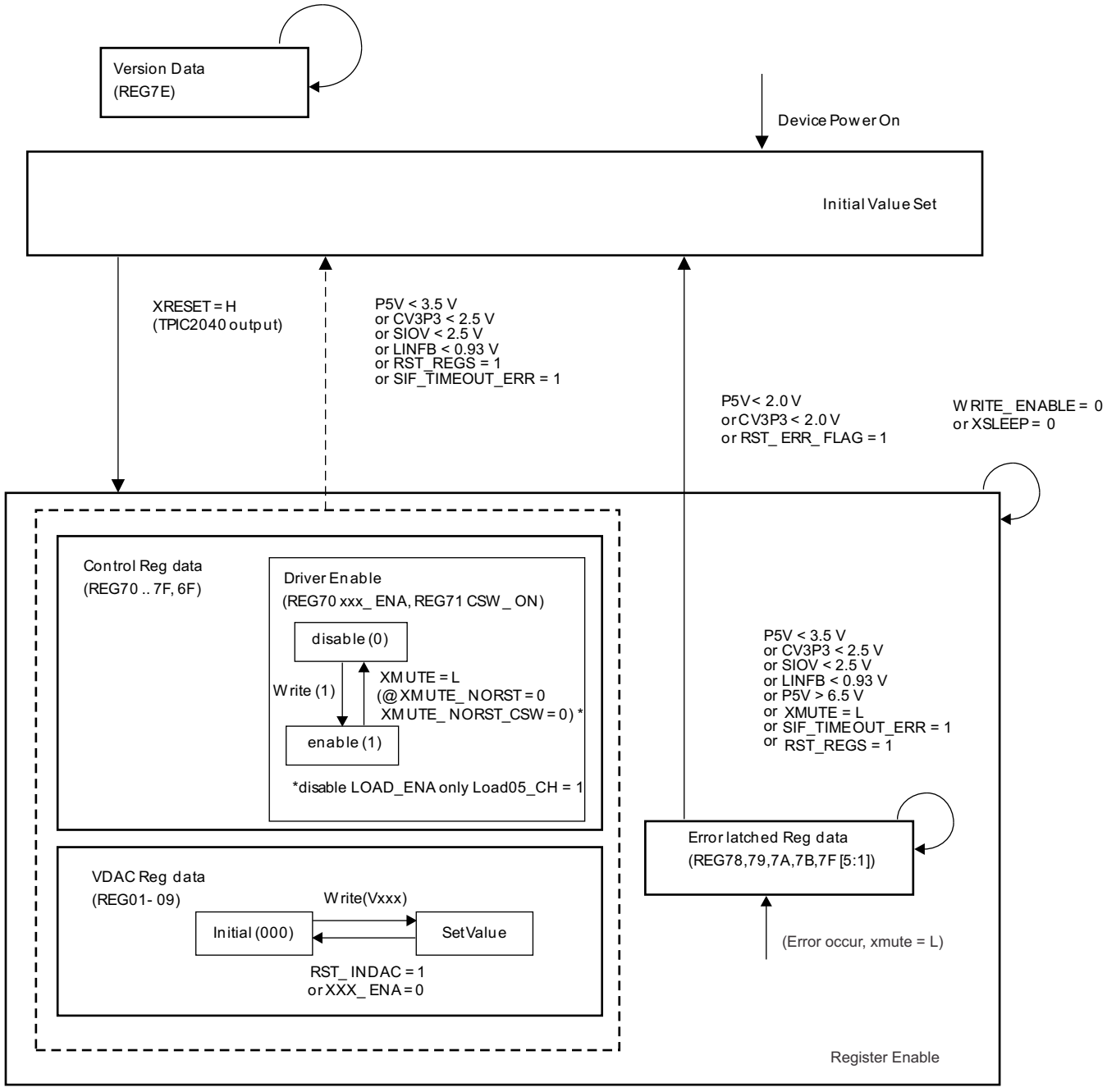


Figure 19. Register State Transition Chart

Two difference forms are prepared in 12-bit DAC register, and the forms can be selected by setting VDAC_MAPSW (REG74h).

Table 5. DAC Register (VDAC_MAPSW = 0)

REG	NAME	F	11	10	9	8	7	6	5	4	3	2	1	0
00h	**N/A**	W	N/A				N/A				N/A			
01h	**VTLT**	W	VTLT[11]	VTLT[10]	VTLT[9]	VTLT[8]	VTLT[7]	VTLT[6]	VTLT[5]	VTLT[4]	VTLT[3]	VTLT[2]	VTLT[1]	VTLT[0]
02h	**VFCS**	W	VFCS[11]	VFCS[10]	VFCS[9]	VFCS[8]	VFCS[7]	VFCS[6]	VFCS[5]	VFCS[4]	VFCS[3]	VFCS[2]	VFCS[1]	VFCS[0]
03h	**VTRK**	W	VTRK[11]	VTRK[10]	VTRK[9]	VTRK[8]	VTRK[7]	VTRK[6]	VTRK[5]	VTRK[4]	VTRK[3]	VTRK[2]	VTRK[1]	VTRK[0]
04h	**VSLD1**	W	VSLD1[11]	VSLD1[10]	VSLD1[9]	VSLD1[8]	VSLD1[7]	VSLD1[6]	VSLD1[5]	VSLD1[4]	VSLD1[3]	VSLD1[2]	*VSLD1[1]	*VSLD1[0]
05h	**VSLD2**	W	VSLD2[11]	VSLD2[10]	VSLD2[9]	VSLD2[8]	VSLD2[7]	VSLD2[6]	VSLD2[5]	VSLD2[4]	VSLD2[3]	VSLD2[2]	*VSLD2[1]	*VSLD2[0]
06h	**N/A**	W	N/A				N/A				N/A			
07h	**N/A**	W	N/A				N/A				N/A			
08h	**VSPM**	W	VSPM[11]	VSPM[10]	VSPM[9]	VSPM[8]	VSPM[7]	VSPM[6]	VSPM[5]	VSPM[4]	VSPM[3]	VSPM[2]	VSPM[1]	VSPM[0]
09h	**VLOAD**	W	VLOAD[11]	VLOAD[10]	VLOAD[9]	VLOAD[8]	VLOAD[7]	VLOAD[6]	VLOAD[5]	VLOAD[4]	VLOAD[3]	VLOAD[2]	VLOAD[1]	VLOAD[0]
0Ah	**N/A**	W	N/A				N/A				N/A			
0Bh	**N/A**	W	N/A				N/A				N/A			

8.6.2 DAC Register (12-Bit Write Only)

Table 6. DAC Register (VDAC_MAPSW = 1)

REG(1)	NAME	F	11	10	9	8	7	6	5	4	3	2	1	0
00h	**N/A**	W	N/A				N/A				N/A			
01h	**VTLT**	W	VTRK[11]	VTRK[10]	VTRK[9]	VTRK[8]	VTRK[7]	VTRK[6]	VTRK[5]	VTRK[4]	VTRK[3]	VTRK[2]	VTRK[1]	VTRK[0]
02h	**VFCS**	W	VFCS[11]	VFCS[10]	VFCS[9]	VFCS[8]	VFCS[7]	VFCS[6]	VFCS[5]	VFCS[4]	VFCS[3]	VFCS[2]	VFCS[1]	VFCS[0]
03h	**VTRK**	W	VTLT[11]	VTLT[10]	VTLT[9]	VTLT[8]	VTLT[7]	VTLT[6]	VTLT[5]	VTLT[4]	VTLT[3]	VTLT[2]	VTLT[1]	VTLT[0]
04h	**VSLD1**	W	VSLD1[11]	VSLD1[10]	VSLD1[9]	VSLD1[8]	VSLD1[7]	VSLD1[6]	VSLD1[5]	VSLD1[4]	VSLD1[3]	VSLD1[2]	*VSLD1[1]	*VSLD1[0]
05h	**VSLD2**	W	VSLD2[11]	VSLD2[10]	VSLD2[9]	VSLD2[8]	VSLD2[7]	VSLD2[6]	VSLD2[5]	VSLD2[4]	VSLD2[3]	VSLD2[2]	*VSLD2[1]	*VSLD2[0]
06h	**VSPM**	W	VSPM[11]	VSPM[10]	VSPM[9]	VSPM[8]	VSPM[7]	VSPM[6]	VSPM[5]	VSPM[4]	VSPM[3]	VSPM[2]	VSPM[1]	VSPM[0]
07h	**N/A**	W	N/A				N/A				N/A			
08h	**N/A**	W	N/A				N/A				N/A			
09h	**VLOAD**	W	N/A				VLOAD[11]	VLOAD[10]	VLOAD[9]	VLOAD[8]	VLOAD[7]	VLOAD[6]	VLOAD[5]	VLOAD[4]
0Ah	**N/A**	W	N/A				N/A				N/A			
0Bh	**N/A**	W	N/A				N/A				N/A			

(1) TPIC2040 process as 0 even if set 1.

8.6.3 Control Register

Table 7. Control Register (8bit Read/Write)(1)

REG	NAME	F	7	6	5	4	3	2	1	0
70h	DriverEna	R/W	TLT_ENA	FCS_ENA	TRK_ENA	SPM_ENA	SLD_ENA	TI reserved	LOAD_ENA	XSLEEP
71h	FuncEna	R/W	SPM_LSMODE	ENDDET_ENA	LIN3P3_DIS	TI reserved	CSW_ON	XMUTE_NORST_CSW	TI reserved	
72h	ACTCfg	R/W	LOAD_O5CH_HIGH	LOADPROT_OFF	ACTPROT_OFF	ACTTEMPTH				
73h	Parm0	R/W	SIF_TIMEOUT_TH		SLEDEND_HZTIME	SLDENDTH[1:0]		SPM_RCOM_SEL		XMUTE_NORST
74h	OptSet	R/W	DIFF_TLT	LOAD05_CH	STATUS_ON_VFCS	VSLD2_POL	LOAD_OCP_IUP	TI reserved	SOMI_HIZ	VDAC_MAPSW
75h	Protect	R/W	TI reserved							TSD_TUP
76h	WriteEna	R/W	WRITE_ENABLE	TI reserved						
77h	ClrReg	W	RST_INDAC	RST_REGS	RST_ERR_FLAG	TI reserved				
78h	ActTemp	R	TI reserved		ACT_TIMER_PROT	ACTTEMP				
79h	UVLOMon	R	TI reserved		XMUTE_DETECT	UVLO_P5V	UVLO_INT3P3	UVLO_SIOV	UVLO_1P2V	OVP_P5V
7Ah	TsdMon	R	TI reserved	TSD_FAULT_SPM	TSD_FAULT_ACT	TI reserved		TSD_SPM	TSD_ACT	TI reserved
7Bh	ProtMon	R	TI reserved	OCP_LOAD	TI reserved	OCP_CSW	SCP_SPM	SCP_SLED	SCP_LOAD	SCP_ACT
7Ch	Protect	R	TI reserved							
7Dh	Protect	R	TI reserved							
7Eh	Version	R	Version							
7Fh	Status	R	ACTTIMER_FAULT	ENDDET	SIF_TIMEOUTERR	PWRERR	TSDERR	OCPSCPERR	TSDFAULT	FG
60h	Protect	R/W	TI reserved							
61h	Protect	R/W	TI reserved							
62h	Protect	R/W	TI reserved							
63h	Protect	R/W	TI reserved							
64h	Protect	R/W	TI reserved							
65h	Protect	R/W	TI reserved							
66h	Protect	R/W	TI reserved							
6Ah	Protect	R/W	TI reserved		CSW_OCP	TI reserved				

(1) VTRK and VLOAD is exclusive, using same DAC block

Table 7. Control Register (8bit Read/Write)(0) (continued)

REG	NAME	F	7	6	5	4	3	2	1	0
6Ch	Parm1	R/W	TI reserved			EDET_DELAY	SLDENDTH[2]			
6Dh	Protect	R/W	TI reserved							
6Eh	Protect	R/W	TI reserved							
6Fh	MonitorSet	R/W	ACTTIMER_FLT_MON	ENDDET_MON	SIF_TIMEOUTERR_MON	PWRERR_MON	TSDERR_MON	OCPSCPERR_MON	TSDFAULT_MON	TI reserved

8.6.4 Detailed Description of Registers

8.6.4.1 REG01 12bit DAC for Tilt (VDAC_MAPSW = 0)

Figure 20. Tilt (REG01)

15	14	13	12	11	10	9	8
				VTLT			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VTLT							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. TILT (REG01) Field Descriptions

Bit	Field	Type	Default	Description
11-0	VTLT	w	0	Digital input code for Tilt. 2's compliment format 0x800(-2048) to 0x7ff(+2047) Output is changed by differential Tilt mode (REG74[7]) TLT_OUT = VTLT × (6.0 / 2048) (DIFF_TLT = 0) TLT_OUT = (VFCS-VTLT) × (6.0 / 2048) (DIFF_TLT = 1) *TLT_OUT should be changed after writing VFCS.* In DIFF_TLT mode *(DIFF_TLT = 1)*, TLT_OUT should be changed after writing VFCS.

8.6.4.2 REG02 12bit DAC for Focus (VDAC_MAPSW = 0)

Figure 21. Focus (REG02)

15	14	13	12	11	10	9	8
				VFCS			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VFCS							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. Focus (REG02) Field Descriptions

Bit	Field	Type	Default	Description
11-0	VFCS	w	0	Digital input code for Focus. 2's compliment format 0x800(-2048) to 0x7ff(+2047) Output is changed by differential Tilt mode (REG74[7]) FCS_OUT = VFCS × (6.0 / 2048) (DIFF_TLT = 0) FCS_OUT = (VFCS + VTLT) × (6.0 / 2048) (DIFF_TLT=1)

8.6.4.3 REG03 12bit DAC for Tracking (VDAC_MAPSW = 0)

Figure 22. Tracking (REG03)

15	14	13	12	11	10	9	8
VTRK							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VTRK							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. Tracking (REG03) Field Descriptions

Bit	Field	Type	Default	Description
11-0	VTRK	w	0	Digital input code for Tracking. 2's compliment format 0x800(-2048) to 0x7ff(+2047) TRK_OUT = VTRK × (6.0 / 2048)

8.6.4.4 REG04 10bit DAC for Sled1 (VDAC_MAPSW = 0)

Figure 23. Sled1 (REG04)

15	14	13	12	11	10	9	8
VSLD1							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VSLD1							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. Sled1 (REG04) Field Descriptions

Bit	Field	Type	Default	Description
11-2	VSLD1	w	0	Digital input code for Sled1. 2's compliment format 0x800(-2048) to 0x7ff(+2047) Two bits on LSB, VSLD1[1:0], will be handled with zero. SLD1_OUT = VSLD1 × (440 mA / 2048)

8.6.4.5 REG05 10bit DAC for Sled2 (VDAC_MAPSW = 0)

Figure 24. Sled2 (REG05)

15	14	13	12	11	10	9	8
VSLD2							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VSLD2							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. Sled2 (REG05) Field Descriptions

Bit	Field	Type	Default	Description
11-2	VSLD2	w	0	Digital input code for Sled2. 2's compliment format 0x800(-2048) to 0x7ff(+2047) Two bits on LSB, VSLD2[1:0], will be handled with zero. SLD2_OUT = VSLD2 × (440mA / 2048)

8.6.4.6 REG08 12bit DAC for Spindle (VDAC_MAPSW = 0)

Figure 25. Spindle (REG08)

15	14	13	12	11	10	9	8
				VSPM			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VSPM							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. Spindle (REG08) Field Descriptions

Bit	Field	Type	Default	Description
11-0	VSPM	w	0	Digital input code for Spindle. 2's compliment format 0x800(-2048) to 0x7ff(+2047) SPM_OUT = VSPM × (6.0 / 2048)

8.6.4.7 REG09 12bit DAC for Load (VDAC_MAPSW = 0)

Figure 26. Load (REG09)

15	14	13	12	11	10	9	8
				VLOAD			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VLOAD							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. Load (REG09) Field Descriptions

Bit	Field	Type	Default	Description
11-0	VLOAD	w	0	Digital input code for Load. 2's compliment format 0x800(-2048) to 0x7ff(+2047) LOAD_OUT = VLOAD × (6.0 / 2048)

8.6.4.8 REG6A 8-Bit Control Register for CSW_OCP (REG6A)

Figure 27. CSW_OCP (REG6A)

7	6	5	4	3	2	1	0
TI reserved		CSW_OCP		TI reserved			
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. CSW_OCP (REG6A) Field Descriptions

Bit	Field	Type	Default	Description
7-6		rw	0	
5-4	CSW_OCP	rw	0	CSW OCP current threshold selection 00: 0.5 A 01: 0.75 A 10: 1 A 11: OCP disable
3-0	TI reserved	rw	0	

8.6.4.9 REG6C 8-Bit Control Register for Parm1 (REG6C)

Figure 28. Parm1 (REG6C)

7	6	5	4	3	2	1	0
TI reserved			EDET_DELAY		TI reserved		SLDENDTH[2]
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. Parm1 (REG6C) Field Descriptions

Bit	Field	Type	Default	Description
7-5	TI reserved	rw	0	
4-3	EDET_DELAY	rw	0	Timing parameter of detection window for sled end detection. (delay time / window width) EDET_DELAY[1:0] 00: 0 ms/0.41 ms 01: 0.62 ms/0.20 ms 10: 0.93 ms/0.30 ms 11: 1.24 ms/0.41 ms
2-1	TI reserved	rw	0	
0	SLDENDTH[2]	rw	0	Sled end detection sensibility setting. Detection threshold for motor BEMF SLDENDTH[2:0] 000: 46 mV 010: 82 mV 011: 22 mV 100: 125 mV 101: 105 mV 111: 145 mV

8.6.4.10 REG6F 8-Bit Control Register for MonitorSet (REG6F)

Figure 29. MonitorSet (REG6F)

7	6	5	4	3	2	1	0
ACTTIMER_FLT_MON	ENDDET_MON	SIF_TIMEOUTERR_MON	PWRERR_MON	TSDERR_MON	OCPERR_MON	TSDFAULT_MON	TI reserved
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. MonitorSet (REG6F) Field Descriptions

Bit	Field	Type	Default	Description
7	ACTTIMER_FLT_MON	rw	0	Assign signal to GPIO pin 1: ACTTIMER fault output to GPOUT pin
6	ENDDET_MON	rw	0	Assign signal to GPIO pin 1: ENDDET monitor output to GPOUT pin
5	SIF_TIMEOUTERR_MON	rw	0	Assign signal to GPIO pin 1: SIF timeout monitor output to GPOUT pin
4	PWRERR_MON	rw	0	Assign signal to GPIO pin 1: PWRERR monitor output to GPOUT pin
3	TSDERR_MON	rw	0	Assign signal to GPIO pin 1: TSDERR fault output to GPOUT pin
2	OCPERR_MON	rw	0	Assign signal to GPIO pin 1: OCPERR fault output to GPOUT pin
1	TSDFAULT_MON	rw	0	Assign signal to GPIO pin 1: TSDFAULT fault output to GPOUT pin
0	TI reserved	rw	0	

8.6.4.11 REG70 8-Bit Control Register for DriverEna (REG70)

Figure 30. DriverEna (REG70)

7	6	5	4	3	2	1	0
TLT_ENA	FCS_ENA	TRK_ENA	SPM_ENA	SLD_ENA	TI reserved	LOAD_ENA	XSLEEP
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. DriverEna (REG70) Field Descriptions

Bit	Field	Type	Default	Description
7	TLT_ENA	rw	0	1 : Tilt enable (with XSLEEP=1) It is reset when XMUTE changes to L.
6	FCS_ENA	rw	0	1: Focus enable (with XSLEEP=1) It is reset when XMUTE changes to L.
5	TRK_ENA	rw	0	1: Track enable (with XSLEEP=1) It is reset when XMUTE changes to L.
4	SPM_ENA	rw	0	1: Spindle enable (with XSLEEP=1) It is reset when XMUTE changes to L.
3	SLD_ENA	rw	0	1: Sled enable (with XSLEEP=1) It is reset when XMUTE changes to L.
1	LOAD_ENA	rw	0	1 : LOAD enable (with XSLEEP=1) Track (bit5:TRK_ENA) will be disabled at LOAD_ENA=1 because of sharing the DAC PWM module. Load priority is higher than TRK_ENA. It is reset when XMUTE changes to L. (with LOAD_05CH=1)
0	XSLEEP	rw	0	1: Operation mode 0 : Power save mode Charge pump enable bit when LIN3P3_DIS is 1. All driver enable bit (Bit[7:1]) change disabled and output change to Hi-Z (regardless of setting xxx_ENA bit is 1) when setting XSLEEP to 0. Therefore set 1 to XSLEEP before setting each enable bits.

8.6.4.12 REG71 8-Bit Control Register for FuncEna (REG71)

Figure 31. FuncEna (REG71)

7	6	5	4	3	2	1	0
SPM_LSMODE	ENDDET_ENA	LIN3P3_DIS	TI reserved	CSW_ON	XMUTE_NORST_CSW	TI reserved	
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. FuncEna (REG71) Field Descriptions

Bit	Field	Type	Default	Description
7	SPM_LSMODE	rw	0	0 : Spindle Normal rotation mode 1 : Light Scribe mode (slow rotation mode)
6	ENDDET_ENA	rw	0	1 : use Sled end detection enable (with SLD_ENA=1)
5	LIN3P3_DIS	rw	0	1 : disable LIN3P3 pre-driver control. This bit will be set 1 when using LINFB pin use for monitoring GPOUT signal. (with GPOUT_ENA) Also the setting one is able to reduce ICC
3	CSW_ON	rw	0	1 : CSWO enable (with XSLEEP=1) It is reset when XMUTE changes to L
2	XMUTE_NORST_CSW	rw	0	Reset option for CSW by XMUTE event 0: Reset CSW_ON bit register at XMUTE=L. 1: XMUTE status does not influence enable bit.
1-0	TI reserved	rw	0	

8.6.4.13 REG72 8-Bit Control Register for ACTCfg (REG72)

Figure 32. ACTCfg (REG72)

7	6	5	4	3	2	1	0
LOAD_O5CH_HIGH	LOADPROT_OFF	ACTPROT_OFF	ACTTEMPTH				
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. ACTCfg (REG72) Field Descriptions

Bit	Field	Type	Default	Description
7	LOAD_05CH_HIGH	rw	0	LOAD output polarity at 0.5CH (REG74h[6]=1) 0: LOADP = Low 1: LOADP = High
6	LOADPROT_OFF	rw	0	1: Load overcurrent protection OFF
5	ACTPROT_OFF	rw	0	0 : Actuator protection ON 1 : Actuator Fault monitor disable (No protection for ACT channel)
4-0	ACTTEMPTH	rw	0	Actuator thermal protection (=ACT Timer) threshold level ACT Timer Protection enable except ACTTEMPTH[4:0] = 0x00 ACTTEMPTH = 0x00 equal to ACTPROT_OFF = 1 By writing value 0x00, ACTTIMER_PROT flag is cleared.

8.6.4.14 REG73 8-Bit Control Register for Parm0 (REG73)

Figure 33. Parm0 (REG73)

7	6	5	4	3	2	1	0
SIF_TIMEOUT_TH		SLEDEND_HZTIME	SLDENDTH[1:0]		SPM_RCOM_SEL		XMUTE_NORST
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. Parm0 (REG73) Field Descriptions

Bit	Field	Type	Default	Description
7-6	SIF_TIMEOUT_TH	rw	0	Watch dog timer for Serial communication 0: disable 1: 1 ms 2: 100 µs 3: 10 µs Set SIF_TIMEOUTERR (REG7F) if communication is suspended for this time period. XRESET processing will be performed if a SIF_TIMEOUTERR occurs.
5	SLEDEND_HZTIME	rw	0	Time window for sled end detection. 0: 400 µs 1: 200 µs Caution) Need to recycle ENDDET_ENA = 0 → 1 after writing this bit.
4-3	SLDENDTH[1:0]	rw	0	Sled end detection sensibility setting. Detection threshold for motor BEMF SLDENDTH[2:0] 000: 46 mV 010: 82 mV 011: 22 mV 100: 125 mV 101: 105 mV 111: 145 mV
2-1	SPM_RCOM_SEL	rw	0	Select resistor value of spindle current sense resistor. Current limit is set as following current. 00: 890 mA; 01: 980 mA; 10: 725 mA; 11: 784 mA
0	XMUTE_NORST	rw	0	Reset driver enable bit (XXX_ENA) register at XMUTE = L. 0: Reset enable bit at XMUTE = L 1: XMUTE status does not influence enable bit.

8.6.4.15 REG74 8-Bit Control Register for OptSet (REG74)

Figure 34. OptSet (REG74)

7	6	5	4	3	2	1	0
DIFF_TLT	LOAD_05CH	RDSTAT_ON_VFCS	VSLD2_POL	LOAD_OCP_IUP	TI reserved	SOMI_HIZ	VDAC_MAPSW
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. OptSet (REG74) Field Descriptions

Bit	Field	Type	Default	Description
7	DIFF_TLT	rw	0	1 : Differential Tilt mode enable (with TLT_ENA = FCS_ENA = 1) Differential Tilt mode (DIFF_TLT = 1), DAC value setting as follows FCS_OUT = (VFCS + VTLT) × 6 / 2048 TLT_OUT = (VFCS – VTLT) × 6 / 2048 In DIFF_TLT mode (DIFF_TLT = 1), TLT_OUT should be changed after writing VFCS.
6	LOAD_05CH	rw	0	The setting of Load motor driving type. Load output changes as follow 0: Step down mode (LOAD output is controlled by DAC code, VLOAD) Use for Slot-in model or step down tray model. 1: 0.5-channel mode (LOAD is only controlled by LOAD_05CH_HIGH) Use for Tray model
5	RDSTAT_ON_VFCS	rw	0	Set Read status data (REG7F) at VFCS write command (REG02) 1: Enable Write and Read mode (Write 12-bits Focus DAC data + Read 8-bits status data)
4	VSLD2_POL	rw	0	change direction of SLED rotation
3	LOAD_OCP_IUP	rw	0	Select overcurrent protection (OCP) threshold for Load channel current 0: 250 mA 1: 425 mA
1	SOMI_HIZ	rw	0	0: SOMI line High-Z at bus idling time. 1: SOMI line Pull Down at bus idling time.
0	VDAC_MAPSW	rw	0	Selection of DAC register channel assignments (REG01~09)

8.6.4.16 REG75 8-Bit Control Register for TSD_TUP (REG75)

Figure 35. TSD_TUP (REG75)

7	6	5	4	3	2	1	0
TI reserved							TSD_TUP
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. TSD_TUP (REG75) Field Descriptions

Bit	Field	Type	Default	Description
7-1	TI reserved	rw	0	
0	TSD_TUP	rw	0	TSD temperature threshold selection (Fault/Error) 0: 135/150°C 1: 155/170°C

8.6.4.17 REG76 8-Bit Control Register for WriteEna (REG76)

Figure 36. WriteEna (REG76)

7	6	5	4	3	2	1	0
WRITE_ENABLE				TI reserved			
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. WriteEna (REG76) Field Descriptions

Bit	Field	Type	Default	Description
7	WRITE_ENABLE	rw	0	0: Register Write disable except REG76 1: Able to write all RW and W register
6-0	TI reserved	rw	0	

8.6.4.18 REG77 8-Bit Control Register for ClrReg (REG77)

Figure 37. ClrReg (REG77)

7	6	5	4	3	2	1	0
RST_INDAC	RST_REGS	RST_ERR_FLAG	TI reserved				
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. ClrReg (REG77) Field Descriptions

Bit	Field	Type	Default	Description
7	RST_INDAC	w	0	1 : Reset all 12-bit input DAC register (REG01~0B) Self clear bit
6	RST_REGS	w	0	1 : Reset all 8-bit R/W Registers (REG70h~77h, 60h-6Fh) Self clear bit
5	RST_ERR_FLAG	w	0	1 : Reset Fault Flag Latch (REG7F[5:1], REG79~REG7B) Self clear bit
4-0	TI reserved	w	0	

8.6.4.19 REG78 8-Bit Control Register for ActTemp (REG78)

Figure 38. ActTemp (REG78)

7	6	5	4	3	2	1	0
TI reserved		ACT_TIMER_PROT	ACTTEMP				
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 26. ActTemp (REG78) Field Descriptions

Bit	Field	Type	Default	Description
7-6	TI reserved	r	0	
5	ACT_TIMER_PROT	r	0	ACT timer protection flag 1: ACT Timer Protection has detected and latched. (ACTTEMP > ACTTEMPTH) This bit holds data after temperature change to low since this is a latch bit. Also driver output keep Hi-Z until setting RST_ERR_FLAG or ACTTEMPTH = 0.
4-0	ACTTEMP	r	0	An integrated value of ACT_TIMER counters at present.

8.6.4.20 REG79 8-Bit Control Register for UVLOMon (REG79)

Figure 39. UVLOMon (REG79)

7	6	5	4	3	2	1	0
TI reserved		XMUTE_DETECT	UVLO_P5V	UVLO_INT3P3	UVLO_SIOV	UVLO_1P2V	OVP_P5V
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 27. UVLOMon (REG79) Field Descriptions

Bit	Field	Type	Default	Description
7-6	TI reserved	r	0	
5	XMUTE_DETECT	r	0	XMUTE flag for detection low input. (>20 µs)(1)
4	UVLO_P5V	r	0	UVLO flag for detection low P5V supply(1)
3	UVLO_INT3P3	r	0	UVLO flag for detection low internal 3.3-V regulator(1)
2	UVLO_SIOV	r	0	UVLO flag for detection low SIOV(1)
1	UVLO_1P2V	r	0	UVLO flag for detection low LINFB(1) No detection in LIN3P3_DIS = 1
0	OVP_P5V	r	0	Overvoltage protection flag for P5Vsply(1)

(1) Latched 1 st event only. Cleared by RST_ERR_FLG (REG77)

8.6.4.21 REG7A 8-Bit Control Register for TsdMon (REG7A)

Figure 40. TsdMon (REG7A)

7	6	5	4	3	2	1	0
TI reserved	TSD_FAULT_SPM	TSD_FAULT_ACT	TI reserved		TSD_SPM	TSD_ACT	TI reserved
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. TsdMon (REG7A) Field Descriptions

Bit	Field	Type	Default	Description
7	TI reserved	r	0	
6	TSD_FAULT_SPM	r	0	Pre alert of thermal protection of Spindle block(1)
5	TSD_FAULT_ACT	r	0	Pre alert of thermal protection of Focus /Track /Tilt Sled1 /Sled2 / /Load /CSW(1)
4-3	TI reserved	r	0	
2	TSD_SPM	r	0	Thermal protection flag for Spindle (1) SPM output Hi-Z until temperature falls on release level 1: Detect (latch)
1	TSD_ACT	r	0	Thermal protection flag for Focus /Track /Tilt Sled1 /Sled2 /Load/CSW(1) Actuator output Hi-Z until temperature falls on release level 1: Detect (latch)
0	TI reserved	r	0	

(1) Cleared by RST_ERR_FLAG bit (REG77)

8.6.4.22 REG7B 8-Bit Control Register for ProtMon (REG7B)

Figure 41. ProtMon (REG7B)

7	6	5	4	3	2	1	0
TI reserved	OCP_LOAD	TI reserved	OCP_CSW	SCP_SPM	SCP_SLED	SCP_LOAD	SCP_ACT
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 29. ProtMon (REG7B) Field Descriptions

Bit	Field	Type	Default	Description
7	TI reserved	r	0	
6	OCP_LOAD	r	0	Overcurrent protection flag bit for Load channel.(1)
4	OCP_CSW	r	0	Overcurrent protection flag bit for CSW channel.(1)
3	SCP_SPM	r	0	Short-circuit protection flag bit for spindle channel.(1)
2	SCP_SLED	r	0	Short-circuit protection flag bit for sled channel.(1)
1	SCP_LOAD	r	0	Short-circuit protection flag bit for load channel.(1)
0	SCP_ACT	r	0	Short-circuit protection flag bit for Fcs/Trk/Tilt channel.(1)

(1) Cleared by RST_ERR_FLAG bit (REG77)

8.6.4.23 REG7E 8-Bit Control Register for Version (REG7E)

Figure 42. Version (REG7E)

7	6	5	4	3	2	1	0
Version							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 30. Version (REG7E) Field Descriptions

Bit	Field	Type	Default	Description
7-0	Version		X	Version[7:4] = revision number of TPIC2040 Version[3:0] = option

8.6.4.24 REG7F 8-Bit Control Register for Status (REG7F)

Figure 43. Status (REG7F)

7	6	5	4	3	2	1	0
ACTTIMER_FAULT	ENDDET	SIF_TIMEOUTERR	PWRERR	TSDERR	OCPERR	TSDFAULT	FG
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 31. Status (REG7F) Field Descriptions

Bit	Field	Type	Default	Description
7	ACTTIMER_FAULT	r	0	Status flag of ACTTIMER protection 1: Pre alert of ACTTIMER protection. It is close to the threshold level. You can get current ACTTIMER value in REG78. Both of this bit and ACT_TIMER_PROT (REG78) will be set when over the threshold.
6	ENDDET	r	0	status flag of END detection 1: end position detected (not latch bit)
5	SIF_TIMEOUTERR	r	0	error flag of serial I/F watch dog timer 1: SIF communication was interrupted, expired watch dog timer
4	PWRERR	r	0	error flag of Power 1: Voltage problem occurred, details in REG79
3	TSDERR	r	0	error flag of any over thermal protections 1: Dispatched thermal protection, details in REG7A
2	OCPERR	r	0	error flag of any over current protection 1: Dispatched OCP, details in REG7Bh
1	TSDFAULT	r	0	warning of TSD of any thermal protection 1: Detect pre thermal protection details in REG7A
0	FG	r	0	FG signal. Spindle rotation pulse for speed monitor

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

NOTE

- Operate every driver channel after 5-V power supplied and stable.
- Appropriate capacity of de-coupling capacitor is required enough value of over 10 µF due to reduce influence of PWM switching noise. And the P5V pin needs to connect a filter of 1 µF. It is effective to put bypass capacitor(about 0.1 µF) near Power pin (P5V_1, P5V_2, P5V_SPM) for PWM switching noise reduction on power and GND line.
- Much current flow to driver circuits, to consider as below matters.
  - Pattern-layout, line-impedance, and noise influence from supply line.

9.1 Application Information

9.1.1 DAC Type

TPIC2040 has seven channels of Actuator. Each channel is assigned to the most suitable DAC engine with a different type respectively. ACT(F/T/Ti) has 12-bit DAC. Upper 8 (MSB sign bit) are converted at a time in 5MHz and LSB 4 bits are output in sequence with 1.25-MHz PWM. SPIN, SLED and Load DAC has same DAC types and sampling rate with 312 kHz. All channel except SLED have x6 gain. Table 32 shows configuration of each actuator.

Table 32. DAC Type

	FCS/TRK/TLT	SLED	SPIN	LOAD
Resolution	12 bit	10 bit	12 bit	12 bit
Type	8-bit oversampling	10-bit voltage	8-bit Oversampling	8-bit Oversampling
Sampling	1.25M / 10bit 312K / 12bit		312K	312K
PWM frequency	312 kHz	About 156 kHz(variable)	156 kHz	312 kHz
Out range	±6 V	±440 mA	±6 V	±6 V
Feed back	Voltage feedback	Current feedback	Power supply compensation	Voltage feedback Shared with TRK

9.1.2 Example of 12-Bit DAC Sampling Rate for FCS/TRK/TLT

The input data is separated in the upper 8bits and the lower 4bits. Upper 8bits (MSB sign 1bit) will be put into 8bit current DAC in every 5 MHz. The lower 4bits will be put into one bit current DAC in sequence from upper to lower bit. This one bit DAC output with PWM in 1.25 MHz. At any PWM duty, 100%, 75%, 50%, 25% or 0%, will be summed in 8bit current DAC in every 1.25 MHz. Thus it takes 3.2 µs for all lower 4bits summing to PWM output. As a result, 12-bit data is sampled in every PWM cycle. Example of sampling rate for FCS/TRK/TLT is Figure 44.

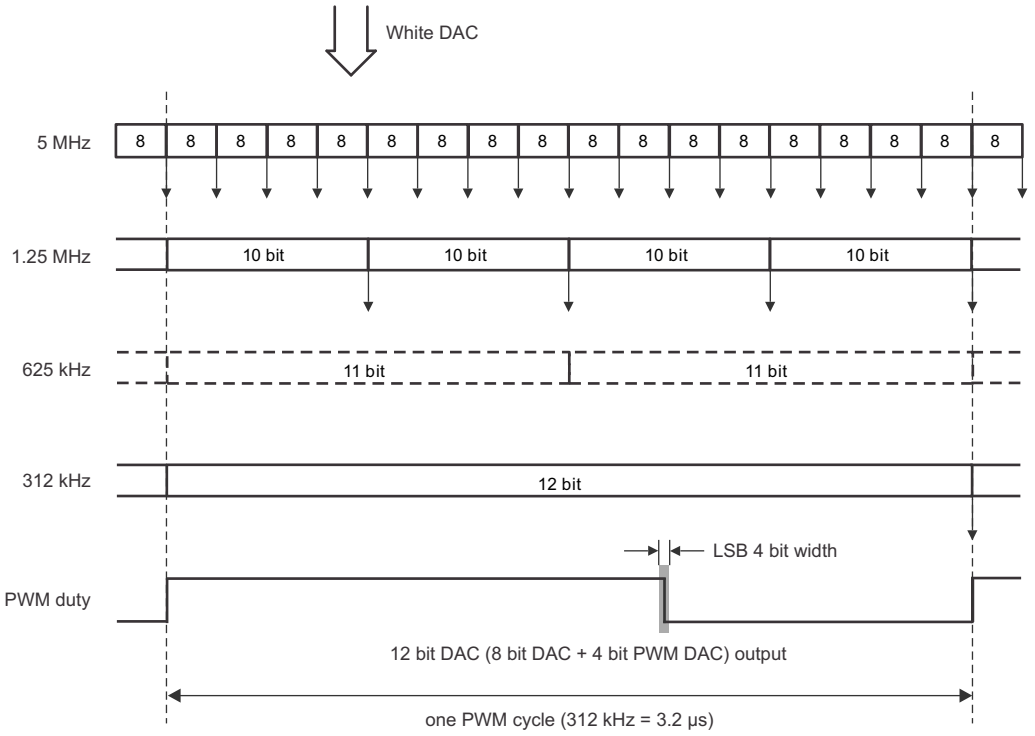


Figure 44. Example of 12-Bit DAC Conversion Time (FCS/TRK/TLT)

9.1.3 Digital Input Coding

The output voltage (current) is commanded via programming to the DAC. All of the DAC input format is 12bit in two's complement though some DAC has a low resolution. When 12 bits data is input 8 bits DAC, TPIC2040 recognizes four subordinate position bits (LSB) as 0. To arrange for 12-bit DAC format, DSP should shift 8bit or 10 bit data to an appropriate bit position. The full scale is ±1.0 V and driver gain is set 6. The output voltage *(Vout)* is given by the following equation:

$$Vout = DACcode \times \frac{6.0}{2048} \quad (1)$$

$$Vdac = 1.0 \times \left(bit[10] \times 0.5^{1} + bit[9] \times 0.5^{2} + bit[8] \times 0.5^{3} + \ldots + bit[0] \times 0.5^{11}\right)$$

$$Vdac = (-1.0) \times \left(bit[10] \times 0.5^{1} + bit[9] \times 0.5^{2} + bit[8] \times 0.5^{3} + \ldots + bit[0] \times 0.5^{11} + 0.5^{12}\right)$$

$$Vout = Vdac \times 6.0\ (V)$$

$$SLEDIout = Vdac \times 0.44\ (A)$$

where

- bit[11:0] is the digital input value, range 000000000000b to 111111111111b. (2)

Table 33. DAC Format

MSB DIGITAL INPUT (BIN) LSB	HEX	DEC	VDAC	ANALOG OUTPUT
1000_0000_0000	0x800	-2048	-0.9995	-5.997
1000_0000_0001	0x801	-2047	-0.9995	-5.997
1111_1111_1111	0xFFF	-1	-0.0005	-0.003
0000_0000_0000	0x000	0	0	0.000
0000_0000_0001	0x001	+1	+0.0005	+0.003
0111_1111_1110	0x7FE	+2046	+0.9990	+5.994
0111_1111_1111	0x7FF	+2047	+0.9995	+5.997

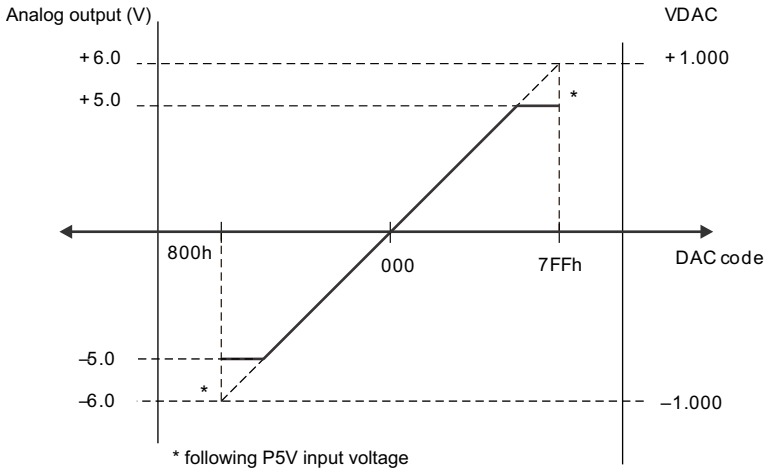


Figure 45. Output Voltage vs DAC Code

9.1.4 Example Timing of Target Control System

TPIC2040 is designed for that meets the requirements updating control data in 400 kHz. The example of control system parameter is listed in Table 34. It takes 0.51 µs for transmit a 16bit data packet to TPIC2040 with 35MHz SCLK. Therefore, DSP can be sent four packets a 400-kHz interval. If SCLK is lower than 28.8MHz, it is required reducing packet quantity under three. For example, Focus/Truck command is updating in every 2.5 µs (400 kHz), and it is able to send another two kind of packet in this same slot. Figure 10 Example DAC control shows the example of the control timing when TPIC2040 is used.

Table 34. Example Timing of Target Control System

SIGNAL	BIT	UPDATE CYCLE (kHz)
Focus	12	400
Track	12	400
Tilt	12	200
Sled1	10	100
Sled2	10	100
Spindle	12	100
Load	12	—

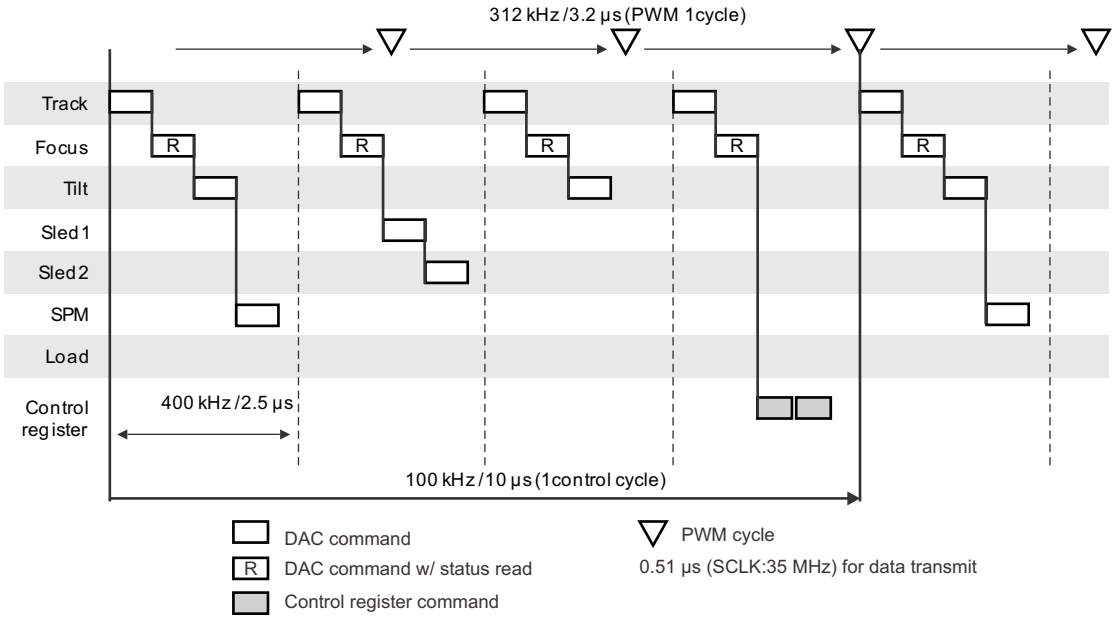


Figure 46. Example DAC Control

9.1.5 Spindle Motor Driver Part

When VSPM is set a positive DAC code then it will be into acceleration mode. IS mode operates then the start-up circuit offers the special start-up pattern sequence to the driver in start-up, and then switches to spin-up mode by detecting the rotor position by BEMF signal from the spindle motor coil.

The spin-down and brake function also be controlled by VSPM DAC value. When it is set the brake command to VSPM, driver goes into active-brake mode, then switch to short-brake mode in slow revolution speed, and then stop automatically. The FG signal is composed from EXOR of three-phase signal, and is output from XFG pin as shown in Figure 47.

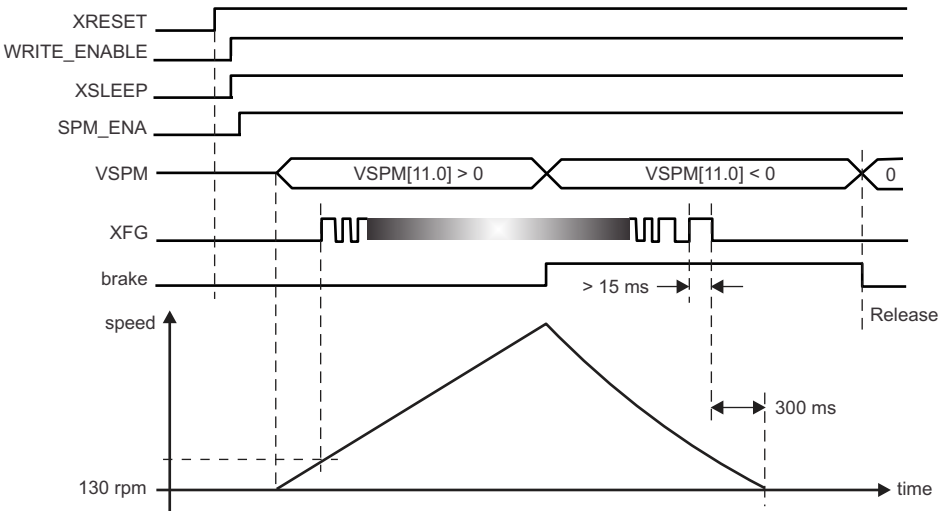


Figure 47. Spindle Operating Sequence

- TI recommends to use down-edge of FG signal for monitoring FG frequency. The FG terminal needs to be pulled up to the appropriate supply voltage by external resistor.
- Short brake mode is asserted after 300 ms of FG signal stays L-level in deceleration.
- The FG output is set to H-level in sleep mode in order to reduce sleep mode current.
- This value is the nominal number of using motor with 16-poles.

- First of all, power supply voltage of P5V must be supplied before any signals input.

9.1.5.1 Spindle PWM Control

The output PWM duty of Spindle is controlled by DAC code (VSPM). The gain in acceleration setting is always six times. However, the maximum output is restricted to P5V_SPM voltage. A dead band which output = 0 exists in the width of plus or minus 0x52 focusing on zero.

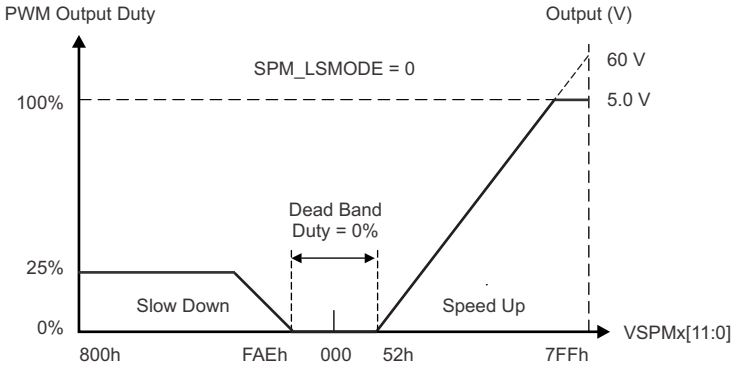


Figure 48. Spindle PWM Control

9.1.5.2 Auto Short Brake Function

TPIC2040 provides auto short brake function which is selecting brake mode automatically by motor speed.

Auto Short Brake is the intelligent brake function that includes two modes: short brake and active brake.

When VSPM value is controlled more than equivalent 75% duty brake, deceleration is done by short brake under the rotation speed is over 3000 rpm. After deceleration, driver goes into Active-brake mode automatically by internal logic circuit under rotation speed is lower 2000 rpm. This function enables low power consumption and silent during braking.

Table 35. Brake Mode

VSPM[11:0]	ROTATION SPEED (RPM)	
	ABOUT 0 TO 2000	ABOUT 3000
0x000 - 0xFAE	2-phase short brake	2-phase short brake
0xFAE - 0xA00	Active brake	Active brake
0xA00 - 0x800	Active brake	3-phase short brake

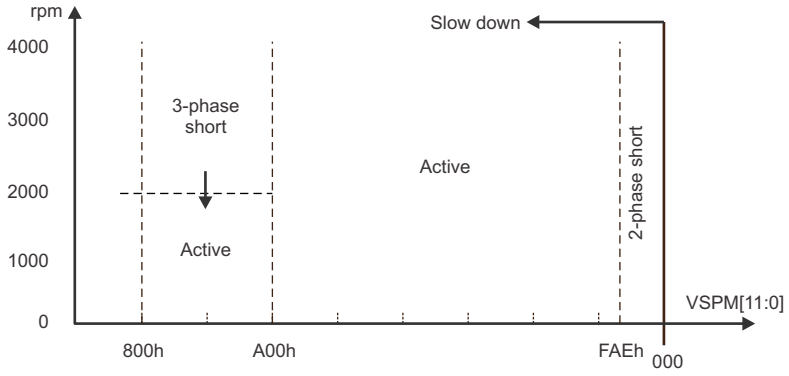


Figure 49. Brake Mode Selections

This value is the nominal number of using motor with 16-poles motor.

9.1.5.3 Spindle Low-Speed Mode

LS mode is the low rotation mode which made the maximum 25% duty. When using SPM_LSMODE = 1, brake mode is always short brake. Figure 50 shows the output duty of LS mode.

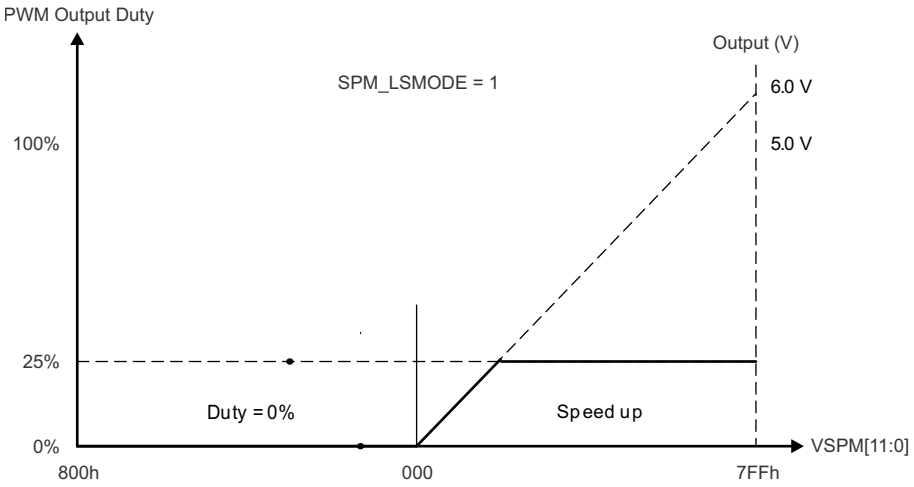


Figure 50. Spindle PWM Control (Low-Speed Mode)

9.1.5.4 Spindle Driver Current Limit Circuit

This IC builds in the SPM current sense resistor which can select resistor value.

The spindle current limit circuit monitors motor current which flows through this resistance, and limits the output current by reducing PWM duty when detecting over current conditions. Table 36 shows resistor value.

A limit current value can be calculated from following formulas.

Limit current = 196 mV / resistor value (3)

Table 36. SPM Current Sense Resistor

SPM_RCOM_SEL[1:0]	RESISTOR VALUE (Ω)	LIMIT CURRENT (mA)
00	0.22	890
01	0.20	980
10	0.27	725
11	0.25	784

9.1.6 Sled Driver Part

9.1.6.1 Sled Channel Input versus Output PWM Duty

The Sled driver outputs the PWM pulse set as DAC code (VSLDx) with current feed back. The maximum output is restricted to 440 mA at 0x7FF and 0x800. A dead band which output = 0 exists in the width of plus or minus focusing on zero.

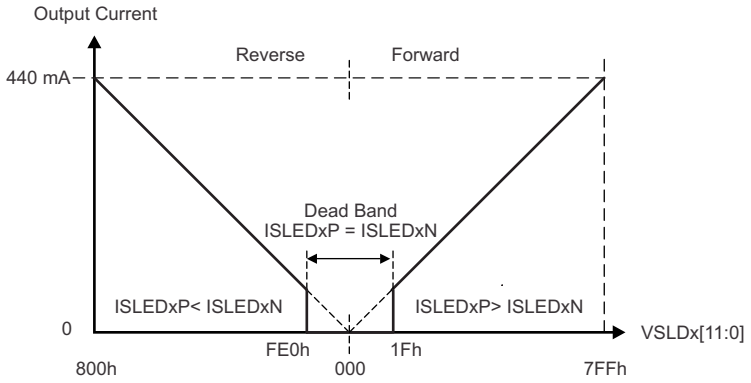


Figure 51. Sled Output Current

- Both outputs of SLED1/2 are L when input code is in dead band.

9.1.6.2 Sled End Detect Function

This device has the function of end position detection for Sled. By this function aim to eliminate the position switch at PUH inner. When this function is enabled, internal logic will detect the sled out zero-cross point and at that time, internal BEMF detect circuit measures the BEMF level of stepping motor. There are six threshold levels. If BEMF is lower than selected threshold, device recognizes motor at stop and ENDDET bit to 1. ENDDET bit will be cleared at the BEMF voltage exceed threshold again.

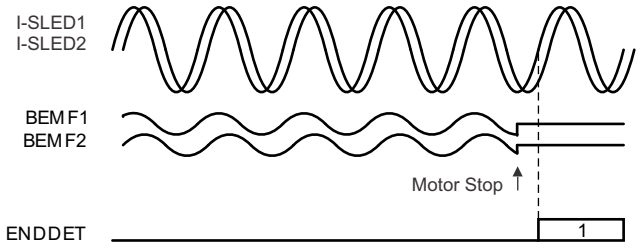


Figure 52. Timing of Sled End Detection

- In order to perform high-precision detection, the sled motor needs to generate higher BEMF voltage. BEMF level depends on the stepping motor characteristic and its speed.
- BEMF detection level is selectable 22, 46, 82, 105, 125, 145 mV.

If the drive speed changes, the timing which BEMF voltage generates will also change. In TPIC2040, detection window can be adjusted to the optimal value by setting EDET_DELAY parameter. Delay time from the point which polarity reverses and width of detection window are adjustable with EDET_DELAY.

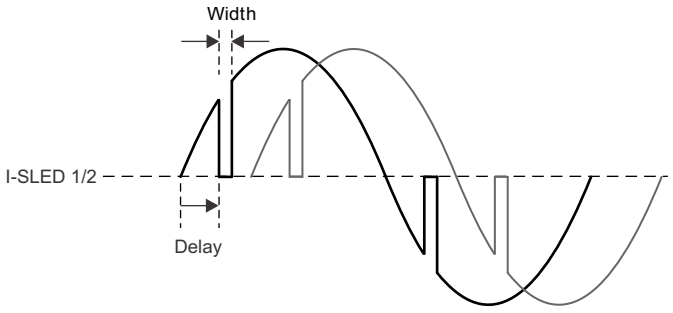


Figure 53. Timing of End Detection Window

9.1.7 Load Driver Part

Load driver outputs the voltage with voltage feedback corresponding to the input DAC value. This channel has power voltage compensation thus it is suit for Slot-in type load control. This channel becomes active exclusively to other actuator channels. Load driver is shared with the TRK driver.

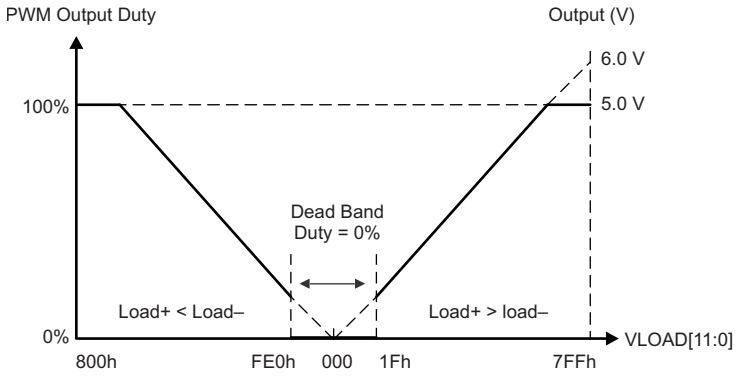


Figure 54. Load Output Duty

- Output voltage is controlled by PWM
- Both LOAD+ and LOAD– are connected to PGND through the internal clamp diode respectively.

9.1.8 Focus/Track/Tilt Driver Part

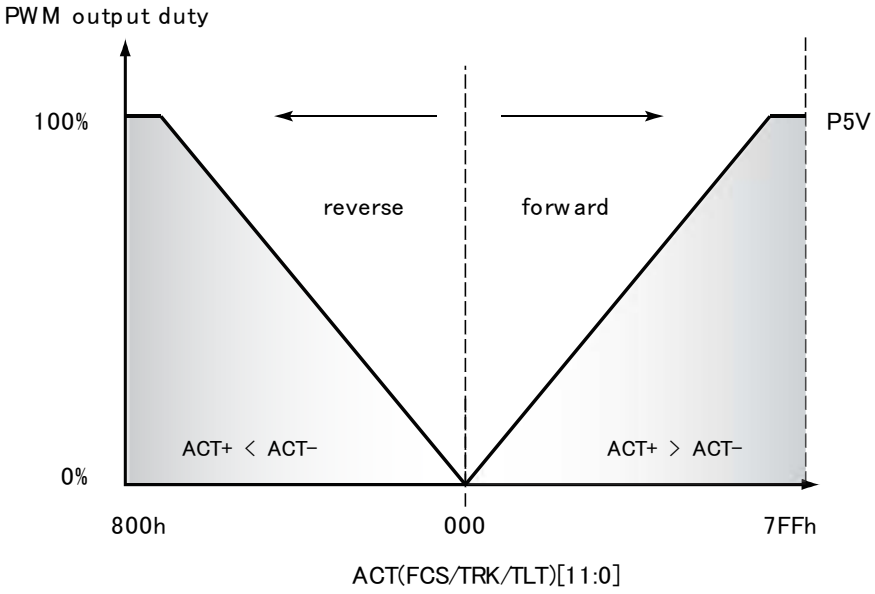


Figure 55. FCS/TRK/TLT Output Duty

9.1.8.1 Differential Tilt Mode

TPIC2040 support differential Tilt mode which output the value calculated from Focus and Tilt. Focus and Tilt can be set in differential mode by DIFF_TLT (REG74) = 1. Because Focus and Tilt are updated at the same time, the update interval of Tilt can be thinned out. Output data changes at after writing VFCS data. Therefore it is necessary to write VFCS data when set VTLT. In differential mode, the output value is calculated as follows.

$$FCS\_OUT = (VFCS + VTLT) \times 6 \quad (4)$$

$$TLT\_OUT = (VFCS – VTLT) \times 6 \quad (5)$$

9.1.9 9-V LDO

TPIC2040 built in function a pre-driver for LDO. The required voltage beyond 1.2 V can be outputted on N-channel FET by choosing external resistance. Arbitrary current can be supplied by selecting the external N-channel FET according to required current capacity. LIN3VG output (= N-channel FET gate control) is controlled to Feedback voltage LINFB is set as 1.215 V. The 22-nF capacitor for phase compensation is certainly installed. And the division resistance for FB is chosen so that it may become less than 3K in total. The example of external components shows Figure 56. The accuracy of output voltage depends for tolerance of resistance.

When not using LDO, it should be open LIN3VG and LINFB should be connected to 3.3 V with LIN3P3_DIS = 1.

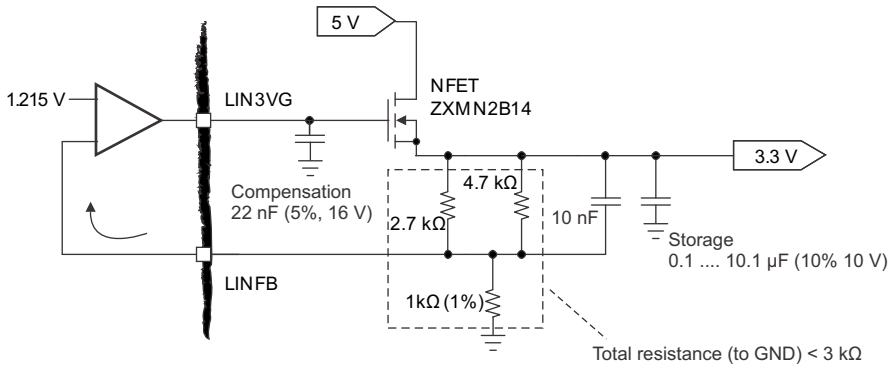


Figure 56. Example Circuit of 3.3-V LDO

9.1.10 Monitor Signal on GPOUT

Able to output a specific signal to GPOUT pin. In order to output a signal, set a signal from REG6F by enabling first and then enable GPOUT_ENA. When two or more signals are set for GPOUT, an output is as logical sum.

It is required to set both LIN3P3_DIS and GPOUT_ENA to 1.

9.2 Typical Application

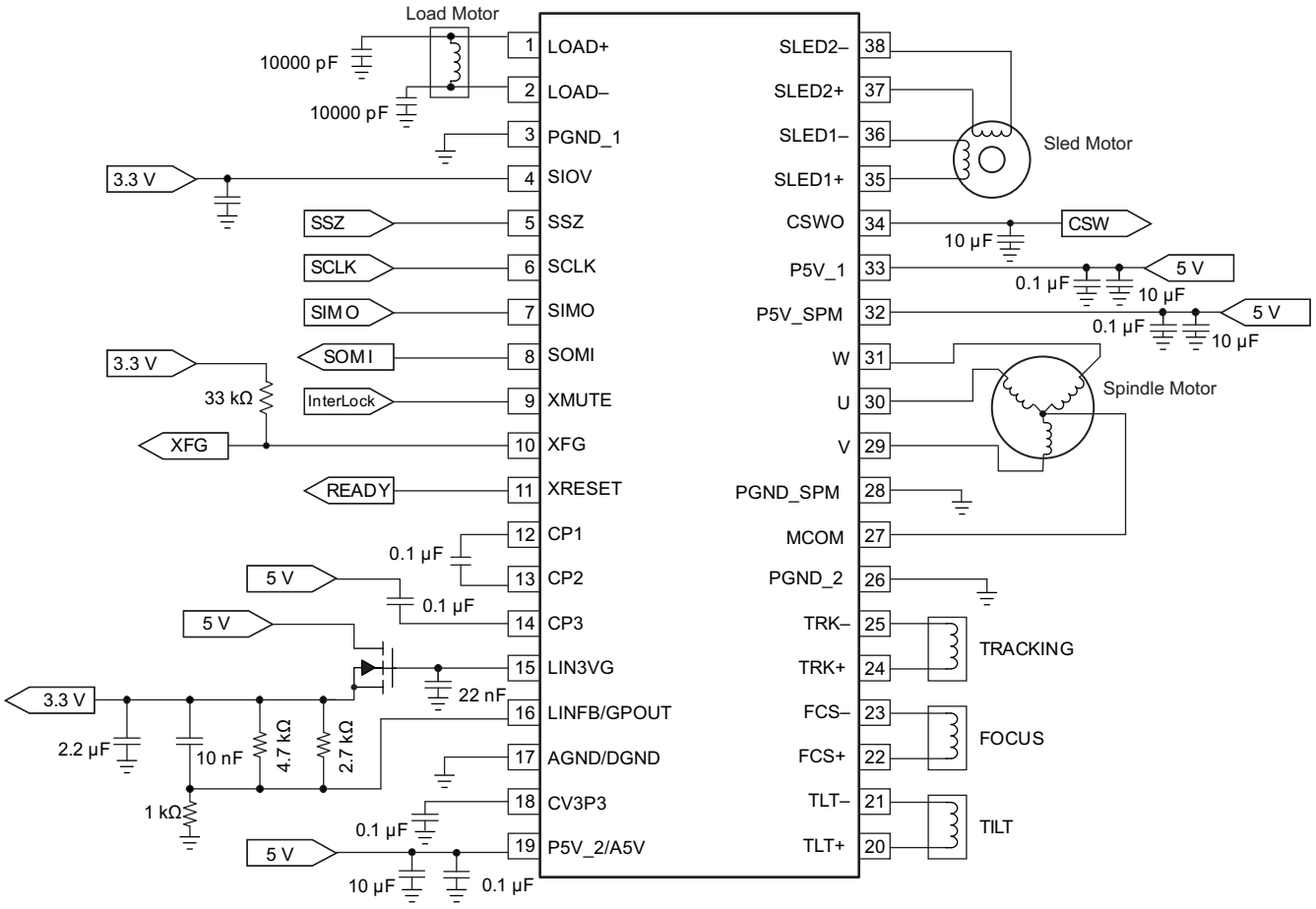


Figure 57. Example of Application Circuit

Table 37. Pin Connection When Specific Function is not Applied

FUNCTION	PIN	NUMBER	CONNECTION
LDO	LIN3VG	15	Open
	LINFB	16	3.3 V (SIOV)

9.2.1 Design Requirements

To begin the design process, determine the following:

1. Motor configuration: The user can use all motor channels or some of them.
2. Power up devices with a 5-V supply.

9.2.2 Detailed Design Procedure

After power up on 5-V supply, the following values may be written to the following registers to enable motors.

1. Set WRITE_ENABLE = 1 on REG76 via SPI.
2. Set XSLEEP = 1 at REG70
3. Enable motor channel by ENA_XXX bits on REG70
4. Change the DAC settings for each motor in REG01-0B. Then, output channels will start driving load.

Table 38. Recommended External Components

PIN	TO	FUNCTION	VALUE (RATE)	UNIT
P5V_1	PGND	Noise decoupling	10.0 (10%16 V)	µF
P5V_2	PGND	Noise decoupling	10.0 (10%16 V)	µF
P5V_SPM	PGND	Noise decoupling	10.0 (10%16 V)	µF
SIOV	PGND	Noise decoupling	1.0 (10%10 V)	µF
LOAD_P	PGND	Prevent surge current	10000(10% 16 V)	pF
LOAD_N	PGND	Prevent surge current	10000(10% 16 V)	pF
CP1	CP2	Charge pump capacitor	0.1 (10% 16 V)	µF
CP3	P5V	Charge pump capacitor (P5V only, prohibit other power supply)	0.1 (10% 16 V)	µF

9.2.3 Application Curves

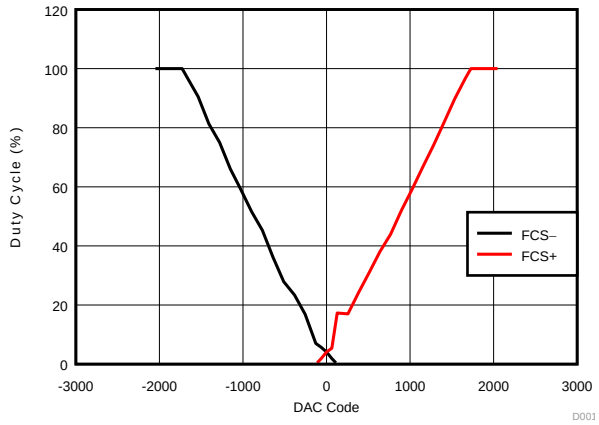


Figure 58. DAC Code vs Duty Cycle for FCS Outputs

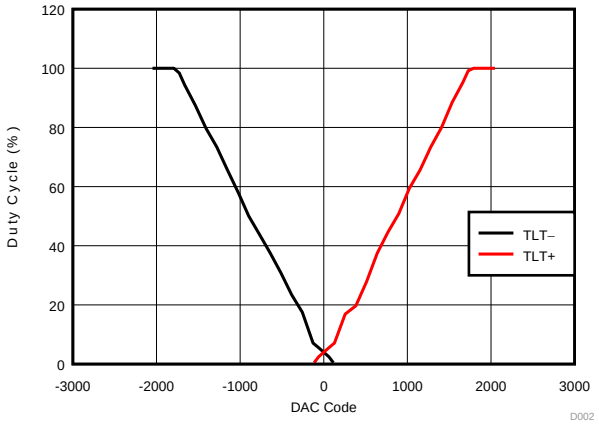


Figure 59. DAC Code vs Duty Cycle for TLT Outputs

10 Power Supply Recommendations

All driver channels should be operated after the required power is supplied and stable.

The appropriate capacity of the decoupling capacitor requires a value over 10 µF to reduce the influence of PWM switching noise. The P5V_1, P5V_2, and P5V_SPM pins must connect to 10-µF decoupling capacitors.

Current flow to the driver circuits takes both pattern-layout, line-impedance, and noise influence from the supply line into consideration.

11 Layout

11.1 Layout Guidelines

1. CV3P3V requires an external capacitor. Because these are reference voltage for device, locate the capacitor as close to device as possible. Keep away from noise sources.
2. TI recommends SCLK ground shielding.
3. LINFB is feedback pin for LDO. External divided resistors should be located closer to LINFB pin.

11.2 Layout Example

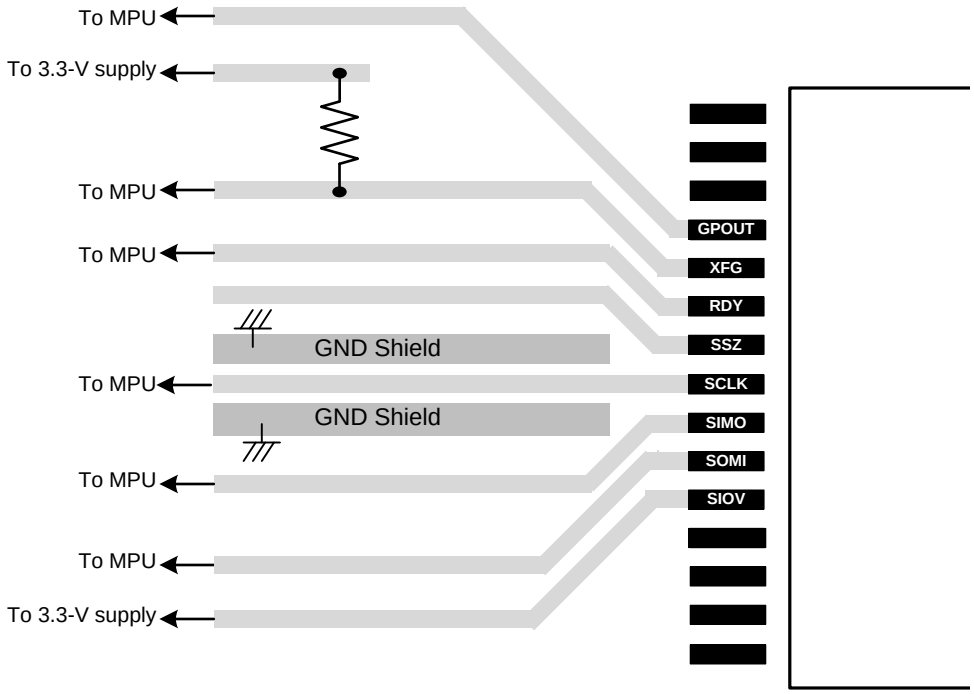


Figure 60. Layout Recommendation

12 器件和文档支持

12.1 器件支持

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12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPIC2040DBTRG4	ACTIVE	TSSOP	DBT	38	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-20 to 75	TPIC2040	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

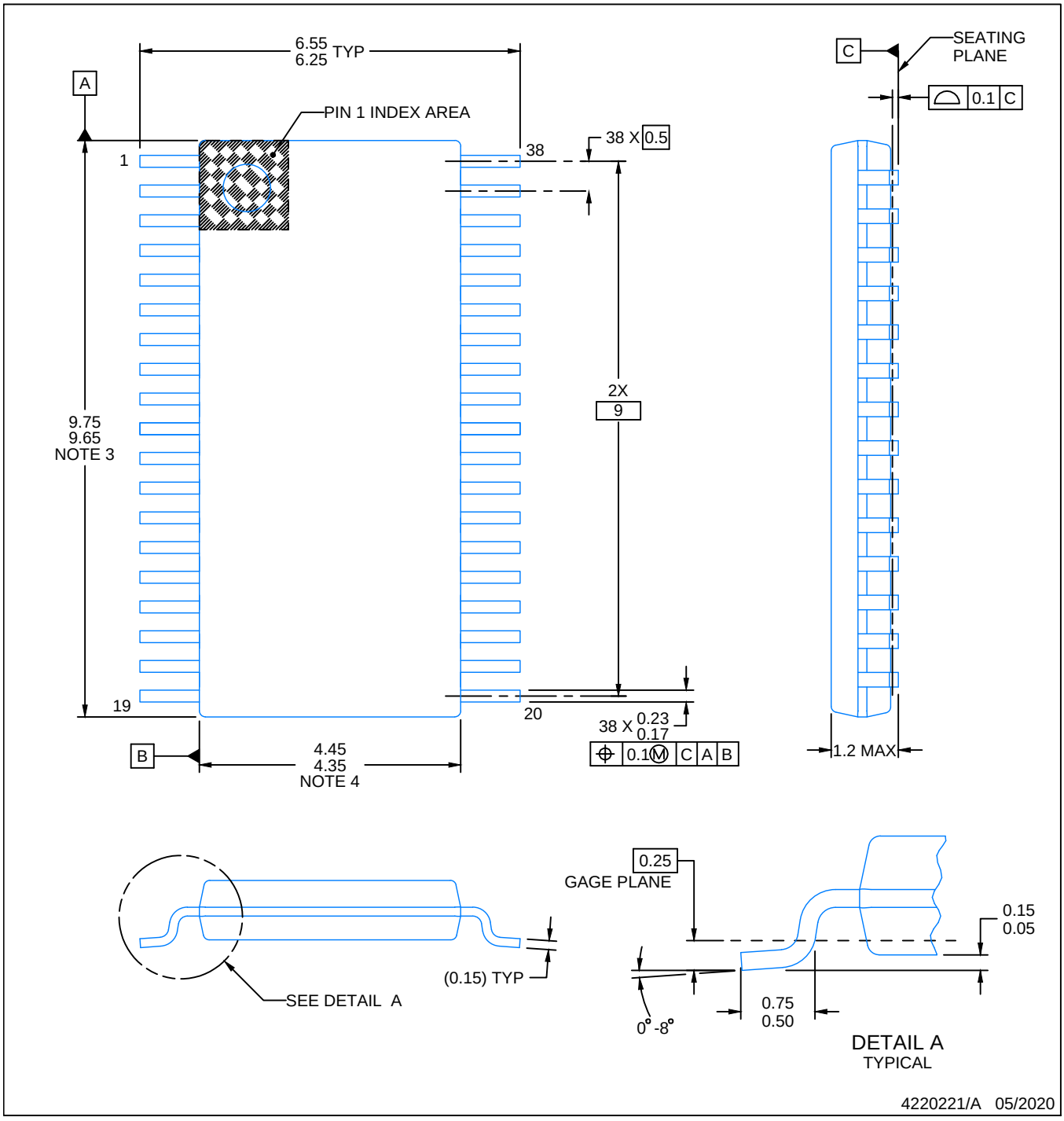
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DBT0038A

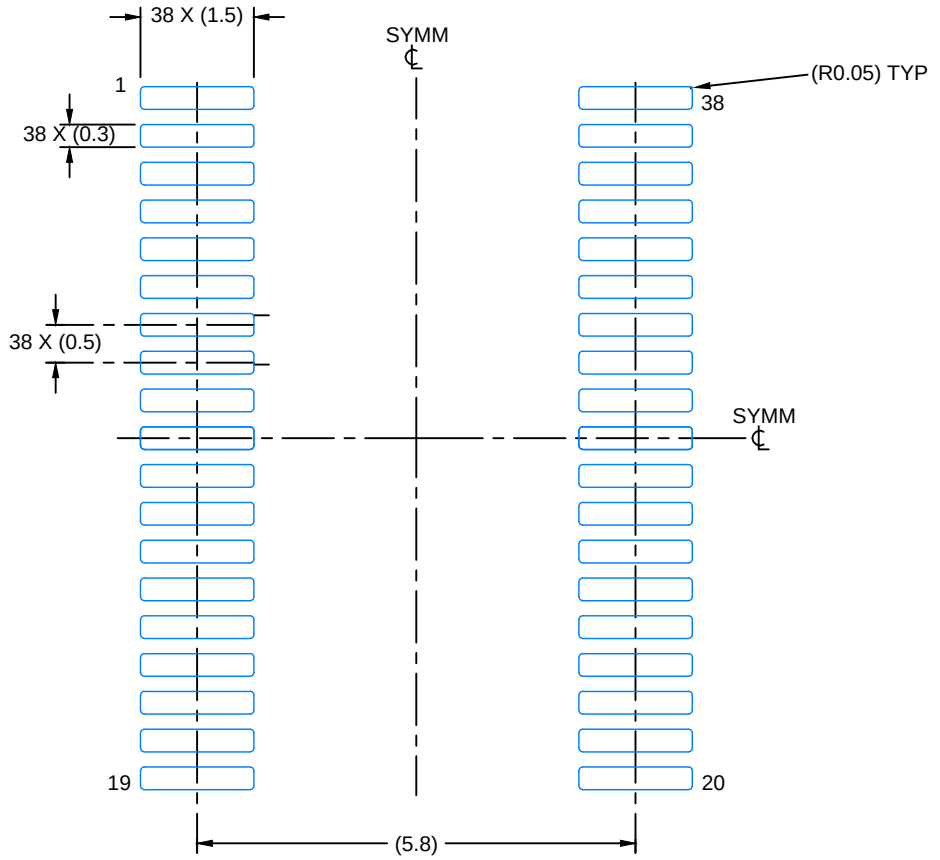
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

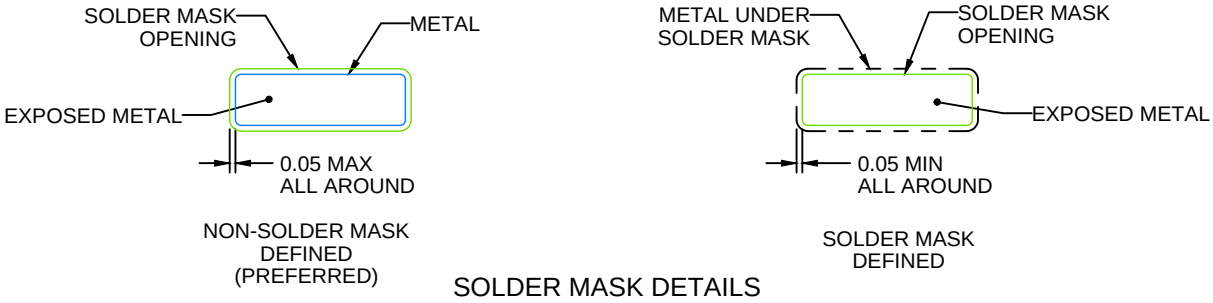


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

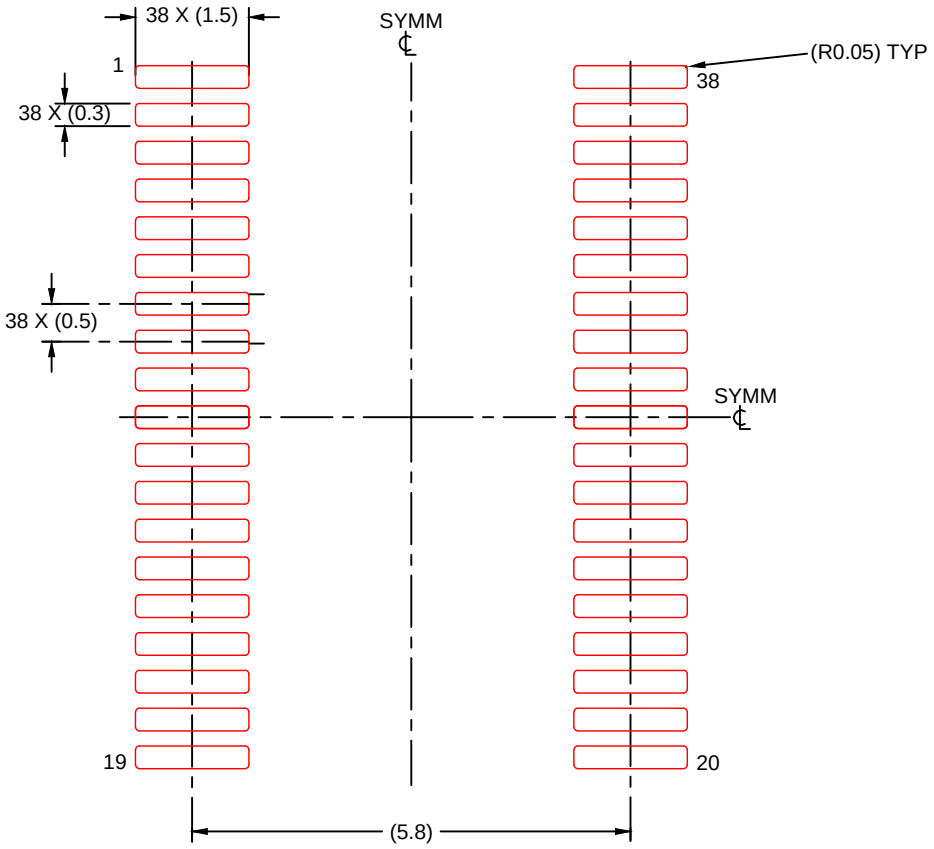


SOLDER MASK DETAILS

4220221/A 05/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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