Compact Sequential Mode RGB LED Driver with I²C Control Interface

Check for Samples: LM3435

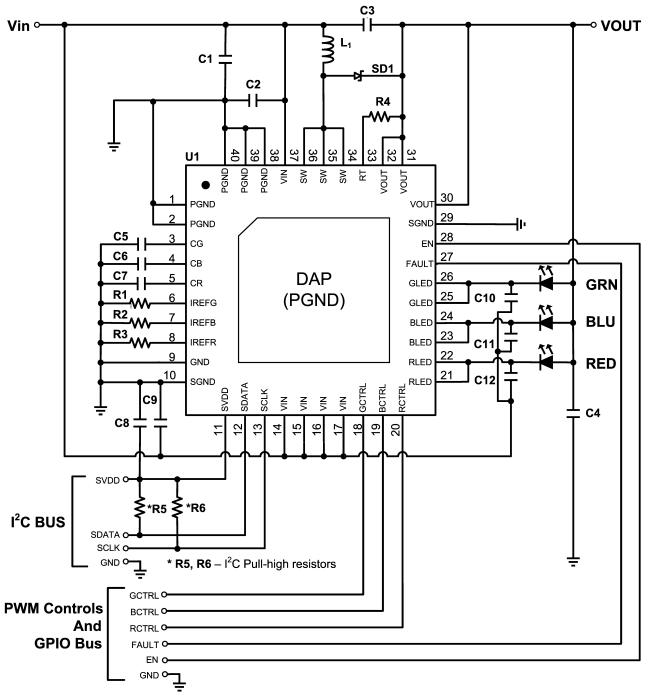
FEATURES

- **Sequential RGB Driving Mode**
- **Low Component Count and Small Solution Size**
- **Stable with Ceramic and Other Low ESR capacitors, No Loop Compensation Required**
- **Fast Transient Response**
- **Programmable Converter Switching Frequency up to 1 MHz**
- **MCU Interface Ready With I²C Bus**
- **Peak Current Limit Protection for the Switcher**
- **LED Fault Detection and Reporting via I²C Bus**

APPLICATIONS

- **Li-ion Batteries/USB Powered RGB LED Driver**
- **Pico/Pocket RGB LED Projector**

TYPICAL APPLICATION



KEY SPECIFICATIONS

- **Support up to 2A LED current**
- **Typical ±3% LED current accuracy**
- **Integrated N-Channel main and P-Channel synchronous MOSFETs**
- **3 Integrated N-Channel current regulating pass switches**
- **LED Currents programmable via I²C bus independently**
- **Input voltage range: 2.7 – 5.5 V**
- **Thermal shutdown**
- **Thermally enhanced WQFN package**

DESCRIPTION

The LM3435, a Synchronously Rectified non-isolated Flyback Converter, features all required functions to implement a highly efficient and cost effective RGB LED driver. Different from conventional Flyback converter, LEDs connect across the VOUT pin and the VIN pin through internal passing elements at corresponding LED pins. Thus, voltage across LEDs can be higher than, equal to or lower than the input supply voltage.

Load current to LEDs is up to 2A with voltage across LEDs ranging from 2.0V to 4.5V. Integrated N-Channel main MOSFET, P-Channel synchronous MOSFET and three N-Channel current regulating pass switches allow low component count, thus reducing complexity and minimize board size. The LM3435 is designed to work exceptionally well with ceramic output capacitors with low output ripple voltage. Loop compensation is not required resulting in a fast load transient response. Non-overlapping RGB LEDs are driven sequentially through individual control. Output voltage hence can be optimized for different forward voltage of LEDs during the non-overlapping period. I²C™ interface eases the programming of the individual RGB LED current up to 1,024 levels per channel.

The LM3435 is available in the thermally enhanced 40-pin WQFN package.

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CONNECTION DIAGRAM

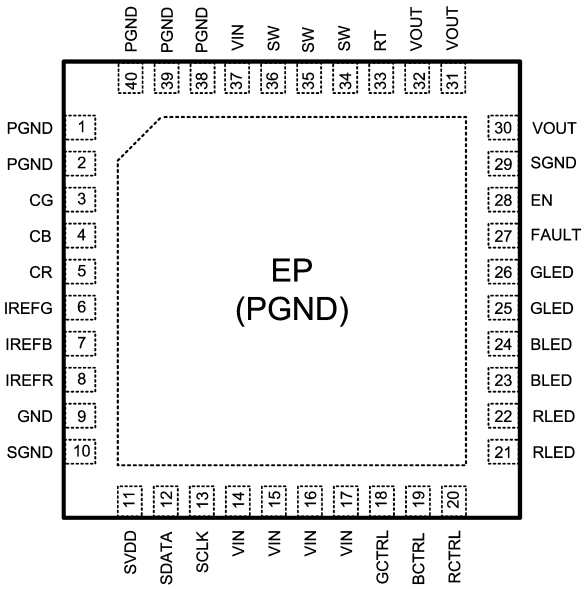


Figure 1. Top View
40-Pin WQFN
See RSB0040A Package

Pin Descriptions

Pin	Name	Type	Description	Application Information
1, 2, 38, 39, 40	PGND	Ground	Power Ground	Ground for power devices, connect to GND.
3	CG	Output	GREEN LED capacitor	Connect a capacitor to Ground for GREEN LED. Minimum 1nF.
4	CB	Output	BLUE LED capacitor	Connect a capacitor to Ground for BLUE LED. Minimum 1nF.
5	CR	Output	RED LED capacitor	Connect a capacitor to Ground for RED LED. Minimum 1nF.
6	IREFG	Output	Current Reference for GREEN LED	Connect a resistor to Ground for GREEN LED current reference generation.
7	IREFB	Output	Current Reference for BLUE LED	Connect a resistor to Ground for BLUE LED current reference generation.
8	IREFR	Output	Current Reference for RED LED	Connect a resistor to Ground for RED LED current reference generation.
9	GND	Ground	Ground	
10, 29	SGND	Ground	I^2C Ground	Ground for I^2C control, connect to GND.
11	SVDD	Power	I^2C VDD	VDD for I^2C control.
12	SDATA	Input / Output	DATA bus	Data bus for I^2C control.
13	SCLK	Input	CLOCK bus	Clock bus for I^2C control.
14, 15, 16, 17, 37	VIN	Power	Input supply voltage	Supply pin to the device. Nominal input range is 2.7V to 5.5V.
18	GCTRL	Input	GREEN LED control	On/Off control signal for GREEN LED. Internally pull-low.
19	BCTRL	Input	BLUE LED control	On/Off control signal for BLUE LED. Internally pull-low.
20	RCTRL	Input	RED LED control	On/Off control signal for RED LED. Internally pull-low.
21, 22	RLED	Output	RED LED cathode	Connect RED LED cathode to this pin.
23, 24	BLED	Output	BLUE LED cathode	Connect BLUE LED cathode to this pin.
25, 26	GLED	Output	GREEN LED cathode	Connect GREED LED cathode to this pin.
27	FAULT	Output	Fault indicator	Pull-up when LED open or short is being detected.

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Pin Descriptions (continued)

Pin	Name	Type	Description	Application Information
28	EN	Input	Enable pin	Internally pull-up. Connect to a voltage lower than 0.2 x VIN to disable the device.
30, 31, 32	VOUT	Input / Output	Output voltage	Connect anodes of LEDs to this pin.
33	RT	Input	ON-time control	An external resistor connected from VOUT to this pin sets the main MOSFET on-time, hence determine the switching frequency.
34, 35, 36	SW	Output	Switch node	Internally connected to the drain of the main N-channel MOSFET and the P-channel synchronous MOSFET. Connect to the output inductor.
EP	EP	Ground	Exposed Pad	Thermal connection pad, connect to the GND pin.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)

		VALUE / INPUTS
VIN to GND		–0.3V to 6.0V
VOUT, RT to VIN		–0.3V to 5.5V
RLED, GLED, BLED to VIN		–0.3V to 5.5V
SW to GND		–0.3V to 11.5V
SW to GND (Transient)		–2V to 13V (<100 ns)
All other inputs to GND		–0.3V to 6.0V
ESD Rating	Human Body Model (2)	±1.5 kV
Storage Temperature		–65°C to +150°C
Junction Temperature (T_J)		–40°C to +125°C

(1) Absolute Maximum Ratings are limits which damage to the device may occur. Operating ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the electrical characteristics.
(2) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

RECOMMENDED OPERATING CONDITIONS (1)

	VALUE / INPUTS
Supply Voltage Range (V_{IN})	2.7V to 5.5V
Junction Temp. Range (T_J)	–40°C to +125°C
Thermal Resistance (θ_{JB})(2)	28°C/W

(1) Absolute Maximum Ratings are limits which damage to the device may occur. Operating ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the electrical characteristics.
(2) θ_{JB} is junction-to-board thermal characteristic parameter. For packages with exposed pad, θ_{JB} is significantly dependent on PC boards. So, only when the PC board under end-user environments is similar to the 2L JEDEC board, the corresponding θ_{JB} can be used to predict the junction temperature. θ_{JB} value is obtained by NS Thermal Calculator© for reference only.

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ELECTRICAL CHARACTERISTICS

Specification with standard type are for $T_A = T_J = +25°C$ only; limits in **boldface** type apply over the full Operating Junction Temperature (T_J) range. Minimum and Maximum are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J = +25°C$, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_{IN} = 5V$ and $V_{OUT} – V_{IN} = 3V$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Supply Characteristics						
I_{IN}	I_{IN} operating current	No switching		5	**10**	mA
I_{IN-SD}	I_{IN} Shutdown current	$V_{EN} = 0V$		8	**30**	µA
I_{SVDD}	SVDD standby supply current	$V_{SVDD} = 5V$, I^2C Bus idle			**1**	µA
V_{INUVLO}	V_{IN} under-voltage lock-out	V_{IN} decreasing	**2.5**			V
V_{INUVLO_hys}	V_{IN} under-voltage lock-out hysteresis	V_{IN} increasing		0.2		V
Enable Input						
V_{EN}	EN Pin input threshold	V_{EN} rising	**0.8 x VIN**			V
		V_{EN} falling			**0.2 x VIN**	V
I_{EN}	Enable Pull-up Current	$V_{EN} = 0V$		5		µA
Logic Inputs (RCTRL, GCTRL and BCTRL)						
V_{CTRL}	CTRL pins input threshold	V_{CTRL} rising (V_{IN} = 2.7V to 5.5V)	**1.35**			V
		V_{CTRL} falling (V_{IN} = 2.7V to 5.5V)			**0.63**	
Switching Characteristics						
$R_{DS-M-ON}$	Main MOSFET $R_{DS(ON)}$	$V_{GS(MAIN)} = V_{IN} = 5.0V$, $I_{SW(sink)} = 100mA$		0.04	**0.1**	Ω
$R_{DS-S-ON}$	Syn. MOSFET $R_{DS(ON)}$	$V_{GS(SYN)} = V_{OUT} - 5.0V$, $I_{SW(source)} = 100mA$		0.06	**0.2**	Ω
Current Limit						
I_{CL}	Peak current limit through main MOSFET threshold			6	**8.5**	A
ON/OFF Timer						
t_{ON}	ON timer pulse width	$R_{RT} = 499 kΩ$		750		ns
t_{ON-MIN}	ON timer minimum pulse width			80		ns
t_{OFF}	OFF timer minimum pulse width			155		ns
RGB Driver Characteristics (RLED, BLED and GLED)						
$R_{DS(RED)}$	Red LED Switch R_{DS}	$V_{OUT} - V_{IN} = 3.3V$, $I_{LED} = 1.5A$, I^2C code = 3FFh		0.1	**0.2**	Ω
$R_{DS(BLU)}$	Blue LED Switch R_{DS}	$V_{OUT} - V_{IN} = 3.3V$, $I_{LED} = 1.5A$, I^2C code = 3FFh		0.1	**0.2**	Ω
$R_{DS(GRN)}$	Green LED Switch R_{DS}	$V_{OUT} - V_{IN} = 3.3V$, $I_{LED} = 1.5A$, I^2C code = 3FFh		0.1	**0.2**	Ω
I_{LEDMAX}	Max. LED current(1)	VIN = 4.5V to 5.5V, 0°C ≤ T_A ≤ 50°C		2		A
$I_{1.5A,3FFh}$	Current accuracy (3FFh)	V_{IN} = 2.7V to 5.5V, R_{IREF} = 16.5 kΩ, $V_{OUT} – V_{IN}$ = 2.4V (RLED), 3.3V (GLED/BLED)	1.455	1.5	1.545	A
			1.425		**1.575**	A
$I_{1.5A,1FFh}$	Current (1FFh)			0.8		A
$I_{1.5A,001h}$	Current (001h)			1.2		mA

(1) Maximum LED current measured at V_{IN} = 4.5V to 5.5V with heat sink on top of LM3435 with no air flow at 0°C ≤ T_A ≤ 50°C. Operating conditions differ from the above is **not** ensured.

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ELECTRICAL CHARACTERISTICS (continued)

Specification with standard type are for $T_A = T_J = +25°C$ only; limits in **boldface** type apply over the full Operating Junction Temperature (T_J) range. Minimum and Maximum are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J = +25°C$, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_{IN} = 5V$ and $V_{OUT} – V_{IN} = 3V$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
FAULT Output Characteristics						
V_{OH}	Output high voltage	V_{IN} = 2.7V to 5.5V, I_{OH} = -100µA	VIN – 0.1			V
		V_{IN} = 2.7V to 5.5V, I_{OH} = -5mA	VIN – 0.5			V
V_{OL}	Output low voltage	V_{IN} = 2.7V to 5.5V, I_{OL} = 100µA			0.1	V
		V_{IN} = 2.7V to 5.5V, I_{OL} = 5mA			0.5	V
Thermal Shutdown						
T_{SD}	Thermal shutdown temperature	TJ rising		163		°C
T_{SD-HYS}	Thermal shutdown temperature hysteresis	TJ falling		20		°C
I^2C Logic Interface Electrical Characteristics (1.7 V < SVDD < V_{IN})						
Logic Inputs SCL, SDA						
V_{IL}	Input Low Level				0.2 x SVDD	V
V_{IH}	Input High Level		0.8 x SVDD			V
I_L	Logic Input Current		-1		1	µA
f_{SCL}	Clock Frequency				400	kHz
Logic Output SDA						
V_{OL}	Output Low Level	I_{SDA} = 3mA		0.3	0.5	V
I_L	Output Leakage Current	V_{SDA} = 2.8V			2	µA

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TYPICAL PERFORMANCE CHARACTERISTICS

All curves taken at VIN = 5V with configuration in typical application for driving one red (OSRAM LRW5AP-KZMX), one green (OSRAM LTW5AP-LZMY) and one blue (OSRAM LBW5AP-JYKX) LEDs with I_{OUT} per channel = 1.5A under T_A = 25°C, unless otherwise specified.

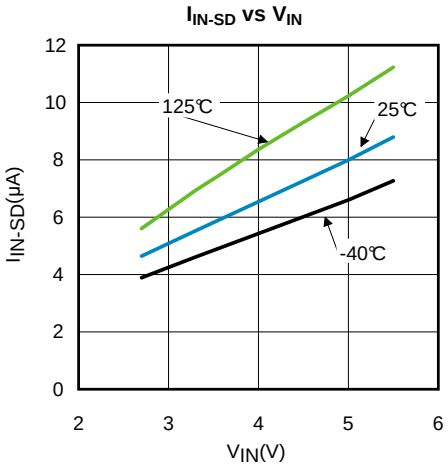


Figure 2.

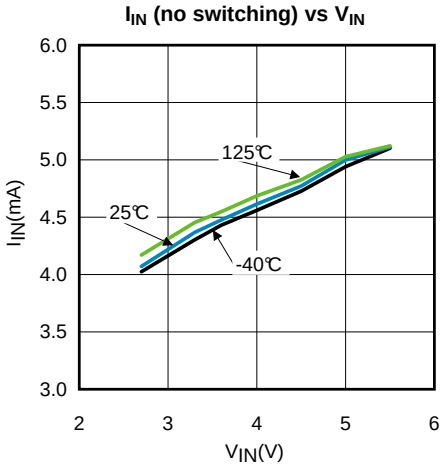


Figure 3.

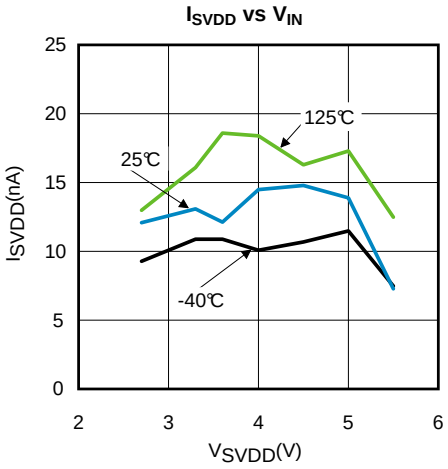


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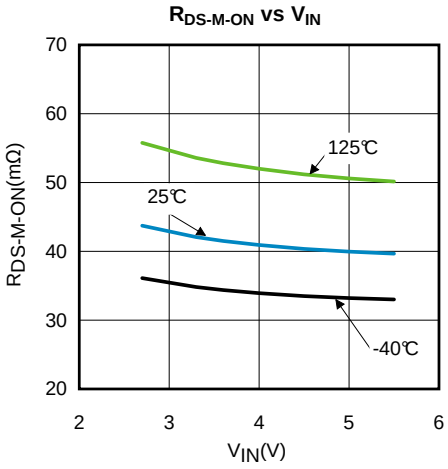


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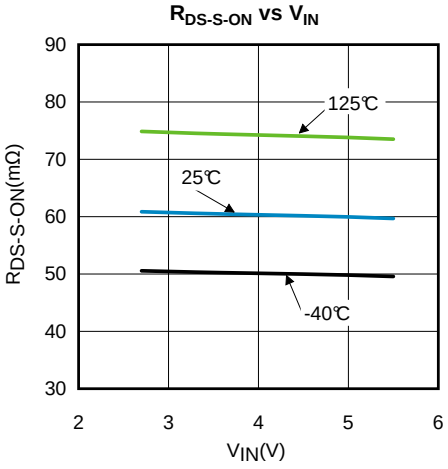


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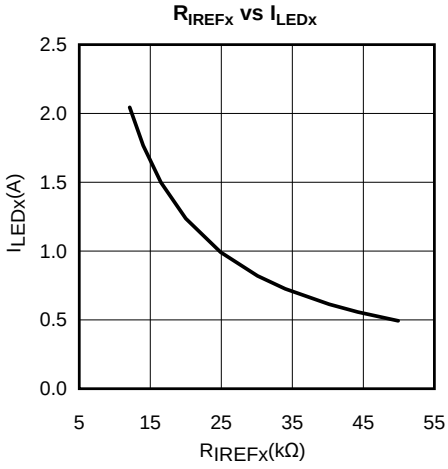


Figure 7.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

All curves taken at VIN = 5V with configuration in typical application for driving one red (OSRAM LRW5AP-KZMX), one green (OSRAM LTW5AP-LZMY) and one blue (OSRAM LBW5AP-JYKX) LEDs with I_{OUT} per channel = 1.5A under T_A = 25°C, unless otherwise specified.

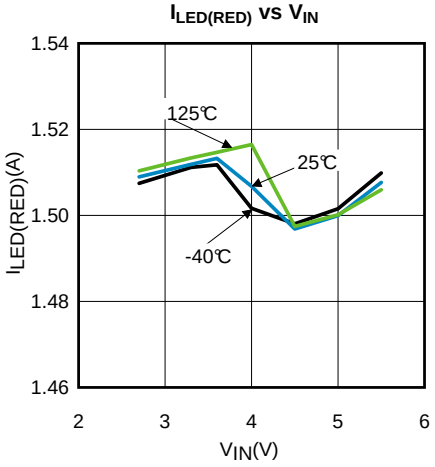


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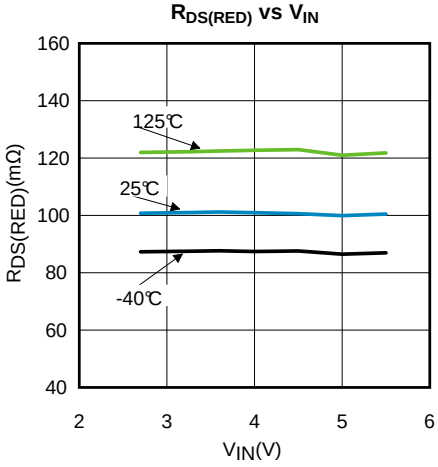


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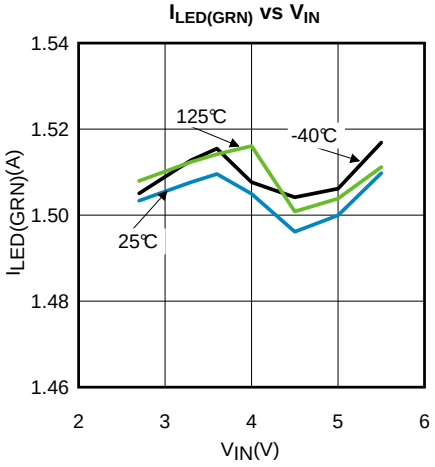


Figure 10.

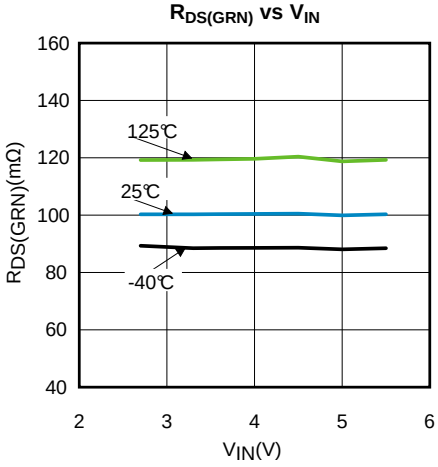


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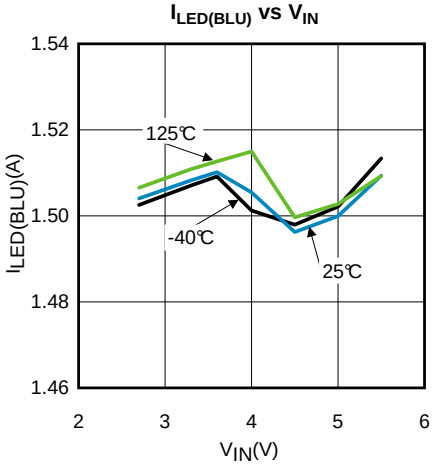


Figure 12.

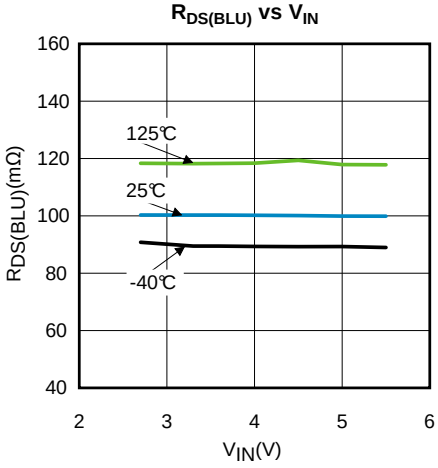


Figure 13.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

All curves taken at VIN = 5V with configuration in typical application for driving one red (OSRAM LRW5AP-KZMX), one green (OSRAM LTW5AP-LZMY) and one blue (OSRAM LBW5AP-JYKX) LEDs with I_{OUT} per channel = 1.5A under T_A = 25°C, unless otherwise specified.

RED Efficiency vs V_{IN} @ T_A = 25°C

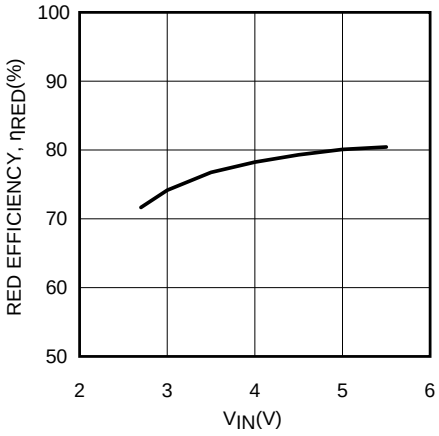


Figure 14.

GREEN Efficiency vs V_{IN} @ T_A = 25°C

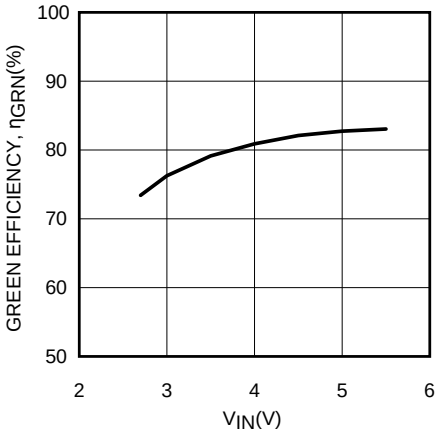


Figure 15.

BLUE Efficiency vs V_{IN} @ T_A = 25°C

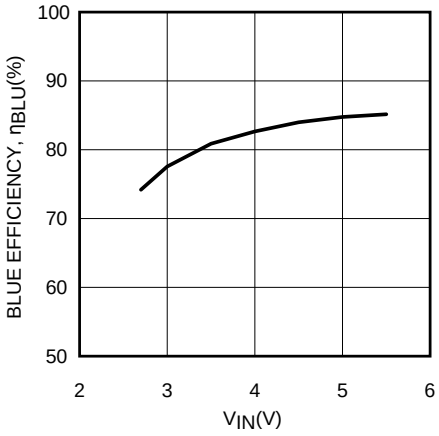


Figure 16.

Power Up Transient

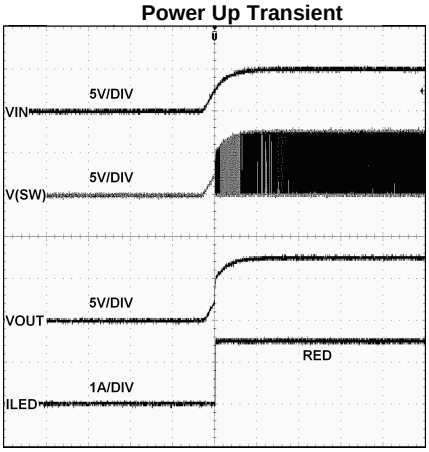


Figure 17. (10ms/DIV)

RGB Sequential Mode Operation

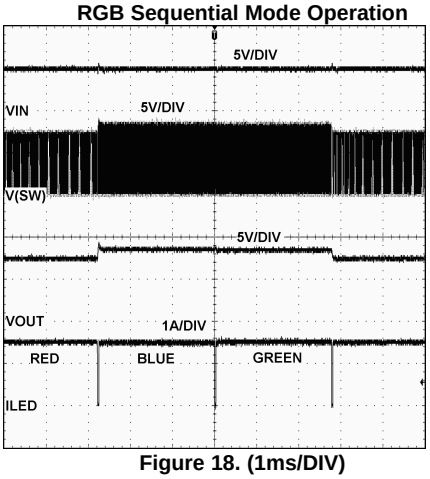


Figure 18. (1ms/DIV)

Color Transition Delay

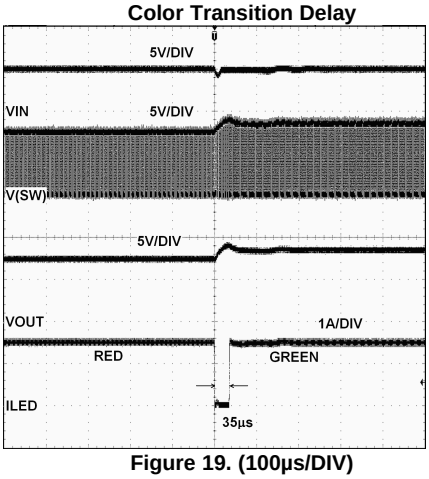
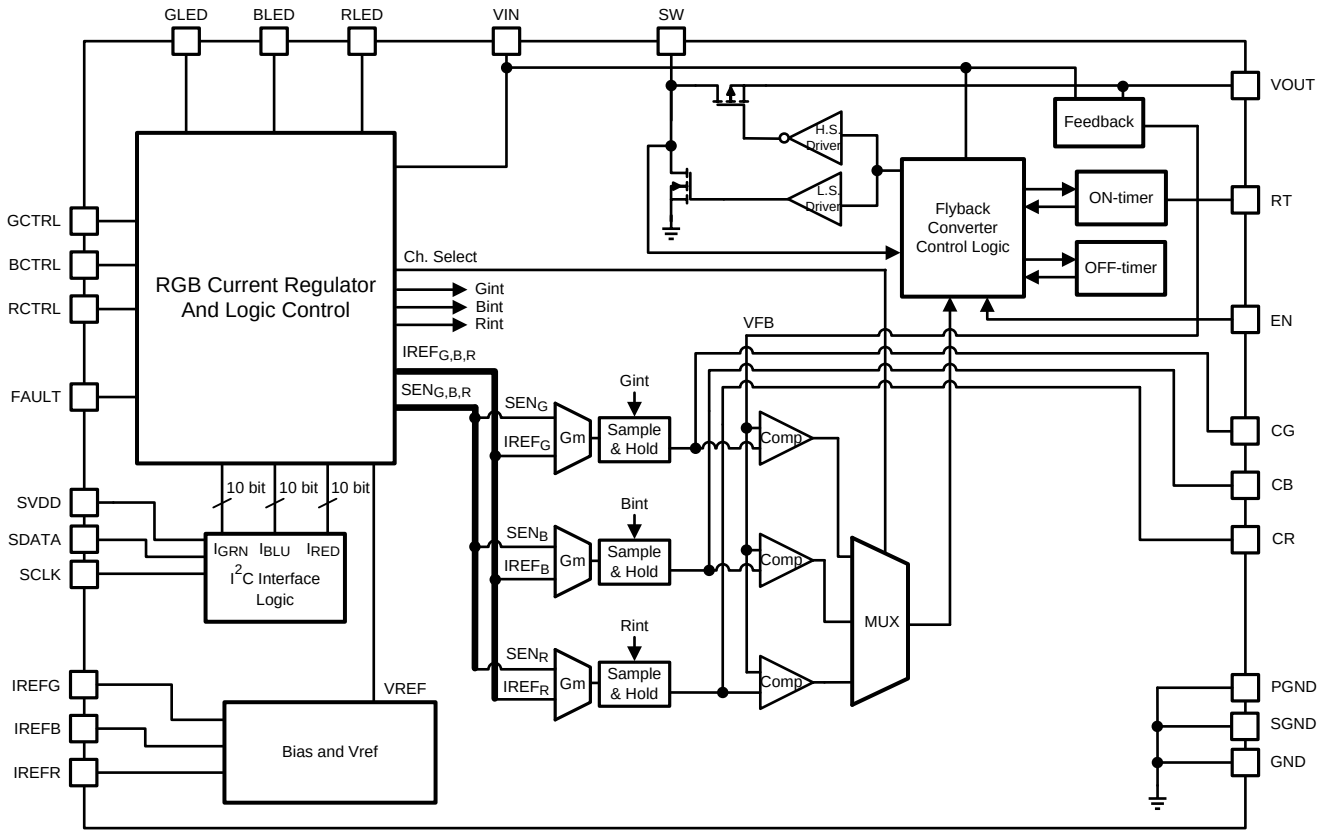


Figure 19. (100µs/DIV)

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SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



OPERATION DESCRIPTION

INTRODUCTION

The LM3435 is a sequential LED driver for portable and pico projectors. The device is integrated with three high current regulators, low side MOSFETs and a synchronous flyback DC-DC converter. Only single LED can be enabled at any given time. The DC-DC converter quickly adjusts the output voltage to an optimal level based on each LED's forward voltage. This minimizes the power dissipation at the current regulators and maximizes the system efficiency. The I^2C compatible synchronous serial interface provides access to the programmable functions and registers of the device. I^2C protocol uses a two-wire interface for bi-directional communications between the devices connected to the bus. The two interface lines are the Serial Data Line (SDA), and the Serial Clock Line (SCL). These lines should be connected to a positive supply, via a pull-up resistor and remain HIGH even when the bus is idle. Every device on the bus is assigned an unique address and acts as either a Master or a Slave depending on whether it generates or receives the serial clock (SCL).

SYNCHRONOUS FLYBACK CONVERTER

The LM3435 integrates a synchronous flyback DC-DC converter to power the three-channel current regulator. The LEDs are connected across VOUT of the flyback converter and VIN through an internal power MOSFET connecting to corresponding LED channel. The maximum current to LED is 2A and the maximum voltage across VOUT and VIN is limited at around 4.7V. The LM3435 integrates the main N-channel MOSFET, the synchronous P-channel MOSFET of the flyback converter and three N-channel MOSFETs as internal passing elements connecting to LED channels in order to minimize the solution components count and PCB space.

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The flyback converter of LM3435 employs a proprietary Projected On-Time (POT) control scheme to determine the on-time of the main N-channel MOSFET with respect to the input and output voltages together with an external switching frequency setting resistor connected to RT pin, R_{RT}. POT control use information of the current passing through R_{RT} from VOUT, voltage information of VOUT and VIN to find an appropriate on-time for the circuit operations. During the on-time period, the inductor connecting to the flyback converter is charged up and the output capacitor is discharged to supply power to the LED. A cycle-by-cycle current limit of typical 6A is imposed on the main N-channel MOSFET for protection. After the on-time period, the main N-channel MOSFET is turned off and the synchronous P-channel MOSFET is turned on in order to discharge the inductor. The off state will last until VOUT is dropped below a reference voltage. Such reference voltage is derived from the required LED current to be regulated at a particular LED channel. The flyback converter under POT control can maintain a fairly constant switching frequency that depends mainly on value of the resistor connected across VOUT and RT pins, R_{RT}. The relationship between the flyback converter switching frequency, F_{SW} and R_{RT} is approximated by the following relationship:

$$F_{SW} = \frac{2.5}{R_{RT}} \times 10^8$$

R_{RT} in Ω and F_{SW} in kHz (1)

In addition, POT control requires no external compensation and achieves fast transient response of the output voltage changes that perfectly matches the requirements of a sequential RGB LED driver. The POT flyback converter only operates at Continuous Conduction Mode. Dead-time between main MOSFET and synchronous MOSFET switching is adaptively controlled by a minimum non-overlap timer to prevent current shoot through. Initial VOUT will be regulated at around 3.2V to 3.5V above VIN before any control signals being turned on. Three small capacitors connected to CR, CG and CB pins are charged by an internal current source and act as soft-start capacitors of the flyback converter during start-up. Once initial voltage of VOUT is settled, the capacitors will be used as a memory element to store the VOUT information for each channel respectively. This information will be used for VOUT regulation of respective LED channel during channel switching. In between the channel switching, a small I^2C programmable blank out time of 5 µs to 35 µs is inserted so that the LED current is available after the correct VOUT for the color is stabilized. This control scheme ensures the minimal voltage headroom for different color LED and hence best conversion efficiency can be achieved.

HIGH CURRENT REGULATORS

The LM3435 contains three internal current regulators powered by the output of the synchronous Flyback Converter, VOUT. Three low side power MOSFETs are included. These current regulators control the current supplied to the LED channels individually and maintain accurate current regulation by internal feedback and control mechanism. The regulation is achieved by a Gm-C circuit comparing the sensing voltage of the internal passing N-channel MOSFET and an internal LED current reference voltage generated from the external reference current setting resistor, RIREFx connect to IREFG, IREFB or IREFR pin, of the corresponding LED channel. The nominal maximum LED current is governed by the equation in below:

$$I_{LEDx} = \frac{24.75}{R_{IREFx}} \times 10^3$$

R_{IREFx} in Ω and I_{LEDx} in Ampere (2)

The LED current setting can be in the range of 0.5A up to 2A maximum. The nominal maximum of the device is 1.5A and for applications need higher than 1.5A LED current, VIN and thermal constrains must be complied. The actual LED current can be adjusted on-the-fly by the internal ten bits register for individual channel. The content of these registers are user programmable via I^2C bus connection. The user can control the LED output current on-the-fly during normal operation. The resolution is 1 out of 1024 part of the LED current setting. The user can program the registers in the range of 1(001H) to 1023(3FFH) for each channel independently, provided the converter is not entered the Discontinuous Conduction Mode. Whenever the converter operation entered the Discontinuous Conduction Mode, the regulation will be deteriorated. A value of “0” may cause false fault detection, so it must be avoided.

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SEQUENTIAL MODE RGB TIMING

LM3435 is a sequential mode RGB driver dedicatedly designed for pico and portable projector applications. By using this device, the system only require one power driver stage for three color LEDs. With LM3435, only single LED can be enabled at any given time period and the DC-DC converter can quickly adjusts the output voltage to an optimized level by controlling the current flowing into the respective LED channel. This approach minimizes the power dissipation of the internal current regulator and effectively maximizes the system efficiency. Timing of the RGB LEDs depends solely on the RCTRL, GCTRL and BCTRL inputs. The Timing Chart in below shows a typical timing of two cycles of even RGB scan. In real applications, the RGB sequence is totally controlled by the system or the video processor. It's not mandatory to follow the simple RGB sequence, but for any change instructed by the I^2C control will only take place at the falling edge of the corresponding CTRL signal.

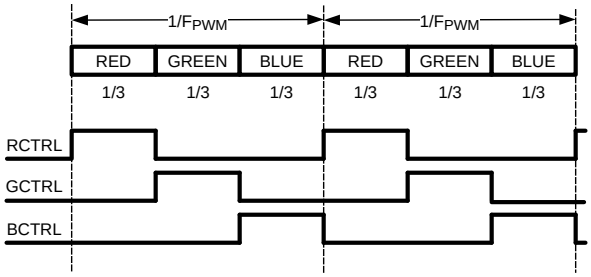


Figure 20. RGB Control Signals Timing Chart

PRIORITIES OF LED CONTROL SIGNALS

The LM3435 does not support color overlapping mode operation. At any instant, only one LED will be enabled even overlapping control signals applied to the control inputs. The decision logics of the device determine which LED channel should be enabled in case overlapping control signals are detected at the control inputs. The GREEN channel has the higher priority over BLUE channel and the RED channel has the lowest priority. However, if a low priority channel is already turned on before the high priority channel control signal comes in, the low priority channel will continue to take the control until the control signal ceased. The timing diagram in below illustrates some typical cases during operation.

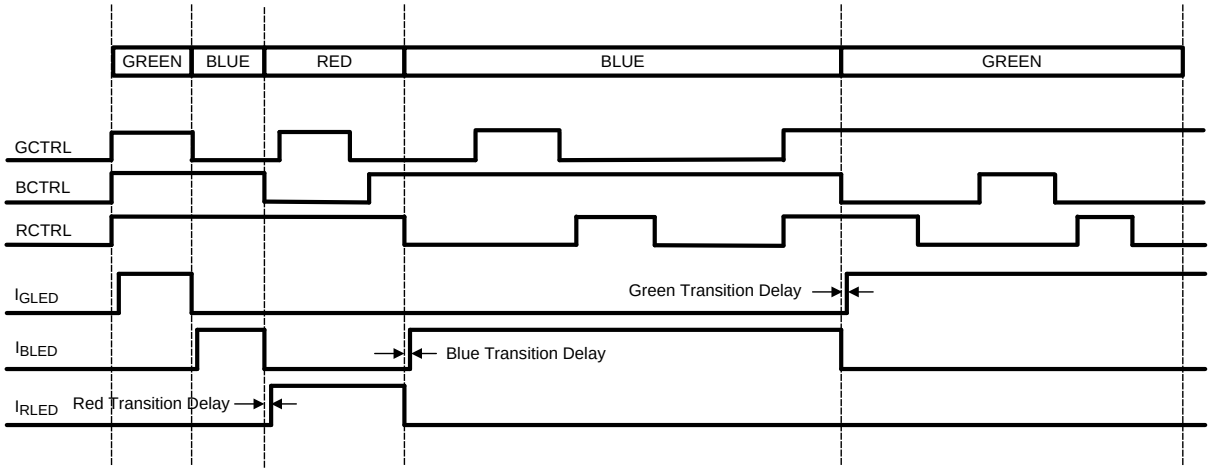


Figure 21. Priorities of LED Control Signals

LED OPEN FAULT REPORTING

The fly-back converter tries to keep VOUT to the forward voltage required by the LED with the desired LED current output. However, if the LED channel is being opened no matter it is due to LED failure or no connection, the fly-back converter will limit the VOUT voltage at around 4.7V above VIN. Once such voltage is achieved, an open-fault-suspect signal will go high. If this open-fault-suspect signal is being detected at 3 consecutive falling edges of the opened channel control signal, “Fault” pin will be latched high and the corresponding channel open fault will be reported through I^2C. The open fault report can be removed either by pulling EN pin low for less than 100ns (a true shutdown will be triggered if the negative pulse on EN is more than 100ns) or by writing a “0” to “bit 0” of the I^2C register ”05h”. The “Fault” pin will be cleared and the I^2C fault register will be reset. In order to reinstate the fault reporting feature, the system need to write a “1” to “bit 0” of the I^2C register “05h”.

LED SHORT FAULT REPORTING

If the VOUT is prohibited to regulate at a potential higher than 1.5V above VIN at a LED channel, such LED is considered being shorted and a short-fault-suspect signal will go high. If this short-fault-suspect signal is being detected at 3 consecutive falling edges of the shorted channel control signal, “Fault” pin will be latched high and the corresponding channel short fault will be reported through I^2C. The short fault report can be removed either by pulling EN pin low for less than 100ns (a true shutdown will be triggered if the negative pulse on EN is more than 100ns) or by writing a “0” to “bit 0” of the I^2C register ”05h”. The “Fault” pin will be cleared and the I^2C fault register will be reset. In order to reinstate the fault reporting feature, the system need to write a “1” to “bit 0” of the I^2C register “05h”. Persistently short of LED can cause permanent damage to the device. Whenever the short fault is detected, the system should turn off the faulty channel immediately by pulling the corresponding PWM control pin to GND.

THERMAL SHUTDOWN

Internal thermal shutdown circuitry is included to protect the device in the event that the maximum junction temperature is exceeded. The threshold for thermal shutdown in LM3435 is around 160°C and it will be resumed to normal operation again once the temperature cools down to below around 140°C.

I^2C Compatible Interface

INTERFACE BUS OVERVIEW

The I^2C compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bi-directional communications between the devices connected to the bus. The two interface lines are the Serial Data Line (SDA), and the Serial Clock Line (SCL). These lines should be connected to a positive supply, via a pull-up resistor and remain HIGH even when the bus is idle. Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the serial clock (SCL).

DATA TRANSACTIONS

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock’s high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

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I²C DATA VALIDITY

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.

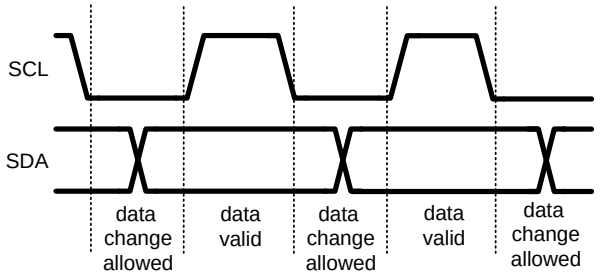


Figure 22. I²C Signals : Data Validity

I²C START and STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

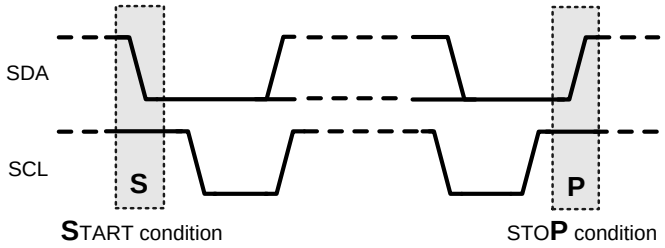


Figure 23. I²C Start and Stop Conditions

I²C ADDRESSES AND TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge bit related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledgement. A receiver which has been addressed must generate an acknowledge bit after each byte has been received. After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM3435 address is 50h or 51H which is determined by the R/W bit. **I²C address (7 bits) for LM3435 is 28H**. For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

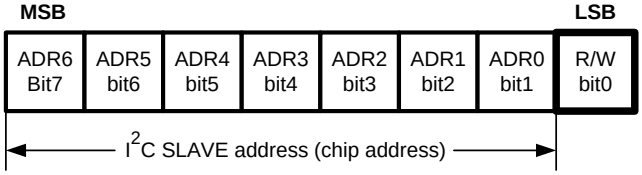
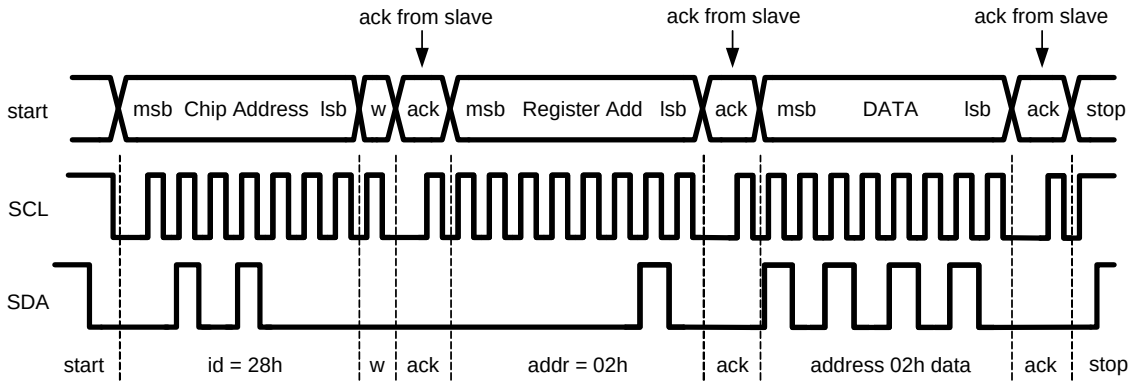


Figure 24. I²C Chip Address

Register changes take an effect at the SCL rising edge during the last ACK from slave.

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w = write (SDA = “0”)
r = read (SDA = “1”)
ack = acknowledge (SDA pulled down by either master or slave)
rs = repeated start
id = 7-bit chip address, 50H (ADDR_SEL=0) or 51H (ADDR_SEL=1) for LM3435.

Figure 25. I²C Write Cycle

When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the Read Cycle waveform.

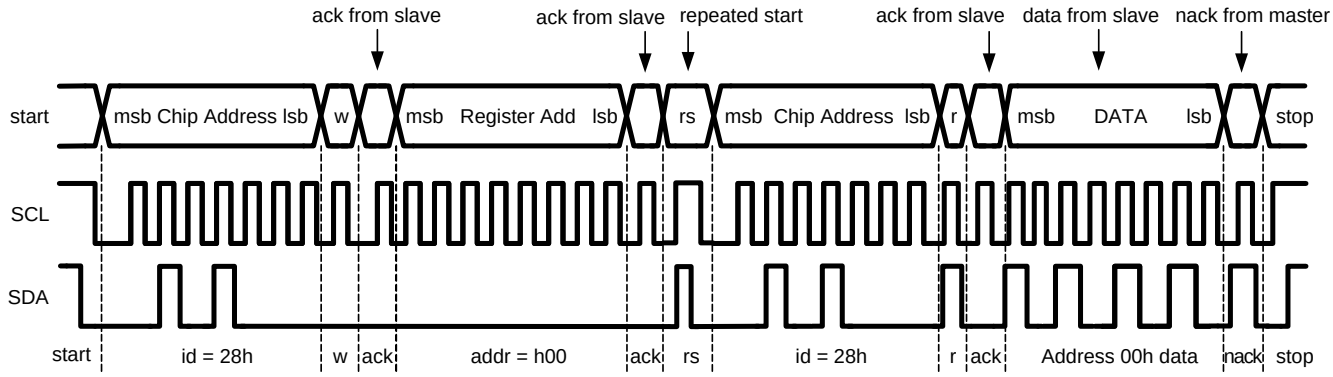


Figure 26. I²C Read Cycle

I²C TIMING PARAMETERS (V_{IN} = 2.7V to 5.5V, S_{VDD} = 1.7V to V_{IN})

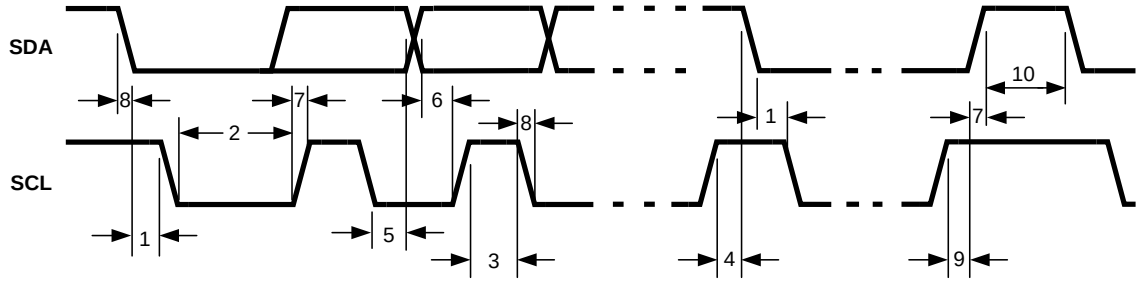


Figure 27. I²C Timing Diagram

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Symbol	Parameter	Limit(1)		Units
		Min	Max	
1	Hold Time (repeated) START Condition	0.6		µs
2	Clock Low Time	1.3		µs
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		ns
5	Data Hold Time (Output direction)	300		ns
5	Data Hold Time (Input direction)	0		ns
6	Data Setup Time	100		ns
7	Rise Time of SDA and SCL	20+0.1Cb	300	ns
8	Fall Time of SDA and SCL	15+0.1Cb	300	ns
9	Set-up Time for STOP condition	600		ns
10	Bus Free Time between a STOP and a START Condition	1.3		µs
Cb	Capacitive Load for Each Bus Line	10	200	pF

(1) **Note:** Data specified by design.

I²C REGISTER DETAILS

The I²C bus interacts with the LM3435 to realize the features of LED current program inter-color delay time program and Fault reporting function. The operation of these functions requires the writing and reading of the internal registers of the LM3435. In below is the master register map of the device.

Table 1. Master Register Map

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
00h	LEDLO	0	0	RLED[1:0]		BLED[1:0]		GLED[1:0]		0011 1111
01h	GLEDH	GLED[9:2]								1111 1111
02h	BLEDH	BLED[9:2]								1111 1111
03h	RLEDH	RLED[9:2]								1111 1111
05h	FLT_RPT	0	0	0	0	0	0	0	FLT_RPT	0000 0001
06h	DELAY	RDLY[1:0]		1	BDLY[1:0]		1	GDLY[1:0]		1111 1111
07h	FAULT	GO	GS	0	BO	BS	0	RO	RS	0000 0000

LED Current Register Definitions

The LED currents for each color can be accurately adjusted by 10 bits resolution (1024 steps) independently. By writing control bytes into the LM3435 LED current Registers, the LED currents can be precisely set to any value in the range of I_{MIN} to I_{REF}.

In below is the LED Current Low register bit definition:

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
00h	LEDLO	0	0	RLED[1:0]		BLED[1:0]		GLED[1:0]		0011 1111

Bits	Description
7:6	Reserved. These bits always read zeros.
5:4	The least significant bits of the 10-bit RLED register. This register is for programming the level of current for the Red LED.
3:2	The least significant bits of the 10-bit BLED register. This register is for programming the level of current for the Blue LED.
1:0	The least significant bits of the 10-bit GLED register. This register is for programming the level of current for the Green LED.

In below is the LED Current High register bit definition:

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
01h	GLEDH	GLED[9:2]								1111 1111
02h	BLEDH	BLED[9:2]								1111 1111

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ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
03h	RLEDH	RLED[9:2]								1111 1111

Bits	Description
7:0	The most 8 significant bits of the 10-bit GLED, BLED and RLED registers respectively. These registers are for programming the level of current of the Green LED, Blue LED and Red LED independently.

Fault Reporting Register Definition

The fault reporting feature of the LM3435 can be selected by the system designer according to their application needs. To select or de-select this feature is realized by writing one bit into the FLT_RPT register.

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
05h	FLT_RPT	0	0	0	0	0	0	0	FLT_RPT	0000 0001

Bits	Description
7:1	Reserved. These bits always read zeros.
0	This bit defines the mode of fault report feature. Writing a " 1 " into this bit enables the fault reporting feature, otherwise no Fault signal output at Pin 27.

Color Transition Delay Register Definition

The transition of one color into next color is not executed immediately. Certain delay is inserted in between to ensure the LED rail voltage stabilized before turning the next LED on. This delay is user programmable by writing control bits into the DELAY register for each color individually. The power up default delay time is 35µs and this delay can be programmed from 5 µs to 35 µs maximum in step of 10 µs.

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
06h	DELAY	RDLY[1:0]		1	BDLY[1:0]		1	GDLY[1:0]		1111 1111

Bits	Description
7:6	These two bits are for programming the Red transition delay.
5	Reserved. This bit always read " 1".
4:3	These two bits are for programming the Blue transition delay.
2	Reserved. This bit always read " 1".
1:0	These two bits are for programming the Green transition delay.

Fault Register Definition

The LM3435 features LED fault detection capability. Whenever a LED fault is detected (open or short), the FAULT output (pin 27) will go high to indicate a LED fault is detected. The details of the fault can be investigated by reading the FAULT register. The FAULT register is read only. The fault status can be cleared by clearing and then re-enabling the FLT_RPT register or power up reset of the device.

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
07h	FAULT	GO	GS	0	BO	BS	0	RO	RS	0000 0000

Bits	Description
7	GO – Green Open. This read only register bit indicates the presence of an OPEN fault of the GREEN LED.
6	GS – Green Short. This read only register bit indicates the presence of an SHORT fault of the GREEN LED.
5	Reserved. This bit always read " 0 ".
4	BO – Blue Open. This read only register bit indicates the presence of an OPEN fault of the BLUE LED.
3	BS – Blue Short. This read only register bit indicates the presence of an SHORT fault of the BLUE LED.
2	Reserved. This bit always read " 0 ".
1	RO – Red Open. This read only register bit indicates the presence of an OPEN fault of the RED LED.
0	RS – Red Short. This read only register bit indicates the presence of an SHORT fault of the RED LED.

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Design Procedures

This section presents a design example of a typical pico projector application. By using LM3435, the system requires only single DC-DC converter to drive three color LEDs instead of using three DC-DC converters with conventional design. The suggested approach not only saves components cost, but also releases invaluable PCB space to the system and enhances system reliability. The handy projector is powered by a single lithium battery cell or a 5Vdc wall mount adaptor. The key specifications of the design are as in below:

- Supply voltage range, V_{IN} = 2.7V to 5.5V
- Preset LED current per channel, I_{LED} = 1.5A
- Minimum LED current per channel, $I_{LED(MIN)}$ = 600mA
- Maximum LED forward voltage drop, V_{LED} = 3.5V at 1.5A
- Flyback converter switching Frequency, F_{SW} = ~500kHz

SETTING THE FLYBACK CONVERTER SWITCHING FREQUENCY, F_{SW}

The LM3435 employs a proprietary Projected On-Time (POT) control scheme, the switching frequency, F_{SW} of the converter is simply set by an external resistor, R_{RT} across RT pin of LM3435 and VOUT of the converter. The flyback converter under POT control can maintain a fairly constant switching frequency that depends mainly on the value of R_{RT}. The relationship between the flyback converter switching frequency, F_{SW} and R_{RT} is approximated by the following relationship:

$$F_{SW} = \frac{2.5}{R_{RT}} \times 10^8$$

R_{RT} in Ω and F_{SW} in kHz (3)

In order to set the flyback converter switching frequency, F_{SW} to 500kHz, the value of R_{RT} can be calculated as in below:

$$R_{RT} = \frac{2.5}{F_{SW}} \times 10^8 = \frac{2.5}{500} \times 10^8 = 500k\Omega$$

(4)

A standard resistor value of 499kΩ can be used in place and the period of switching, T_{SW} is about 2µs.

SETTING THE NOMINAL LED CURRENT

The nominal LED current of the LEDs are set by resistors connected to IREFR, IREFG and IREFB pins. The current for each channel can be set individually and it is not mandatory that all channel currents are the same. Just for simplicity, we assume all channels are set to 1.5A in this example. The LED current and the value of R_{IREFR}, R_{IREFG} and R_{IREFB} is governed by the following equation.

$$I_{LEDx} = \frac{24.75}{R_{IREFx}} \times 10^3$$

R_{IREFx} in Ω and I_{LEDx} in Ampere (5)

The resistance value for the current setting resistors is calculated as in below:

$$R_{IREFx} = \frac{24.75}{I_{LEDx}} \times 10^3 = \frac{24.75}{1.5} \times 10^3 = 16.5k\Omega$$
$$R_{IREFR} = R_{IREFG} = R_{IREFB} = 16.5k\Omega$$

(6)

In order to achieve the required LED current accuracy, high quality resistors with tolerance not higher than +/-1% are recommended.

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INDUCTOR SELECTION

Selecting the correct inductor is one of the major task in application design of a LED driver system. The most critical inductor parameters are inductance, current rating, DC resistance and size. As an rule of thumb, for same physical size inductor, higher the inductance means higher the DC resistance, consequently more power loss with the inductor and lower the DC-DC conversion efficiency. With LM3435, the inductor governs the inductor ripple current and limits the minimum LED current that can be supported. However for the POT control in LM3435, a minimum inductor ripple current of about 300mA$_{pk-pk}$ is required for proper operation. The relationship of the ON-Duty, D and the input/output voltages can be derived by applying the Volt-Second Balance equation across the inductor. The waveforms of the inductor current and voltage are shown in below.

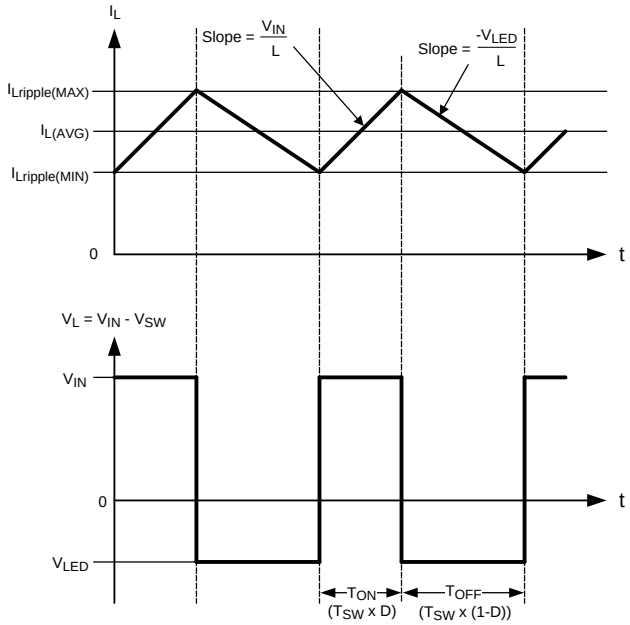


Figure 28. Inductor Switching Waveforms

Applying the Volt-Second Balance equation with the inductor voltage waveform,

$$V_{IN} \times D = V_{LED} \times |1-D|$$
$$(V_{IN} + V_{LED}) \times D = V_{LED}$$
$$D = \frac{V_{LED}}{V_{IN} + V_{LED}} \quad (7)$$

Referring to the inductor current waveform, the average inductor current, $I_{L(AVG)}$ can be derived as in below:

$$I_{L(AVG)} = I_{Lripple(MIN)} + \frac{I_{Lripple(MAX)} - I_{Lripple(MIN)}}{2}$$
$$I_{Lripple(MAX)} - I_{Lripple(MIN)} = \frac{V_{IN}}{L} \times T_{ON}$$
$$T_{ON} = T_{SW} \times D$$
$$I_{Lripple(MAX)} - I_{Lripple(MIN)} = \frac{V_{IN}}{L} \times T_{SW} \times D \quad (8)$$

The minimum LED current, $I_{LED(MIN)}$ happens when the inductor current just entered the Critical Conduction Mode operation, i.e. $I_{Lripple(MIN)}$=0.

Applying this condition to the last equation:

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$$I_{L(AVG,MIN)} = \frac{I_{Lripple(MAX)}}{2} = \frac{V_{IN} \times T_{SW} \times D}{2 \times L} \quad (9)$$

The relationship of the LED current, I_{LED} and the average inductor current, $I_{L(AVG)}$ is shown in below:

$$I_{L(AVG)} = I_{LED} \times \frac{1}{1-D}$$
$$I_{LED} = I_{L(AVG)} \times (1-D) \quad (10)$$

By combining last two equations, the minimum LED current, $I_{LED(MIN)}$ can be calculated as in below:

$$I_{LED(MIN)} = I_{L(AVG,MIN)} \times (1-D) = \frac{V_{IN} \times T_{SW} \times D}{2 \times L} \times (1-D) \quad (11)$$

By rearranging the terms, the inductance, L required for any specific minimum LED current, $I_{LED(MIN)}$ can be found with the equation in below:

$$L = \frac{V_{IN}}{2 \times I_{LED(MIN)}} \times T_{SW} \times D \times (1-D) \quad (12)$$

From the equation, it can be noted that for lower minimum LED current, the inductance required will be higher. As mentioned in before, higher the inductance means higher DC resistance in same size inductor. Additionally, the POT control in LM3435, a minimum inductor ripple current is required to maintain proper operation. The restrictions limit the lowest current can be programed by I^2C control.

In this example, the $I_{LED(MIN)}$=600mA and the highest ripple will happen when the input voltage is maximum, i.e. V_{IN}=5.5V. The ON Duty, D with average LED forward voltage of 3.5V is calculated in below:

$$D = \frac{V_{LED}}{V_{IN(MAX)} + V_{LED}} = \frac{3.5V}{5.5V + 3.5V} = 0.39 \quad (13)$$

The required inductance for this case is:

$$L = \frac{5.5V}{2 \times 0.6A} \times 2\mu s \times 0.39 \times (1-0.39)$$
$$L = 2.18\mu H \quad (14)$$

A standard inductance value of 2.2µH is suggested and the minimum LED current, $I_{LED(MIN)}$ is about 595mA @ V_{IN}=5.5V.

Other than the inductance, the worst case inductor current, $I_{L(MAX)}$ must be calculated so that an inductor with appropriate saturation current level can be specified. The maximum inductor current, $I_{L(MAX)}$ can be calculated with the equation in below:

$$I_{L(MAX)} = I_{L(AVG)} + \frac{I_{Lripple(MAX)} + I_{Lripple(MIN)}}{2} = \frac{I_{LED}}{(1-D)} + \frac{V_{IN}}{2 \times L} \times T_{SW} \times D \quad (15)$$

The highest inductor current occurs when the input voltage is minimum, i.e. V_{IN}=2.7V. The ON Duty, D for this condition can be calculated as in below:

$$D = \frac{V_{LED}}{V_{IN(MIN)} + V_{LED}} = \frac{3.5V}{2.7V + 3.5V} = 0.56 \quad (16)$$

The maximum inductor current, $I_{L(MAX)}$ is calculated in below:

$$I_{L(MAX)} = \frac{1.5A}{(1-0.56)} + \frac{2.7V}{2 \times 2.2\mu H} \times 2\mu s \times 0.56 = 4.1A \quad (17)$$

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The calculated maximum inductor current is 4.1A, however the inductance can drop as temperature rise. In order to accommodate all possible variations, an inductor with saturation current specification not less than 5A is suggested.

INPUT CAPACITORS SELECTION

Input capacitors are required for all supply input pins to ensure that V_{IN} does not drop excessively during high current switching transients. LM3435 have supply input pins located in different sides of the device. Individual capacitors are needed for the supply input pins locally. All capacitors must be placed as close as possible to the supply input pins and have low impedance return ground path to the device grounds and back to supply ground. Capacitors C_{IN1} and C_{IN2} are the main input capacitors and additionally, C_{IN3} is added to de-couple high frequency interference. The capacitance for C_{IN1} and C_{IN2} is recommended in the range of 22µF to 47µF and C_{IN3} is 0.1µF. Compact applications normally have stringent space limitations, small size surface mount capacitors are usually preferred. Low ESR Multi-Layer Ceramic Capacitors (MLCC) are the best choices. MLCC capacitors with X5R and X7R dielectrics are recommended for its low leakage and low capacitance variation against temperature and frequency.

OUTPUT CAPACITORS SELECTION

Two output capacitors are required with LM3435 configuration, one for V_{OUT} to Ground, C_{OUT2} and one for de-coupling the LED current ripple, C_{OUT1}. The LM3435 operates at frequencies high enough to allow the use of MLCC capacitors without compromising transient response. Low ESR characteristic of the MLCC allow higher inductor ripple without significant increase of the output ripple. The capacitance recommended for C_{OUT1} is 10µF and C_{OUT2} is 22µF. Again, high quality MLCC capacitors with X5R and X7R dielectrics are recommended. For certain conditions, acoustic problem may be encountered with using MLCC, Low Acoustic Noise Type capacitors are strongly recommended for all output capacitors. Alternatively, the acoustic noise can also be lowered by using smaller size capacitors in parallel to achieve the required capacitance.

OTHER CAPACITORS SELECTION

Three small startup capacitors connected to CG, CB and CR pins are needed for proper operation. The suggested capacitance for C_{CR}, C_{CG} and C_{CB} is 1nF. Also three capacitors connected to GLED, BLED and RLED pins to protect the device from high transient stress due to the inductance of the connecting wires for the LEDs. The suggested capacitance for C_G, C_B and C_R is 0.47µH. MLCC capacitors with X5R and X7R dielectrics are recommended. All capacitors must be placed as close as possible to the device pins.

DIODE SELECTION

A schottky barrier diode is added across the SW and VOUT pins, equivalently, its across the internal P-channel MOSFET of the synchronous converter, that can help to improve the conversion efficiency by few percents. A very low forward voltage and 1A rated forward current part is suggested in the schematic diagram. The key selection criteria are the forward voltage and the rated forward current.

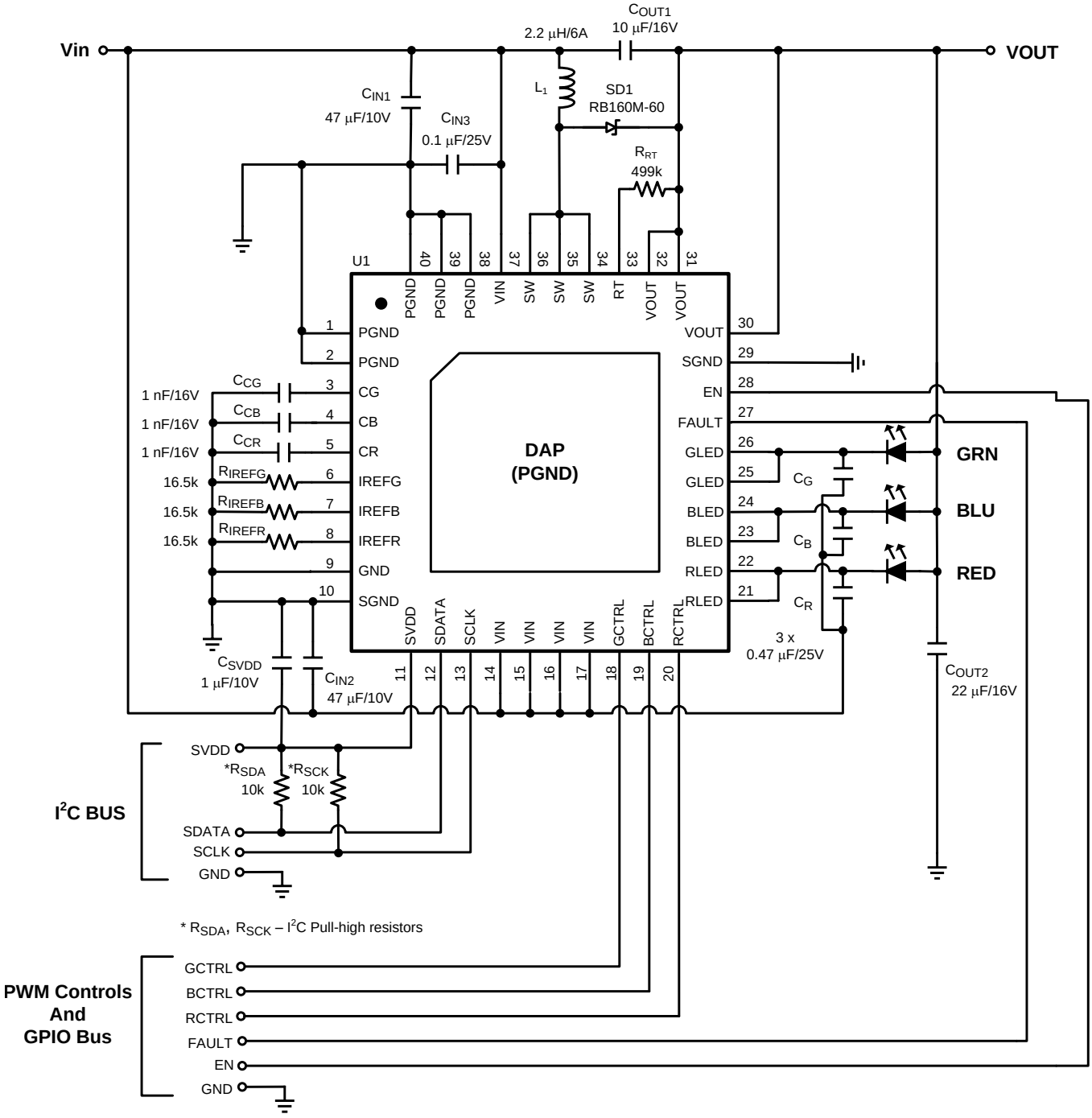
PCB LAYOUT CONSIDERATIONS

The performance of any switching converters depends as much upon the layout of the PCB as the component selection. PCB layout considerations are therefore critical for optimum performance. The layout must be as neat and compact as possible, and all external components must be as close as possible to their associated pins. The PGND connection to C_{IN} and VOUT connection to C_{OUT} should be as short and direct as possible with thick traces. The inductor should connect close to the SW pin with short and thick trace to reduce the potential electro-magnetic interference.

It is expected that the internal power elements of the LM3435 will produce certain amount of heat during normal operation, good use of the PC board's ground plane can help considerably to dissipate heat. The exposed pad on the bottom of the IC package can be soldered to a copper pad with thermal vias that can help to conduct the heat to the bottom side ground plane. The bottom side ground plane should be as large as possible.

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SCHEMATIC OF THE EXAMPLE APPLICATION FOR PICO PROJECTOR



REVISION HISTORY

Changes from Revision B (May 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	21

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3435SQ/NOPB	ACTIVE	WQFN	RSB	40	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L3435SQ	Samples
LM3435SQX/NOPB	ACTIVE	WQFN	RSB	40	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L3435SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

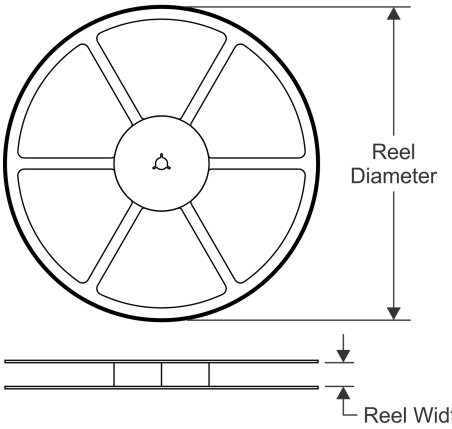
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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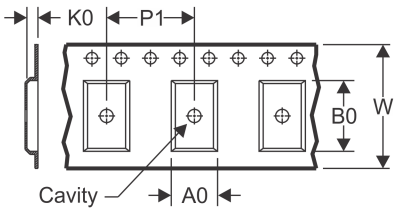
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

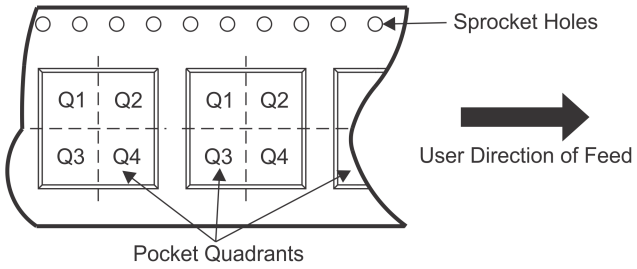


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

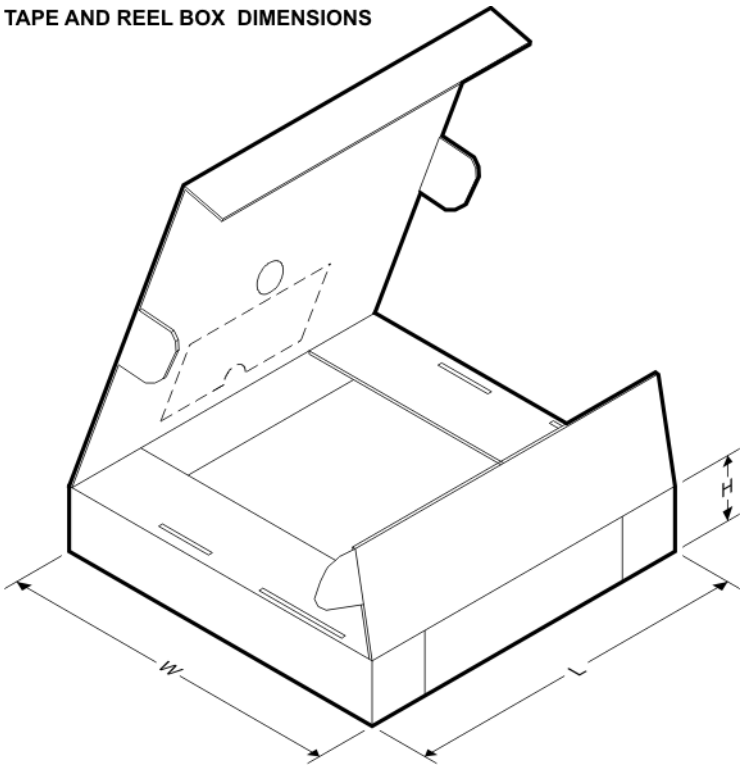
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3435SQ/NOPB	WQFN	RSB	40	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LM3435SQX/NOPB	WQFN	RSB	40	4500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

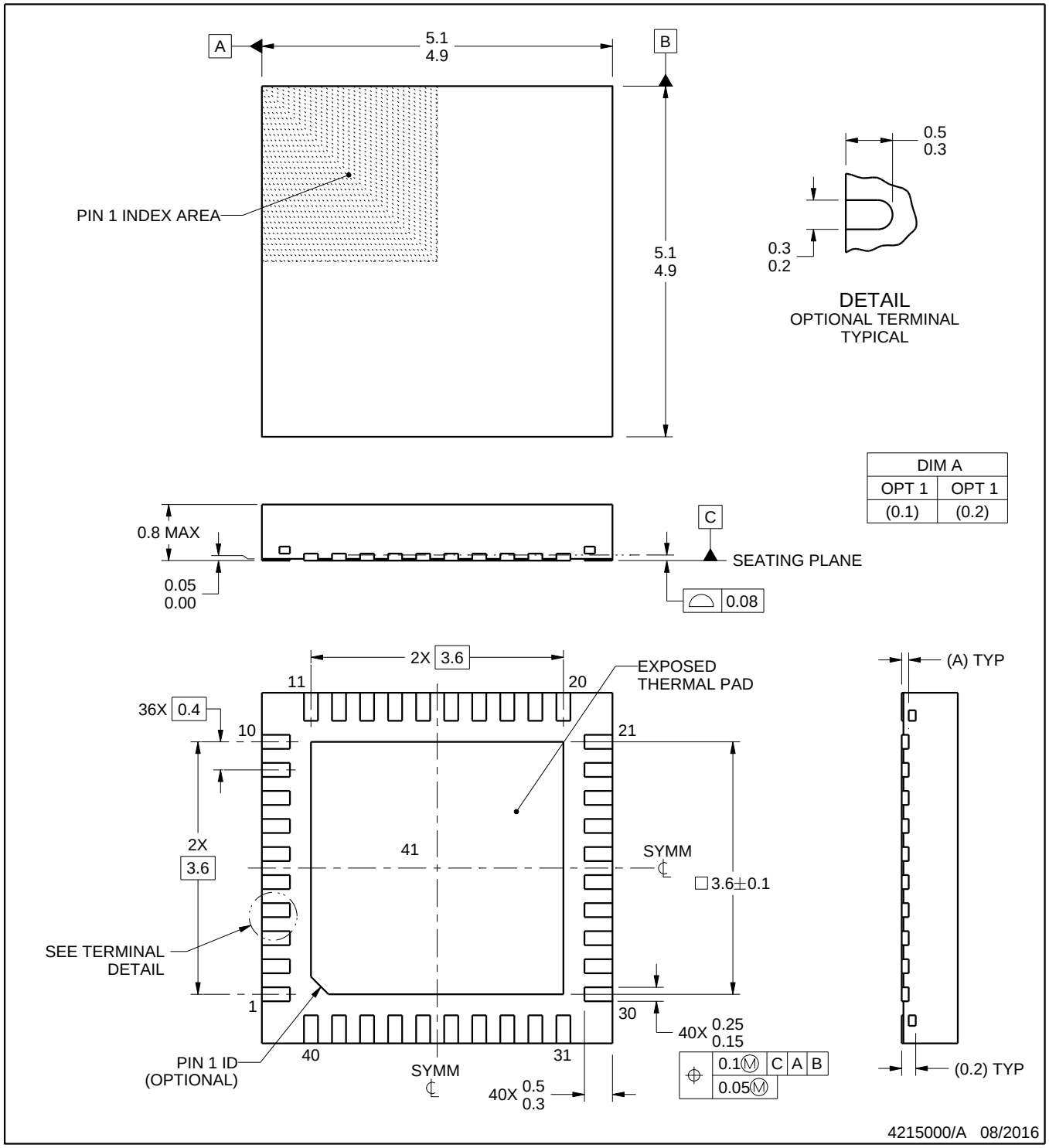
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3435SQ/NOPB	WQFN	RSB	40	1000	208.0	191.0	35.0
LM3435SQX/NOPB	WQFN	RSB	40	4500	367.0	367.0	35.0

PACKAGE OUTLINE

RSB0040A

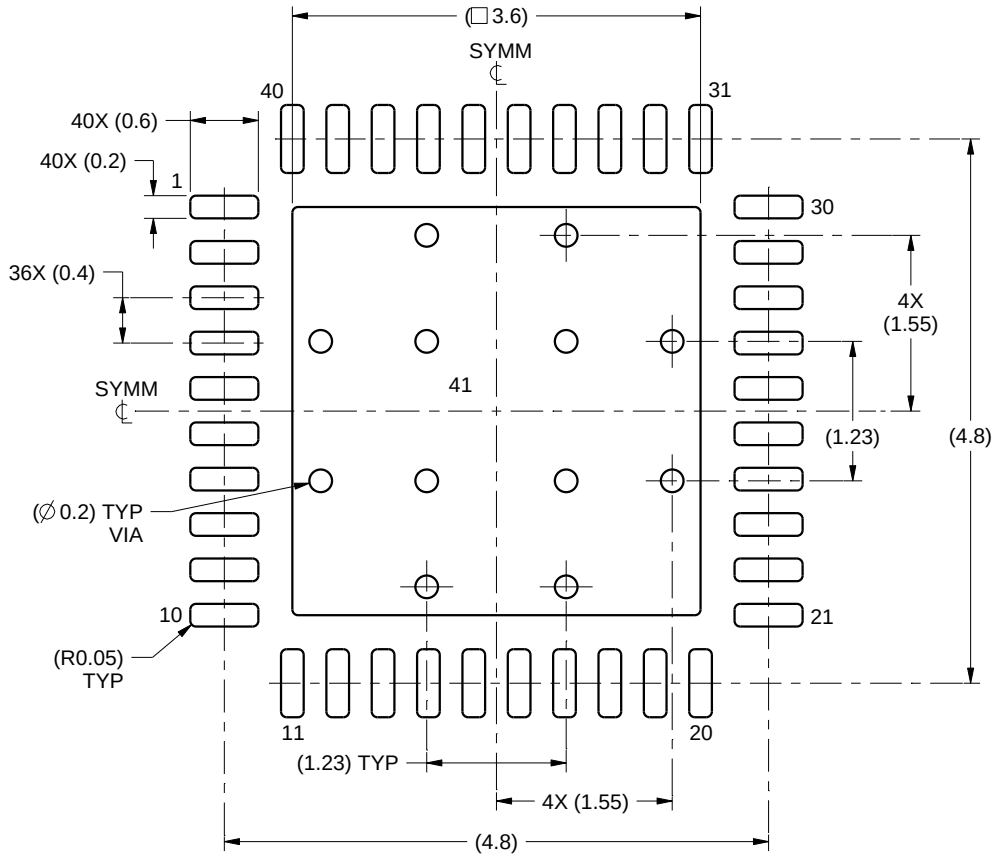
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

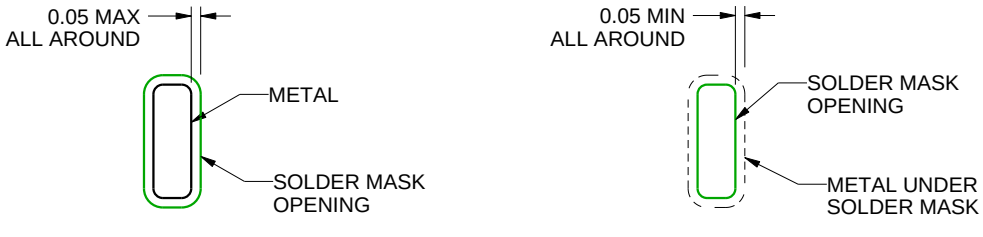


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

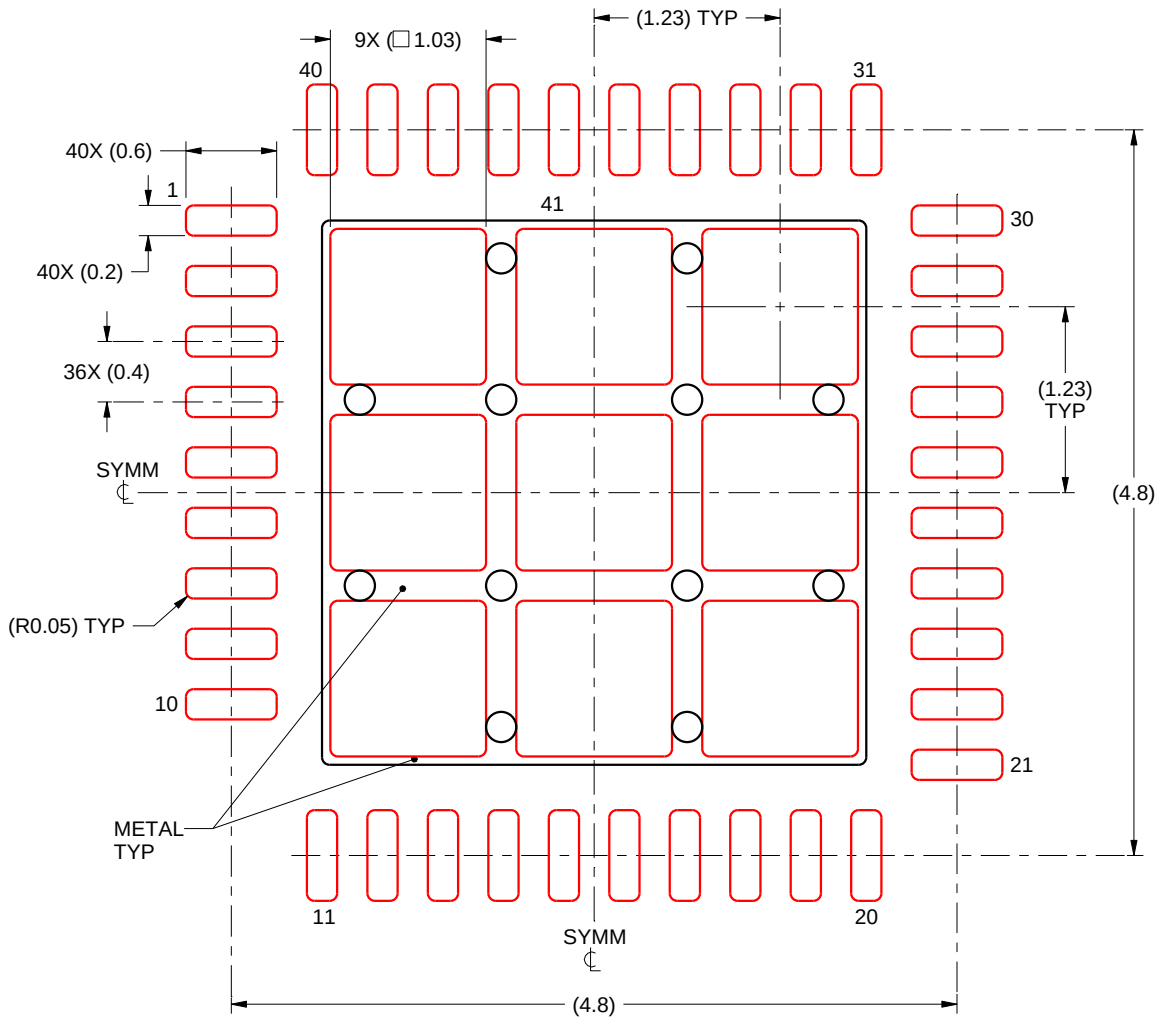


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 41
73.7% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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