TS3L110 四路 SPDT 高带宽 10/100 Base-T LAN 开关 差分 8 通道至 4 通道多路复用器/多路信号分离器

1 特性

- 高带宽（BW = 500MHz，典型值）
- 低串扰（X_{TALK} = –30dB，典型值）
- 具有接近零传播延迟的双向数据流
- 平缓的低导通状态电阻（r_{on} = 4Ω 典型值，$r_{on(flat)}$ = 1Ω）
- 可在数据 I/O 端口（0 至 5V）上进行开关
- V_{CC} 工作范围为 3V 至 3.6V
- I_{off} 支持局部断电模式运行
- 数据和控制输入具有下冲钳位二极管
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范
- ESD 性能测试符合 JESD 22 标准
  - 2000V 人体放电模型（A114-B，II 类）
  - 1000V 充电器件模型 (C101)
- 适合 10 Base-T 和 100 Base-T 信令

2 应用

- 10 和 100 Base-T 信号开关

3 说明

TS3L110 局域网 (LAN) 开关是一款具有单开关使能端 ($\overline{E}$) 输入的 4 位、2 选 1 多路复用器/多路信号分离器。当 $\overline{E}$ 为低时，开关启用，I 端口连接至 Y 端口。当 $\overline{E}$ 为高时，开关禁用，I 和 Y 端口之间存在高阻抗状态。选择 (S) 输入可控制多路复用器/多路信号分离器的数据路径。

TS3L110 器件可用于代替 LAN 应用中的机械继电器。此器件具有平缓的低导通状态电阻 (r_{on})、高带宽和低串扰，适合 10/100 Base-T 和各种其他 LAN 应用中的数字输入 D 类音频放大器。TS3L110 器件可用于将信号从 10/100 Base-T 以太网收发器路由至笔记本电脑或扩展坞中的 RJ-45 LAN 连接器。此器件专为低通道间偏差和低串扰而设计。

该器件完全 适用于 I_{off} 为了部分断电的应用。I_{off} 特性可确保在关断时防止损坏电流通过器件回流。该器件可在关断时提供隔离。

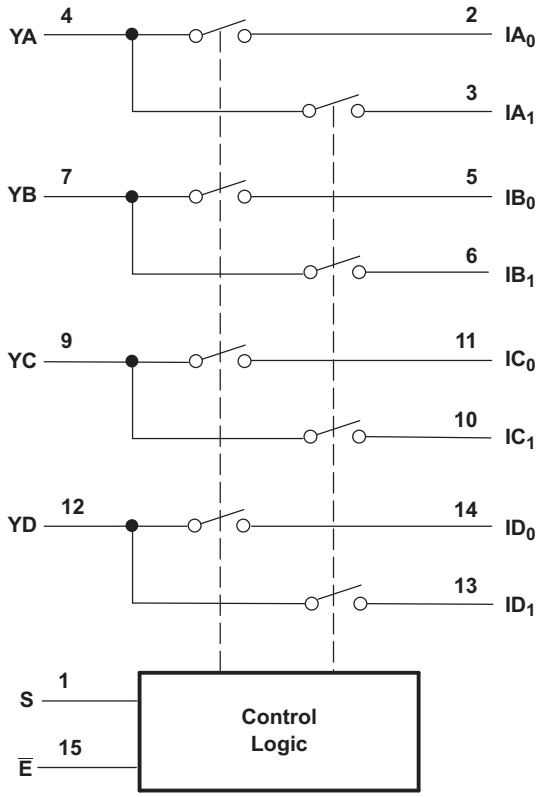
为了确保加电或断电期间的高阻抗状态，$\overline{E}$ 应通过一个上拉电阻器连接至 V_{CC}；该电阻器的最小值由驱动器的电流吸入能力来决定。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TS3L110	SOIC (D) 16	9.90mm x 3.91mm
	SSOP (DBQ) 16	4.90mm x 3.90mm
	TVSOP (DGV) 16	3.60mm x 4.40mm
	TSSOP (PW) 16	5.00mm x 4.40mm
	VQFN (RGV) 16	4.00mm x 4.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

逻辑图（正逻辑）



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (May 2019) to Revision B **Page**

- Change pin 10 to IC_1, pin 11 to IC_0, pin 13 to ID_1, and pin 14 to ID_0 in the *Pin Configuration and Functions* 3

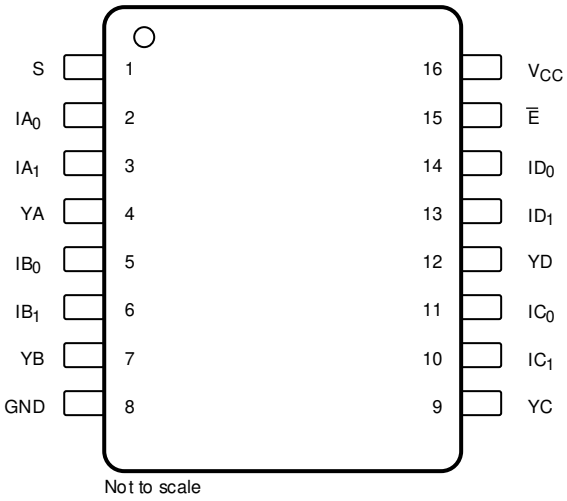
Changes from Original (September 2004) to Revision A **Page**

- 添加了*器件信息* 表、*ESD 额定值* 表、*热性能信息* 表、*特性* *说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购* 信息部分。 1

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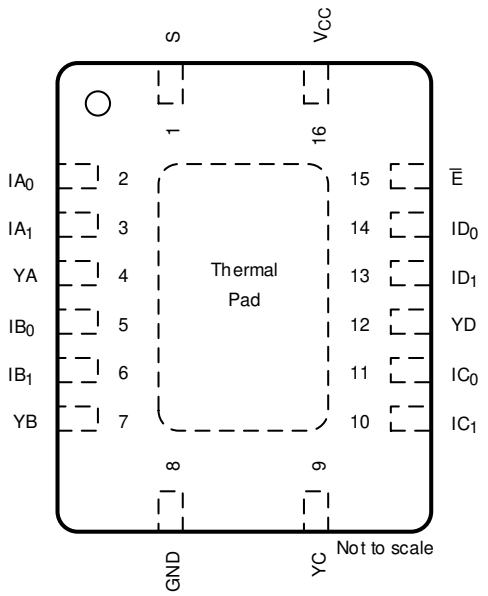
5 Pin Configuration and Functions

D, DBQ, DGV, or PW Package
SOIC, SSOP, TVSOP, TSSOP 16 Pins
Top View



Not to scale

RGY Package
VQFN 16 Pins
Top View



Not to scale

Pin Functions

PIN		DESCRIPTION
NAME	NO.	
S	1	Select input
IA_0	2	Data I/Os
IA_1	3	Data I/Os
YA	4	Data I/Os
IB_0	5	Data I/Os
IB_1	6	Data I/Os
YB	7	Data I/Os
GND	8	Ground (0 V) reference
YC	9	Data I/Os
IC_1	10	Data I/Os
IC_0	11	Data I/Os
YD	12	Data I/Os
ID_1	13	Data I/Os
ID_0	14	Data I/Os
$\overline{E}$	15	Enable input
V_{CC}	16	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VDD and GND.

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6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_{IN}	Control input voltage range(2)(3)		–0.5	7	V
$V_{I/O}$	Switch I/O voltage range(2)(3)(4)		–0.5	7	V
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O}$ < 0		–50	mA
$I_{I/O}$	ON-state switch current(5)			±128	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance	D package(6)		73	°C/W
		DBQ package(6)		90	
		DGV package(6)		120	
		PW package(6)		108	
		RGY package(7)		39	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.
(7) The package thermal impedance is calculated in accordance with JESD 51-5.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. e.

6.3 Recommended Operating Conditions(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level control input voltage ($\overline{E}$, S)	2	5.5	V
V_{IL}	Low-level control input voltage ($\overline{E}$, S)	0	0.8	V
$V_{I/O}$	Input/output voltage	0	5.5	V
T_A	Operating free-air temperature	–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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6.4 Thermal Information

THERMAL METRIC(1)		TS3L110					UNIT
		D (SOIC)	DBQ (SSOP)	DGV (TVSOP)	PW (TSSOP)	RGV (VQFN)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.0	114.5	139.3	111.5	50.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.3	60.5	57.4	42.0	48.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	50.3	58.2	73.7	57.8	26.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.3	15.3	7.2	4.2	2.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.0	57.6	73.0	57.2	26.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	-	-	10.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics(1)

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(2)	MAX	UNIT
V_{IK}	$\overline{E}$, S	V_{CC} = 3.6 V,	I_{IN} = –18 mA				–1.8	V
I_{IH}	$\overline{E}$, S	V_{CC} = 3.6 V,	V_{IN} = 5.5 V				±1	µA
I_{IL}	$\overline{E}$, S	V_{CC} = 3.6 V,	V_{IN} = GND				±1	µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			1	µA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0,	Switch ON or OFF		0.7	1.5	mA
C_{in}	$\overline{E}$, S	f = 1 MHz,	V_{IN} = 0			2.5	3.5	pF
$C_{io(OFF)}$	I port	V_I = 0,	f = 1 MHz, Outputs open,	Switch OFF		3.5	5	pF
	Y port	V_I = 0,	f = 1 MHz, Outputs open,	Switch OFF		5.5	7	
$C_{io(ON)}$	I or Y port	V_I = 0,	f = 1 MHz, Outputs open,	Switch ON		10.5	13	pF
r_{on}		V_{CC} = 3 V,	1.25 V ≤ V_I ≤ V_{CC},	I_O = –10 mA to –30 mA		4	8	Ω
$r_{on(flat)}$(3)		V_{CC} = 3 V,	V_I = 1.25 V and V_{CC},	I_O = –10 mA to –30 mA		1		Ω
Δr_{on}(4)		V_{CC} = 3 V,	1.25 V ≤ V_I ≤ V_{CC},	I_O = –10 mA to –30 mA		0.9	2	Ω

(1) V_I, V_O, I_I, and I_O refer to I/O pins. V_{IN} refers to the control inputs.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) $r_{on(flat)}$ is the difference of r_{on} in a given channel at specified voltages.
(4) Δr_{on} is the difference of r_{on} in a given device.

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6.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V, R_L = 200 Ω, C_L = 10 pF (unless otherwise noted) (see Figure 5 and Figure 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
t_{pd}(2)	I or Y	Y or I		0.25		ns
t_{PZH}, t_{PZL}	$\overline{E}$ or S	I or Y	0.5		7	ns
t_{PHZ}, t_{PLZ}	$\overline{E}$ or S	I or Y	0.5		5	ns
$t_{sk(p)}$(3)	I or Y	Y or I		0.1	0.2	ns

(1) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(3) Skew between opposite transitions of the same output $|t_{PHL} – t_{PLH}|$. This parameter is not production tested.

6.7 Dynamic Characteristics

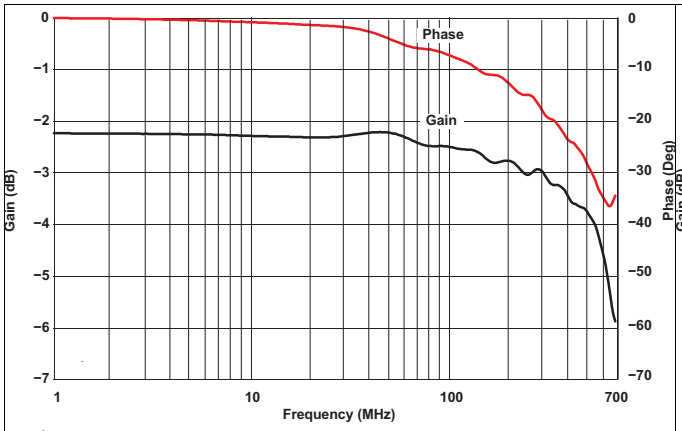
over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS			TYP(1)	UNIT
X_{TALK}	R_L = 100 Ω,	f = 250 MHz,	See Figure 7	–26	dB
O_{IRR}	R_L = 100 Ω,	f = 250 MHz,	See Figure 8	–28	dB
BW	R_L = 100 Ω,		See Figure 6	500	MHz

(1) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

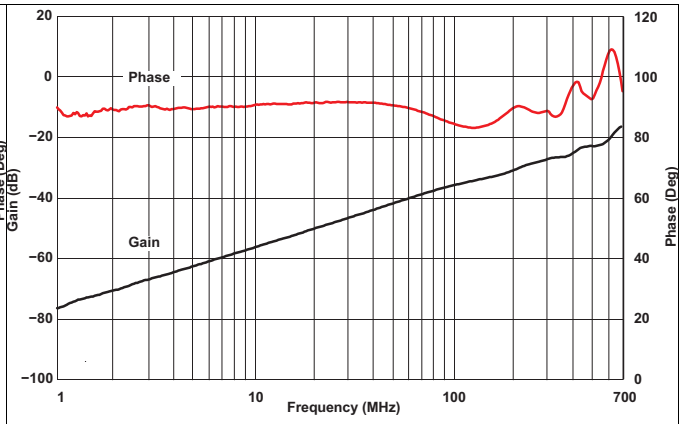
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6.8 Typical Characteristics



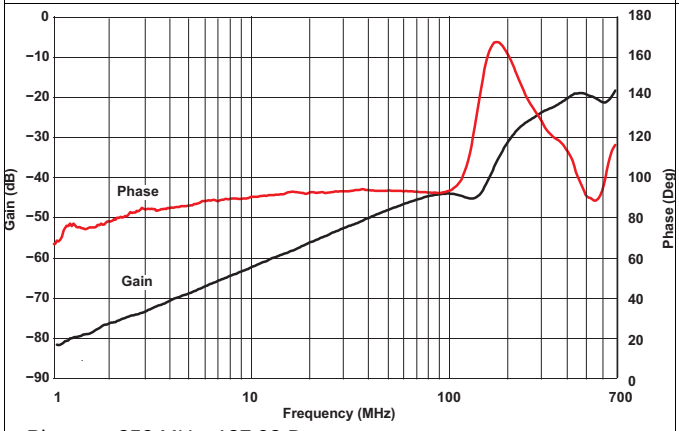
Phase at 627 MHz, −36 Deg
Gain −3 dB at 627 MHz

Figure 1. Gain and Phase vs Frequency



Phase at 250 MHz, 88.2 Deg
Gain −28.5 dB at 250 MHz

Figure 2. OFF Isolation vs Frequency



Phase at 250 MHz, 137.92 Deg
Gain −26 dB at 250 MHZ

Figure 3. Crosstalk vs Frequency

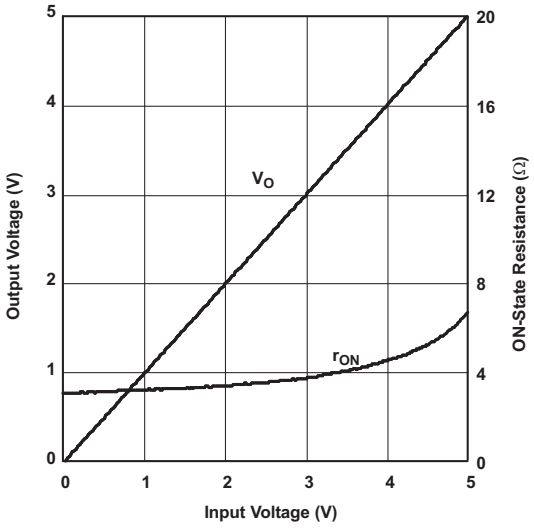
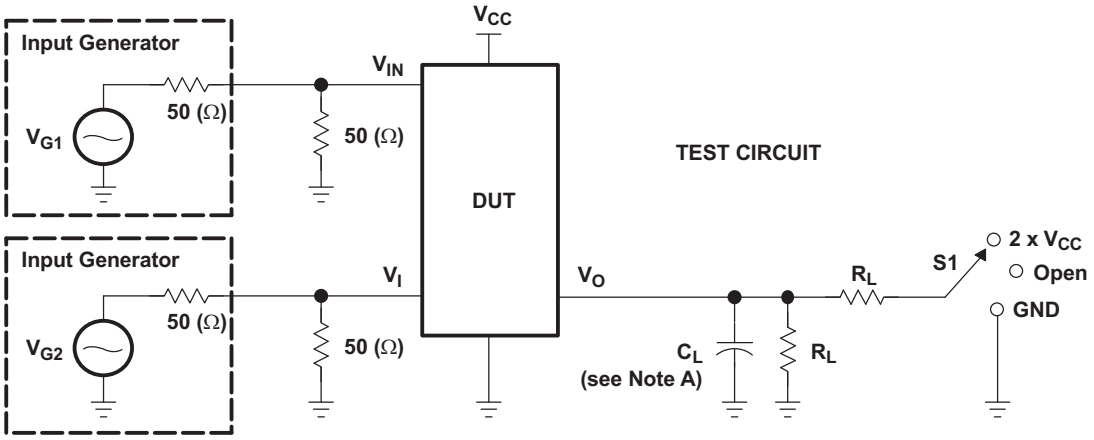


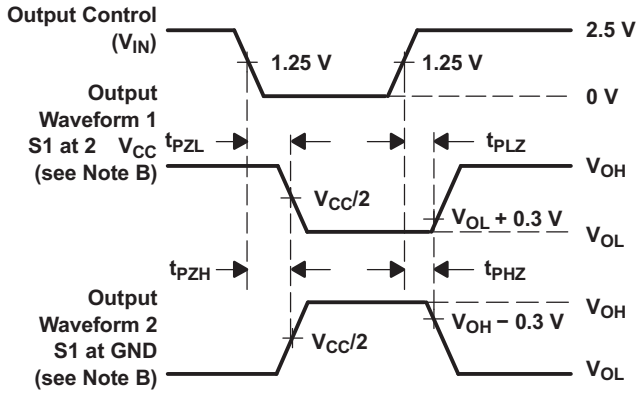
Figure 4. Output Voltage and ON-State Resistance vs Input Voltage

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7 Parameter Measurement Information



TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
t_{PLZ}/t_{PZL}	3.3 V ± 0.3 V	2 x V_{CC}	200 (Ω)	GND	10 pF	0.3 V
t_{PHZ}/t_{PZH}	3.3 V ± 0.3 V	GND	200 (Ω)	V_{CC}	10 pF	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

D. The outputs are measured one at a time, with one transition per measurement.

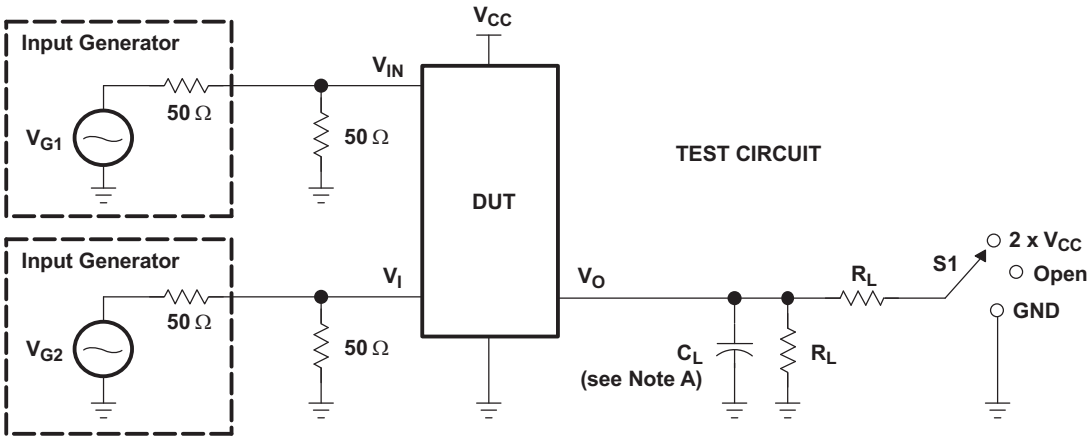
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PLZ} and t_{PHH} are the same as t_{en}.

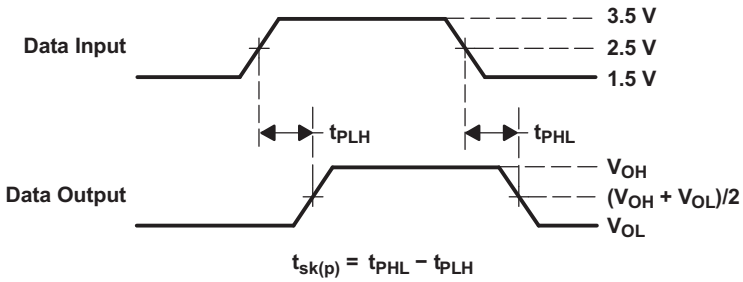
Figure 5. Test Circuit and Voltage Waveforms

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Parameter Measurement Information (continued)



TEST	V_{CC}	S1	R_L	V_{IN} (see Note B)	C_L
$t_{sk(p)}$	3.3 V ± 0.3 V	GND	200 Ω	V_{CC} or GND	10 pF



VOLTAGE WAVEFORMS
PULSE SKEW [$t_{sk(p)}$]

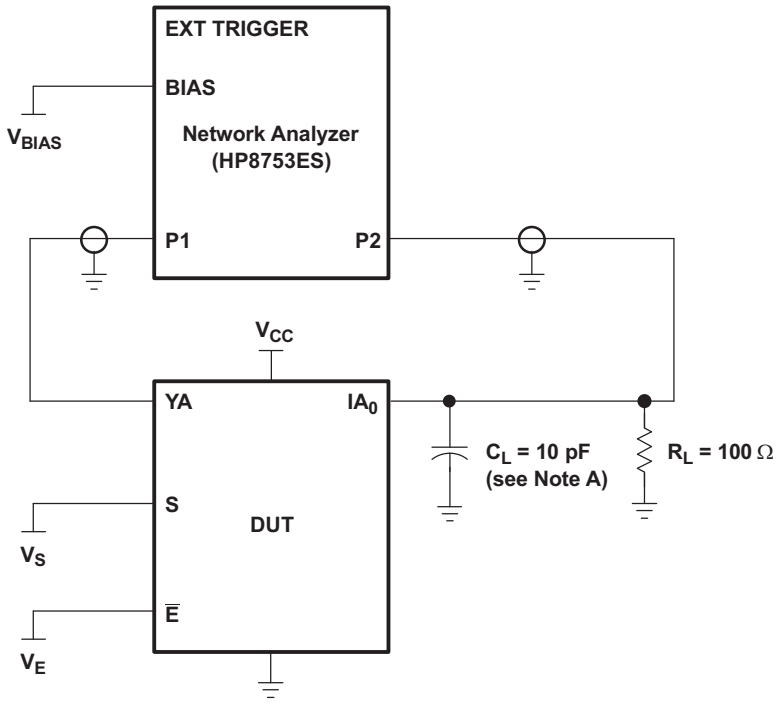
A. C_L includes probe and jig capacitance.

B. Switch is ON during the measurement of $t_{sk(p)}$, that is, voltage at E = 0 and S = V_{CC} or GND.

Figure 6. Test Circuit and Voltage Waveforms

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Parameter Measurement Information (continued)



A. C_L includes probe and jig capacitance.

Figure 7. Test Circuit for Frequency Response (BW)

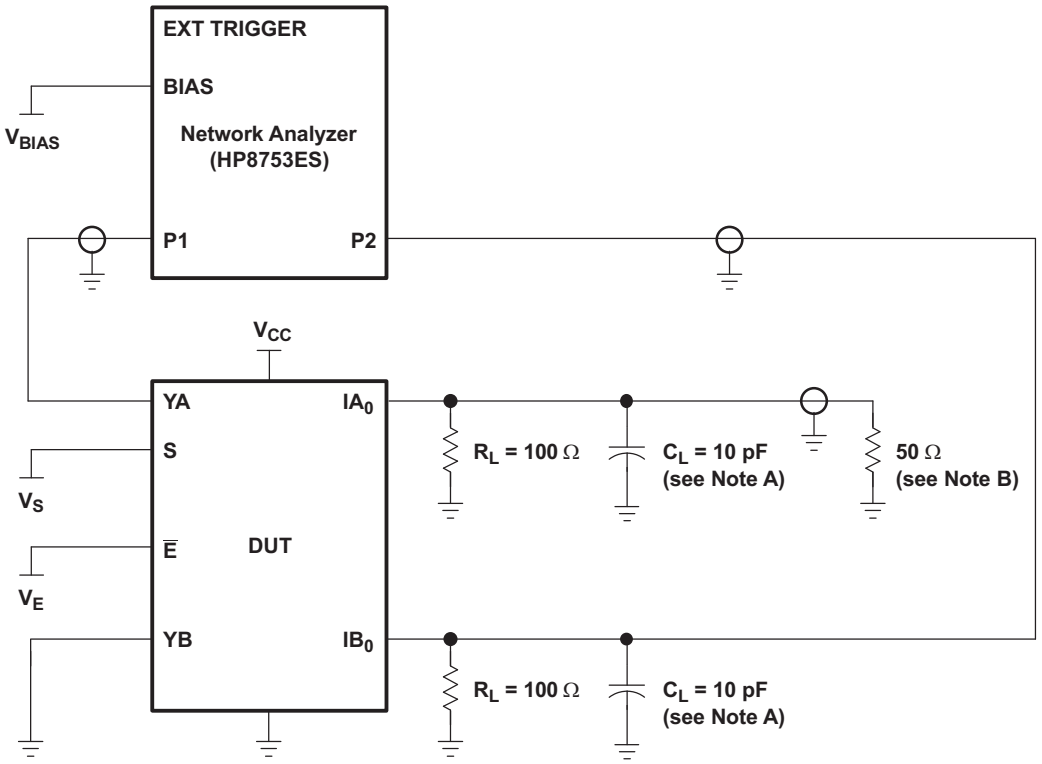
Frequency response is measured at the output of the ON channel. For example, when V_S = 0, V_E = 0, and YA is the input, the output is measured at IA_0. All unused analog I/O ports are left open.

HP8753ES Setup

- Average = 4
- RBW = 3 kHz
- V_{BIAS} = 0.35 V
- ST = 2 s
- P1 = 0 dBM

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Parameter Measurement Information (continued)



A. C_L includes probe and jig capacitance.

B. A 50-Ω termination resistor is needed to match the loading of the network analyzer

Figure 8. Test Circuit for Crosstalk (X_{TALK})

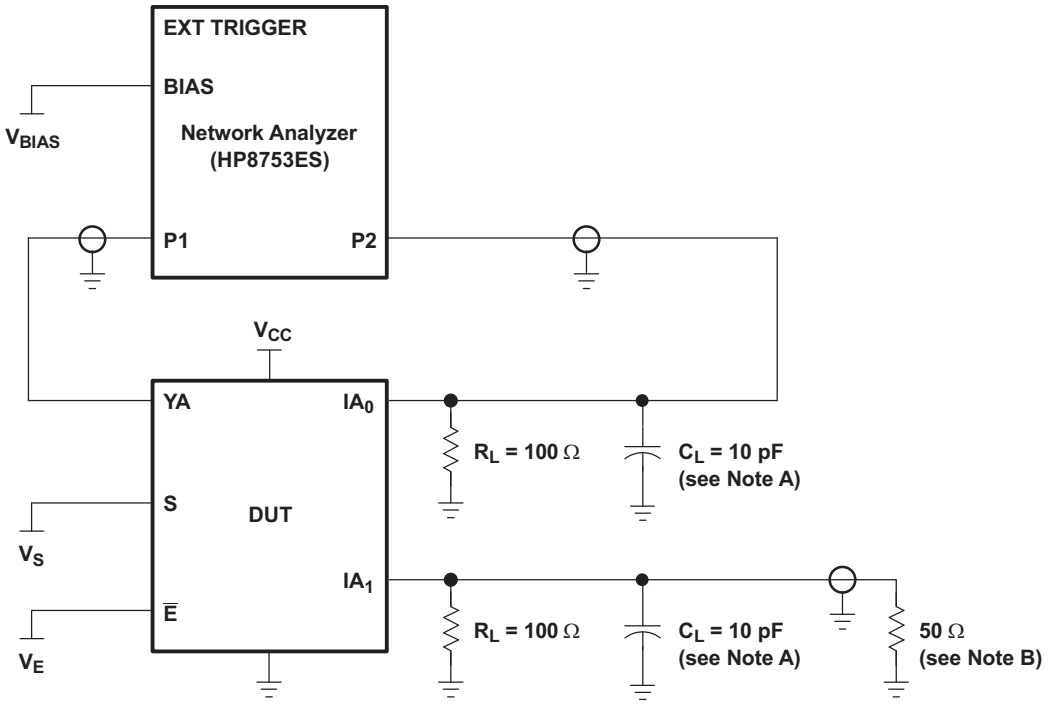
Crosstalk is measured at the output of the nonadjacent ON channel. For example, when V_S = 0, V_E = 0, and YA is the input, the output is measured at IB_0. All unused analog input (Y) ports are connected to GND, and output (I) ports are connected to GND through 50-Ω pulldown resistors.

HP8753ES Setup

- Average = 4
- RBW = 3 kHz
- V_{BIAS} = 0.35 V
- ST = 2 s
- P1 = 0 dBM

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Parameter Measurement Information (continued)



A. C_L includes probe and jig capacitance.

B. A 50-Ω termination resistor is needed to match the loading of the network analyzer

Figure 9. Test Circuit for OFF Isolation (O_{IRR})

OFF isolation is measured at the output of the OFF channel. For example, when $V_S = V_{CC}$, $V_E = 0$, and YA is the input, the output is measured at IA_0. All unused analog input (Y) ports are left open, and output (I) ports are connected to GND through 50-Ω pulldown resistors.

HP8753FS Setup

- Average = 4
- RBW = 3 kHz
- V_{BIAS} = 0.35 V
- ST = 2 s
- P1 = 0 dBM

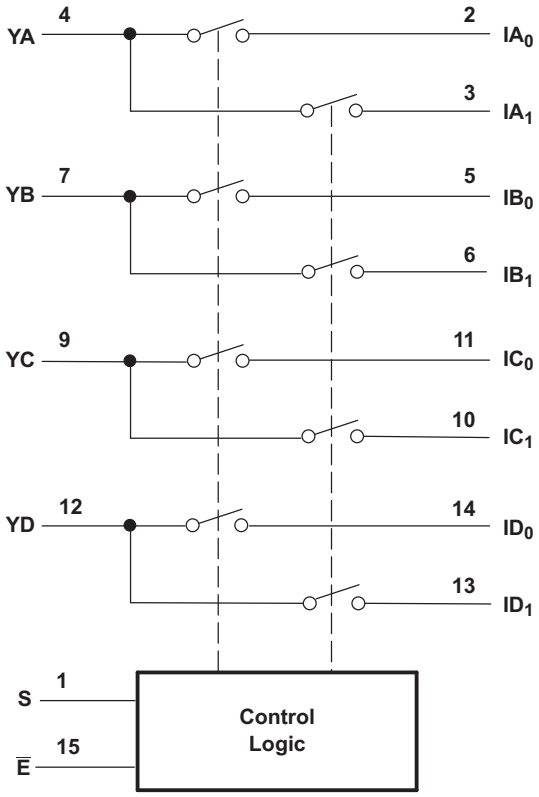
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8 Detailed Description

8.1 Overview

The TI TS3L110 LAN switch is a 4-bit 1-of-2 multiplexer/demultiplexer with a single switch-enable (E) input. When E is low, the switch is enabled, and the I port is connected to the Y port. When E is high, the switch is disabled, and the high-impedance state exists between the I and Y ports. The select (S) input controls the data path of the multiplexer/demultiplexer.

8.2 Functional Block Diagram



8.3 Feature Description

I_{off} supports Partial-Power-Down Mode Operation.

The TS3L110 device ensures the signal path is high impedance state when V_{CC} = 0 V.

8.4 Device Functional Modes

The TS3L110 supports a power down mode which reduces the current consumption of the device and places all the signal paths in a high impedance state. To place the TS3L100 in power down mode, set the $\overline{E}$ pin with a logic high voltage as seen in Table 1.

Table 1. Function Table

INPUTS		INPUT/OUTPUT YX	FUNCTION
$\overline{E}$	S		
L	L	IX_0	$YX = IX_0$
L	H	IX_1	$YX = IX_1$
H	X	Z	Disconnect

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

There are many Local Area Network (LAN) applications in which the ethernet hubs or controllers have a limited number of I/Os or need to route signals from a single ethernet PHY to multiple ethernet jacks. The TS3L110 solution can effectively expand the limited I/Os by switching between multiple Ethernet jacks to interface them to a single Ethernet PHY.

9.2 Typical Application

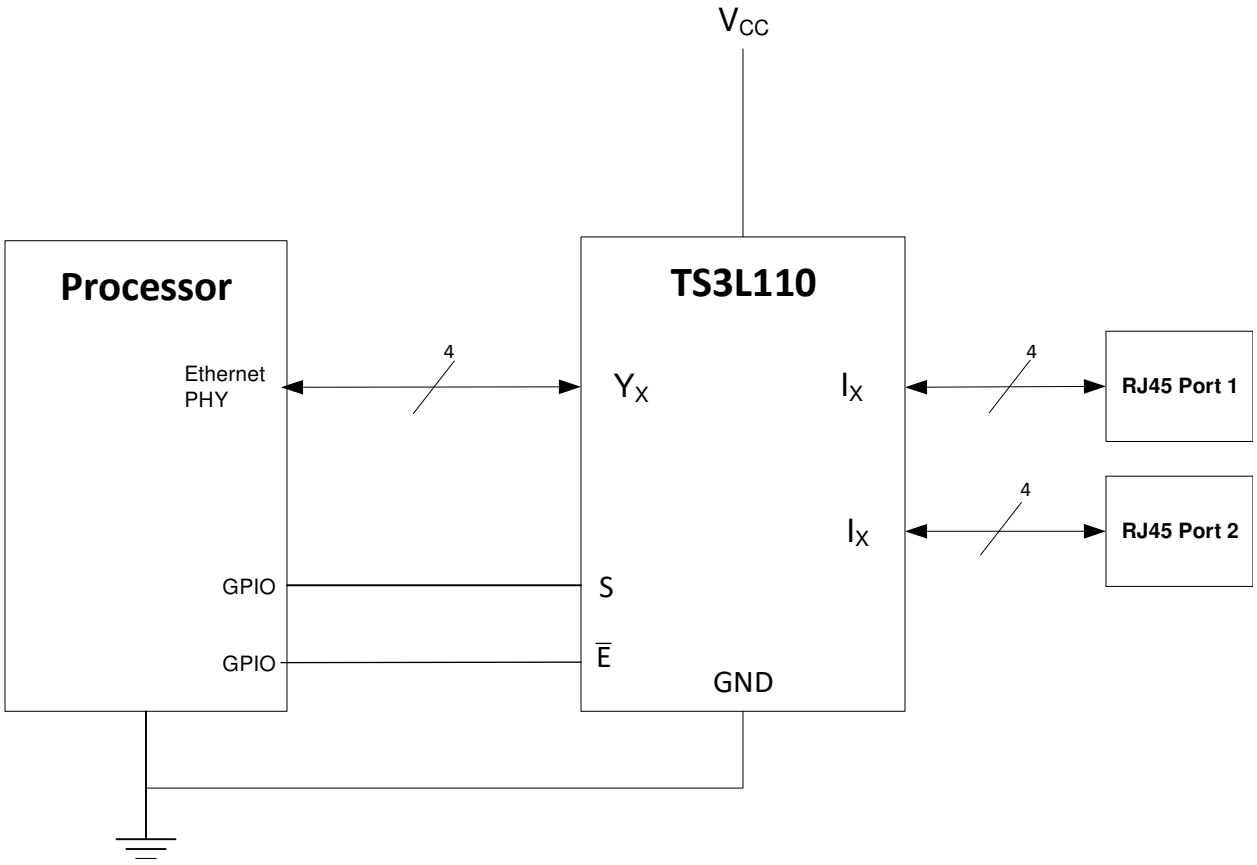


Figure 10. Typical Application Schematic

9.2.1 Design Requirements

Ensure that all of the signals passing through the switch are within the recommended operating ranges. To ensure proper performance, see Recommended Operating Conditions.

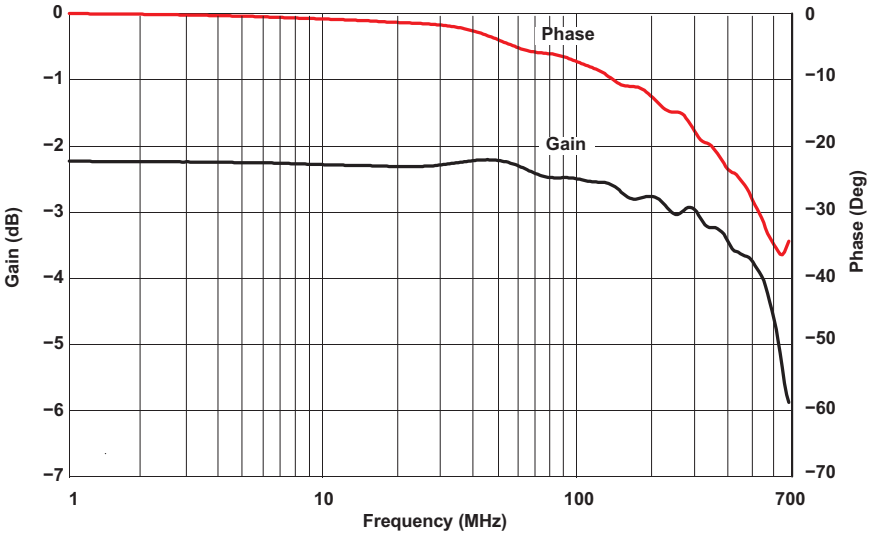
9.2.2 Detailed Design Procedure

The TS3L110 can be properly operated without any external components. TI recommends that the digital control pins S and $\overline{E}$ be pulled up to VCC or down to GND to avoid undesired switch positions that could result from the floating pin. Connect the exposed thermal pad to ground.

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Typical Application (continued)

9.2.3 Application Curves



Phase at 627 MHz, −36 Deg

Gain −3 dB at 627 MHz

Figure 11. Gain and Phase vs Frequency

10 Power Supply Recommendations

Power to the device is supplied through the VCC pins. TI recommends placing a bypass capacitor as close to the supply pin (VCC) as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

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11 Layout

11.1 Layout Guidelines

- TI recommends keeping the high-speed signals as short as possible.
- Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.
- When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
- Do not route traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
- Avoid stubs on the high-speed signals because they cause signal reflections. If a stub is unavoidable, then the stub must be less than 200 mm.
- Route all high-speed signal traces over continuous GND planes, with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.
- Due to high-frequency signals, a printed-circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 12.
- The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

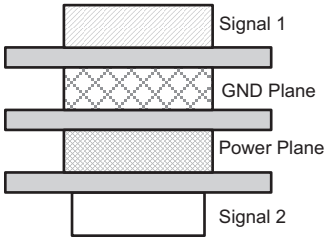


Figure 12. Four-Layer Board Stackup

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11.2 Layout Example

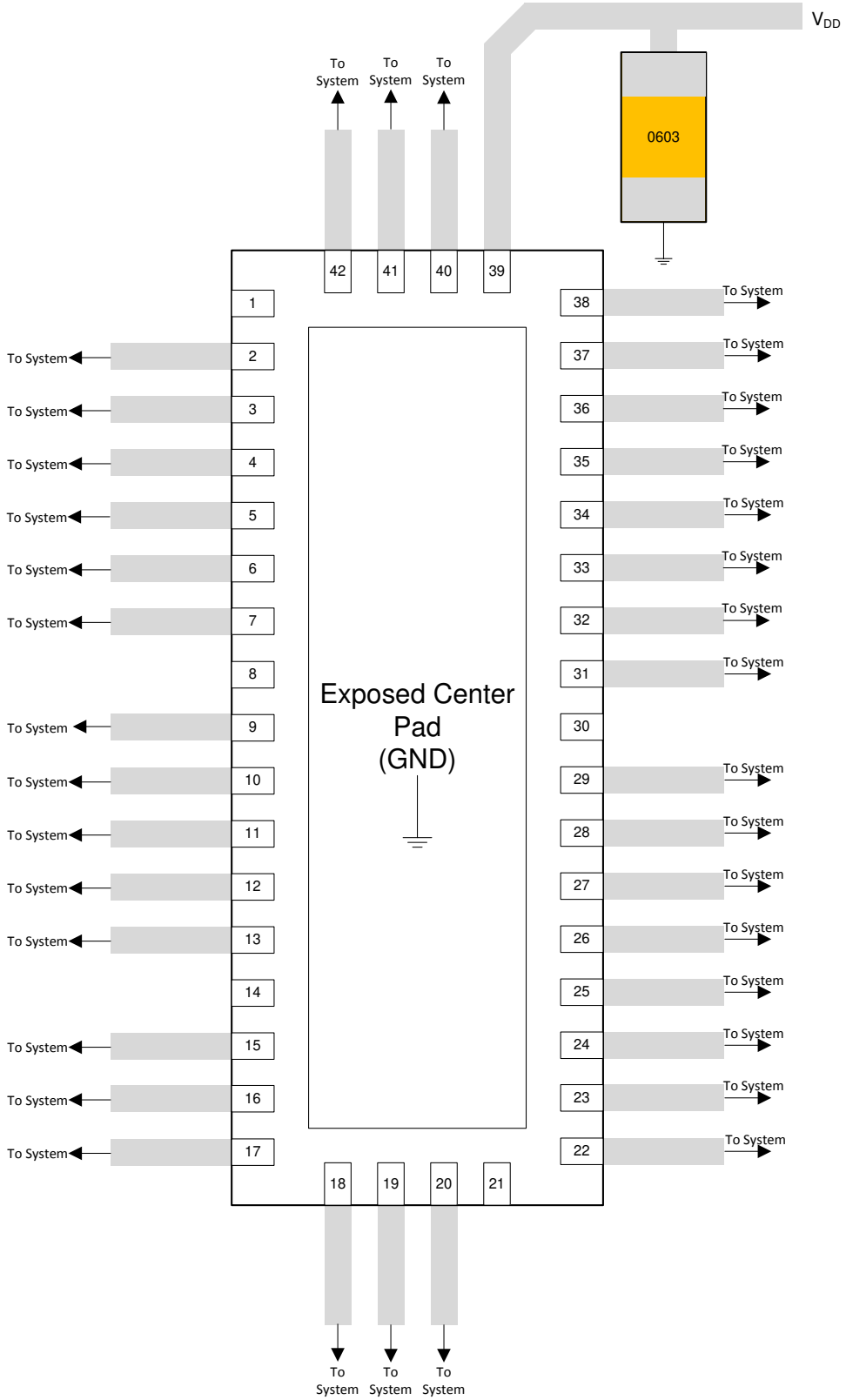


Figure 13. Layout Example

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3L110D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3L110	Samples
TS3L110DBQR	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TK110	Samples
TS3L110DBQRG4	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TK110	Samples
TS3L110DE4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3L110	Samples
TS3L110DG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3L110	Samples
TS3L110DGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TK110	Samples
TS3L110DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3L110	Samples
TS3L110PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TK110	Samples
TS3L110PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TK110	Samples
TS3L110PWRE4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TK110	Samples
TS3L110PWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TK110	Samples
TS3L110RGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TK110	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

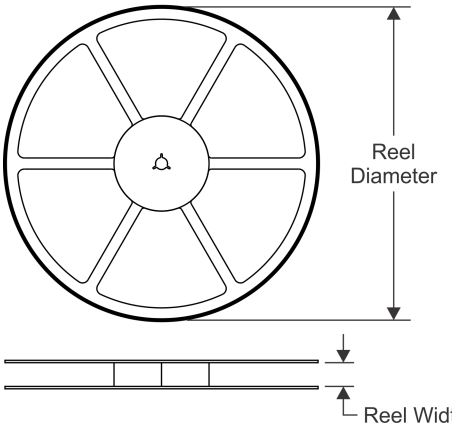
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

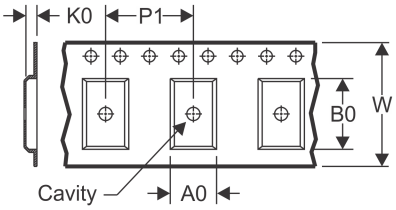
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

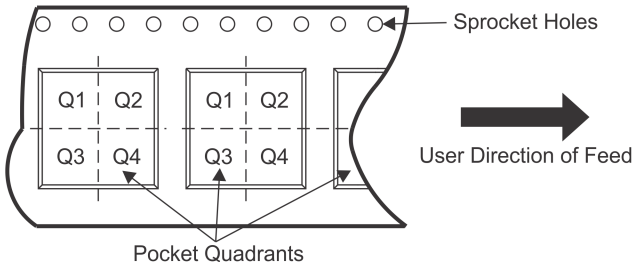


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

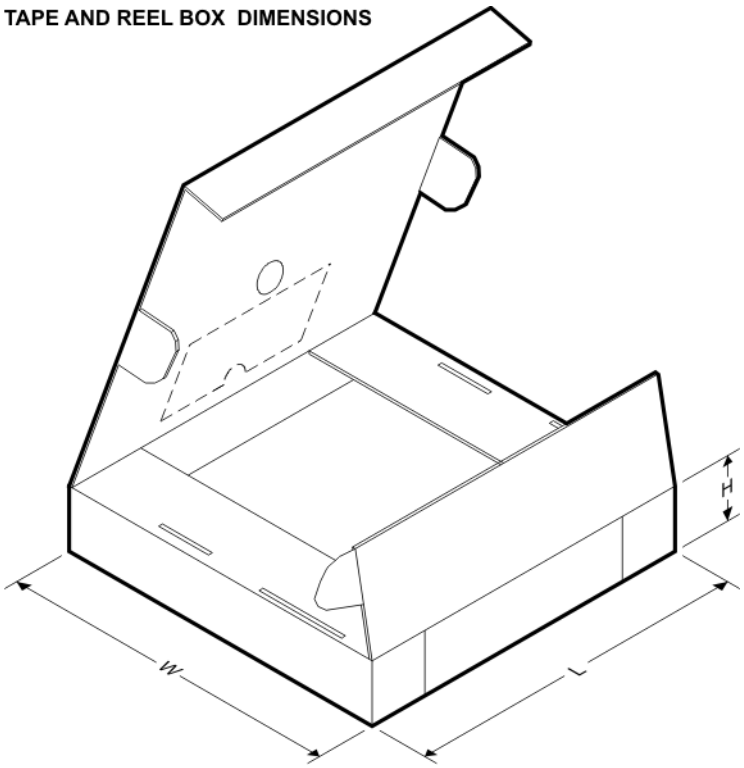
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3L110DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TS3L110DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
TS3L110DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TS3L110PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TS3L110RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

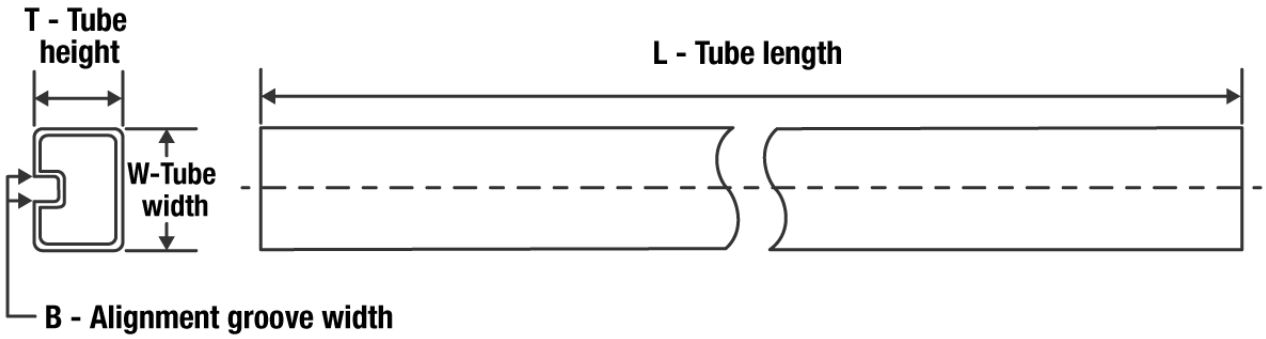
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3L110DBQR	SSOP	DBQ	16	2500	340.5	338.1	20.6
TS3L110DGVR	TVSOP	DGV	16	2000	853.0	449.0	35.0
TS3L110DR	SOIC	D	16	2500	340.5	336.1	32.0
TS3L110PWR	TSSOP	PW	16	2000	853.0	449.0	35.0
TS3L110RGYR	VQFN	RGY	16	3000	853.0	449.0	35.0

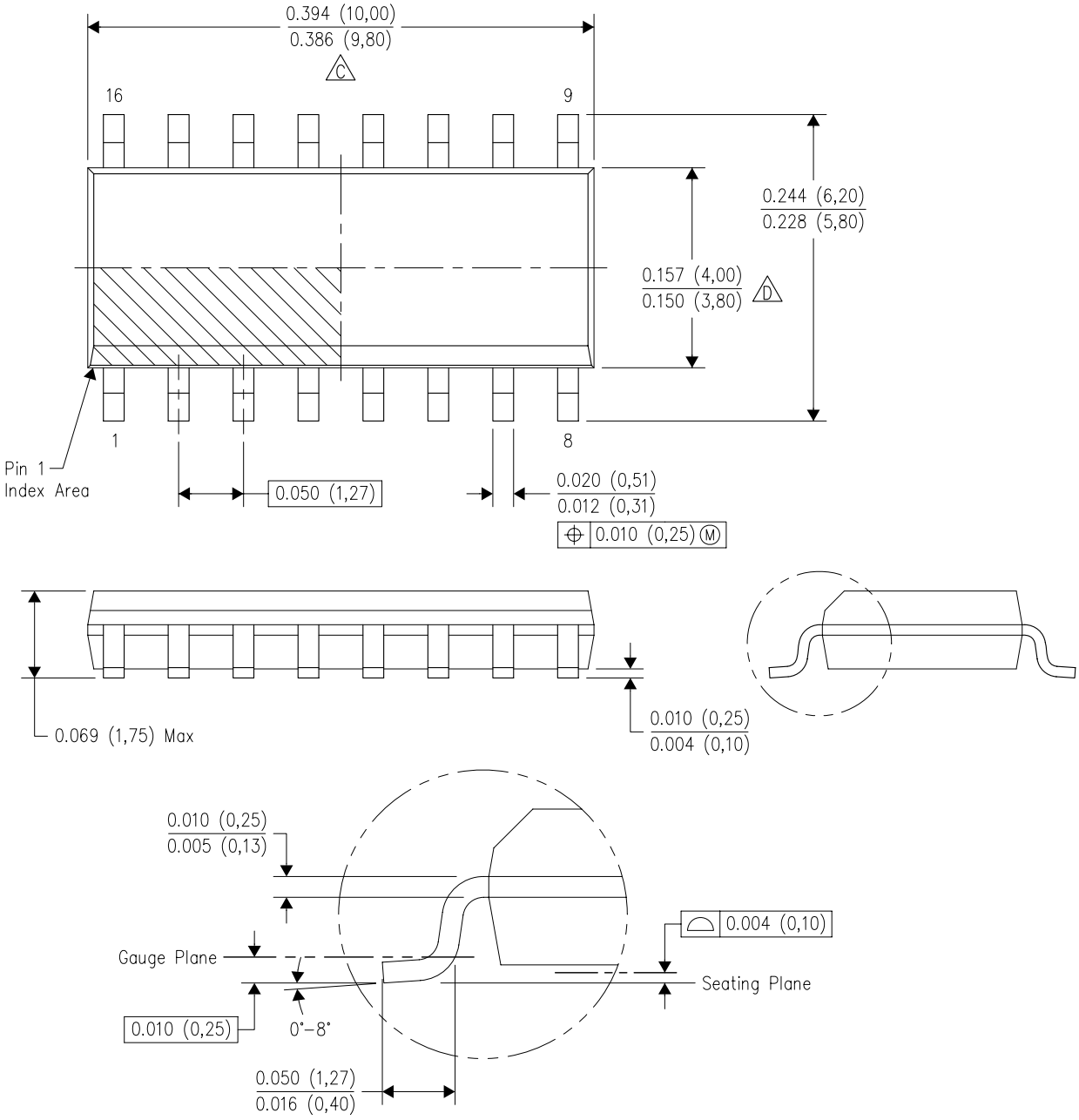
TUBE



*All dimensions are nominal

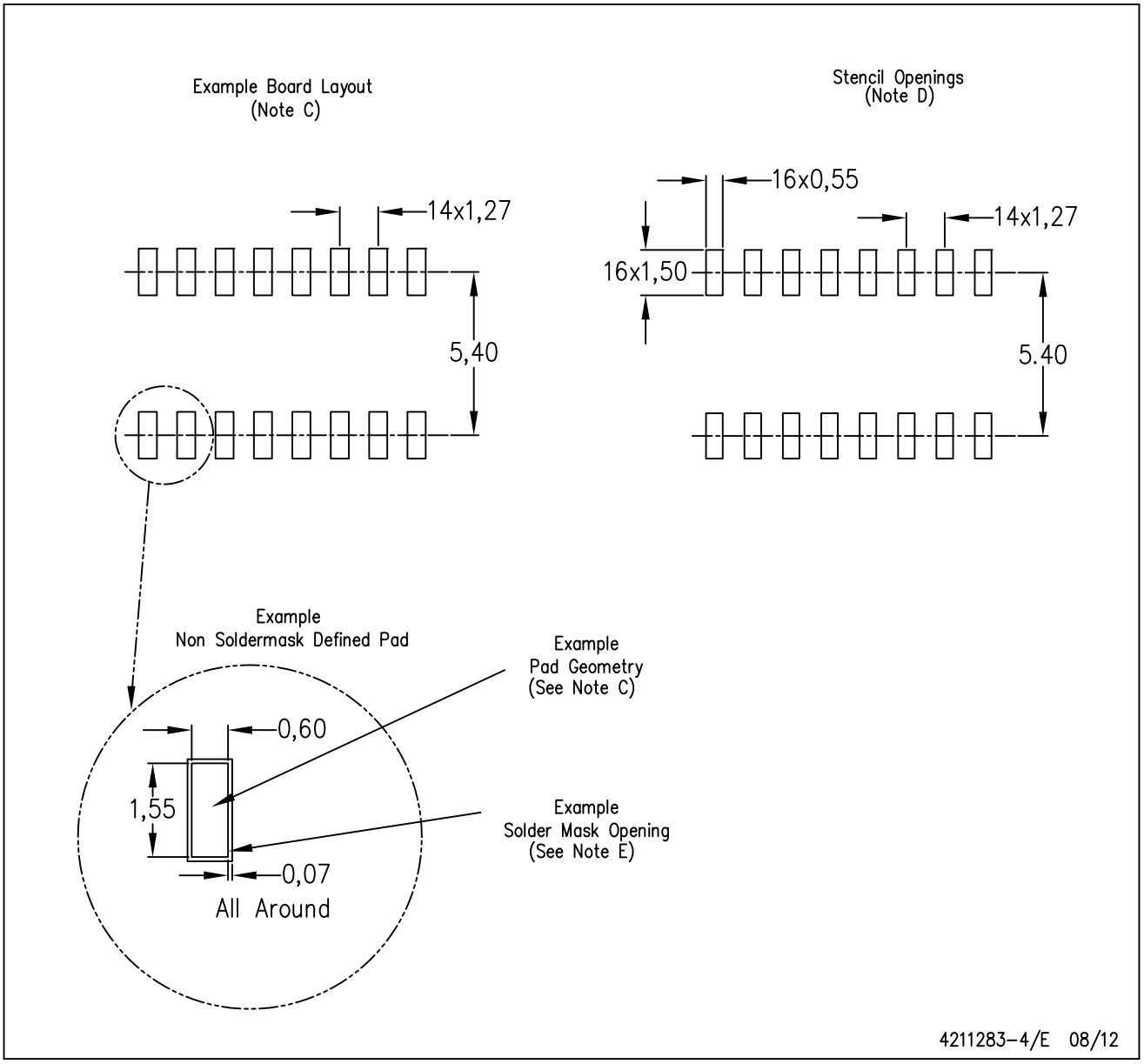
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TS3L110D	D	SOIC	16	40	507	8	3940	4.32
TS3L110DE4	D	SOIC	16	40	507	8	3940	4.32
TS3L110DG4	D	SOIC	16	40	507	8	3940	4.32
TS3L110PW	PW	TSSOP	16	90	530	10.2	3600	3.5

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



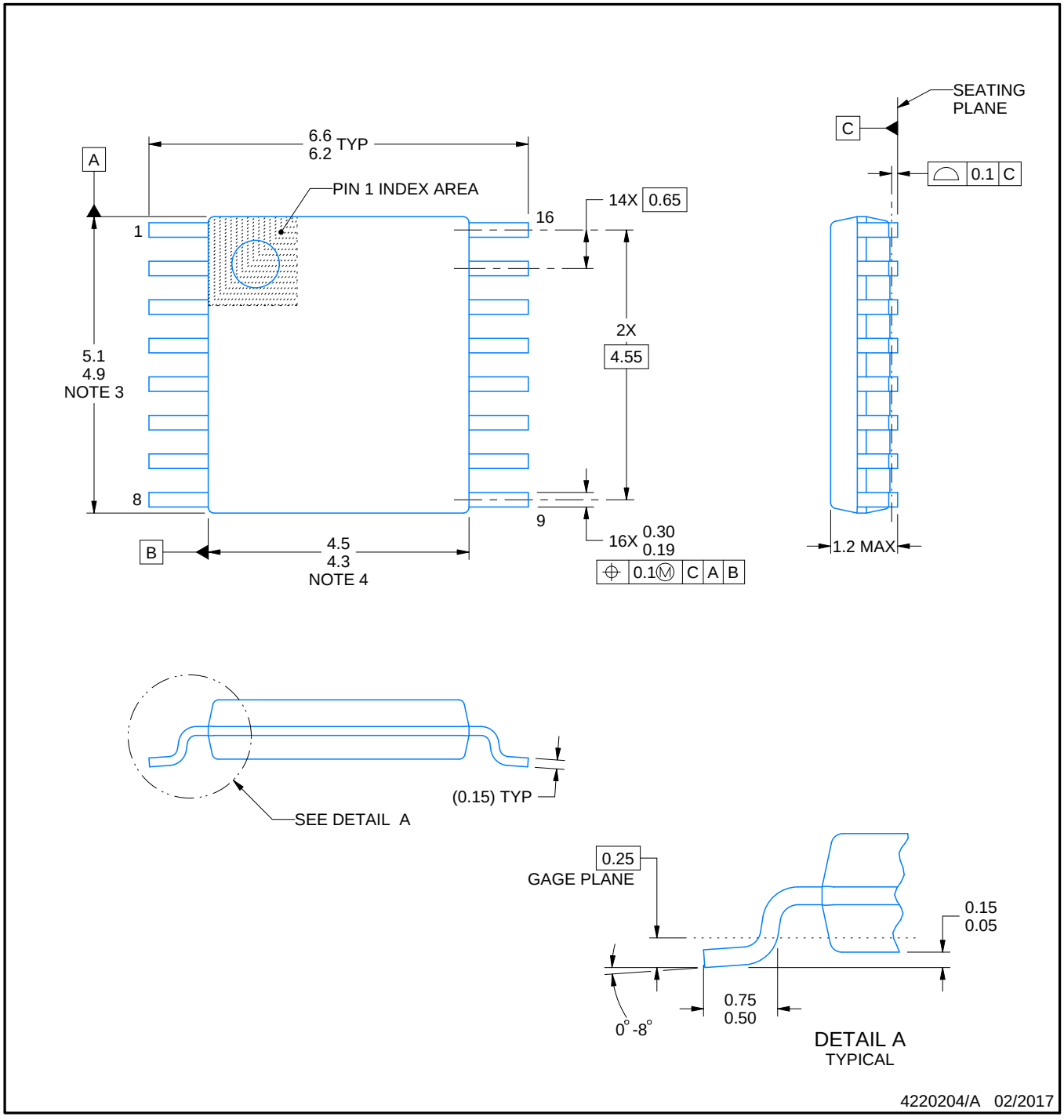
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

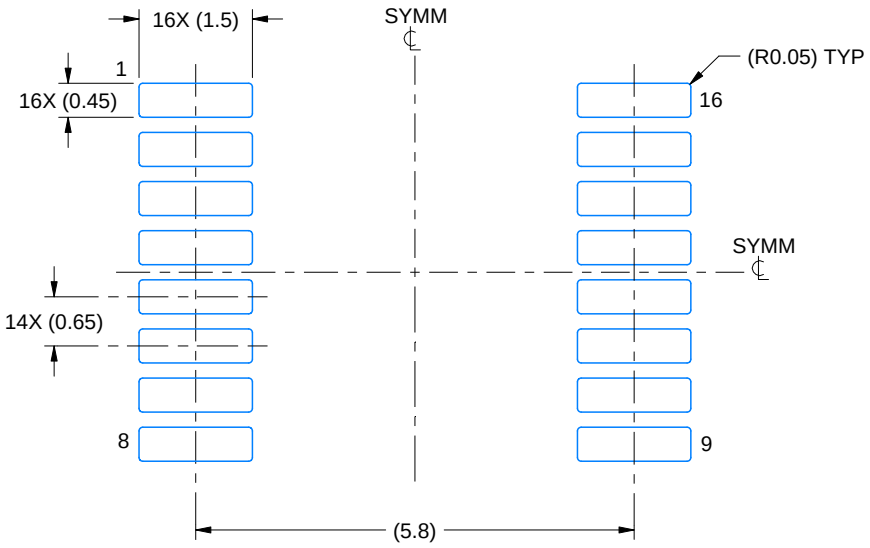
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

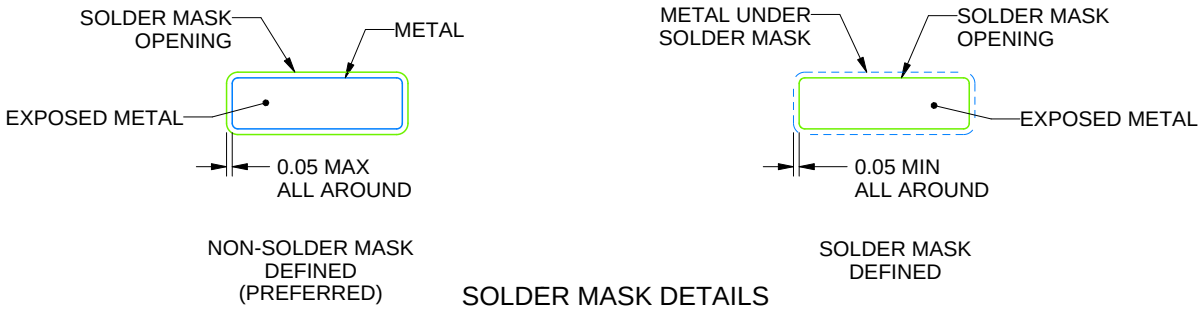


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

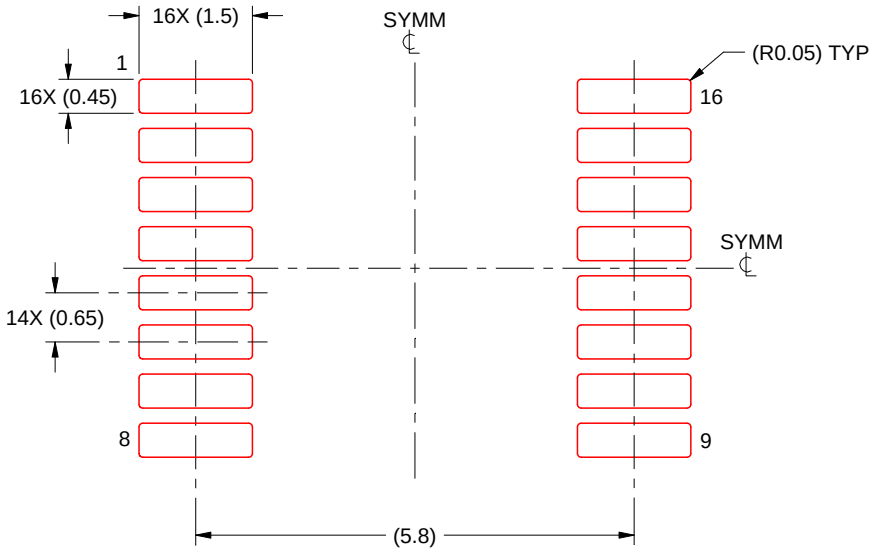


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

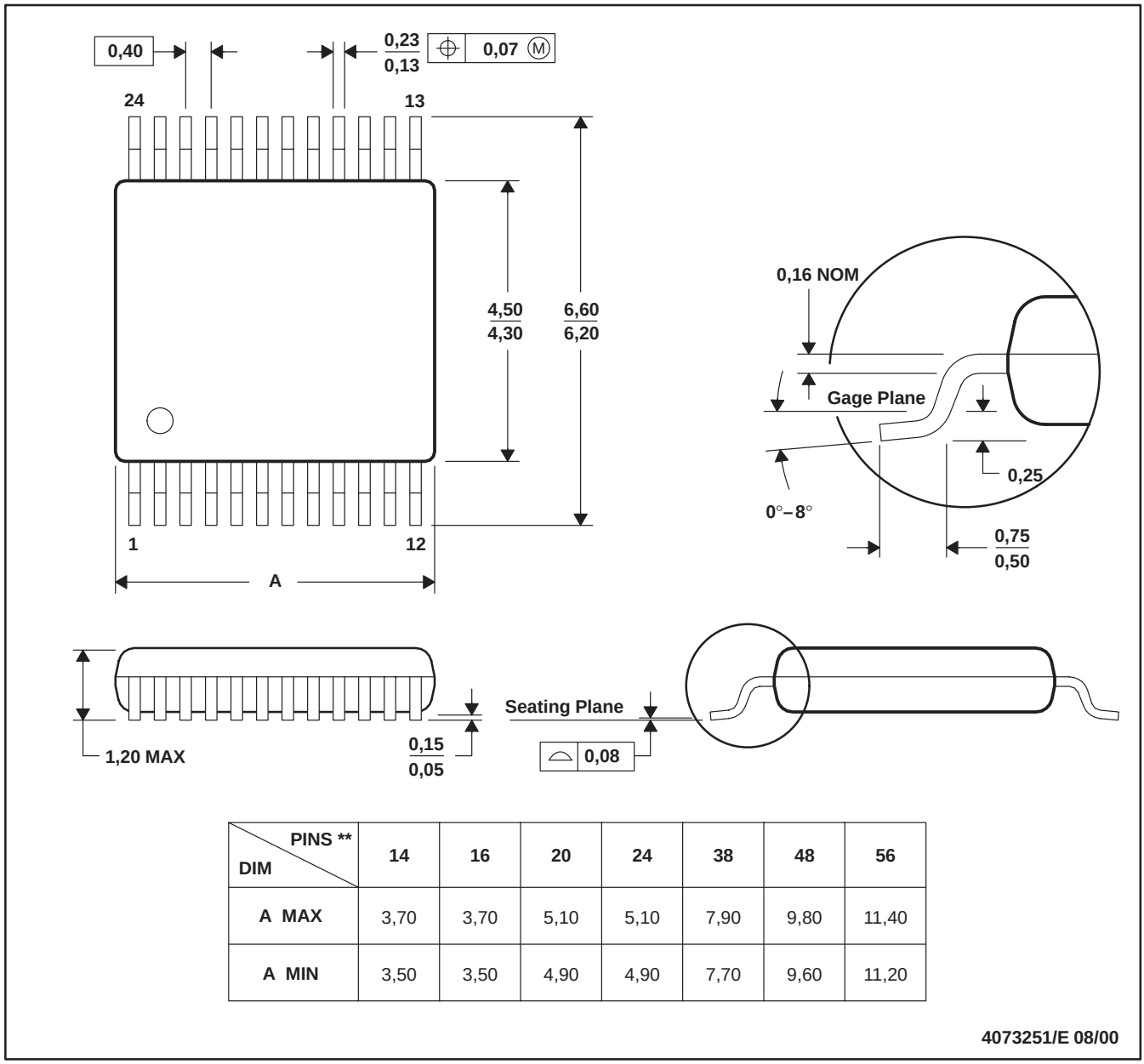
4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

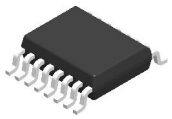
24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

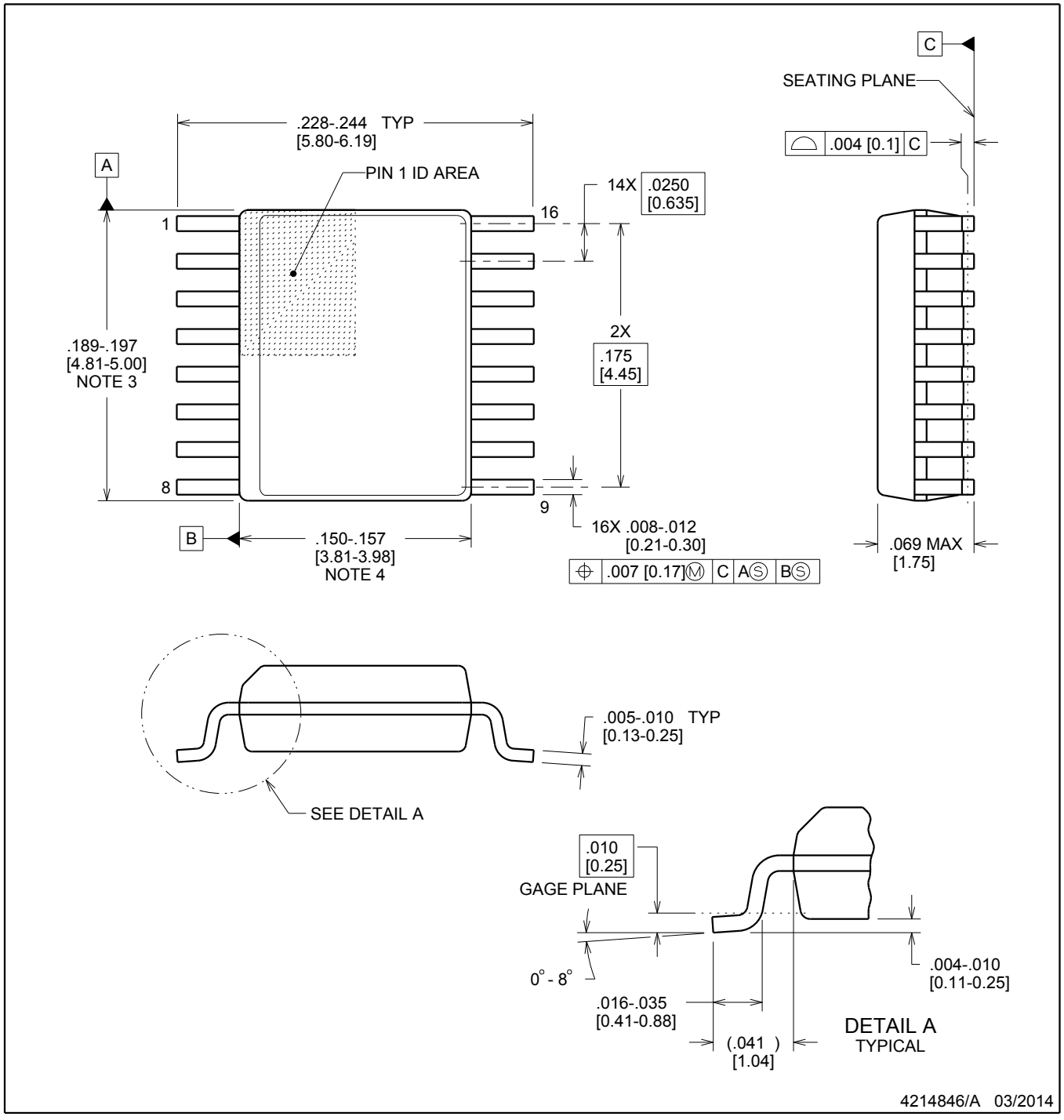


PACKAGE OUTLINE

DBQ0016A

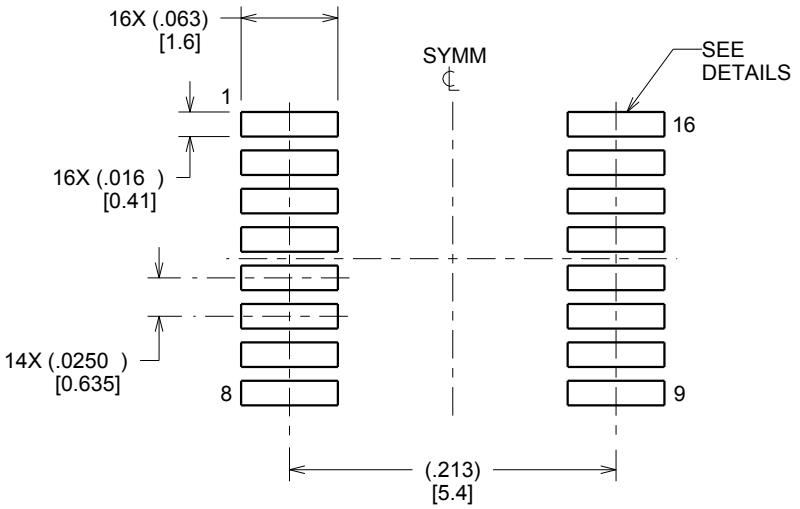
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

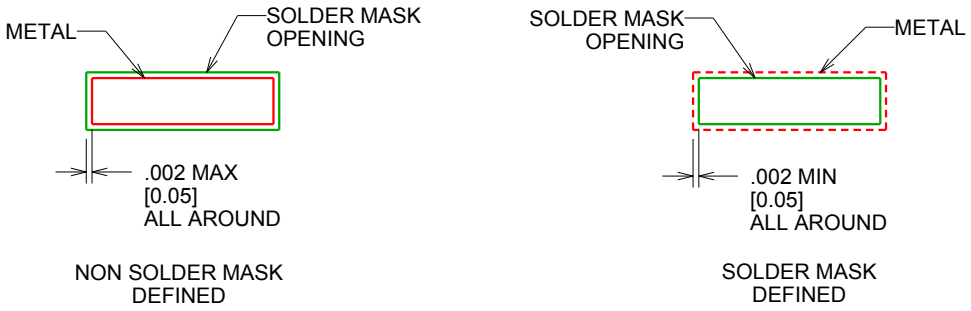


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

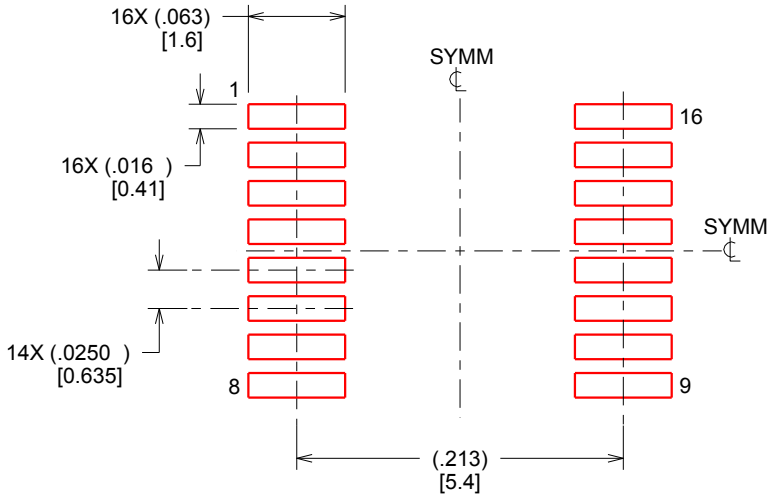
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



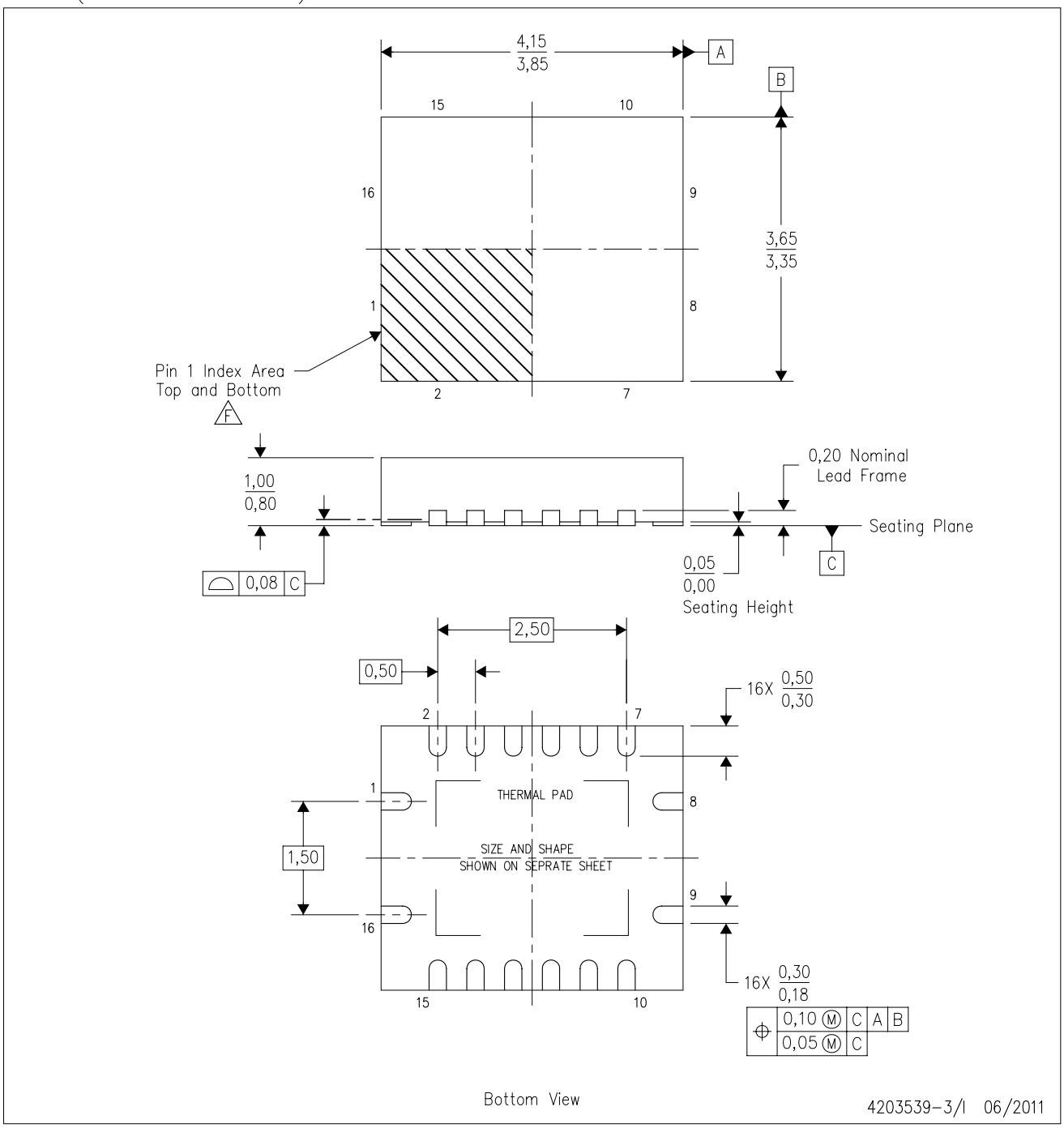
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

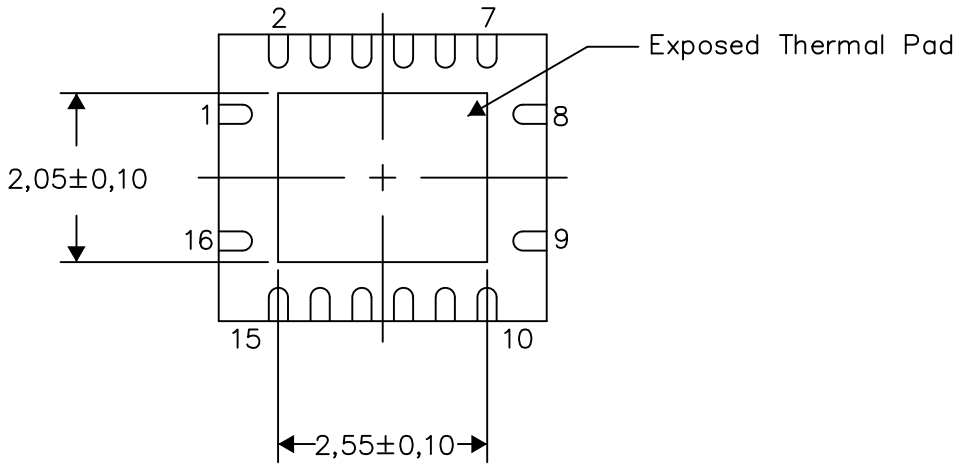
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



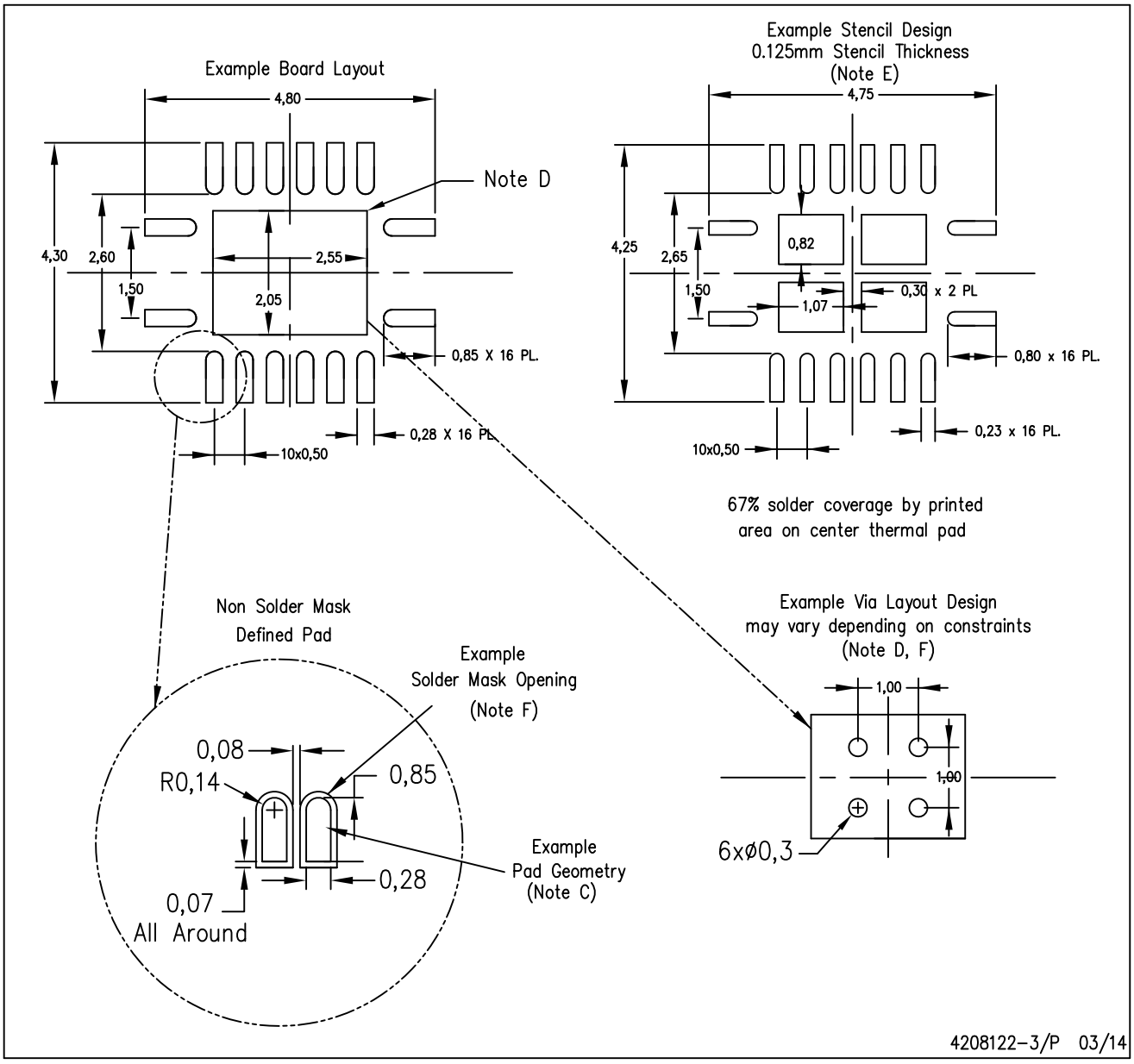
Bottom View

Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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