具有精确阈值的 TLV40x1 小尺寸、低功耗比较器

1 特性

- 宽电源电压范围：1.6V 至 5.5V
- 可调节阈值低至 0.2V 和 1.2V
- 3.2V 的固定阈值
- 高阈值精度
  - 25°C 时为 0.5%
  - 工作温度范围内精度为 1%
- 低静态电流：2µA
- 传播延迟：360ns
- 推挽和开漏输出选项
- 已知启动条件
- 同相和反相输入选项
- 精密迟滞
- 温度范围：-40°C 至 +125°C
- 封装：
  - 0.73mm × 0.73mm DSBGA（4 凸点）

2 应用

- 自诊断
- 锂离子电池监测
- 电池管理和保护
- 电流和电压感应
- 模拟前端
- 电源管理
- 非隔离式电源
- 负载点稳压器
- 直流/直流电源
- 交流/直流电源
- 系统控制和监控

3 说明

TLV40x1 器件是低功耗高精度比较器，具有精密阈值和 360ns 的传播延迟。这些比较器采用 0.73mm × 0.73mm 超小型 DSBGA 封装，使得 TLV40x1 适用于空间关键型设计，例如要求低功耗和对工作条件变化作出快速响应的便携式或电池供电设计。

经过出厂修整的开关阈值和精密迟滞相结合，使得 TLV40x1 非常适合在必须将慢速输入信号转换为纯净数字输出的严苛、嘈杂环境中进行电压和电流监测。同样地，输入端的短暂毛刺也得以抑制，因此可确保稳定的输出运行，不会引起误触发。

TLV40x1R1/2 提供多种配置，从而使系统设计人员可实现他们所需的输出响应和性能。例如，TLV4021 和 TLV4031 具有开漏输出级，而 TLV4041 和 TLV4051 具有推挽式输出级。此外，TLV4021 和 TLV4041 具有同相输入，而 TLV4031 和 TLV4051 具有反相输入。

器件信息 (1)

器件型号	封装	封装尺寸（标称值）
TLV40x1Ry、TLV4021S5	DSBGA (4)	0.73mm × 0.73mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

图 1. 持续电压监控器

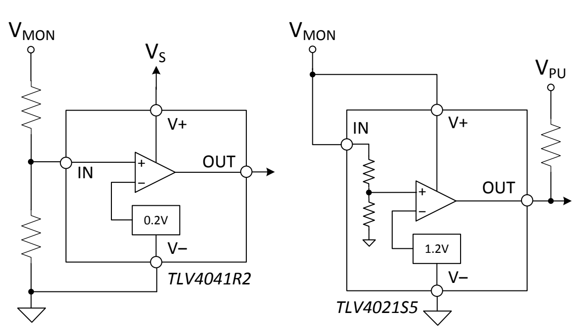

表 1. TLV40x1 系列内部基准比较器

器件	开关阈值	输入/输出配置
TLV4021R2	0.2V、0.18V	OD/同相
TLV4021R1	1.2V、1.18V	OD/同相
TLV4031R2	0.2V、0.18V	OD/反相
TLV4031R1	1.2V、1.18V	OD/反相
TLV4041R2	0.2V、0.18V	PP/同相
TLV4041R1	1.2V、1.18V	PP/同相
TLV4051R2	0.2V、0.18V	PP/反相
TLV4051R1	1.2V、1.18V	PP/反相
TLV4021S5	3.254V、3.2V	OD/同相

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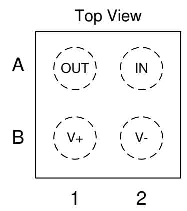
4 修订历史记录

Changes from Original (October 2018) to Revision A	Page
• 已更改 从“产品预览”更改为“生产数据”	1

5 Pin Configuration and Functions

YKA Package
4-Bump DSBGA
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
OUT	A1	O	Comparator output: OUT is push-pull on TLV4041/4051 and open-drain on TLV4021/4031
V+	B1	P	Positive (highest) power supply
V–	B2	P	Negative (lowest) power supply
IN	A2	I	Comparator input: IN is non-Inverting on TLV4021/4041 and inverting on TLV4031/4051

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)		–0.3	6	V
Input voltage (IN) from (V–) (2)		–0.3	6	V
Input Current (IN)(2)			±10	mA
Output voltage (OUT) from (V-)	TLV4021, TLV4031	–0.3	6	V
	TLV4041, TLV4051	–0.3	(V+) + 0.3	V
Output short-circuit duration(3)			10	s
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to (V–). Input signals that can swing more than 0.3 V below (V–) must be current-limited to 10 mA or less.
In addition, IN can be greater than (V+) and OUT as long as it is within the –0.3 V to 6 V range. Input signals that can swing beyond this range must be current-limited to 10 mA or less.
(3) Short-circuit to ground.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	1.6	5.5	V
Ambient temperature, T_A	–40	125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TLV40x1	UNIT
		YKA (DSBGA)	
		4 BUMPS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	205.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	74.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_S = 1.8 V to 5 V, typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Postive-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = 25°C	TLV40x1R2	0.197	0.2	0.203	V
	Postive-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = -40℃ to +125℃		0.196		0.204	
V_{IT-}	Negative-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = 25°C		0.177	0.18	0.183	
	Negative-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = -40°C to +125°C		0.176		0.184	
V_{IT+}	Postive-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = 25°C	TLV40x1R1	1.194	1.2	1.206	V
	Postive-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = -40℃ to +125℃		1.188		1.212	
V_{IT-}	Negative-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = 25°C		1.174	1.18	1.186	
	Negative-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = -40°C to +125°C		1.168		1.192	
V_{HYS} (1)	Input hysteresis voltage	V_S = 1.8 V and 5 V, T_A = 25℃	TLV40x1Ry		20		mV
V_{IT+}	Postive-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = 25°C	TLV4021S5	3.238	3.254	3.270	
	Postive-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = -40℃ to +125℃		3.221		3.287	
V_{IT-}	Negative-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = 25°C		3.184	3.2	3.216	
	Negative-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = -40℃ to +125℃		3.168		3.232	
V_{HYS} (1)	Input hysteresis voltage	V_S = 1.8 V and 5 V, T_A = 25°C	TLV40x1S5		54		mV
V_{IN}	Input voltage range	T_A = -40℃ to +125℃		V–		5.5	V
I_{BIAS}	Input bias current	Over V_{IN} range			10		pA
I_{BIAS}	Input bias current (TLV4021S5 only)	IN = 3.3 V			1.65		µA
V_{OL}	Voltage output swing from (V–)	I_{SINK} = 200 µA, OUT asserted low, V_S = 5 V, T_A = –40°C to +125°C				100	mV
		I_{SINK} = 3 mA, OUT asserted low, V_S = 5 V, T_A = –40°C to +125°C				400	mV
V_{OH}	Voltage output swing from (V+) (TLV4041/4051 only)	I_{SOURCE} = 200 µA, OUT asserted high, V_S = 5 V, T_A = –40°C to +125°C				100	mV
		I_{SOURCE} = 3 mA, OUT asserted high, V_S = 5 V, T_A = –40°C to +125°C				400	mV
$I_{O\text{-}LKG}$	Open-drain output leakage current (TLV4021/4031 only)	V_S = 5 V, OUT asserted high V_{PULLUP} = (V+), T_A = 25°C			20		pA
I_{SC}	Short-circuit current	V_S = 5 V, sinking, T_A = 25°C			55		mA
I_{SC}	Short-circuit current	V_S = 5 V, sourcing, T_A = 25°C (TLV4041/4051 only)			50		mA
I_Q	Quiescent current	No load, T_A = 25°C, Output Low, V_S = 1.8 V			2	3.5	µA
		No load, T_A = –40°C to +125°C, Output Low, V_S = 1.8 V				5	µA
V_{POR} (2)	Power-on reset voltage				1.45		V

(1) See Section 7.4.3 (Switching Thresholds and Hysteresis) for more details.
(2) See Section 7.4.1 (Power ON Reset) for more details.

6.6 Switching Characteristics

Typical values are at T_A = 25°C, V_S = 3.3 V, C_L = 15 pF; Input overdrive = 100 mV for TLV40x1Ry & 5% for TLV4021S5, R_P=4.99 kΩ for open-drain options (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay, high-to-low (1)	Midpoint of input to midpoint of output		360		ns
t_{PLH}	Propagation delay, low-to-high (1)	Midpoint of input to midpoint of output		360		ns
t_{PHL}	Propagation delay, high-to-low (1)(TLV4021S5 only)	Midpoint of input to midpoint of output		2		µs
t_{PLH}	Propagation delay, low-to-high (1)(TLV4021S5 only)	Midpoint of input to midpoint of output		2		µs
t_R	Rise time (TLV4041/4051 only)	20% to 80%		10		ns
t_F	Fall time	20% to 80%		10		ns
t_{ON}	Power-up time (2)			500		µs

(1) High-to-low and low-to-high refers to the transition at the input.
(2) During power on cycle, V_S must exceed 1.6 V for t_{ON} before the output will reflect the condition on the input. Prior to t_{ON} elapsing, the output is controlled by the POR circuit.

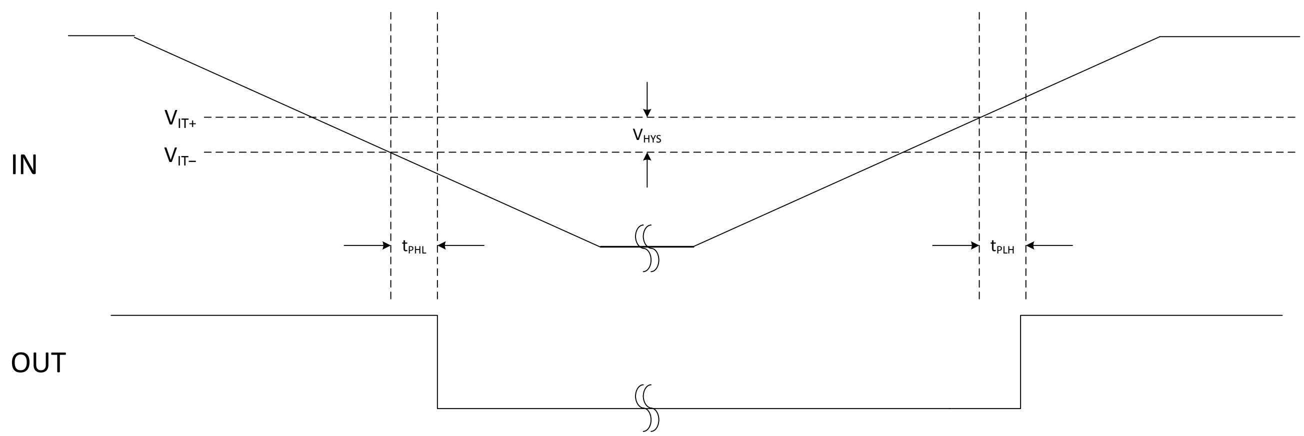


图 2. Timing Diagram Non-Inverting Input

6.7 Typical Characteristics

at T_J = 25°C and V_S = 3.3 V (unless otherwise noted)

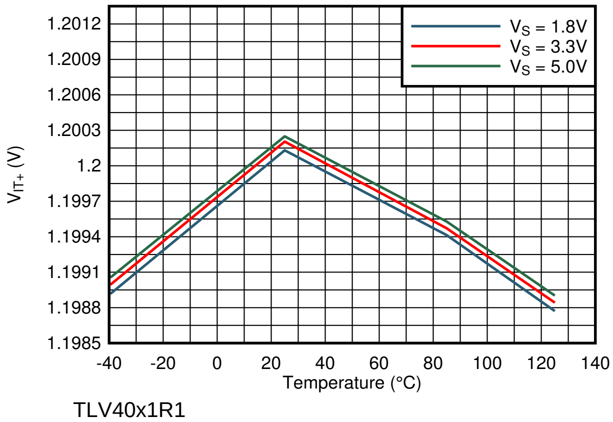


图 3. Positive Threshold vs Temperature

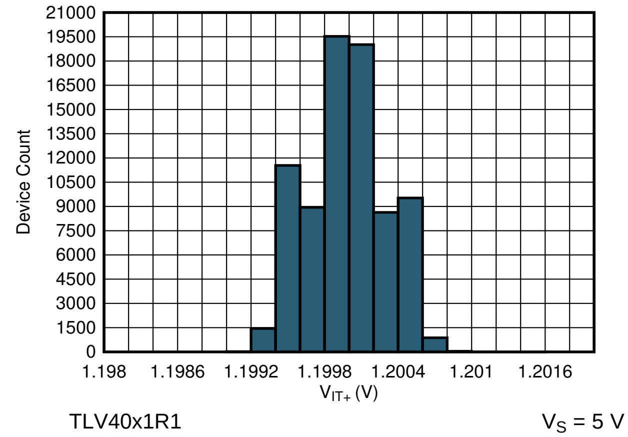


图 4. Positive Threshold Histogram

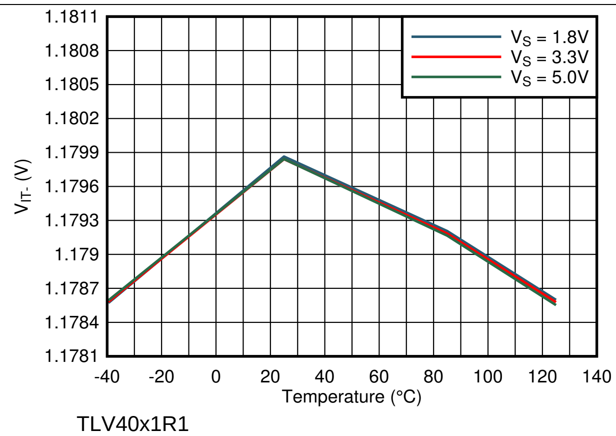


图 5. Negative Threshold vs Temperature

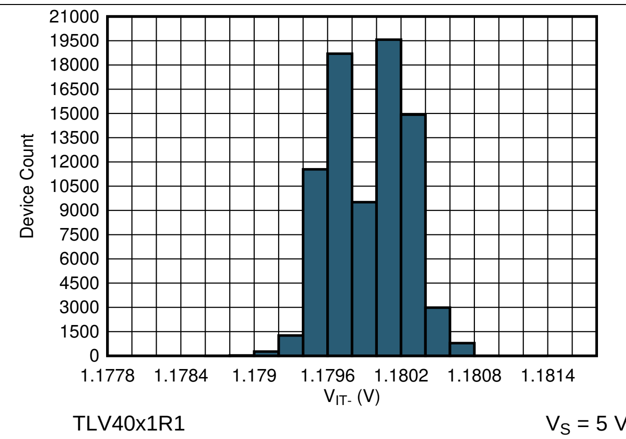


图 6. Negative Threshold Histogram

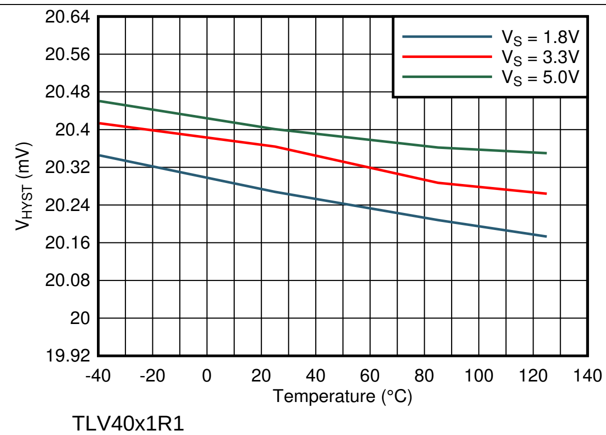


图 7. Hysteresis vs Temperature

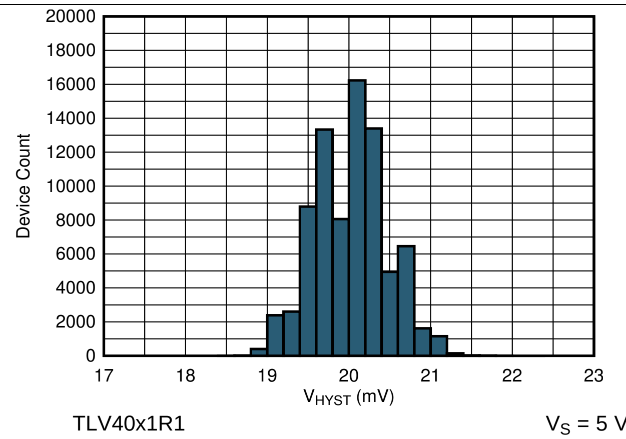


图 8. Hysteresis Histogram

Typical Characteristics (接下页)

at T_J = 25°C and V_S = 3.3 V (unless otherwise noted)

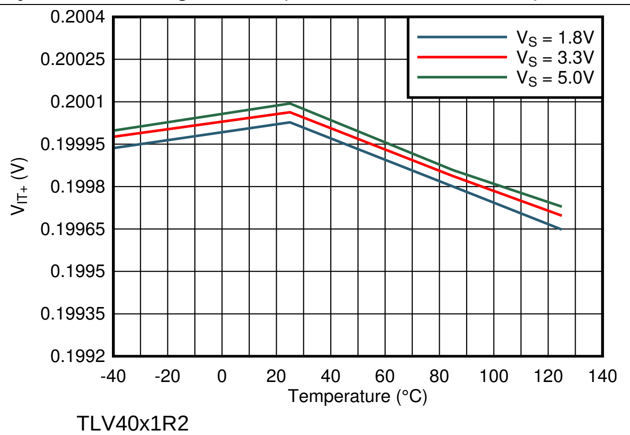


图 9. Positive Threshold vs Temperature

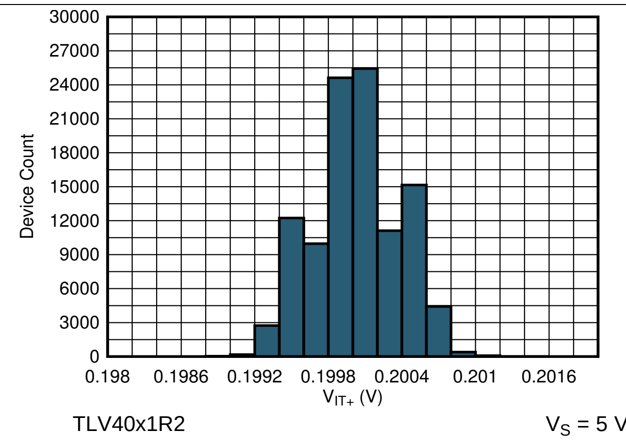


图 10. Positive Threshold Histogram

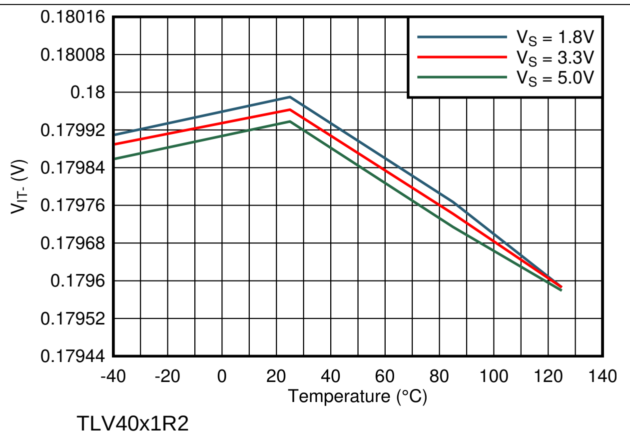


图 11. Negative Threshold vs Temperature

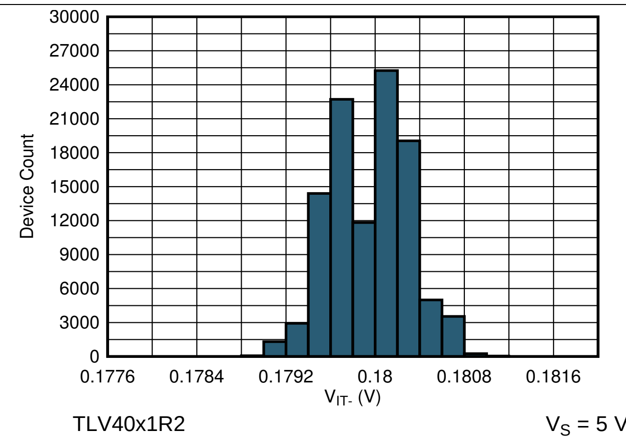


图 12. Negative Threshold Histogram

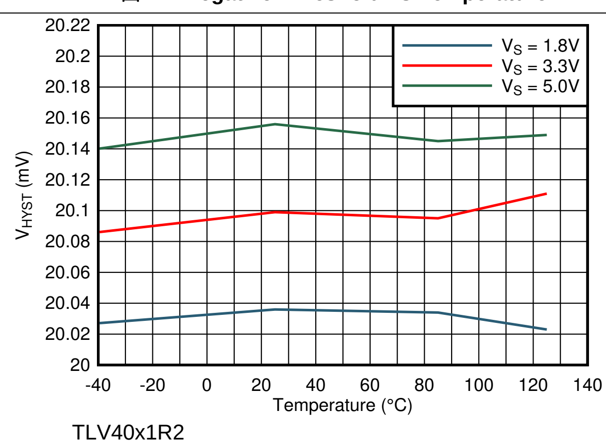


图 13. Hysteresis vs Temperature

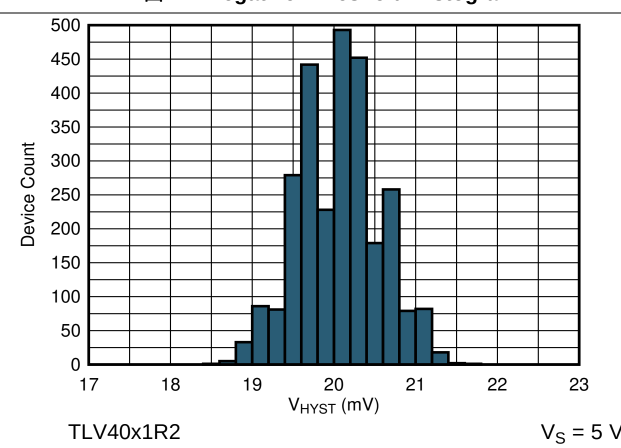


图 14. Hysteresis Histogram

Typical Characteristics (接下页)

at T_J = 25°C and V_S = 3.3 V (unless otherwise noted)

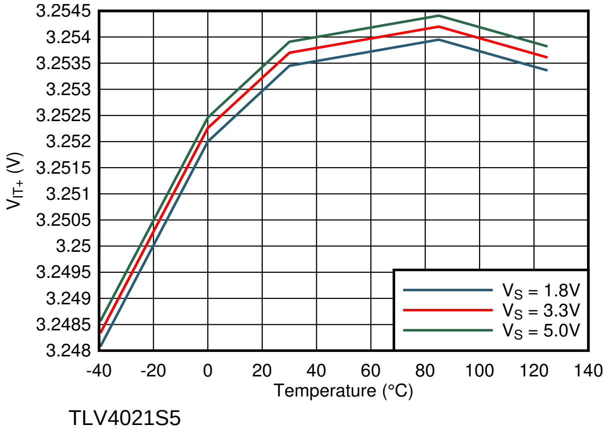


图 15. Positive Threshold vs Temperature

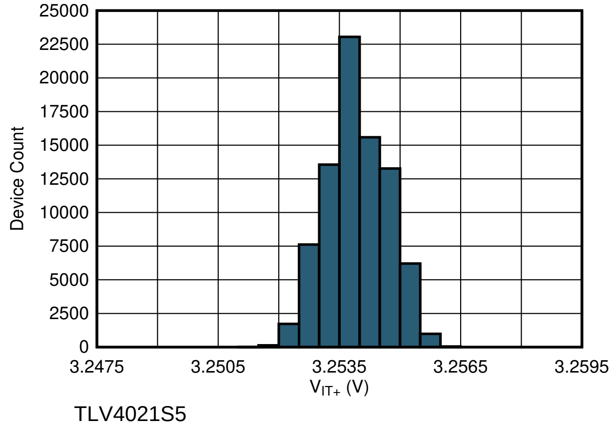


图 16. Positive Threshold Histogram

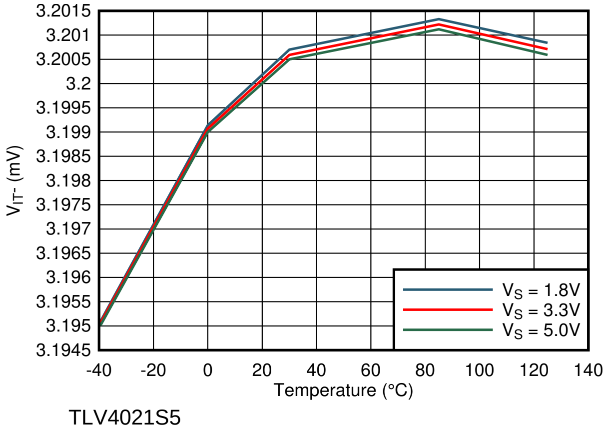


图 17. Negative Threshold vs Temperature

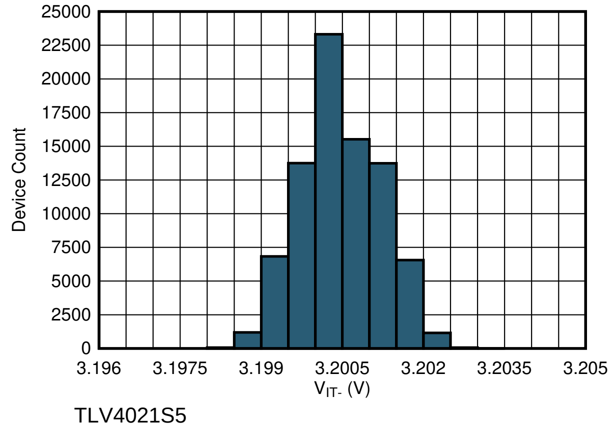


图 18. Negative Threshold Histogram

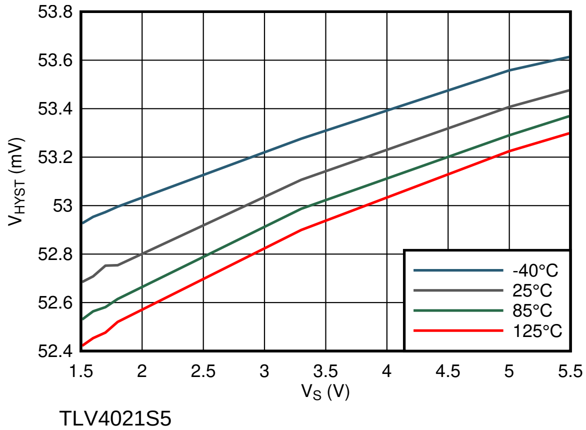


图 19. Hysteresis vs Supply Voltage

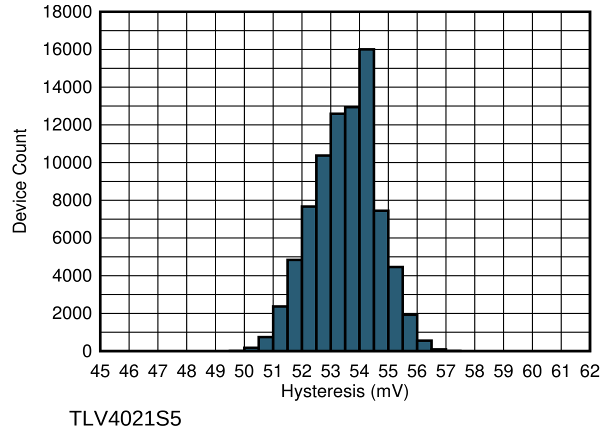


图 20. Hysteresis Histogram

Typical Characteristics (接下页)

at T_J = 25°C and V_S = 3.3 V (unless otherwise noted)

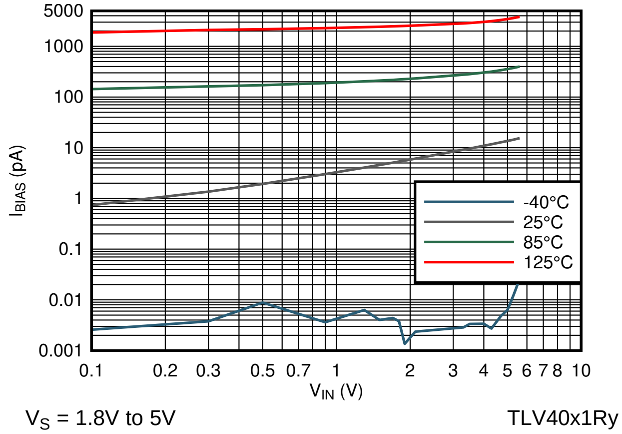


图 21. Bias Current vs Common Mode Voltage

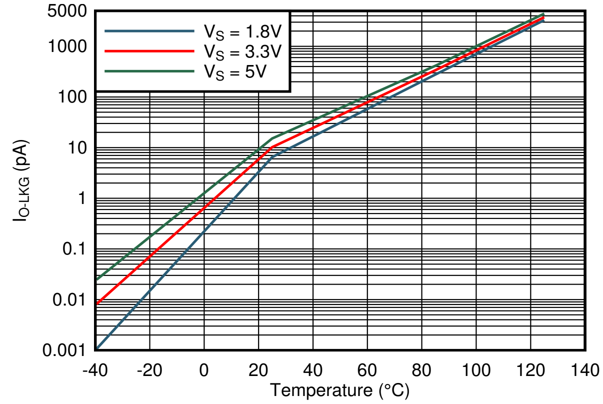


图 22. Output Current Leakage vs Temperature

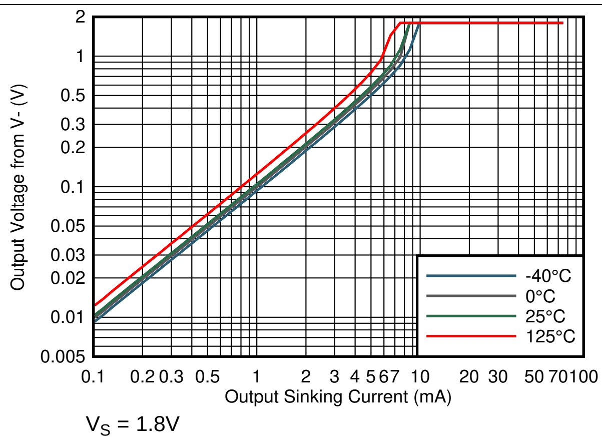


图 23. Output Voltage vs Output Sinking Current

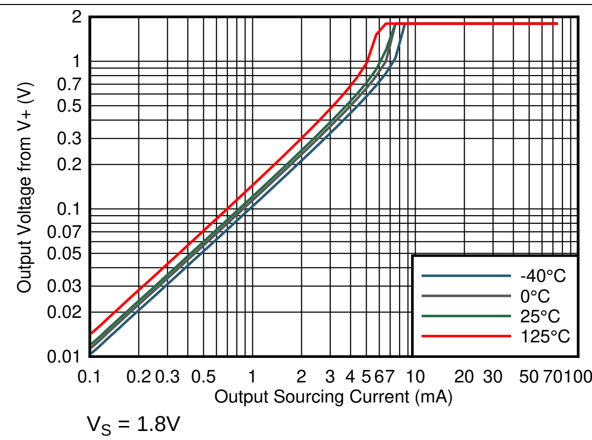


图 24. Output Voltage vs Output Sourcing Current

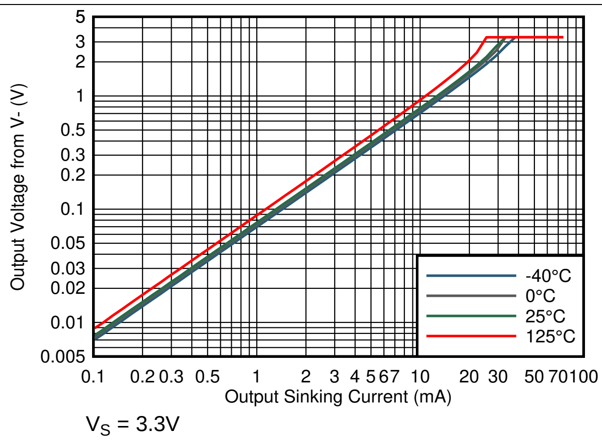


图 25. Output Voltage vs Output Sinking Current

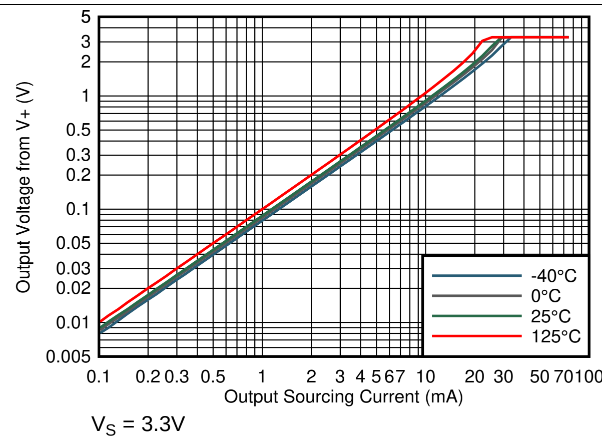


图 26. Output Voltage vs Output Sourcing Current

Typical Characteristics (接下页)

at T_J = 25°C and V_S = 3.3 V (unless otherwise noted)

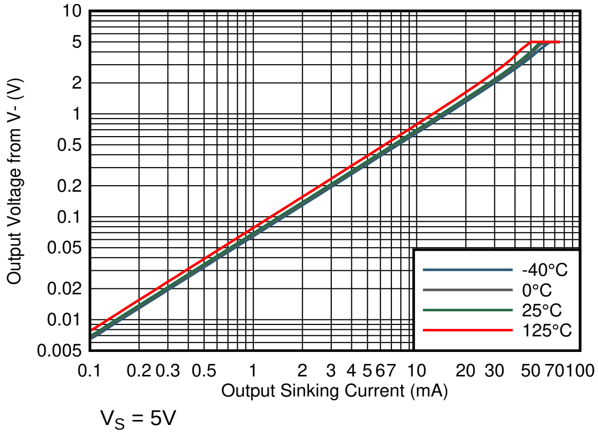


图 27. Output Voltage vs Output Sinking Current

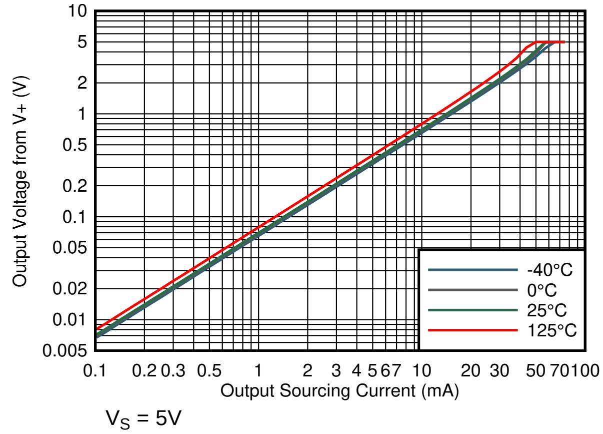


图 28. Output Voltage vs Output Sourcing Current

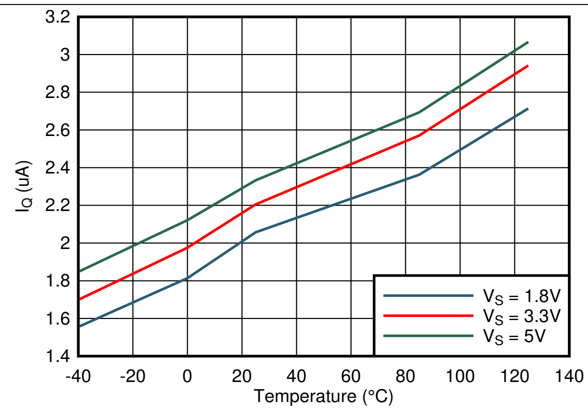


图 29. Supply Current vs Temperature

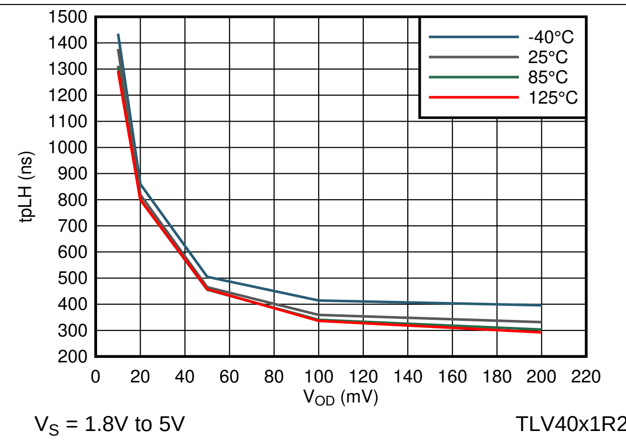


图 30. Propagation Delay Low-High vs Input Overdrive

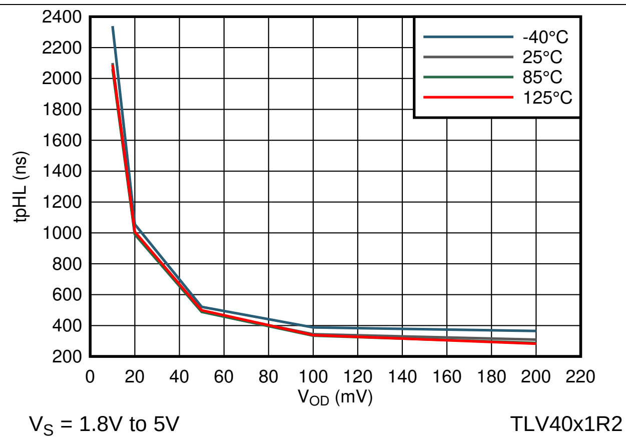


图 31. Propagation Delay High-Low vs Input Overdrive

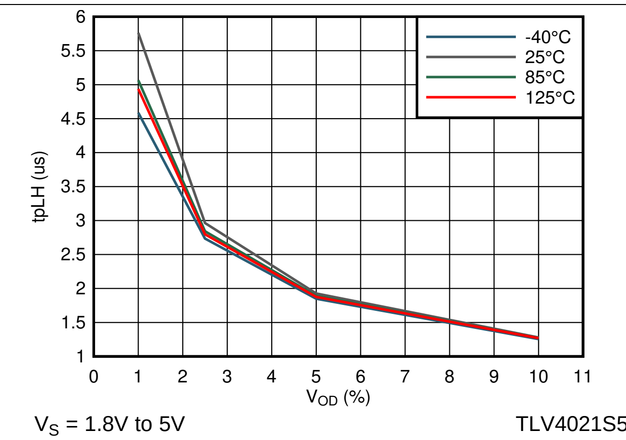
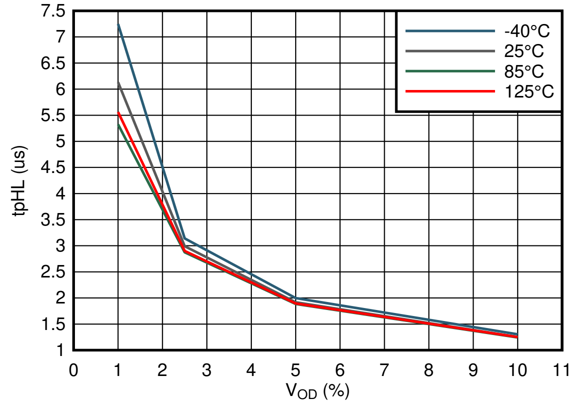


图 32. Propagation Delay Low-High vs Input Overdrive

Typical Characteristics (接下页)

at T_J = 25°C and V_S = 3.3 V (unless otherwise noted)



V_S = 1.8V to 5V

TLV4021S5

图 33. Propagation Delay High-Low vs Input Overdrive

7 Detailed Description

7.1 Overview

The TLV40x1 devices are low-power comparators that are well suited for compact, low-current, precision voltage detection applications. With high-accuracy, switching thresholds options of 0.2V, 1.2V, and 3.2V, 2uA of quiescent current, and propagation delay of 450ns and 2us, the TLV40x1 comparator family enables power conscious systems to monitor and respond quickly to fault conditions.

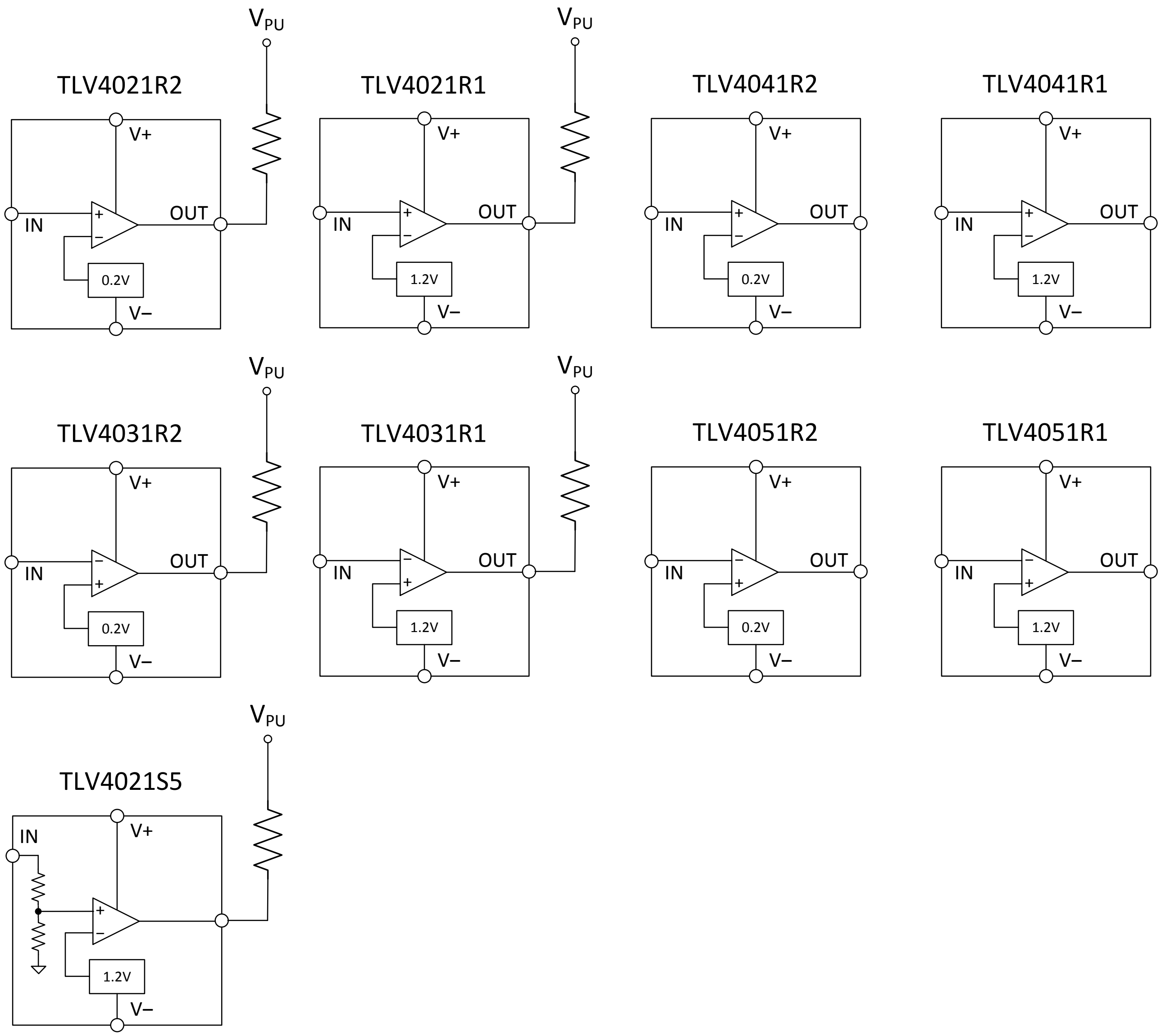
The TLV40x1Ry comparators assert the output signal as shown in 表 2. V_{IT+} represents the positive-going input threshold that causes the comparator output to change state, while V_{IT-} represents the negative-going input threshold that causes the output to change state. Since V_{IT+} and V_{IT-} are factory trimmed and warranted over temperature, the TLV40x1 is equally suited for undervoltage and overvoltage applications. In order to monitor any voltage above the internal reference voltage, an external resistor divider network is required.

The TLV4021S5 functions similar to the TLV40x1Ry comparators except the resistor divider is internal to the device. Having the resistor divider internal to the device allows the TLV4021S5 to have switching thresholds higher than the internal reference voltage of 1.2V without any external components.

表 2. TLV40x1 Truth Table

DEVICE	(V_{IT+}, V_{IT-})	OUTPUT TOPOLOGY	INPUT VOLTAGE	OUTPUT LOGIC LEVEL
TLV4021R2 TLV4021R1	0.2V, 0.18V 1.2V, 1.18V	Open-Drain	IN > V_{IT+}	Output high impedance
			IN < V_{IT-}	Output asserted low
TLV4041R2 TLV4041R1	0.2V, 0.18V 1.2V, 1.18V	Push-Pull	IN > V_{IT+}	Output asserted high
			IN < V_{IT-}	Output asserted low
TLV4031R2 TLV4031R1	0.2V, 0.18V 1.2V, 1.18V	Open-Drain	IN > V_{IT+}	Output asserted low
			IN < V_{IT-}	Output high impedance
TLV4051R2 TLV4051R1	0.2V, 0.18V 1.2V, 1.18V	Push-Pull	IN > V_{IT+}	Output asserted low
			IN < V_{IT-}	Output asserted high
TLV4021S5	3.254V, 3.2V	Open-Drain	IN > V_{IT+}	Output high impedance
			IN < V_{IT-}	Output asserted low

7.2 Functional Block Diagram



7.3 Feature Description

The TLV40x1 is a family of 4-pin, precision, low-power comparators with precision switching thresholds. The TLV40x1 comparators feature a rail-to-rail input stage with factory programmed switching thresholds for both rising and falling input waveforms. The comparator family also supports open-drain and push-pull output configurations as well as non-inverting and inverting inputs.

7.4 Device Functional Modes

7.4.1 Power ON Reset (POR)

The TLV40x1 comparators have a Power-on-Reset (POR) circuit which provides system designers a known start-up condition for the output of the comparators. When the power supply (V_S) is ramping up or ramping down, the POR circuit will be active when V_S is below V_{POR}. For the TLV4021 and TLV4031, the POR circuit will force the output to High-Z, and for the TLV4041 and TLV4051, the POR circuit will hold the output low at (V-). When V_S is greater than, or equal to, the minimum recommended operating voltage, the comparator output reflects the state of the input (IN).

The following pictures represent how the TLV40x1 outputs respond for V_S rising and falling. For the comparators with open-drain outputs (TLV4021/4031), IN is connected to (V-) to highlight the transition from POR circuit control to standard comparator operation where the output reflects the input condition. Note how the output goes low when V_S reaches 1.45V. Likewise, for the comparators with push-pull outputs (TLV4041/4051), the input is connected to (V+). Note how the output goes high when V_S reaches 1.45V.

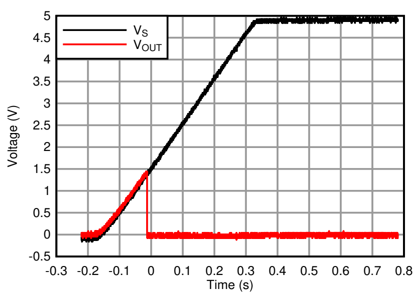


图 34. TLV4021/4031 Output for V_S Rising

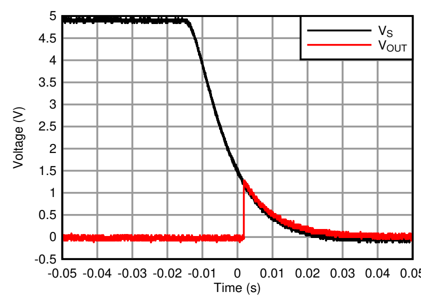


图 35. TLV4021/4031 Output for V_S Falling

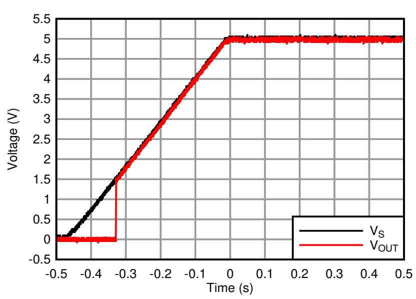


图 36. TLV4041/4051 Output for V_S Rising

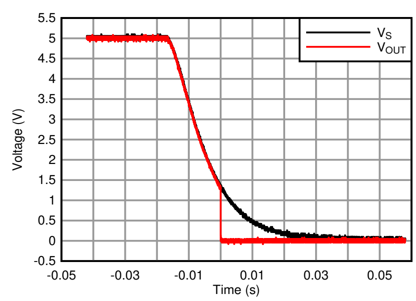


图 37. TLV4041/4051 Output for V_S Falling

7.4.2 Input (IN)

The TLV40x1 comparators have two inputs: one external input (IN) and one internal input that is connected to the integrated voltage reference. The comparator rising threshold is trimmed to the reference voltage (V_{IT+}) while the falling threshold is trimmed to (V_{IT-}). Since the rising and falling thresholds are both trimmed and warranted in the Electrical Characteristics Table, the TLV40x1 is equally suited for undervoltage and overvoltage detection. The difference between (V_{IT+}) and (V_{IT-}) is referred to as the comparator hysteresis and is 20 mV for TLV40x1Ry and 54 mV for TLV4021S5. The integrated hysteresis makes the TLV40x1 less sensitive to supply-rail noise and provides stable operation in noisy environments without having to add external positive feedback to create hysteresis.

Device Functional Modes (接下页)

The comparator input (IN) is able to swing 5.5 V above (V-) regardless of the device supply voltage. This includes the instance when no supply voltage is applied to the comparator (V_S = 0 V). As a result, the TLV40x1 is referred to as fault tolerant, meaning it maintains the same high input impedance when V_S is unpowered or ramping up. While not required in most cases, in order to reduce sensitivity to transients and layout parasitics for extremely noisy applications, place a 1 nF to 100 nF bypass capacitor at the comparator input.

For the TLV40x1Ry comparators, the input bias current is typically 10 pA for input voltages between (V-) and (V+) and the value typically doubles for every 10°C temperature increase. The comparator input is protected from voltages below (V-) by an internal diode connected to (V-). As the input voltage goes below (V-), the protection diode becomes forward biased and begins to conduct causing the input bias current to increase exponentially. A series resistor is recommended to limit the input current when sources have signal content that is less than (V-).

For the TLV4021S5, the input bias current is limited by the internal resistor divider with typical impedance of 2M ohms.

7.4.3 Switching Thresholds and Hysteresis (V_{HYS})

The TLV40x1 transfer curve is shown in 图 38.

- V_{IT+} represents the positive-going input threshold that causes the comparator output to change from a logic low state to a logic high state.
- V_{IT-} represents the negative-going input threshold that causes the comparator output to change from a logic high state to a logic low state.
- V_{HYS} represents the difference between V_{IT+} and V_{IT-} and is 20 mV for TLV40x1Ry and 54 mV for TLV4021S5.

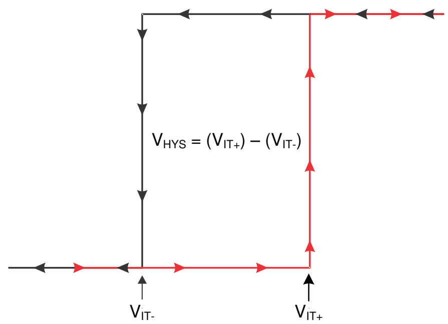


图 38. Transfer Curve

V_{IT+} and V_{IT-} have mV's of variation over temperature. The significant portion of the variation of these parameters is a result of the internal bandgap voltage from which V_{IT+} and V_{IT-} are derived. The following hysteresis histograms demonstrate the performance of the TLV40x1 hysteresis circuitry. Since the bandgap reference is used to set V_{IT+} and V_{IT-}, each of these parameters have a tendency to error (track) in the same direction. For example, if V_{IT+} has a positive 0.5% error, V_{IT-} would have a tendency to have a similar positive percentage error. As a result, the variation of hysteresis will never be equal to the difference of the highest V_{IT+} value of its range and the lowest V_{IT-} value of its range.

Device Functional Modes (接下页)

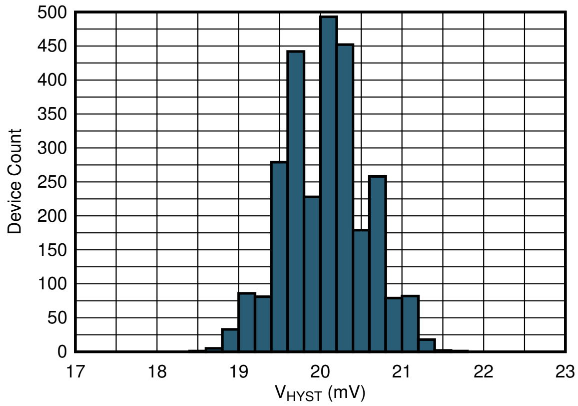


图 39. V_{HYST} Histogram (TLV40x1R2, V_S=5V)

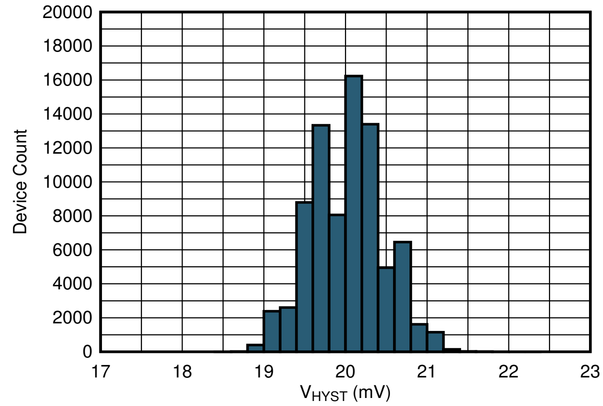


图 40. V_{HYST} Histogram (TLV40x1R1, V_S=5V)

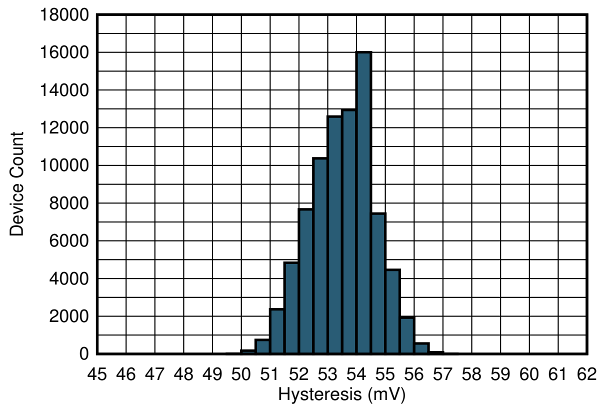


图 41. V_{HYST} Histogram (TLV40x1S5, V_S=5V)

7.4.4 Output (OUT)

The TLV4041 and TLV4051 feature a push-pull output stage which eliminates the need for an external pull-up resistor while providing a low impedance output driver. Likewise, the TLV4021 and TLV4031 feature an open-drain output stage which enables the output logic levels to be pulled-up to an external source as high as 5.5 V independent of the supply voltage.

In a typical TLV40x1 application, OUT is connected to an enable input of a processor or a voltage regulator such as a dc-dc converter or low-dropout regulator (LDO). The open-drain output versions (TLV4021/4031) are used if the power supply of the comparator is different than the supply voltage of the device being controlled. In this usage case, a pull-up resistor holds OUT high when the comparator output goes high impedance. The correct interface-voltage level is provided (also known as level-shifting) by connecting the pull-up resistor on OUT to the appropriate voltage rail. The TLV4021/4031 output can be pulled up to 5.5 V, independent of the device supply voltage (V_S). However, if level-shifting is not required, the push-pull output versions (TLV4041/4051) should be utilized in order to eliminate the need for the pull-up resistor.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV40x1 is a 4-pin, low-power comparator with a precision, integrated reference. The comparators in this family are well suited for monitoring voltages and currents in portable, battery powered devices.

8.1.1 Monitoring (V+)

Many applications monitor the same rail that is powering the comparator. In these applications the resistor divider is simply connected to the (V+) rail.

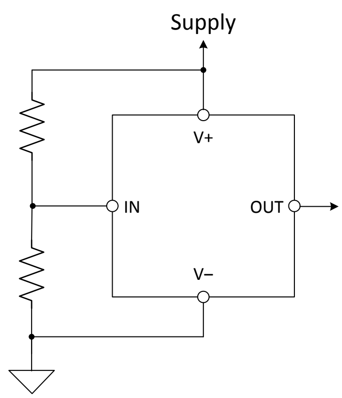


图 42. Supply Monitoring

Application Information (接下页)

8.1.2 Monitoring a Voltage Other than (V+)

Some applications monitor rails other than the one that is powering the comparator. In these applications the resistor divider used to set the desired threshold is connected to the rail that is being monitored.

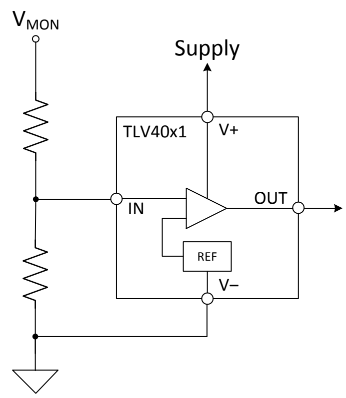


图 43. Monitoring a Voltage Other than the Supply

The TLV40x1Ry can monitor a voltage greater than the maximum (V+) with the use of an external resistor divider network. Likewise, the TLV40x1 can monitor voltages as low as the internal reference voltage (0.2 V or 1.2 V). The TLV40x1Ry also has the advantage of being able to monitor high impedance sources since the input bias current of the input (IN) is low. This provides an advantage over voltage supervisors that can only monitor the voltage rail that is powering them. Supervisors configured in this fashion have limitations in source impedance and minimum sensing voltage.

8.1.3 V_{PULLUP} to a Voltage Other than (V+)

For applications where the output of the comparator needs to interface with a reset/enable pin that operates from a different supply voltage, the open-drain comparators (TLV4021/4031) should be selected. In these usage cases, the output can be pulled up to any voltage that is lower than 5.5V (independent of (V+)). This technique is commonly referred to as "level-shifting."

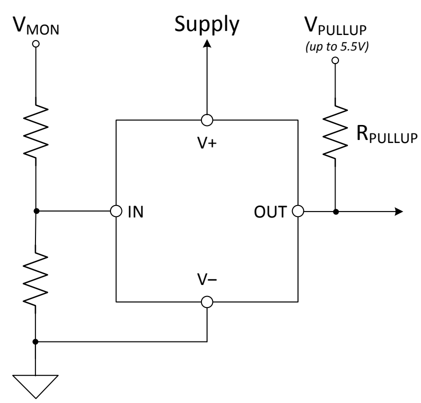


图 44. Level-Shifting

8.2 Typical Application

8.2.1 Under-Voltage Detection

Under-voltage detection is frequently required in battery-powered, portable electronics to alert the system that a battery voltage has dropped below the usable voltage level. 图 45 shows a simple under-voltage detection circuit using the TLV4041R1 which is a non-inverting comparator with an integrated 1.2 V reference and a push-pull output stage. The non-inverting TLV4041 option was selected in this example since the micro-controller required an active low signal when an undervoltage level occurs. However, if an active high signal was required, the TLV4051 option with an inverting input stage would be utilized.

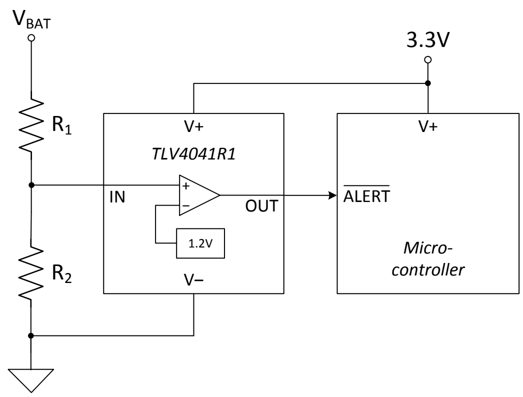


图 45. Under-Voltage Detection

8.2.1.1 Design Requirements

For this design, follow these design requirements:

- Operate from 3.3 V power supply that powers the microcontroller.
- Under-voltage alert is active low.
- Logic low output when V_{BAT} is less than 2.0V.

8.2.1.2 Detailed Design Procedure

Configure the circuit as shown in 图 45. Connect (V+) to 3.3 V which also powers the micro-controller. Resistors R_1 and R_2 create the under-voltage alert level of 2.0 V. When the battery voltage sags down to 2.0 V, the resistor divider voltage crosses the (V_{IT-}) threshold of the TLV4041R1. This causes the comparator output to transition from a logic high to a logic low. The push-pull option of the TLV40x1 family is selected since the comparator operating voltage is shared with the microcontroller which is receiving the under-voltage alert signal. The TLV4041 option with the 1.2 V internal reference is selected because it is the closest internal reference option that is less than the critical under-voltage level of 2.0 V. Choosing the internal reference option that is closest to the critical under-voltage level minimizes the resistor divider ratio which optimizes the accuracy of the circuit. Error at the falling edge threshold of (V_{IT-}) is amplified by the inverse of the resistor divider ratio. So minimizing the resistor divider ratio is a way of optimizing voltage monitoring accuracy.

公式 1 is derived from the analysis of 图 45.

$$V_{IT-} = \frac{R_2}{R_1 + R_2} \times V_{BAT} \quad (1)$$

where

- R_1 and R_2 are the resistor values for the resistor divider connected to IN
- V_{BAT} is the voltage source that is being monitored for an undervoltage condition.
- V_{IT-} is the falling edge threshold where the comparator output changes state from high to low

Rearranging 公式 1 and solving for R_1 yields 公式 2.

Typical Application (接下页)

$$R_1 = \frac{(V_{BAT} - V_{IT-})}{V_{IT-}} \times R_2 \quad (2)$$

For the specific undervoltage detection of 2.0 V using the TLV4041R1, the following results are calculated.

$$R_1 = \frac{(2.0 - 1.18)}{1.18} \times 1M = 695\ k\Omega \quad (3)$$

where

- R_2 is set to 1 MΩ
- V_{BAT} is set to 2.0 V
- V_{IT-} is set to1.18 V

Choose R_{TOTAL} (R_1 + R_2) such that the current through the divider is at least 100 times higher than the input bias current (I_{BIAS}). The resistors can have high values to minimize current consumption in the circuit without adding significant error to the resistive divider.

8.2.1.3 Application Curve

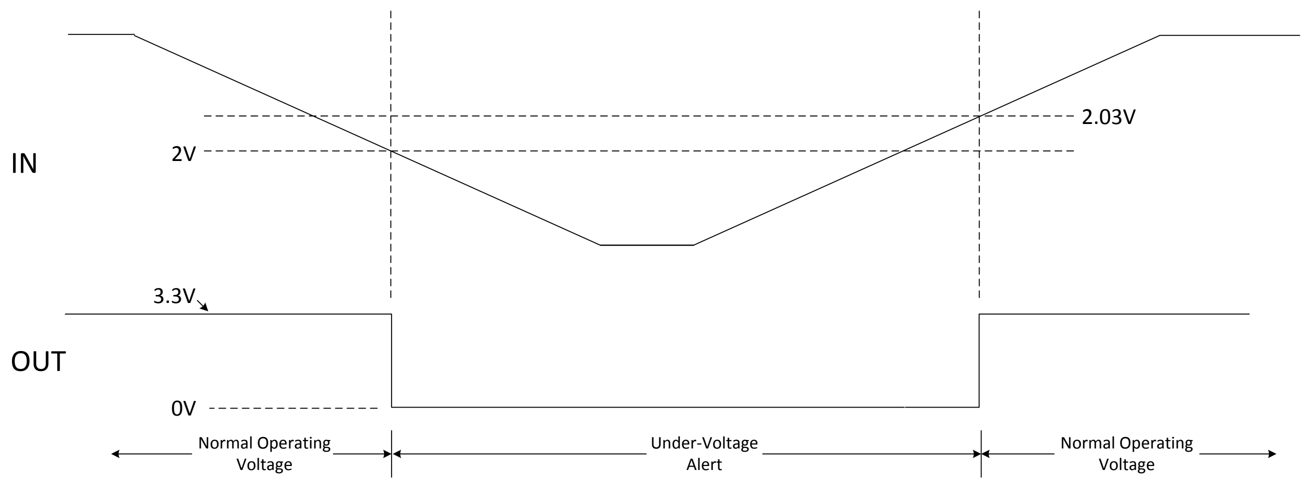


图 46. Under-Voltage Detection

8.2.2 Additional Application Information

8.2.2.1 Pull-up Resistor Selection

For the TLV4021 (open-drain output versions of the TLV40x1 family), care should be taken in selecting the pull-up resistor (R_{PU}) value to ensure proper output voltage levels. First, consider the required output high logic level requirement of the logic device that is being driven by the comparator when calculating the maximum R_{PU} value. When in a logic high output state, the output impedance of the comparator is very high but there is a finite amount of leakage current that needs to be accounted for. Use $I_{O\text{-}LKG}$ from the EC Table and the V_{IH} minimum from the logic device being driven to determine R_{PU} maximum using 公式 4.

$$R_{PU}(max) = \frac{(V_{PU} - V_{IH(min)})}{I_{O-LKG}} \quad (4)$$

Typical Application (接下页)

Next, determine the minimum value for R_{PU} by using the V_{IL} maximum from the logic device being driven. In order for the comparator output to be recognized as a logic low, V_{IL} maximum is used to determine the upper boundary of the comparator's V_{OL}. V_{OL} maximum for the comparator is available in the EC Table for specific sink current levels and can also be found from the V_{OUT} versus I_{SINK} curve in the Typical Application curves. A good design practice is to choose a value for V_{OL} maximum that is 1/2 the value of V_{IL} maximum for the input logic device. The corresponding sink current and V_{OL} maximum value will be needed to calculate the minimum R_{PU}. This method will ensure enough noise margin for the logic low level. With V_{OL} maximum determined and the corresponding I_{SINK} obtained, the minimum R_{PU} value is calculated with 公式 5.

$$R_{PU}(\min) = \frac{(V_{PU} - V_{OL(max)})}{I_{SINK}} \quad (5)$$

Since the range of possible R_{PU} values is large, a value between 5 kΩ and 100 kΩ is generally recommended. A smaller R_{PU} value provides faster output transition time and better noise immunity, while a larger R_{PU} value consumes less power when in a logic low output state.

8.2.2.2 Input Supply Capacitor

Although an input capacitor is not required for stability, for good analog design practice, connect a 100 nF low equivalent series resistance (ESR) capacitor from (V+) to (V-).

8.2.2.3 Sense Capacitor

Although not required in most cases, for extremely noisy applications, place a 1 nF to 100 nF bypass capacitor from the comparator input (IN) to the (V-) for good analog design practice. This capacitor placement reduces device sensitivity to transients.

8.3 What to Do and What Not to Do

Do connect a 100 nF decoupling capacitor from (V+) to (V-) for best system performance.

If the monitored voltage is noisy, do connect a decoupling capacitor from the comparator input (IN) to (V-).

Don't use resistors for the voltage divider that cause the current through them to be less than 100 times the input current of the comparator without also accounting for the impact on accuracy.

Don't use a pull-up resistor that is too small because the larger current sunk by the output may exceed the desired low-level output voltage (V_{OL}).

9 Power Supply Recommendations

These devices operate from an input voltage supply range between 1.7 V and 5.5 V.

10 Layout

10.1 Layout Guidelines

A power supply bypass capacitor of 100 nF is recommended when supply output impedance is high, supply traces are long, or when excessive noise is expected on the supply lines. Bypass capacitors are also recommended when the comparator output drives a long trace or is required to drive a capacitive load. Due to the fast rising and falling edge rates and high-output sink and source capability of the TLV40x1 output stage, higher than normal quiescent current can be drawn from the power supply when the output transitions. Under this circumstance, the system would benefit from a bypass capacitor across the supply pins.

10.2 Layout Example

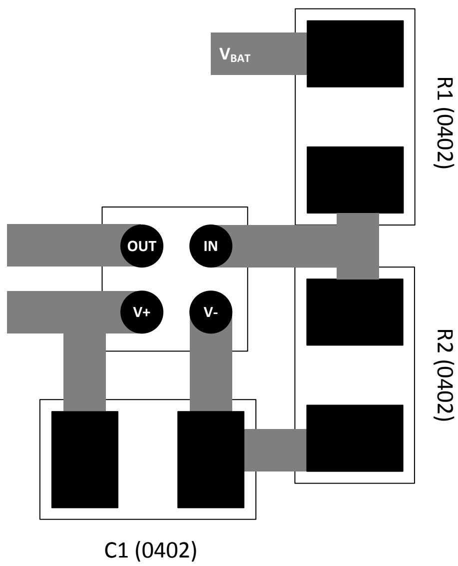


图 47. Layout Example

11 器件和文档支持

11.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 **3.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
TLV4021	单击此处	单击此处	单击此处	单击此处	单击此处
TLV4031	单击此处	单击此处	单击此处	单击此处	单击此处
TLV4041	单击此处	单击此处	单击此处	单击此处	单击此处
TLV4051	单击此处	单击此处	单击此处	单击此处	单击此处

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

E2E is a trademark of Texas Instruments.

11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV4021R1YKAR	ACTIVE	DSBGA	YKA	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Z	Samples
TLV4021R2YKAR	ACTIVE	DSBGA	YKA	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	6	Samples
TLV4021S5MYKAR	ACTIVE	DSBGA	YKA	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Q	Samples
TLV4021S5YKAR	ACTIVE	DSBGA	YKA	4	3000	RoHS & Green	SAC396 | SNAGCU	Level-1-260C-UNLIM	-40 to 125	O	Samples
TLV4031R1YKAR	ACTIVE	DSBGA	YKA	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1	Samples
TLV4031R2YKAR	ACTIVE	DSBGA	YKA	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	7	Samples
TLV4041R1YKAR	ACTIVE	DSBGA	YKA	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	2	Samples
TLV4041R2YKAR	ACTIVE	DSBGA	YKA	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8	Samples
TLV4041R5DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	23XT	Samples
TLV4051R1YKAR	ACTIVE	DSBGA	YKA	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C	Samples
TLV4051R2YKAR	ACTIVE	DSBGA	YKA	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9	Samples
TLV4051R5DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	23ZT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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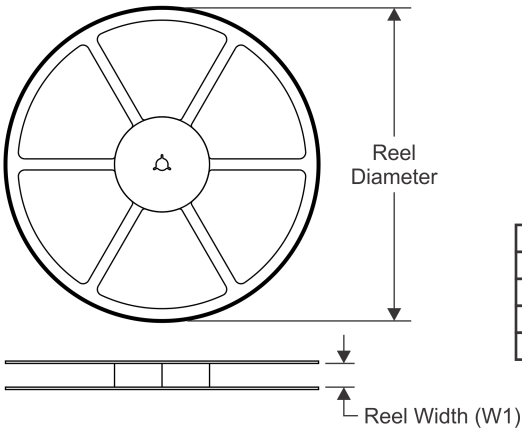
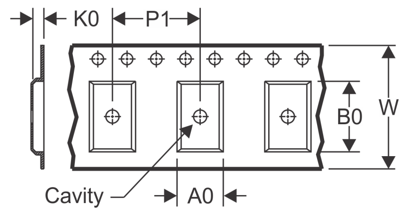
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

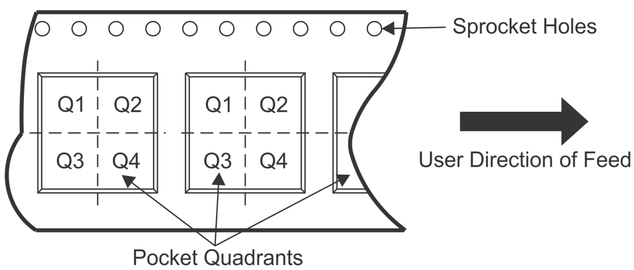


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

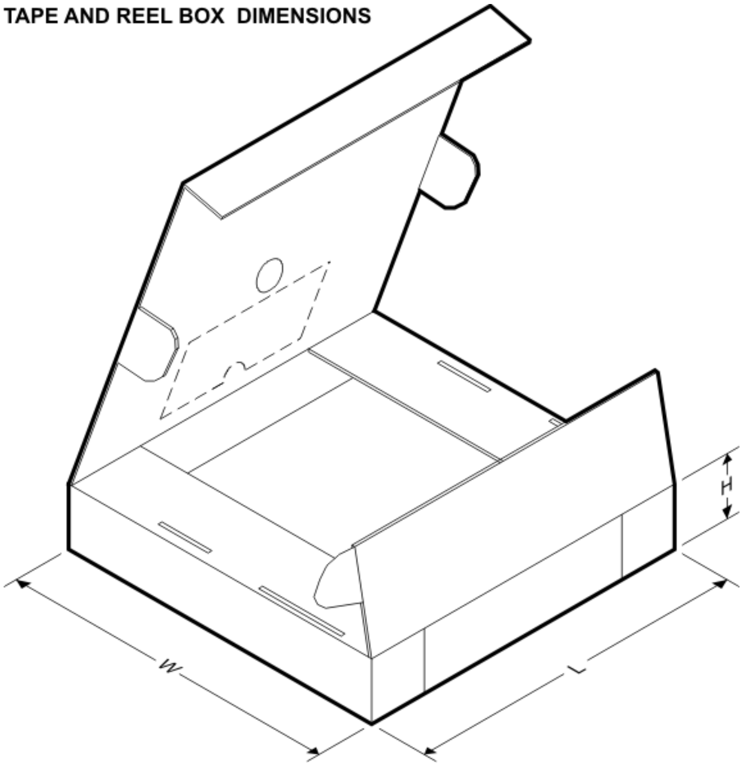
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

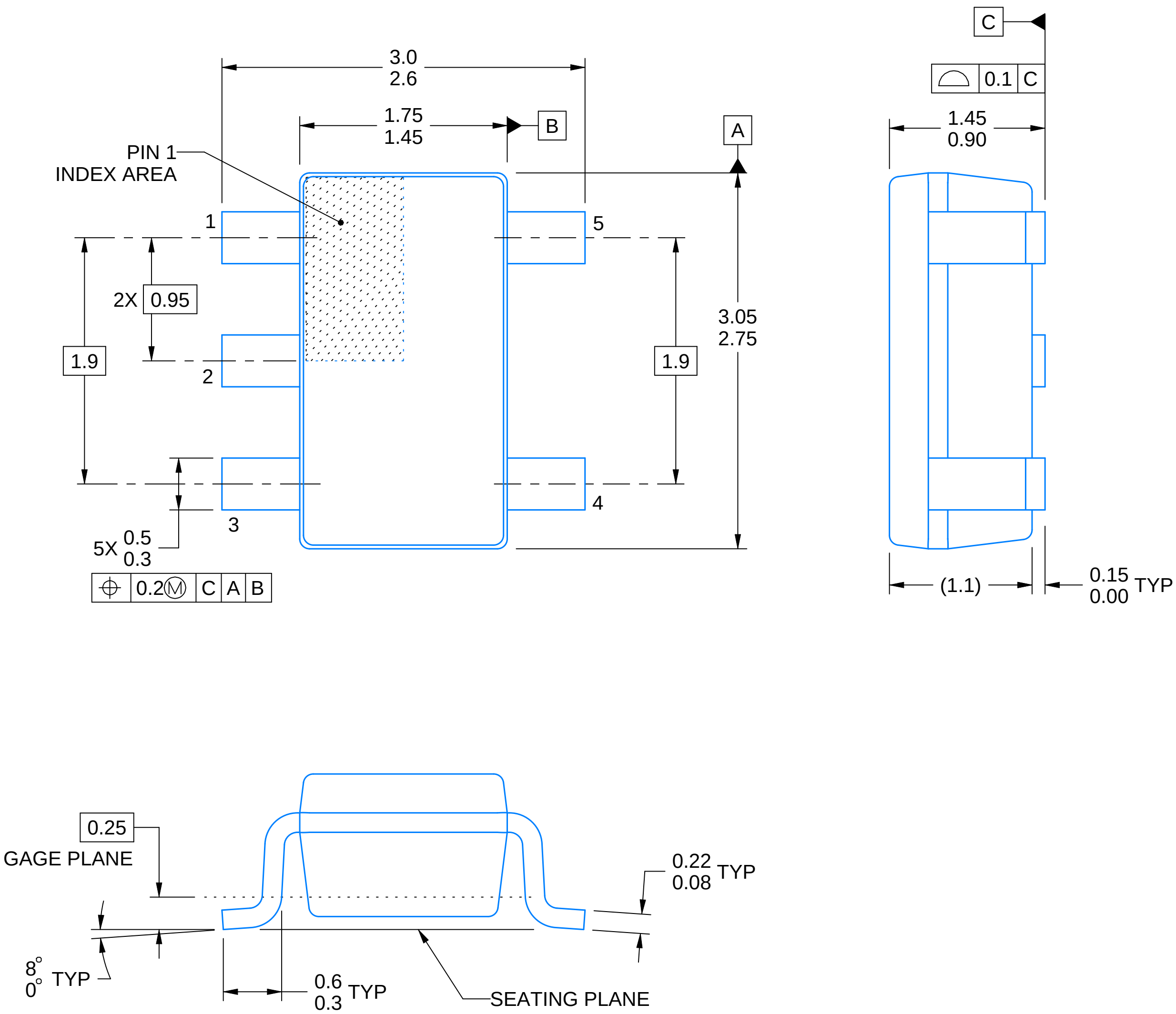
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV4021R1YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV4021R2YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV4021S5MYKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV4021S5YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV4021S5YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV4031R1YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV4031R2YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV4041R1YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV4041R2YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV4041R5DBVR	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV4051R1YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV4051R2YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV4051R5DBVR	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV4021R1YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
TLV4021R2YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
TLV4021S5MYKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
TLV4021S5YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
TLV4021S5YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
TLV4031R1YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
TLV4031R2YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
TLV4041R1YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
TLV4041R2YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
TLV4041R5DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV4051R1YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
TLV4051R2YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
TLV4051R5DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0



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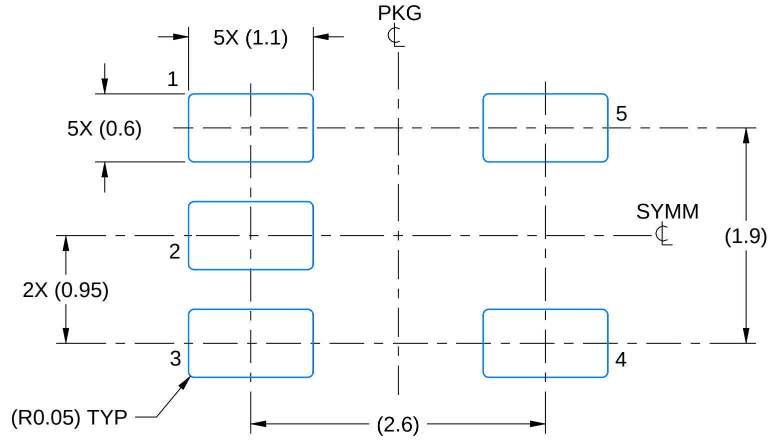
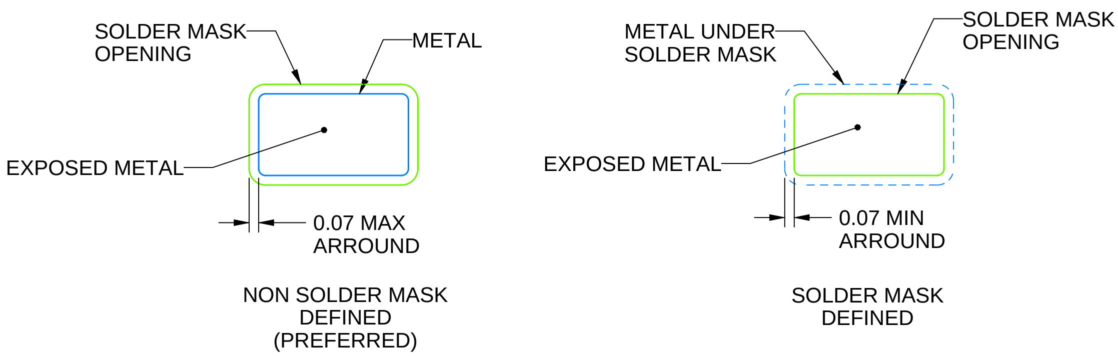
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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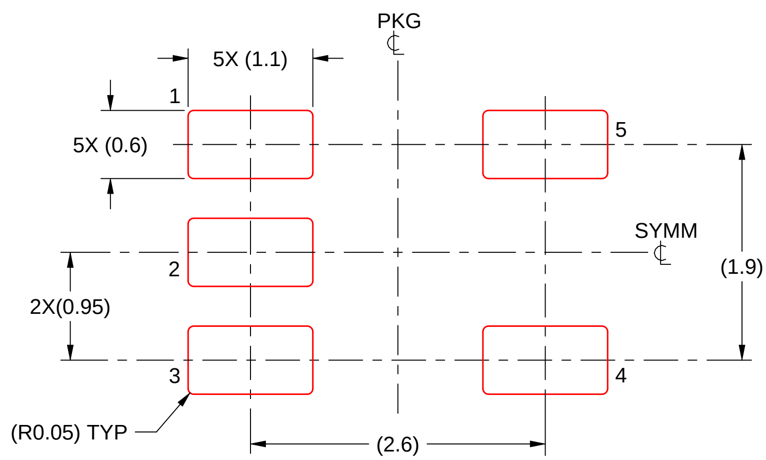
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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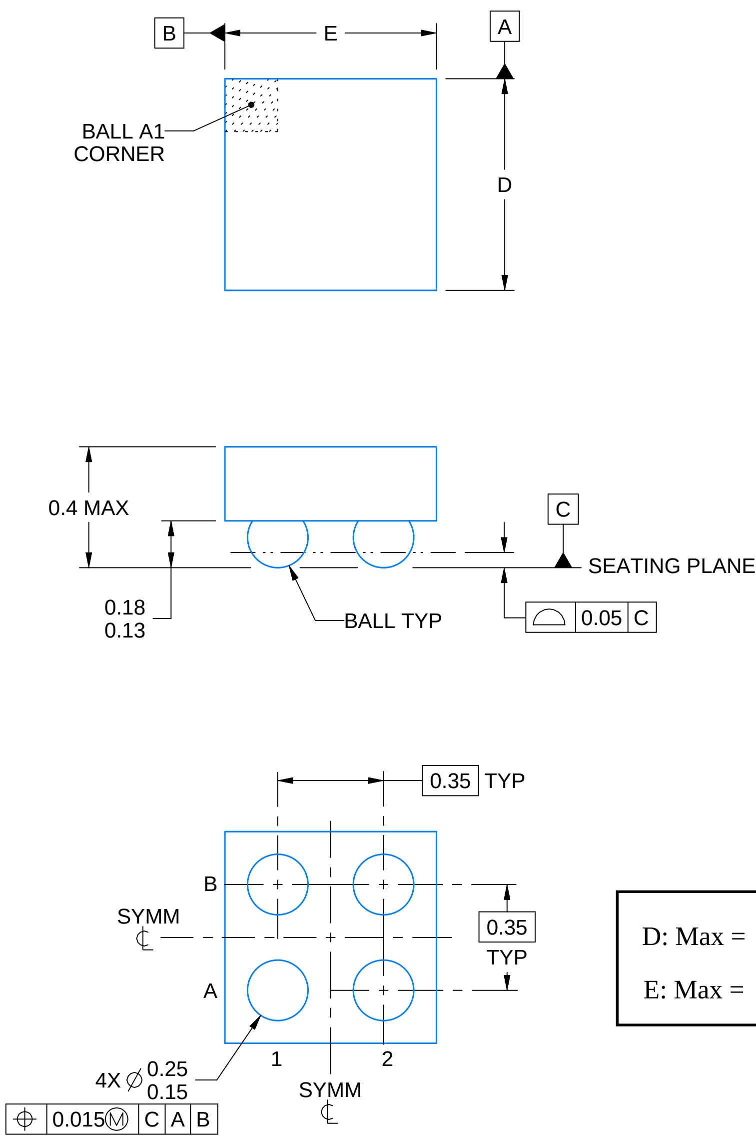
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

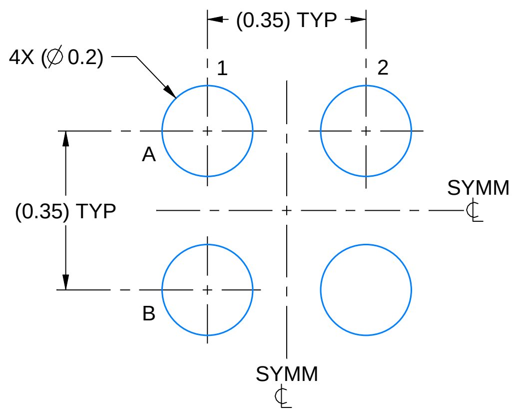


D: Max = 0.76 mm, Min = 0.7 mm	
E: Max = 0.76 mm, Min = 0.7 mm	

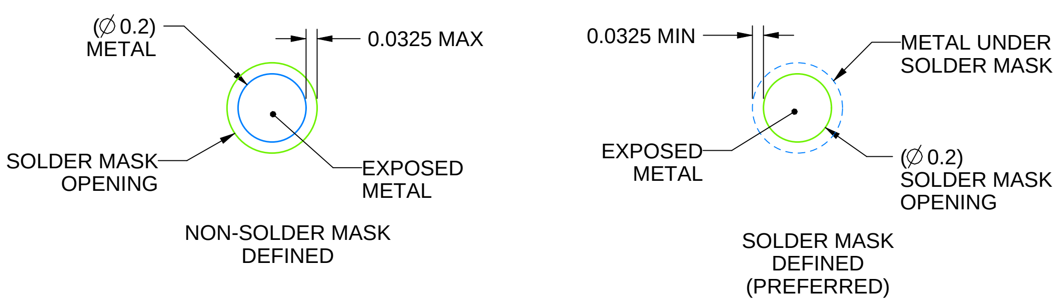
4221909/B 08/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



SOLDER MASK DETAILS
NOT TO SCALE

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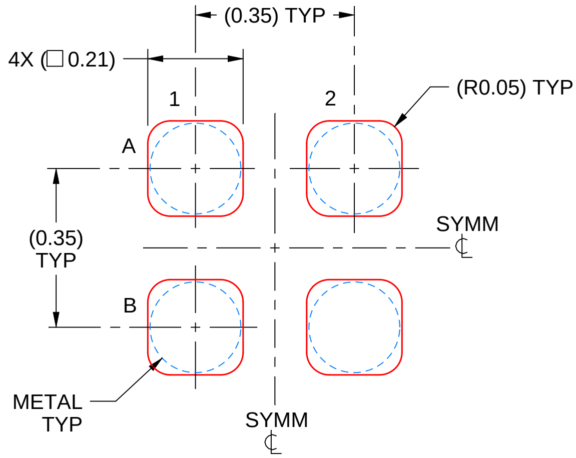
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm - 0.1 mm THICK STENCIL
SCALE:60X

4221909/B 08/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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