LM3401 Hysteretic PFET Controller for High Power LED Drive

Check for Samples: LM3401

FEATURES

- **Hysteretic Control for Speed and Simplicity**
- **Input Operating Range of 4.5V-35V**
- **1.5MHz Maximum Switching Frequency**
- **Low 200mV Reference Voltage**
- **Programmable Current Limit**
- **High speed CMOS Compatible Enable/Dimming**
- **Adjustable Hysteresis**
- **Input UVLO**
- **No output Capacitor Required**
- **8-pin VSSOP Package**

APPLICATIONS

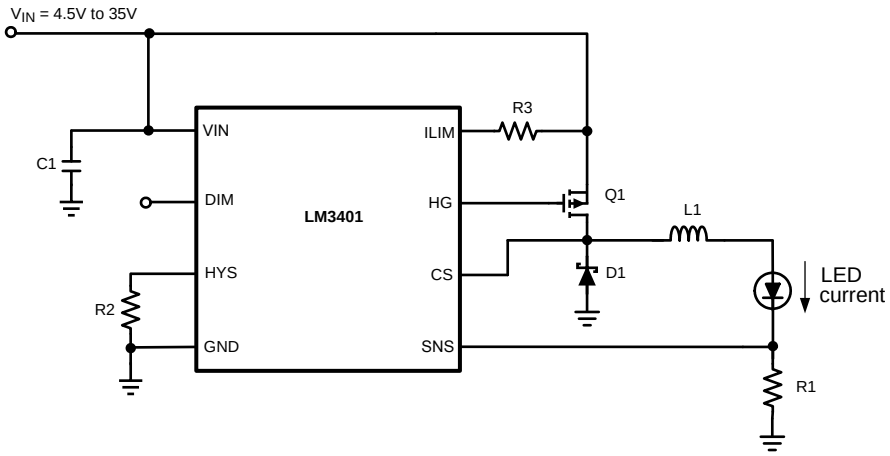
- **LED Driver**
- **Battery Charger**

DESCRIPTION

The LM3401 is a switching controller designed to provide constant current to high power LEDs. The LM3401 drives an external P-MOSFET switch for step-down (Buck) regulators. The LM3401 delivers constant current within ±6% accuracy to a wide variety and number of series connected LEDs. Output current is adjusted with an external current sensing resistor to drive high power LEDs in excess of 1A.

For improved accuracy and efficiency, the LM3401 features dual-side hysteresis, very low reference voltage, and short propagation delay. A cycle by cycle current limit provides protection against over current and short circuit failures. Additional features include adjustable hysteresis and a CMOS compatible input pin for PWM dimming.

TYPICAL APPLICATION CIRCUIT



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

CONNECTION DIAGRAM

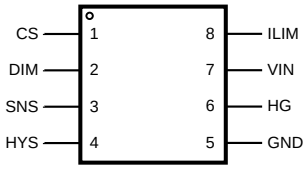


Figure 1. Top View
8-Lead VSSOP
See DGK Package

PIN DESCRIPTIONS

Pin #	Pin Name	Description
1	CS	Current sense pin. Connect to the PFET drain
2	DIM	Dimming input pin. When DIM is low, the HG drive is off. Can be connected to a logic level PWM signal
3	SNS	Current feedback pin – to LED cathode. Connect a resistor from this pin to ground to set the DC LED current
4	HYS	Hysteresis adjust pin. Connect a resistor from this pin to GND to set the hysteresis window
5	GND	Ground pin
6	HG	Gate drive output. Connect to the PFET gate
7	VIN	Power supply input
8	ILIM	Current limit adjust pin. Connect a resistor from this pin to the PFET source to set the current limit threshold

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ABSOLUTE MAXIMUM RATINGS (1)

If Military/Aerospace specified devices are required, contact the Texas Instruments Semiconductor Sales Office/ Distributors for availability and specifications.

	VALUE / UNIT
VIN	-0.3V to 36V
CS	-2.0V to 36V
SNS	-0.3V to 8V
ILIM	-0.3V to 36V
DIM	-0.3V to 36V
HYS	-0.3V to 4V
Storage Temperature	-65°C to +150°C
Lead Temperature	
Vapor Phase (60sec)	215°C
Infrared (15sec)	220°C
ESD Rating Human Body Model (2)	2.5kV

(1) Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. Operating Ratings indicate conditions for which the device is intended to be functional, but **do not** include specific performance limits. For specified specifications, see Electrical Characteristics.
(2) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

RECOMMENDED OPERATING CONDITIONS(1)

	VALUE / UNIT
VIN	4.5V to 35V
Junction Temperature Range	-40°C to +125°C
Thermal Resistance θ_{JA} (2)	151°C/W
Power Dissipation (2)	0.66W

(1) Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. Operating Ratings indicate conditions for which the device is intended to be functional, but **do not** include specific performance limits. For specified specifications, see Electrical Characteristics.
(2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_{J_MAX}, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D_MAX} = (T_{J_MAX} - T_A)/\theta_{JA}$. The maximum power dissipation of 0.66W is determined using T_A = 25°C, θ_{JA} = 151°C/W, and T_{J_MAX} = 125°C. θ_{JA} will vary with board size and copper area. The θ_{JA} spec is based on a JEDEC standard 4-layer board.

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ELECTRICAL CHARACTERISTICS

Specifications in standard type are for T_J = 25°C only, and limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Unless otherwise stated, V_{IN} = 24V. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only (1).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SYSTEM						
V_{REF}	Reference Voltage		**188**	200	**212**	mV
ΔV_{REF} / ΔV_{IN}	Line regulation	5V < VIN < 35V		0.002		mV/V
I_Q	Operating VIN Current (2)			1.05		mA
I_{HYS}	Hysteresis Pin Source Current	HYS pin = 50 mV to 500 mV	**15**	20	**25**	µA
SNS_{HYS_MU}	SNS Comparator Hysteresis Multiplier	HYS pin = 250 mV	**0.168**	0.20	**0.224**	-
T_{DLY}	SNS Comparator to HG Delay	SNS rising		46	**80**	ns
T_{DIM}	DIM to HG Delay	DIM rising		69	**120**	ns
I_{ILIM}	ILIM Pin Sink Current		**4**	5.5	**8**	µA
V_{CL_OFF}	Current Limit Comparator Offset		**-10**	0	**+10**	mV
V_{ZC}	Zero Cross Comparator Threshold	Measured at CS pin	**-70**	-130	**-200**	mV
V_{DIM}	DIM Threshold Voltage		**1.85**	2.0	**2.25**	V
	Hysteresis			286		mV
I_{SNS}	SNS pin Bias Current	V_{SNS} = 200 mV		300	**780**	nA
UVLO	UVLO threshold	Vin rising		4.3	**4.48**	V
	Hysteresis			0.5		V
DRIVER						
Ton_min	Minimum on-time			150		ns
R_{HG}	Gate Drive Resistance	Source Current = 100 mA		5.3		Ω
		Sink Current = 100 mA		10.5		Ω
I_{HG}	Driver Output Current	Source, HG = VIN -2.5V		0.41		A
		Sink, HG = VIN -2.5V		0.33		A
V_{HG}	HG on voltage	Referenced to VIN, steady state voltage	**-4.2**	-4.7	**-5.5**	V

(1) All room temperature limits are 100% production tested. All limits at temperature extremes are specified through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) IQ specifies the current into the VIN pin and applies to non-switching operation.

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TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, V_{IN} = 24V, T_A = 25°C.

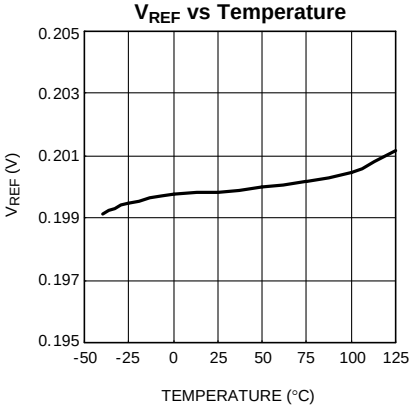


Figure 2.

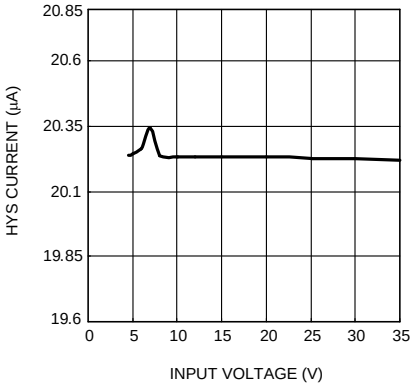


Figure 3.

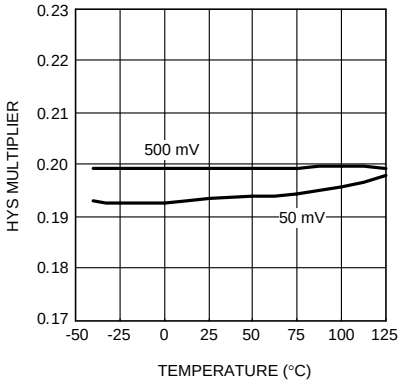


Figure 4.

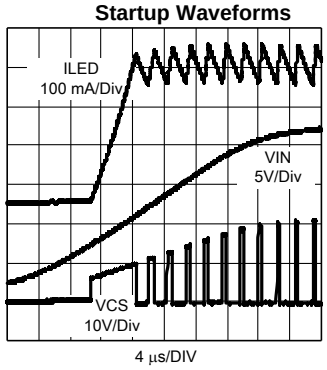


Figure 5.

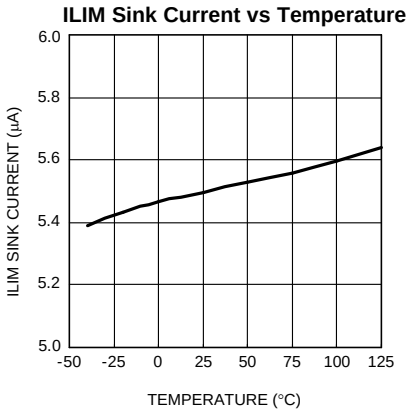


Figure 6.

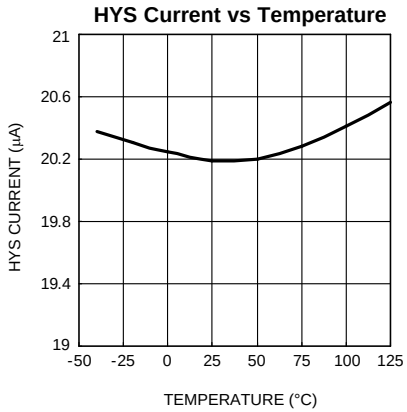


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, V_{IN} = 24V, T_A = 25°C.

UVLO Threshold vs Temperature

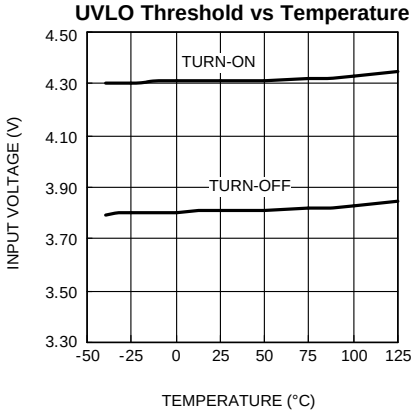


Figure 8.

SNS to HG Propagation Delay vs V_{IN}

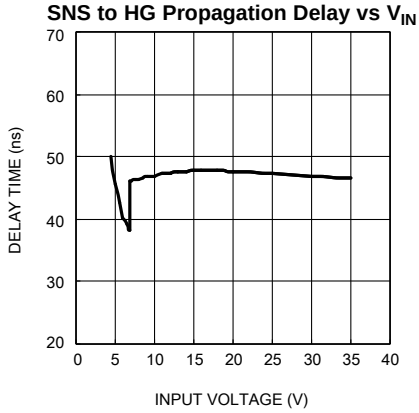


Figure 9.

Line Transient Response

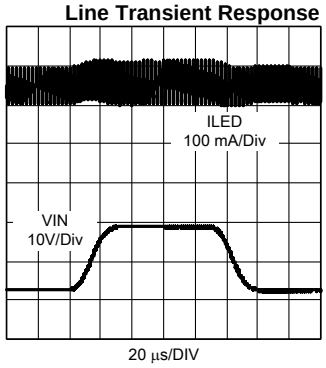


Figure 10.

Initial HG Voltage vs Input Voltage

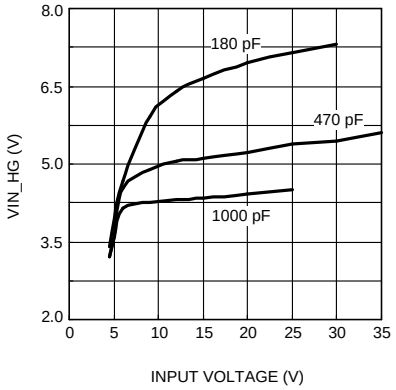


Figure 11.

350 mA Efficiency

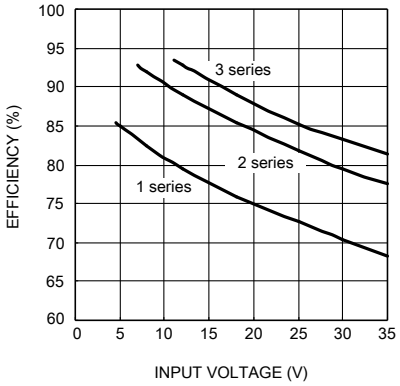


Figure 12.

700 mA and 1A Efficiency

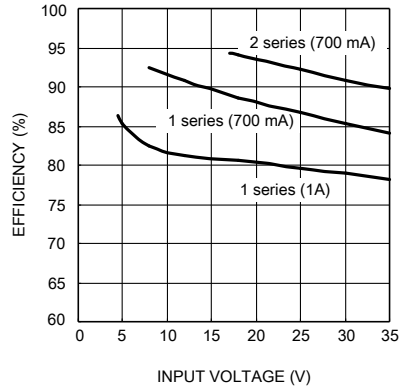


Figure 13.

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BLOCK DIAGRAM

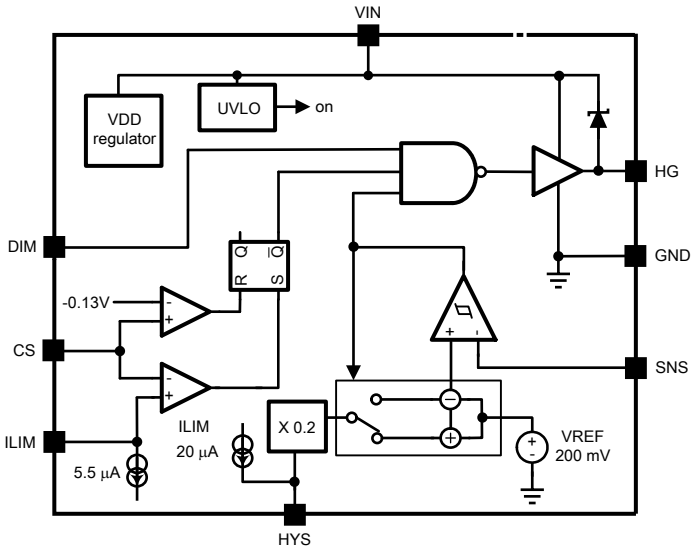


Figure 14. Block Diagram

Operational Description

HYSTERETIC CONTROL

The LM3401 is a step-down DC-DC controller designed to provide a constant current source for driving a high power LED string.

The LM3401 uses comparator-based voltage mode hysteretic control for a simple and stable design. Hysteretic control does not utilize an internal oscillator, but relies on output conditions to directly control switching. The LM3401 controls LED current within the adjustable hysteresis window by monitoring peak and valley voltage at the SNS pin. A dual sided hysteresis window is used to optimize accuracy.

Regulated LED current flows to ground through a sense resistor at the SNS pin. The voltage generated at the SNS pin is compared to the 200 mV internal reference. When the SNS voltage falls below the reference voltage minus hysteresis, the output of the hysteretic comparator goes low. This results in the driver output, HG, pulling the gate of the PFET low and turning on the PFET.

With the PFET on, LED current ramps up through the PFET and the inductor. As the LED current increases, the SNS voltage reaches its upper threshold (reference voltage plus hysteresis). This forces the output of the comparator and HG to go high, which turns the PFET off. When the PFET turns off, current flows through the catch diode, and LED and inductor current ramp down. When the SNS voltage falls to its lower threshold, the cycle repeats. The resulting LED current, SNS, and switch node waveforms are shown in Figure 15.

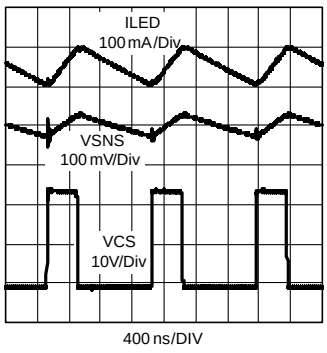


Figure 15. Hysteretic Switching Waveforms

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OUTPUT CURRENT SETTING

The LED average current is programmed using a resistor between SNS and GND, shown as R1 in the typical application schematic. The SNS resistor (R_{SNS}) can be calculated as follows:

$$R_{SNS} = \frac{V_{SNS}}{I_{LED}} \quad (1)$$

Where V_{SNS} is 200 mV typically, and I_{LED} is the DC average LED current.

The sense resistor power rating must be higher than its power dissipation. The required power rating can be calculated (in Watts) as follows:

$$W_{RSNS} = V_{SNS} \times I_{LED} \quad (2)$$

When selecting a sense resistor, thermal de-rating must also be taken into consideration.

While R_{SNS} sets the DC LED current, the AC peak LED current will be higher than the DC setting. This peak current must not be greater than the maximum peak current rating of the LED, I_{LED_max}. Peak LED current can be calculated from the equation below:

$$I_{LED_PK} = I_{LED} + \frac{I_{LED_RIP}}{2} \quad (3)$$

The LED ripple current, I_{LED_RIP}, is described below in the Hysteresis Adjust section.

HYSTERESIS ADJUST

Adjustable hysteresis (via the HYS pin) provides direct control over the LED ripple current. The HYS pin also gives some control over the switching frequency. Although the hysteresis value can be set after the inductor is selected, a preliminary value must be set in order to begin the frequency calculation. The hysteresis window must be set small enough to keep the peak LED current below its maximum rating, I_{LED_max}.

The maximum SNS pin hysteresis can be calculated as shown:

$$SNS_{HYS_MAX} = (I_{LED_max} - I_{LED}) \times R_{SNS} \quad (4)$$

Any SNS_{HYS} value between 10mV and this maximum is acceptable.

The SNS_{HYS} value is set with a single resistor from the HYS pin to GND, shown as R2 in the typical application schematic. The HYS pin voltage, V_{HYS}, is internally multiplied by SNS_{HYS_MU} (0.2 typical) to generate the hysteresis at the SNS pin, SNS_{HYS}. The hysteresis setting resistor can be determined from the following equation:

$$R2 = \frac{SNS_{HYS} \times 5}{20\ \mu A} \quad (5)$$

Where 20 µA is the typical HYS source current, and SNS_{HYS} is the resulting SNS pin hysteresis voltage. The hysteresis voltage can be set within a range of 10 mV to 100 mV (50 mV to 500 mV at the HYS pin). The SNS_{HYS} value defines both the upper and lower threshold of the SNS pin. For example, with a V_{HYS} setting of 100 mV, SNS_{HYS} will be 20 mV. Therefore, the total hysteretic window will be 40 mV, or 20 mV above and 20mV below the 200 mV reference voltage. This directly correlates to peak-to-peak inductor and LED ripple current, approximated by the following equation:

$$I_{LED_RIP} = \frac{SNS_{HYS} \times 2}{R_{SNS}} \quad (6)$$

If LED ripple current is a design priority, the preliminary R2 value can be determined using a target LED ripple current as shown:

$$R2 = \frac{I_{LED_RIP} \times R_{SNS} \times 5}{40\ \mu A} \quad (7)$$

A more precise equation for ripple current is given in the Inductor Selection section. Once an inductor is selected the more precise equation should be used to determine the actual ripple current and LED peak current. Larger hysteresis values will result in lower switching frequency and higher ripple current for a given inductor. Typical examples are shown in Figure 16 below.

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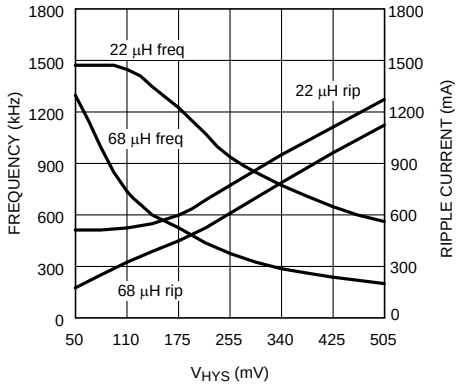


Figure 16. Switching Frequency and Ripple Current vs Hysteresis

SWITCHING FREQUENCY

Although hysteretic control is a simple control method, the switching frequency depends on application conditions and components. If the inductance, input voltage, or LED forward voltage is changed, there will be a change in the switching frequency. Therefore, care must be taken to select components which will provide the desired frequency range. Usually, the best approach is to determine a nominal switching frequency for the application and then select the inductor accordingly. Once the inductor is selected, V_{HYS} can be adjusted to set the frequency range more precisely. This design process usually involves a few iterations to select appropriate standard values that will result in the desired frequency and ripple current.

Switching frequency can be approximately calculated using the formula:

$$f_{SW} = \frac{D}{\frac{2 \times SNS_{HYS} \times L}{R_{SNS} \times (V_{IN} - V_{ANODE})} + (2 \times delay)} \quad (8)$$

Where D is the duty cycle, defined as $(V_{OUT} + V_{DIODE}) / V_{IN}$, V_{ANODE} is 200 mV plus the sum of LED forward voltages, and delay is the sum of the LM3401 propagation delay time and the PFET delay time. The LM3401 propagation delay is 46 ns typically (See the Propagation Delay curve). Alternately, the inductor value can be calculated from a known frequency by re-arranging the same equation:

$$L = \frac{\left[\frac{D}{f_{SW}} - (2 \times delay)\right] \times R_{SNS} \times (V_{IN} - V_{ANODE})}{2 \times SNS_{HYS}} \quad (9)$$

Switching frequency for a typical application is shown in Figure 17 along with the calculated frequency.

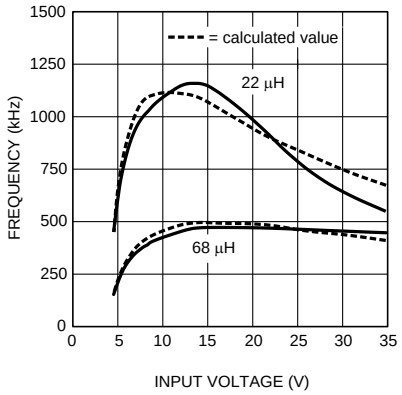


Figure 17. Frequency vs Input Voltage

Maximum switching frequency will typically occur around the input voltage which corresponds to 25% duty cycle.

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If the input voltage falls below the forward voltage of the LED string, the LM3401 will operate at 100% duty cycle. In this state, the anode voltage will be equal to the input voltage and LED current is determined by the v-i curve of the LED. At 100% duty cycle, LED current will be continuous with a maximum value equal to the I_{LED_PK} level set at the HYS pin.

In some applications, maximum operating frequency will be limited by the minimum on-time as shown in the following equation:

$$t_{on} = \frac{D}{f_{SW}} \tag{10}$$

When the on-time reaches minimum (150 ns typical) due to increasing input voltage, the frequency will be reduced in order to maintain the proper duty cycle.

INDUCTOR SELECTION

The most important parameters for the inductor are the inductance and the current rating. The LM3401 operates over a wide frequency range and can use a wide range of inductance values.

Once an inductance value is determined from the frequency equation, the maximum operating current must be verified.

Although peak-to-peak ripple current is controlled by the hysteresis value, there is some variation due to propagation delay. This means that the inductance has a direct effect on LED current line regulation.

In general, a larger inductor will result in lower frequency and better line regulation. The actual peak-to-peak inductor current can be calculated as follows:

$$I_{LED_RIP} = I_{L_RIP} = \frac{2 \times SNS_{HYS}}{R_{SNS}} + \frac{(V_{IN} - V_{ANODE}) \times 2 \times delay}{L} \tag{11}$$

Use the maximum value of Vin to determine the worst case I_{LED_RIP} value. This value should be used to determine the peak current, I_{LED_PK}, shown in the Output Current Setting section.

Since the LM3401 can operate at 100% duty cycle, the inductor must be rated to handle I_{LED_PK} continuously.

RIPPLE REDUCTION CAPACITOR

The typical application schematic shown on the front page is the simplest application of the LM3401. In this schematic, inductor current is equal to LED current. Therefore, the equations for ripple current apply to both LED ripple and inductor ripple.

However, LED ripple current can be reduced without altering the inductor current by using a bypass capacitor placed in parallel with the LED string (shown as C2 in the Figure 24 schematic).

This allows larger hysteresis values to be used while significantly reducing ripple current in the LED string. Figure 18 below shows this effect: inductor ripple current is unaffected while LED ripple current is dramatically reduced.

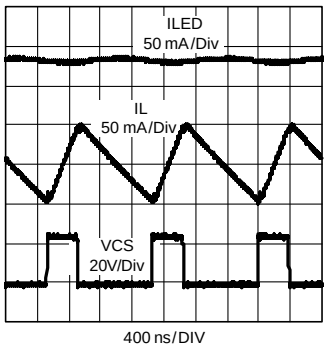


Figure 18. LED Ripple Current Reduction with a 1 µF Ripple Reduction Capacitor

If a ripple reduction capacitor is used, the equation for SNS_{HYS_MAX} only applies for 100% duty operation.

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LED average DC current and peak inductor current are not affected by the ripple reduction capacitor. However, LED peak current is reduced and switching frequency may shift slightly.

Any type of capacitor can be used, provided the working voltage rating is sufficient. In general, higher capacitance and lower ESR will provide more ripple reduction; a typical value greater than 100 nF is recommended. Smaller capacitance values will be less effective, and large ESR values may actually increase LED ripple current.

Despite its effectiveness to smooth LED ripple current, there are two notable disadvantages to using a ripple reduction capacitor.

First, when used, care must be taken to avoid shorting the LED anode to ground. If this occurs, the capacitor will force a large negative voltage spike at the SNS pin which could damage the IC.

Second, this capacitor will limit the maximum PWM dimming frequency because it takes some additional time to charge and discharge. Additionally, ceramic capacitors can generate audible noise due to fast voltage changes during dimming. To reduce audible noise, use the smallest possible case size, use dimming frequencies below 500 Hz, or use a non-ceramic ripple reduction capacitor.

A small bypass capacitor, in the range of 100 pF to 200 pF can also be used to reduce high frequency switching noise. This is recommended in higher current applications, where switching noise can adversely affect the SNS or DIM pins. A small capacitor for noise reduction will have little to no effect on the LED ripple current or dimming but may help solve potential EMI problems.

HG AND PFET SELECTION

When switching, the HG pin swings from V_{IN} (off state) to 4.7V below V_{IN} (typical). As long as the DIM pin is high and the SNS pin is below the upper threshold, HG will stay low, driving the PFET on.

The PFET should be selected based on the maximum Drain-Source voltage (V_{DS}), Drain current rating (Id), maximum Gate-Source voltage (V_{GS}), on-resistance ($R_{DS(on)}$), and Gate capacitance.

The voltage across the PFET in the off state is equal to the sum of the input voltage and the diode forward voltage. The V_{DS} must therefore be selected to provide some margin beyond this voltage.

Since the peak current through the PFET is equal to the peak current through the inductor, Id must be rated higher than the maximum I_{LED_PK}. The LM3401 is capable of 100% duty cycle, therefore, the PFET drain current should be rated to handle I_{LED_PK} continuously. In this case there is no ripple, so $I_{PK} = I_{AVE}$.

Although the typical HG voltage is V_{IN} - 4.7V, this voltage can go much lower during the initial PFET turn-on time. How far HG swings at turn-on depends on several factors including the gate capacitance, on-time, and input voltage. As shown in the Typical Performance Characteristics, the initial HG voltage swing increases with decreasing PFET gate capacitance. Therefore, A PFET must be selected with a maximum V_{GS} rating larger than the initial HG voltage. Conversely, when driving PFETs with larger gate capacitance, the initial HG voltage will be lower. In some cases, a low V_{GS} threshold PFET may be required to ensure complete turn-on. Use the Typical Performance curve as a guideline to selecting a proper PFET.

Note that HG will eventually settle around the typical voltage of V_{IN} - 4.7V regardless of the PFET gate capacitance.

HG has an absolute minimum voltage of 1.2V typically. When the input voltage is below approximately 6V, this minimum limit causes a reduction in drive voltage. At 5V input, for example, HG will swing to 1.2V (or a gate drive voltage of -3.8V). This may not be sufficient to drive some PFETs, and at this reduced HG voltage, $R_{DS(on)}$ is likely to increase and trigger current limit. Therefore, a low V_{GS} threshold PFET is also recommended for lower input voltage applications.

The power loss in the PFET consists of switching losses and conducting losses. Although switching losses are difficult to precisely calculate, the equations below can be used to estimate total power dissipation, which is the sum of PD_{COND} and PD_{SW}.

$$PD_{FET_COND} = R_{DS(on)} \times I_{LED}^2 \times D \quad (12)$$

$$PD_{FET_SW} = \frac{f_{SW} \times I_{LED} \times V_{IN} \times (P_{on} + P_{off})}{2} \quad (13)$$

Where P_{on} = PFET turn-on time, P_{off} = PFET turn-off time, and D is the duty cycle. A value of 10 ns to 50 ns is typical for t_{on} and t_{off}. Longer PFET on and off times will degrade both efficiency and accuracy.

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Increasing $R_{DS(on)}$ will increase power losses and degrade efficiency. FET $_{RDS(on)}$ has a positive temperature coefficient. At 125°C, the $R_{DS(on)}$ may be as much as 150% higher than the value at 25°C. The Gate capacitance of the PFET has a direct impact on both PFET transition time and the power dissipation in the LM3401. Most of the power dissipated in the LM3401 is used to drive the PFET switch. This power can be calculated as follows:

The average amount of gate driver current required during switching (I_G) is:

$$I_G = Q_g \times f_{SW} \quad (14)$$

Where Q_g is the PFET gate charge.

And the total power dissipated in the IC is:

$$PD = (Iq \times V_{IN}) + (I_G \times 4.7V) \quad (15)$$

Where Iq is typically 1.05 mA and 4.7V is the typical HG voltage.

Maximum power dissipation within the LM3401 is limited by ambient temperature. Use the following equation to determine maximum allowable power dissipation, or maximum allowable ambient temperature:

$$PD_{max} = \frac{(125℃ - T_{a_max})}{\theta_{JA}} \quad (16)$$

Where θ_{JA} is the typical thermal resistance of 151°C/W. In general, keeping the gate capacitance below 2000 pF is recommended to keep propagation delay, switching losses, and power losses low. PFETs with very fast rise times may cause excessive ringing at the HG node when combined with the inductance of a long HG trace. To reduce this ringing, a small resistor can be added between HG and the PFET gate. A typical value of 10Ω is usually sufficient.

CURRENT LIMIT OPERATION

The LM3401 current limit monitors inductor current at each switching cycle. Current is sensed across the $R_{DS(on)}$ of the PFET at the CS pin. When the PFET current exceeds the current limit threshold, HG is turned off and the current limit latch is set. In current limit mode, the PFET is held off until the inductor current falls to near zero.

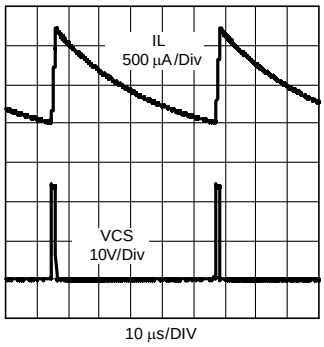


Figure 19. Typical Current Limit Operation

The current limit threshold is adjusted with a setting resistor, shown as R3 in the typical application schematic, connected from I_{LIM} to the V_{IN} node of the PFET.

An internal 5.5 µA (typical) current sink at the ILIM pin creates a voltage across the setting resistor. This voltage is compared to the sensed voltage at the CS pin. Current limit is activated and latched when the voltage at the CS pin drops below the voltage at the ILIM pin.

The current limit setting resistor, R3, can be calculated from the equation below. The minimum current limit occurs at maximum $R_{DS(on)}$ and minimum I_{ILIM} value.

$$R3 = \frac{I_{LIM_PK} \times R_{DS(on)}}{4\ \mu A} \quad (17)$$

Where 4 µA is the minimum I_{ILIM} value and I_{LIM_PK} is the peak inductor current limit threshold. I_{LIM_PK} should be set somewhat higher than the maximum LED current, I_{LED_PK}, to avoid false current limit triggering. The temperature variation of the PFET $R_{DS(on)}$ will result in an equivalent variation in current limit. To ensure that current limit is not falsely triggered, use the highest $R_{DS(on)}$ value over the temperature range to set the R3 value.

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When current limit is activated, the HG driver remains off until the CS voltage rises to -130 mV (typical). This ensures that inductor current is close to 0A when the current limit latch is released. The actual minimum inductor current will depend on the catch diode forward voltage characteristic, which determines the CS pin negative voltage.

Although the LM3401 monitors voltage at the CS pin to reset the current limit, there is also a minimum off time of typically 3 µs. When current limit is triggered, HG will be turned off for at least this amount of time, regardless of the inductor current.

The current limit comparator imposes typically 150 ns of blanking time at the beginning of each switching cycle. This ensures that the PFET is fully on and any switch node ringing has dissipated when the current is sensed. However a slower PFET may not fully turn on within the blanking time. In this case, the current limit threshold must be increased or a faster PFET must be used.

Because the current limit comparator has a limited differential voltage capability, a maximum of 1MΩ is recommended for R3.

PWM DIMMING

The DIM pin is a CMOS compatible input for a PWM (Pulse Width Modulation) dimming signal. PWM dimming adjusts LED brightness by varying the duty cycle, which varies the average LED current. This type of dimming is recommended, because LED peak current remains constant regardless of brightness, which results in more predictable LED color and performance as compared to analog dimming. Figure 20 shows a typical PWM dimming waveform.

When DIM is high (above 2V typically) the LM3401 operates normally and the LED string will be driven at the set current. When pulled low, DIM will disable HG and switching will stop. The PFET will remain off as long as DIM is low. When the LM3401 is powered up or enabled with the DIM pin, the LED current will very rapidly increase to its set point.

There is minimal delay time between a DIM logic change and HG switching. Also, because the LM3401 requires no output capacitor, minimal time is required to ramp-up the LED current. This allows for low duty cycle, high frequency PWM dimming signals to be used.

A dimming frequency greater than 100 Hz is recommended to avoid visible flicker. The LM3401 is capable of PWM dimming frequencies up to 10 kHz with a duty cycle between 1 and 100%. Any DIM signal pulse width longer than 100 ns can be used. In most cases, the maximum dimming frequency is limited by the inductor size and input voltage to anode voltage ratio. Less inductance and higher V_{IN}/V_{ANODE} ratios will allow the inductor and LED current to increase faster, thus allowing for a faster PWM frequency, or lower dimming duty cycle.

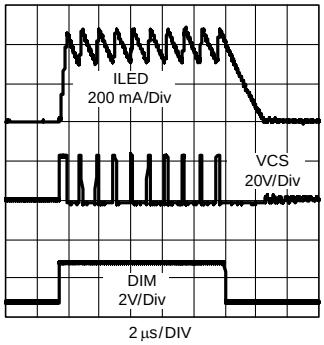


Figure 20. Typical PWM DIM Signal and LED Current L = 22 µH

DIM is a high impedance pin, which is somewhat sensitive to noise. If there is excessive switching noise at the DIM pin, a small bypass filter capacitor can be used. See the Ripple Reduction Capacitor section. V_{IN} can also be used for PWM dimming when a logic signal is not available. In this mode of operation DIM should be connected to V_{IN} through a 10 kΩ resistor. There is typically 10 us of startup delay time when using V_{IN} for dimming. Depending on the application, this delay limits the maximum dimming frequency to typically several hundred Hz.

Higher dimming frequency and lower dimming duty cycle can be achieved by using a FET switch in parallel with the LED string. This is shown in Figure 21 below.

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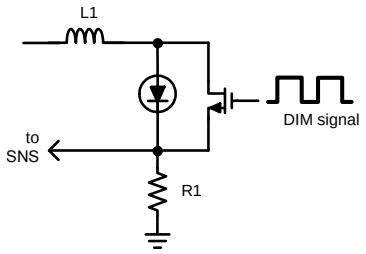


Figure 21. Parallel FET Dimming

When the FET switches on, inductor current flows through the FET and the regulated average inductor current is unchanged. Using this method, inductor current rise time does not limit the dimming frequency. A ripple reduction capacitor should not be used with the parallel FET dimming method since it significantly slows the LED current rise time. However, a small noise filter capacitor can be used.

INPUT CAPACITOR SELECTION

An input bypass capacitor is required between V_{IN} and ground. The input capacitor prevents large voltage transients at the input and provides the instantaneous current when the PFET turns on. The important parameters for the input capacitor are the voltage rating and the RMS current rating. Follow the manufacturer's recommended voltage de-rating. RMS current can be calculated with the equation below. The highest RMS current will occur around 50% duty cycle.

$$I_{rms} = I_{LED} \times \sqrt{\frac{V_{ANODE}}{V_{IN}} \times \left(1 - \frac{V_{ANODE}}{V_{IN}}\right)} \quad (18)$$

A ceramic input capacitor must be placed close to the drain of the PFET. This minimizes the trace inductance between V_{IN} and the PFET, which is a source of switching noise. If the input capacitor is not properly located, switching noise can cause current limit and stability problems.

CATCH DIODE SELECTION

The catch diode provides the current path to the LED string during the PFET off-time and must be rated higher than the average current through the diode, which can be calculated as shown:

$$I_{DIODE} = I_{LED} \times (1\text{-}D) \quad (19)$$

The peak reverse voltage across the catch diode is approximately equal to the input voltage. Therefore, the diode's peak reverse voltage rating should be larger than the maximum input voltage, plus some safety margin.

A Schottky diode is recommended because its low forward voltage maximizes efficiency. For high temperature applications, diode leakage current may become significant and require a higher reverse voltage rating or a low leakage diode to achieve acceptable performance.

LED CURRENT ACCURACY

The total accuracy of average LED current is affected by several factors, both internal and external to the LM3401. Total static accuracy is the part-to-part variation and can be calculated from the equation below:

$$I_{LED_Acc\%} = \sqrt{R_{SNS\%}^2 + V_{SNS\%}^2} \quad (20)$$

Where the worst case $V_{SNS\%}$ is ±6%, and $R_{SNS\%}$ is the sense resistor accuracy. Because these factors are not correlated, the RSS (root-sum-square) method of calculation is used.

The LED current will also show some variation with input voltage. This is primarily due to propagation delay and the dynamic resistance of the LED. In longer on-time operation, the error due to dynamic resistance tends to dominate, while at shorter on-time, the propagation delay will dominate. These two effects counteract each other, resulting in typical regulation curves similar to those shown in Figure 22. A larger inductor will reduce the error due to propagation delay and will result in better overall line regulation.

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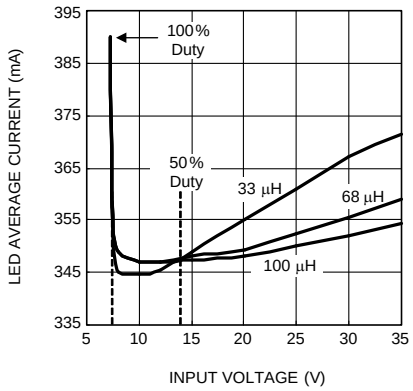


Figure 22. LED DC current line regulation LED Vf = 7.0V

For most applications, the average LED current will be the highest at the maximum input voltage and lowest at a duty cycle somewhat greater than 50%. The maximum LED current variation can be estimated as:

$$I_{LED_reg}\ (A) = \frac{(V_{IN_max} - V_{IN_60\%}) \times delay}{2 \times L} \quad (21)$$

Where $V_{IN_60\%}$ is the input voltage corresponding to a duty cycle of 60%. Since the actual input voltage where minimum LED current occurs varies with the application, this is an approximation. As the duty cycle approaches 100%, the average LED current will approach I_{LED_PK}. The average LED current will be the highest at the point that 100% duty cycle is reached. In the case that 100% duty cycle can occur, maximum LED current variation is calculated as:

$$I_{LED_var_100\%}\ (A) = \frac{SNS_{HYS}}{R_{SNS}} \quad (22)$$

PCB LAYOUT

PCB layout is very important in all switching regulator designs. Poor layout can cause EMI problems, excess switching noise, and improper device operation. The following key points should be followed to ensure a quality layout.

Traces carrying large AC currents should be as wide and short as possible to minimize trace inductance. These areas, shown as darker regions in Figure 23, are:

- V_{IN} between the input capacitor and PFET
- GND between the input capacitor and catch diode
- The switch node

As shown in Figure 23, place the input capacitor ground as close as possible to the anode of the catch diode. The VIN side of the input capacitor should be placed close to the top of the PFET.

The CS node (the node connecting the catch diode cathode, inductor, and PFET source) should be kept as small as possible. This node is one of the main sources for radiated EMI. The SNS and HYS pins are sensitive to noise. Be sure to route the SNS trace away from the inductor and the switch node, which are sources of noise.

The SNS and HYS resistors should be placed close to their respective pins and grounded close to the GND pin. An isolated ground area shown as SGND in Figure 23 is recommended for the SNS, HYS, and GND pin connections. The two ground areas, GND and SGND, should be connected on an inner or bottom layer. This connection is shown as two vias in Figure 23.

A large, continuous ground plane can also be used, as long as the input capacitor and catch diode ground area is somewhat isolated.

The HG trace should be kept as short as possible to minimize inductance and gate ringing (See HG and PFET selection section).

Finally, for accurate current limit sensing, the CS pin and ILIM resistor connections should be made at the PFET pads, via separate traces.

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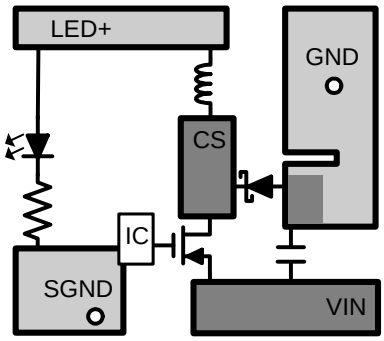


Figure 23. Example PCB Layout

DESIGN EXAMPLE

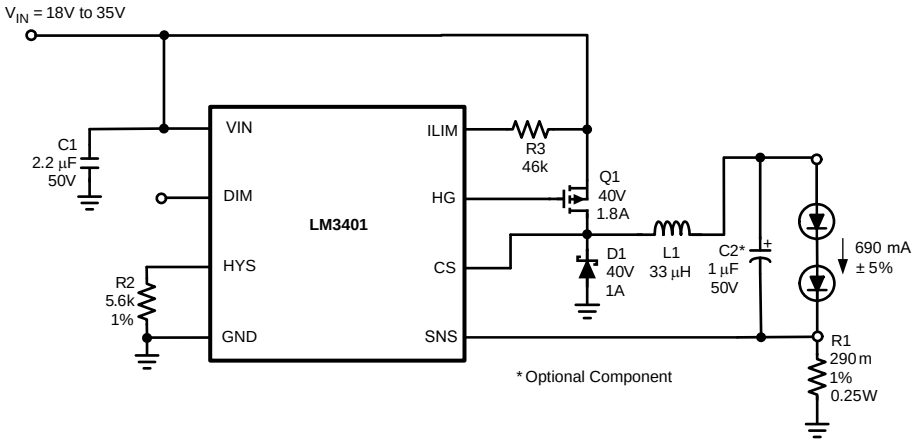


Figure 24. Example Circuit

The following design example is intended to illustrate the step-by-step design process described in the previous sections. The example refers to the circuit in Figure 24, and the results are summaized in Table 1. The resulting circuit will drive a string of 2 Luxeon V Star LEDs at 700 mA from an input voltage between 18V and 35V.

The example LEDs have a maximum DC current rating of 700 mA, a forward voltage of 5.4V to 8.3V, and a maximum peak current rating of 1.0A.

First, set the LED DC current with R1:

$$R1 = \frac{200\ mV}{700\ mA} = 286\ m\Omega \quad (23)$$

And the required wattage is:

$$W_{RSNS} = 700\ mA^2 \times 0.286 = 140\ mW \quad (24)$$

Select a standard value of 290 mΩ, 1/4W resistor, which will result in a 690 mA LED DC current.

To keep the peak LED current below I_{LED_MAX}, the maximum hysteresis is determined by:

$$SNS_{HYS_MAX} = (1.0A - .690A) \times 0.29\Omega = 90\ mV \quad (25)$$

Which gives a maximum R2 value of:

$$R2 = \frac{90\ mV \times 5}{20\ \mu A} = 22.48\ k\Omega \quad (26)$$

Next, a preferred switching frequency of 1 MHz is selected for this example.

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Since this is a relatively high switching frequency, a low starting point of 25 mV is selected for the comparator hysteresis to maintain good line regulation. This will allow a larger inductor at the same operating frequency and is well below the calculated maximum. Set a preliminary hysteresis value with R2:

$$R2 = \frac{25\ mV \times 5}{20\ \mu A} = 6.25\ k\Omega \tag{27}$$

For 1 MHz switching frequency and 25 mV hysteresis, inductance can be calculated. Because frequency varies with input voltage and LED forward voltage, for this calculation, assume typical values of 24V and 13.6V respectively, and a PFET delay time of 15 ns.

$$L = \frac{\left[\frac{0.60}{1\ MHz} - (2 \times 60\ ns)\right] \times [0.29 \times (24V - 13.8V)]}{2 \times 25\ mV} = 29.6\ \mu H \tag{28}$$

Select a value of 33 µH and the hysteresis can be adjusted downward by re-arranging the same frequency equation:

$$SNS_{HYS} = \frac{\left[\frac{0.60}{1\ MHz} - (2 \times 60\ ns)\right] \times [0.29 \times (24V - 13.8V)]}{2 \times 33\ \mu H} = 22.4\ mV \tag{29}$$

This gives a new R2 value of 5.6k. This will result in a typical operating frequency of 1 MHz at $24V_{IN}$. Next, it must be verified that the peak LED current is within the maximum allowed.

For now, the design is created without using a ripple reduction capacitor. Therefore, LED ripple current is equal to inductor ripple current. Maximum LED ripple current is calculated as:

$$I_{LED_RIP} = \frac{2 \times 22.4\ mV}{0.29\Omega} + \frac{(35V - 11V) \times 2 \times 60\ ns}{33\ \mu H} = 227\ mA \tag{30}$$

Note that the maximum input voltage and minimum anode voltage were used for this worst case calculation.

Now peak LED current can be determined:

$$I_{LED_PK} = 690\ mA + \frac{227\ mA}{2} = 804\ mA \tag{31}$$

This confirms that the component selections will keep LED peak current below the maximum LED rating. Notice if a ripple reduction capacitor is chosen, the peak inductor current is still 804mA, but the LED peak current is reduced. Therefore, the inductor must be rated for a DC current greater than 804 mA. Now that the inductor value has been selected and verified, the operating frequency range can be determined. Lowest operating frequency occurs at minimum input voltage and maximum anode voltage. For this example the values are 18V minimum input and 16.8V maximum anode voltage (200 mV SNS voltage plus the maximum LED forward voltages) and calculate:

$$f_{SW} = \frac{0.96}{\frac{2 \times 22.4\ mV \times 33\ \mu H}{0.29\Omega \times (18V - 16.8V)} + (2 \times 60\ ns)} = 219\ kHz \tag{32}$$

At duty cycles close to 100% (96% in this case) the frequency equation becomes less accurate. Actual switching frequency will typically be lower than the calculated value.

To estimate maximum operating frequency, calculate using a V_{IN} which corresponds to a duty cycle of 25%. In this particular example, 25% duty cycle would occur above $35V_{IN}$ ($V_{IN} = (V_{OUT} + V_{DIODE})/0.25 = 69.9V$), therefore maximum frequency will occur at the maximum input voltage corresponding to a duty cycle of 50% ($D = (V_{OUT} + V_{DIODE})/35V = 0.50$):

$$f_{SW} = \frac{0.50}{\frac{2 \times 22.4\ mV \times 33\ \mu H}{0.29\Omega \times (35V - 16.8V)} + (2 \times 60\ ns)} = 1.25\ MHz \tag{33}$$

Using the equation in the Switching Frequency section, it can be verified that this maximum frequency is within the minimum on-time limited frequency (and below the maximum operating frequency).

The maximum frequency calculation is only an estimate, the actual maximum should be verified on the bench.

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The next step is to select a PFET. The critical PFET parameters must meet the minimum circuit requirements of 35V input, 804 mA DC current, and adequate gate drive voltage rating.

Therefore, select a PFET with the following ratings:

- 40V maximum V_{DS}
- –20V maximum V_{GS}
- 1.8A continuous Id
- 130mohm maximum $R_{DS(on)}$

Typically the PFET may be only sourcing 690 mA for about 50% duty cycle. However, at minimum input voltage the duty cycle will increase close to 100%. Therefore, the PFET Id rating should be based on its continuous, not pulsed, current capability.

Now the power dissipation should be verified. Assume the selected PFET has a gate capacitance of 200 pF, which is within recommendation, and a gate charge of 15 nC. Maximum frequency and input voltage are used for a worst case calculation:

I_G = 15 nC x 1.25 MHz = 18.75 mA PD = (1.05 mA x 35V) + (18.75 mA x 4.7V) = 0.125W T_{a_max} = 125°C - (151°C/W x 0.125W) = 106°C (34)

With the selected components, the maximum ambient temperature is above 100°C, sufficient for most applications. Note that this limit applies to the IC only and depends on the pcb type and size. Lower ambient temperature limits may apply to the PFET and other components.

Now the current limit threshold is set with R3 at 0.95A, which is 120% of the maximum peak current. The worst case $R_{DS(on)}$ value at 125°C is used, which is 150% of nominal, and the worst case ILIM pin sink current.

$$R3 = \frac{0.95A \times 195\ m\Omega}{4\ \mu A} = 46.3\ k\Omega \quad (35)$$

The typical current limit threshold will be higher than 1A and can be determined by using typical values for $R_{DS(on)}$ and I_{LIM} sink current. The PFET, inductor, and catch diode must be able to handle this current for short periods of time.

The next component is the input capacitor, C1. A low ESR ceramic capacitor must be used and properly located on the PCB. For this design, the capacitor working voltage must be rated to at least 40V, and 50V is recommended. A 2.2 µF input capacitor should be sufficient, assuming a good PCB layout. The worst case input RMS current is calculated below 50% at duty cycle:

$$I_{rms} = 690\ mA \times \sqrt{\frac{13.8V}{27.6V} \times \left(1 - \frac{13.8V}{27.6V}\right)} = 345\ mA \quad (36)$$

It must be verified that the selected input capacitor can tolerate this current. An additional bulk capacitor placed at the input voltage connection is also recommended.

Next, select D1, the catch diode. A Schottky diode should be used. The reverse voltage rating must be greater than 35V and the average forward current rating must be greater than:

I_{DIODE} = 690 mA x (1 - 0.31) = 480 mA (37)

This calculation assumes the minimum duty cycle, which is maximum input voltage and minimum anode voltage. The diode must also be able to handle peak currents as high as the current limit threshold for short periods. We select a 1A diode to ensure adequate capability over temperature.

If desired, a ripple reduction capacitor can be added at C2 to reduce the LED ripple current. A minimum starting value of 100 nF is recommended for C2, and a value of 1 µF will work well in most applications. In case of an open LED failure, the ripple reduction capacitor must be rated to the maximum input voltage of 35V. If C2 is used, LED ripple current is reduced and the calculated maximum R2 value no longer applies as a limit.

Finally, check the accuracy. The static accuracy is calculated below using a 1% sense resistor.

$$I_{LED_Acc\%} = \sqrt{0.01^2 + 0.06^2} = 6.1\% \quad (38)$$

To estimate line regulation, maximum input voltage and 60% duty cycle input voltage is used. For this example 60% duty cycle occurs at (13.6V + 0.2V)/0.60 or 23V input.

$$I_{LED_reg} = \frac{(35V - 23V) \times 60\ ns}{2 \times 33\ \mu H} = 11\ mA \quad (39)$$

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This is the estimated amount of LED current variation over the input voltage range. If the minimum input voltage was below 17V, the LED current variation would be calculated using the 100% duty cycle equation.

Table 1. Design Example Summary

Parameter	Value	Result	Comment
R1	290 mΩ	690 mA DC	1%
R2	5.6 kΩ	±22.4 mV hysteresis	V_{HYS} = 112 mV(adjustable)
L1	33 µH, >804 mA		
f_{sw}	-	1MHz typical	219 kHz min
I_{ripple}	-	227 mA p-p	worst case
I_{LED_PK}	-	804 mA	worst case
PFET	40V, 1.8A, 130 mΩ		
R3	46 kΩ	0.95A minimum peak current limit	adjustable
C1	2.2 µF, 50V ceramic	>345 mA rms	
D1	40V, 1A		Schottky
Accuracy	±6.1%	±42 mA max variation	part-to-part
Regulation	1.6%	11 mA variation	vs VIN
Ta_max	108°C		worst case
C2	1.0 µF, 50V	LED ripple reduction	optional

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REVISION HISTORY

Changes from Revision B (May 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	19

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3401MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	SNHB	Samples
LM3401MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	SNHB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

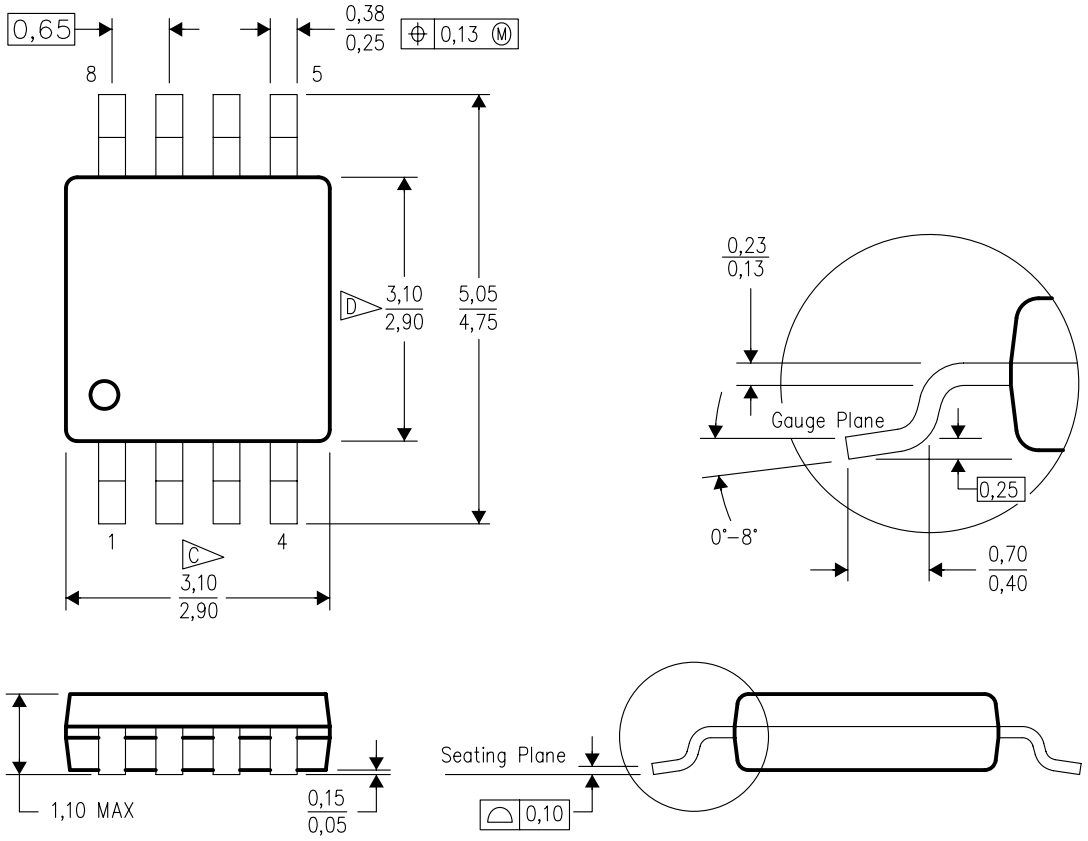
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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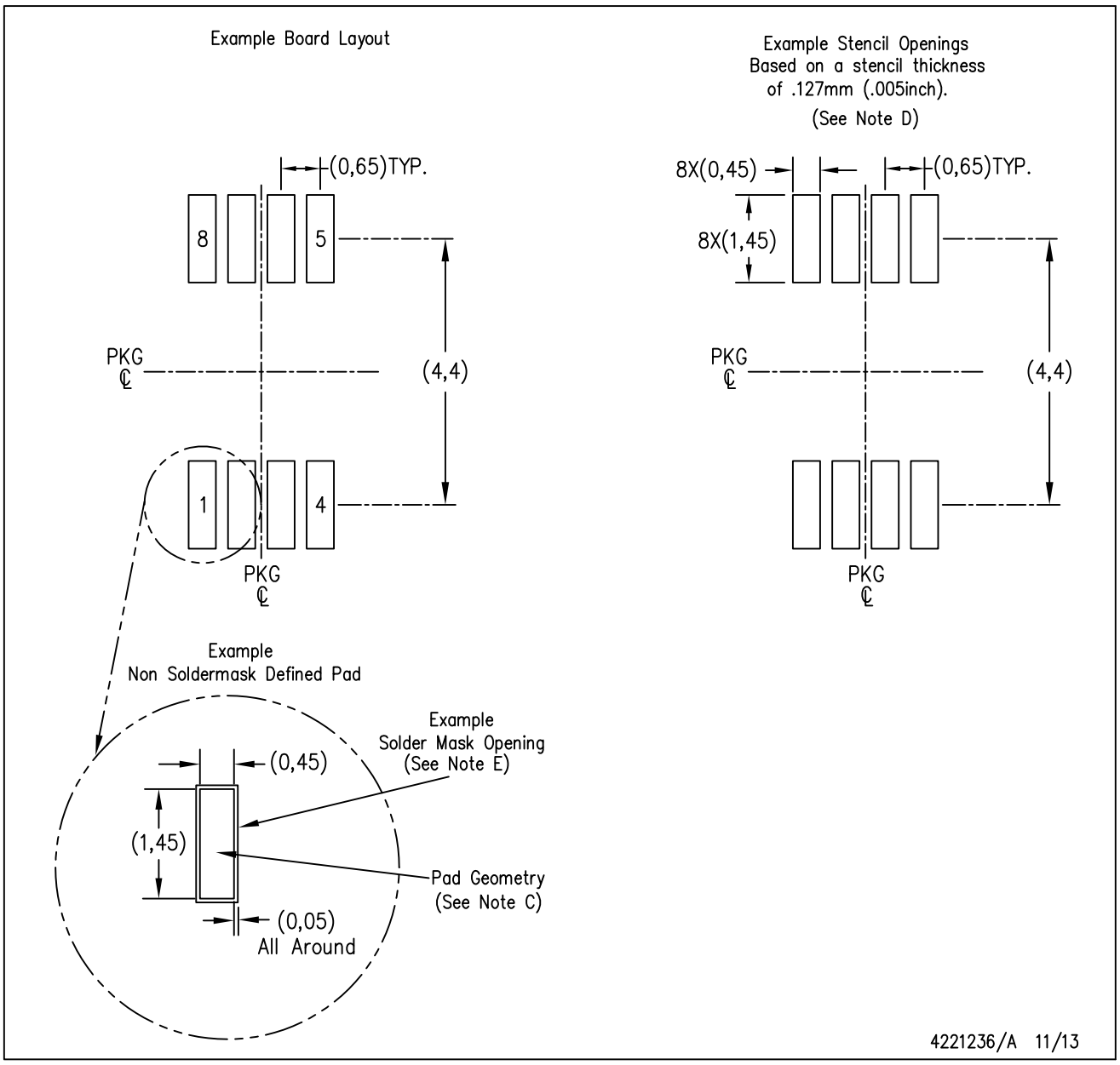
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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