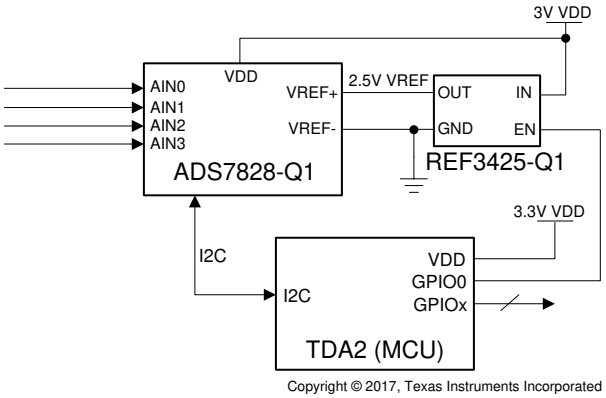
REF34-Q1 低温漂、低功耗、小型串联电压基准

1 特性

- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：–40°C 至 +125°C 的工作环境温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C6
- 初始精度：±0.05%（最大值）
- 温度系数：6ppm/°C（最大值）
- 工作温度范围：−40°C 至 +125°C
- 输出电压选项：2.5V、3.0V、3.3V、4.096V、5.0V
- 输出电流：±10mA
- 低静态电流：95 µA（最大值）
- 关断模式电流低至：3 µA（最大值）
- 宽输入电压：12V
- 输出 1/f 噪声（0.1Hz 至 10Hz）：3.8μV_{PP}/V
- 出色的长期稳定性（25ppm/1000 小时）
- 采用 6 引脚和 5 引脚 SOT-23 封装

2 应用

- 车身控制模块
- 车载充电器
- 牵引逆变器
- 电池管理系统
- 高级驾驶辅助系统



简化版原理图

3 说明

REF34-Q1 器件是一系列低温漂 (6ppm/°C)、低功耗、高精度 CMOS 电压基准。该器件具有 ±0.05% 初始精度、低运行电流以及小于 95 µA 的功耗。该器件还提供 3.8μV_{PP}/V 的极低输出噪声，这使得器件在用于高分辨率数据转换器和噪声关键型系统时能够保持较高的信号完整性。

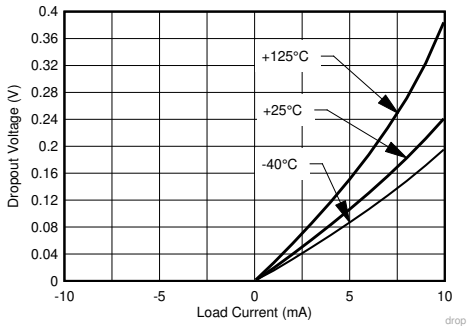
这些器件的低输出电压迟滞和低长期输出电压漂移进一步提高了稳定性和系统可靠性。此外，此器件的小尺寸和低运行电流 (95 µA) 使其非常适合电池供电类应用。REF34-Q1 具有一个可将器件设置为关断模式的使能引脚，在该模式下，器件消耗较低的待机电流 (3 µA)，以帮助降低待机期间的总体系统功耗。

REF34-Q1 系列具有 −40°C 至 +125°C 的较宽额定温度范围。有关其他电压选项，请联系 TI 销售代表。

器件信息 (1)

器件型号	封装	封装尺寸（标称值）
REF34xx-Q1	SOT-23 (6)	2.90mm × 1.60mm
REF34xxS-Q1	SOT-23 (5)	2.90mm × 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



不同温度条件下压降与电流负载间的关系

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (September 2018) to Revision B (August 2020)	Page
• Added information for REF34xxS-Q1	3
• Added information for REF34xxS-Q1	3

Changes from Revision * (July 2018) to Revision A (September 2018)	Page
• 将“预告信息”更改为“量产数据”	1

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5 Device Comparison Table

PRODUCT(1)		V_{OUT}
REF3425-Q1	REF3425S-Q1	2.5 V
REF3430-Q1	REF3430S-Q1	3.0 V
REF3433-Q1	REF3433S-Q1	3.3 V
REF3440-Q1	REF3440S-Q1	4.096 V
REF3450-Q1	REF3450S-Q1	5.0 V

(1) For full orderable part number please refer to 节 14.

6 Pin Configuration and Functions

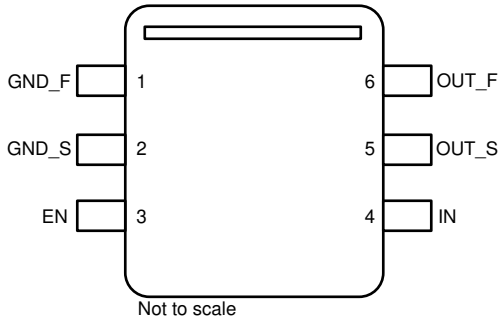


图 6-1. DBV Package 6-Pin SOT-23 (Top View)

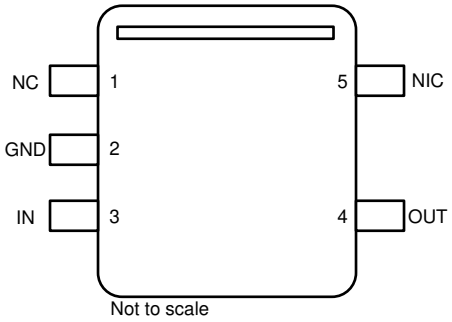


图 6-2. DBV Package 5-Pin SOT-23 (Top View)

Pin Functions

PIN			TYPE	DESCRIPTION
NAME	REF34xx-Q1	REF34xxS-Q1		
GND_F	1	-	Ground	Ground force connection
GND_S	2	-	Ground	Ground sense connection
GND	-	2	Ground	Ground connection
ENABLE	3	-	Input	Enable connection. Enables or disables the device.
IN	4	3	Power	Input supply voltage connection
OUT_S	5	-	Output	Reference voltage output sense connection
OUT_F	6	-	Output	Reference voltage output force connection
OUT	-	4	Output	Reference voltage output connection
NC	-	1	-	Test pin, connect from 0V to 18V
NIC	-	5	-	No internal connection

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	IN	V_{REF} + 0.05	13	V
	EN	– 0.3	IN + 0.3	
Output voltage	V_{REF}	– 0.3	5.5	V
Output short circuit current			20	mA
Temperature	Operating, T_A	– 55	150	°C
	Storage T_{stg}	– 65	170	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2500	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IN	Supply input voltage (I_L = 0 mA, T_A = 25°C)	V_{REF} + V_{DO} (1)		12	V
EN	Enable voltage	0		IN	V
I_L	Output current	– 10		10	mA
T_A	Operating temperature	– 40	25	125	°C

(1) Dropout voltage

7.4 Thermal Information

THERMAL METRIC(1)		REF34-Q1 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	122.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

At T_A = 25°C unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT								
	Output voltage accuracy	T_A = 25°C			–0.05%		0.05%	
	Output voltage temperature coefficient(1)	–40°C ≤ T_A ≤ 125°C				2.5	6	ppm/°C
LINE AND LOAD REGULATION								
$\Delta V_{(O\Delta VIN)}$	Line regulation	V_{IN} = 2.55 V to 12 V , T_A = 25°C				2		ppm/V
		V_{IN} = V_{REF} + V_{DO} (5) to 12 V, −40°C ≤ T_A ≤ 125°C					15	
$\Delta V_{(O\Delta IL)}$	Load regulation	I_L = 0 mA to 10 mA, V_{IN} = 3 V, T_A = 25°C	Sourcing			20		ppm/mA
		I_L = 0 mA to 10 mA, V_{IN} = 3 V, −40°C ≤ T_A ≤ 125°C	Sourcing				30	
		I_L = 0 mA to –10 mA, V_{IN} = V_{REF}+ V_{DO} (6), T_A = 25°C	Sinking	REF3425-Q1		40		
				REF3430-Q1		43		
				REF3433-Q1		48		
				REF3440-Q1		60		
				REF3450-Q1		70		
		I_L = 0 mA to –10 mA, V_{IN} = V_{REF}+ V_{DO} (6), −40°C ≤ T_A ≤ 125°C	Sinking	REF3425-Q1			70	
				REF3430-Q1			75	
				REF3433-Q1			84	
				REF3440-Q1			98	
				REF3450-Q1			140	
I_{SC}	Short-circuit current (Output shorted to ground)	V_{REF} = 0, T_A = 25°C				18	22	mA
NOISE								
e_n p-p	Output voltage noise(2)	f = 0.1 Hz to 10 Hz				5		µV p-p/V
		f = 0.1 Hz to 10 Hz (REF3440-Q1 and REF3450-Q1)				3.8		µV p-p/V
		f = 10 Hz to 10 kHz				24		µV rms
e_n	Output voltage noise density	f = 1 kHz				0.25		ppm/√Hz
		f = 1 kHz (REF3440-Q1 and REF3450-Q1)				0.2		ppm/√Hz
HYSTERESIS AND LONG TERM STABILITY								
	Long-term stability(3)	0 - 1000 hours at 35°C				25		ppm
		1000 - 2000 hours at 35°C				10		
	Output voltage hysteresis(4)	T_A = 25°C to −40°C to 125°C to 25°C, Cycle 1				30		ppm
		T_A = 25°C to −40°C to 125°C to 25°C, Cycle 2				10		

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At T_A = 25°C unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TURNON							
t_{ON}	Turn on time	0.1% of output voltage settling, C_L = 10 µF			2.5		ms
CAPACITIVE LOAD							
C_L	Stable output capacitor value	−40°C ≤ T_A ≤ 125°C		0.1		10	µF
OUTPUT VOLTAGE							
V_{REF}	Output voltage	REF3425Q1			2.5		V
		REF3430Q1			3		V
		REF3433Q1			3.3		V
		REF3440Q1			4.096		V
		REF3450Q1			5.0		V
POWER SUPPLY							
V_{IN}	Input voltage			V_{REF} + V_{DO}		12	V
I_L	Output current capacity	V_{IN} = V_{REF} + V_{DO} (6) to 12 V	Sourcing	10			mA
		V_{IN} = V_{REF} + V_{DO} (6) to 12 V	Sinking	– 10			
I_Q	Quiescent current	−40°C ≤ T_A ≤ 125°C	Active mode		72	95	µA
		−40°C ≤ T_A ≤ 125°C	Shutdown mode		2.5	3	
V_{DO}	Dropout voltage	I_L = 0 mA, T_A = 25°C			50		mV
		I_L = 0 mA, −40°C ≤ T_A ≤ +125°C				100	
		I_L = 10 mA, −40°C ≤ T_A ≤ +125°C				500	
V_{EN}	ENABLE pin voltage	Voltage reference in active mode (EN = 1)		1.6			V
		Voltage reference in shutdown mode (EN = 0)				0.5	
I_{EN}	ENABLE pin leakage current	V_{EN} = V_{IN}=12 V, −40°C ≤ T_A ≤ 125°C			1	2	µA

(1) Temperature drift is specified according to the box method. See 节 9.3 for more details.
(2) The peak-to-peak noise measurement procedure is explained in more detail in 节 8.5.
(3) Long-term stability measurement procedure is explained in more in detail in 节 8.2.
(4) The thermal hysteresis measurement procedure is explained in more detail in 节 8.3.
(5) The dropout voltage in line regulation test condition is 50 mV.
(6) The dropout voltage in test condition is 500 mV.

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7.6 Typical Characteristics

at T_A = 25°C, V_{IN} = V_{EN} = 12 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

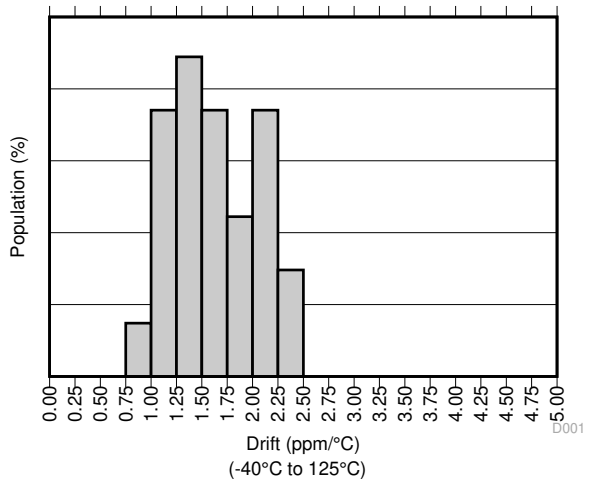


图 7-1. Temperature Drift

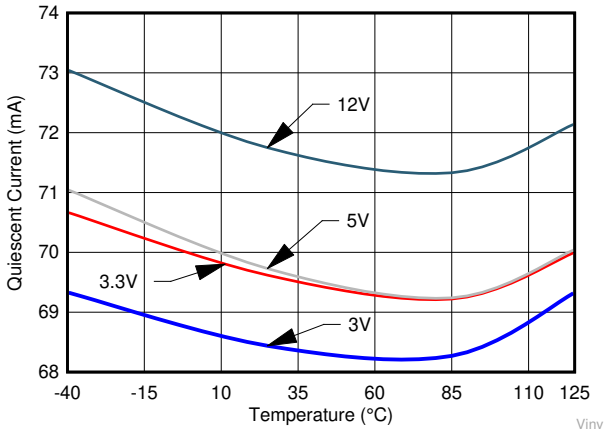


图 7-2. V_{IN} vs I_Q Over Temperature

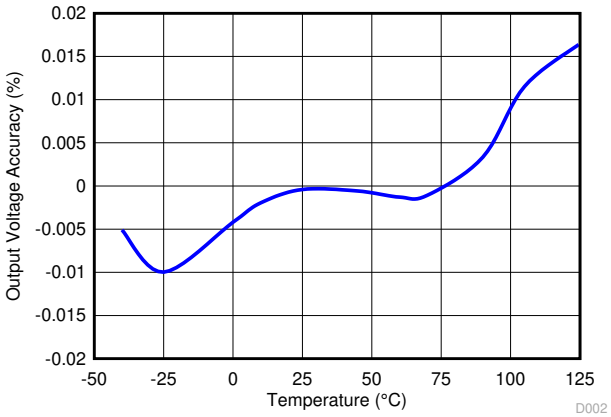


图 7-3. Output Voltage Accuracy vs Temperature

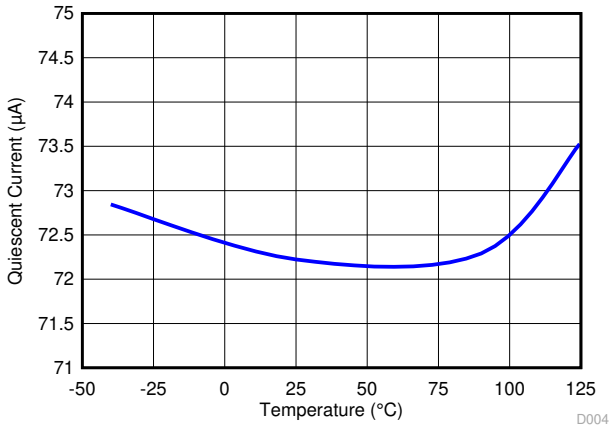


图 7-4. Quiescent Current vs Temperature

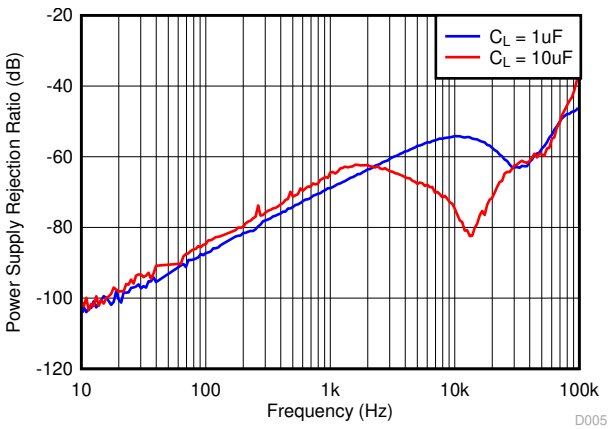


图 7-5. Power-Supply Rejection Ratio vs Frequency

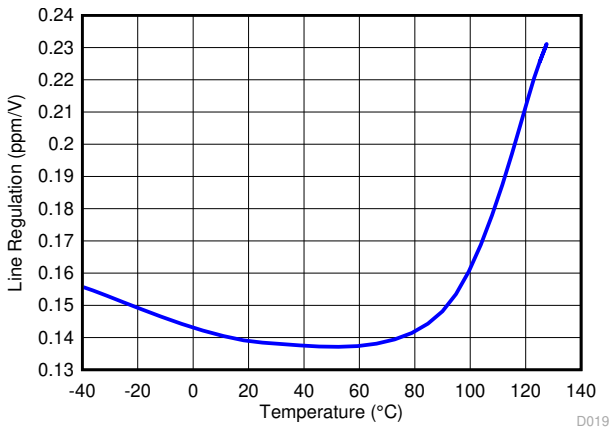


图 7-6. Line Regulation

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7.6 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = 12 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

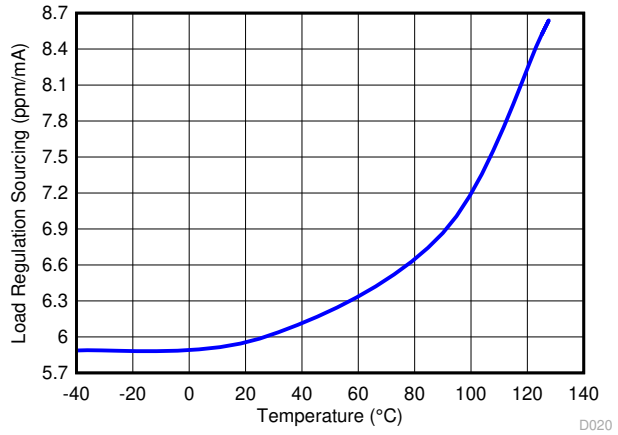


图 7-7. Load Regulation Sourcing

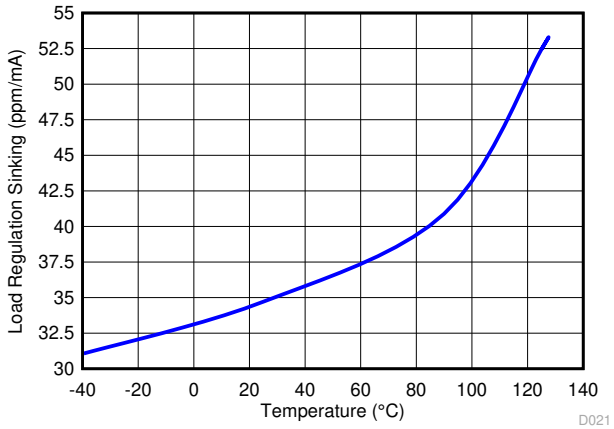


图 7-8. Load Regulation Sinking

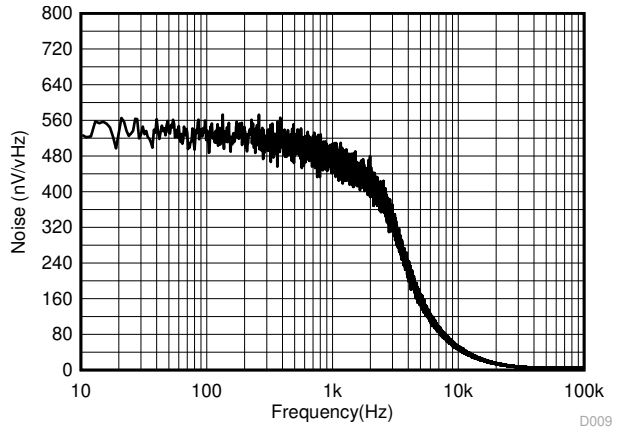


图 7-9. Noise Performance 10 Hz to 10 kHz

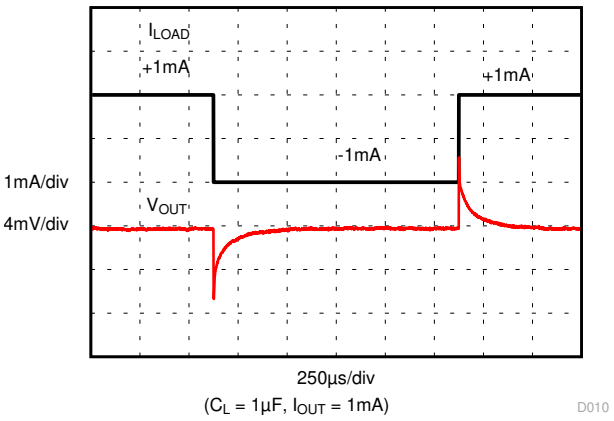


图 7-10. Load Transient

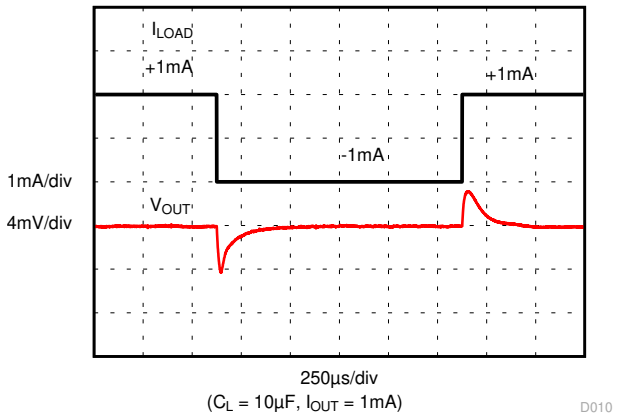


图 7-11. Load Transient

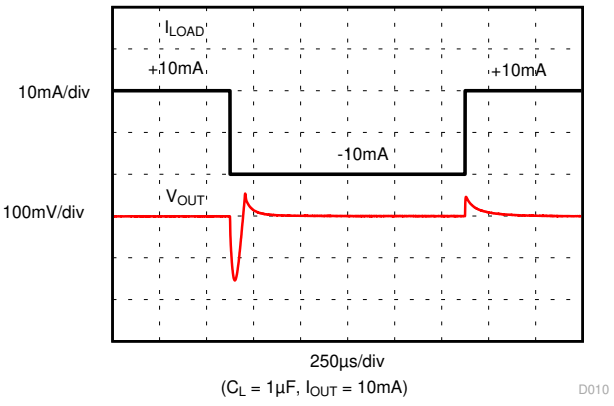


图 7-12. Load Transient

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7.6 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = 12 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

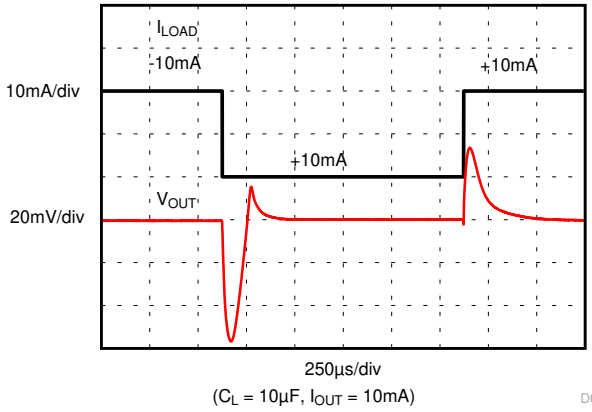


图 7-13. Load Transient

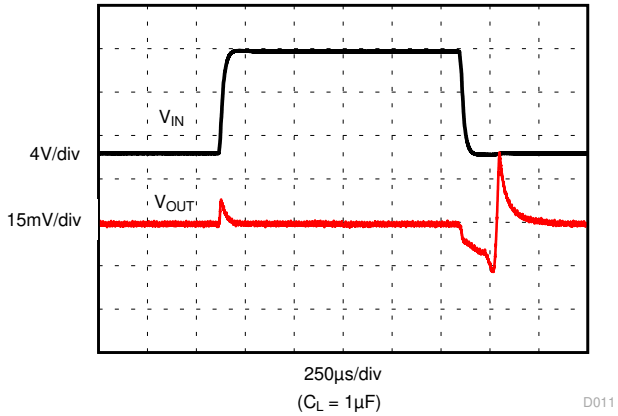


图 7-14. Line Transient

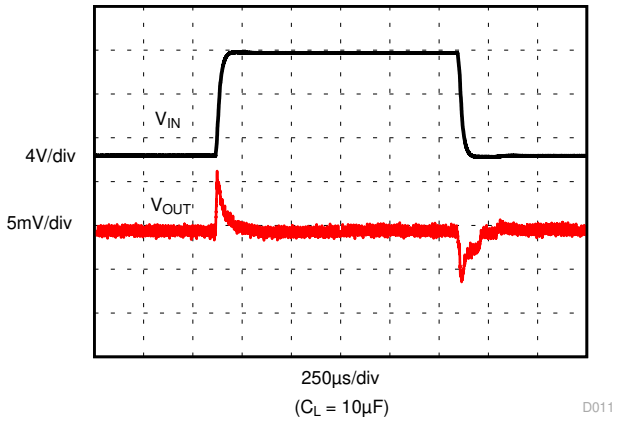


图 7-15. Line Transient

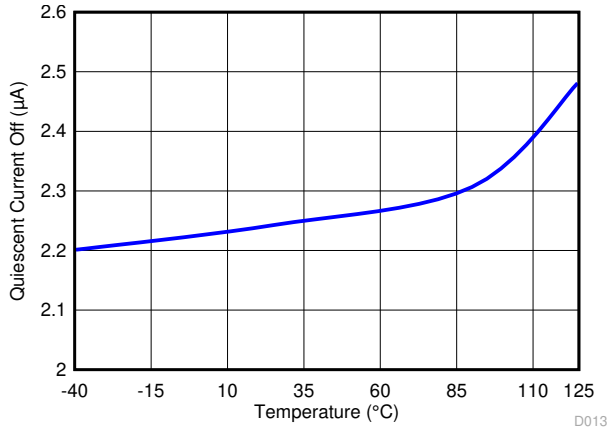


图 7-16. Quiescent Current Shutdown Mode

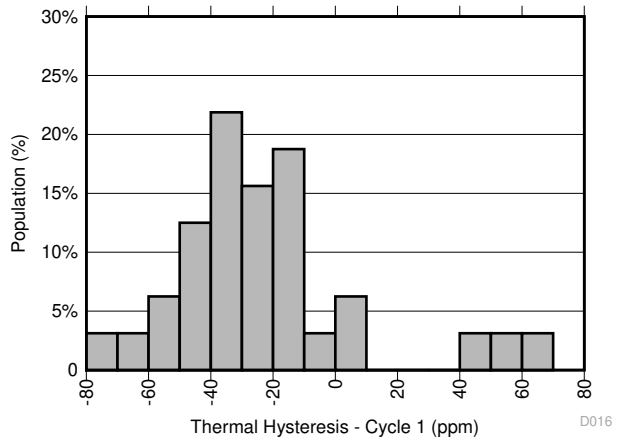


图 7-17. Thermal Hysteresis Distribution (Cycle 1)

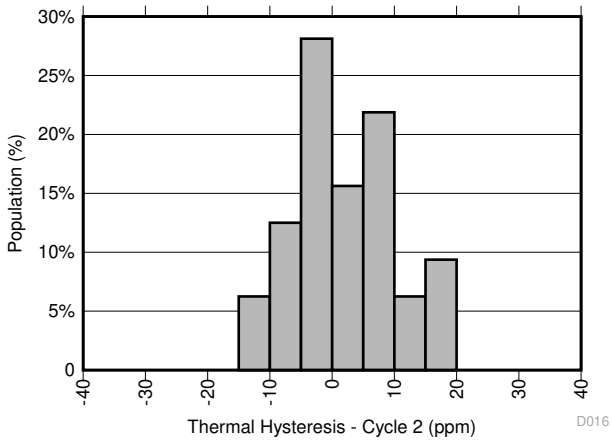
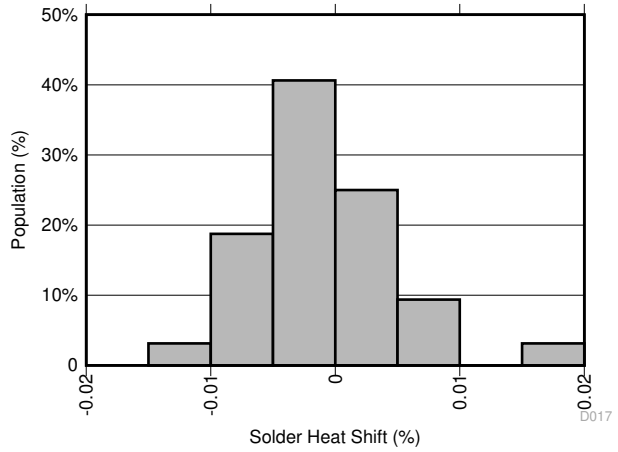


图 7-18. Thermal Hysteresis Distribution (Cycle 2)

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7.6 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = 12 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)



Refer to 节 8.1 for more information

图 7-19. Solder Heat Shift Distribution

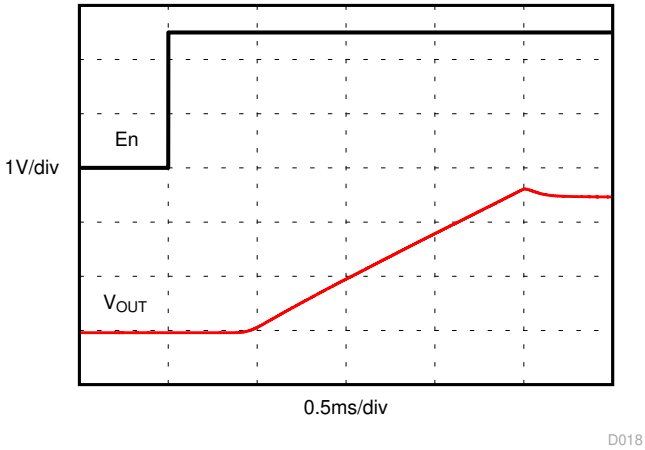


图 7-20. Turnon Time (Enable)

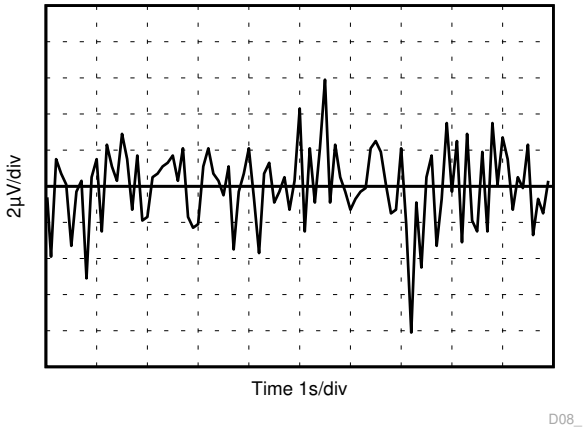


图 7-21. 0.1-Hz to 10-Hz Noise (V_{REF})

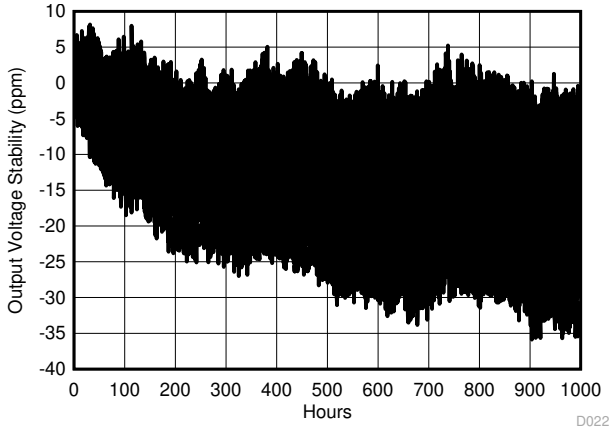


图 7-22. Long Term Stability - 1000 hours (V_{REF})

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8 Parameter Measurement Information

8.1 Solder Heat Shift

The materials used in the manufacture of the REF34-Q1 have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated. Mechanical and thermal stress on the device die can cause the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

In order to illustrate this effect, a total of 32 devices were soldered on four printed circuit boards [16 devices on each printed circuit board (PCB)] using lead-free solder paste and the paste manufacturer suggested reflow profile. The reflow profile is as shown in 图 8-1. The printed circuit board is comprised of FR4 material. The board thickness is 1.65 mm and the area is 114 mm × 152 mm. All measurements were taken after baking at 150°C.

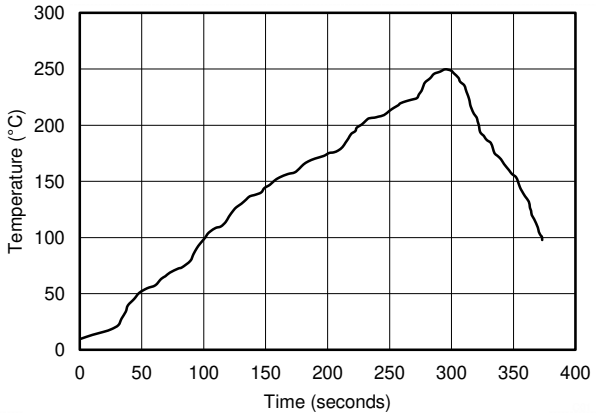


图 8-1. Reflow Profile

The reference output voltage is measured before and after the reflow process; the typical shift is displayed in 图 8-2. Although all tested units exhibit very low shifts (< 0.01%), higher shifts are also possible depending on the size, thickness, and material of the printed circuit board. An important note is that the histograms display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, the device must be soldered in the second pass to minimize its exposure to thermal stress.

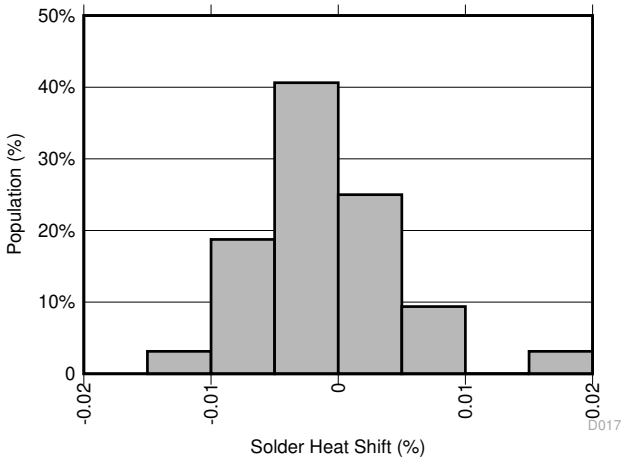


图 8-2. Solder Heat Shift Distribution, V_{REF} (%)

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8.2 Long-Term Stability

One of the key parameters of the REF34-Q1 references is long-term stability. Typical characteristic expressed as: curves shows the typical drift value for the REF34-Q1 is 25 ppm from 0 to 1000 hours. This parameter is characterized by measuring 32 units at regular intervals for a period of 1000 hours. It is important to understand that long-term stability is not ensured by design and that the output from the device may shift beyond the typical 25 ppm specification at any time. For systems that require highly stable output voltages over long periods of time, the designer should consider burning in the devices prior to use to minimize the amount of output drift exhibited by the reference over time

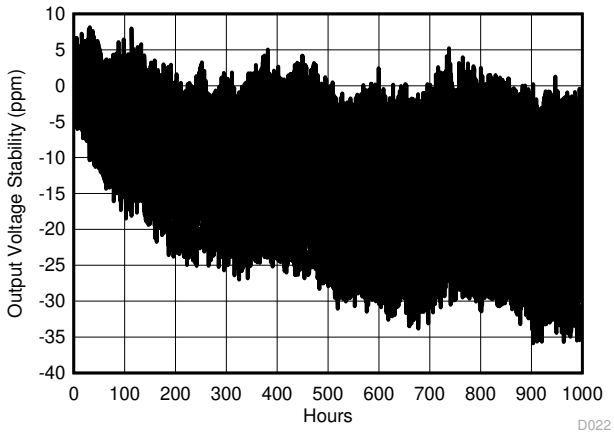


图 8-3. Long Term Stability - 1000 hours (V_{REF})

8.3 Thermal Hysteresis

Thermal hysteresis is measured with the REF34-Q1 soldered to a PCB, similar to a real-world application. Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. Hysteresis can be expressed by 方程式 1:

$$V_{HYST} \left(\frac{| V_{PRE} - V_{POST} |}{V_{NOM}} \right) \times 10^6 \text{ (ppm)} \quad (1)$$

where

- V_{HYST} = thermal hysteresis (in units of ppm)
- V_{NOM} = the specified output voltage
- V_{PRE} = output voltage measured at 25°C pre-temperature cycling
- V_{POST} = output voltage measured after the device has cycled from 25°C through the specified temperature range of – 40°C to +125°C and returns to 25°C.

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Typical thermal hysteresis distribution is as shown in 图 8-4.

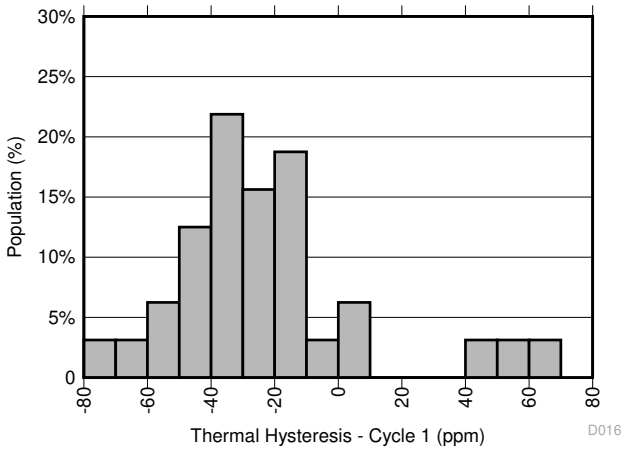


图 8-4. Thermal Hysteresis Distribution (V_{REF})

8.4 Power Dissipation

The REF34-Q1 voltage references are capable of source and sink up to 10 mA of load current across the rated input voltage range. However, when used in applications subject to high ambient temperatures, the input voltage and load current must be carefully monitored to ensure that the device does not exceeded its maximum power dissipation rating. The maximum power dissipation of the device can be calculated with 方程式 2:

$$T_J \quad T_A + P_D \times R_{\theta JA} \tag{2}$$

where

- P_D is the device power dissipation
- T_J is the device junction temperature
- T_A is the ambient temperature
- $R_{\theta JA}$ is the package (junction-to-air) thermal resistance

Because of this relationship, acceptable load current in high temperature conditions may be less than the maximum current-sourcing capability of the device. In no case should the device be operated outside of its maximum power rating because doing so can result in premature failure or permanent damage to the device.

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8.5 Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise can be seen in 图 8-5 . Device noise increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although care must be taken to ensure the output impedance does not degrade ac performance. Peak-to-peak noise measurement setup is shown in 图 8-5.

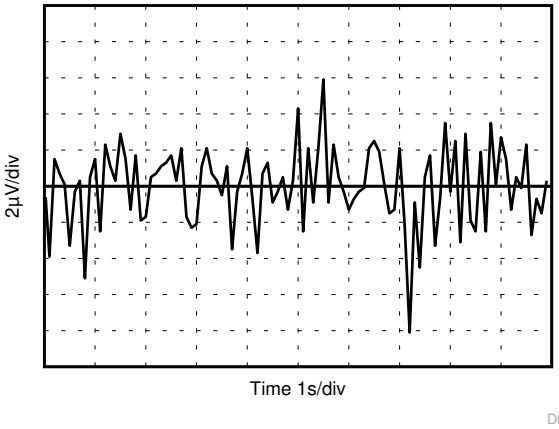


图 8-5. 0.1-Hz to 10-Hz Noise (V_{REF})

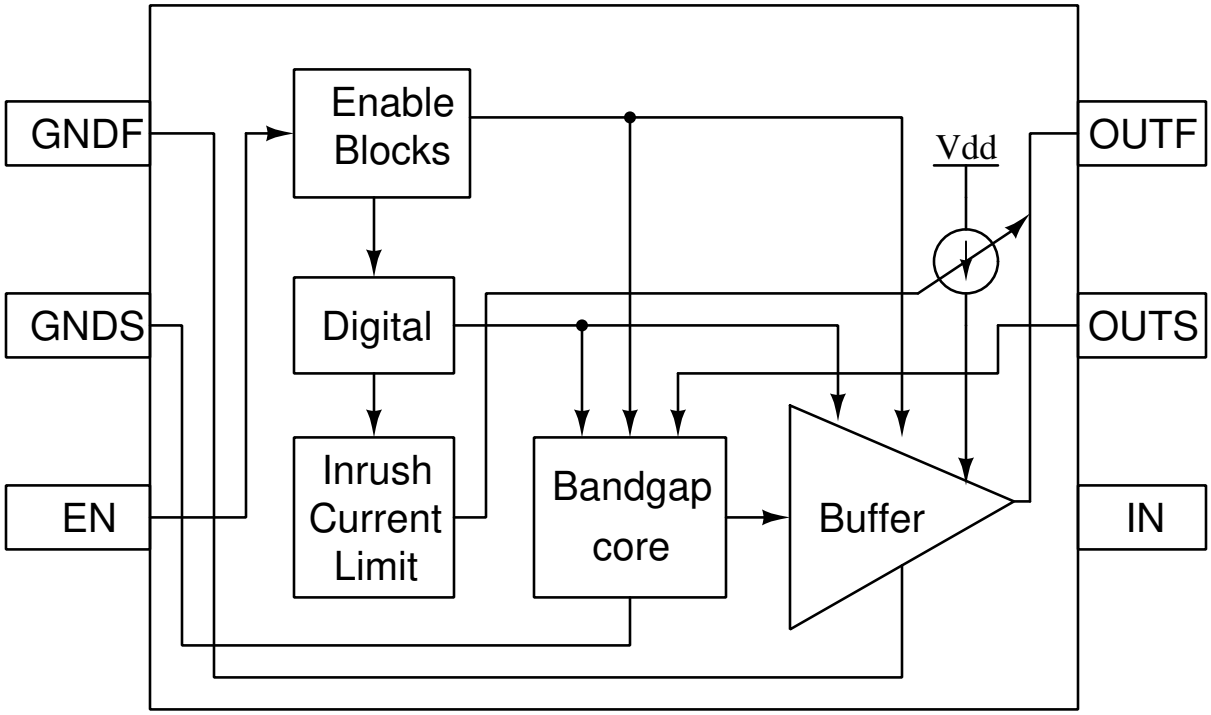
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9 Detailed Description

9.1 Overview

The REF34-Q1 devices are a family of low-noise, precision bandgap voltage references that are specifically designed for excellent initial voltage accuracy and drift. The 节 9.2 is a simplified block diagram of the REF34-Q1 showing basic band-gap topology.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Supply Voltage

The REF34-Q1 family of references features an extremely low dropout voltage. For loaded conditions, a typical dropout voltage versus load is shown on the front page. The REF34-Q1 family features a low quiescent current that is extremely stable over changes in both temperature and supply. The typical room temperature quiescent current is 72 μA, and the maximum quiescent current over temperature is just 95 μA. Supply voltages below the specified levels can cause the REF34-Q1 to momentarily draw currents greater than the typical quiescent current. Use a power supply with a fast rising edge and low output impedance to easily prevent this issue.

9.3.2 Low Temperature Drift

The REF34-Q1 devices are designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by 方程式 3:

$$\text{Drift} = \left(\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF} \times \text{Temperature Range}} \right) \times 10^6 \quad (3)$$

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9.3.3 Load Current

The REF34-Q1 family is specified to deliver a current load of ±10 mA per output. The V_{REF} output of the device are protected from short circuits by limiting the output short-circuit current to 18 mA. The device temperature increases according to 方程式 4:

$$T_J \quad T_A + P_D \times R_{\theta JA} \tag{4}$$

where

- T_J = junction temperature (°C),
- T_A = ambient temperature (°C),
- P_D = power dissipated (W), and
- $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

The REF34-Q1 maximum junction temperature must not exceed the absolute maximum rating of 150°C.

9.4 Device Functional Modes

9.4.1 EN Pin

When the EN pin of the REF34-Q1 is pulled high, the device is in active mode. The device must be in active mode for normal operation. The REF34-Q1 can be placed in a low-power mode by pulling the ENABLE pin low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device reduces to 2 µA in shutdown mode. The EN pin must not be pulled higher than VIN supply voltage. See the 节 *7.4* for logic high and logic low voltage levels.

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10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

As the REF34-Q1 devices have many applications and setups, there are many situations that this data sheet can not characterize in detail. Basic applications includes positive/negative voltage reference and data acquisition systems.

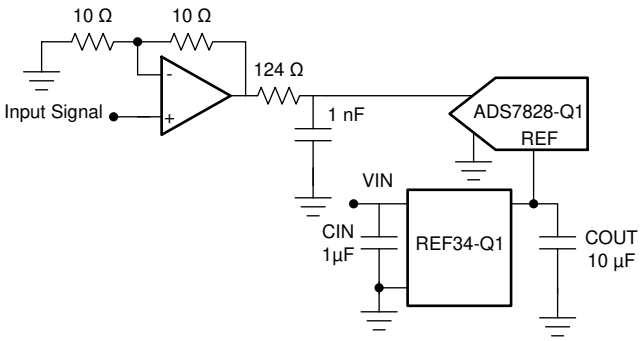
表 10-1. Typical Applications and Companion ADC/DAC

APPLICATIONS	ADC/DAC/Controller
ADAS	ADS7828-Q1
HEV/EV	ADS7951-Q1, ADS1120-Q1, ADS1258, BQ76PL455A-Q1

10.2 Typical Applications

10.2.1 Basic Voltage Reference Connection

The circuit shown in 图 10-1 shows the basic configuration for the REF34-Q1 references. Connect bypass capacitors according to the guidelines in *节 10.2.1.2.1*.



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图 10-1. Basic Reference Connection

10.2.1.1 Design Requirements

A detailed design procedure is based on a design example. For this design example, use the parameters listed in 表 10-2 as the input parameters.

表 10-2. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{IN}	12 V
Output voltage V_{OUT}	5 V
REF3450-Q1 input capacitor	1 µF
REF3450-Q1 output capacitor	10 µF

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Input and Output Capacitors

A 1- µ F to 10- µ F electrolytic or ceramic capacitor can be connected to the input to improve transient response in applications where the supply voltage may fluctuate. Connect an additional 0.1- µ F ceramic capacitor in parallel to reduce high frequency supply noise.

A ceramic capacitor of at least a 0.1 µ F must be connected to the output to improve stability and help filter out high frequency noise. An additional 1- µ F to 10- µ F electrolytic or ceramic capacitor can be added in parallel to improve transient performance in response to sudden changes in load current; however, keep in mind that doing so increases the turnon time of the device.

Best performance and stability is attained with low-ESR, low-inductance ceramic chip-type output capacitors (X5R, X7R, or similar). If using an electrolytic capacitor on the output, place a 0.1- µ F ceramic capacitor in parallel to reduce overall ESR on the output.

10.2.1.2.2 4-Wire Kelvin Connections

Current flowing through a PCB trace produces an IR voltage drop, and with longer traces, this drop can reach several millivolts or more, introducing a considerable error into the output voltage of the reference. A 1-inch long, 5-millimeter wide trace of 1-ounce copper has a resistance of approximately 100 m Ω at room temperature; at a load current of 10 mA, this can introduce a full millivolt of error. In an ideal board layout, the reference must be mounted as close as possible to the load to minimize the length of the output traces, and, therefore, the error introduced by voltage drop. However, in applications where this is not possible or convenient, force and sense connections (sometimes referred to as Kelvin sensing connections) are provided as a means of minimizing the IR drop and improving accuracy.

Kelvin connections work by providing a set of high impedance voltage-sensing lines to the output and ground nodes. Because very little current flows through these connections, the IR drop across their traces is negligible, and the output and ground

It is always advantageous to use Kelvin connections whenever possible. However, in applications where the IR drop is negligible or an extra set of traces cannot be routed to the load, the force and sense pins for both V_{OUT} and GND can simply be tied together, and the device can be used in the same fashion as a normal 3-terminal reference (as shown in 图 8-4).

10.2.1.2.3 V_{IN} Slew Rate Considerations

In applications with slow-rising input voltage signals, the reference exhibits overshoot or other transient anomalies that appear on the output. These phenomena also appear during shutdown as the internal circuitry loses power.

To avoid such conditions, ensure that the input voltage wave-form has both a rising and falling slew rate close to 6 V/ms.

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10.2.1.2.4 Shutdown/Enable Feature

The REF34-Q1 references can be switched to a low power shut-down mode when a voltage of 0.5 V or lower is input to the ENABLE pin. Likewise, the reference becomes operational for ENABLE voltages of 1.6 V or higher. During shutdown, the supply current drops to less than 2 μA, useful in applications that are sensitive to power consumption.

If using the shutdown feature, ensure that the ENABLE pin voltage does not fall between 0.5 V and 1.6 V because this causes a large increase in the supply current of the device and may keep the reference from starting up correctly. If not using the shutdown feature, however, the ENABLE pin can simply be tied to the IN pin, and the reference remains operational continuously.

10.2.1.3 Application Curves

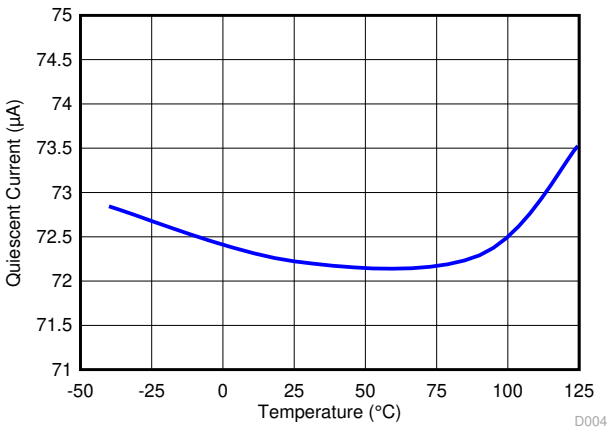


图 10-2. Quiescent Current vs Temperature

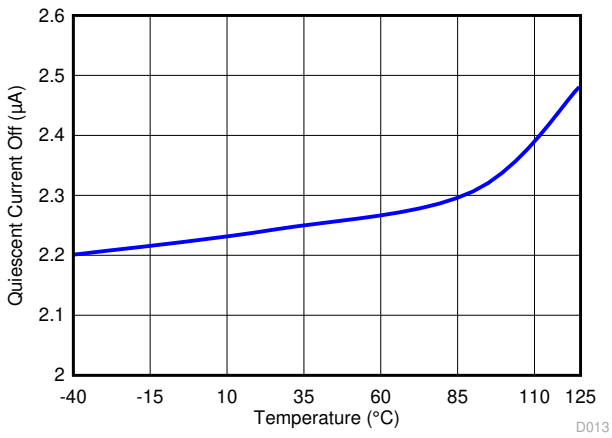


图 10-3. Quiescent Current Shutdown Mode

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10.2.2 Advanced Driver Assistance Systems (ADAS) Microcontroller Connection

10.2.2.1 Basic Voltage Reference Connection

The circuit shown in 图 10-4 shows the basic configuration for the REF34-Q1 references.

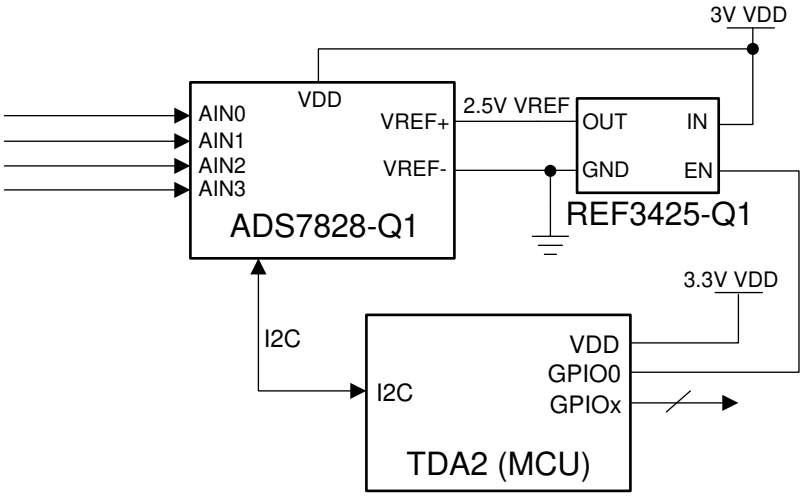


图 10-4. ADAS Microcontroller Application

10.2.2.2 Design Requirements

In ADAS applications it is common to use an ADC with a MCU to monitor the voltage rails to the MCU/DSP/FPGAs. In figure 图 10-4 the automotive TI Jacinto™ TDA2 MCU is using a ADS7828-Q1 to monitor several analog input signals and in ADAS these signals will be the system power rails. It is important to monitor these power rails because tighter rail requirements allow for further system monitoring and optimization. The REF3425-Q1 is used in this application to provide the precise voltage reference signal. In these systems it is not typical to have calibration and such the most precise low power voltage reference is necessary to be able to measure down to 1% accuracy on key power rails.

For this design example, use the parameters listed in 表 10-3 as the input parameters and desired output parameters.

表 10-3. Typical Core Voltage Rail Monitoring

Specification	Requirement
Input Voltage V_{IN}	3V
Output Voltage	2.5V
Voltage Power Rail	1V
Max Error on Voltage Power Rail	1%
Temperature Range	-40°C to 125°C

10.2.2.3 Detailed Design Procedure

It is important to keep track of the error margin in this system to make sure that the total error of the voltage reference and ADC are less than the maximum 1% error allowed. To calculate the total RSS error of a voltage reference use 方程式 5.

$$\text{Error}_{\text{VREF}}\big|_{\text{Total}} \sqrt{(\text{Accuracy})^2 + (\text{TempCo})^2 + (\text{TempHyst})^2 + (\text{LongTerm Drift})^2 + (1/f\ \text{Noise})^2} \quad (5)$$

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With the RSS error of the voltage reference, the ADC error needs also needs to be calculated using the RSS method as seen in 方程式 6. 方程式 7 can then be used to sum both errors. It is important to make sure that only the applicable voltage reference error in relation to the measured signal is used.

$$\text{Total Unadjusted Error} = \text{Error}_{\text{ADC}}\big|_{\text{Total}} \sqrt{(\text{Gain Error})^2 + (\text{Offset Error})^2 + (\text{INL Error})^2 + (\text{DNL Error})^2} \quad (6)$$

$$\text{Error}_{\text{VREF+ADC}}\big|_{\text{Total}} \quad \sqrt{\left(\text{Error}_{\text{VREF@AIN}}\big|_{\text{Total}}\right)^2 + \left(\text{Error}_{\text{ADC}}\big|_{\text{Total}}\right)^2} \quad (7)$$

10.2.2.4 Enable Feature in ADAS

In ADAS applications it is important to have a low quiescent current when the automotive application does not require the ADAS system to be in use. This creates a need for a low standby power so the battery life is preserved but there is also need for the system to still be readily available to start-up with minimal delays. In such situations the MCU and other systems will go into a standby mode to ensure that the power consumption is lowered to the absolute minimum. The REF3425-Q1 offers an enable pin that can be controlled by the MCU to activate shutdown mode with causes the REF3425-Q1 to go into stand by and consume 3 μA (maximum) and allow for a longer battery life.

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11 Power Supply Recommendations

The REF34-Q1 family of references feature an extremely low-dropout voltage. These references can be operated with a supply of only 50 mV above the output voltage. TI recommends a supply bypass capacitor ranging between 0.1 µF to 10 µF.

12 Layout

12.1 Layout Guidelines

图 12-1 illustrates an example of a PCB layout for a data acquisition system using the REF34-Q1. Some key considerations are:

- Connect low-ESR, 0.1- µ F ceramic bypass capacitors at V_{IN}, V_{REF} of the REF34-Q1.
- Decouple other active devices in the system per the device specifications.
- Using a solid ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

12.2 Layout Example

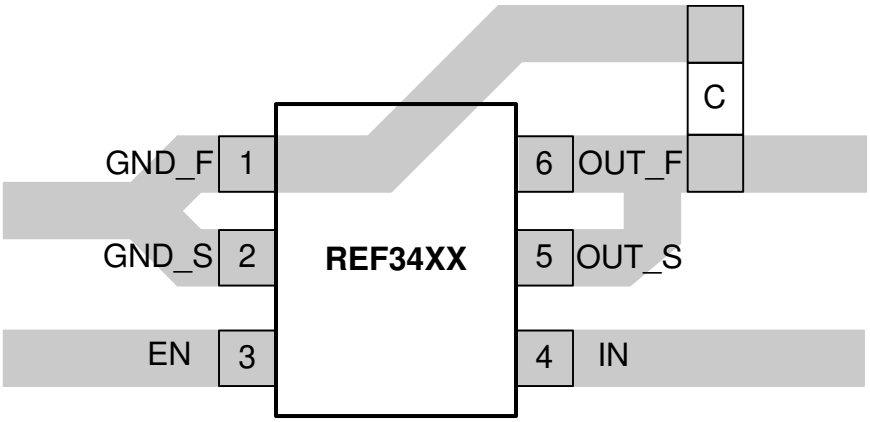


图 12-1. Layout Example (REF34xx-Q1)

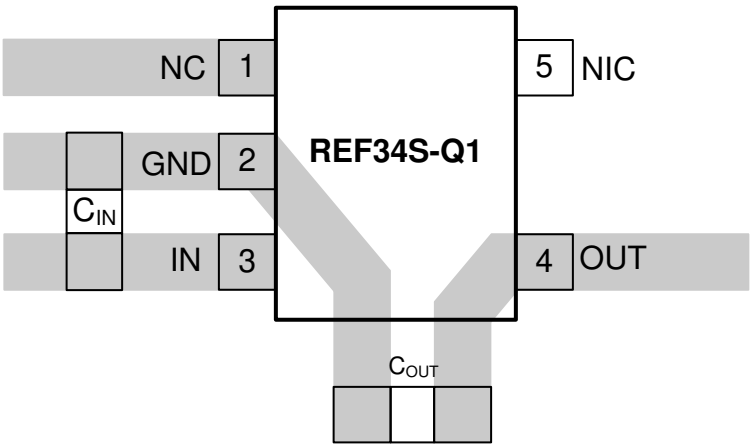


图 12-2. Layout Example (REF34xxS-Q1)

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13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- *INA21x Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors*
- *Low-Drift Bidirectional Single-Supply Low-Side Current Sensing Reference Design*

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF3425QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1OLC	Samples
REF3425QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2E93	Samples
REF3425SQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2D6C	Samples
REF3430QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1OMC	Samples
REF3430QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2FW3	Samples
REF3430SQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2D7C	Samples
REF3433QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1ONC	Samples
REF3433QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2FV3	Samples
REF3433SQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2D8C	Samples
REF3440QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1OOC	Samples
REF3440QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2FQ3	Samples
REF3440SQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2D9C	Samples
REF3450QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1OPC	Samples
REF3450QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2FX3	Samples
REF3450SQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2DAC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

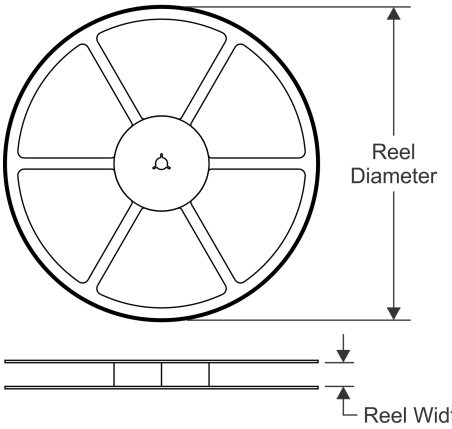
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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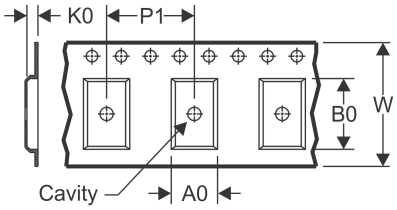
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

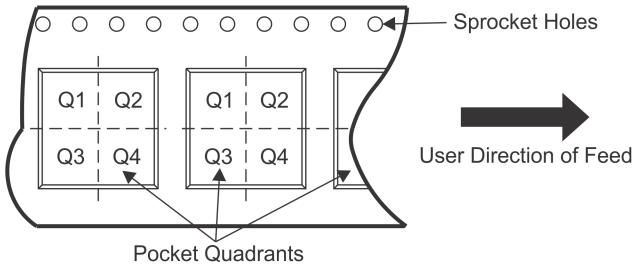


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

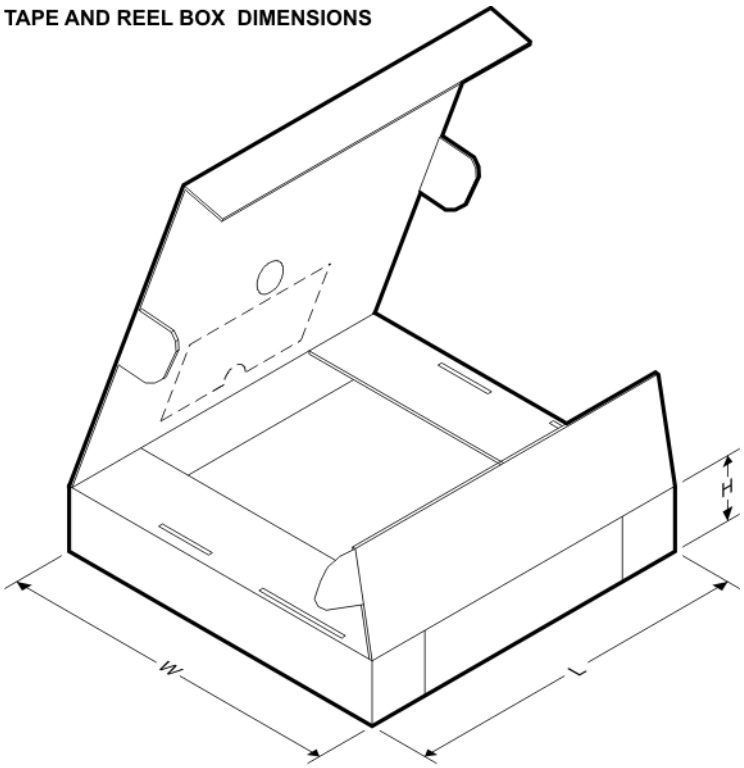
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF3425QDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF3425QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF3425SQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF3430QDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF3430QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF3430SQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF3433QDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF3433SQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF3440QDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF3440QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF3440SQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF3450QDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF3450QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF3450SQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

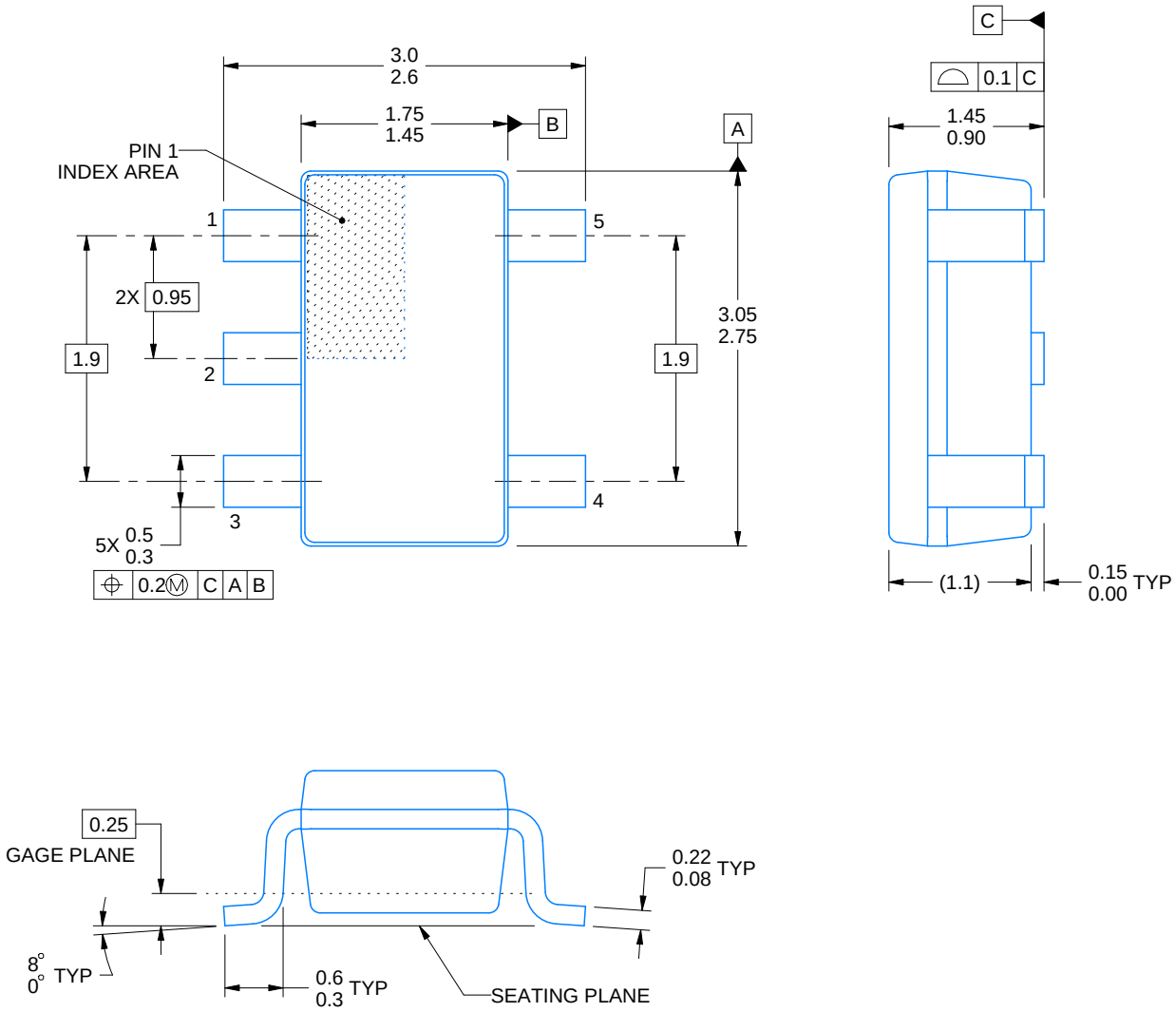
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF3425QDBVRQ1	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF3425QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
REF3425SQDBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0
REF3430QDBVRQ1	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF3430QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
REF3430SQDBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0
REF3433QDBVRQ1	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF3433SQDBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0
REF3440QDBVRQ1	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF3440QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
REF3440SQDBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0
REF3450QDBVRQ1	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF3450QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
REF3450SQDBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

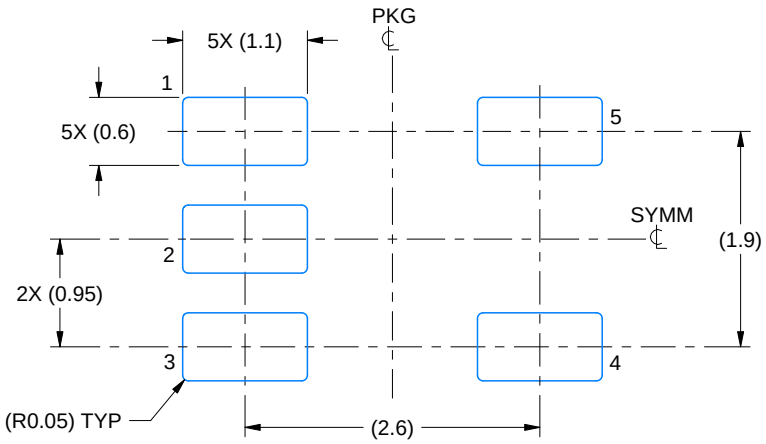
SMALL OUTLINE TRANSISTOR



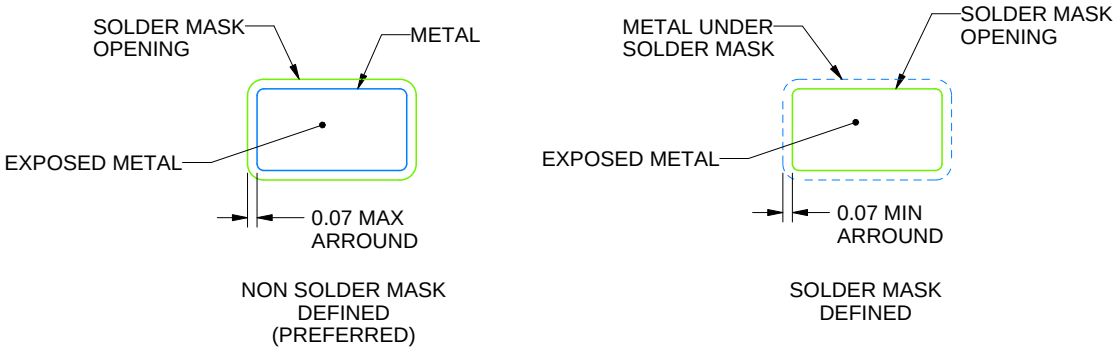
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

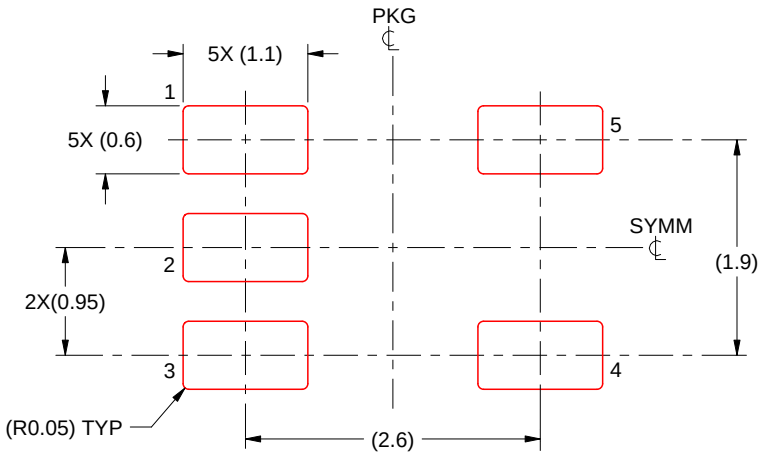


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

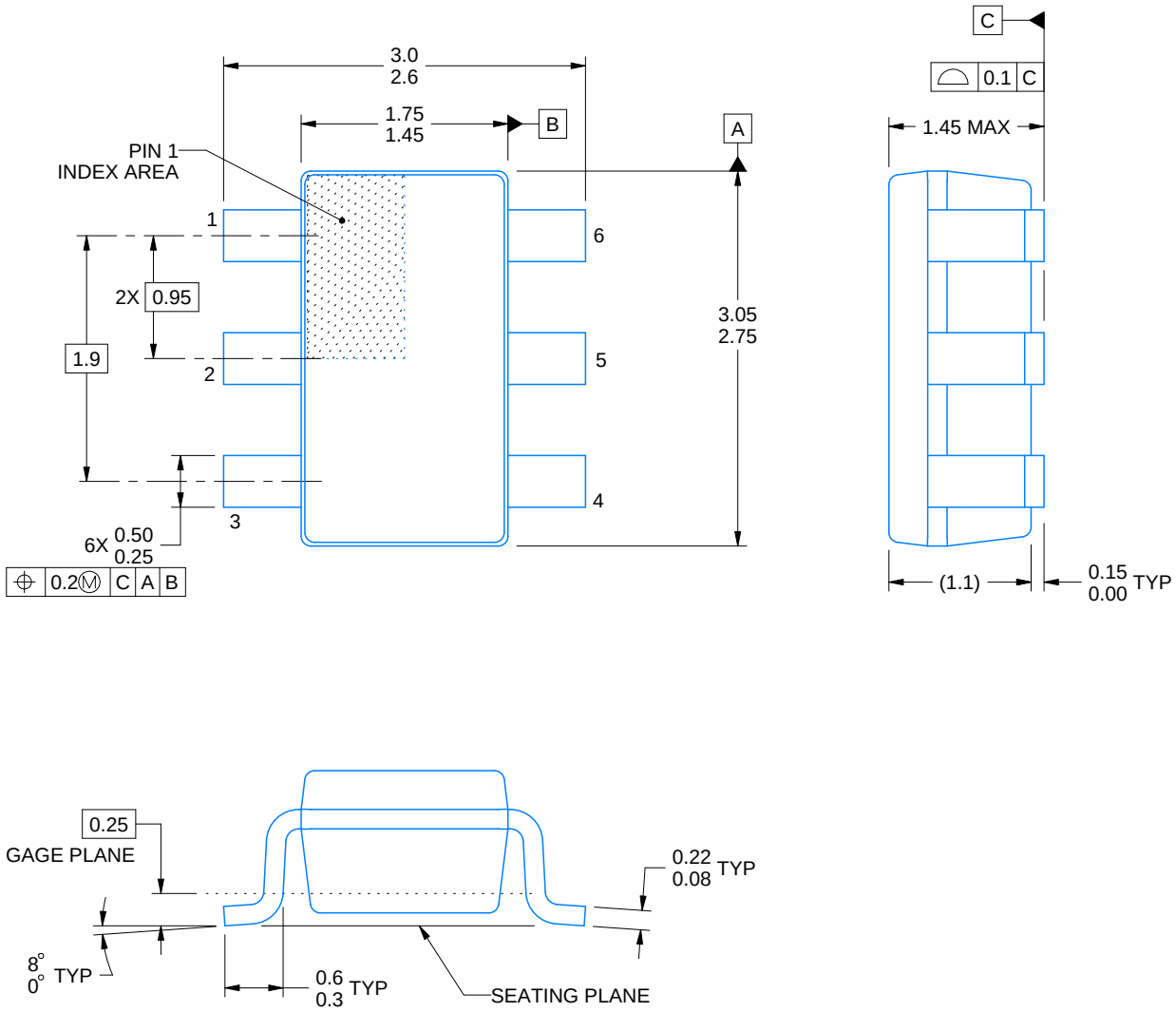
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

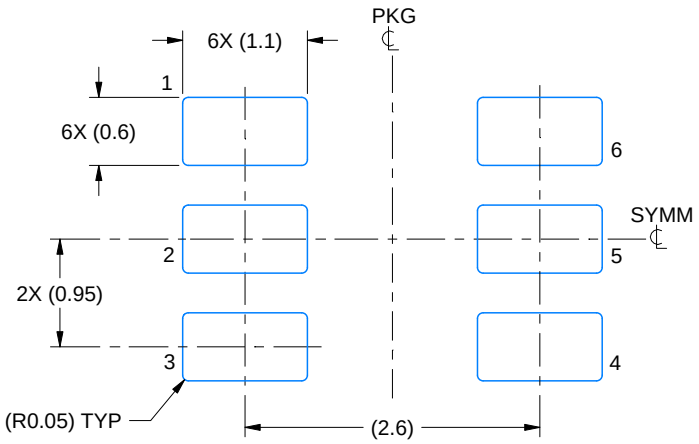
SMALL OUTLINE TRANSISTOR



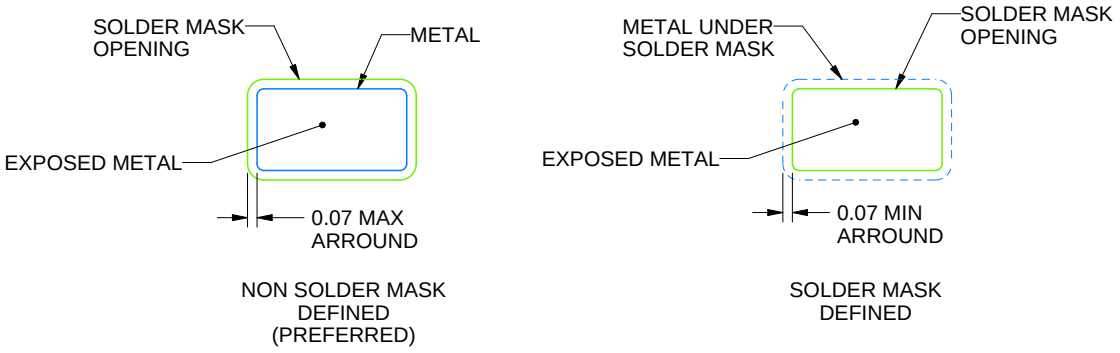
4214840/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

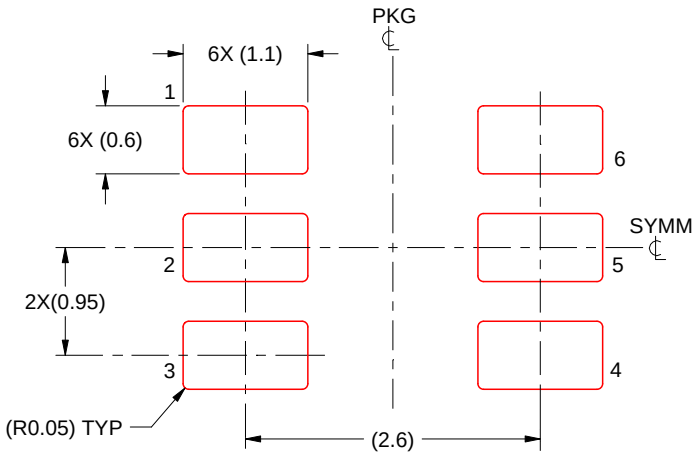


SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



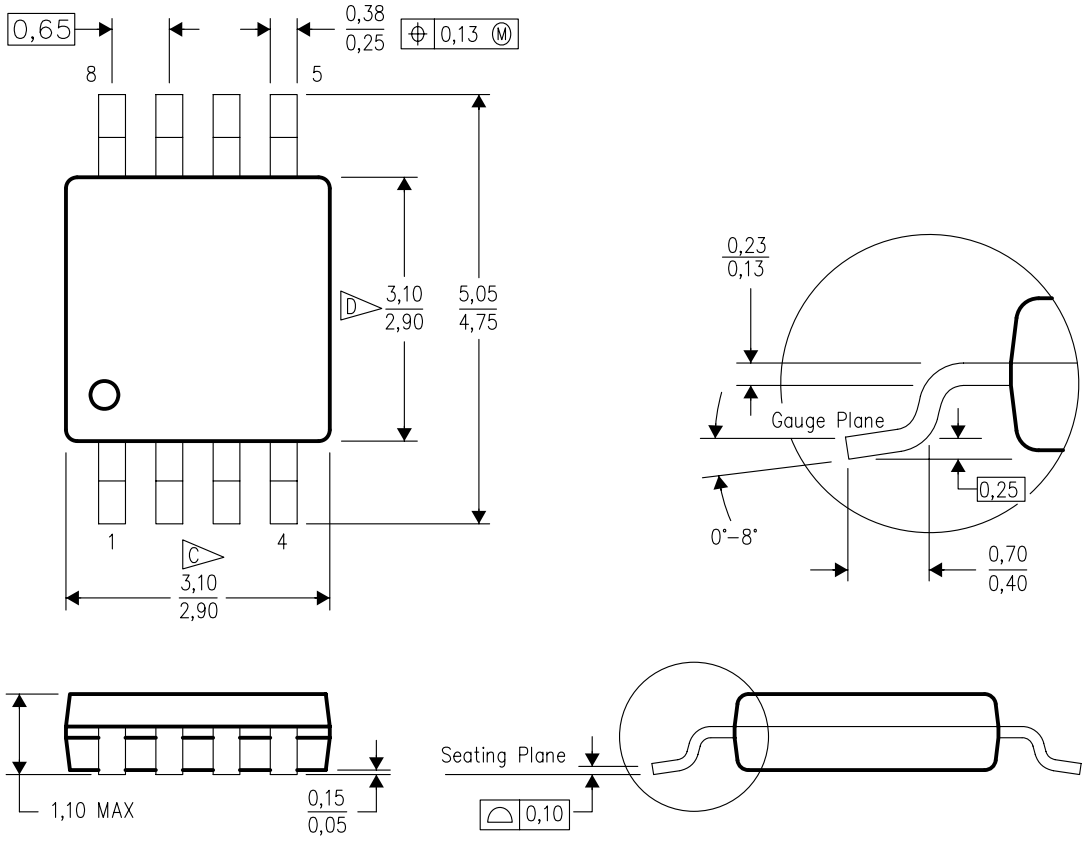
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

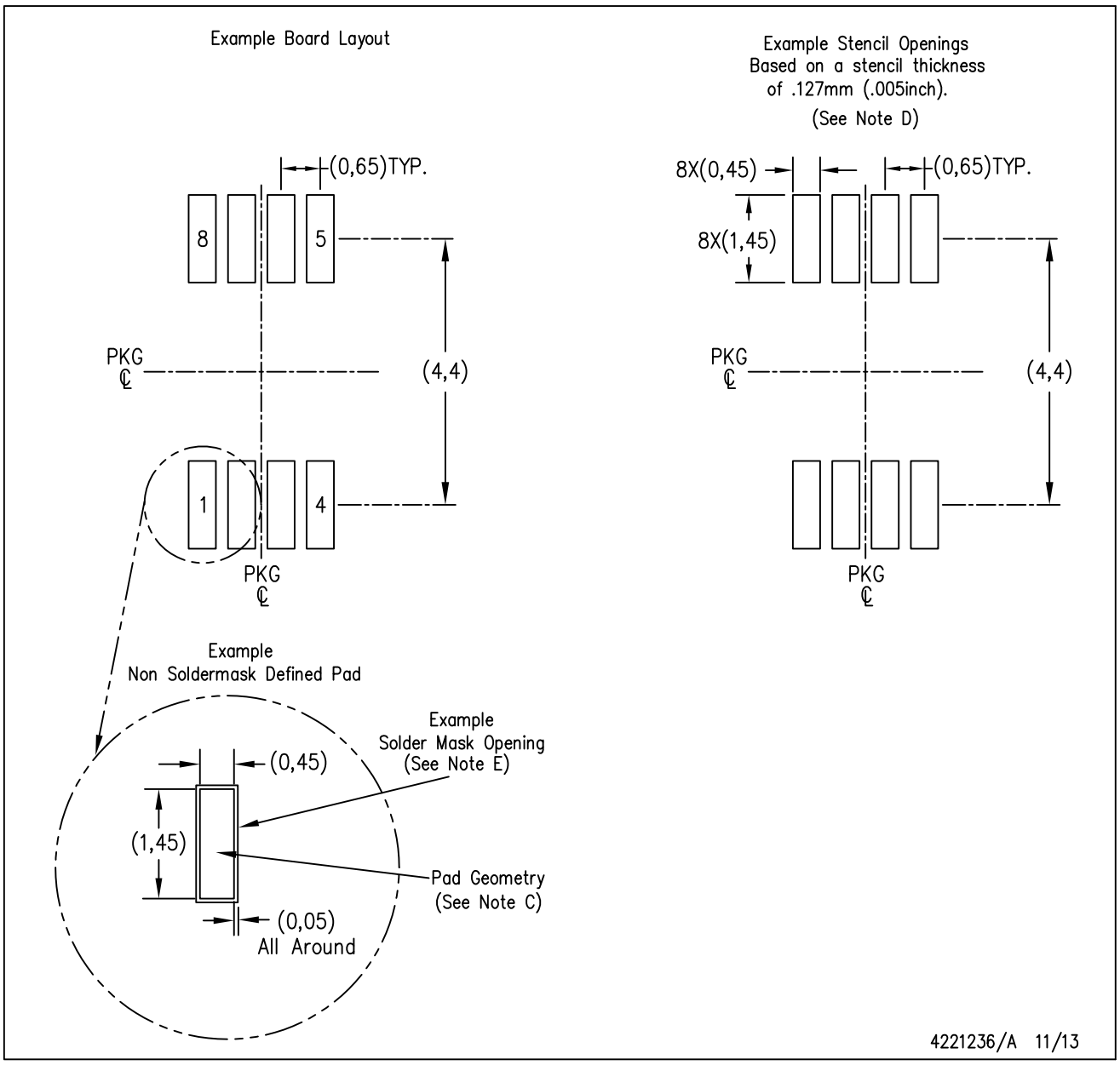
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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