TMUX110x 5V、低泄漏电流、1:1 (SPST) 精密开关

1 特性

- 宽电源电压范围：1.08V 至 5.5V
- 低泄漏电流：3pA
- 低电荷注入：–1.5pC
- 低导通电阻：1.8Ω
- –40°C 至 +125°C 工作温度
- 1.8V 逻辑兼容
- 失效防护逻辑
- 轨至轨运行
- 双向信号路径
- 先断后合开关
- ESD 保护 HBM：2000V

2 应用

- 采样保持电路
- 反馈增益开关
- 信号隔离
- 现场变送器
- 可编程逻辑控制器 (PLC)
- 工厂自动化和控制
- 超声波扫描仪
- 患者监护和诊断
- 心电图 (ECG)
- 数据采集系统 (DAQ)
- ATE 测试设备
- 电池测试设备
- 仪表：实验室、分析、便携
- 智能仪表：水表和燃气表
- 光纤网络
- 光学测试设备

3 说明

TMUX1101 和 TMUX1102 是精密互补金属氧化物半导体 (CMOS) 单极单投 (SPST) 开关。1.08V 至 5.5V 的宽电源电压工作范围 可支持 医疗设备到工业系统的大量应用。这些器件可支持源极 (S) 和漏极 (D) 引脚上 GND 到 V_{DD} 范围的双向模拟和数字信号。

逻辑控制输入 (SEL) 具有兼容 1.8V 逻辑电平的阈值。当器件在有效电源电压范围内运行时，该阈值可确保 TTL 和 CMOS 的逻辑兼容性。SEL 为逻辑 1 时，TMUX1101 的开关打开，而 SEL 为逻辑 0 时，TMUX1102 打开。失效防护逻辑电路要求先在 SEL 引脚上施加电压，然后在电源引脚上施加电压，从而保护器件免受潜在的损害。

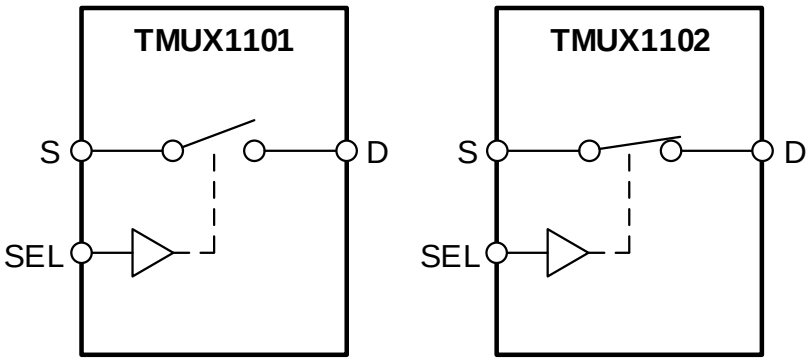
TMUX110x 器件是精密开关和多路复用器器件系列中的一部分。这些器件具有非常低的导通和关断泄漏电流以及较低的电荷注入，因此可用于高精度测量 应用提供了出色的功能性与安全性。
3nA 的低电源电流和小型封装选项使其可用于便携式应用标准。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TMUX1101 TMUX1102	SC70 (5) (DCK)	2.00mm × 1.25mm
	SOT-23 (5) (DBV)	2.90mm x 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

TMUX110x 方框图



ALL SWITCHES SHOWN FOR A LOGIC 0 INPUT

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (July 2019) to Revision B **Page**

- 删除了*器件信息* 表中的*产品预览* 说明 ... 1
- Deleted the *Product Preview* note from the *Device Comparison Table* table ... 3
- Added DBV (SOT-23) thermal values to *Thermal Information* ... 4

Changes from Original (March 2019) to Revision A **Page**

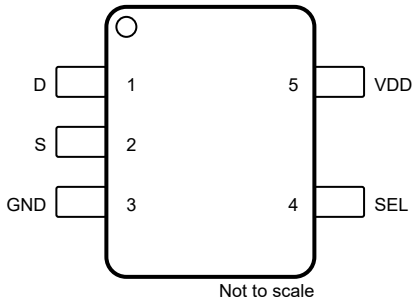
- 将文档从*预告信息*更改为*混合*状态。 ... 1

5 Device Comparison Table

PRODUCT	DESCRIPTION
TMUX1101	Low-Leakage-Current, 1:1 (SPST), Precision Switch (Logic High)
TMUX1102	Low-Leakage-Current, 1:1 (SPST), Precision Switch (Logic Low)

6 Pin Configuration and Functions

DCK Package
5-Pin SC70
Top View



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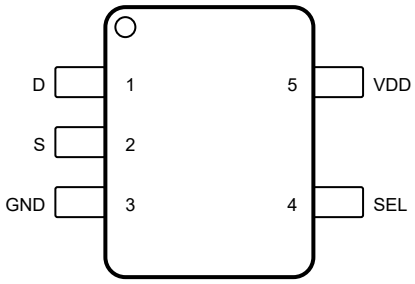
DBV Package
5-Pin SOT-23
Top View



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Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
D	1	I/O	Drain pin. Can be an input or output.
S	2	I/O	Source pin. Can be an input or output.
GND	3	P	Ground (0 V) reference
SEL	4	I	Logic control input. Controls the switch state as shown in Truth Tables.
VDD	5	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.

(1) I = input, O = output, I/O = input and output, P = power

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	–0.5	6	V
V_{SEL}	Logic control input pin voltage (SEL)	–0.5	6	V
I_{SEL}	Logic control input pin current (SEL)	–30	30	mA
V_S or V_D	Source or drain voltage (S, D)	–0.5	V_{DD}+0.5	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (S, D)	–30	30	mA
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002, all pins(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	1.08		5.5	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (S, D)	0		V_{DD}	V
V_{SEL}	Logic control input pin voltage (SEL)	0		5.5	V
T_A	Ambient temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TMUX1101 / TMUX1102		UNIT
		DCK (SC70)	DBV (SOT-23)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	348.5	224.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	238.3	150.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	205.7	130.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	141.4	74.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	204.7	129.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics (V_{DD} = 5 V ±10 %)

at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-resistance	25°C		1.8	4	Ω
			–40°C to +85°C			4.5	Ω
			–40°C to +125°C			4.9	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-resistance	25°C		0.85		Ω
			–40°C to +85°C			1.6	Ω
			–40°C to +125°C			1.6	Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 5 V Switch Off V_D = 4.5 V / 1.5 V V_S = 1.5 V / 4.5 V Refer to Off-leakage current	25°C	–0.08	±0.005	0.08	nA
			–40°C to +85°C	–0.3		0.3	nA
			–40°C to +125°C	–0.9		0.9	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 5 V Switch Off V_D = 4.5 V / 1.5 V V_S = 1.5 V / 4.5 V Refer to Off-leakage current	25°C	–0.08	±0.005	0.08	nA
			–40°C to +85°C	–0.3		0.3	nA
			–40°C to +125°C	–0.9		0.9	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 5 V Switch On V_D = V_S = 2.5 V Refer to On-leakage current	25°C	–0.025	±0.003	0.025	nA
			–40°C to +85°C	–0.2		0.2	nA
			–40°C to +125°C	–0.95		0.95	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 5 V Switch On V_D = V_S = 4.5 V / 1.5 V Refer to On-leakage current	25°C	–0.1	±0.01	0.1	nA
			–40°C to +85°C	–0.35		0.35	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS (SEL)							
V_{IH}	Input logic high		–40°C to +125°C	1.49		5.5	V
V_{IL}	Input logic low		–40°C to +125°C	0		0.87	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.06	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C		0.003		µA
			–40°C to +125°C			1	µA

(1) When V_S is 4.5 V, V_D is 1.5 V or when V_S is 1.5 V, V_D is 4.5 V.

Electrical Characteristics (V_{DD} = 5 V ±10 %) (continued)

at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time from control input	V_S = 3 V R_L = 200 Ω, C_L = 15 pF Refer to Transition time	25°C		12		ns
			–40°C to +85°C			17	ns
			–40°C to +125°C			18	ns
Q_C	Charge Injection	V_S = 1 V R_S = 0 Ω, C_L = 1 nF Refer to Charge injection	25°C		–1.5		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Off isolation	25°C		–62		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Off isolation	25°C		–40		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF Refer to Bandwidth	25°C		300		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		6		pF
C_{DOFF}	Drain off capacitance	f = 1 MHz	25°C		10		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		17		pF

7.6 Electrical Characteristics (V_{DD} = 3.3 V ±10 %)

at T_A = 25°C, V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-resistance	25°C		3.7	8.8	Ω
			–40°C to +85°C			9.5	Ω
			–40°C to +125°C			9.8	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-resistance	25°C		1.9		Ω
			–40°C to +85°C		2		Ω
			–40°C to +125°C		2.2		Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 3.3 V Switch Off V_D = 3 V / 1 V V_S = 1 V / 3 V Refer to Off-leakage current	25°C	–0.05	±0.001	0.05	nA
			–40°C to +85°C	–0.2		0.2	nA
			–40°C to +125°C	–0.9		0.9	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 3.3 V Switch Off V_D = 3 V / 1 V V_S = 1 V / 3 V Refer to Off-leakage current	25°C	–0.05	±0.001	0.05	nA
			–40°C to +85°C	–0.2		0.2	nA
			–40°C to +125°C	–0.9		0.9	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 3.3 V Switch On V_D = V_S = 3 V / 1 V Refer to On-leakage current	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.35		0.35	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS (SEL)							
V_{IH}	Input logic high		–40°C to +125°C	1.35		5.5	V
V_{IL}	Input logic low		–40°C to +125°C	0		0.8	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C		0.002		µA
			–40°C to +125°C			0.65	µA

(1) When V_S is 3 V, V_D is 1 V or when V_S is 1 V, V_D is 3 V.

Electrical Characteristics (V_{DD} = 3.3 V ±10 %) (continued)

at T_A = 25°C, V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time from control input	V_S = 2 V R_L = 200 Ω, C_L = 15 pF Refer to Transition time	25°C		14		ns
			–40°C to +85°C			20	ns
			–40°C to +125°C			22	ns
Q_C	Charge Injection	V_S = 1 V R_S = 0 Ω, C_L = 1 nF Refer to Charge injection	25°C		–1.5		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Off isolation	25°C		–62		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Off isolation	25°C		–40		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF Refer to Bandwidth	25°C		300		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		6		pF
C_{DOFF}	Drain off capacitance	f = 1 MHz	25°C		10		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		17		pF

7.7 Electrical Characteristics (V_{DD} = 1.8 V ±10 %)

at T_A = 25°C, V_{DD} = 1.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-resistance	25°C		40		Ω
			–40°C to +85°C			80	Ω
			–40°C to +125°C			80	Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 1.98 V Switch Off V_D = 1.62 V / 1 V V_S = 1 V / 1.62 V Refer to Off-leakage current	25°C	–0.05	±0.001	0.05	nA
			–40°C to +85°C	–0.2		0.2	nA
			–40°C to +125°C	–0.9		0.9	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 1.98 V Switch Off V_D = 1.62 V / 1 V V_S = 1 V / 1.62 V Refer to Off-leakage current	25°C	–0.05	±0.001	0.05	nA
			–40°C to +85°C	–0.2		0.2	nA
			–40°C to +125°C	–0.9		0.9	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 1.98 V Switch On V_D = V_S = 1.62 V / 1 V Refer to On-leakage current	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.35		0.35	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS (SEL)							
V_{IH}	Input logic high		–40°C to +125°C	1.07		5.5	V
V_{IL}	Input logic low		–40°C to +125°C	0		0.68	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C		0.001		µA
			–40°C to +125°C			0.45	µA

(1) When V_S is 1.62 V, V_D is 1 V or when V_S is 1 V, V_D is 1.62 V.

Electrical Characteristics (V_{DD} = 1.8 V ±10 %) (continued)

at T_A = 25°C, V_{DD} = 1.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time from control input	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to Transition time	25°C		25		ns
			–40°C to +85°C			44	ns
			–40°C to +125°C			44	ns
Q_C	Charge Injection	V_S = 1 V R_S = 0 Ω, C_L = 1 nF Refer to Charge injection	25°C		–1.5		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Off isolation	25°C		–62		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Off isolation	25°C		–40		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF Refer to Bandwidth	25°C		300		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		6		pF
C_{DOFF}	Drain off capacitance	f = 1 MHz	25°C		10		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		17		pF

7.8 Electrical Characteristics (V_{DD} = 1.2 V ±10 %)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-resistance	25°C		70		Ω
			–40°C to +85°C			105	Ω
			–40°C to +125°C			105	Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 1.32 V Switch Off V_D = 1 V / 0.8 V V_S = 0.8 V / 1 V Refer to Off-leakage current	25°C	–0.05	±0.001	0.05	nA
			–40°C to +85°C	–0.2		0.2	nA
			–40°C to +125°C	–0.9		0.9	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 1.32 V Switch Off V_D = 1 V / 0.8 V V_S = 0.8 V / 1 V Refer to Off-leakage current	25°C	–0.05	±0.001	0.05	nA
			–40°C to +85°C	–0.2		0.2	nA
			–40°C to +125°C	–0.9		0.9	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 1.32 V Switch On V_D = V_S = 1 V / 0.8 V Refer to On-leakage current	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.35		0.35	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS (SEL)							
V_{IH}	Input logic high		–40°C to +125°C	0.96		5.5	V
V_{IL}	Input logic low		–40°C to +125°C	0		0.36	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C		0.001		µA
			–40°C to +125°C			0.38	µA

(1) When V_S is 1 V, V_D is 0.8 V or when V_S is 0.8 V, V_D is 1 V.

Electrical Characteristics (V_{DD} = 1.2 V ±10 %) (continued)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time from control input	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to Transition time	25°C		55		ns
			–40°C to +85°C			190	ns
			–40°C to +125°C			190	ns
Q_C	Charge Injection	V_S = 1 V R_S = 0 Ω, C_L = 1 nF Refer to Charge injection	25°C		–1.5		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Off isolation	25°C		–62		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Off isolation	25°C		–42		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF Refer to Bandwidth	25°C		300		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		6		pF
C_{DOFF}	Drain off capacitance	f = 1 MHz	25°C		10		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		17		pF

7.9 Typical Characteristics

at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

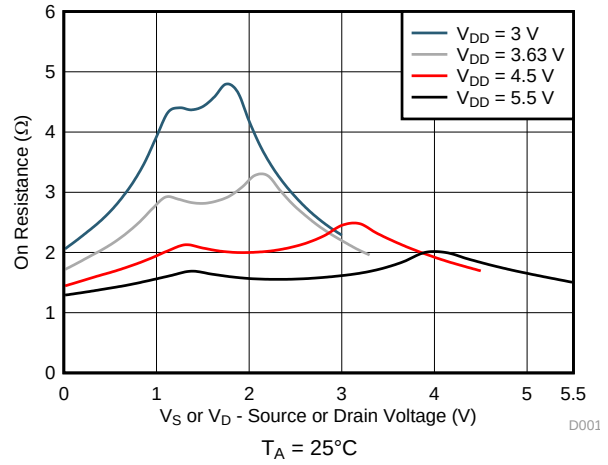


图 1. On-Resistance vs Source or Drain Voltage

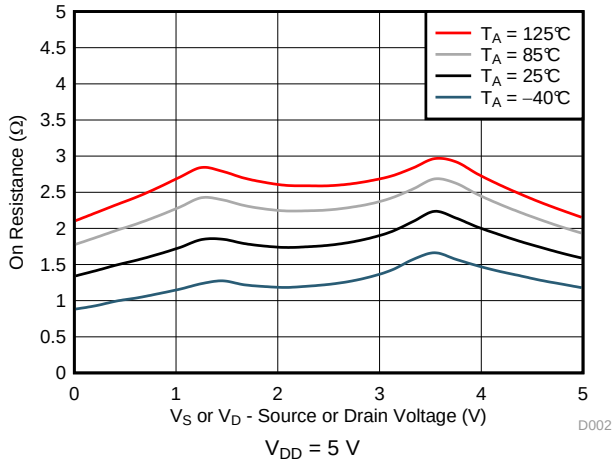


图 2. On-Resistance vs Temperature

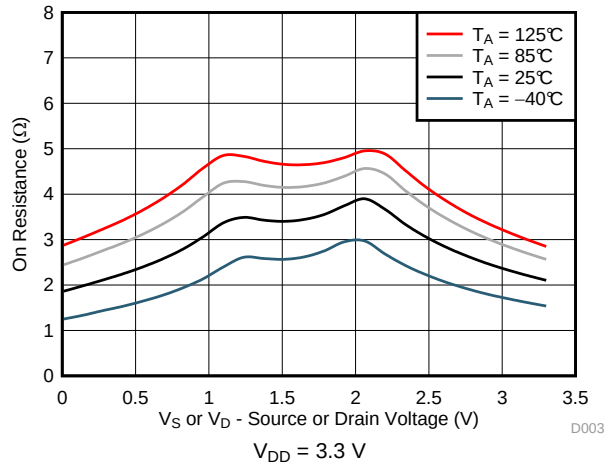


图 3. On-Resistance vs Temperature

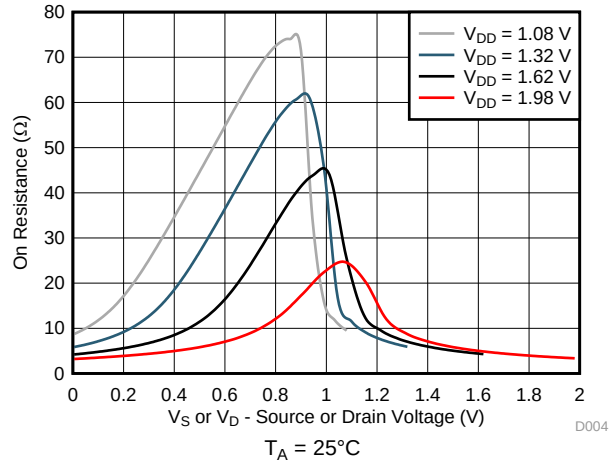


图 4. On-Resistance vs Source or Drain Voltage

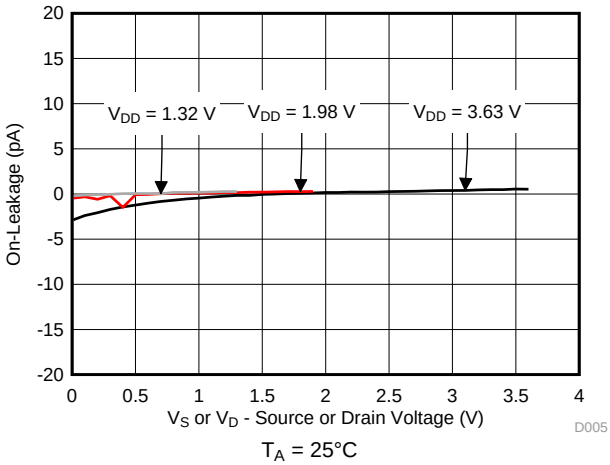


图 5. On-Leakage vs Source or Drain Voltage

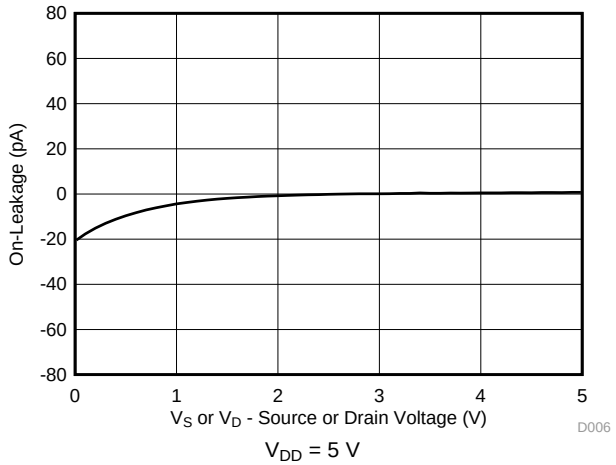
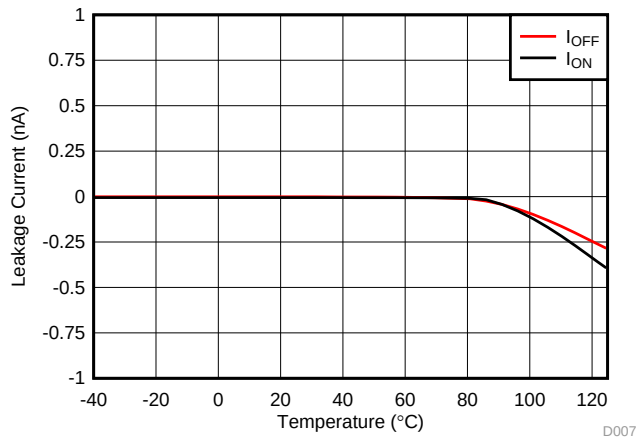


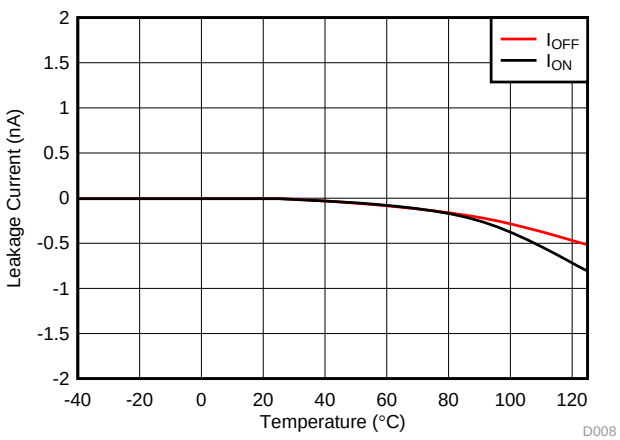
图 6. On-Leakage vs Source or Drain Voltage

Typical Characteristics (接下页)



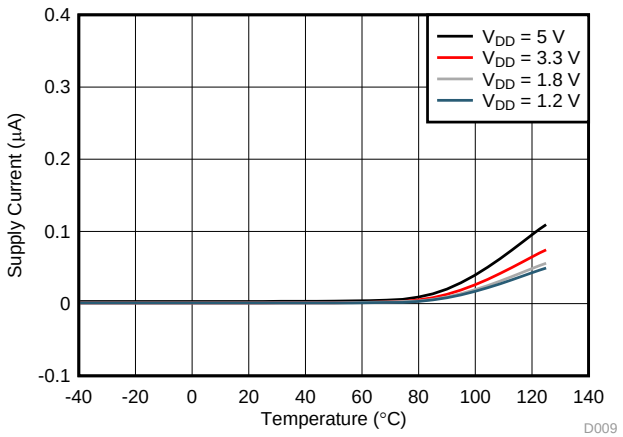
V_{DD} = 3.3 V

图 7. Leakage Current vs Temperature



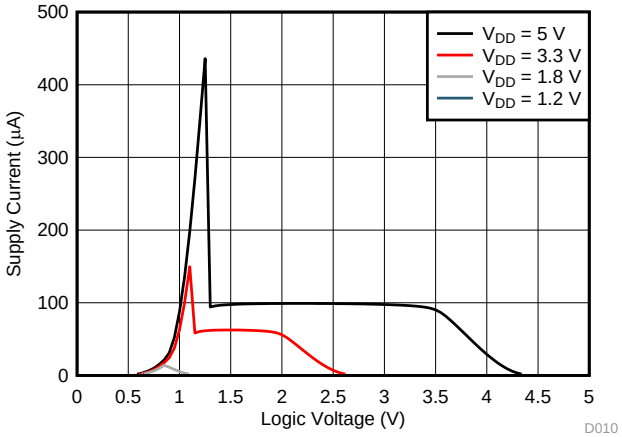
V_{DD} = 5 V

图 8. Leakage Current vs Temperature



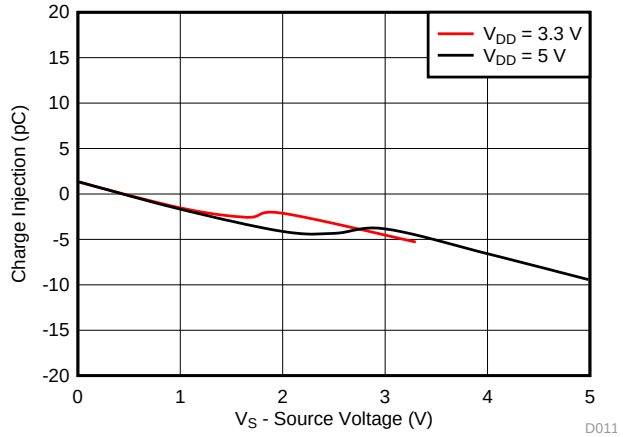
V_{SEL} = 5.5 V

图 9. Supply Current vs Temperature



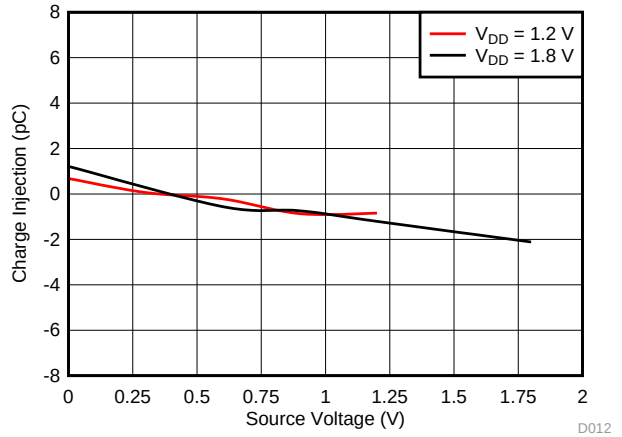
T_A = 25°C

图 10. Supply Current vs Logic Voltage



T_A = -40°C to 125°C

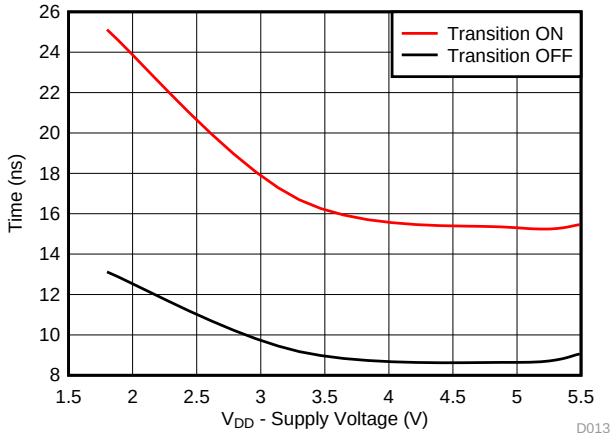
图 11. Charge Injection vs Source Voltage



T_A = –40°C to 125°C

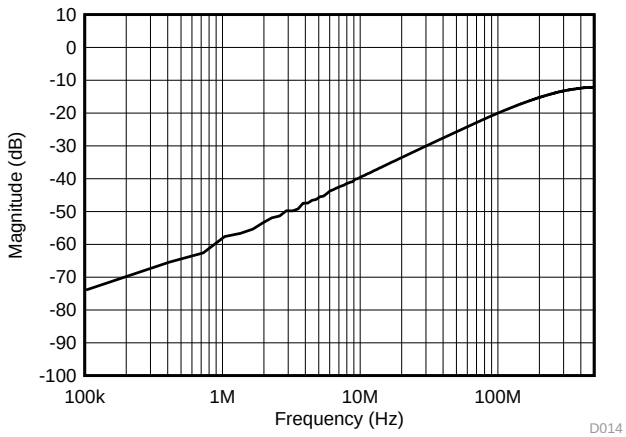
图 12. Charge Injection vs Source Voltage

Typical Characteristics (接下页)



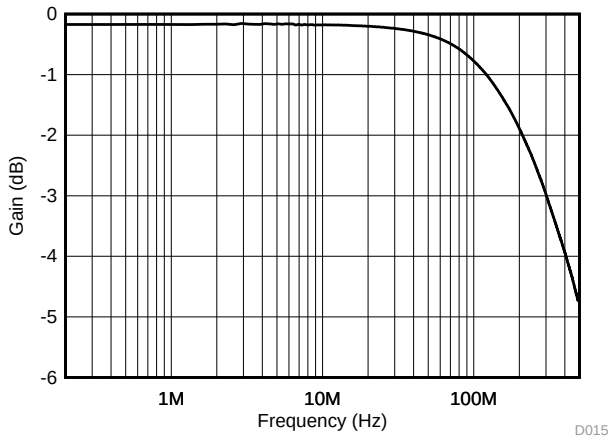
T_A = -40°C to +125°C

图 13. Output $T_{TRANSITION}$ vs Supply Voltage



T_A = -40°C to +125°C

图 14. Off-Isolation vs Frequency



T_A = -40°C to +125°C

图 15. On Response vs Frequency

8 Parameter Measurement Information

8.1 On-resistance

The on-resistance of a device is the ohmic resistance between the source (S) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in 图 16. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$:

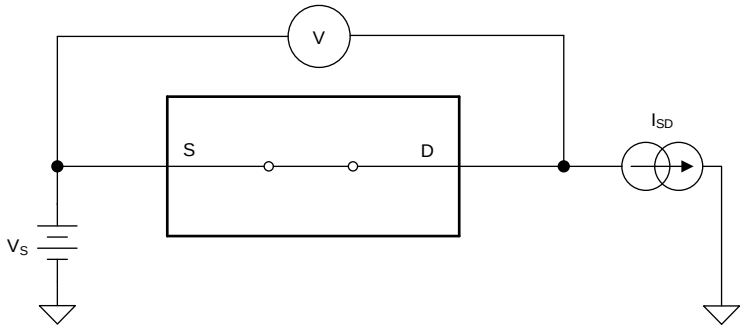


图 16. On-Resistance measurement setup

8.2 Off-leakage current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current
2. Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

The setup used to measure both off-leakage currents is shown in 图 17.

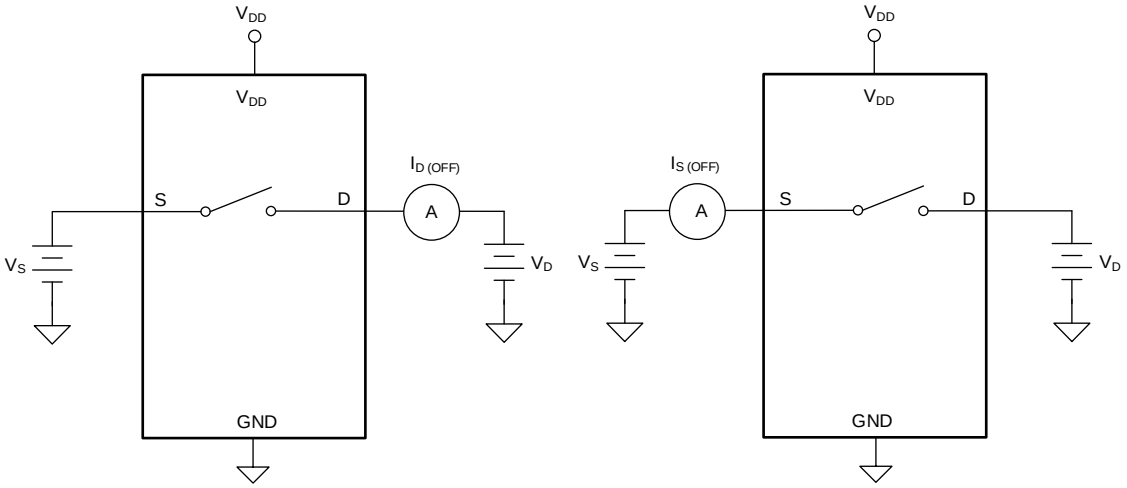


图 17. Off-leakage measurement setup

8.3 On-leakage current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. 图 18 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

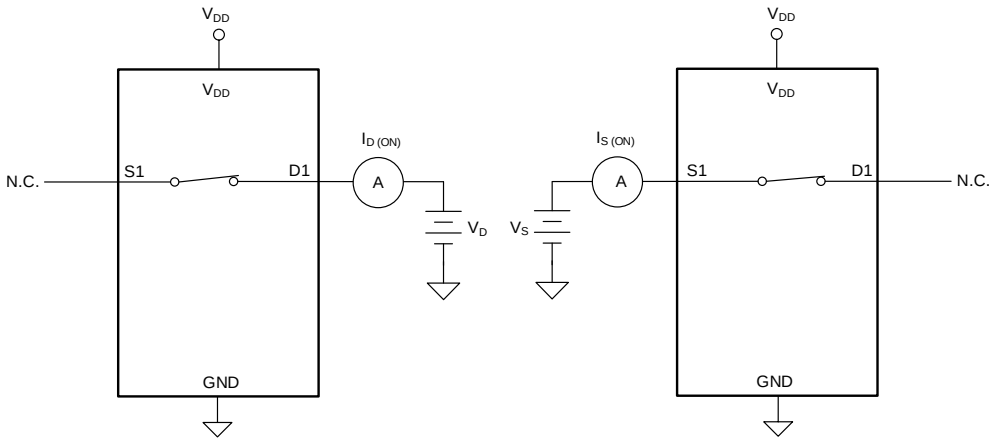


图 18. On-leakage measurement setup

8.4 Transition time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the address signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 图 19 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

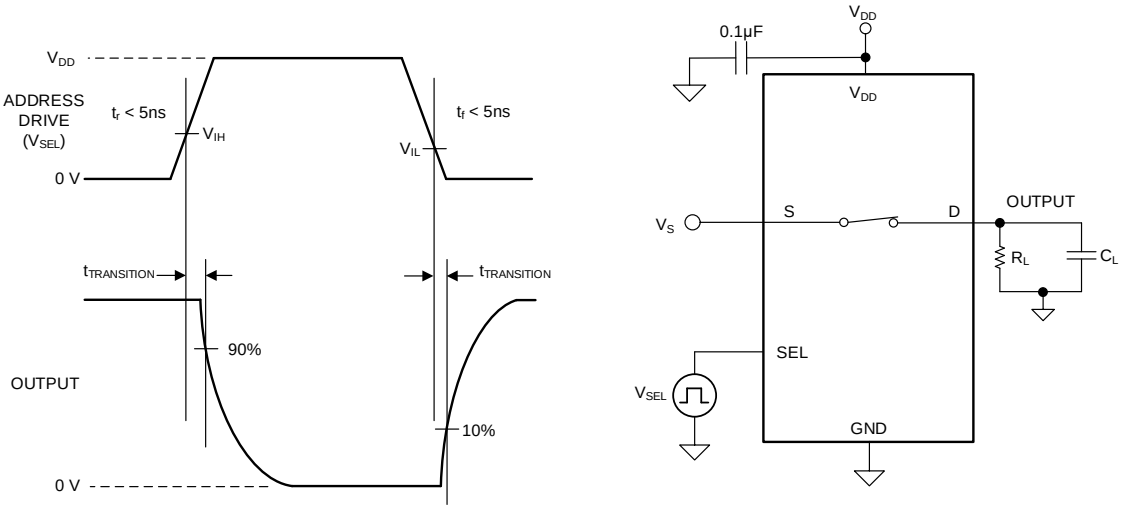


图 19. Transition-time measurement setup

8.5 Charge injection

The TMUX110x devices have a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. 图 20 shows the setup used to measure charge injection from source (S) to drain (D).

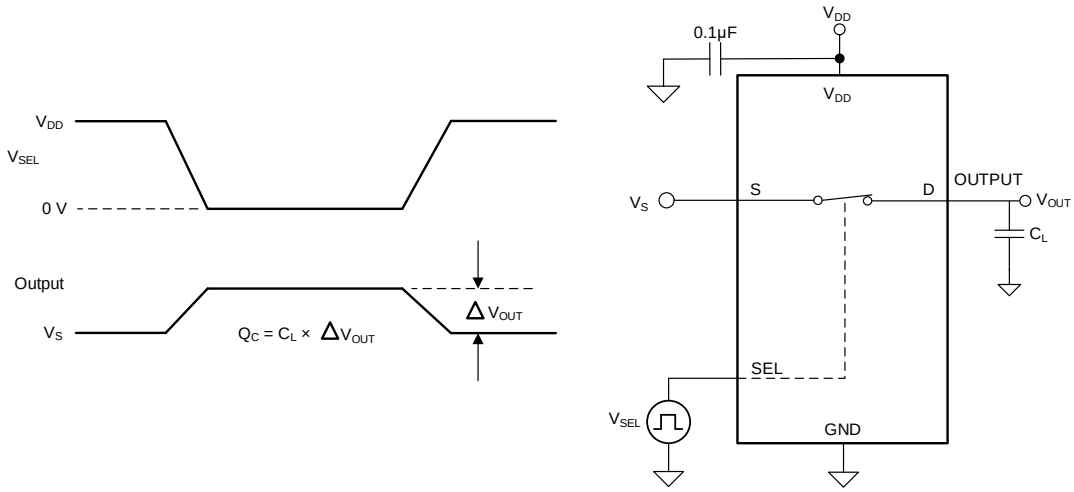


图 20. Charge-injection measurement setup

8.6 Off isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (S) of an off-channel. The characteristic impedance, Z_0, for the measurement is 50 Ω. 图 21 shows the setup used to measure off isolation. Use off isolation equation to compute off isolation.

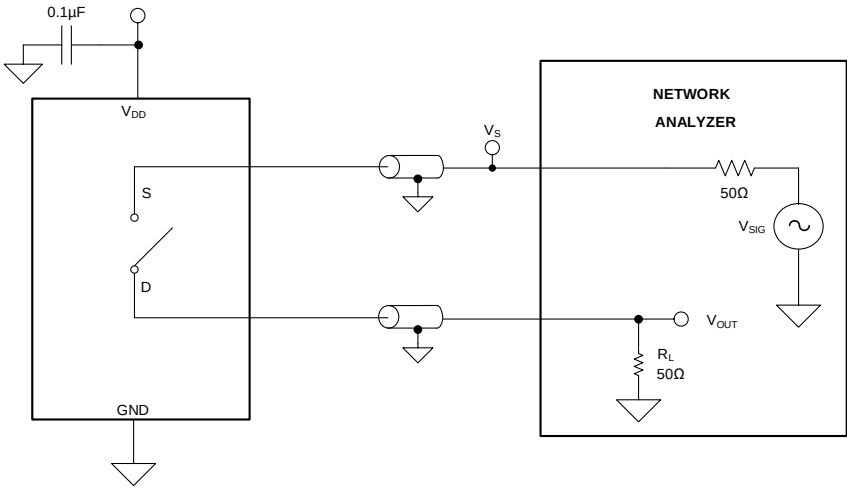


图 21. Off isolation measurement setup

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (1)$$

8.7 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (S) of an on-channel, and the output is measured at the drain pin (D) of the device. The characteristic impedance, Z_0, for the measurement is 50 Ω. 图 22 shows the setup used to measure bandwidth.

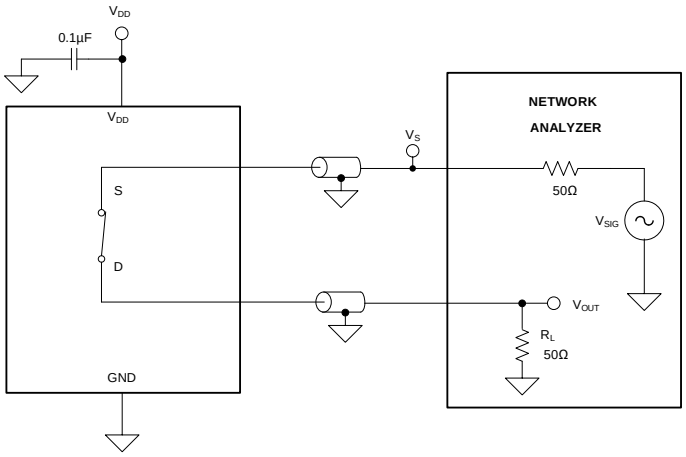


图 22. Bandwidth measurement setup

9 Detailed Description

9.1 Overview

The TMUX1101 and TMUX1102 are 1:1 (SPST) switches. The TMUX110x devices have a controllable single-pole, single-throw switch that is turned on or off based on the state of the select pin. The switch of the TMUX1101 is turned on with a Logic 1 on the select pin, while a Logic 0 is required to turn on switch in the TMUX1102. 图 23 shows the functional block diagram for the TMUX110x devices.

9.2 Functional Block Diagram

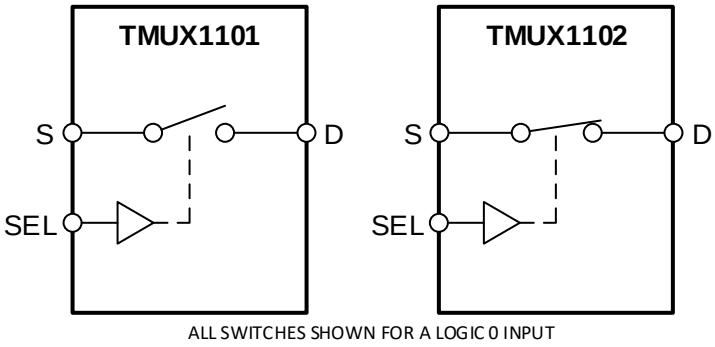


图 23. TMUX110x Functional Block Diagram

9.3 Feature Description

9.3.1 Bidirectional operation

The TMUX110x conducts equally well from source (S) to drain (D) or from drain (D) to source (S). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

9.3.2 Rail to rail operation

The valid signal path input/output voltage for TMUX110x ranges from GND to V_{DD}.

9.3.3 1.8 V Logic compatible inputs

The TMUX110x devices have 1.8-V logic compatible control for all logic control inputs. The logic input thresholds scale with supply but still provide 1.8-V logic control when operating at 5.5 V supply voltage. 1.8-V logic level inputs allows the TMUX110x devices to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. The current consumption of the TMUX110x devices increase when using 1.8V logic with higher supply voltage as shown in 图 10. For more information on 1.8 V logic implementations refer to *Simplifying Design with 1.8 V logic Muxes and Switches*.

9.3.4 Fail-safe logic

The TMUX110x supports Fail-Safe Logic on the control input pin (SEL) allowing for operation up to 5.5 V, regardless of the state of the supply pin. This feature allows voltages on the control pin to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pin. For example, the Fail-Safe Logic feature allows the select pin of the TMUX110x devices to be ramped to 5.5 V while V_{DD} = 0 V. Additionally, the feature enables operation of the TMUX110x with V_{DD} = 1.2 V while allowing the select pin to interface with a logic level of another device up to 5.5 V.

Feature Description (接下页)

9.3.5 Ultra-low Leakage Current

The TMUX110x devices provide extremely low on-leakage and off-leakage currents. The TMUX110x devices are capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultra-low leakage currents. 图 24 shows typical leakage currents of the TMUX110x devices versus temperature at V_{DD} = 5V.

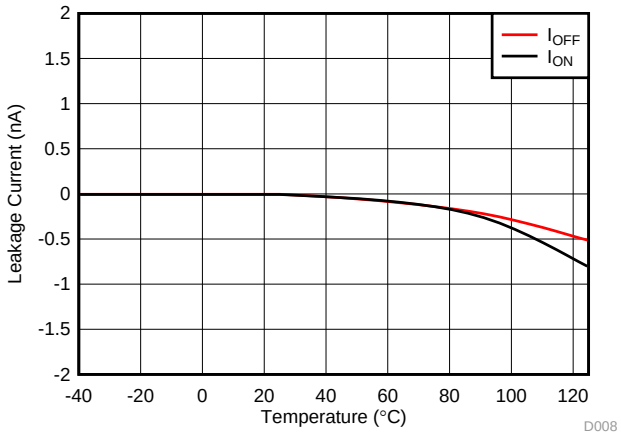


图 24. Leakage Current vs Temperature

9.3.6 Ultra-low Charge Injection

The TMUX110x devices have a transmission gate topology, as shown in 图 25. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

The TMUX110x devices have special charge-injection cancellation circuitry that reduces the source-to-drain charge injection to -1.5 pC at V_S = 1 V as shown in 图 26.

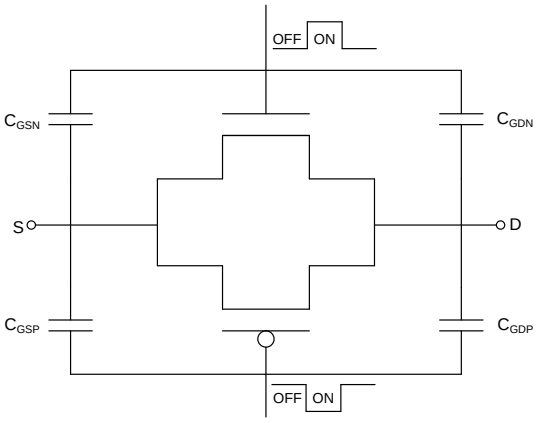


图 25. Transmission Gate Topology

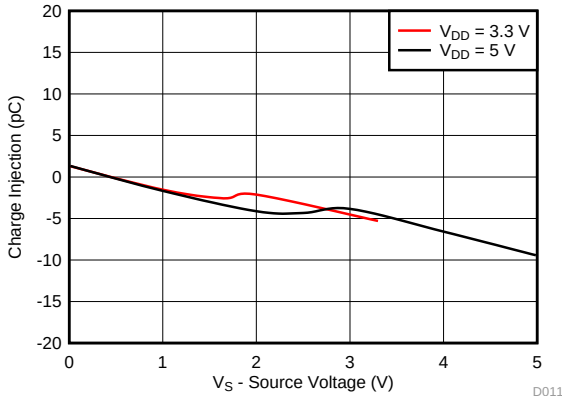


图 26. Charge Injection vs Source Voltage

9.4 Device Functional Modes

The TMUX110x devices have a controllable single-pole, single-throw switch that is turned on or turned off based on the state of the corresponding select pin. The control pin can be as high as 5.5 V.

The TMUX110x devices can be operated without any external components except for the supply decoupling capacitors. Unused logic control pins should be tied to GND or V_{DD} in order to ensure the device does not consume additional current as highlighted in *Implications of Slow or Floating CMOS Inputs*. Unused signal path inputs (Sx or Dx) should be connection to GND.

9.4.1 Truth Tables

表 1 and 表 2 show the truth tables for the TMUX1101 and TMUX1102 respectively.

表 1. TMUX1101 Truth table

SEL	SWITCH STATE
0	OFF (HI-Z)
1	ON

表 2. TMUX1102 Truth table

SEL	SWITCH STATE
0	ON
1	OFF (HI-Z)

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TMUX11xx family offers ulta-low input/output leakage currents and low charge injection. These devices operate up to 5.5 V, and offer true rail-to-rail input and output of both analog and digital signals. The TMUX110x have a low on-capacitance which allows faster settling time when multiplexing inputs in the time domain. These features make the TMUX11xx devices a family of precision, high-performance switches and multiplexers for low-voltage applications.

10.2 Typical Application - Sample-and-Hold Circuit

One useful application to take advantage of the TMUX1101 and TMUX1102's performance is the sample-and-hold circuit. A sample-and-hold circuit can be useful for an analog to digital converter (ADC) to sample a varying input voltage with improved reliability and stability. It can also be used to store the output samples from a single digital-to-analog converter (DAC) in a multi-output application. A simple sample-and-hold circuit can be realized using an analog switch such as the TMUX1101, and TMUX1102 analog switches. 图 27 shows a single channel sample-and hold circuit using either of the TMUX110x devices.

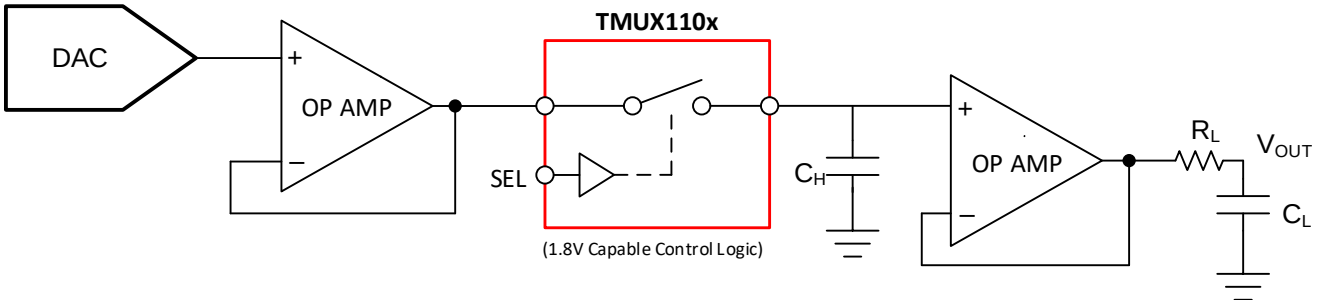


图 27. Single Channel Sample-and-Hold Circuit Example

An optional op amp is used before the switch since driving large capacitive loads is a typical limitation of buffered DACs. The additional buffer stage is included following the DAC to prevent potential stability problems from driving a large capacitive load.

Ideally, the switch delivers only the input signals to the holding capacitors. However, when the switch is toggled, some amount of charge is transferred to the switch output in the form of charge injection, resulting in a pedestal sampling error. The TMUX1101 and TMUX1102 switches have excellent charge injection performance of only -1.5 pC, making them ideal choices for this implementation to minimize sampling error. The pedestal error voltage is indirectly related to the size of the capacitance on the output, for better precision a larger capacitor is required due to charge injection.

Typical Application - Sample-and-Hold Circuit（接下页）

10.2.1 Design Requirements

The purpose of this precision design is to implement an optimized single channel sample-and-hold circuit using a precision 1:1 (SPST) CMOS switch. The sample-and-hold circuit needs to be capable of supporting high accuracy with minimized pedestal error and fast settling time.

10.2.2 Detailed Design Procedure

The TMUX1101 or TMUX1102 switch is used in conjunction with the voltage holding capacitors (C_H) to implement the sample-and-hold circuit. The basic operation is:

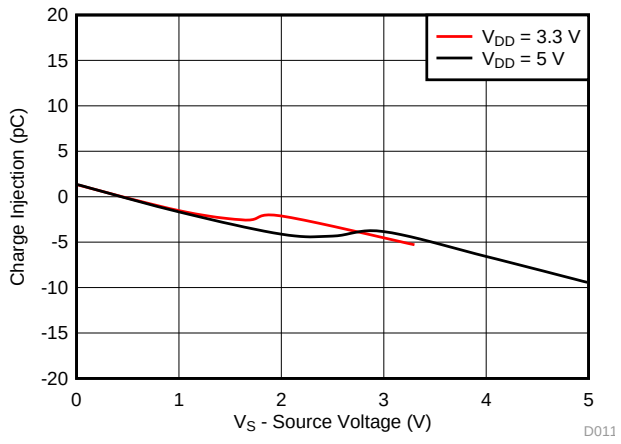
1. When the switch is closed, it samples the input voltage and charges the holding capacitors (C_H) to the input voltage values.
2. When the switch is open, the holding capacitors (C_H) holds its previous value, maintaining stable voltage at the amplifier output (V_{OUT}).

Due to switch and capacitor leakage current, as well as amplifier bias current, the voltage on the hold capacitors droops with time. The TMUX1101 and TMUX1102 minimize the droops due to its ultra-low leakage performance. At 25°C, the TMUX1101 and TMUX1102 have extremely low leakage current of 3pA typical.

Refer to *Sample & Hold Glitch Reduction for Precision Outputs Reference Design* for more information on sample-and-hold circuits.

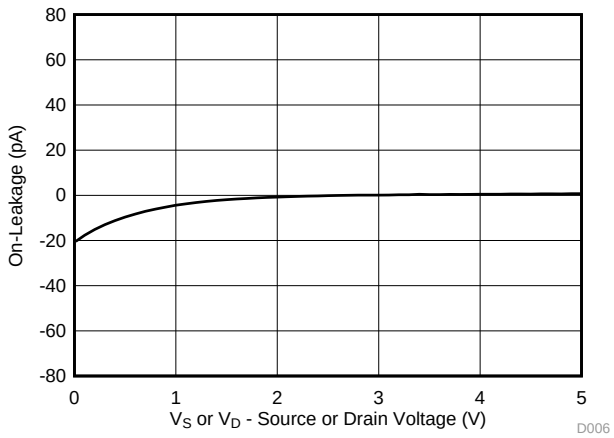
10.2.3 Application Curve

TMUX1101 and TMUX1102 have excellent charge injection performance and ultra-low leakage current, making them ideal choices to minimize sampling error for the sample-and-hold application. The charge injection and leakage performance are shown in 图 28 and 图 29 respectively.



T_A = –40°C to +125°C

图 28. Charge Injection vs Source Voltage



V_{DD} = 5 V

图 29. On-Leakage vs Source or Drain Voltage

10.3 Typical Application - Switched Gain Amplifier

Switches and multiplexers are commonly used in the feedback path of amplifier circuits to provide configurable gain control. By using various resistor values on the switch path, the TMUX110x allows the system to have multiple gain settings. An external resistor ensures the amplifier isn't operating in an open loop configuration. A transimpedance amplifier (TIA) for photodiode inputs is a common circuit that requires gain control using a switch to convert the output current of the photodiode into a voltage for the MCU or processor. The amount of light present during a photodiode measurement is dependent on the time of day and available light source. An external switch such as the TMUX110x can be utilized to increase the gain when a smaller photodiode current is present. The leakage current, capacitance, and charge injection performance of the TMUX110x are key specifications to evaluate when selecting a device for gain control. An example switched gain amplifier circuit is shown in 图 30.

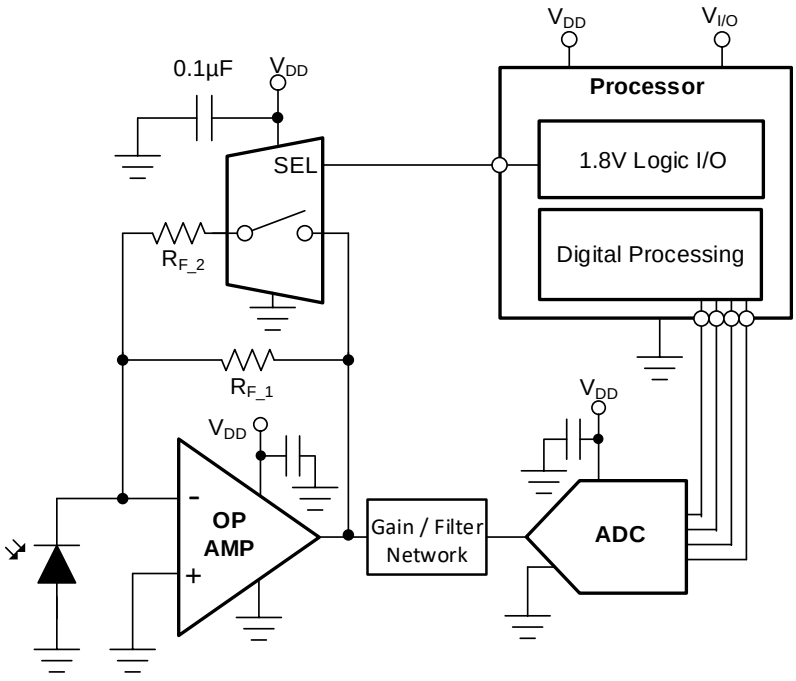


图 30. Configurable Gain Setting of a TIA circuit

10.3.1 Design Requirements

For this design example, use the parameters listed in 表 3.

表 3. Design parameters

PARAMETERS	VALUES
Supply (V_{DD})	3.3 V
Input / Output signal range	0 µA to 10 µA
Control logic thresholds	1.8 V compatible

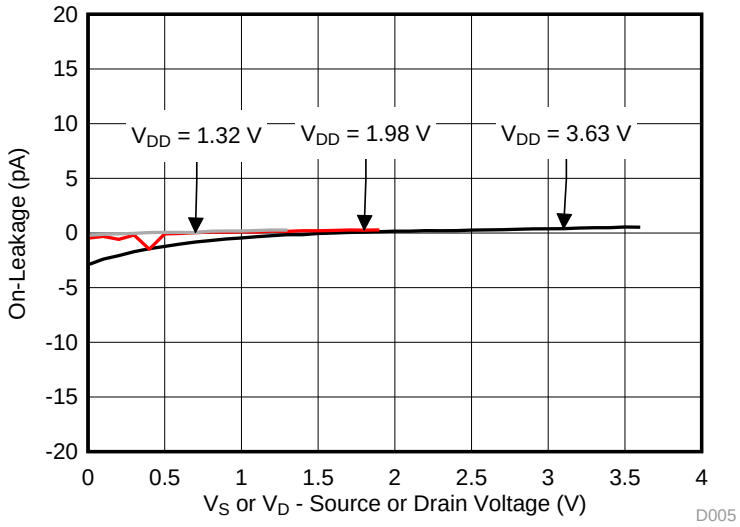
10.3.2 Detailed Design Procedure

The TMUX110x devices can be operated without any external components except for the supply decoupling capacitors. All inputs signals passing through the switch must fall within the recommended operating conditions of the TMUX110x, including signal range and continuous current. For this design example, with a supply of 3.3 V, the signals can range from 0 V to 3.3 V when the device is powered. The max continuous current can be 30 mA.

Photodiodes commonly have a current output that ranges from a few hundred picoamps to tens of microamps based on the amount of light being absorbed. The TMUX110x devices have a typical On-leakage current of less than 10 pA, which would lead to an accuracy well within 1% of a full scale 10 µA signal. The low ON and OFF capacitance of the TMUX110x improves system stability by minimizing the total capacitance on the output of the amplifier. Lower capacitance leads to less overshoot and ringing in the system, which can cause the amplifier circuit to become unstable if the phase margin is not at least 45°. Refer to *Improve Stability Issues with Low C_{ON} Multiplexers* for more information on calculating the phase margin vs. percent overshoot.

10.3.3 Application Curve

The TMUX110x devices are capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultra-low leakage currents.



T_A = 25°C

图 31. On-Leakage vs Source or Drain Voltage

11 Power Supply Recommendations

The TMUX110x devices operate across a wide supply range of 1.08 V to 5.5 V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{DD} supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μF to 10 μF from V_{DD} to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

12 Layout

12.1 Layout Guidelines

12.1.1 Layout Information

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners.图 32 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

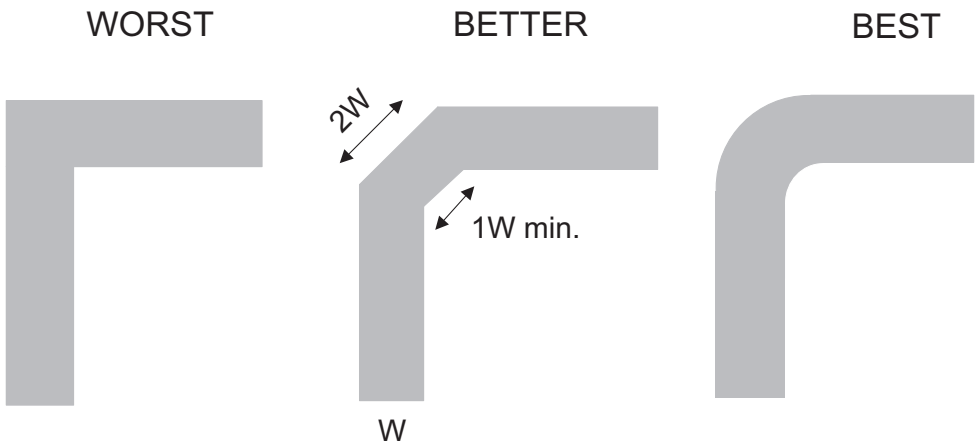


图 32. Trace example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Layout Guidelines (接下页)

图 33 illustrates an example of a PCB layout with the TMUX110x. Some key considerations are:

- Decouple the V_{DD} pin with a 0.1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

12.2 Layout Example

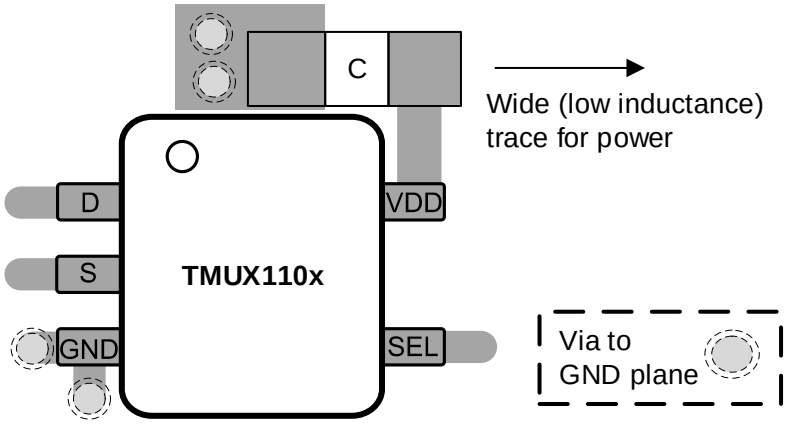


图 33. TMUX110x Layout example

13 器件和文档支持

13.1 文档支持

13.1.1 相关文档

德州仪器 (TI)，*《通过采样保持减少干扰实现精密输出的参考设计》*。

德州仪器 (TI)，*《真差分 4 x 2 多路复用器、模拟前端、同步采样 ADC 电路》*。

德州仪器 (TI)，*《使用低 CON 多路复用器改善稳定性问题》*。

德州仪器 (TI)，*《使用 1.8V 逻辑多路复用器和开关简化设计》*。

德州仪器 (TI)，*《利用关断保护信号开关消除电源排序》*。

德州仪器 (TI)，*《高电压模拟多路复用器的系统级保护》*。

13.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 **4.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
TMUX1101	单击此处	单击此处	单击此处	单击此处	单击此处
TMUX1102	单击此处	单击此处	单击此处	单击此处	单击此处

13.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX1101DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1W1F	Samples
TMUX1101DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	101	Samples
TMUX1102DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1W3F	Samples
TMUX1102DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	102	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

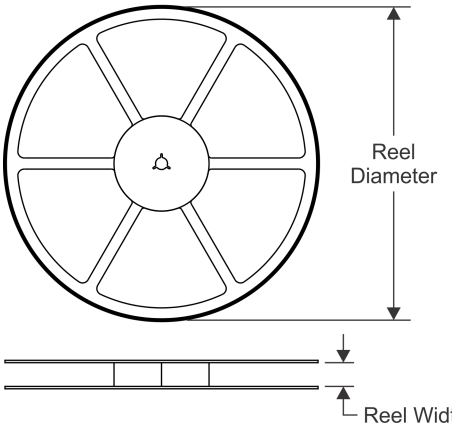
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

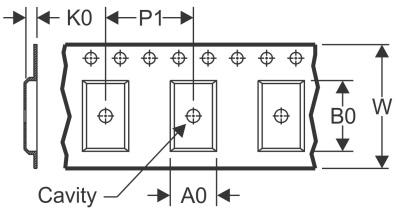
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

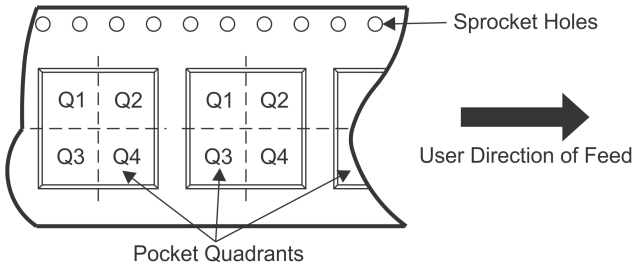


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

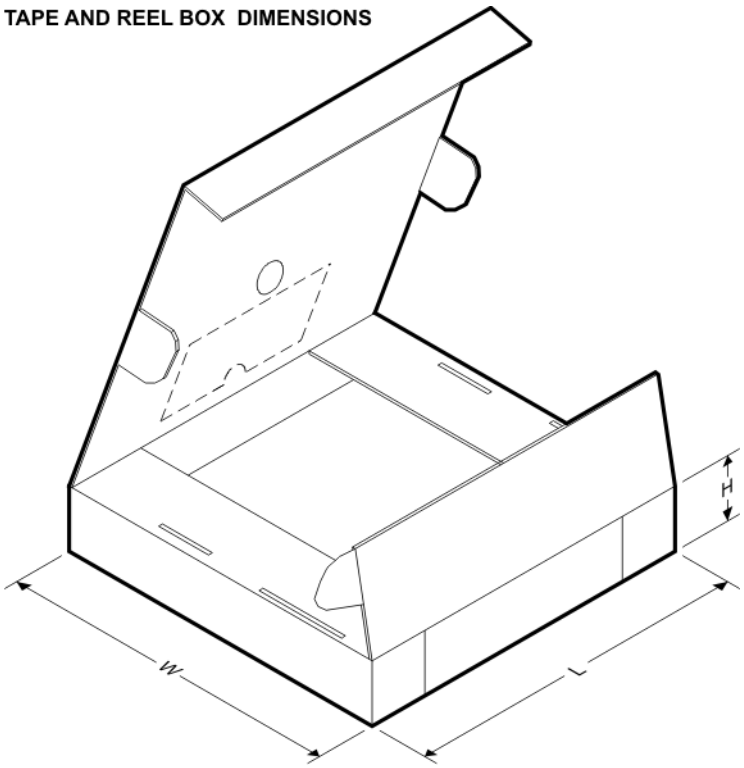
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX1101DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TMUX1101DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TMUX1102DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TMUX1102DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

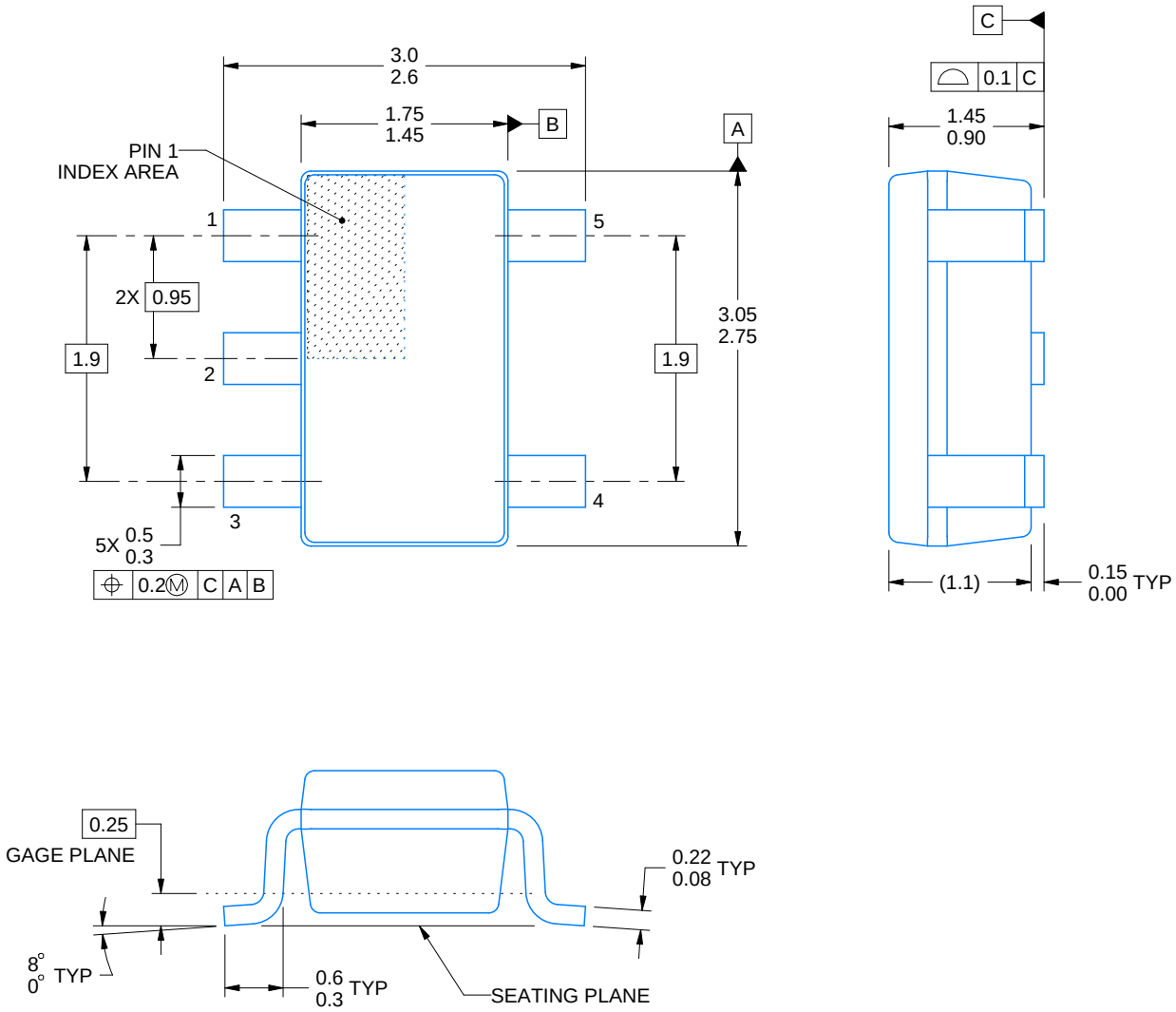
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX1101DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TMUX1101DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TMUX1102DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TMUX1102DCKR	SC70	DCK	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

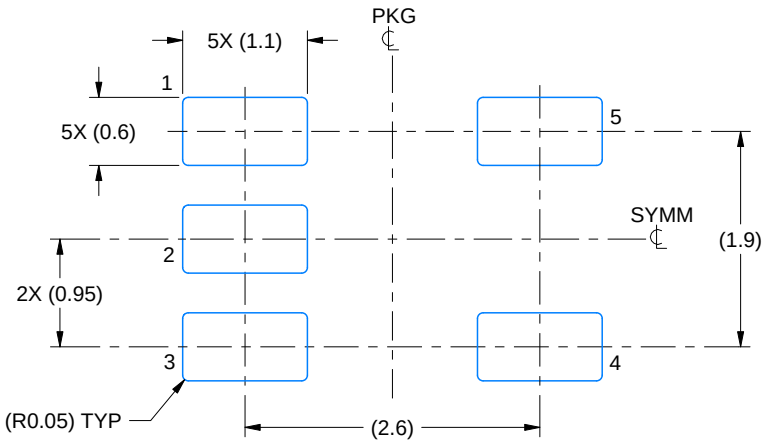
SMALL OUTLINE TRANSISTOR



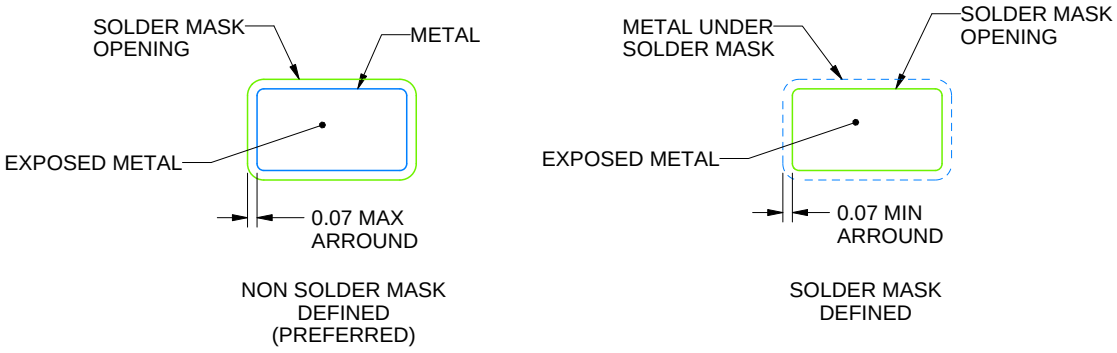
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

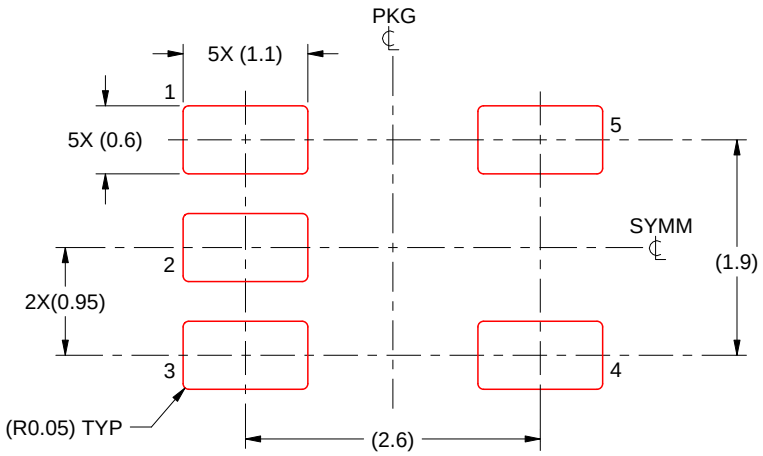


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



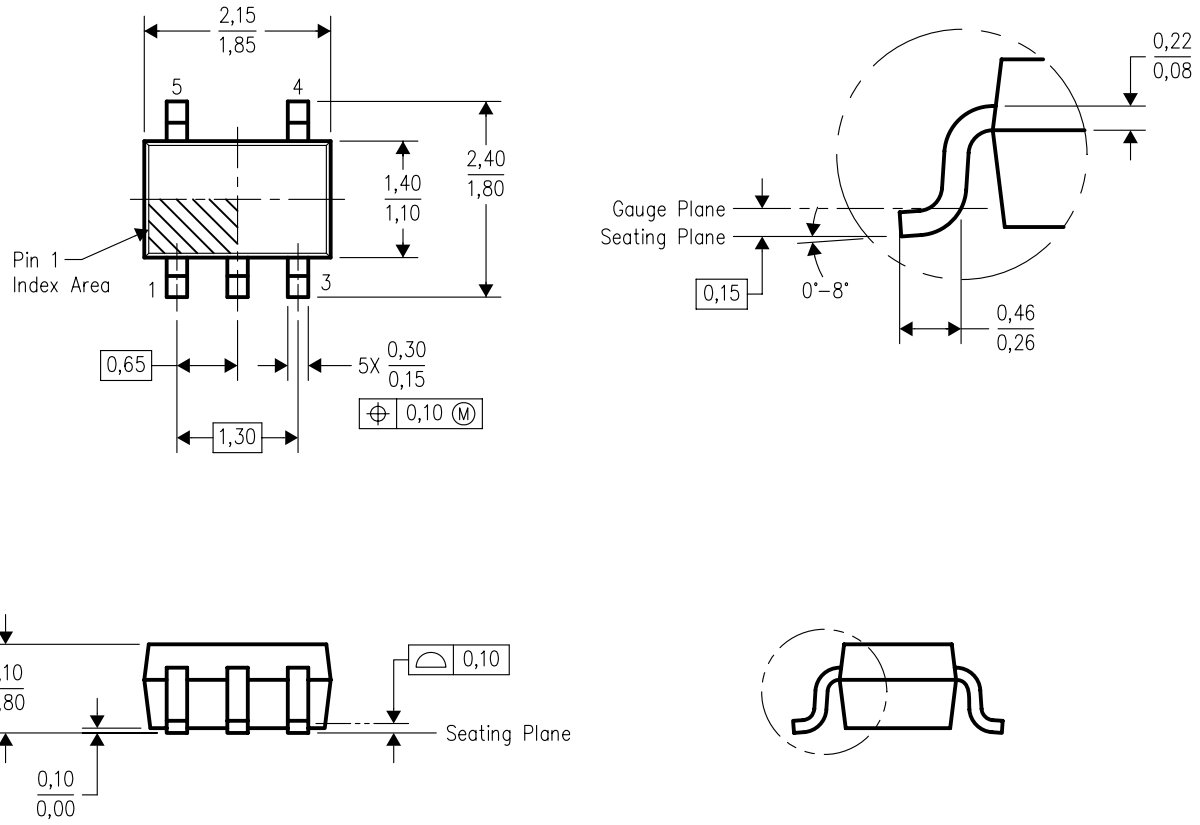
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

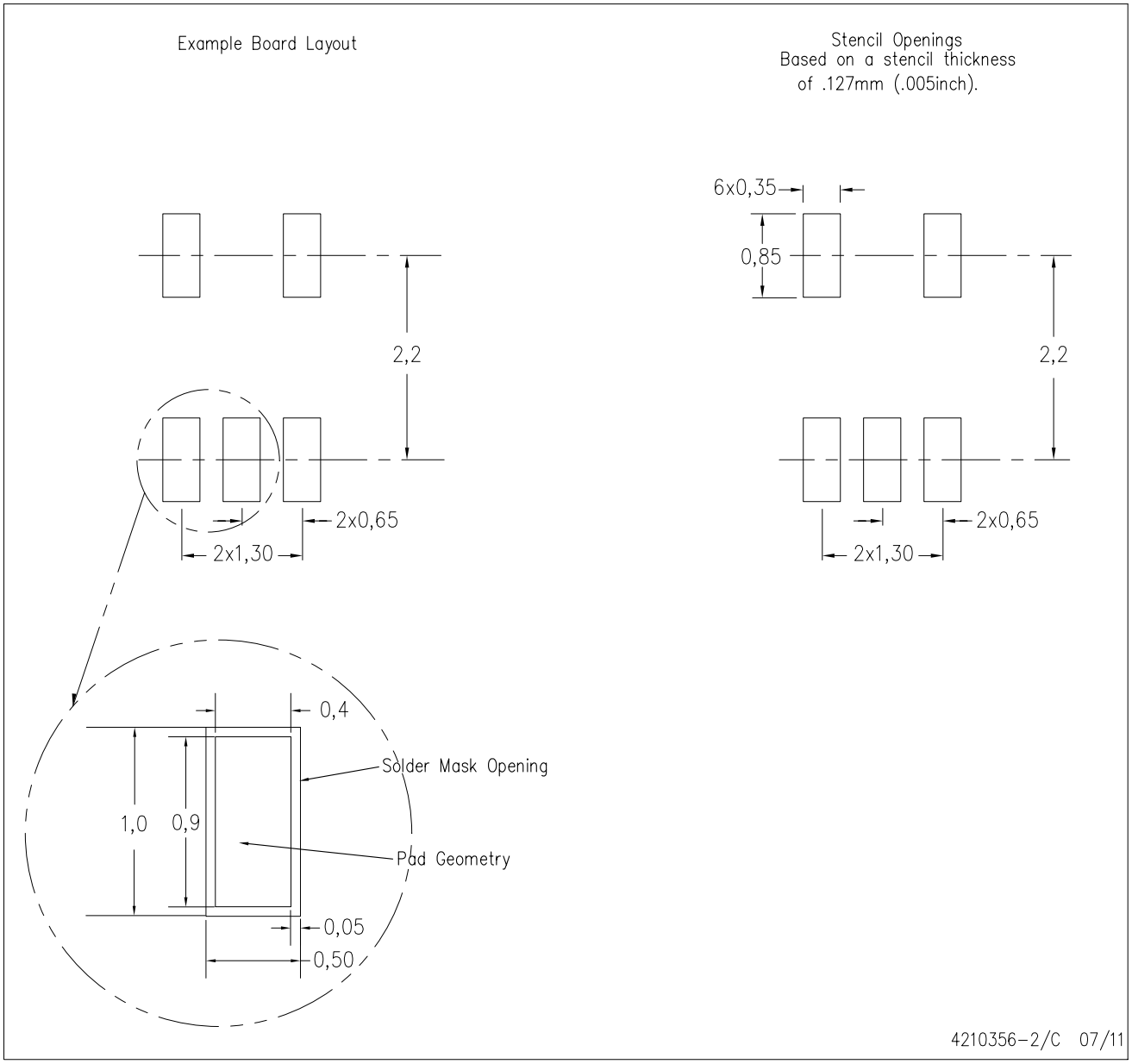
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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