LM3710/LM3711 Microprocessor Supervisory Circuits with Power Fail Input, Low Line Output, Manual Reset and Watchdog Timer

Check for Samples: LM3710, LM3711

FEATURES

- **Standard Reset Threshold Voltage: 3.08V**
- **Custom Reset Threshold Voltages: For other voltages between 2.2V and 5.0V in 10mV increments, contact TI**
- **No External Components Required**
- **Manual-Reset Input**
- **$\overline{\text{RESET}}$ (LM3710) or RESET (LM3711) Outputs**
- **Precision Supply Voltage Monitor**
- **Factory Programmable Reset and Watchdog Timeout Delays**
- **Separate Power Fail Comparator**
- **Available in DSBGA Package for Minimum Footprint**
- **±0.5% Reset Threshold Accuracy at Room Temperature**
- **±2% Reset Threshold Accuracy Over Temperature Extremes**
- **Reset Assertion Down to 1V V_{CC} ($\overline{\text{RESET}}$ Option Only)**
- **28 µA V_{CC} Supply Current**

APPLICATIONS

- **Embedded Controllers and Processors**
- **Intelligent Instruments**
- **Automotive Systems**
- **Critical µP Power Monitoring**

DESCRIPTION

The LM3710/LM3711 series of microprocessor supervisory circuits provide the maximum flexibility for monitoring power supplies and battery controlled functions in systems without backup batteries. The LM3710/LM3711 series are available in VSSOP-10 and 9-bump DSBGA packages.

Built-in features include the following:

Reset: Reset is asserted during power-up, power-down, and brownout conditions. $\overline{\text{RESET}}$ is ensured down to V_{CC} of 1.0V.

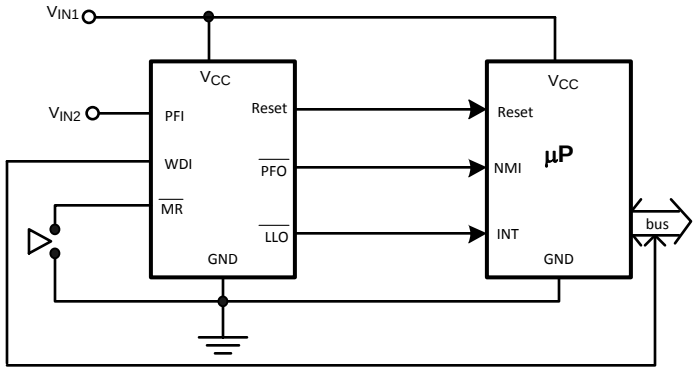
Manual Reset Input: An input that asserts reset when pulled low.

Power-Fail Input: A 1.225V threshold detector for power fail warning, or to monitor a power supply other than V_{CC}.

Low Line Output: This early power failure warning indicator goes low when the supply voltage drops to a value which is 2% higher than the reset threshold voltage.

Watchdog Timer: The WDI (Watchdog Input) monitors one of the µP's output lines for activity. If no output transition occurs during the watchdog timeout period, reset is activated.

Typical Application



Connection Diagram

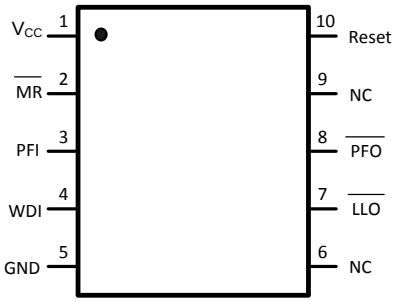


Figure 1. VSSOP-10

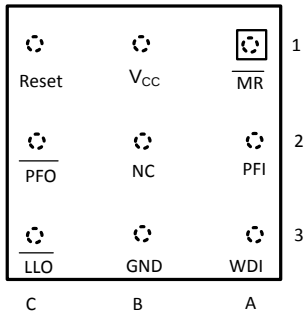


Figure 2. Top View
(looking from the coating side)
DSBGA 9 Bump Package

PIN DESCRIPTIONS

Pin No.		Name	Function
DSBGA	VSSOP		
A1	2	$\overline{MR}$	Manual-Reset input. When $\overline{MR}$ is less than V_{MRT} (Manual Reset Threshold) $\overline{RESET}$/RESET is engaged.
B1	1	V_{CC}	Power Supply input.
C1	10	$\overline{RESET}$	Reset Logic Output. Pulses low for t_{RP} (Reset Timeout Period) when triggered, and stays low whenever V_{CC} is below the reset threshold or when $\overline{MR}$ is below V_{MRT}. It remains low for t_{RP} after either V_{CC} rises above the reset threshold, or after $\overline{MR}$ input rises above V_{MRT} (LM3710 only).
		RESET	Reset Logic Output. RESET is the inverse of $\overline{RESET}$ (LM3711 only).
C2	8	$\overline{PFO}$	Power-Fail Logic Output. When PFI is below V_{PFT}, $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high.
C3	7	$\overline{LLO}$	Low-Line Logic Output. Early Power-Fail warning output. Low when V_{CC} falls below V_{LLOT} (Low-Line Output Threshold). This output can be used to generate an NMI (Non-Maskable Interrupt) to provide an early warning of imminent power-failure.
B3	5	GND	Ground reference for all signals.
A3	4	WDI	Watchdog Input Transition Monitor: If no transition activity occurs for a period exceeding t_{WD} (Watchdog Timeout Period), reset is engaged.
A2	3	PFI	Power-Fail Comparator Input. When PFI is less than V_{PFT} (Power-Fail Reset Threshold), the $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high.
B2	6, 9	NC	No Connect. Test input used at factory only. Leave floating.

Block Diagram

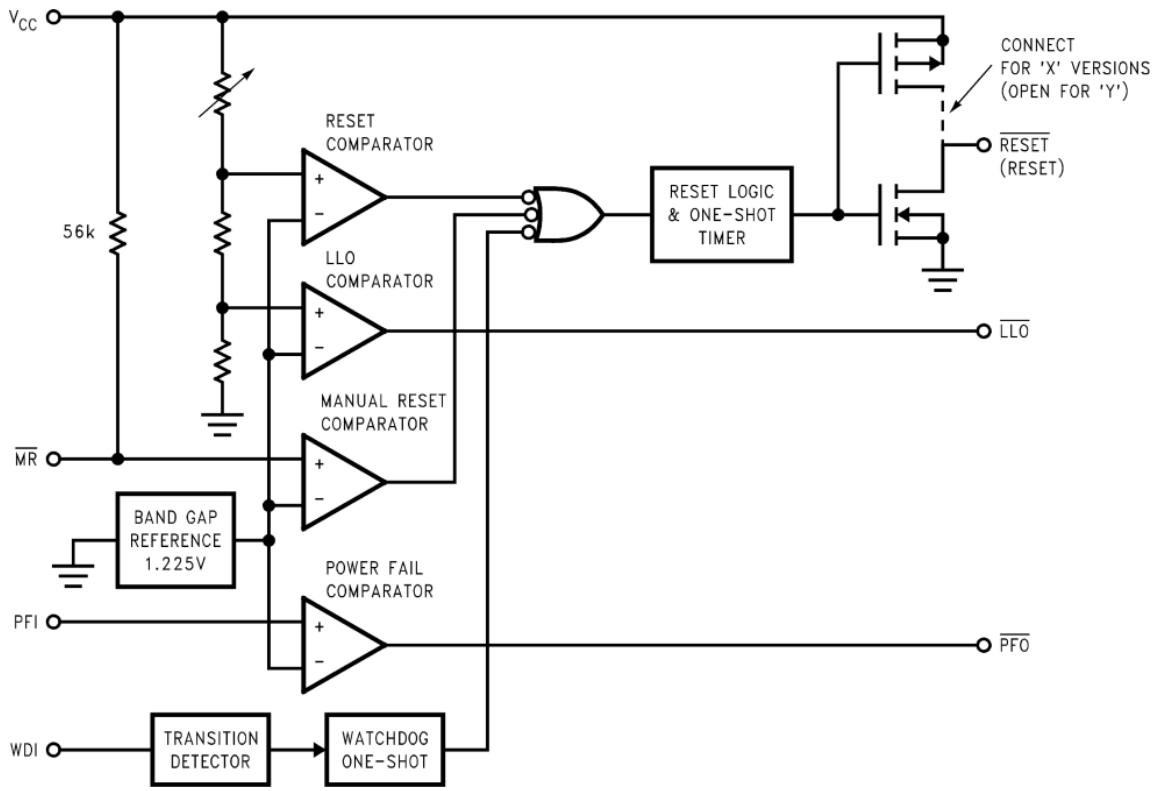


Table Of Functions

Part Number	Active Low Reset	Active High Reset	Output (X = totem-pole) (Y = open-drain)	Reset Timeout Period	Watchdog Timeout Period	Manual Reset	Power Fail Comparator	Low Line Output
LM3710	x		X, Y(1)	Customized	Customized	x	x	x
LM3711		x	X	Customized	Customized	x	x	x

(1) Available upon request. Contact TI.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage (V_{CC})	−0.3V to 6.0V
All Other Inputs	−0.3V to V_{CC} + 0.3V
ESD Ratings [3] Human Body Model Machine Model	 1.5kV 150V
Power Dissipation	[4]

(1) **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. **Operating Ratings** indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed conditions.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

(3) The Human Body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

(4) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J(MAX)$, the junction-to-ambient thermal resistance, θ_{J-A}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperture is calculated using:

$$P(MAX) = \frac{T_J(MAX) - T_A}{\theta_{J-A}}$$

Where the value of θ_{J-A} for the VSSOP-10 package is 195°C/W in a typical PC board mounting and the DSBGA package is 220°C/W.

Operating Ratings[1]

Temperature Range	$-40°C \le T_J \le 85°C$

(1) **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. **Operating Ratings** indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed conditions.

LM3710/LM3711 Series Electrical Characteristics

Limits in the standard typeface are for T_J = 25°C and limits in **boldface type** apply over full operating range. Unless otherwise specified: V_{CC} = +2.2V to 5.5V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
V_{CC}	Operating Voltage Range: V_{CC}	LM3710	**1.0**		**5.5**	V
		LM3711	**1.2**		**5.5**	
I_{CC}	V_{CC} Supply Current	All inputs = V_{CC}; all outputs floating		28	**50**	µA
RESET THRESHOLD						
V_{RST}	Reset Threshold	V_{CC} falling	−0.5 **−2**	V_{RST}	+0.5 **+2**	%
		V_{CC} falling: T_A = 0°C to 70°C	**−1.5**		**+1.5**	
V_{RSTH}	Reset Threshold Hysteresis			0.0032•V_{RST}		mV
t_{RP}	Reset Timeout Period	Reset Timeout Period = E, J, N, S Reset Timeout Period = F, K, P, T Reset Timeout Period = G, L, Q, U Reset Timeout Period = H, M, R, V	**1** **20** **140** **1120**	1.4 28 200 1600	**2** **40** **280** **2240**	ms
t_{RD}	$V_{CC}$to Reset Delay	V_{CC}falling at 1mV/µs		20		µs
RESET (LM3711)						
V_{OL}	RESET	V_{CC} > 2.25V, I_{SINK} = 900µA			**0.3**	V
		V_{CC} > 2.7V, I_{SINK} = 1.2mA			**0.3**	
		V_{CC} > 4.5V, I_{SINK} = 3.2mA			**0.4**	
V_{OH}	RESET	V_{CC} > 1.2V, I_{SOURCE} = 50µA	**0.8 V_{CC}**			V
		V_{CC} > 1.8V, I_{SOURCE} = 150µA	**0.8 V_{CC}**			
		V_{CC} > 2.25V, I_{SOURCE} = 300µA	**0.8 V_{CC}**			
		V_{CC} > 2.7V, I_{SOURCE} = 500µA	**0.8 V_{CC}**			
		V_{CC} > 4.5V, I_{SOURCE} = 800µA	**V_{CC} − 1.5V**			

LM3710/LM3711 Series Electrical Characteristics (continued)

Limits in the standard typeface are for T_J = 25°C and limits in **boldface type** apply over full operating range. Unless otherwise specified: V_{CC} = +2.2V to 5.5V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LKG}	Output Leakage Current	V_{RESET} = 5.5V			**1.0**	µA
$\overline{\text{RESET}}$ (LM3710)						
V_{OL}	$\overline{\text{RESET}}$	V_{CC} > 1.0V, I_{SINK} = 50µA			**0.3**	V
		V_{CC} > 1.2V, I_{SINK} = 100µA			**0.3**	
		V_{CC} > 2.25V, I_{SINK} = 900µA			**0.3**	
		V_{CC} > 2.7V, I_{SINK} = 1.2mA			**0.3**	
		V_{CC} > 4.5V, I_{SINK} = 3.2mA			**0.4**	
V_{OH}	$\overline{\text{RESET}}$	V_{CC} > 2.25V, I_{SOURCE} = 300µA	**0.8 V_{CC}**			
		V_{CC} > 2.7V, I_{SOURCE} = 500µA	**0.8 V_{CC}**			
		V_{CC} > 4.5V, I_{SOURCE} = 800µA	**V_{CC} − 1.5V**			
WDI						
WDI	Watchdog Input Current		**−1**		**+1**	µA
WDI_T	Watchdog Input Threshold		**0.2•V_{CC}**	1.225	**0.8•V_{CC}**	V
t_{WD}	Watchdog Timeout Period	Watchdog Timeout Period = E, F, G, H Watchdog Timeout Period = J, K, L, M Watchdog Timeout Period = N, P, Q, R Watchdog Timeout Period = S, T, U, V	**4.3** **71** **1120** **17900**	6.2 102 1600 25600	**9.3** **153** **2400** **38400**	ms
PFI/$\overline{\text{MR}}$						
V_{PFT}	PFI Input Threshold		**1.200**	1.225	**1.250**	V
V_{MRT}	$\overline{\text{MR}}$ Input Threshold	$\overline{\text{MR}}$, Low			**0.8**	V
		$\overline{\text{MR}}$, High	**2.0**			
V_{PFTH}/ V_{MRTH}	PFI/$\overline{\text{MR}}$ Threshold Hysteresis	PFI/$\overline{\text{MR}}$ falling: V_{CC} = $V_{RST\ MAX}$ to 5.5V		0.0032•V_{RST}		mV
I_{PFI}	Input Current (PFI only)		**−75**		**75**	nA
R_{MR}	$\overline{\text{MR}}$ Pull-up Resistance		**35**	56	**75**	kΩ
t_{MD}	$\overline{\text{MR}}$ to Reset Delay			12		µS
t_{MR}	$\overline{\text{MR}}$ Pulse Width		**25**			µS
$\overline{\text{PFO}}$, $\overline{\text{LLO}}$						
V_{OL}	$\overline{\text{PFO}}$, $\overline{\text{LLO}}$ Output Voltage	V_{CC} > 2.25V, I_{SINK} = 900µA			**0.3**	V
		V_{CC} > 2.7V, I_{SINK} = 1.2mA			**0.3**	
		V_{CC} > 4.5V, I_{SINK} = 3.2mA			**0.4**	
V_{OH}		V_{CC} > 2.25V, I_{SOURCE} = 300µA	**0.8 V_{CC}**			
		V_{CC} > 2.7V, I_{SOURCE} = 500µA	**0.8 V_{CC}**			
		V_{CC} > 4.5V, I_{SOURCE} = 800µA	**V_{CC} − 1.5V**			
$\overline{\text{LLO}}$ OUTPUT						
V_{LLOT}	$\overline{\text{LLO}}$ Output Threshold ($V_{\overline{LLO}}$ − V_{RST}, V_{CC} falling)		**1.01•V_{RST}**	1.02•V_{RST}	**1.03•V_{RST}**	V
V_{LLOTH}	Low-Line Comparator Hysteresis			0.0032•V_{RST}		mV
t_{CD}	Low-Line Comparator Delay	V_{CC} falling at 1mV/µs		20		µs

Typical Performance Characteristics

Supply Current vs Supply Voltage

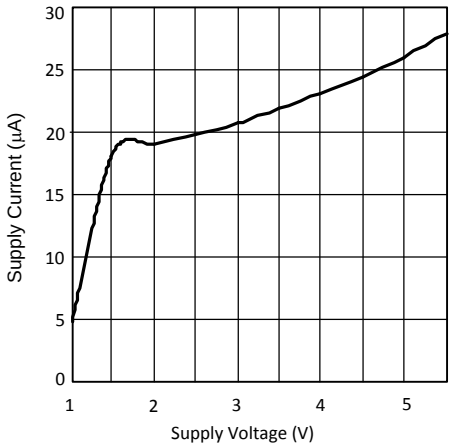


Figure 3.

3.3V Supply Current vs Temperature

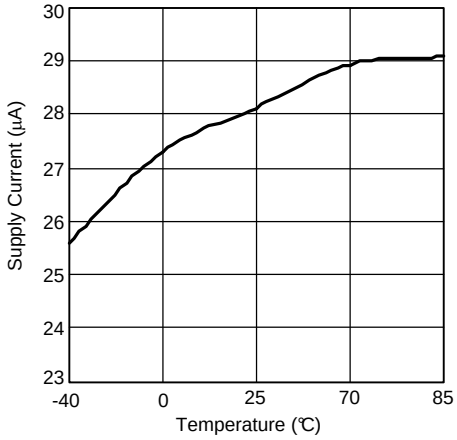


Figure 4.

Normalized Reset Threshold Voltage vs Temperature

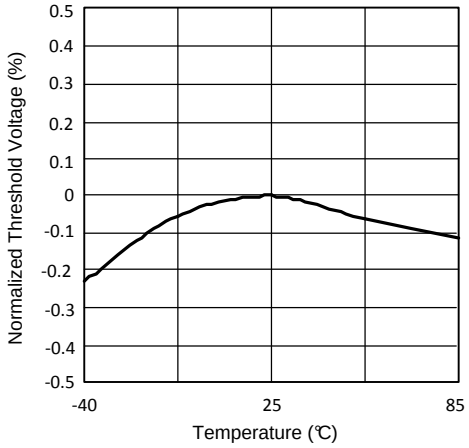


Figure 5.

Reset Timeout Period vs V_{CC}

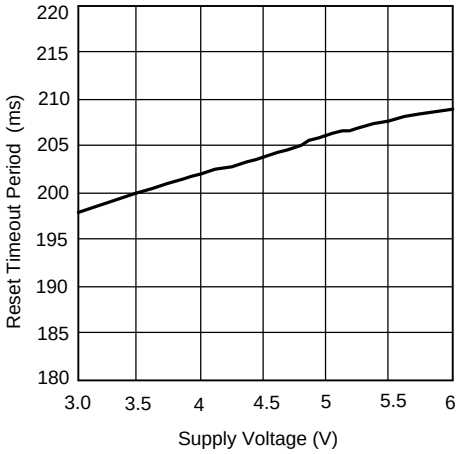


Figure 6.

Reset Timeout Period vs Temperature

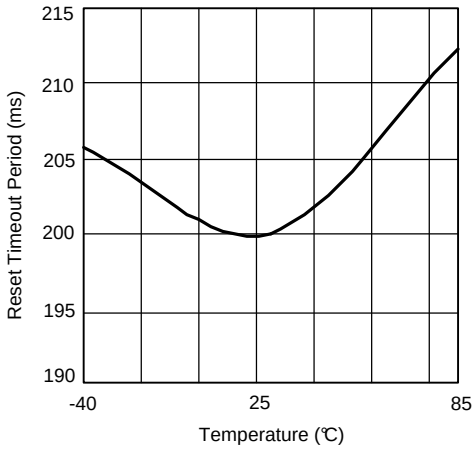


Figure 7.

Max. Transient Duration vs Reset Comparator Overdrive (V_{CC} = 3.3V)

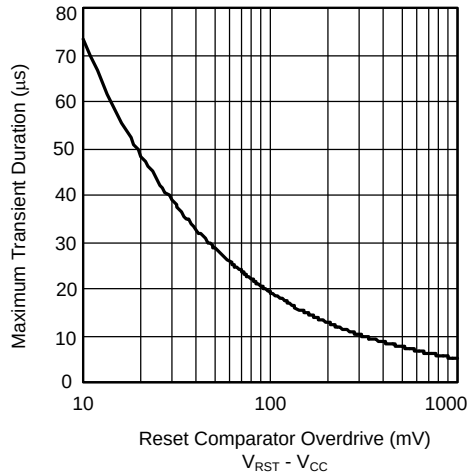


Figure 8.

Typical Performance Characteristics (continued)

Watchdog Timeout Period vs Temperature (t_{WD} programmed as 6.2ms)

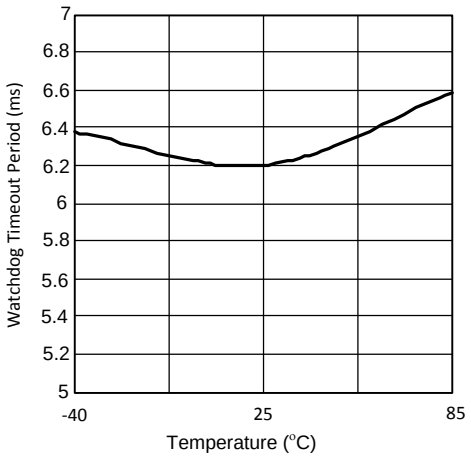


Figure 9.

Low-Line Comparator Propagation Delay vs Temperature

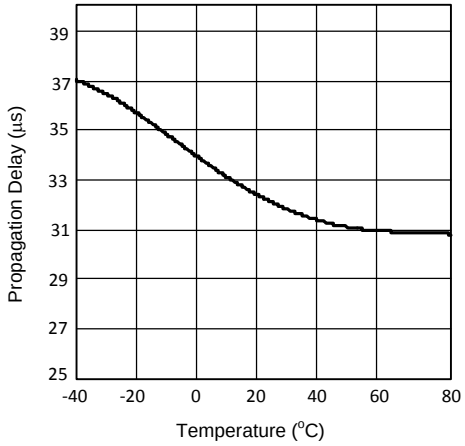


Figure 10.

CIRCUIT INFORMATION

RESET OUTPUT

The Reset input of a µP initializes the device into a known state. The LM3710/LM3711 microprocessor supervisory circuits assert a forced reset output to prevent code execution errors during power-up, power-down, and brownout conditions.

$\overline{\text{RESET}}$ is ensured valid for V_{CC} > 1V. Once V_{CC} exceeds the reset threshold, an internal timer maintains the output for the reset timeout period. After this interval, reset goes high. The LM3710 offers an active-low $\overline{\text{RESET}}$; The LM3711 offers an active-high RESET.

Any time V_{CC} drops below the reset threshold (such as during a brownout), the reset activates. When V_{CC} again rises above the reset threshold, the internal timer starts. Reset holds until V_{CC} exceeds the reset threshold for longer than the reset timeout period. After this time, reset releases.

The Manual Reset input ($\overline{\text{MR}}$) will initiate a forced reset also. See the MANUAL RESET INPUT ($\overline{\text{MR}}$) section.

RESET THRESHOLD

The LM3710/LM3711 family is available with a reset voltage of 3.08V. Other reset thresholds in the 2.20V to 5.0V range, in steps of 10 mV, are available; contact Texas Instruments for details.

MANUAL RESET INPUT ($\overline{\text{MR}}$)

Many µP-based products require a manual reset capability, allowing the operator to initiate a reset. The $\overline{\text{MR}}$ input is fully debounced and provides an internal 56 kΩ pull-up. When the $\overline{\text{MR}}$ input is pulled below V_{MRT} (1.225V) for more than 25 µs, reset is asserted after a typical delay of 12 µs. Reset remains active as long as $\overline{\text{MR}}$ is held low, and releases after the reset timeout period expires after $\overline{\text{MR}}$ rises above V_{MRT}. Use $\overline{\text{MR}}$ with digital logic to assert or to daisy chain supervisory circuits. It may be used as another low-line comparator by adding a buffer.

POWER-FAIL COMPARATOR (PFI/$\overline{\text{PFO}}$)

The PFI is compared to a 1.225V internal reference, V_{PFT}. If PFI is less than V_{PFT}, the Power Fail Output $\overline{\text{PFO}}$ drops low. The power-fail comparator signals a falling power supply, and is driven typically by an external voltage divider that senses either the unregulated supply or another system supply voltage. The voltage divider generally is chosen so the voltage at PFI drops below V_{PFT} several milliseconds before the main supply voltage drops below the reset threshold, providing advanced warning of a brownout.

The voltage threshold is set by R_1 and R_2 and is calculated as follows:

$$V_{PFT} = \left(\frac{R1 + R2}{R2}\right) \times 1.225V \quad (1)$$

Note this comparator is completely separate from the rest of the circuitry, and may be employed for other functions as needed.

LOW-LINE OUTPUT ($\overline{\text{LLO}}$)

The low-line output comparator is typically used to provide a non-maskable interrupt to a µP when V_{CC} begins falling. $\overline{\text{LLO}}$ monitors V_{CC} and goes low when V_{CC} falls below V_{LLOT} (typically 1.02 • V_{RST}) with hysteresis of 0.0032 • V_{RST}.

WATCHDOG TIMER INPUT (WDI)

The watchdog timer input monitors one of the microprocessor's output lines for activity. Each time a transition occurs on this monitored line, the watchdog counter is reset. However, if no transition occurs and the timeout period is reached, the LM3710/LM3711 assumes that the microprocessor has locked up and the reset output is activated.

WDI is a high impedance input.

SPECIAL PRECAUTIONS FOR THE DSBGA PACKAGE

As with most integrated circuits, the LM3710 and LM3711 are sensitive to exposure from visible and infrared (IR) light radiation. Unlike a plastic encapsulated IC, the DSBGA package has very limited shielding from light, and some sensitivity to light reflected from the surface of the PC board or long wavelength IR entering the die from the side may be experienced. This light could have an unpredictable affect on the electrical performance of the IC. Care should be taken to shield the device from direct exposure to bright visible or IR light during operation.

DSBGA MOUNTING

The DSBGA package requires specific mounting techniques which are detailed in TI Application Note AN-1112 (SNVA009). Referring to the section ***Surface Mount Assembly Considerations***, it should be noted that the pad style which must be used with the 9-pin package is the NSMD (non-solder mask defined) type.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

Timing Diagrams

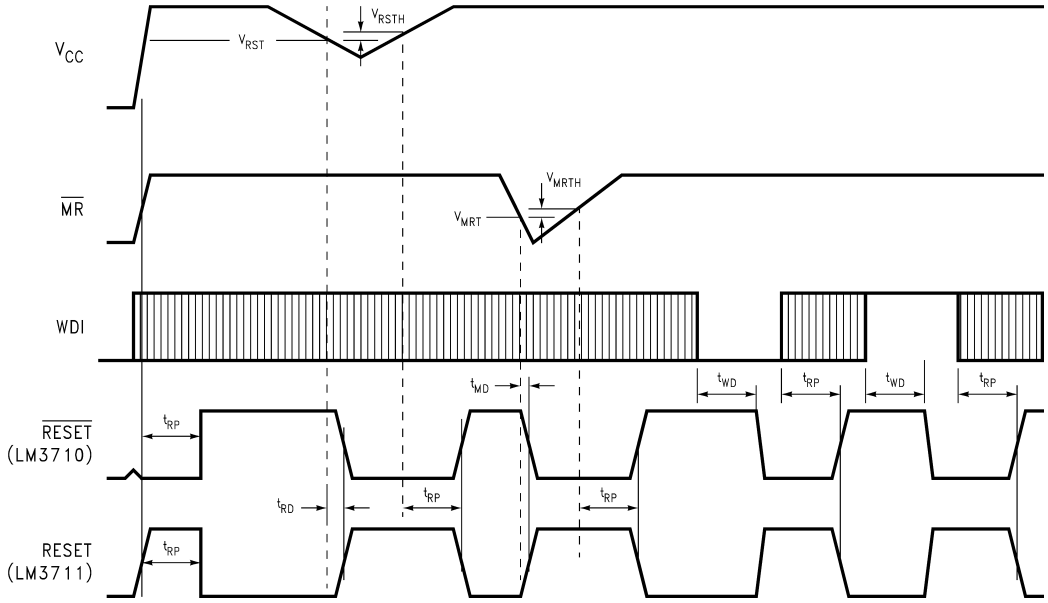


Figure 11. LM3710/LM3711 Reset Time with $\overline{MR}$ and WDI

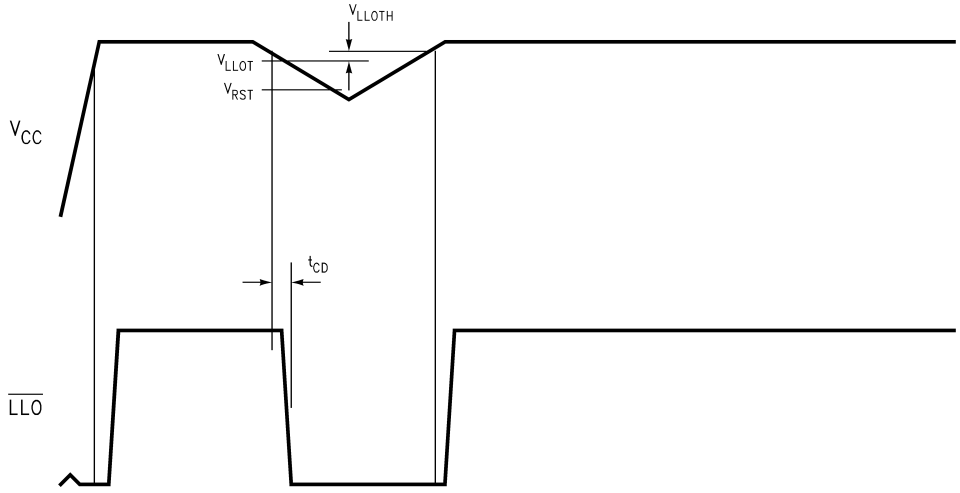


Figure 12. $\overline{LLO}$ Output

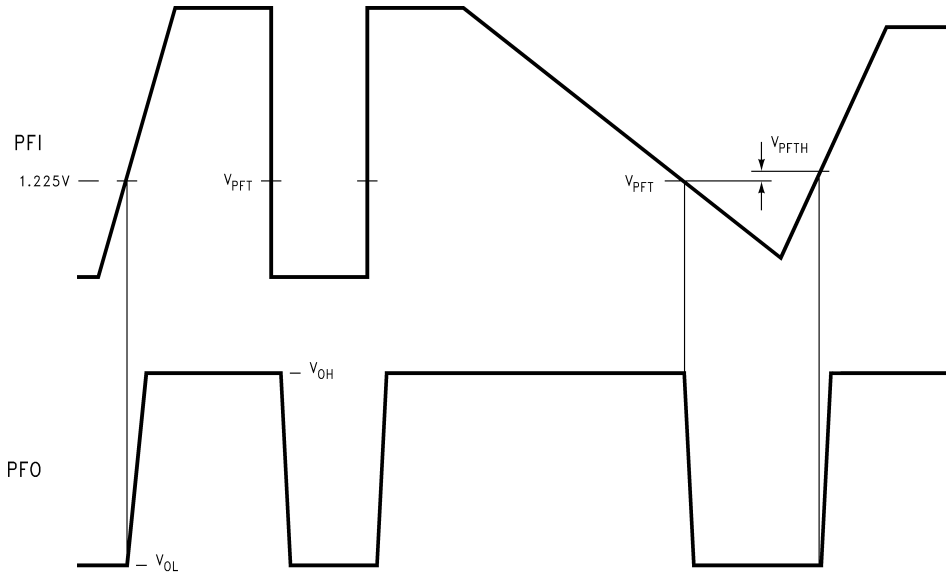


Figure 13. PFI Comparator Timing Diagram

Typical Application Circuits

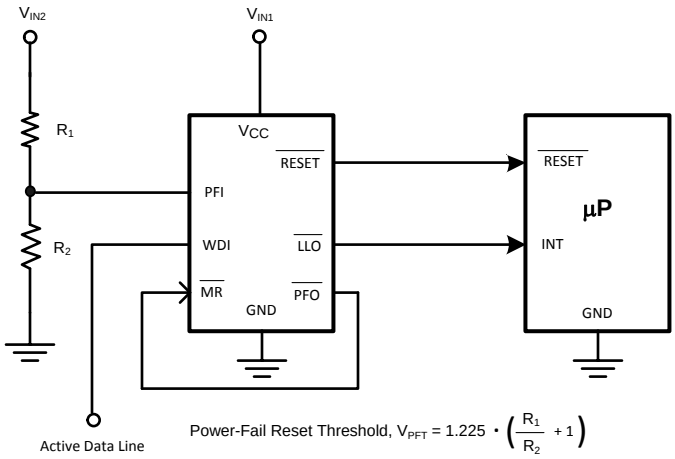


Figure 14. Monitoring Two Critical Supplies And Dataline

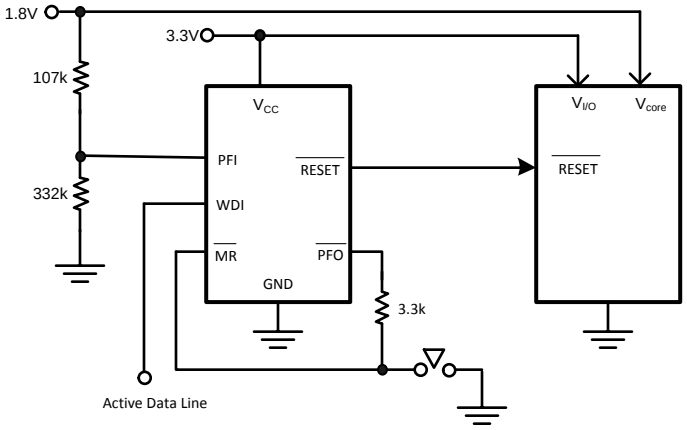


Figure 15. Monitoring Two Supplies plus Manual Reset And Dataline

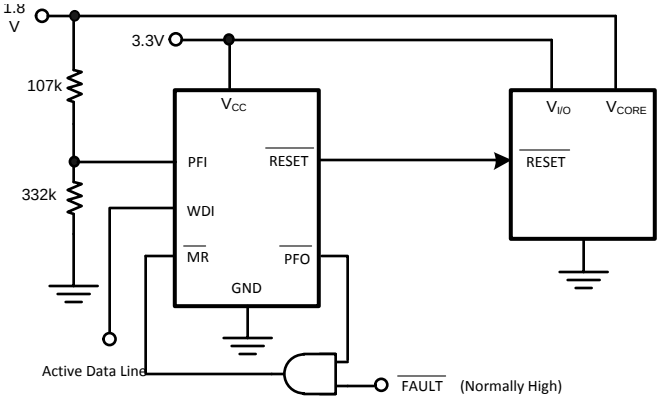
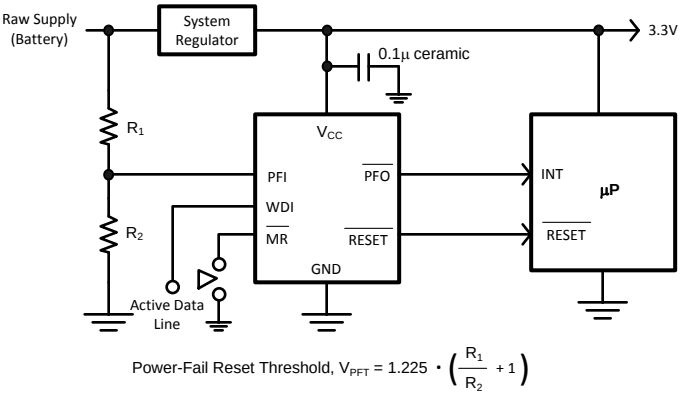


Figure 16. Monitoring Dual Supplies plus External Fault Input And Dataline



Note: $\overline{MR}$ input with its 1.225V nominal threshold, may monitor an additional supply voltage. An internal 56 kΩ pull-up resistor is included on this input.

Figure 17. Microprocessor Supervisor with Early Warning Detector

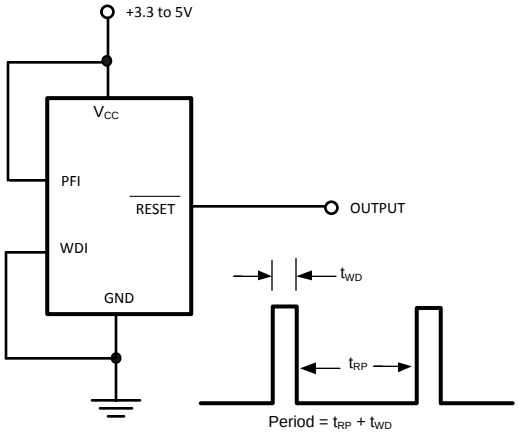


Figure 18. LM3710 Long Period oscillator

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E **Page**

- Changed layout of National Data Sheet to TI format 12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3710XKMM-463/NOPB	ACTIVE	VSSOP	DGS	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM		R74B	Samples
LM3710XQMM-308/NOPB	ACTIVE	VSSOP	DGS	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	R37B	Samples
LM3710YQMM-232/NOPB	ACTIVE	VSSOP	DGS	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM		R77B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

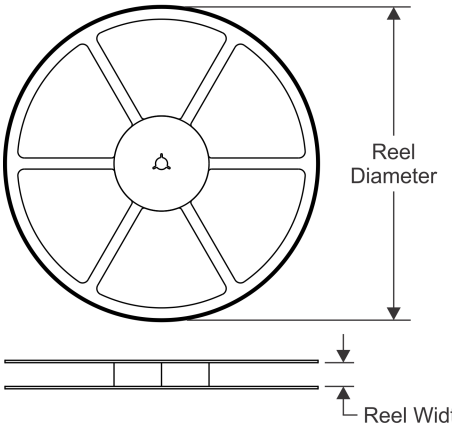
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

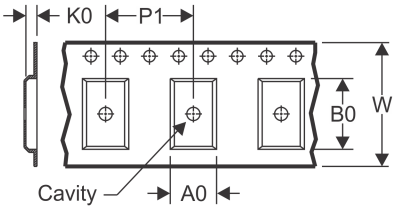
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

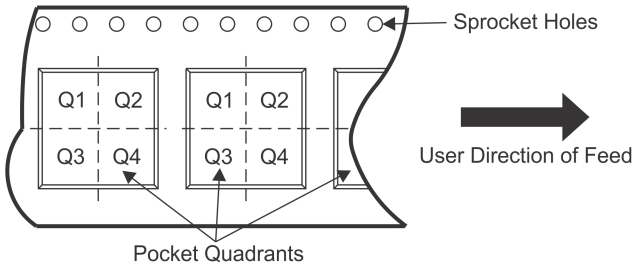


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

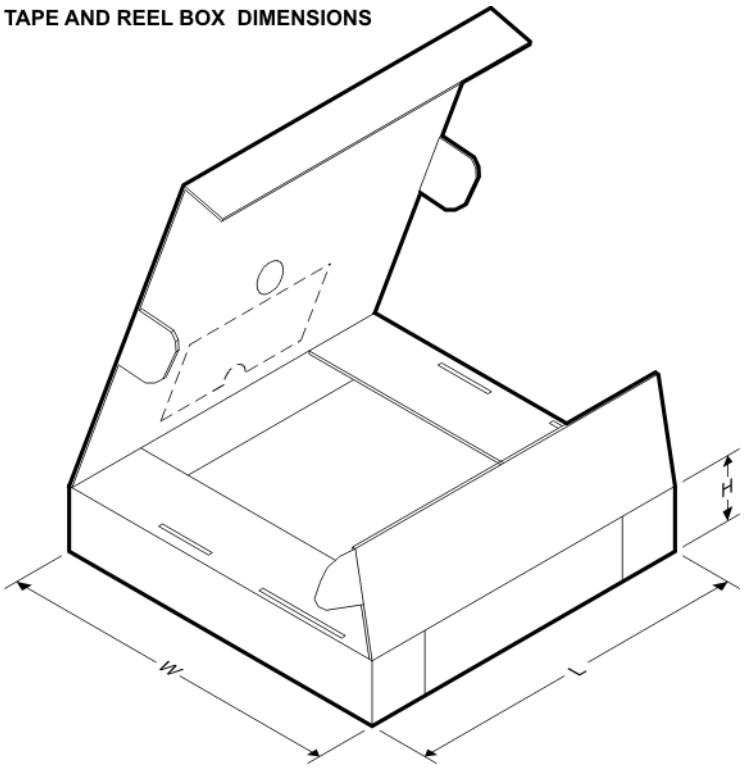
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3710XKMM-463/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3710XQMM-308/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3710YQMM-232/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

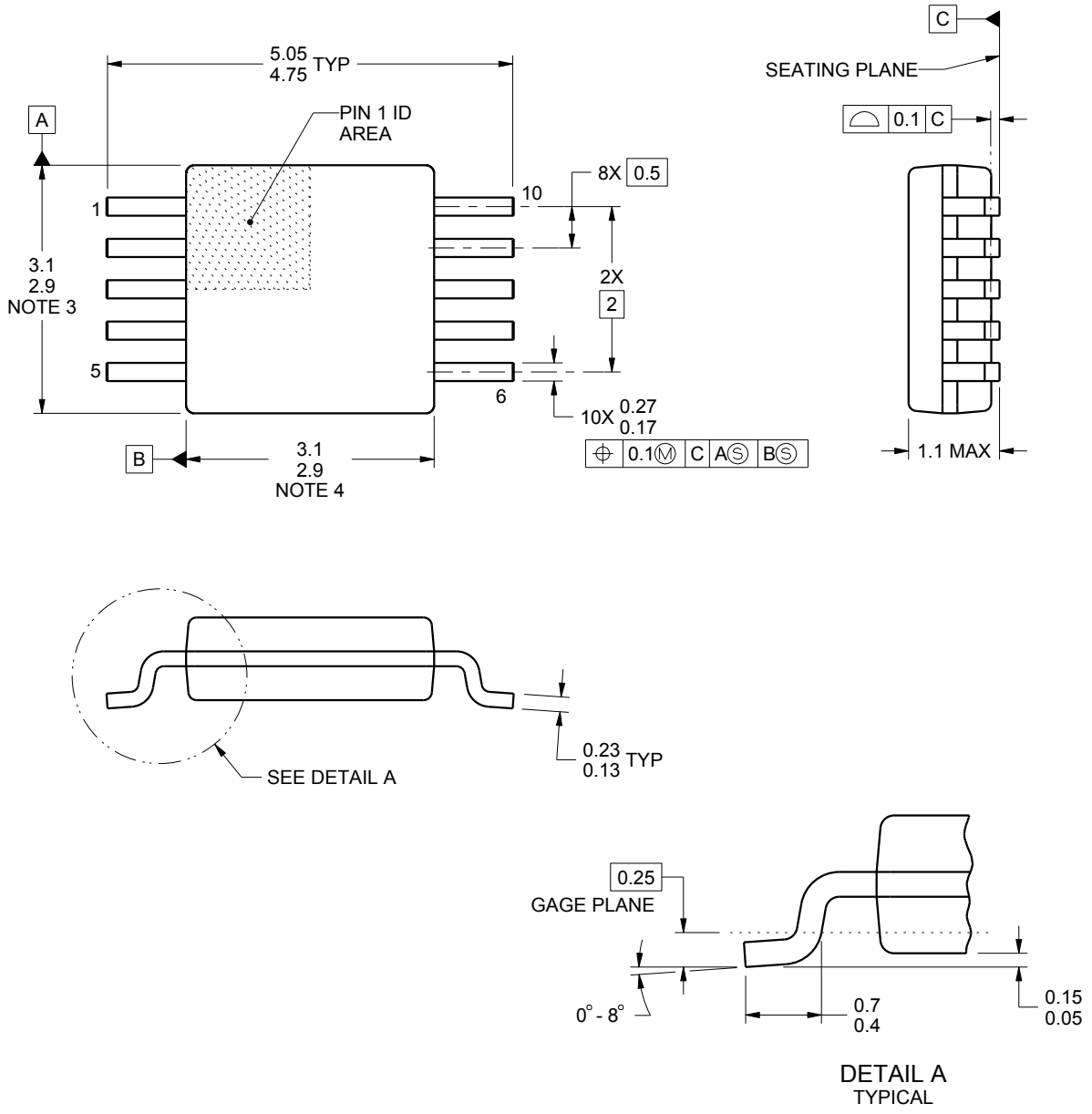
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3710XKMM-463/NOPB	VSSOP	DGS	10	1000	208.0	191.0	35.0
LM3710XQMM-308/NOPB	VSSOP	DGS	10	1000	208.0	191.0	35.0
LM3710YQMM-232/NOPB	VSSOP	DGS	10	1000	208.0	191.0	35.0

PACKAGE OUTLINE

DGS0010A

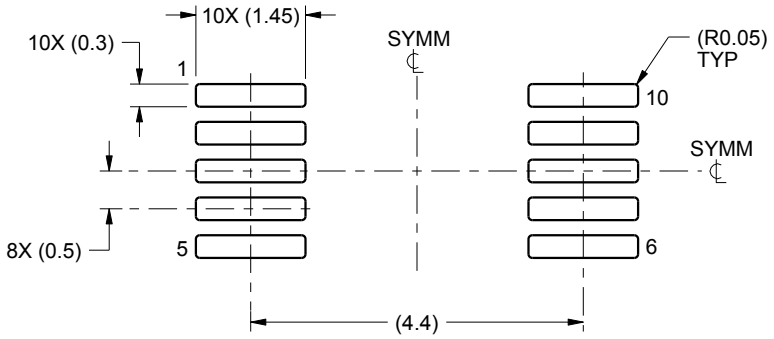
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

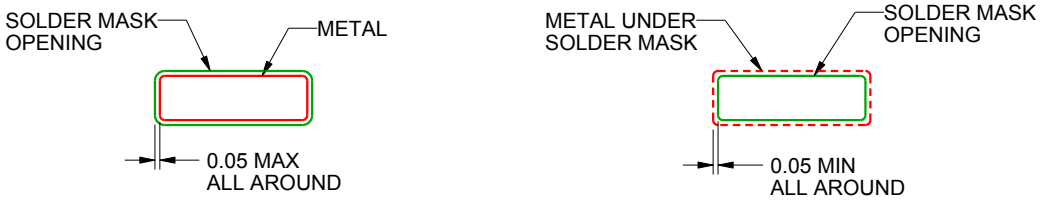


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

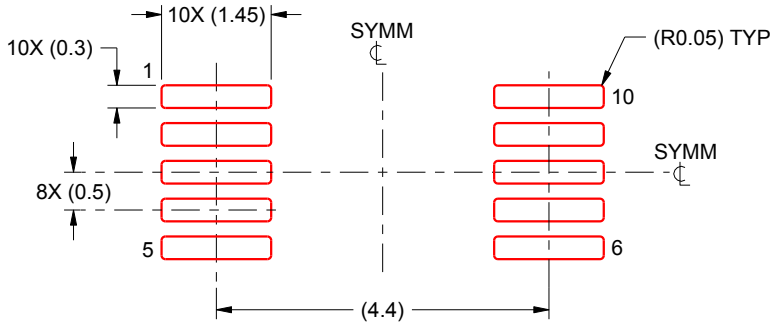


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265