



TLV717P 适用于便携式设备且具有折返电流限值的 150mA 低压降稳压器

1 特性

- 超低压降：电流为 150mA 时，压降为 215mV
 - 精度：0.5%（典型值）
 - 低 I_Q ：35 μ A
 - 可提供固定输出电压：
1.2V 至 5V
 - 高电源抑制比 (PSRR):
 - 1kHz 时为 70dB
 - 1MHz 时为 50dB
 - 搭配 0.1 μ F 有效输出电容使用时可保持稳定
 - 折返电流限制
 - 封装：1mm x 1mm DQN
- (1) 可提供电压选项的完整列表请参阅此文档末尾的封装选项附录。
- (2) 更多信息，请参见 [Input and Output Capacitor Requirements](#)。

2 应用

- 个人电脑 (PC) 和笔记本电脑
- 智能手机
- 便携式电子设备和电池供电类设备
- 电子销售点

3 说明

TLV717P 系列低压降线性稳压器 (LDO) 具有较低的静态电流，并且线路和负载瞬态性能出色，适用于功耗敏感型应用。此系列器件可提供典型值为 0.5% 的精度。

当负载电阻减小时，TLV717P 系列可提供折返电流以降低输出电流。电流折返初始典型值为 350mA；输出短路电流限值的典型值为 40mA。

此外，这些器件还能在采用仅 0.1 μ F 的有效输出电容时保持稳定。这一特性允许使用具有较高偏置电压和温度降额的成本有效电容器。这些器件在不产生输出负载的情况下可调节至特定的精度。

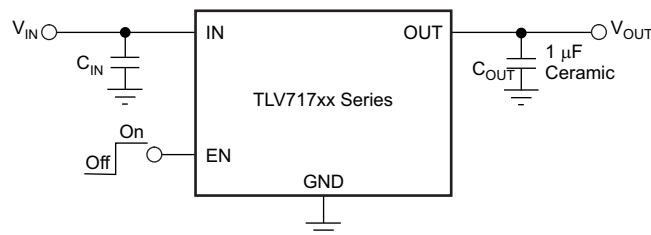
TLV717P 系列采用 1mm × 1mm DQN 封装，非常适合手持式应用。TLV717P 提供了一个有源下拉电路，用于使输出负载快速放电。

器件信息⁽¹⁾

器件型号	封装	封装尺寸（标称值）
TLV717P	X2SON (4)	1.00mm x 1.00mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

典型应用电路



Copyright © 2016, Texas Instruments Incorporated



目录

1	特性	1	8	Application and Implementation	11
2	应用	1	8.1	Application Information.....	11
3	说明	1	8.2	Typical Application	11
4	修订历史记录	2	9	Power Supply Recommendations	13
5	Pin Configuration and Functions	3	10	Layout	13
6	Specifications	4	10.1	Layout Guidelines	13
6.1	Absolute Maximum Ratings	4	10.2	Layout Example	13
6.2	ESD Ratings.....	4	10.3	Power Dissipation	13
6.3	Recommended Operating Conditions.....	4	11	器件和文档支持	14
6.4	Thermal Information	4	11.1	器件支持	14
6.5	Electrical Characteristics.....	5	11.2	文档支持	14
6.6	Typical Characteristics	6	11.3	社区资源	14
7	Detailed Description	9	11.4	商标	14
7.1	Overview	9	11.5	静电放电警告	14
7.2	Functional Block Diagram	9	11.6	Glossary	14
7.3	Feature Description.....	9	12	机械封装和可订购信息	15
7.4	Device Functional Modes.....	10			

4 修订历史记录

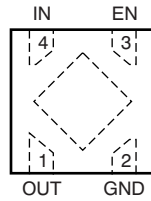
注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (February 2012) to Revision B	Page
• 已删除 TLV717xx 的所有实例；已替换为通用部件号“TLV717P”	1
• 已更新应用	1
• 已添加 ESD 额定值表，特性 描述 部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分	1
• Changed $T_J = -25^{\circ}\text{C}$ to $T_J = 25^{\circ}\text{C}$ in the conditions statement in <i>Absolute Maximum Ratings</i>	4
• Changed T_A to T_J throughout <i>Electrical Characteristics</i>	5
• Changed T_A to T_J in the conditions statement in <i>Typical Characterisitcs</i>	6
• Changed T_A to T_J in the conditions statement in <i>Typical Characterisitcs</i>	7
• Changed T_A to T_J in the conditions statement in <i>Typical Characterisitcs</i>	8
• Changed junction temperature range from -40°C to 125°C to -40°C to 85°C in <i>Overview</i>	9
• Deleted TLV717xx functional block diagram	9

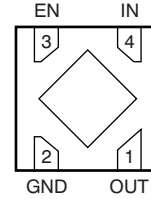
Changes from Original (October 2011) to Revision A	Page
• 已更改 文档状态从 产品预览 改为 生产数据	1

5 Pin Configuration and Functions

**DQN Package
4-Pin X2SON
Top View**



**DQN Package
4-Pin X2SON
Bottom View**



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	3	I	Enable pin. Driving EN over 1.2 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
GND	2	—	Ground pin
IN	4	I	Input pin. A small capacitor is recommended from this pin to ground to assure stability. See the Input and Output Capacitor Requirements section in the Application and Implementation for more details.
OUT	1	O	Regulated output voltage pin. A small 1-μF ceramic capacitor is recommended from this pin to ground to assure stability. See the Input and Output Capacitor Requirements section in the Application and Implementation for more details.
Thermal pad	—	—	Connect to GND for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

At $T_J = 25^{\circ}\text{C}$, unless otherwise noted. All voltages are with respect to GND.⁽¹⁾

		MIN	MAX	UNIT
Voltage	Input range, V_{IN}	−0.3	6	V
	Enable range, V_{EN}	−0.3	$V_{IN} + 0.3$	
	Output range, V_{OUT}	−0.3	6	
Current	Maximum output, I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation, P_{DISS}		See Thermal Information		
Temperature	Junction, T_J	−55	150	$^{\circ}\text{C}$
	Storage junction, T_{stg}	−55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	1.7	5.5	V
V_{OUT}	Output voltage	1.2	5	V
I_{OUT}	Output current	0	150	mA
V_{EN}	Enable pin voltage	0	V_{IN}	V
T_J	Junction temperature	−40	85	$^{\circ}\text{C}$

6.4 Thermal Information

THERMAL METRIC		TLV717P	UNIT
		DQN (X2SON)	
		4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	393.3	$^{\circ}\text{C/W}$
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	140.3	$^{\circ}\text{C/W}$
$R_{\theta JB}$	Junction-to-board thermal resistance	330	$^{\circ}\text{C/W}$
Ψ_{JT}	Junction-to-top characterization parameter	6.5	$^{\circ}\text{C/W}$
Ψ_{JB}	Junction-to-board characterization parameter	329	$^{\circ}\text{C/W}$
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	147.5	$^{\circ}\text{C/W}$

6.5 Electrical Characteristics

At operating temperature range ($T_J = -40^{\circ}\text{C}$ to 85°C), $T_J = 25^{\circ}\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or 1.7 V (whichever is greater), $I_{OUT} = 10\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{OUT} = 1\text{ }\mu\text{F}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		1.7		5.5	V
V_{OUT}	Output voltage range		1.2		5	V
I_{OUT}	Output current		150			mA
DC output accuracy		$T_J = +25^{\circ}\text{C}$	0.5%			
		$V_{OUT} \geq 1.2\text{ V}$, $-40^{\circ}\text{C} \leq T_J \leq +85^{\circ}\text{C}$	-1.5%		1.5%	
		$V_{OUT} \leq 1.2\text{ V}$			25	mV
$\Delta V_O/V_{IN}$	Line regulation	$V_{OUT(NOM)} + 0.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$		1	5	mV
$\Delta V_O/I_{OUT}$	Load regulation	$0\text{ mA} \leq I_{OUT} \leq 150\text{ mA}$		10	20	mV
V_{DO}	Dropout voltage	$V_{IN} = 0.98 \times V_{OUT(NOM)}$, $I_{OUT} = 150\text{ mA}$	$1.2\text{ V} \leq V_{OUT} < 1.5\text{ V}$	330	500	mV
			$1.5\text{ V} \leq V_{OUT} < 1.8\text{ V}$	330	450	
			$1.8\text{ V} \leq V_{OUT} \leq 5\text{ V}$	215	350	
I_{GND}	Ground pin current	$I_{OUT} = 0\text{ mA}$		35	55	μA
I_{SHDN}	Shutdown current	$V_{EN} \leq 0.4\text{ V}$, $2\text{ V} \leq V_{IN} \leq 4.5\text{ V}$		0.1	0.5	μA
PSRR	Power-supply rejection ratio	$V_{IN} = 3.3\text{ V}$, $V_{OUT} = 2.8\text{ V}$, $I_{OUT} = 30\text{ mA}$	$f = 10\text{ Hz}$	70		dB
			$f = 100\text{ Hz}$	70		
			$f = 1\text{ kHz}$	65		
			$f = 10\text{ kHz}$	60		
			$f = 100\text{ kHz}$	43		
V_{NOISE}	Output noise voltage	$BW = 100\text{ Hz to }100\text{ kHz}$, $V_{IN} = 2.3\text{ V}$, $V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 10\text{ mA}$		55		μV_{RMS}
t_{STR}	Start-up time	$C_{OUT} = 1\text{ }\mu\text{F}$, $I_{OUT} = 150\text{ mA}$		100		μs
I_{SC}	Short current limit	$V_{IN} = \min(V_{OUT(NOM)} + 1\text{ V}, 5.5\text{ V})$, $V_{OUT} = 0\text{ V}$		40		mA
V_{HI}	Enable high (enabled)		0.9		V_{IN}	V
V_{LO}	Enable low (disabled)		0		0.4	V
I_{EN}	EN pin current	$EN = 5.5\text{ V}$		0.01		μA
$R_{PULLDOWN}$	Pulldown resistor			120		Ω
UVLO	Undervoltage lockout	V_{IN} rising		1.6		V

6.6 Typical Characteristics

At operating temperature range ($T_J = -40^\circ\text{C}$ to 85°C), $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or 1.7 V (whichever is greater), $I_{OUT} = 10\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{OUT} = 1\text{ }\mu\text{F}$, unless otherwise noted.

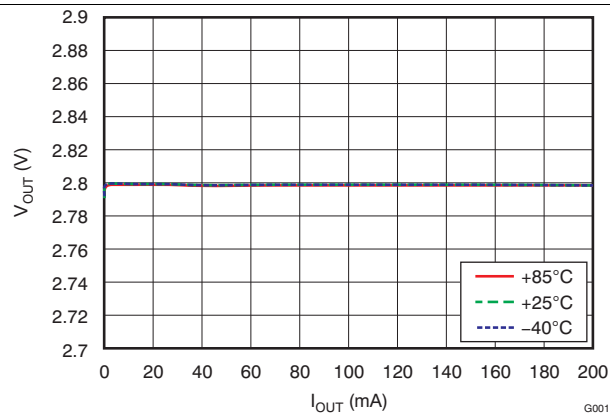


Figure 1. Load Regulation

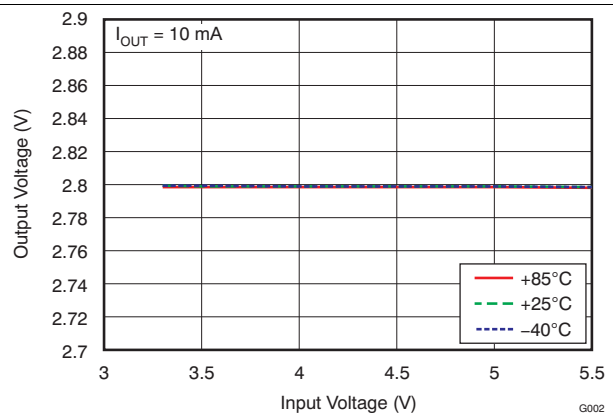


Figure 2. Line Regulation

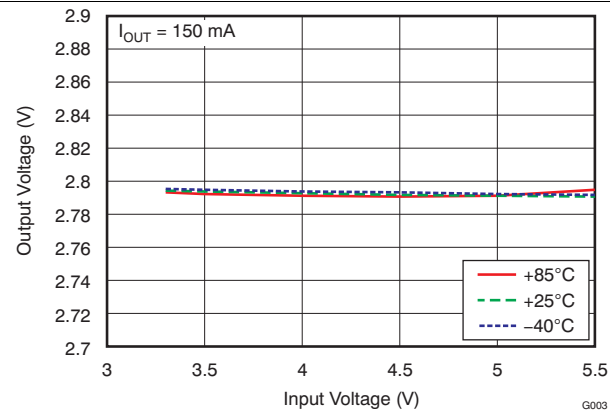


Figure 3. Line Regulation

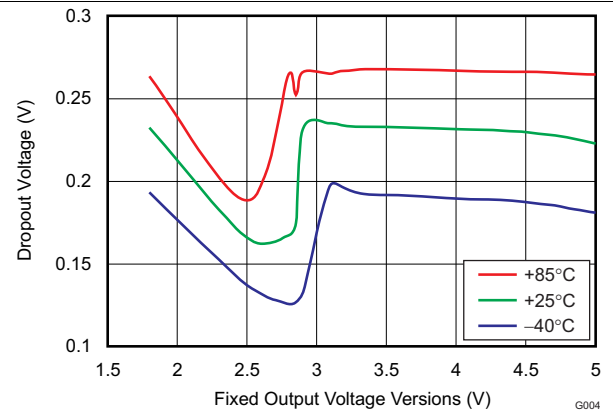


Figure 4. Dropout Voltage vs Fixed Output Voltage Versions

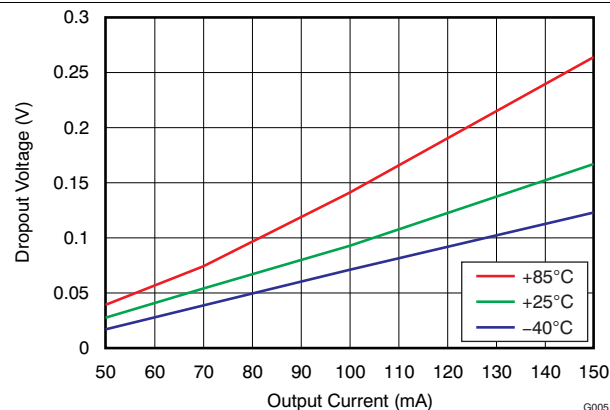


Figure 5. Dropout Voltage vs Output Current

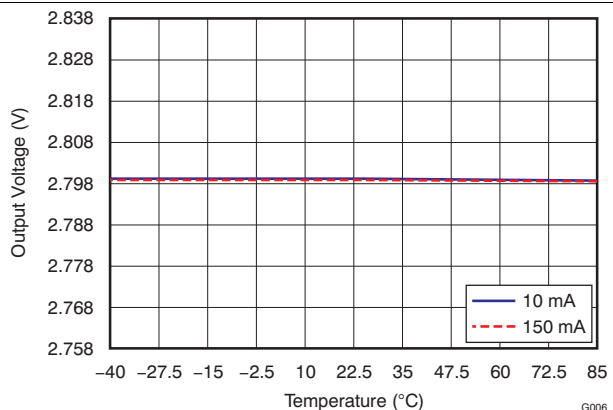


Figure 6. Output Voltage vs Temperature

Typical Characteristics (continued)

At operating temperature range ($T_J = -40^{\circ}\text{C}$ to 85°C), $T_J = 25^{\circ}\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or 1.7 V (whichever is greater), $I_{OUT} = 10\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{OUT} = 1\text{ }\mu\text{F}$, unless otherwise noted.

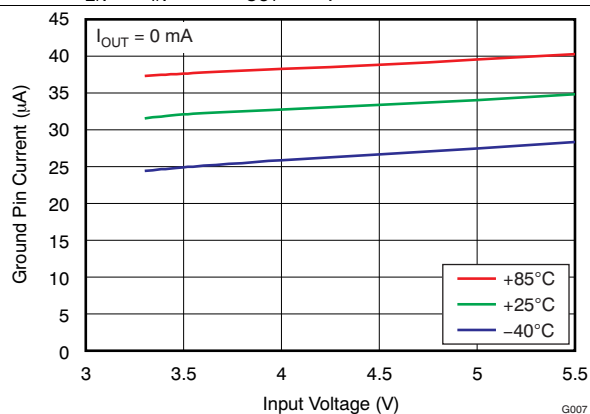


Figure 7. Ground Pin Current vs Input Voltage

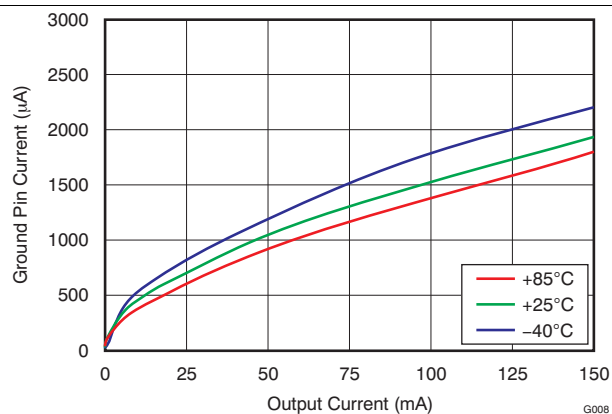


Figure 8. Ground Pin Current vs Output Current

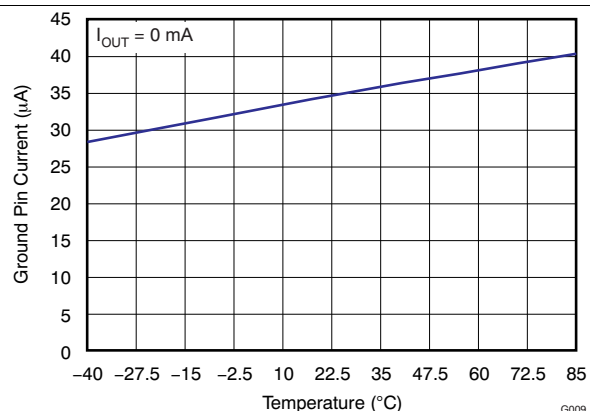


Figure 9. Ground Pin Current vs Temperature

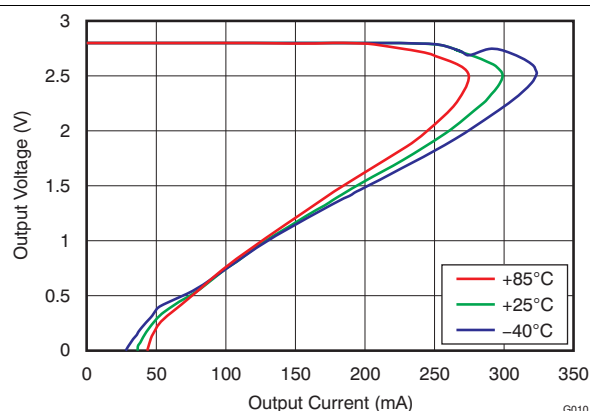


Figure 10. Output Voltage vs Output Current

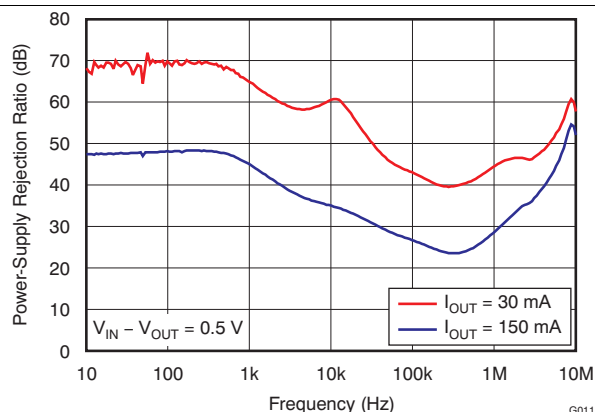


Figure 11. TLV71728PSRR vs Frequency

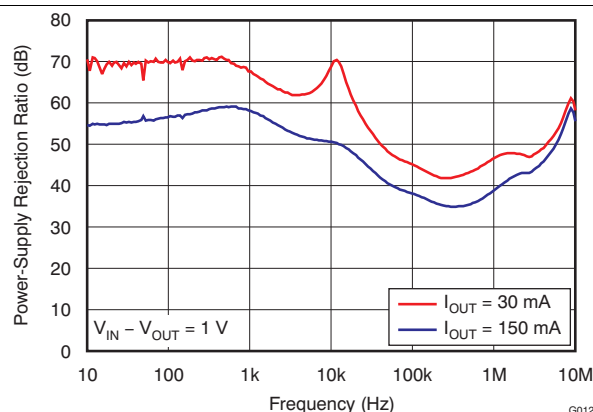


Figure 12. TLV71728PSRR vs Frequency

Typical Characteristics (continued)

At operating temperature range ($T_J = -40^{\circ}\text{C}$ to 85°C), $T_J = 25^{\circ}\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or 1.7 V (whichever is greater), $I_{OUT} = 10\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{OUT} = 1\text{ }\mu\text{F}$, unless otherwise noted.

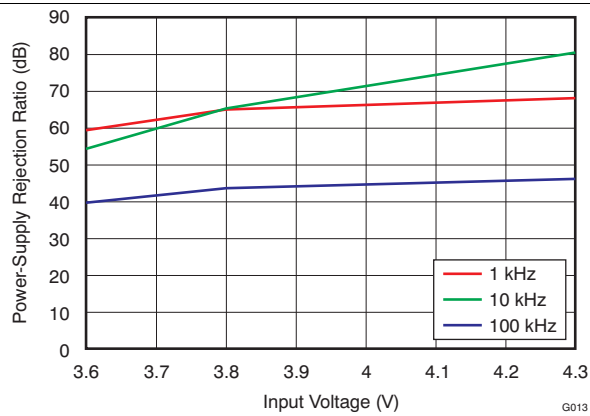


Figure 13. PSRR vs Input Voltage

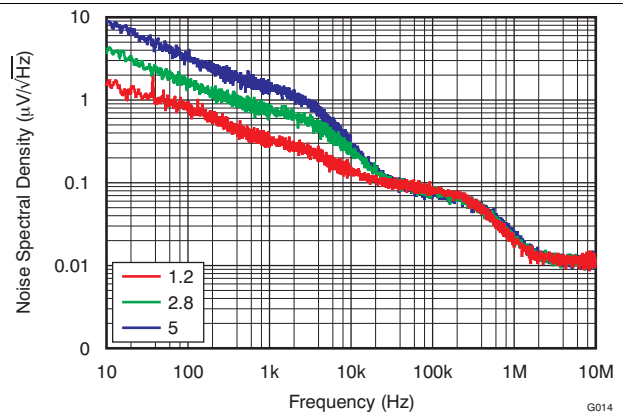


Figure 14. Output Spectral Noise Density vs Frequency

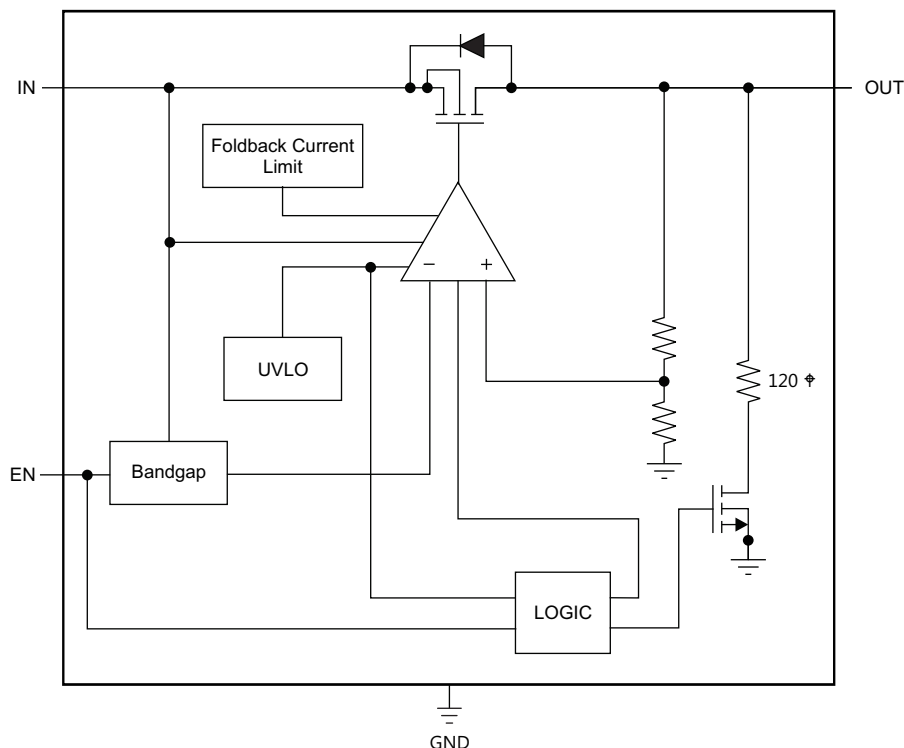
7 Detailed Description

7.1 Overview

The TLV717P belongs to a new family of next-generation value low-dropout (LDO) regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise, very good PSRR with little ($V_{IN} - V_{OUT}$) headroom, make this family of devices ideal for RF portable applications.

This family of regulators offers current foldback. Device operating junction temperature is -40°C to 85°C .

7.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

7.3 Feature Description

7.3.1 Internal Current Limit

The TLV717P has an internal foldback current limit that helps to protect the regulator during fault conditions. The current supplied by the device is gradually throttled down as the output voltage decreases. When the output is shorted, the LDO supplies a typical current of 40 mA. Output voltage is not regulated when the device is in current limit, and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The advantage of foldback current limit is that the I_{LIMIT} value is less than the fixed current limit. Therefore, the power that the PMOS pass transistor dissipates $[(V_{IN} - V_{OUT}) \times I_{LIMIT}]$ is much less.

The TLV717P PMOS pass element has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

Feature Description (continued)

7.3.2 Shutdown

The enable pin (EN) is active high. The device is enabled when the voltage at the EN pin goes above 0.9 V. This relatively lower voltage value required to turn the LDO on can be exploited to power the LDO with a GPIO of recent processors whose GPIO logic 1 voltage level is lower than traditional microcontrollers. The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, EN can be connected to the IN pin.

7.3.3 Undervoltage Lockout (UVLO)

The TLV717P uses an undervoltage lockout circuit ($UVLO = 1.6\text{ V}$) to keep the output shut off until the internal circuitry operates properly.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage has previously exceeded the UVLO rising voltage and has not decreased below the UVLO falling threshold.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and not decreased below the enable falling threshold.
- The output current is less than the current limit.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout may result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The input voltage is less than the UVLO falling voltage, or has not yet exceeded the UVLO rising threshold.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.

When the device is disabled, the active pulldown resistor discharges the output.

[Table 1](#) lists the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER		
	V_{IN}	V_{EN}	I_{OUT}
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > UVLO_{RISE}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$
Dropout mode	$UVLO_{RISE} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$
Disabled mode (any true condition disables the device)	$V_{IN} < UVLO_{FALL}$	$V_{EN} < V_{EN(LO)}$	—

8 Application and Implementation

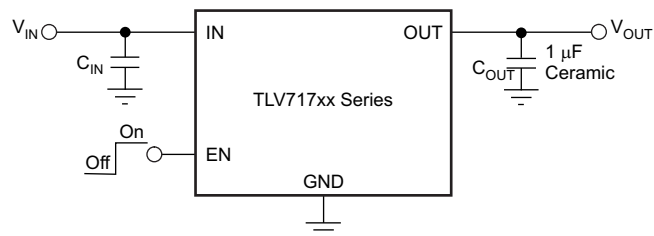
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV717P is a low-dropout regulator (LDO) with low quiescent current that delivers excellent line and load transient performance. This LDO regulator offers a foldback current limit. The operating junction temperature of this device series is -40°C to 85°C .

8.2 Typical Application



Copyright © 2016, Texas Instruments Incorporated

Figure 15. Typical Application Circuit

8.2.1 Design Requirements

Table 2 lists the parameters for this application.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	3.8 V
Output voltage	2.8 V $\pm 1\%$
Output current	30 to 150 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

TI recommends X5R- and X7R-type ceramic capacitors because they have minimal variation in value and equivalent series resistance (ESR) over temperature. The TLV717P is designed to be stable with an effective capacitance of 0.1 μF or larger at the output, though TI recommends a 1- μF ceramic capacitor for typical applications. Thus, the device is stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1 μF . This effective capacitance refers to the capacitance that the LDO detects under operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature derating into consideration. In addition to allowing the use of cheaper dielectrics, this capability of being stable with 0.1- μF effective capacitance also enables the use of smaller footprint capacitors that have higher derating in size- and space-constrained applications. Using a 0.1- μF rated capacitor at the LDO output does not ensure stability because the effective capacitance under the specified operating conditions would be less than 0.1 μF . Maximum ESR should be less than 200 m Ω .

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1- μF to 1- μF , low ESR capacitor across the IN and GND pins of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast, rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2 Ω , a 0.1- μF input capacitor may be necessary to ensure stability.

8.2.2.2 Dropout Voltage

The TLV717P uses a PMOS pass transistor to achieve low dropout. When $(V_{IN} - V_{OUT})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout. As with any linear regulator, PSRR and transient response are degraded as $(V_{IN} - V_{OUT})$ approaches dropout.

8.2.2.3 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude but increases the duration of the transient response.

8.2.3 Application Curves

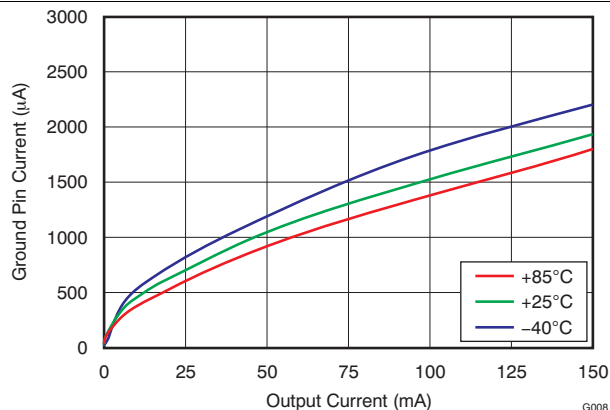


Figure 16. Ground Pin Current vs Output Current

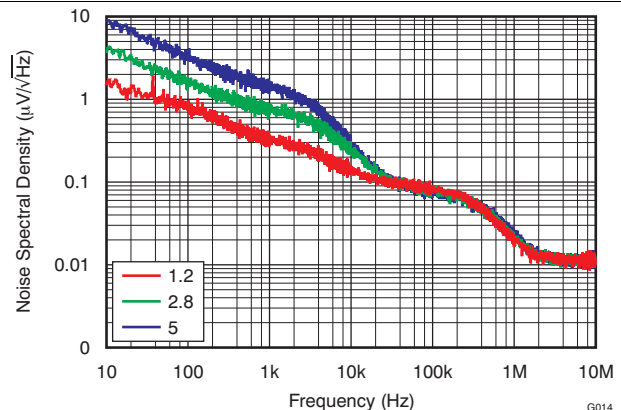


Figure 17. Output Spectral Noise Density vs Frequency

9 Power Supply Recommendations

Connect a low-output impedance power supply directly to the IN pin of the TLV717P. Inductive impedances between the input supply and the IN pin can create significant voltage excursions at the IN pin during start-up or load transient events. If inductive impedances are unavoidable, use an input capacitor.

10 Layout

10.1 Layout Guidelines

Input and output capacitors should be placed as close to the device pins as possible. To improve AC performance (such as PSRR, output noise, and transient response), TI recommends designing the board with separate ground planes for V_{IN} and V_{OUT} , with the ground plane connected only at the device GND pin. In addition, the output capacitor ground connection should be connected directly to the device GND pin. High ESR capacitors may degrade PSRR performance.

10.2 Layout Example

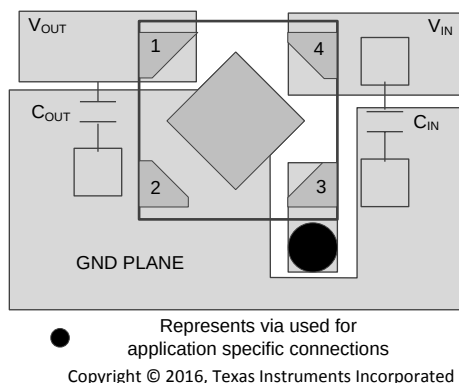


Figure 18. Recommended Layout Example

10.3 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed-circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to ambient air. Performance data for JEDEC-low and high-K boards are given in [Thermal Information](#). Using heavier copper increases the effectiveness in removing heat from the device. The addition, plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in [Equation 1](#).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 评估模块

评估模块 (EVM) 可与 TLV717P 配套使用，协助评估初始电路性能。SLVU553 详细介绍了 TLV71733PEVM-072 的设计套件和评估模块。

EVM 可通过德州仪器 (TI) 网站上的 [TLV717P](#) 产品文件夹获取，也可[直接从 TI 网上商店](#)购买。

11.1.2 器件命名规则

表 3. 器件命名规则⁽¹⁾

产品	V _{OUT}
TLV717xx(x)Pyyyz	XX(X) 是标称输出电压。对于分辨率为 100mV 的输出电压，订货编号中使用两位数字；否则，使用三位数字（例如，28 = 2.8V；475 = 4.75 V）。 P 表示有源输出放电功能。TLV717P 系列的所有器件在禁用时都可以使输出进行有源放电。 YYY 为封装标识符。 Z 为封装数量。R 表示 3000 片，T 表示 250 片。

(1) 要获得最新的封装和订货信息，请参见本文档末尾的封装选项附录，或者访问器件产品文件夹 ([www.ti.com](#))。

11.2 文档支持

11.2.1 相关文档

《TLV71733PEVM-072 评估模块用户指南》，[SLVU553](#)

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改, 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内, 且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定, 否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应用相关的风险, 客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息, 不能构成从 TI 获得使用这些产品或服务 的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可, 或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分, 仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时, 如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分, 则会失去相关 TI 组件 或服务的所有明示或暗示授权, 且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意, 尽管任何应用相关信息或支持仍可能由 TI 提供, 但他们将独力负责满足与其产品及其应用中使用的 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意, 他们具备制定与实施安全措施所需的全部专业技术和知识, 可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中, 为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此, 此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III (或类似的生命攸关医疗设备) 的授权许可, 除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意, 对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用, 其风险由客户单独承担, 并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品, 这些产品主要用于汽车。在任何情况下, 因使用非指定产品而无法达到 ISO/TS16949 要求, TI 不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com.cn/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com.cn/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com.cn/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址: 上海市浦东新区世纪大道1568号, 中建大厦32楼邮政编码: 200122
Copyright © 2016, 德州仪器半导体技术(上海)有限公司

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV71712PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	UX	Samples
TLV71712PDQNR3	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UX	Samples
TLV71712PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	UX	Samples
TLV71713PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VC	Samples
TLV71713PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VC	Samples
TLV71715PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	UY	Samples
TLV71715PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	UY	Samples
TLV717185PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VN	Samples
TLV717185PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VN	Samples
TLV71718PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	UZ	Samples
TLV71718PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	UZ	Samples
TLV71721PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AR	Samples
TLV71721PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AR	Samples
TLV71725PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VA	Samples
TLV71725PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VA	Samples
TLV71727PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AS	Samples
TLV71727PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AS	Samples
TLV717285PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM		VE	Samples
TLV717285PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VE	Samples
TLV71728PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VD	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV71728PDQNR3	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VD	Samples
TLV71728PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VD	Samples
TLV71729PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VI	Samples
TLV71729PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VI	Samples
TLV71730PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VF	Samples
TLV71730PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VF	Samples
TLV71733PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VG	Samples
TLV71733PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VG	Samples
TLV71736PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VH	Samples
TLV71736PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VH	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

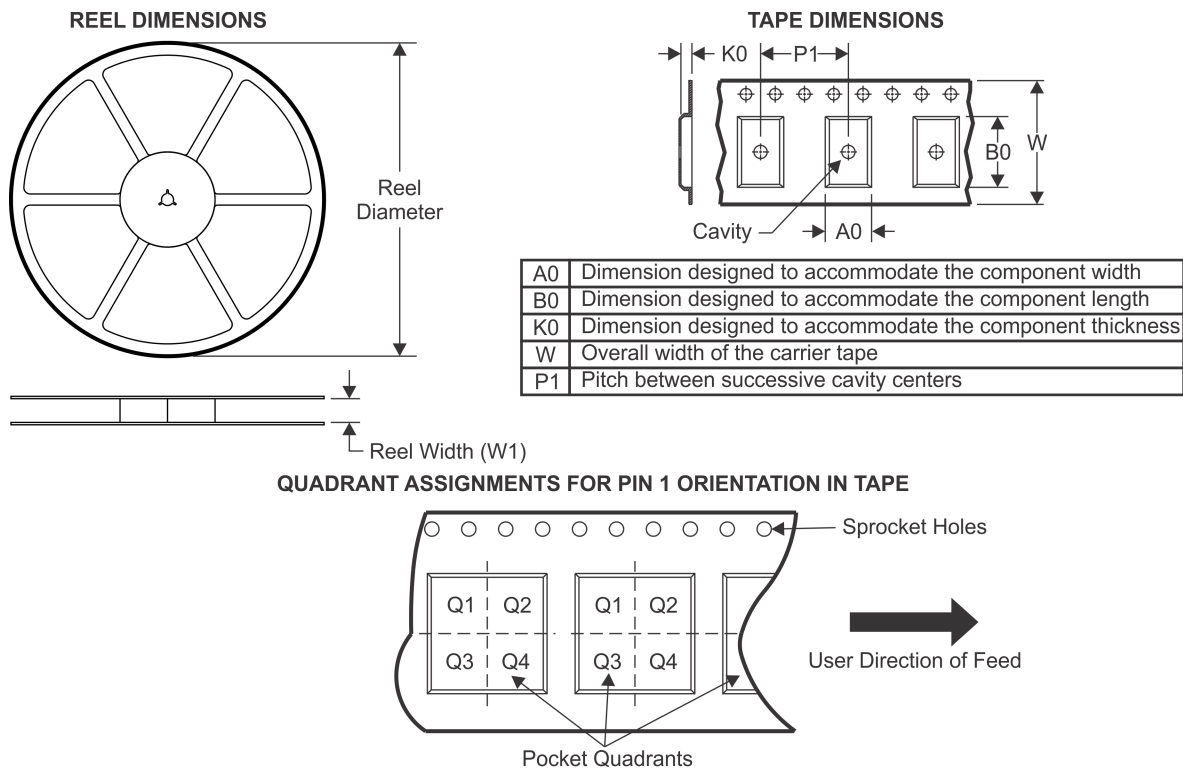
⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

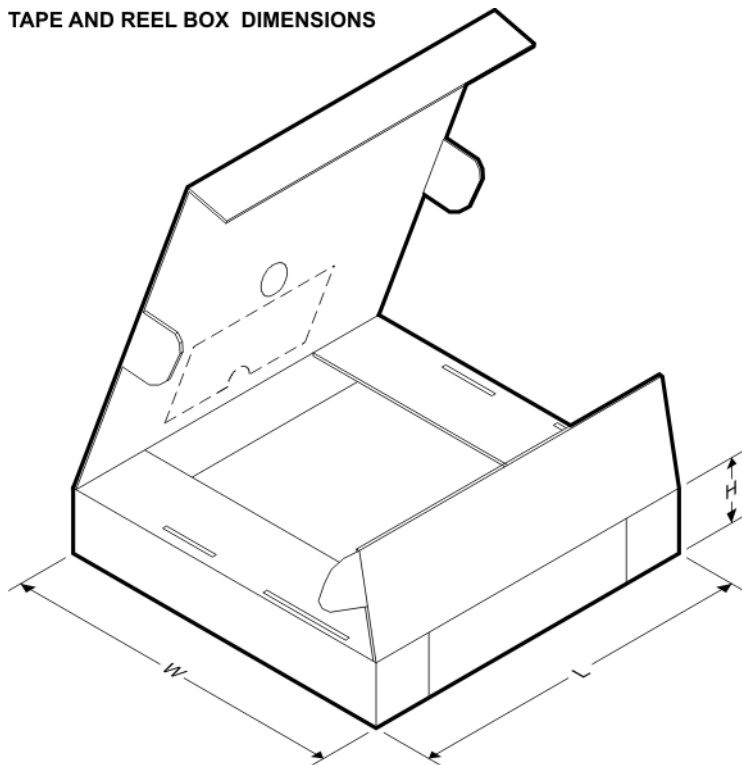
TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV71712PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71712PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71712PDQNR3	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	2.0	8.0	Q3
TLV71712PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71712PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71713PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71713PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71713PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71713PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71715PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71715PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71715PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71715PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV717185PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV717185PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV71718PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV71718PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV71721PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV71721PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71721PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71721PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71725PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71725PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71725PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71725PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71727PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV71727PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV717285PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV717285PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV717285PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV717285PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71728PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71728PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71728PDQNR3	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	2.0	8.0	Q3
TLV71728PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71728PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71729PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV71729PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV71730PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71730PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71730PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71730PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71733PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV71733PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV71736PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71736PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71736PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71736PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV71712PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71712PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV71712PDQNR3	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71712PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71712PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV71713PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV71713PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71713PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV71713PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71715PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71715PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV71715PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71715PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV717185PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV717185PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV71718PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV71718PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV71721PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV71721PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71721PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV71721PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71725PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV71725PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71725PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71725PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV71727PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV71727PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV717285PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV717285PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV717285PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV717285PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71728PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71728PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV71728PDQNR3	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71728PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV71728PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71729PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV71729PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV71730PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71730PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV71730PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV71730PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71733PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV71733PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV71736PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71736PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV71736PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71736PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0

DQN 4

GENERIC PACKAGE VIEW

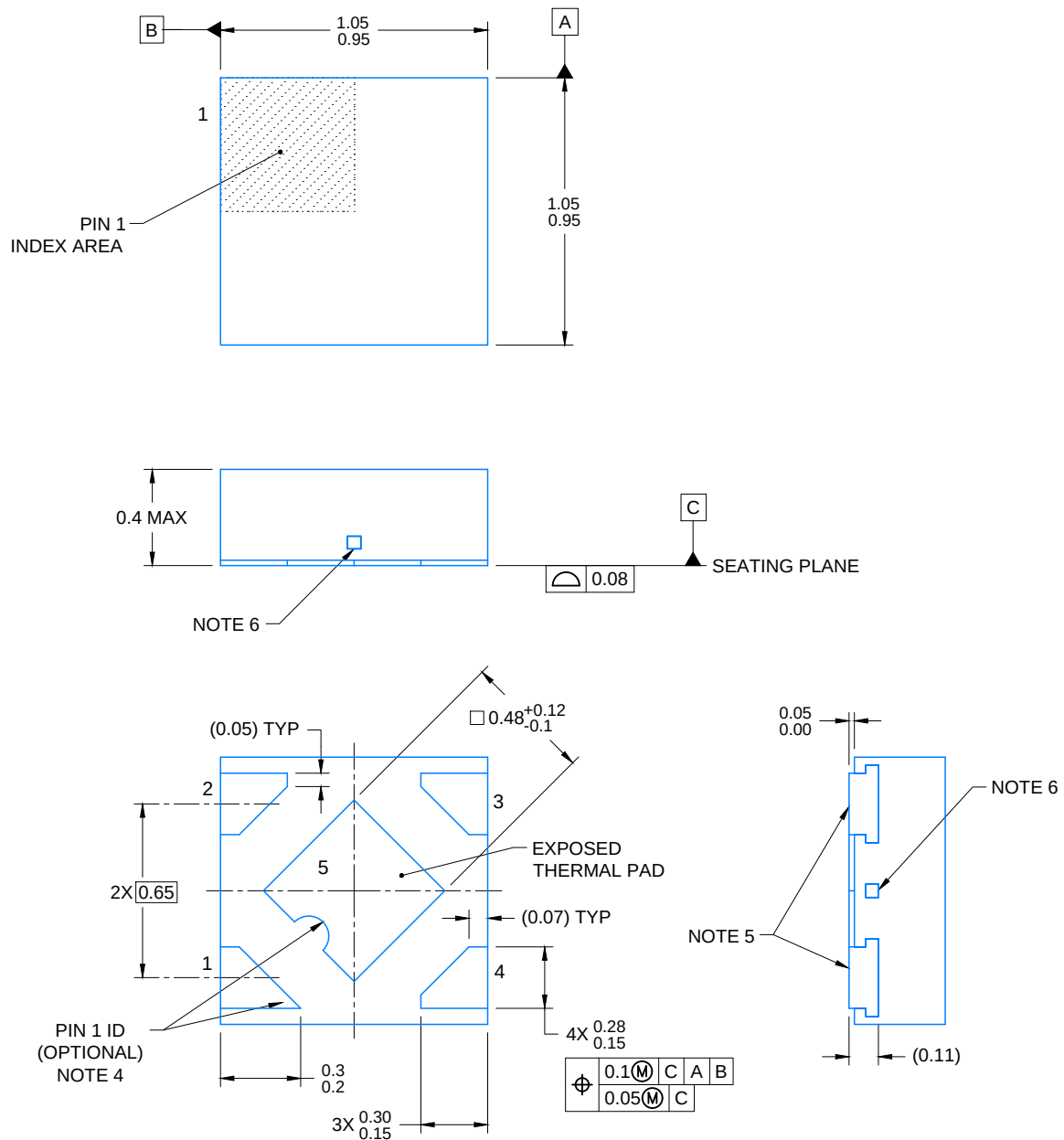
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

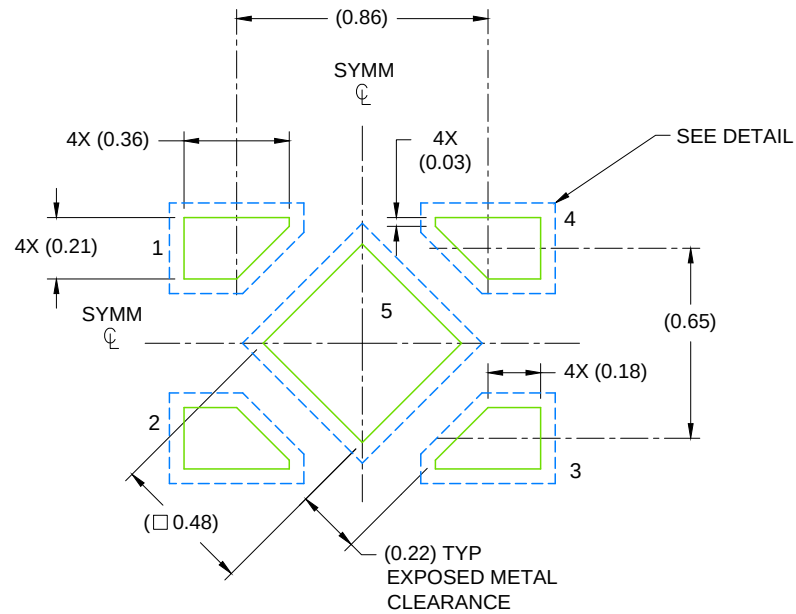
4210367/F



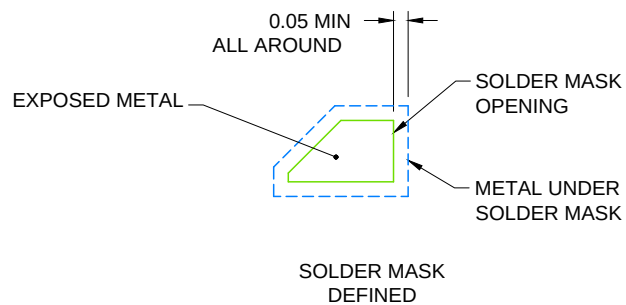
4215302/E 12/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE
SCALE: 40X

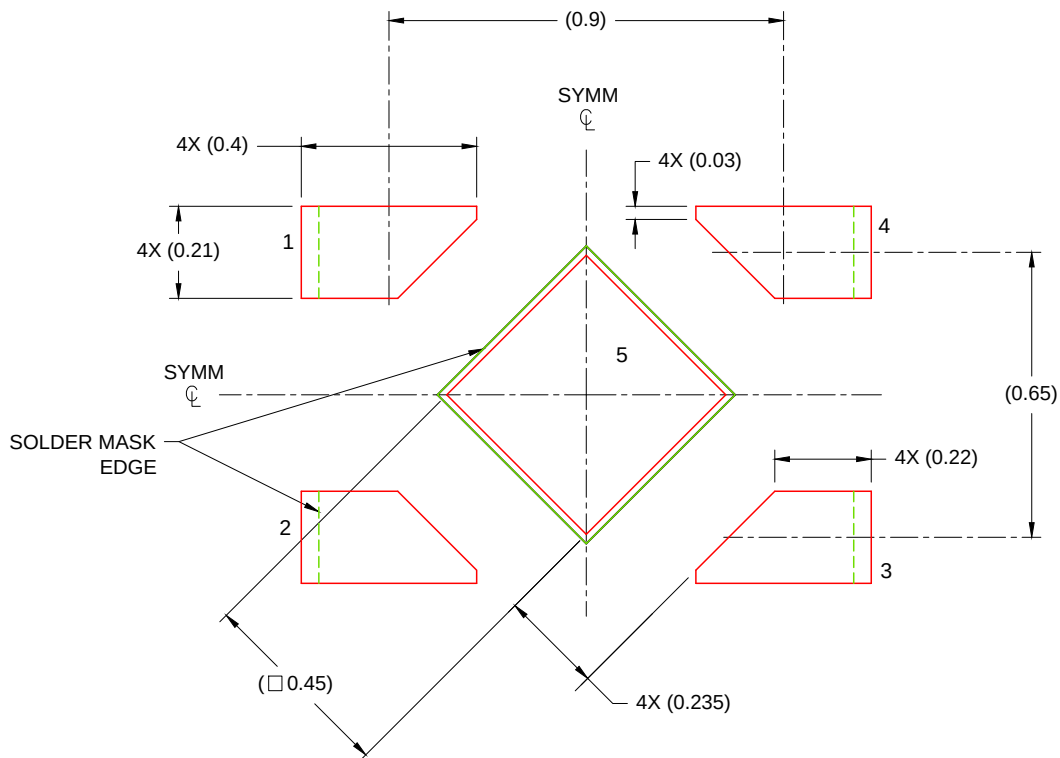


SOLDER MASK DETAIL

4215302/E 12/2016

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
 BASED ON 0.075 - 0.1mm THICK STENCIL

EXPOSED PAD
 88% PRINTED SOLDER COVERAGE BY AREA
 SCALE: 60X

4215302/E 12/2016

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI 均以“原样”提供技术性 & 可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用 TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的 TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及 TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它 TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对 TI 及其代表造成的损害。

TI 所提供产品均受 TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及 [ti.com.cn](http://www.ti.com.cn) 上或随附 TI 产品提供的其他可适用条款的约束。TI 提供所述资源并不扩展或以其他方式更改 TI 针对 TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2020 德州仪器半导体技术（上海）有限公司