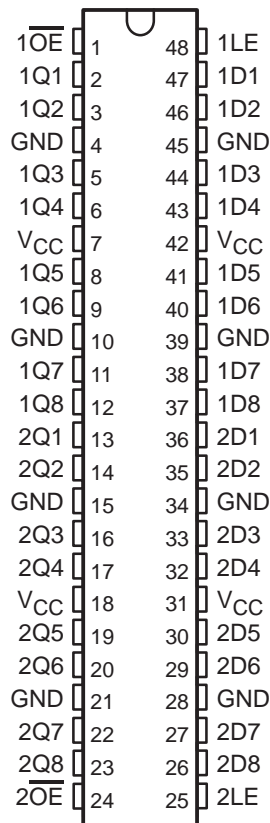


# SN54ABT16373A, SN74ABT16373A 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS160C – DECEMBER 1992 – REVISED MAY 1997

- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54ABT16373A . . . WD PACKAGE  
SN74ABT16373A . . . DGG OR DL PACKAGE  
(TOP VIEW)



## description

The 'ABT16373A are 16-bit transparent D-type latches with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16373A is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT16373A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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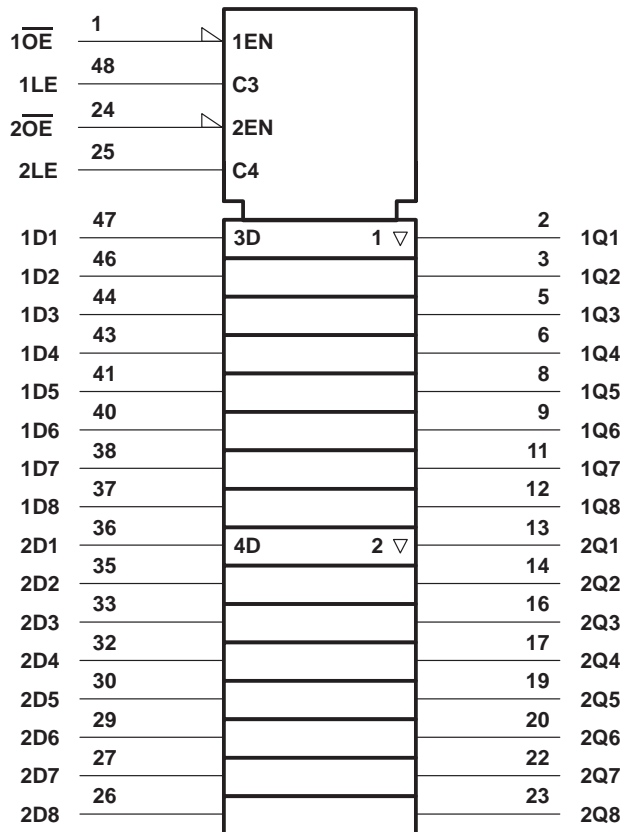
# SN54ABT16373A, SN74ABT16373A 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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FUNCTION TABLE  
(each 8-bit section)

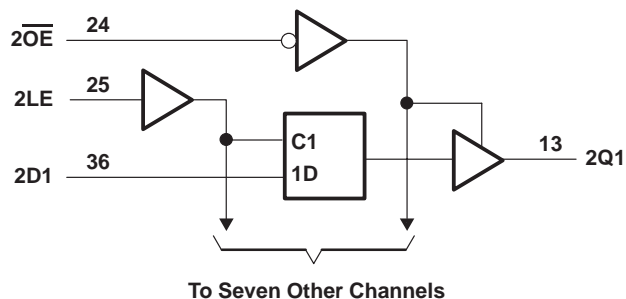
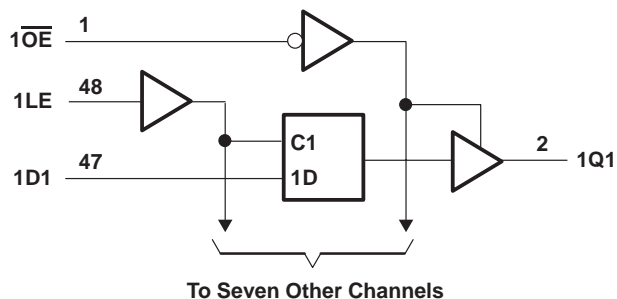
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



# SN54ABT16373A, SN74ABT16373A 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ .....	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT16373A .....	96 mA
SN74ABT16373A .....	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package .....	89°C/W
DL package .....	94°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

## recommended operating conditions (see Note 3)

		SN54ABT16373A		SN74ABT16373A		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



# SN54ABT16373A, SN74ABT16373A

## 16-BIT TRANSPARENT D-TYPE LATCHES

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABT16373A		SN74ABT16373A		UNIT		
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX			
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V		
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA			2.5		2.5		2.5	V		
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA			3		3		3			
	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -24 mA			2		2			2	
I <sub>OH</sub> = -32 mA				2*							
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA				0.55		0.55	V		
		I <sub>OL</sub> = 64 mA				0.55*		0.55			
V <sub>hys</sub>				100					mV		
I <sub>I</sub>	V <sub>CC</sub> = 0 to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND					±1		±1	μA		
I <sub>OZPU</sub> ‡	V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$					±50		±50	μA		
I <sub>OZPD</sub> ‡	V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$					±50		±50	μA		
I <sub>OZH</sub>	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 2.7 V, $\overline{OE} \geq 2$ V					10		10	μA		
I <sub>OZL</sub>	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 0.5 V, $\overline{OE} \geq 2$ V					-10		-10	μA		
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V					±100		±100	μA		
I <sub>CEX</sub>	Outputs high	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V				50		50	μA		
I <sub>O</sub> §		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V				-50	-100	-180	-50	-180	mA
I <sub>CC</sub>	Outputs high	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND				2		2	2	mA	
	Outputs low					85		85	85		
	Outputs disabled					2		2	2		
ΔI <sub>CC</sub> ¶		V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND				1.5		1.5	1.5	mA	
C <sub>i</sub>		V <sub>I</sub> = 2.5 V or 0.5 V				3.5				pF	
C <sub>o</sub>		V <sub>O</sub> = 2.5 V or 0.5 V				9.5				pF	

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ This parameter is characterized, but not production tested.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C#		SN54ABT16373A		SN74ABT16373A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high	3.3		3.3		3.3		ns
t <sub>su</sub>	Setup time, data before LE↓	1.5		2.4		1.5		ns
t <sub>h</sub>	Hold time, data after LE↓	1		2.2		1		ns

# These values apply only to the SN74ABT16373A.



**SN54ABT16373A, SN74ABT16373A**  
**16-BIT TRANSPARENT D-TYPE LATCHES**  
**WITH 3-STATE OUTPUTS**

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT16373A					UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN	MAX		
			MIN	TYP	MAX				
$t_{PLH}$	D	Q	1.4	3.7	5.3	1.4	6.5	ns	
$t_{PHL}$			2	4	5.4	2	6.5		
$t_{PLH}$	LE	Q	1.7	4.1	5.7	1.7	7	ns	
$t_{PHL}$			2.3	4.3	5.6	2.3	6.3		
$t_{PZH}$	$\overline{OE}$	Q	1.1	3.4	5	1.1	6.4	ns	
$t_{PZL}$			1.5	3.5	4.9	1.5	5.8		
$t_{PHZ}$	$\overline{OE}$	Q	2.4	5.1	7.1	2.4	8.3	ns	
$t_{PLZ}$			1.6	4.4	6.3	1.6	8		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT16373A					UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN	MAX		
			MIN	TYP	MAX				
$t_{PLH}$	D	Q	1.4	3.7	5.3	1.4	6.3	ns	
$t_{PHL}$			2	4	5.4	2	6.2		
$t_{PLH}$	LE	Q	1.7	4.1	5.7	1.7	6.7	ns	
$t_{PHL}$			2.3	4.3	5.6	2.3	6.1		
$t_{PZH}$	$\overline{OE}$	Q	1.1	3.4	5	1.1	6.1	ns	
$t_{PZL}$			1.5	3.5	4.9	1.5	5.6		
$t_{PHZ}$	$\overline{OE}$	Q	2.4	5.1	7.1	2.4	8.1	ns	
$t_{PLZ}$			1.6	4.4	5.8	1.6	6.5		

# SN54ABT16373A, SN74ABT16373A 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS160C – DECEMBER 1992 – REVISED MAY 1997

## PARAMETER MEASUREMENT INFORMATION

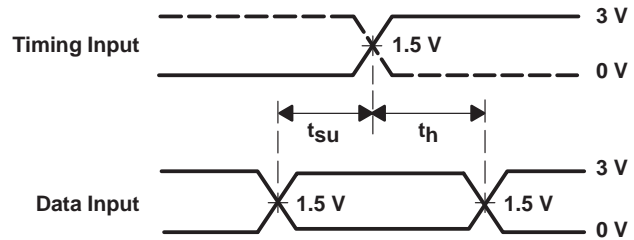


LOAD CIRCUIT

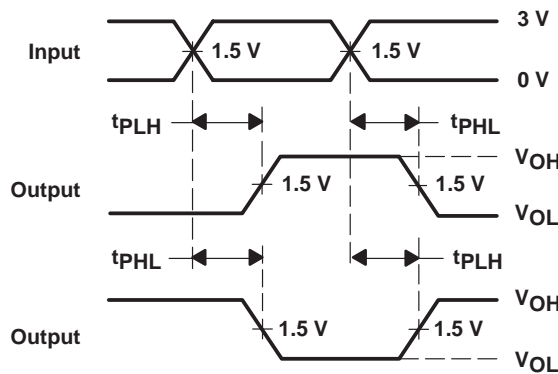
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



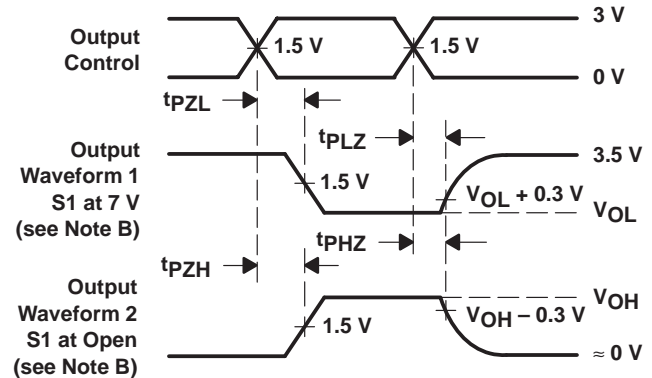
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9320001QXA	ACTIVE	CFP	WD	48	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9320001QX A SNJ54ABT16373A WD	<a href="#">Samples</a>
74ABT16373ADGGRE4	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A	<a href="#">Samples</a>
74ABT16373ADGGRG4	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A	<a href="#">Samples</a>
SN74ABT16373ADGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A	<a href="#">Samples</a>
SN74ABT16373ADL	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A	<a href="#">Samples</a>
SN74ABT16373ADLR	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A	<a href="#">Samples</a>
SN74ABT16373ADLRG4	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A	<a href="#">Samples</a>
SNJ54ABT16373AWD	ACTIVE	CFP	WD	48	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9320001QX A SNJ54ABT16373A WD	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54ABT16373A, SN74ABT16373A :**

- Catalog : [SN74ABT16373A](#)
- Enhanced Product : [SN74ABT16373A-EP](#), [SN74ABT16373A-EP](#)
- Military : [SN54ABT16373A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16373ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74ABT16373ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16373ADGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74ABT16373ADLR	SSOP	DL	48	1000	367.0	367.0	55.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ABT16373ADL	DL	SSOP	48	25	473.7	14.24	5110	7.87

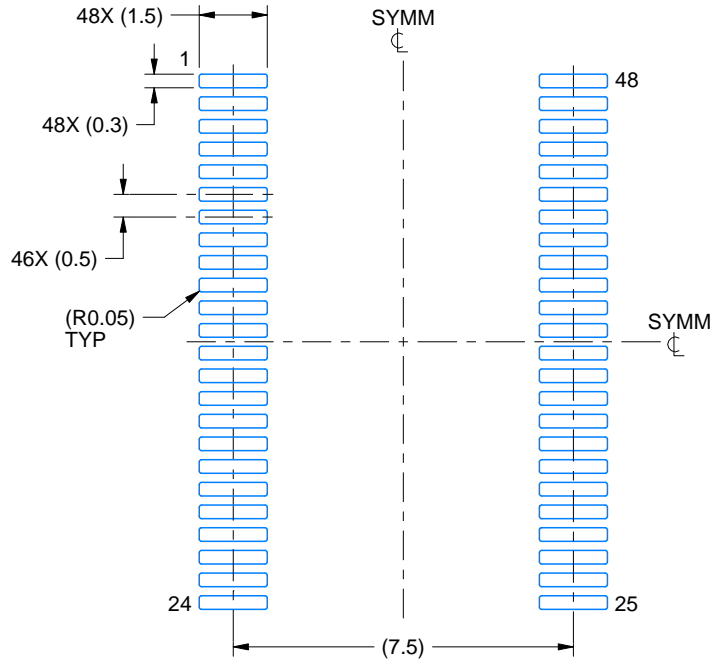


# EXAMPLE BOARD LAYOUT

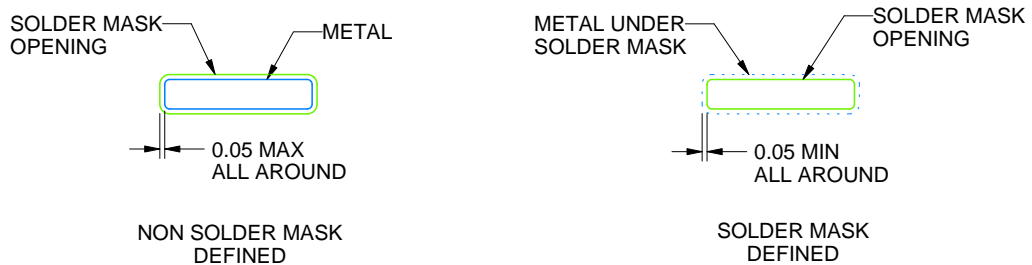
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

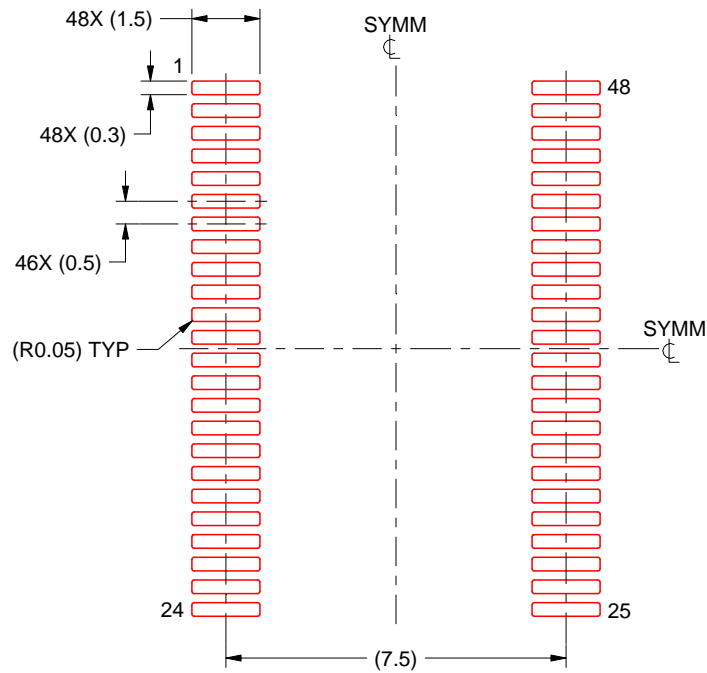
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

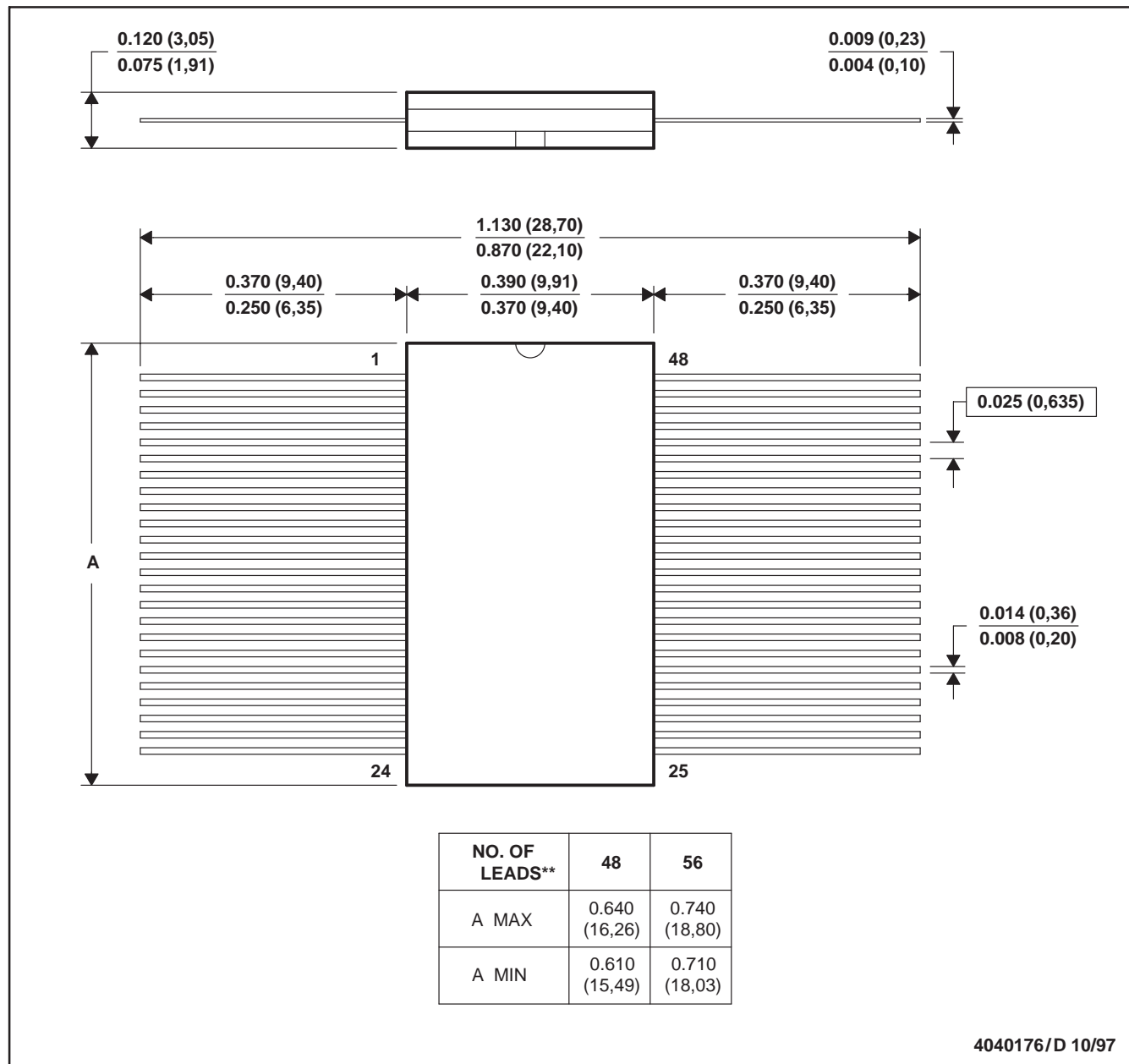


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

WD (R-GDFP-F\*\*)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN

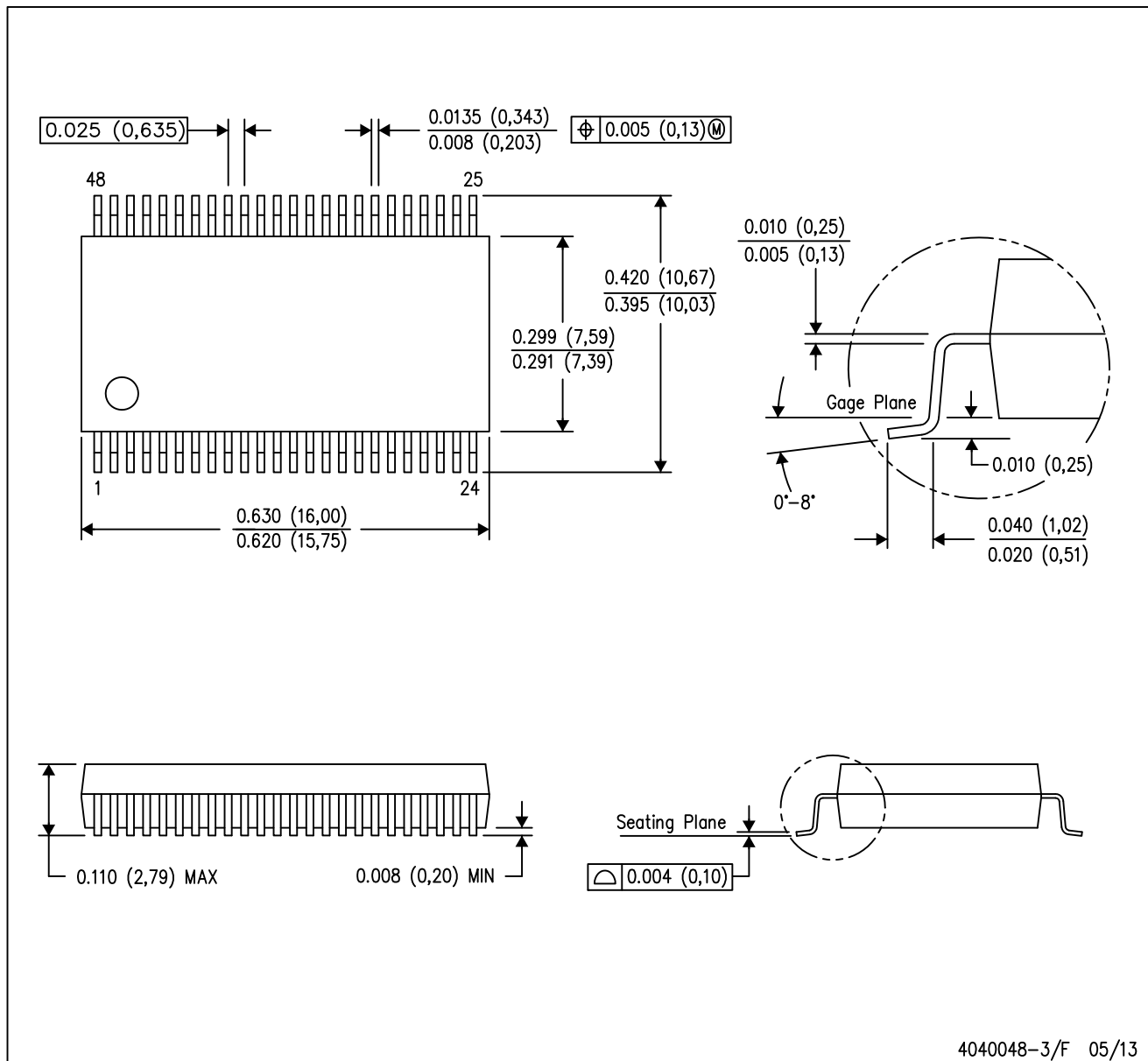


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only  
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA  
 GDFP1-F56 and JEDEC MO-146AB

# MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

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