# ±1°C Remote and Local Temperature Sensor With N-Factor and Series Resistance Correction

**Check for Samples: TMP411-Q1**

## FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified With the Following Results**
  - **Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C4B**
- **±1°C Remote Diode Sensor**
- **±1°C Local Temperature Sensor**
- **Programmable Non-Ideality Factor**
- **Series Resistance Cancellation**
- **Alert Function**
- **Programmable Resolution: 9 to 12 Bits**
- **Programmable Threshold Limits**
- **Two-Wire/ SMBus™ Serial Interface**
- **Minimum and Maximum Temperature Monitors**
- **Multiple Interface Addresses**
- **$\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$ Pin Configuration**
- **Diode Fault Detection**

## APPLICATIONS

- **Automotive**

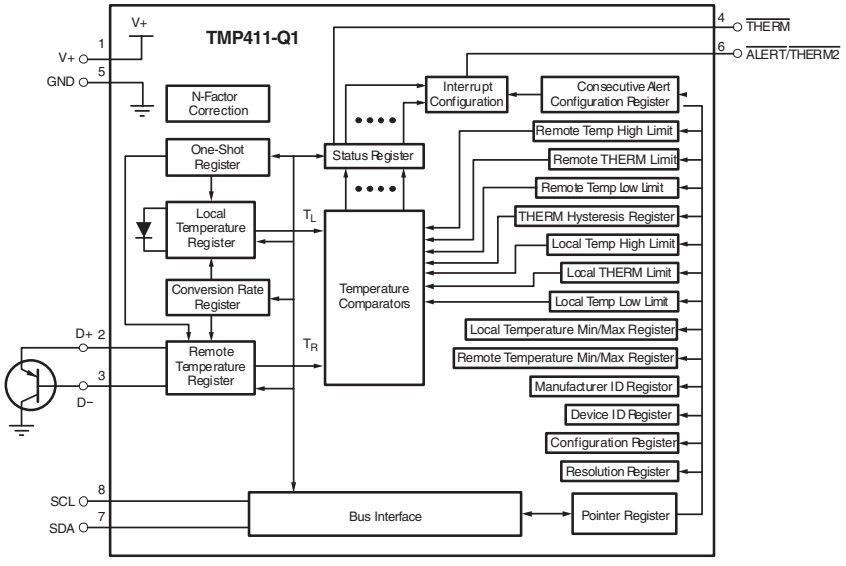
## DESCRIPTION

The TMP411-Q1 is a remote temperature sensor monitor with a built-in local temperature sensor. The remote temperature-sensor diode-connected transistors are typically low-cost, NPN- or PNP-type transistors or diodes that are an integral part of microcontrollers, microprocessors, or FPGAs.

Remote accuracy is ±1°C for multiple IC manufacturers, with no calibration needed. The two-wire serial interface accepts SMBus write byte, read byte, send byte, and receive byte commands to program the alarm thresholds and to read temperature data.

Features that are included in the TMP411-Q1 are: series resistance cancellation, programmable non-ideality factor, programmable resolution, programmable threshold limits, minimum and maximum temperature monitors, wide remote temperature measurement range (up to 150°C), diode fault detection, and temperature alert function.

The TMP411-Q1 is available in an VSSOP-8 package.




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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

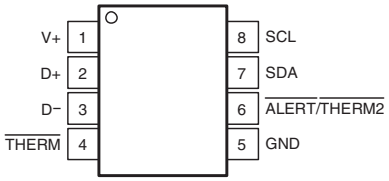
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## Table 1. ORDERING INFORMATION(1)

| ORDERABLE PART NUMBER | $I^2C$ ADDRESS | DEFAULT LOCAL HIGH TEMPERATURE LIMIT | DEFAULT REMOTE HIGH TEMPERATURE LIMIT | DEFAULT TEMPERATURE RANGE |
|---|---|---|---|---|
| TMP411AQDGKRQ1 | 100 1100 | +85°C | +85°C | Standard |
| TMP411BQDGKRQ1 | 100 1101 | +85°C | +85°C | Standard |
| TMP411CQDGKRQ1 | 100 1110 | +85°C | +85°C | Standard |
| TMP411DQDGKRQ1 | 100 1100 | +110°C | +110°C | Standard |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

**VSSOP PACKAGE**
**(TOP VIEW)**




## PIN ASSIGNMENTS

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | V+ | Positive supply (2.7 V to 5.5 V) |
| 2 | D+ | Positive connection to remote temperature sensor |
| 3 | D− | Negative connection to remote temperature sensor |
| 4 | $\overline{\text{THERM}}$ | Thermal flag, active-low, open-drain; requires pullup resistor to V+ |
| 5 | GND | Ground |
| 6 | $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ | Alert (reconfigurable as second thermal flag), active-low, open-drain; requires pullup resistor to V+ |
| 7 | SDA | Serial data line for SMBus, open-drain; requires pullup resistor to V+ |
| 8 | SCL | Serial clock line for SMBus, open-drain; requires pullup resistor to V+ |


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## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| Power supply, $V_S$ | | 7 | V |
| Input voltage | Pins 2, 3, 4 only | –0.5 V to $V_S$ + 0.5 | V |
| Input voltage | Pins 6, 7, 8 only | −0. 5 V to 7 | V |
| Input current | | 10 | mA |
| Operating temperature range | | −55°C to 127 | °C |
| Storage temperature range | | –60°C to 130 | °C |
| Junction temperature ($T_J$ max) | | 150 | °C |
| ESD rating | Human-body model (HBM) AEC-Q100 Classification Level H2 | 2 | kV |
| | Charged-device model (CDM) AEC-Q100 Classification Level C4B | 750 | V |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may degrade device reliability.

## ELECTRICAL CHARACTERISTICS

at $T_A$ = −40°C to +125°C and $V_S$ = 2.7V to 5.5V, unless otherwise noted.

| PARAMETERS | | | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **Temperature Error** | | | | | | | | |
| $TE_{LOCAL}$ | Local temperature sensor | | $T_A$ = −40°C to 125°C | | | ±1.25 | ±2.5 | °C |
| $TE_{REMOTE}$ | Remote temperature sensor(1) | | $T_A$ = 15°C to 85°C, $V_S$ = 3.3 V | | | ±0.0625 | ±1 | °C |
| | | | $T_A$ = 15°C to 75°C, | $T_{DIODE}$ = −40°C to 150°C, $V_S$ = 3.3 V | | ±0.0625 | ±1 | °C |
| | | | $T_A$ = −40°C to 100°C, | | | ±1 | ±3 | °C |
| | | | $T_A$ = −40°C to 125°C, | | | ±3 | ±5 | °C |
| | vs supply | Local/remote | $V_S$ = 2.7 V to 5.5 V | | | ±0.2 | ±0.5 | °C/V |
| **Temperature Measurement** | | | | | | | | |
| | Conversion time (per channel) | | One-shot mode | | 105 | 115 | 125 | ms |
| | Resolution | | | | | | | |
| | Local temperature sensor (programmable) | | | | 9 | | 12 | Bits |
| | Remote temperature sensor | | | | | 12 | | Bits |
| | Remote Sensor Source Currents | High | Series resistance 3 kΩ max. | | | 120 | | µA |
| | | Medium high | | | | 60 | | µA |
| | | Medium low | | | | 12 | | µA |
| | | Low | | | | 6 | | µA |
| η | Remote transistor ideality factor | | Optimized ideality factor | | | 1.008 | | |
| **SMBus Interface** | | | | | | | | |
| $V_{IH}$ | Logic input high voltage (SCL, SDA) | | | | 2.1 | | | V |
| $V_{IL}$ | Logic Input low voltage (SCL, SDA) | | | | | | 0.8 | V |
| | Hysteresis | | | | | | 500 | mV |
| | SMBus output low sink current | | | | 6 | | | mA |
| | Logic input current | | | | −1 | | 1 | µA |
| | SMBus input capacitance (SCL, SDA) | | | | | 3 | | pF |
| | SMBus clock frequency | | | | | | 3.4 | MHz |
| | SMBus timeout | | | | 25 | 30 | 35 | ms |

(1) Tested with less than 5-Ω effective series resistance and 100-pF differential input capacitance. $T_A$ is the ambient temperature of the TMP411-Q1. $T_{DIODE}$ is the temperature at the remote diode sensor.

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## ELECTRICAL CHARACTERISTICS (continued)

at $T_A$ = −40°C to +125°C and $V_S$ = 2.7V to 5.5V, unless otherwise noted.

| PARAMETERS | | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| | SCL falling edge to SDA valid time | | | | 1 | µs |
| **Digital Outputs** | | | | | | |
| $V_{OL}$ | Output low voltage | $I_{OUT}$ = 6 mA | | 0.15 | 0.4 | V |
| $I_{OH}$ | High-level output leakage current<br>ALERT/THERM2 Output low sink current | $V_{OUT} = V_S$<br>ALERT/THERM2 forced to 0.4 V | | 0.1 | 1 | µA |
| | $\overline{\text{THERM}}$ output low sink current | $\overline{\text{THERM}}$ forced to 0.4 V | 6 | | | mA |


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## ELECTRICAL CHARACTERISTICS (continued)

at $T_A$ = −40°C to +125°C and $V_S$ = 2.7V to 5.5V, unless otherwise noted.

| PARAMETERS | | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| $V_S$ | Specified voltage range | | 2.7 | | 5.5 | V |
| $I_Q$ | Quiescent current | 0.0625 conversions per second, $V_S$ = 3.3 V | | 28 | 30 | µA |
| | | Eight conversions per second, $V_S$ = 3.3 V | | 400 | 475 | µA |
| | | Serial bus inactive, shutdown mode | | 3 | 10 | µA |
| | | Serial bus active, $f_S$ = 400 kHz, shutdown mode | | 90 | | µA |
| | | Serial bus active, $f_S$ = 3.4 MHz, shutdown mode | | 350 | | µA |
| | Undervoltage lockout | | 2.3 | 2.4 | 2.6 | V |
| POR | Power-on-reset threshold | | | 1.6 | 2.3 | V |
| **Temperature Range** | | | | | | |
| | Specified range | | −40 | | 125 | °C |
| $T_{stg}$ | Storage range | | −60 | | 130 | °C |
| | Thermal resistance. VSSOP-8 | | | 150 | | °C/W |

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## TYPICAL CHARACTERISTICS

At $T_A$ = 25°C and $V_S$ = 5 V, unless otherwise noted.

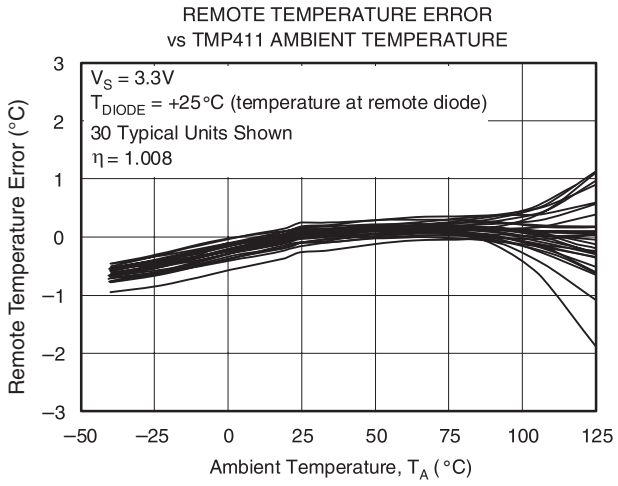



**Figure 1.**

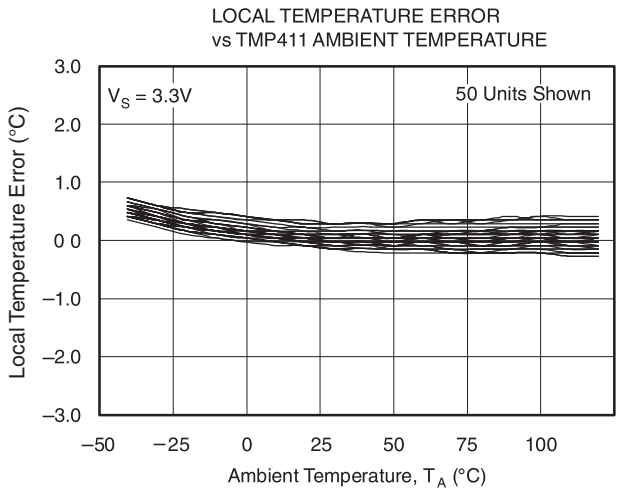



**Figure 2.**

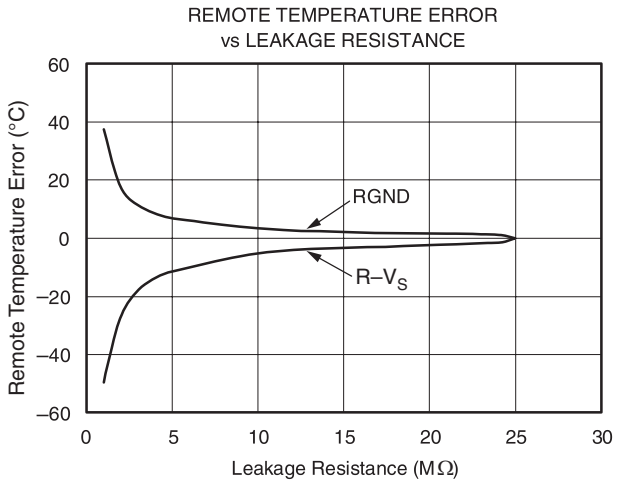



**Figure 3.**

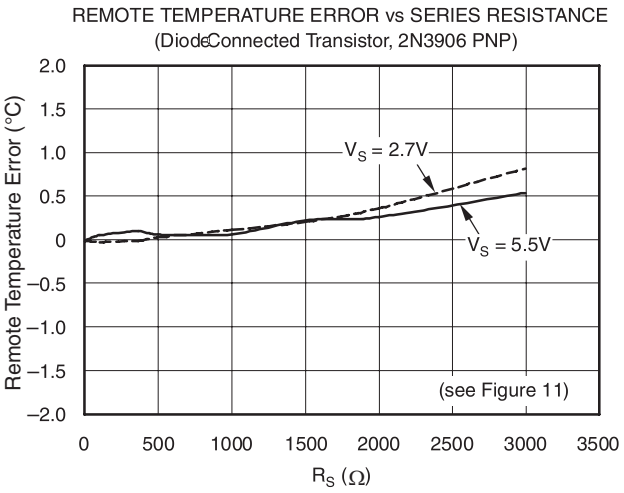



**Figure 4.**

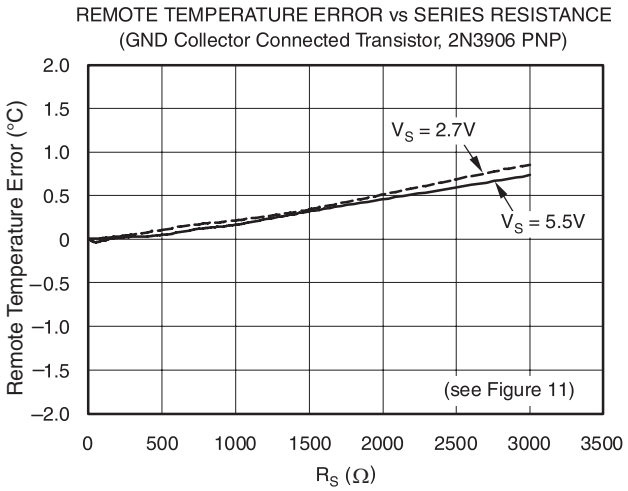



**Figure 5.**

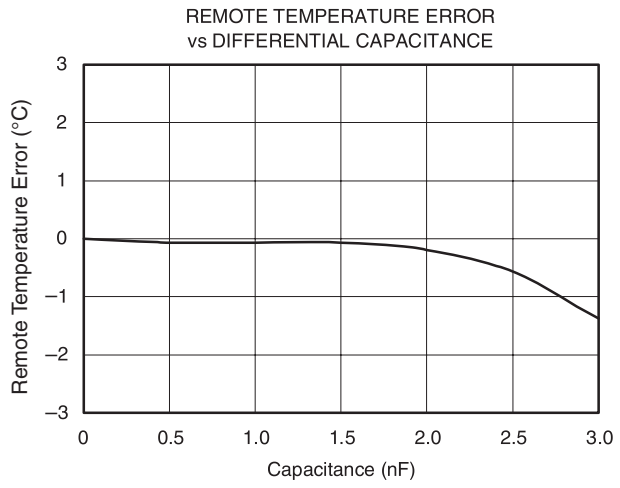



**Figure 6.**


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## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = 25°C and $V_S$ = 5 V, unless otherwise noted.

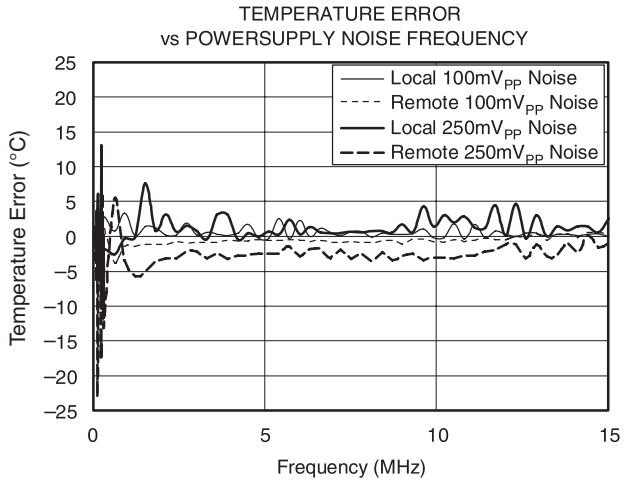



**Figure 7.**

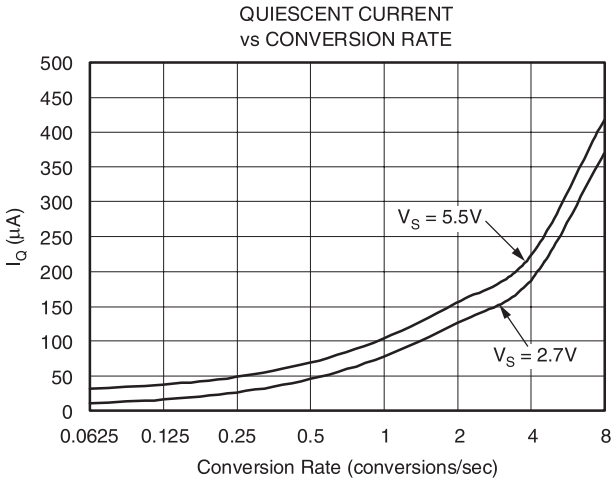



**Figure 8.**

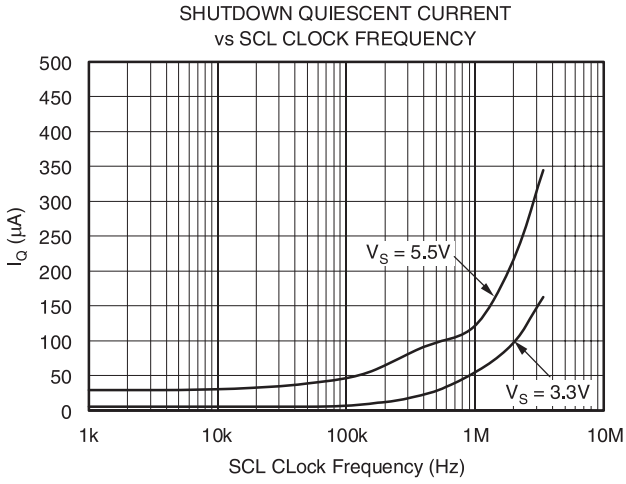



**Figure 9.**

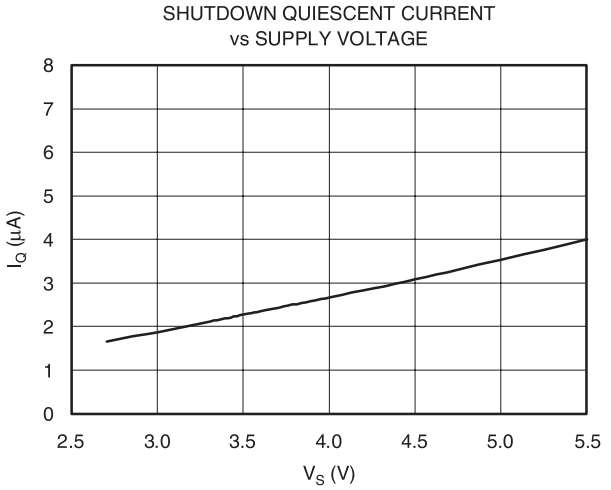


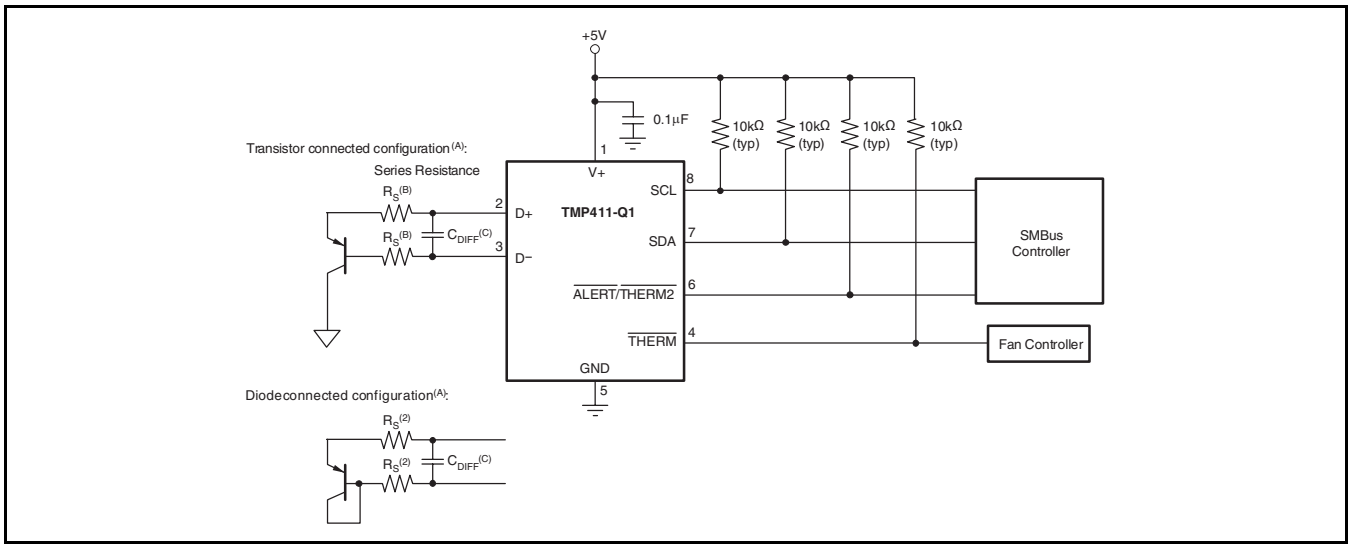

**Figure 10.**

## APPLICATION INFORMATION

The TMP411-Q1 is a dual-channel digital temperature sensor that combines a local die-temperature measurement channel and a remote junction-temperature measurement channel in a single VSSOP-8 package. The TMP411-Q1 is two-wire- and SMBus interface-compatible and is specified over an ambient temperature range of −40°C to 125°C. The TMP411-Q1 contains multiple registers for holding configuration information, temperature measurement results, temperature comparator maximum/minimum limits, and status information.

User-programmed high- and low-temperature limits stored in the TMP411-Q1 can be used to trigger an over- or undertemperature alarm (ALERT) on local and remote temperatures. Additional thermal limits can be programmed into the TMP411-Q1 and used to trigger another flag (THERM) that can be used to initiate a system response to rising temperatures.

The TMP411-Q1 requires only a transistor connected between D+ and D− for proper remote temperature-sensing operation. The SCL and SDA interface pins require pullup resistors as part of the communication bus, whereas ALERT and THERM are open-drain outputs that also need pullup resistors. ALERT and THERM may be shared with other devices if desired for a wired-OR implementation. A 0.1-µF power-supply bypass capacitor is recommended for good local bypassing. Figure 11 shows a typical configuration for the TMP411-Q1.




A. Diode−connected configuration provides better settling time. Transistor−connected configuration provides better series resistance cancellation.

B. $R_S$ (optional) should be <1.5 kΩ in most applications. Selection of RS depends on specific application; see Filtering section.

C. $C_{DIFF}$ (optional) should be <1000 pF in most applications. Selection of $C_{DIFF}$ depends on specific application; see Filtering section and Figure 6, *Remote Temperature Error vs Differential Capacitance*.

**Figure 11. Basic Connections**


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## SERIES RESISTANCE CANCELLATION

Series resistance in an application circuit that typically results from printed circuit board (PCB) trace resistance and remote line length (see Figure 11) is automatically cancelled by the TMP411-Q1, preventing what would otherwise result in a temperature offset.

A total of up to 3 kΩ of series line resistance is cancelled by the TMP411-Q1, eliminating the need for additional characterization and temperature offset correction.

See the two Remote Temperature Error vs Series Resistance typical characteristics curves (Figure 4 and Figure 5) for details on the effect of series resistance and power-supply voltage on sensed remote temperature error.

## DIFFERENTIAL INPUT CAPACITANCE

The TMP411-Q1 tolerates differential input capacitance of up to 1000 pF with minimal change in temperature error. The effect of capacitance on sensed remote temperature error is illustrated in typical characteristic Remote Temperature Error vs Differential Capacitance (Figure 6).

## TEMPERATURE MEASUREMENT DATA

Temperature measurement data are taken over a default range of 0°C to 127°C for both local and remote locations. Measurements from –55°C to 150°C can be made both locally and remotely by reconfiguring the TMP411-Q1 for the extended temperature range. To change the TMP411-Q1 configuration from the standard to the extended temperature range, switch bit 2 (RANGE) of the Configuration Register from low to high.

Temperature data resulting from conversions within the default measurement range are represented in binary form, as shown in Table 2, Standard Binary column. Note that any temperature below 0°C results in a data value of zero (00h). Likewise, temperatures above 127°C result in a value of 127 (7Fh). The device can be set to measure over an extended temperature range by changing bit 2 of the Configuration Register from low to high. The change in measurement range and data format from standard binary to extended binary occurs at the next temperature conversion. For data captured in the extended temperature range configuration, an offset of 64 (40h) is added to the standard binary value, as shown in Table 1, Extended Binary column. This configuration allows measurement of temperatures below 0°C. Note that binary values corresponding to temperatures as low as –64°C, and as high as 191°C are possible; however, most temperature-sensing diodes only measure with the range of –55°C to 150°C. Additionally, the TMP411-Q1 is rated only for ambient local temperatures ranging from –40°C to 125°C. Parameters in the Absolute Maximum Ratings table must be observed.

**Table 2. Temperature Data Format (Local and Remote Temperature High Bytes)**

| TEMP (°C) | LOCAL/REMOTE TEMPERATURE REGISTER HIGH BYTE VALUE (1°C RESOLUTION) | | | |
|---|---|---|---|---|
| | STANDARD BINARY | | EXTENDED BINARY | |
| | BINARY | HEX | BINARY | HEX |
| −64 | 0000 0000 | 00 | 0000 0000 | 00 |
| −50 | 0000 0000 | 00 | 0000 1110 | 0E |
| −25 | 0000 0000 | 00 | 0010 0111 | 27 |
| 0 | 0000 0000 | 00 | 0100 0000 | 40 |
| 1 | 0000 0001 | 01 | 0100 0001 | 41 |
| 5 | 0000 0101 | 05 | 0100 0101 | 45 |
| 10 | 0000 1010 | 0A | 0100 1010 | 4A |
| 25 | 0001 1001 | 19 | 0101 1001 | 59 |
| 50 | 0011 0010 | 32 | 0111 0010 | 72 |
| 75 | 0100 1011 | 4B | 1000 1011 | 8b |
| 100 | 0110 0100 | 64 | 1010 0100 | A4 |
| 125 | 0111 1101 | 7D | 1011 1101 | BD |
| 127 | 0111 1111 | 7F | 1011 1111 | BF |
| 150 | 0111 1111 | 7F | 1101 0110 | D6 |

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**Table 2. Temperature Data Format (Local and Remote Temperature High Bytes) (continued)**

| TEMP (°C) | LOCAL/REMOTE TEMPERATURE REGISTER HIGH BYTE VALUE (1°C RESOLUTION) | | | |
|---|---|---|---|---|
| | STANDARD BINARY | | EXTENDED BINARY | |
| | BINARY | HEX | BINARY | HEX |
| 175 | 0111 1111 | 7F | 1110 1111 | EF |
| 191 | 0111 1111 | 7F | 1111 1111 | FF |

**NOTE**

Whenever changing between standard and extended temperature ranges, be aware that the temperatures stored in the temperature limit registers are NOT automatically reformatted to correspond to the new temperature range format. These temperature limit values must be reprogrammed in the appropriate binary or extended binary format.

Both local and remote temperature data use two bytes for data storage. The high byte stores the temperature with 1°C resolution. The second or low byte stores the decimal fraction value of the temperature and allows a higher measurement resolution; see Table 3. The measurement resolution for the remote channel is 0.0625°C, and is not adjustable. The measurement resolution for the local channel is adjustable; it can be set for 0.5°C, 0.25°C, 0.125°C, or 0.0625°C by setting the RES1 and RES0 bits of the Resolution Register; see the Resolution Register section.


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**Table 3. Decimal Fraction Temperature Data Format (Local and Remote Temperature Low Bytes)**

| TEMP (°C) | REMOTE TEMPERATURE REGISTER LOW BYTE VALUE | | LOCAL TEMPERATURE REGISTER LOW BYTE VALUE | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 0.0625°C RESOLUTION | | 0.5°C RESOLUTION | | 0.25°C RESOLUTION | | 0.125°C RESOLUTION | | 0.0625°C RESOLUTION | |
| | STANDARD AND EXTENDED BINARY | HEX | STANDARD AND EXTENDED BINARY | HEX | STANDARD AND EXTENDED BINARY | HEX | STANDARD AND EXTENDED BINARY | HEX | STANDARD AND EXTENDED BINARY | HEX |
| 0.0000 | 0000 0000 | 00 | 0000 0000 | 00 | 0000 0000 | 00 | 0000 0000 | 00 | 0000 0000 | 00 |
| 0.0625 | 0001 0000 | 10 | 0000 0000 | 00 | 0000 0000 | 00 | 0000 0000 | 00 | 0001 0000 | 10 |
| 0.1250 | 0010 0000 | 20 | 0000 0000 | 00 | 0000 0000 | 00 | 0010 0000 | 20 | 0010 0000 | 20 |
| 0.1875 | 0011 0000 | 30 | 0000 0000 | 00 | 0000 0000 | 00 | 0010 0000 | 20 | 0011 0000 | 30 |
| 0.2500 | 0100 0000 | 40 | 0000 0000 | 00 | 0100 0000 | 40 | 0100 0000 | 40 | 0100 0000 | 40 |
| 0.3125 | 0101 0000 | 50 | 0000 0000 | 00 | 0100 0000 | 40 | 0100 0000 | 40 | 0101 0000 | 50 |
| 0.3750 | 0110 0000 | 60 | 0000 0000 | 00 | 0100 0000 | 40 | 0110 0000 | 60 | 0110 0000 | 60 |
| 0.4375 | 0111 0000 | 70 | 0000 0000 | 00 | 0100 0000 | 40 | 0110 0000 | 60 | 0111 0000 | 70 |
| 0.5000 | 1000 0000 | 80 | 1000 0000 | 80 | 1000 0000 | 80 | 1000 0000 | 80 | 1000 0000 | 80 |
| 0.5625 | 1001 0000 | 90 | 1000 0000 | 80 | 1000 0000 | 80 | 1000 0000 | 80 | 1001 0000 | 90 |
| 0.6250 | 1010 0000 | A0 | 1000 0000 | 80 | 1000 0000 | 80 | 1010 0000 | A0 | 1010 0000 | A0 |
| 0.6875 | 1011 0000 | B0 | 1000 0000 | 80 | 1000 0000 | 80 | 1010 0000 | A0 | 1011 0000 | B0 |
| 0.7500 | 1100 0000 | C0 | 1000 0000 | 80 | 1100 0000 | C0 | 1100 0000 | C0 | 1100 0000 | C0 |
| 0.8125 | 1101 0000 | D0 | 1000 0000 | 80 | 1100 0000 | C0 | 1100 0000 | C0 | 1101 0000 | D0 |
| 0.8750 | 1110 0000 | E0 | 1000 0000 | 80 | 1100 0000 | C0 | 1110 0000 | E0 | 1110 0000 | E0 |
| 0.9375 | 1111 0000 | F0 | 1000 0000 | 80 | 1100 0000 | C0 | 1110 0000 | E0 | 1111 0000 | F0 |

## REGISTER INFORMATION

The TMP411-Q1 contains multiple registers for holding configuration information, temperature measurement results, temperature comparator maximum and minimum, limits, and status information. These registers are described in Figure 12 and Table 4.

## POINTER REGISTER

Figure 12 shows the internal register structure of the TMP411-Q1. The 8-bit Pointer Register is used to address a given data register. The Pointer Register identifies which of the data registers should respond to a read or write command on the two-wire bus. This register is set with every write command. A write command must be issued to set the proper value in the Pointer Register before executing a read command. Table 4 describes the pointer address of the registers available in the TMP411-Q1. Please note read pointer address 0x05, 0x07, 0x19, and 0x20 have different power-on-reset values for A, B, C vs D. The power-on-reset (POR) value of the Pointer Register is 00h (0000 0000b).

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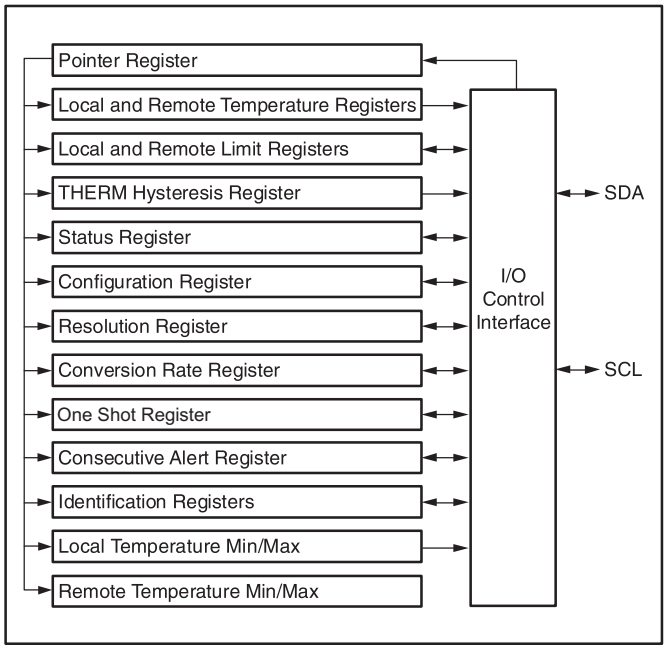



**Figure 12. Internal Register Structure**

**Table 4. Register Map**

| POINTER ADDRESS (HEX) | | POWER-ON RESET (HEX) FOR A,B, AND C | POWER-ON RESET (HEX) FOR D | BIT DESCRIPTIONS | | | | | | | | REGISTER DESCRIPTIONS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| READ | WRITE | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 00 | NA(1) | 00 | 00 | LT11 | LT10 | LT9 | LT8 | LT7 | LT6 | LT5 | LT4 | Local Temperature (High Byte) |
| 01 | NA | 00 | 00 | RT11 | RT10 | RT9 | RT8 | RT7 | RT6 | RT5 | RT4 | Remote Temperature (High Byte) |
| 02 | NA | XX | XX | BUSY | LHIGH | LLOW | RHIGH | RLOW | OPEN | RTHRM | LTHRM | Status Register |
| 03 | 09 | 00 | 00 | MASK1 | SD | AL/TH | 0 | 0 | RANGE | 0 | 0 | Configuration Register |
| 04 | 0A | 08 | 08 | 0 | 0 | 0 | 0 | R3 | R2 | R1 | R0 | Conversion Rate Register |
| 05 | 0B | 55 | 6E | LTH11 | LTH10 | LTH9 | LTH8 | LTH7 | LTH6 | LTH5 | LTH4 | Local Temperature High Limit (High Byte) |
| 06 | 0C | 00 | 00 | LTL11 | LTL10 | LTL9 | LTL8 | LTL7 | LTL6 | LTL5 | LTL4 | Local Temperature Low Limit (High Byte) |
| 07 | 0D | 55 | 6E | RTH11 | RTH10 | RTH9 | RTH8 | RTH7 | RTH6 | RTH5 | RTH4 | Remote Temperature High Limit (High Byte) |
| 08 | 0E | 00 | 00 | RTL11 | RTL10 | RTL9 | RTL8 | RTL7 | RTL6 | RTL5 | RTL4 | Remote Temperature Low Limit (High Byte) |
| NA | 0F | XX | XX | X(2) | X | X | X | X | X | X | X | One-Shot Start |
| 10 | NA | 00 | 00 | RT3 | RT2 | RT1 | RT0 | 0 | 0 | 0 | 0 | Remote Temperature (Low Byte) |
| 13 | 13 | 00 | 00 | RTH3 | RTH2 | RTH1 | RTH0 | 0 | 0 | 0 | 0 | Remote Temperature High Limit (Low Byte) |
| 14 | 14 | 00 | 00 | RTL3 | RTL2 | RTL1 | RTL0 | 0 | 0 | 0 | 0 | Remote Temperature Low Limit (Low Byte) |
| 15 | NA | 00 | 00 | LT3 | LT2 | LT1 | LT0 | 0 | 0 | 0 | 0 | Local Temperature (Low Byte) |
| 16 | 16 | 00 | 00 | LTH3 | LTH2 | LTH1 | LTH0 | 0 | 0 | 0 | 0 | Local Temperature High Limit (Low Byte) |
| 17 | 17 | 00 | 00 | LTL3 | LTL2 | LTL1 | LTL0 | 0 | 0 | 0 | 0 | Local Temperature Low Limit (Low Byte) |
| 18 | 18 | 00 | 00 | NC7 | NC6 | NC5 | NC4 | NC3 | NC2 | NC1 | NC0 | N-factor Correction |
| 19 | 19 | 55 | 6E | RTHL11 | RTHL10 | RTHL9 | RTHL8 | RTHL7 | RTHL6 | RTHL5 | RTHL4 | Remote $\overline{\text{THERM}}$ Limit |
| 1A | 1A | 1C | 1C | 0 | 0 | 0 | 1 | 1 | 1 | RES1 | RES0 | Resolution Register |

(1) NA = not applicable; register is write- or read-only.


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**Table 4. Register Map (continued)**

| POINTER ADDRESS (HEX) | | POWER-ON RESET (HEX) FOR A,B, AND C | POWER-ON RESET (HEX) FOR D | BIT DESCRIPTIONS | | | | | | | | REGISTER DESCRIPTIONS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| READ | WRITE | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 20 | 20 | 55 | 6E | LTHL11 | LTHL10 | LTHL9 | LTHL8 | LTHL7 | LTHL6 | LTHL5 | LTHL4 | Local $\overline{\text{THERM}}$ Limit |
| 21 | 21 | 0A | 0A | TH11 | TH10 | TH9 | TH8 | TH7 | TH6 | TH5 | TH4 | $\overline{\text{THERM}}$ Hysteresis |
| 22 | 22 | 81 | 81 | TO_EN | 0 | 0 | 0 | C2 | C1 | C0 | 0 | Consecutive Alert Register |
| 30 | 30 | FF | FF | LMT11 | LMT10 | LMT9 | LMT8 | LMT7 | LMT6 | LMT5 | LMT4 | Local Temperature Minimum (High Byte) |
| 31 | 31 | F0 | F0 | LMT3 | LMT2 | LMT1 | LMT0 | 0 | 0 | 0 | 0 | Local Temperature Minimum (Low Byte) |
| 32 | 32 | 00 | 00 | LXT11 | LXT10 | LXT9 | LXT8 | LXT7 | LXT6 | LXT5 | LXT4 | Local Temperature Maximum (High Byte) |
| 33 | 33 | 00 | 00 | LXT3 | LXT2 | LXT1 | LXT0 | 0 | 0 | 0 | 0 | Local Temperature Maximum (Low Byte) |
| 34 | 34 | FF | FF | RMT11 | RMT10 | RMT9 | RMT8 | RMT7 | RMT6 | RMT5 | RMT4 | Remote Temperature Minimum (High Byte) |
| 35 | 35 | F0 | F0 | RMT3 | RMT2 | RMT1 | RMT0 | 0 | 0 | 0 | 0 | Remote Temperature Minimum (Low Byte) |
| 36 | 36 | 00 | 00 | RXT11 | RXT10 | RXT9 | RXT8 | RXT7 | RXT6 | RXT5 | RXT4 | Remote Temperature Maximum (High Byte) |
| 37 | 37 | 00 | 00 | RXT3 | RXT2 | RXT1 | RXT0 | 0 | 0 | 0 | 0 | Remote Temperature Maximum (Low Byte) |
| NA | FC | XX | XX | X(2) | X | X | X | X | X | X | X | Software Reset |
| FE | NA | 55 | 55 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | Manufacturer ID |
| FF | NA | 12 | 12 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | Device ID for TMP411-Q1A |
| FF | NA | 13 | 13 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | Device ID for TMP411-Q1B |
| FF | NA | 10 | 10 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | Device ID for TMP411-Q1C |

(2) X = indeterminate state

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## TEMPERATURE REGISTERS

The TMP411-Q1 has four 8-bit registers that hold temperature measurement results. Both the local channel and the remote channel have a high-byte register that contains the most-significant bits (MSBs) of the temperature analog-to-digital converter (ADC) result and a low-byte register that contains the least-significant bits (LSBs) of the temperature ADC result. The local-channel high-byte address is 00h; the local-channel low-byte address is 15h. The remote-channel high byte is at address 01h; the remote-channel low-byte address is 10h. These registers are read-only and are updated by the ADC each time a temperature measurement is completed.

The TMP411-Q1 contains circuitry to assure that a low-byte register-read command returns data from the same ADC conversion as the immediately preceding high-byte read command. This assurance remains valid only until another register is read. For proper operation, the high byte of a temperature register should be read first. The low-byte register should be read in the next read command. The low byte register may be left unread if the LSBs are not needed. Alternatively, the temperature registers may be read as a 16-bit register by using a single two-byte read command from address 00h for the local-channel result or from address 01h for the remote-channel result. The high byte is output first, followed by the low byte. Both bytes of this read operation are from the same ADC conversion. The power-on-reset value of both temperature registers is 00h.

## LIMIT REGISTERS

The TMP411-Q1 has 11 registers for setting comparator limits for both the local and remote measurement channels. These registers have read and write capability. The High and Low Limit Registers for both channels span two registers, as do the temperature registers. The local-temperature high limit is set by writing the high byte to pointer address 0Bh and writing the low byte to pointer address 16h, or by using a single two-byte write command (high byte first) to pointer address 0Bh. The local-temperature high limit is obtained by reading the high byte from pointer address 05h and the low byte from pointer address 16h or by using a two-byte read command from pointer address 05h. The power-on-reset value of the local temperature high limit is 55h/6Eh/00h (85°C in standard temperature mode for TMP411A-Q1 to TMP411C-Q1; 110°C in standard temperature mode for TMP411D-Q1, 21°C in extended temperature range).

Similarly, the local-temperature low limit is set by writing the high byte to pointer address 0Ch and writing the low byte to pointer address 17h, or by using a single two-byte write command to pointer address 0Ch. The local-temperature low limit is read by reading the high byte from pointer address 06h and the low byte from pointer address 17h, or by using a two-byte read from pointer address 06h. The power-on-reset value of the local-temperature low-limit register is 00h/00h (0°C in standard temperature mode; –64°C in extended mode).

The remote-temperature high limit is set by writing the high byte to pointer address 0Dh and writing the low byte to pointer address 13h, or by using a two-byte write command to pointer address 0Dh. The remote-temperature high limit is obtained by reading the high byte from pointer address 07h and the low byte from pointer address 13h, or by using a two-byte read command from pointer address 07h. The power-on-reset value of the Remote Temperature High Limit Register is 55h/6Eh/00h (85°C in standard temperature mode for TMP411A-Q1 to TMP411C-Q1; 110°C in standard temperature mode for TMP411D-Q1; 21°C in extended temperature mode).

The remote-temperature low limit is set by writing the high byte to pointer address 0Eh and writing the low byte to pointer address 14h, or by using a two-byte write to pointer address 0Eh. The remote-temperature low limit is read by reading the high byte from pointer address 08h and the low byte from pointer address 14h, or by using a two-byte read from pointer address 08h. The power-on-reset value of the Remote Temperature Low Limit Register is 00h/00h (0°C in standard temperature mode; –64°C in extended mode).

The TMP411-Q1 also has $\overline{\text{THERM}}$ limit registers for both the local and the remote channels. These registers are eight bits and allow for $\overline{\text{THERM}}$ limits set to 1°C resolution. The local-channel $\overline{\text{THERM}}$ limit is set by writing to pointer address 20h. The remote-channel $\overline{\text{THERM}}$ limit is set by writing to pointer address 19h. The local channel $\overline{\text{THERM}}$ limit is obtained by reading from pointer address 20h; the remote channel $\overline{\text{THERM}}$ limit is read by reading from pointer address 19h. The power-on-reset value of the $\overline{\text{THERM}}$ limit registers is 55h/6Eh/00h (85°C in standard temperature mode for TMP411A-Q1 to TMP411C-Q1; 110°C in standard temperature mode for TMP411D-Q1; 21°C in extended temperature mode). The $\overline{\text{THERM}}$ limit comparators also have hysteresis. The hysteresis of both comparators is set by writing to pointer address 21h. The hysteresis value is obtained by reading from pointer address 21h. The value in the Hysteresis Register is an unsigned number (always positive). The power-on-reset value of this register is 0Ah (10°C).


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Whenever changing between standard and extended temperature ranges, be aware that the temperatures stored in the temperature limit registers are not automatically reformatted to correspond to the new temperature range format. These values must be reprogrammed in the appropriate binary or extended binary format.

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## STATUS REGISTER

The TMP411-Q1 has a Status Register to report the state of the temperature comparators. Table 5 shows the Status Register bits. The Status Register is read-only and is read by reading from pointer address 02h.

The BUSY bit reads as 1 if the ADC is making a conversion. It reads as 0 if the ADC is not converting.

The OPEN bit reads as 1 if the remote transistor was detected as open since the last read of the Status Register. The OPEN status is only detected when the ADC is attempting to convert a remote temperature.

The RTHRM bit reads as 1 if the remote temperature has exceeded the remote THERM limit and remains greater than the remote THERM limit less the value in the shared Hysteresis Register; see Figure 18.

The LTHRM bit reads as 1 if the local temperature has exceeded the local THERM limit and remains greater than the local THERM limit less the value in the shared Hysteresis Register; see Figure 18.

The LHIGH and RHIGH bit values depend on the state of the AL/TH bit in the Configuration Register. If the AL/TH bit is 0, the LHIGH bit reads as 1 if the local high limit was exceeded since the last clearing of the Status Register. The RHIGH bit reads as 1 if the remote high limit was exceeded since the last clearing of the Status Register. If the AL/TH bit is 1, the remote high limit and the local high limit are used to implement a THERM2 function. LHIGH reads as 1 if the local temperature has exceeded the local high limit and remains greater than the local high limit less the value in the Hysteresis Register.

The RHIGH bit reads as 1 if the remote temperature has exceeded the remote high limit and remains greater than the remote high limit less the value in the Hysteresis Register. The LLOW and RLOW bits are not affected by the AL/TH bit.

The LLOW bit reads as 1 if the local low limit was exceeded since the last clearing of the Status Register. The RLOW bit reads as 1 if the remote low limit was exceeded since the last clearing of the Status Register.

The values of the LLOW, RLOW, and OPEN (as well as LHIGH and RHIGH when AL/TH is 0) are latched and read as 1 until the Status Register is read or a device reset occurs. These bits are cleared by reading the Status Register, provided that the condition causing the flag to be set no longer exists. The values of BUSY, LTHRM, and RTHRM (as well as LHIGH and RHIGH when ALERT/THERM2 is 1) are not latched and are not cleared by reading the Status Register. They always indicate the current state, and are updated appropriately at the end of the corresponding ADC conversion. Clearing the Status Register bits does not clear the state of the ALERT pin; an SMBus alert response address command must be used to clear the ALERT pin.

The TMP411-Q1 NORs LHIGH, LLOW, RHIGH, RLOW, and OPEN, so a status change for any of these flags from 0 to 1 automatically causes the ALERT pin to go low (only applies when the ALERT/THERM2 pin is configured for ALERT mode).

**Table 5. Status Register Format**

| STATUS REGISTER (Read = 02h, Write = NA) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **BIT #** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| **BIT NAME** | BUSY | LHIGH | LLOW | RHIGH | RLOW | OPEN | RTHRM | LTHRM |
| **POR VALUE** | 0(1) | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

(1) The BUSY bit changes to 1 almost immediately (<<100 µs) following power up, as the TMP411-Q1 begins the first temperature conversion. The BUSY bit is high whenever the TMP411-Q1 is converting a temperature reading.


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## CONFIGURATION REGISTER

The Configuration Register sets the temperature range, controls shutdown mode, and determines how the ALERT/THERM2 pin functions. The Configuration Register is set by writing to pointer address 09h and read by reading from pointer address 03h.

The MASK bit (bit 7) enables or disables the ALERT pin output if AL/TH = 0. If AL/TH = 1, then the MASK bit has no effect. If MASK is set to 0, the ALERT pin goes low when one of the temperature measurement channels exceeds its high or low limits for the chosen number of consecutive conversions. If the MASK bit is set to 1, the TMP411-Q1 retains the ALERT pin status, but the ALERT pin does not go low.

The shutdown (SD) bit (bit 6) enables or disables the temperature measurement circuitry. If SD = 0, the TMP411-Q1 converts continuously at the rate set in the conversion rate register. When SD is set to 1, the TMP411-Q1 immediately stops converting and enters a shutdown mode. When SD is set to 0 again, the TMP411-Q1 resumes continuous conversions. A single conversion can be started when SD = 1 by writing to the One-Shot Register.

The AL/TH bit (bit 5) controls whether the ALERT pin functions in ALERT mode or THERM2 mode. If AL/TH = 0, the ALERT pin operates as an interrupt pin. In this mode, the ALERT pin goes low after the set number of consecutive out-of-limit temperature measurements occurs.

If AL/TH = 1, the ALERT/THERM2 pin implements a THERM function (THERM2). In this mode, THERM2 functions similarly to the THERM pin except that the local high limit and remote high limit registers are used for the thresholds. THERM2 goes low when either RHIGH or LHIGH is set.

The temperature range is set by configuring bit 2 of the Configuration Register. Setting this bit low configures the TMP411-Q1 for the standard measurement range (0°C to 127°C), and temperature conversions are stored in the standard binary format. Setting bit 2 high configures the TMP411-Q1 for the extended measurement range (–55°C to 150°C) temperature conversions are stored in the extended binary format (see Table 1).

The remaining bits of the Configuration Register are reserved and must always be set to 0. The power-on-reset value for this register is 00h. Table 6 summarizes the bits of the Configuration Register.

**NOTE**

The TMP411x-Q1 device family is set to standard temperature range as default. Therefore, the device always needs to be configured to extended temperature range after power-up if this feature is used.

**Table 6. Configuration Register Bit Descriptions**

| CONFIGURATION REGISTER (Read = 03h, Write = 09h, POR = 00h) | | | |
|---|---|---|---|
| **BIT** | **NAME** | **FUNCTION** | **POWER-ON RESET VALUE** |
| 7 | MASK | 0 = ALERT enabled; 1 = ALERT masked | 0 |
| 6 | SD | 0 = Run; 1 = Shut down | 0 |
| 5 | AL/TH | 0 = ALERT mode; 1 = THERM mode | 0 |
| 4, 3 | Reserved | — | 0 |
| 2 | Temperature range | 0 = 0°C to 127°C; 1 = –55°C to 150°C | 0 |
| 1, 0 | Reserved | — | 0 |

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## RESOLUTION REGISTER

The RES1 and RES0 bits (resolution bits 1 and 0) of the Resolution Register set the resolution of the local temperature measurement channel. Remote temperature measurement channel resolution is not affected. Changing the local channel resolution also affects the conversion time and rate of the TMP411-Q1. The Resolution Register is set by writing to pointer address 1Ah and is read by reading from pointer address 1Ah. Table 7 shows the resolution bits for the Resolution Register.

**Table 7. Resolution Register: Local Channel Programmable Resolution**

| RESOLUTION REGISTER (Read = 1Ah, Write = 1Ah, POR = 1Ch) | | | |
|---|---|---|---|
| **RES1** | **RES0** | **RESOLUTION** | **CONVERSION TIME (Typical)** |
| 0 | 0 | 9 bits (0.5°C) | 12.5 ms |
| 0 | 1 | 10 bits (0.25°C) | 25 ms |
| 1 | 0 | 11 bits (0.125°C) | 50 ms |
| 1 | 1 | 12 bits (0.0625°C) | 100 ms |

Bits 2 through 4 of the Resolution Register must always be set to 1. Bits 5 through 7 of the Resolution Register must always be set to 0. The power-on-reset value of this register is 1Ch.

## CONVERSION RATE REGISTER

The Conversion Rate Register controls the rate at which temperature conversions are performed. This register adjusts the idle time between conversions but not the conversion timing itself, thereby allowing the TMP411-Q1 power dissipation to be balanced with the temperature register update rate. Table 8 shows the conversion rate options and corresponding current consumption.

## ONE-SHOT CONVERSION

When the TMP411-Q1 is in shutdown mode (SD = 1 in the Configuration Register), a single conversion on both channels is started by writing any value to the One-Shot Start Register, pointer address 0Fh. This write operation starts one conversion; the TMP411-Q1 returns to shutdown mode when that conversion completes. The value of the data sent in the write command is irrelevant and is not stored by the TMP411-Q1. When the TMP411-Q1 is in shutdown mode, an initial 200 µs is required before a one-shot command can be given. (NOTE: When a shutdown command is issued, the TMP411-Q1 completes the current conversion before shutting down.) This wait time only applies to the 200 µs immediately following shutdown. One-shot commands can be issued without delay thereafter.

**Table 8. Conversion Rate Register**

| CONVERSION RATE REGISTER (Read = 04h, Write = 0Ah, POR = 08h) | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **R7** | **R6** | **R5** | **R4** | **R3** | **R2** | **R1** | **R0** | **CONVERSION/SEC** | **AVERAGE IQ (TYP) (µA)** | |
| | | | | | | | | | **$V_S$ = 2.7V** | **$V_S$ = 5.5V** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.0625 | 11 | 32 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0.125 | 17 | 38 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0.25 | 28 | 49 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0.5 | 47 | 69 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 80 | 103 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 2 | 128 | 155 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 4 | 190 | 220 |
| 07h to 0Fh | | | | | | | | 8 | 373 | 413 |


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## N-FACTOR CORRECTION REGISTER

The TMP411-Q1 allows for a different *n*-factor value to be used for converting remote-channel measurements to temperature. The remote channel uses sequential current excitation to extract a differential $V_{BE}$ voltage measurement to determine the temperature of the remote transistor. Equation 1 relates this voltage and temperature.

$$V_{BE2} - V_{BE1} = \frac{nkT}{q} \ln\left(\frac{I_2}{I_1}\right) \quad (1)$$

The value *n* in Equation 1 is a characteristic of the particular transistor used for the remote channel. The default value for the TMP411-Q1 is *n* = 1.008. The value in the N-Factor Correction Register may be used to adjust the effective n-factor according to Equation 2 and Equation 3.

$$n_{eff} = \frac{1.008 \cdot 300}{(300 - N_{ADJUST})} \quad (2)$$

$$N_{ADJUST} = 300 - \left(\frac{300 \cdot 1.008}{n_{eff}}\right) \quad (3)$$

The *n*-correction value must be stored in twos-complement format, yielding an effective data range from −128 to 127, as shown in Table 9. The n-correction value may be written to and read from pointer address 18h. The register power-on-reset value is 00h, thus having no effect unless written to.

**Table 9. N-Factor Range**

| $N_{ADJUST}$ | | | N |
|---|---|---|---|
| BINARY | HEX | DECIMAL | |
| 0111 1111 | 7F | 127 | 1.747977 |
| 0000 1010 | 0A | 10 | 1.042759 |
| 0000 1000 | 08 | 8 | 1.035616 |
| 0000 0110 | 06 | 6 | 1.028571 |
| 0000 0100 | 04 | 4 | 1.021622 |
| 0000 0010 | 02 | 2 | 1.014765 |
| 0000 0001 | 01 | 1 | 1.011371 |
| 0000 0000 | 00 | 0 | 1.008 |
| 1111 1111 | FF | −1 | 1.004651 |
| 1111 1110 | FE | −2 | 1.001325 |
| 1111 1100 | FC | −4 | 0.994737 |
| 1111 1010 | FA | −6 | 0.988235 |
| 1111 1000 | F8 | −8 | 0.981818 |
| 1111 0110 | F6 | −10 | 0.975484 |
| 1000 0000 | 80 | −128 | 0.706542 |

## MINIMUM AND MAXIMUM REGISTERS

The TMP411-Q1 stores the minimum and maximum temperature measured since power on, chip reset, or minimum and maximum register reset for both the local and remote channels. The Local Temperature Minimum Register may be read by reading the high byte from pointer address 30h and the low byte from pointer address 31h. The Local Temperature Minimum Register may also be read by using a two-byte read command from pointer address 30h. The Local Temperature Minimum Register is reset at power on, by executing the chip-reset command, or by writing any value to any of pointer addresses 30h through 37h. The reset value for these registers is FFh/F0h.

The Local Temperature Maximum Register may be read by reading the high byte from pointer address 32h and the low byte from pointer address 33h. The Local Temperature Maximum Register may also be read by using a two-byte read command from pointer address 32h. The Local Temperature Maximum Register is reset at power on by executing the chip reset command, or by writing any value to any of pointer addresses 30h through 37h. The reset value for these registers is 00h/00h.

The Remote Temperature Minimum Register may be read by reading the high byte from pointer address 34h and the low byte from pointer address 35h. The Remote Temperature Minimum Register may also be read by using a two-byte read command from pointer address 34h. The Remote Temperature Minimum Register is reset at power on by executing the chip reset command, or by writing any value to any of pointer addresses 30h through 37h. The reset value for these registers is FFh/F0h.

The Remote Temperature Maximum Register may be read by reading the high byte from pointer address 36h and the low byte from pointer address 37h. The Remote Temperature Maximum Register may also be read by using a two-byte read command from pointer address 36h. The Remote Temperature Maximum Register is reset at power on by executing the chip reset command, or by writing any value to any of pointer addresses 30h through 37h. The reset value for these registers is 00h/00h.

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## SOFTWARE RESET

The TMP411-Q1 may be reset by writing any value to Pointer Register FCh. This restores the power-on-reset state to all of the TMP411-Q1 registers as well as aborting any conversion in process and clearing the ALERT and THERM pins.

The TMP411-Q1 also supports reset via the two-wire general call address (00000000). The TMP411-Q1 acknowledges the general call address and responds to the second byte. If the second byte is 00000110, the TMP411-Q1 executes a software reset. The TMP411-Q1 takes no action in response to other values in the second byte.

## CONSECUTIVE ALERT REGISTER

The value in the Consecutive Alert Register (address 22h) determines how many consecutive out-of-limit measurements must occur on a measurement channel before the ALERT signal is activated. The value in this register does not affect bits in the Status Register. Values of one, two, three, or four consecutive conversions can be selected; one conversion is the default. This function allows additional filtering for the ALERT pin. The consecutive alert bits are shown in Table 10.

**Table 10. Consecutive Alert Register**

| CONSECUTIVE ALERT REGISTER (READ = 22h, WRITE = 22h, POR = 01h) | | | NUMBER OF CONSECUTIVE OUT-OF-LIMIT MEASUREMENTS |
|---|---|---|---|
| C2 | C1 | C0 | |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 1 | 1 | 4 |

**NOTE**

Bit 7 of the Consecutive Alert Register controls the enable/disable of the timeout function. See the Timeout Function section for a description of this feature.

## THERM HYSTERESIS REGISTER

The THERM Hysteresis Register, shown in Table 12, stores the hysteresis value used for the THERM pin alarm function. This register must be programmed with a value that is less than the Local Temperature High Limit Register value, Remote Temperature High Limit Register value, Local THERM Limit Register value, or Remote THERM Limit Register value; otherwise, the respective temperature comparator does not trip on the measured temperature falling edges. Allowable hysteresis values are shown in Table 11. The default hysteresis value is 10°C, whether the device is operating in the standard or extended mode setting.

**Table 11. Allowable THERM Hysteresis Val**

| TEMPERATURE (°C) | THERM HYSTERESIS VALUE | |
|---|---|---|
| | TH[11:4] (STANDARD BINARY) | (HEX) |
| 0 | 0000 0000 | 00 |
| 1 | 0000 0001 | 01 |
| 5 | 0000 0101 | 05 |
| 10 | 0000 1010 | 0A |
| 25 | 0001 1001 | 19 |
| 50 | 0011 0010 | 32 |
| 75 | 0100 1011 | 4B |
| 100 | 0110 0100 | 64 |
| 125 | 0111 1101 | 7D |
| 127 | 0111 1111 | 7F |
| 150 | 1001 0110 | 96 |
| 175 | 1010 1111 | AF |
| 200 | 1100 1000 | C8 |
| 225 | 1110 0001 | E1 |


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**Table 11. Allowable THERM Hysteresis Val (continued)**

| TEMPERATURE (°C) | THERM HYSTERESIS VALUE | |
|---|---|---|
| | TH[11:4] (STANDARD BINARY) | (HEX) |
| 255 | 1111 1111 | FF |

## BUS OVERVIEW

The TMP411-Q1 is SMBus interface-compatible. In SMBus protocol, the device that initiates the transfer is called a master, and the devices controlled by the master are slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated. START is indicated by pulling the data line (SDA) from a high to low logic level while SCL is high. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge bit. During data transfer, SDA must remain stable while SCL is high, because any change in SDA while SCL is high is interpreted as a control signal.

Once all data has been transferred, the master generates a STOP condition. STOP is indicated by pulling SDA from low to high while SCL is high.

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## SERIAL INTERFACE

The TMP411-Q1 operates only as a slave device on either the two-wire bus or the SMBus. Connections to either bus are made via the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP411-Q1 supports the transmission protocol for fast (1-kHz to 400-kHz) and high-speed (1-kHz to 3.4-MHz) modes. All data bytes are transmitted MSB-first.

## SERIAL BUS ADDRESS

To communicate with the TMP411-Q1, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing a read or write operation. The address of the TMP411A-Q1 and TMP411D-Q1 is 4Ch (1001 100b).

## READ/WRITE OPERATIONS

Accessing a particular register on the TMP411-Q1 is accomplished by writing the appropriate value to the Pointer Register. The value for the Pointer Register is the first byte transferred after the slave address byte with the R/W bit low. Every write operation to the TMP411-Q1 requires a value for the Pointer Register (see Figure 14).

When reading from the TMP411-Q1, the last value stored in the Pointer Register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the Pointer Register. This transaction is accomplished by issuing a slave address byte with the R/W bit low, followed by the Pointer Register byte. No additional data are required. The master can then generate a START condition and send the slave address byte with the R/W bit high to initiate the read command. See Figure 15 for details of this sequence. If repeated reads from the same register are desired, it is not necessary to continually send the Pointer Register bytes, because the TMP411-Q1 retains the Pointer Register value until it is changed by the next write operation. Note that register bytes are sent MSB-first, followed by the LSB.

**Table 12. THERM Hysteresis Register Format**

| THERM HYSTERESIS REGISTER (Read = 21h, Write = 21h, POR = 0Ah) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **BIT #** | **D7D7** | **D6D6** | **D5D5** | **D4D4** | **D3D3** | **D2D2** | **D1D1** | **D0D0** |
| **BIT NAME** | TH11 | TH10 | TH9 | TH8 | TH7 | TH6 | TH5 | TH4 |
| **POR VALUE** | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |


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## TIMING DIAGRAMS

The TMP411-Q1 is two-wire and SMBus-compatible. Figure 13 to Figure 17 describe the various operations on the TMP411-Q1. Bus definitions are given as follows. Parameters for Figure 13 are defined in Table 13.

**Bus Idle:** Both SDA and SCL lines remain high.

**Start Data Transfer:** A change in the state of the SDA line, from high to low, while the SCL line is high, defines a START condition. Each data transfer is initiated with a START condition.

**Stop Data Transfer:** A change in the state of the SDA line from low to high while the SCL line is high defines a STOP condition. Each data transfer terminates with a STOP or a repeated START condition.

**Data Transfer:** The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

**Acknowledge:** Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, data transfer termination can be signaled by the master generating a Not-Acknowledge on the last byte that has been transmitted by the slave.

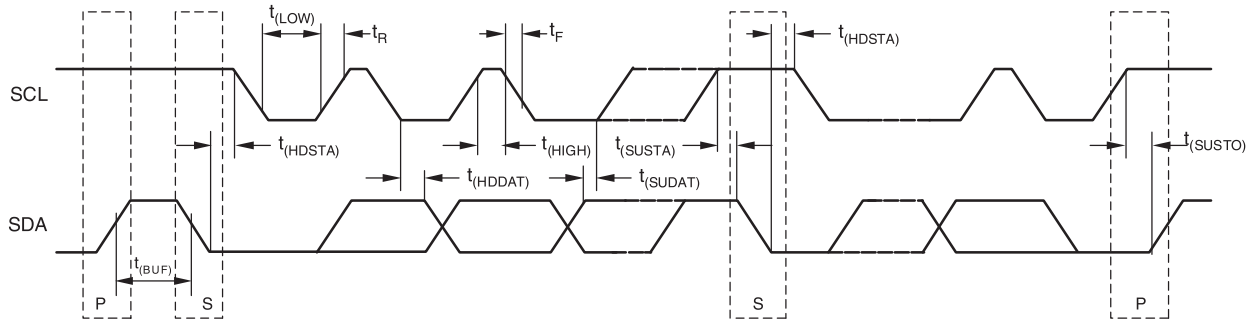


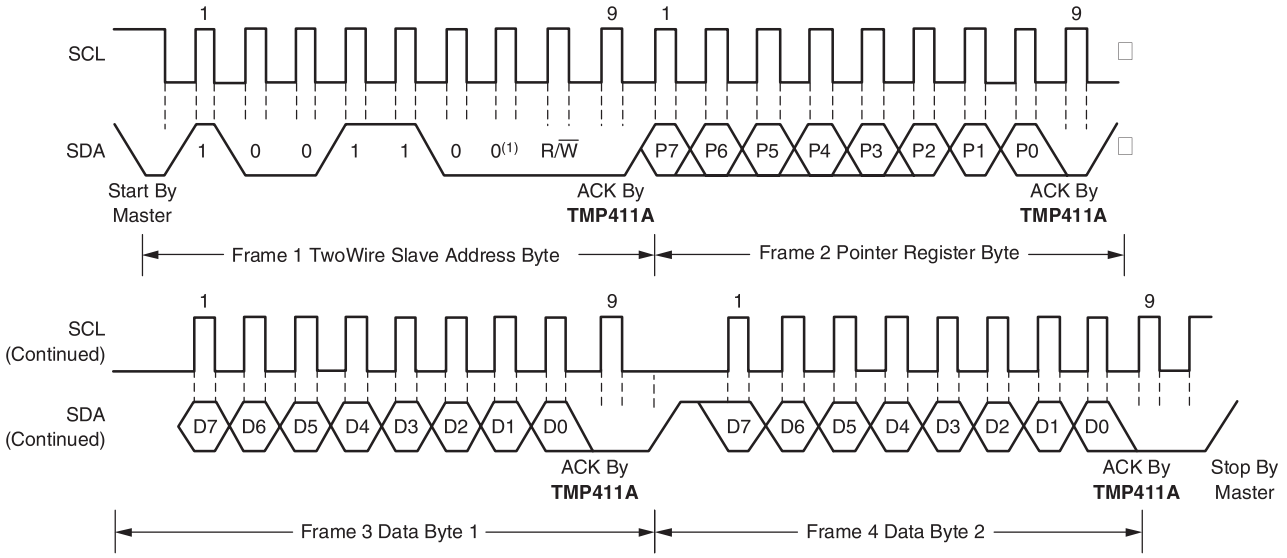

**Figure 13. Two-Wire Timing Diagram**

**Table 13. Timing Diagram Definitions for Figure 13**

| PARAMETER | | FAST MODE | | HIGH-SPEED MODE | | UNITS |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $f_{(SCL)}$ | SCL operating frequency | 0.001 | 0.4 | 0.001 | 3.4 | MHz |
| $t_{(BUF)}$ | Bus free time between STOP and START conditions | 600 | | 160 | | ns |
| $t_{(HDSTA)}$ | Hold time after repeated START condition. After this period, the first clock is generated. | 100 | | 100 | | ns |
| $t_{(SUSTA)}$ | Repeated START condition setup time | 100 | | 100 | | ns |
| $t_{(SUSTO)}$ | STOP condition setup time | 100 | | 100 | | ns |
| $t_{(HDDAT)}$ | Data hold time | 0(1) | | 0(2) | | ns |
| $t_{(SUDAT)}$ | Data setup time | 100 | | 10 | | ns |
| $t_{(LOW)}$ | SCL clock LOW period | 1300 | | 160 | | ns |
| $t_{(HIGH)}$ | SCL clock HIGH period | 600 | | 60 | | ns |
| $t_f$ | Clock and data fall time | | 300 | | 160 | ns |
| $t_r$ | Clock and data rise time | | 300 | | 160 | ns |
| $t_r$ | for SCLK ≤ 100 kHz | | 1000 | | | ns |

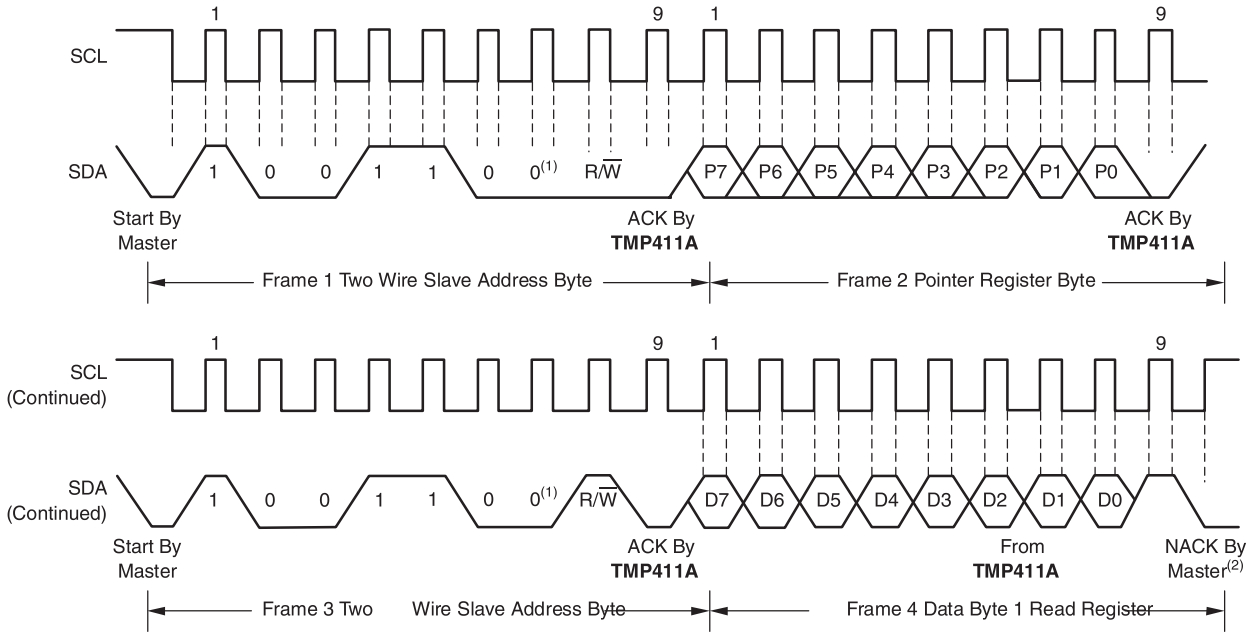
(1) For cases with fall time of SCL less than 20 ns and/or the rise time or fall time of SDA less than 20 ns, the hold time should be greater than 20 ns.
(2) For cases with fall time of SCL less than 10 ns and/or the rise or fall time of SDA less than 10 ns, the hold time should be greater than 10 ns.

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A. Slave address 1001 100 (TMP411A and TMP411D) shown. Slave address changes for TMP411B and TMP411C. See Ordering Information table for more details.

**Figure 14. Two-Wire Timing Diagram for Write Word Format**

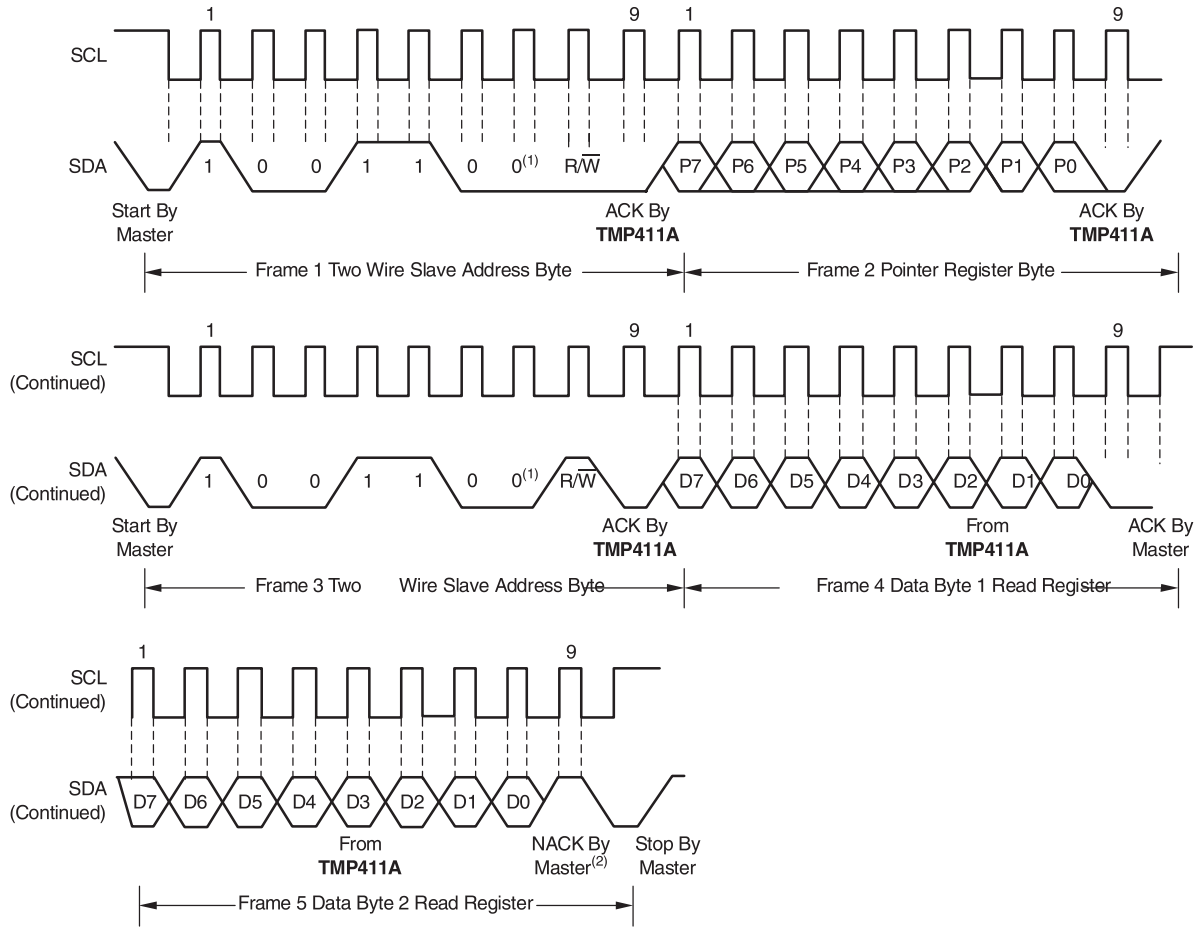



(1) Slave address 1001 100 (TMP411A and TMP411D) shown

(2) Master should leave SDA high to terminate a single-byte read operation.

**Figure 15. Two-Wire Timing Diagram for Single-Byte Read Format**

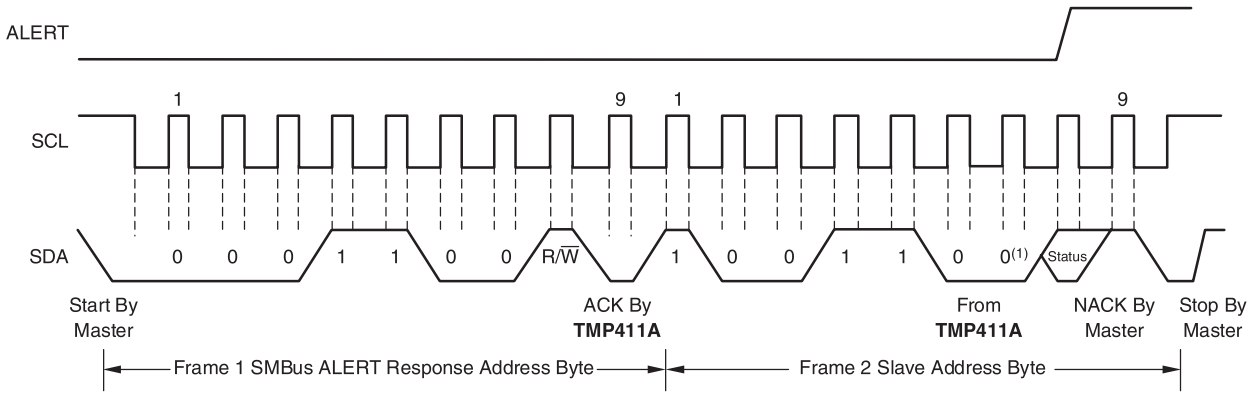

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(1) Slave address 1001 100 (TMP411A and TMP411D) shown

(2) Master should leave SDA high to terminate a two−byte read operation.

**Figure 16. Two-Wire Timing Diagram for Two-Byte Read Format**




(1) Slave address 1001 100 (TMP411A) shown

**Figure 17. Timing Diagram for SMBus $\overline{\text{ALERT}}$**

### HIGH-SPEED MODE

For the two-wire bus to operate at frequencies above 400 kHz, the master device must issue a high-speed mode (Hs-mode) master code (00001XXX) as the first byte after a START condition to switch the bus to high-speed operation. The TMP411-Q1 does not acknowledge this byte, but switches the input filters on SDA and SCL and the output filter on SDA to operate in Hs-mode, allowing transfers at up to 3.4 MHz. After the Hs-mode master code has been issued, the master transmits a two-wire slave address to initiate a data transfer operation. The bus continues to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP411-Q1 switches the input and output filters back to fast-mode operation.

### TIME-OUT FUNCTION

When bit 7 of the Consecutive Alert Register is set high, the TMP411-Q1 time-out function is enabled. The TMP411-Q1 resets the serial interface if either SCL or SDA is held low for 30 ms (typical) between a START and STOP condition. If the TMP411-Q1 is holding the bus low, it releases the bus and waits for a START condition. To avoid activating the time-out function, it is necessary to maintain a communication speed of at least 1 kHz for the SCL operating frequency. The default state of the time-out function is enabled (bit 7 = high).

### $\overline{\text{THERM}}$ (PIN 4) AND $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ (PIN 6)

The TMP411-Q1 has two pins dedicated to alarm functions, the $\overline{\text{THERM}}$ and $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pins. Both pins are open-drain outputs that each require a pullup resistor to V+. These pins can be wire-ORed together with other alarm pins for system monitoring of multiple sensors. The $\overline{\text{THERM}}$ pin provides a thermal interrupt that cannot be software-disabled. The $\overline{\text{ALERT}}$ pin is intended for use as an earlier warning interrupt, and can be software disabled, or masked. The $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin can also be configured for use as $\overline{\text{THERM2}}$, a second $\overline{\text{THERM}}$ pin (Configuration Register: AL/TH bit = 1). The default setting configures pin 6 to function as $\overline{\text{ALERT}}$ (AL/TH = 0).

The $\overline{\text{THERM}}$ pin asserts low when either the measured local or remote temperature is outside of the temperature range programmed in the corresponding Local or Remote THERM Limit Register. The THERM temperature limit range can be programmed with a wider range than that of the limit registers, which allows $\overline{\text{ALERT}}$ to provide an earlier warning than $\overline{\text{THERM}}$. The $\overline{\text{THERM}}$ alarm resets automatically when the measured temperature returns to within the THERM temperature limit range minus the hysteresis value stored in the THERM Hysteresis Register. The allowable values of hysteresis are shown in Table 11. The default hysteresis is 10°C. When the $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin is configured as a second thermal alarm (Configuration Register: bit 7 = 0, bit 5 = 1), it functions the same as $\overline{\text{THERM}}$, but uses the temperatures stored in the Local/Remote Temperature High/Low Limit Registers to set its comparison range.

When $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ (pin 6) is configured as $\overline{\text{ALERT}}$ (Configuration Register: bit 7 = 0, bit 5 = 0), the pin asserts low when either the measured local or remote temperature violates the range limit set by the corresponding Local/Remote Temperature High/Low Limit Registers. This alert function can be configured to assert only if the range is violated a specified number of consecutive times (1, 2, 3, or 4). The consecutive violation limit is set in the Consecutive Alert Register. False alerts that occur as a result of environmental noise can be prevented by requiring consecutive faults. $\overline{\text{ALERT}}$ also asserts low if the remote temperature sensor is open-circuit. When the MASK function is enabled (Configuration Register: bit 7 = 1), $\overline{\text{ALERT}}$ is disabled (that is, masked). $\overline{\text{ALERT}}$ resets when the master reads the device address, as long as the condition that caused the alert no longer persists, and the Status Register has been reset.


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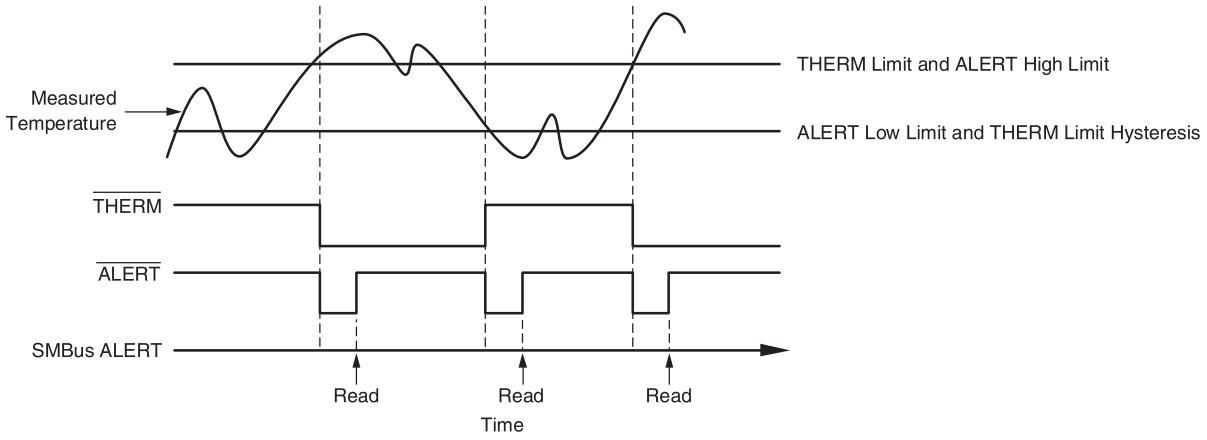



**Figure 18. SMBus Alert Timing Diagram**

## SMBUS ALERT FUNCTION

The TMP411-Q1 supports the SMBus alert function. When pin 6 is configured as an alert output, the ALERT pin of the TMP411-Q1 may be connected as an SMBus alert signal. When a master detects an alert condition on the ALERT line, the master sends an SMBus alert command (0001 1001) on the bus. If the ALERT pin of the TMP411-Q1 is active, the device acknowledges the SMBus alert command and responds by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates whether the temperature exceeding one of the temperature high limit settings or falling below one of the temperature low limit settings caused the alert condition. This bit will is if the temperature is greater than or equal to one of the temperature high-limit settings; this bit is low if the temperature is less than one of the temperature low-limit settings. See Figure 17 for details of this sequence.

If multiple devices on the bus respond to the SMBus alert command, arbitration during the slave address portion of the SMBus alert command determines which device clears its alert status. If the TMP411-Q1 wins the arbitration, its ALERT pin becomes inactive at the completion of the SMBus alert command. If the TMP411-Q1 loses the arbitration, the ALERT pin remains active.

## SHUTDOWN MODE (SD)

The TMP411-Q1 shutdown mode allows the user to save maximum power by shutting down all device circuitry other than the serial interface, reducing current consumption to typically less than 3 μA; see typical characteristic curve Shutdown Quiescent Current vs Supply Voltage. Shutdown mode is enabled when the SD bit of the Configuration Register is high; the device shuts down once the current conversion is completed. When SD is low, the device maintains a continuous conversion state.

## SENSOR FAULT

The TMP411-Q1 senses a fault at the D+ input resulting from incorrect diode connection or an open circuit. The detection circuitry consists of a voltage comparator that trips when the voltage at D+ exceeds (V+) − 0.6 V (typical). The comparator output is continuously checked during a conversion. If a fault is detected, the last valid measured temperature is used for the temperature measurement result, the OPEN bit (Status Register, bit 2) is set high, and, if the alert function is enabled, ALERT asserts low.

When not using the remote sensor with the TMP411-Q1, the D+ and D− inputs must be connected together to prevent meaningless fault warnings.

## UNDERVOLTAGE LOCKOUT

The TMP411-Q1 senses when the power-supply voltage has reached a minimum voltage level for the ADC converter to function. The detection circuitry consists of a voltage comparator that enables the ADC converter after the power supply (V+) exceeds 2.45 V (typical). The comparator output is continuously checked during a conversion. The TMP411-Q1 does not perform a temperature conversion if the power-supply output is not adequate. The last valid measured temperature is used for the temperature measurement result.

## GENERAL-CALL RESET

The TMP411-Q1 supports reset via the two-wire general-call address 00h (0000 0000b). The TMP411-Q1 acknowledges the general-call address and responds to the second byte. If the second byte is 06h (0000 0110b), the TMP411-Q1 executes a software reset. This software reset restores the power-on-reset state to all TMP411-Q1 registers, aborts any conversion in progress, and clears the ALERT and THERM pins. The TMP411-Q1 takes no action in response to other values in the second byte.

## IDENTIFICATION REGISTERS

The TMP411-Q1 allows for the two-wire bus controller to query the device for manufacturer and device IDs. This feature allows for software identification of the device at the particular two-wire bus address. The manufacturer ID is obtained by reading from pointer address FEh. The TMP411-Q1 manufacturer code is 55h. The device ID depends on the specific model; see the Register Map (Table 4). These registers are read-only.

## FILTERING

Remote junction temperature sensors are usually implemented in a noisy environment. Noise is most often created by fast digital signals, and it can corrupt measurements. The TMP411-Q1 has a built-in 65-kHz filter on the inputs of D+ and D− to minimize the effects of noise. However, a bypass capacitor placed differentially across the inputs of the remote temperature sensor is recommended to make the application more robust against unwanted coupled signals. The value of the capacitor should be between 100 pF and 1 nF. Some applications attain better overall accuracy with additional series resistance; however, this increased accuracy is setup-specific. When series resistance is added, the value should not be greater than 3 kΩ.

If filtering is needed, the suggested component values are 100 pF and 50 Ω on each input. Exact values are application-specific.


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## REMOTE SENSING

The TMP411-Q1 is designed to be used with either discrete transistors or substrate transistors built into processor chips and ASICs. Either NPN or PNP transistors can be used, as long as the base-emitter junction is used as the remote temperature sense. Either a transistor or diode connection can also be used; see Figure 11.

Errors in remote temperature-sensor readings are the consequence of the ideality factor and current excitation used by the TMP411-Q1 versus the manufacturer-specified operating current for a given transistor. Some manufacturers specify a high-level and low-level current for the temperature-sensing substrate transistors. The TMP411-Q1 uses 6 μA for $I_{LOW}$ and 120 μA for $I_{HIGH}$. The TMP411-Q1 allows for different n-factor values; see the N-Factor Correction Register section.

The ideality factor (n) is a measured characteristic of a remote temperature sensor diode as compared to an ideal diode. The ideality factor for the TMP411-Q1 is trimmed to be 1.008. For transistors whose ideality factor does not match the TMP411-Q1, Equation 4 can be used to calculate the temperature error. Note that for the equation to be used correctly, actual temperature (°C) must be converted to Kelvin (K).

$$T_{ERR} = \left(\frac{n - 1.008}{1.008}\right) \times (273.15 + T(°C)) \quad (4)$$

where:

- $n$ = Ideality factor of remote temperature sensor
- T(°C) = actual temperature
- $T_{ERR}$ = Error in TMP411-Q1 reading due to $n \neq 1.008$
- Degree delta is the same for °C and °K

For $n$ = 1.004 and T(°C) = 100°C:

$$T_{ERR} = \left(\frac{1.004 - 1.008}{1.008}\right) \times (273.15 + 100°C)$$

$$T_{ERR} = -1.48°C \quad (5)$$

If a discrete transistor is used as the remote temperature sensor with the TMP411-Q1, the best accuracy can be achieved by selecting the transistor according to the following criteria:

1. Base-emitter voltage > 0.25 V at 6 μA, at the highest sensed temperature.
2. Base-emitter voltage < 0.95 V at 120 μA, at the lowest sensed temperature.
3. Base resistance < 100 Ω.
4. Tight control of $V_{BE}$ characteristics indicated by small variations in $h_{FE}$ (that is, 50 to 150).

Based on these criteria, two recommended small-signal transistors are the 2N3904 (NPN) or 2N3906 (PNP).

## MEASUREMENT ACCURACY AND THERMAL CONSIDERATIONS

The temperature measurement accuracy of the TMP411-Q1 depends on the remote and/or local temperature sensor being at the same temperature as the system point being monitored. Clearly, if the temperature sensor is not in good thermal contact with the part of the system being monitored, then there is a delay in the response of the sensor to a temperature change in the system. For remote temperature sensing applications using a substrate transistor (or a small, SOT23 transistor) placed close to the device being monitored, this delay is usually not a concern.

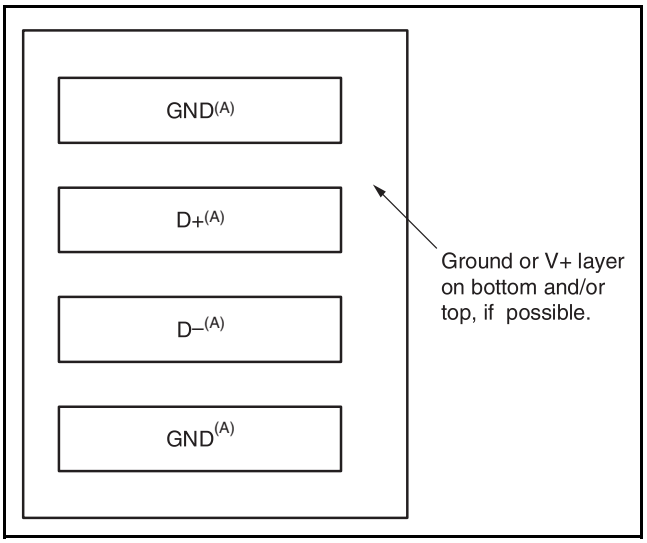
The local temperature sensor inside the TMP411-Q1 monitors the ambient air around the device. The thermal time constant for the TMP411-Q1 is approximately two seconds. This constant implies that if the ambient air changes quickly by 100°C, it would take the TMP411-Q1 about 10 seconds (that is, five thermal time constants) to settle to within 1°C of the final value. In most applications, the TMP411-Q1 package is in electrical and therefore thermal contact with the printed circuit board (PCB), as well as subjected to forced airflow. The accuracy of the measured temperature directly depends on how accurately the PCB and forced airflow temperatures represent the temperature that the TMP411-Q1 is measuring. Additionally, the internal power dissipation of the TMP411-Q1 can cause the temperature to rise above the ambient or PCB temperature. The internal power dissipated as a result of exciting the remote temperature sensor is negligible because of the small currents used. For a 5.5-V supply and maximum conversion rate of eight conversions per second, the TMP411-Q1 dissipates 1.82 mW ($PD_{IQ}$ = 5.5 V × 330 μA). If both the $\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$ and $\overline{\text{THERM}}$ pins are each sinking 1 mA, an additional power of 0.8 mW is dissipated ($PD_{OUT}$ = 1 mA × 0.4 V + 1 mA × 0.4 V = 0.8 mW). Total power dissipation is then 2.62 mW ($PD_{IQ}$ + $PD_{OUT}$) and, with a $\theta_{JA}$ of 150°C/W, causes the junction temperature to rise approximately 0.393°C above the ambient.

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## LAYOUT CONSIDERATIONS

Remote temperature sensing on the TMP411-Q1 measures very small voltages using very low currents; therefore, noise at the IC inputs must be minimized. Most applications using the TMP411-Q1 have high digital content, with several clocks and logic-level transitions creating a noisy environment. Layout should adhere to the following guidelines:

1. Place the TMP411-Q1 as close to the remote junction sensor as possible.
2. Route the D+ and D− traces next to each other and shield them from adjacent signals through the use of ground guard traces, as shown in Figure 19. If a multilayer PCB is used, bury these traces between ground or VDD planes to shield them from extrinsic noise sources. Five-mil (0.127-mm) PCB traces are recommended.
3. Minimize additional thermocouple junctions caused by copper-to-solder connections. If these junctions are used, make the same number and approximate locations of copper-to-solder connections in both the D+ and D− connections to cancel any thermocouple effects.
4. Use a 0.1-µF local bypass capacitor directly between the V+ and GND of the TMP411-Q1, as shown in Figure 20. Minimize filter capacitance between D+ and D− to 1000 pF or less for optimum measurement performance. This capacitance includes any cable capacitance between the remote temperature sensor and TMP411-Q1.
5. If the connection between the remote temperature sensor and the TMP411-Q1 is less than 8 inches (20 cm), use a twisted-wire pair connection. Beyond 8 inches (20 cm), use a twisted, shielded pair with the shield grounded as close to the TMP411-Q1 as possible. Leave the remote sensor connection end of the shield wire open to avoid ground loops and 60-Hz pickup.




A. 5-mil (0.127-mm) traces with 5-mil (0.127-mm) spacing

**Figure 19. Example Signal Traces**

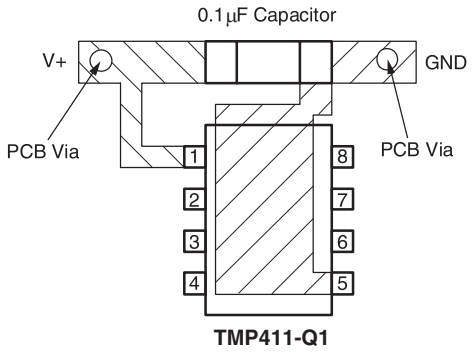



**Figure 20. Suggested Bypass Capacitor Placement**


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## REVISION HISTORY

The following table summarizes the revisions of the TMP411-Q1 Data Sheet.

Note: numbering may vary from previous versions.

**Table 14. Revision History**

| Revision | Literature Number | Date | Notes |
|---|---|---|---|
| * | SBOS527 | December, 2010 | See (1) |
| A | SBOS527A | March, 2012 | See (2) |
| B | SBOS527B | August, 2012 | See (3) |
| C | SBOS527C | September, 2012 | See (4) |
| D | SBOS527D | October, 2012 | See (5) |

(1) TMP411-Q1 Data Sheet, (SBOS527) – initial release.
(2) TMP411-Q1 Data Sheet, (SBOS527A):
  (a) Removed all existing Applications, and added automotive.
  (b) Changed the Ordering Information Table. Removed Preview devices TMP411xQDRQ1, and added device TMP411DQDGKRQ1
(3) TMP411-Q1 Data Sheet, (SBOS527B):
  (a) Added table note to Ordering Information Table, and added default to the Local Temperature High Limit column header.
  (b) Added another column to Table 4: Power-on Reset (HEX) for D.
(4) TMP411-Q1 Data Sheet, (SBOS527C):
  (a) Removed part of sentence from Description: "wide remote temperature measurement range (up to 150°C)".
  (b) Changed extended Default Local Temperature High Limit to standard, and removed extended table note and package columns in the Ordering Information Table.
  (c) Removed the last two sentences in the first paragraph in the Temperature Measurement Data section; also added "which is referred to as standard temperature mode."
  (d) Removed paragraph after "Likewise, temperatures above 127°C result in a value of 127 (7Fh)." in the Temperature Measurement Data section.
  (e) Removed Extended Binary columns from Table 2 and first paragraph beginning with "Note:" underneath the table.
  (f) Removed "AND EXTENDED" from columns in Table 3.
  (g) Added the sentence "Please note read pointer address 0x05, 0x07, 0x19, and 0x20 have different power-on-reset values for A, B, C vs D" before last sentence in the Pointer Register section.
  (h) Added space in between One and Shot in Figure 12 so it reads One Shot Register instead of OneShot Register.
  (i) Changed last sentence of first, and third paragraph, and the sixth sentence of the last paragraph in the Limit Registers section to: "The power-on-reset value of the local-temperature high limit is 55h for TMP411A-Q1 and 6Eh for TMP411D-Q1 (85°C for TMP411A-Q1 and 110°C for TMP411D-Q1)"
  (j) Removed "–64°C in extended mode" from the second and fourth paragraphs in the Limit Registers section.
  (k) Removed last paragraph in the Limit Registers section.
  (l) Replaced last sentence of sixth paragraph in the Configuration Register section with "This bit is set to 0 by default and cannot be changed."
  (m) Removed: 1 = −55°C to 150°C from temperature range row in Table 6.
  (n) Added "and TMP411D-Q1" to the second to last sentence in the Serial Bus Address section; removed last sentence.
  (o) Updated layout of Consecutive Alert Register and Therm Hysteresis Register sections to make them easier to read.
  (p) Fixed ALERT active low for $I_{OH}$ in Electrical Characteristics table.
  (q) Changed second to last sentence in the sixth paragraph of the Configuration Register section from: Setting this bit low configures the TMP411-Q1 for the standard measurement range (0°C to 127°C); temperature conversions are stored in the standard binary format, to: Setting this bit low configures the TMP411-Q1 for the standard measurement range (0°C to 127°C), and temperature conversions are stored in the standard binary format.
  (r) Removed ", whether the device is operating in the standard or extended mode setting." from the last sentence in the Therm Hysteresis Register section.
(5) TMP411-Q1 Data Sheet, (SBOS527D):
  (a) Added Default Local High Temperature Limit and Default Remote High Temperature Limit columns to the Ordering Information table; changed last column header from Default Local Temperature High Limit to Default Temperature Range.

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**Table 14. Revision History (continued)**

| Revision | Literature Number | Date | Notes |
|---|---|---|---|
| E | SBOS527E | November, 2012 | See(6) |

(6) TMP411-Q1 Data Sheet, (SBOS527E):
- (a) Added "wide remote temperature measurement range (up to 150°C)" back into the Description section.
- (b) Removed ", which is referred to as standard temperature mode" in first paragraph of Temperature Measurement Data section.
- (c) Added last two sentences of first paragraph back in to Temperature Measurement Data section.
- (d) Added paragraph after "Likewise, temperatures above 127°C result in a value of 127 (7Fh)." back into Temperature Measurement Data section.
- (e) Added Extended Binary columns back into Table 2.
- (f) Added note after Table 2.
- (g) Added "AND EXTENDED" back in to the STANDARD BINARY column headers in Table 3.
- (h) Replaced last sentence of first paragraph in Limit Registers section with: The power-on-reset value of the local temperature high limit is 55h/6Eh/00h (85°C in standard temperature mode for TMP411A-Q1 to TMP411C-Q1; 110°C in standard temperature mode for TMP411D-Q1, 21°C in extended temperature range).
- (i) Added –64°C in extended mode back in to second and fourth paragraphs in Limit Registers section.
- (j) Replaced last sentence of fourth paragraph in Limit Registers section with: The power-on-reset value of the Remote Temperature High Limit Register is 55h/6Eh/00h (85°C in standard temperature mode for TMP411A-Q1 to TMP411C-Q1; 110°C in standard temperature mode for TMP411D-Q1; 21°C in extended temperature mode).
- (k) Replaced sentence in fifth paragraph of Limit Registers section with: The power-on-reset value of the $\overline{\text{THERM}}$ limit registers is 55h/6Eh/00h (85°C in standard temperature mode for TMP411A-Q1 to TMP411C-Q1; 110°C in standard temperature mode for TMP411D-Q1; 21°C in extended temperature mode).
- (l) Added last paragraph back into the Limit Registers section.
- (m) Replaced this sentence: This bit is set to 0 by default and cannot be changed, with this sentence: Setting bit 2 high configures the TMP411-Q1 for the extended measurement range (–55°C to 150°C) temperature conversions are stored in the extended binary format (see Table 1) in the Configuration Register section.
- (n) Added note to Configuration Register section.
- (o) Added 1 = –55°C to 150°C back to temperature range row in Table 6.
- (p) Added "whether the device is operating in the standard or extended mode setting" to last sentence in Therm Hysteresis Register section.


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**Table 14. Revision History (continued)**

| Revision | Literature Number | Date | Notes |
|---|---|---|---|
| F | SBOS527F | November, 2013 | See (7) |

(7) TMP411-Q1 Data Sheet, (SBOS527F):
(a) Changed device CDM ESD Classification Level from C3B to C4B in FEATURES list item and in the ABSOLUTE MAXIMUM RATINGS table.
(b) Deleted $T_A$ and Top-Side Marking columns from Table 1.
(c) Changed package throughout document from MSOP to VSSOP.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TMP411AQDGKRQ1 | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAUAG | Level-3-260C-168 HR | | 411AQ | Samples |
| TMP411BQDGKRQ1 | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 411BQ | Samples |
| TMP411CQDGKRQ1 | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 411CQ | Samples |
| TMP411DQDGKRQ1 | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | 411DQ | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TMP411-Q1 :**

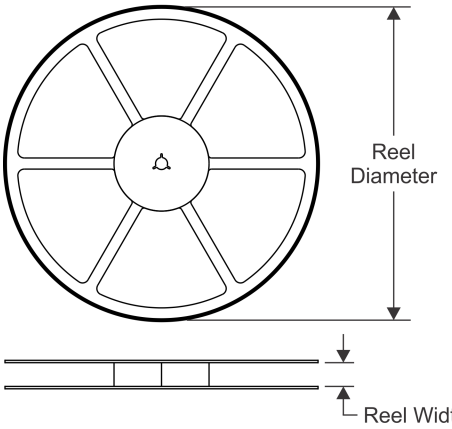
- Catalog: TMP411

NOTE: Qualified Version Definitions:

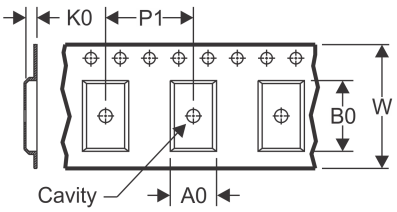
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

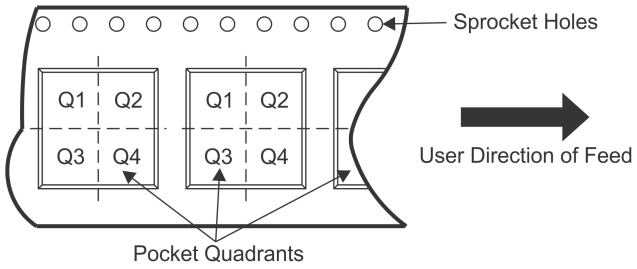



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

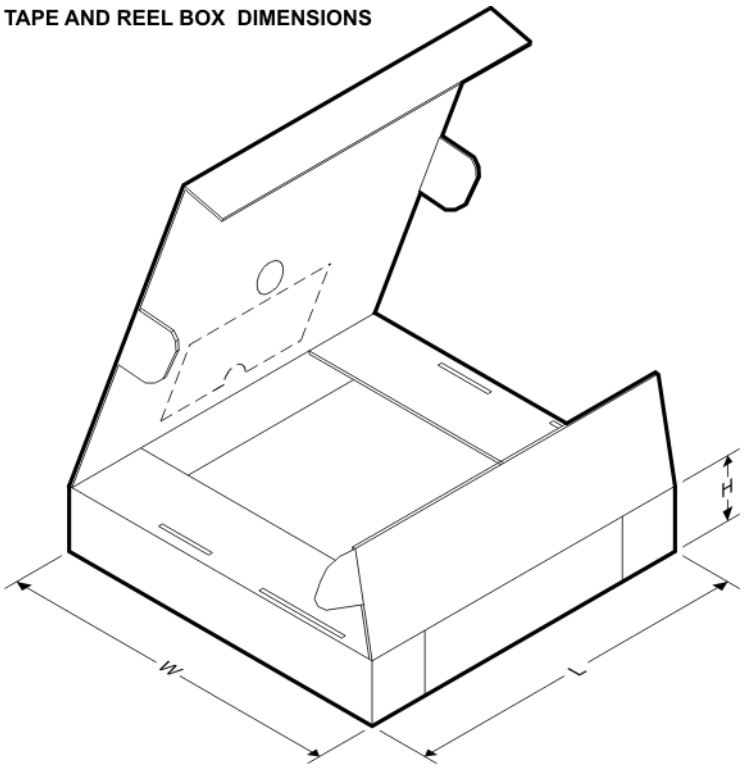
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TMP411AQDGKRQ1 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.3 | 1.3 | 8.0 | 12.0 | Q1 |
| TMP411BQDGKRQ1 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TMP411CQDGKRQ1 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TMP411DQDGKRQ1 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.3 | 1.3 | 8.0 | 12.0 | Q1 |

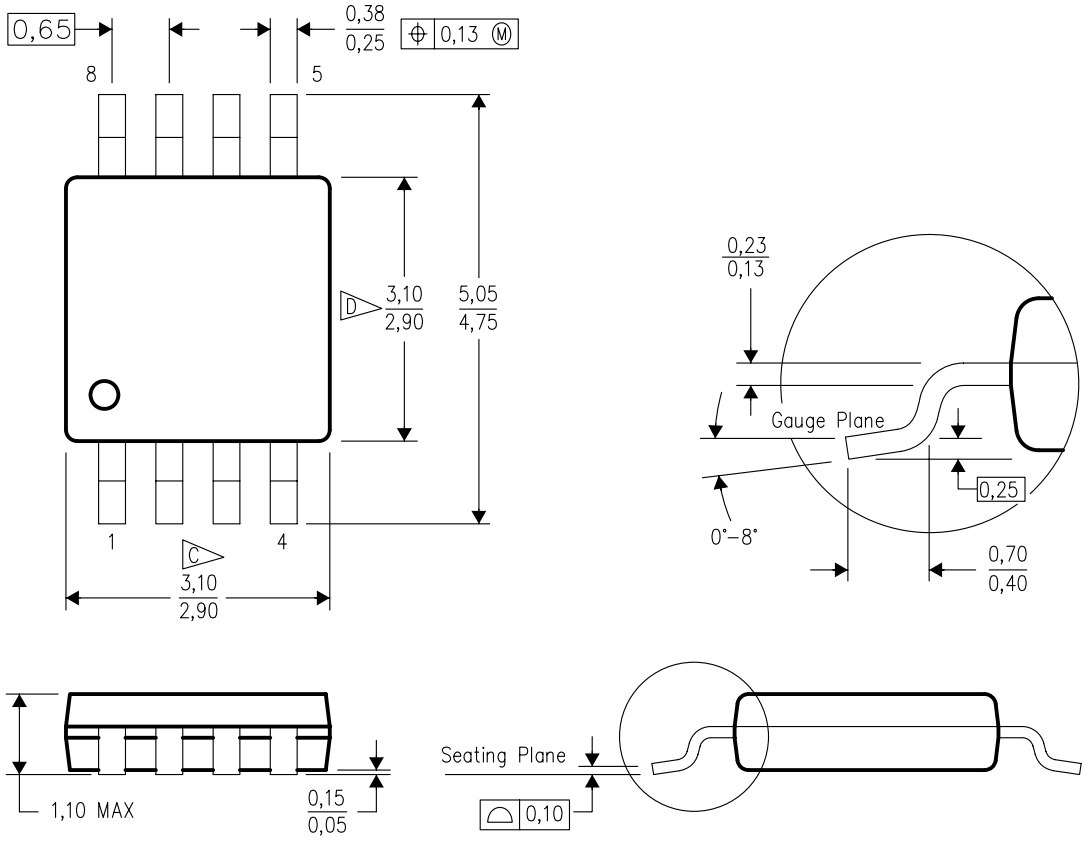
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TMP411AQDGKRQ1 | VSSOP | DGK | 8 | 2500 | 367.0 | 367.0 | 38.0 |
| TMP411BQDGKRQ1 | VSSOP | DGK | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| TMP411CQDGKRQ1 | VSSOP | DGK | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| TMP411DQDGKRQ1 | VSSOP | DGK | 8 | 2500 | 367.0 | 367.0 | 38.0 |

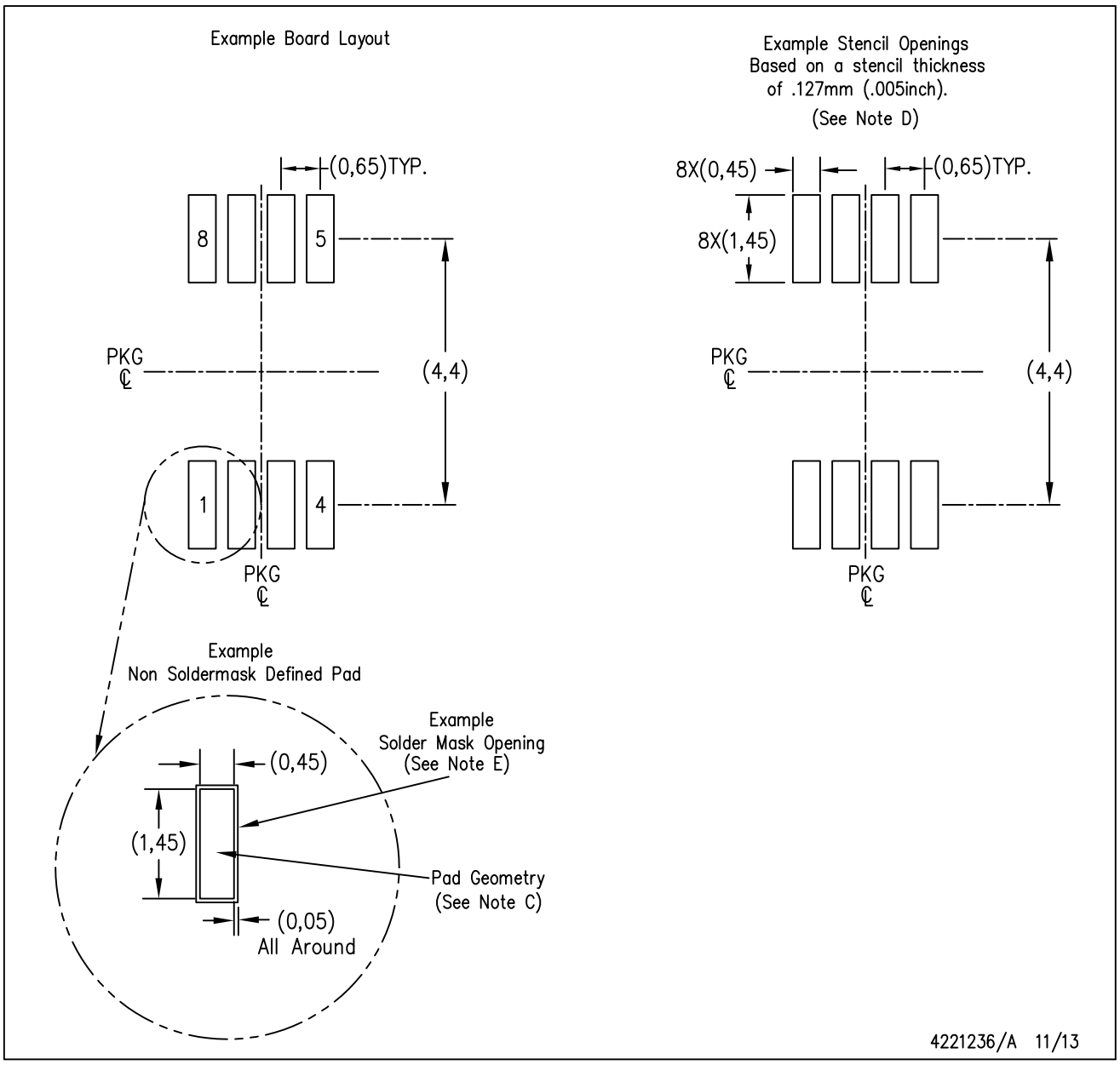
## DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

# DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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